# T7 Datasheet

*Smart Automotive Processor*

**Revision 1.1**

**Jul. 30, 2018**

# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | May.11, 2018 | Initial release version. |
| 1.1 | Jul.30, 2018 | **Chapter 5 Electrical Characteristics**<br>1. Update LPDDR3 electrical parameters in Section 5.11.1.2.<br>2. Update SMHC electrical parameters in Section 5.11.3. |

  

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# Contents



# Figures



# Tables



# About This Document

## Purpose

The document describes features of each module, pin/signal characteristics, current consumption, the interface timing, thermal and package of the T7 processor. For details about register descriptions of each module, see the ***Allwinner T7 User Manual***.

## Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

## Conventions

### Symbol Conventions

The symbols that may be found in this document are defined as follows.

| Symbol | Description |
|---|---|
|  **WARNING** | A warning means that injury or death is possible if the instructions are not obeyed. |
|  **CAUTION** | A caution means that damage to equipment is possible. |
|  **NOTE** | Provides additional information to emphasize or supplement important points of the main text. |

### Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

| Symbol | Description |
|---|---|
| - | The cell is blank. |

### Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

| Type | Symbol | Value |
|---|---|---|
| Data capacity | 1K | 1024 |
| | 1M | 1,048,576 |
| | 1G | 1,073,741,824 |
| Frequency, data rate | 1k | 1000 |
| | 1M | 1,000,000 |
| | 1G | 1,000,000,000 |

# 1. Overview

The T7 processor represents Allwinner's latest achievement in smart automotive processors. The processor is ideal for applications that require 3D graphics, advanced video processing, rich user interfaces, lower power consumption and higher system integration. It will bring the advanced consumer electronics experiences into the vehicles of the future, and achieve a good balance of high performance, drive safety, drive video record and device connectivity.

The T7 processor has some very exciting features:

- **CPU**: T7 is based on Hexa-core Cortex™-A7 CPU architecture with 1024KB L2 cache.
- **CPUS**: CPUS is a heterogeneous processor independent of ARM. It is mainly used for standby management, including power management, IO control, peripheral status monitoring and so on. And it is low power consumption.
- **GPU**: T7 adopts the extensively implemented and technically mature Mali400 MP4. It is applied to identify the real-time traffic, and provides possibilities for automatic drive.
- **Video Engine**: High-definition H.265 decoder is up to 1080p@60fps and H.265 encoder is up to 1080p@60fps.
- **Camera**: Supports 2 individual parallel CSI interfaces, 4-channel TVIN and 2 individual MIPI-CSI, which can easily finish multi-channel video recording.
- **EVE**: Integrated Embedded Visual Engine(EVE) can detect vehicle, lane, pedestrian, traffic sign, and traffic signals. Detection speed is up to 30fps for VGA images.
- **ISP**: T7 equips two 4M ISP with advanced features like better 2D/3D de-noise, contrast enhancement, AE/AF/AWB statistics, color correction, gamma correction, sharpening, and anti-flick detection statistics, etc.
- **Display**: Content can be displayed on 4-lane MIPI DSI displays, or RGB panel, or LVDS panel.TV-out interface for TV encoder is also supported.
- **Audio**: Integrated analog audio codec supports 2-ch high-quality stereo playback DAC, one stereo line-out output, and one differential phone-out output; 3-ch high-quality stereo recording ADC, three differential microphone inputs, and one stereo line-in input. Digital audio interfaces support I2S/PCM for connecting to an external audio codec, OWA for connecting to external amplifier, and DMIC for digital audio recording.
- **Memory**: Supports external memory interfaces to NAND Flash, SD/eMMC, Nor Flash and SDRAM port. SDRAM port can be configured to support DDR3, DDR3L, LPDDR2, LPDDR3.
- **Peripherals**: To reduce total system cost, T7 has a broad range of hardware peripherals to meet the flexible peripheral configuration requirements such as UART, SPI, CIR_RX, USB2.0 OTG, USB2.0_HOST, TWI, etc.
- **Reliability:** Pass the AEC-Q100 Grade3 Certification test.

# 2. Features

## 2.1. CPU Architecture

- Hexa-core ARM Cortex™-A7 Processor
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- Large Physical Address Extensions(LPAE)
- 32KB L1 Instruction cache and 32KB L1 Data cache for per CPU
- 1024KB L2 cache shared

## 2.2. GPU Architecture

- Mali400 MP4, up to 400MHz
- Embedded four pixel processors capable of processing 1600M pix/sec
- Built-in MMU for each processor and L2 cache with 128KB size
- Supports OpenGL ES1.1/2.0 and OpenVG1.1 3D graphics standard

## 2.3. Internal Memory

### 2.3.1. Boot ROM

- Supports eMMC, SD card, Nand flash, SPI Nor flash and SPI Nand flash
- Supports mandatory upgrade process through SMHC0 and USB
- Supports normal Boot and secure Boot
- Boot select pin(FEL) is used to select boot process: jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process
- Supports super standby wakeup process
- Supports Pin Boot select
- Supports eFuse Boot select

## 2.4. External Memory Interfaces

### 2.4.1. SDRAM

- Compatible with JEDEC standard DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- DDR3/DDR3L interface with the maximum frequency of 800MHz
- LPDDR3 interface with the maximum frequency of 672MHz
- LPDDR2 interface with the maximum frequency of 533MHz
- Up to 3GB memory capacity
- 32-bit data bus width
- Supports Memory Dynamic Frequency Scale(MDFS)

### 2.4.2. NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 2 ready_busy signals
- Supports SLC/MLC/TLC flash and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

### 2.4.3. SMHC

- Up to four SMHC controllers(SDC0,SDC1,SDC2,SDC3)
- Compatible with eMMC standard specification V5.0, SD physical layer specification V2.0 ,SDIO card specification V3.0
- 1-/4-/8-bit bus width, only SDC2 supports up to 8-bit,shared with NAND flash pins
- Embedded special DMA to do data transfer
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

## 2.5. Video and Graphic

### 2.5.1. Video Decoder

- Supports video decoding up to 1080p@60fps
- Supports multi-formats:
  - H.265 MP/L4.1: 1080p@60fps
  - H.264 BP/MP/HP Level4.2: 1080p@45fps
  - H.263 BP: 1080p@45fps
  - MPEG4 SP/ASP L5: 1080p@45fps
  - MPEG2 MP/HL: 1080p@45fps
  - MPEG1 MP/HL: 1080p@45fps
  - xvid: 1080p@45fps
  - Sorenson Spark: 1080p@45fps
  - VP8: 1080p@45fps
  - AVS/AVS+: 1080p@45fps
  - WMV9/VC1: 1080p@30fps
  - JPEG: 16384 x 16384@45Mbps

### 2.5.2. Video Encoder

- Supports H.265 MP video encoding up to 1080p@60fps
- Supports H.264 MP video encoding up to 1080p@60fps
- Supports input formats: titled(128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Supports Alpha blending
- Supports Thumb generation
- Supports 4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

### 2.5.3. Display Engine(DE)

- Output size up to 2048x2048
- Four alpha blending channels for main display, two channels for aux display
- Four overlay layers in each channel, and has a independent scaler

- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports write back for high efficient dual display and miracast

### 2.5.4. De-interlacer

- Off-line processing mode
- Supports NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined data format
- Input video resolution from 32 x 32 to 2048 x 2048 pixel
- Supports weave/pixel-motion-adaptive de-interlacer method
- Noise reduction function

### 2.5.5. G2D

- Layer size up to 2048 x 2048 pixels
- Horizontal and vertical flip, clockwise 0/90/180/270 degree rotate
- Multiple formats convert function
- Alpha blending, Window clip, BitBlit, and MaskBlit

## 2.6. Embedded Visual Engine(EVE)

- Detection speed: 30fps for VGA images (working frequency: 300MHz)
- Supports classic HAAR and LBP feature, total feature up to 4000 and 1000 respectively
- Supports 4K input and built-in zoom, extract ROI
- Supports 4 channel integral Image, processes 130 million features per second
- Supports up to 3 channel feature calculation
- The minimum resolution of target object in single image detection is 20 x 20

## 2.7. Video Output Interfaces

### 2.7.1. MIPI DSI

- Supports 4 lanes MIPI DSI up to 1920 x 1200@60fps
- 1/2/3/4 data lanes configuration and up to 1Gbit/s per lane
- Supports video mode with sync pulse/sync event, burst mode/command mode
- Pixel format: RGB888, RGB666, RGB666 packed, and RGB565

### 2.7.2. LVDS

- Supports LVDS interface up to 1920 x 1200@60fps
- Dual link LVDS mode output ,up to 1920 x 1200@60fps
- Single link LVDS mode output ,up to 1366 x 768@60fps
- Multiplex pin with RGB interface

### 2.7.3. RGB

- Supports 18-bit RGB interface

- Up to 1366 x 768@60fps
- Supports BT656 output
- Supports RGB666 and RGB565 with dither function

### 2.7.4. TVOUT

- Supports 1-ch TV CVBS output
- Supports NTSC and PAL mode
- Plug status auto detecting

## 2.8. ISP

- Supports 2 individual image signal processor(ISP)
- Adjustable 3A functions, including automatic exposure(AE), automatic white balance(AWB) and automatic focus (AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D/3D denoising
- Sensor build-in WDR, 2F-line base WDR, local tone mapping
- 1/64 to 1x scaling output for 4 channels
- Graphics mirror and flip
- ISP tuning tools for the PC
- Maximum frame rate of 30fps for the 1920 x 2688 resolution

## 2.9. Video Input Interfaces

### 2.9.1. Parallel CSI

- Two individual parallel CSI interfaces, with 16-bit data wide per interface
- Supports 8-,10-,12-,16-bit digital camera(DC) interface
- Supports DDR sample mode
- Supports CCIR656 protocol for NTSC and PAL
- Supports ITU-R BT.656/BT.1120 time-multiplexed format
- Supports 16-bit interface with separate syncs
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution to 1080p@30fps
- Maximum pixel clock for parallel to 148.5MHz

### 2.9.2. MIPI CSI

- Two individual MIPI CSI camera control interfaces
- Supports MIPI-DPHY v1.0 and MIPI-CSI2 v1.0
- Supports virtual channel
- Supports formats: YUV422-8bit/10bit, YUV420-8bit/10bit, RAW-8, RAW-10, RAW-12, RGB888, RGB565
- 1/2/3/4 data lanes configuration and up to 1Gbit/s per lane
- Maximum video capture resolution up to 8M@30fps

### 2.9.3. TVIN

- 4 channel CVBS input or 1 channel YPbPr with 1 channel CVBS
- Supports YPbPr input, 576p/480p/576i/480i
- Supports CVBS input, NTSC and PAL mode
- Supports YUV422, YUV420 format writeback

- One channel 3D comb filter
- Detection for signal locked and 625 lines
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

## 2.10. Audio Interfaces

### 2.10.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
  - Up to 100±2dB SNR during DAC playback
  - Supports DAC sample rate from 8 kHz to 192 kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Three audio analog-to-digital(ADC) channels
  - Up to 92±2dB SNR during ADC recording
  - Supports ADC sample rate from 8 kHz to 48 kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Two audio analog outputs:
  - One stereo line-out output (LINEOUTL and LINEOUTR)
  - One differential phone-out output (PHONEOUTP and PHONEOUTN)
- Four audio inputs:
  - Three differential microphone inputs (MICIN1P and MICIN1N,MICIN2P and MICIN2N, MICIN3P and MICIN3N)
  - One stereo line-in input (LINEINL and LINEINR)
- Supports analog/digital volume control
- One low-noise analog microphone bias output
- Supports dynamic range controller adjusting the DAC playback and ADC recording

### 2.10.2. I2S/PCM

- Up to three I2S/PCM interfaces
- Compliant with standard Philips Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master and slave mode configured
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 kHz to 192 kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- Supports programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)

### 2.10.3. One Wire Audio(OWA)

- IEC-60958 transmitter and receiver functionality
- Compatible with S/PDIF protocol
- Supports channel status insertion for the transmitter
- Supports channel status capture on the receiver
- Hardware parity generation on the transmitter
- Hardware parity checking on the receiver

### 2.10.4. DMIC

- Supports up to 8 channels
- Supports sample rate from 8 kHz to 48 kHz

## 2.11. Security Engine

- Encryption and decryption algorithms implemented by using hardware, including AES,DES and 3DES
- Signature and verification algorithms implemented by using hardware, including RSA512,RSA1024,RSA2048
- HASH tamper proofing algorithms implemented by using hardware, including SHA1,SHA256,SHA384,SHA512, HMAC_SHA1 and HMAC_SHA256
- True hardware random number(TRNG) generator and pseudo hardware random number(PRNG) generator
- Integrated 2.5 Kbits efuse storage space

# 2.12. External Peripherals

### 2.12.1. USB

- One USB 2.0 OTG(USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) and Low-Speed(LS,1.5 Mbit/s) in host mode
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) in device mode
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 10 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
  - Supports (8KB+64Bytes) FIFO for EPs(including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- Three USB 2.0 Host(USB1,USB2,USB3), with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) and Low-Speed(LS,1.5 Mbit/s) device
- One USB HSIC, share USB3 controller with one USB 2.0 analog PHY

### 2.12.2. EMAC

- Compliant with IEEE 802.3-2002 standard
- Supports 10/100/1000 Mbit/s data transfer rates
- Supports MII/RMII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 Kbytes
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 Kbytes of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 Kbytes TXFIFO for transmission packets and 16 Kbytes RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

### 2.12.3. TWI

- Up to 10 TWIs(7 in CPU domain, 3 in CPUS domain)
- Software-programmable for Slave or Master
- Supports Repeated START signal

- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Supports speeds up to 400 kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

### 2.12.4. UART

- Up to 10 UART controllers(5 in CPU domain, 5 in CPUS domain)
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 5 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

### 2.12.5. SPI

- Full-duplex synchronous serial interface
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports mode0, mode1, mode2 and mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 0 bit to 32 bits
- Supports the SPI NAND flash and SPI NOR flash
- Supports standard SPI, dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI

### 2.12.6. CIR_RX

- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

### 2.12.7. LRADC

- One LRADC controller with 2 input channels
- 6-bit resolution
- Sample rate up to 250Hz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Voltage input range between 0 to 2.0V
- Power supply voltage:3.0V, reference voltage:2.0V

### 2.12.8. GPADC

- One general purpose ADC(GPADC) controller with 6 input channels
- 12-bit resolution

- 8-bit effective SAR type A/D converter
- Power supply voltage: 3.0V
- Analog input range: 0 V to 3.0 V
- Maximum sampling frequency: 1 MHz
- Supports data compare and interrupt
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

### 2.12.9. PWM

- 8 PWM channels(4 PWM pairs)
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0 ~ 24MHz/100MHz
- Various duty-cycle: 0% ~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

### 2.12.10. TSC

- Supports SPI/SSI interface, interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Supports multiple transport stream packet (188, 192, 204) format
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

### 2.12.11. SCR

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

### 2.12.12. RSB™

- Designed and implemented by the Allwinner Technology
- Up to 20MHz speed with ultra low power
- Supports push-pull bus
- Supports host mode and multi-devices
- Programmable output delay of CD signal
- Supports parity check for address and data transmission

## 2.13. Package

- PBGA 547 balls, 0.8mm ball pitch, 21mm x 21mm

# 3. Block Diagram

Figure 3-1 shows the block diagram of the T7 processor.

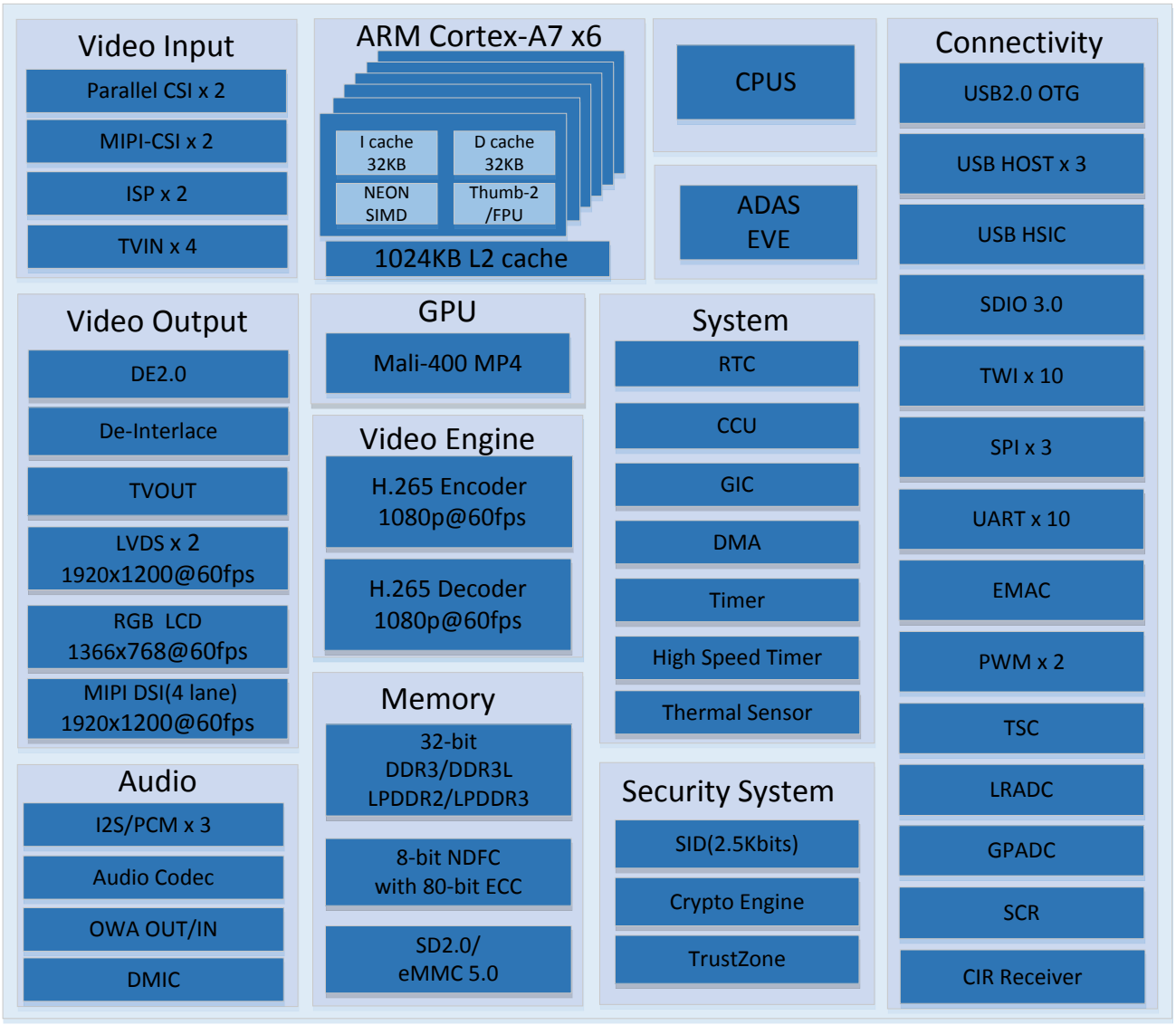



**Figure 3-1. T7 Block Diagram**

The typical application diagram is shown in Figure 3-2.

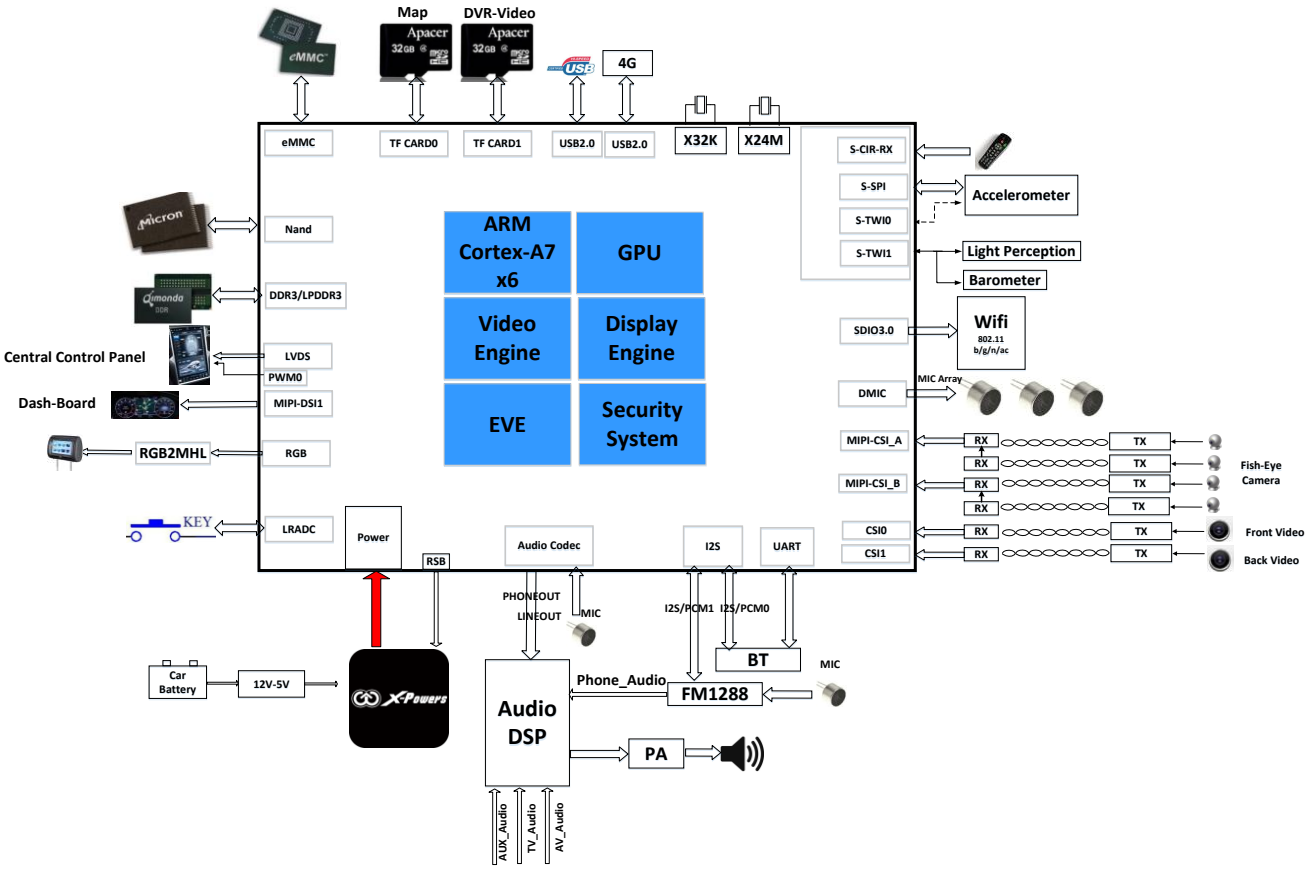



**Figure 3-2. T7 Application Diagram**

# 4. Pin Description

## 4.1. Pin Quantity

Table 4-1 lists the pin quantity of the T7.

**Table 4-1. Pin Quantity**

| Pin Type | Quantity |
|---|---|
| I/O | 332 |
| Power | 65 |
| Ground | 142 |
| DDR Power | 8 |
| Total | 547 |

## 4.2. Pin Characteristics

Table 4-2 lists the characteristics of T7 pins from the following ten aspects.

**[1]**. **Ball#** : Package ball numbers associated with each signals.

**[2]**.**Pin Name** : The name of the package pin.

**[3]**.**Signal Name** : The signal name for that pin in the mode being used.

**[4]**.**Function** : Multiplexing function number.

**[5]**.**Ball Reset Rel. Function** : The function is automatically configured after RESET from low to high.

**[6]**.**Type** : Denotes the signal direction

I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
A I/O (Analog Input/Output),
P (Power),
G (Ground)

**[7]**.**Ball Reset State** : The state of the terminal at reset.

**[8]**.**Pull Up/Down** : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

**[9]**.**Buffer Strength** : Defines drive strength of the associated output buffer.

**[10]**.**Power Supply** : The voltage supply for the terminal's IO buffers.

Table 4-2. Pin Characteristics

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| **DRAM**[(3)(4)] | | | | | | | | | |
| AB13 | SA0[(6)] | SA0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AB16 | SA1[(6)] | SA1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA15 | SA2[(6)] | SA2 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W16 | SA3[(6)] | SA3 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y13 | SA4[(6)] | SA4 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AB7 | SA5[(6)] | SA5 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y7 | SA6[(6)] | SA6 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W6 | SA7[(6)] | SA7 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA6 | SA8[(6)] | SA8 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AB4 | SA9[(6)] | SA9 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W13 | SA10[(6)] | SA10 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA12 | SA11[(6)] | SA11 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W12 | SA12[(6)] | SA12 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y5 | SA13[(6)] | SA13 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AB12 | SA14[(6)] | SA14 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W15 | SA15[(6)] | SA15 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AE13 | SDQ0 | SDQ0 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC12 | SDQ1 | SDQ1 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE12 | SDQ2 | SDQ2 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD12 | SDQ3 | SDQ3 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC10 | SDQ4 | SDQ4 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD10 | SDQ5 | SDQ5 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE10 | SDQ6 | SDQ6 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC9 | SDQ7 | SDQ7 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD18 | SDQ8 | SDQ8 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC17 | SDQ9 | SDQ9 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD17 | SDQ10 | SDQ10 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC16 | SDQ11 | SDQ11 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD15 | SDQ12 | SDQ12 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC15 | SDQ13 | SDQ13 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD14 | SDQ14 | SDQ14 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC14 | SDQ15 | SDQ15 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD7 | SDQ16 | SDQ16 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE7 | SDQ17 | SDQ17 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE6 | SDQ18 | SDQ18 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC6 | SDQ19 | SDQ19 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC5 | SDQ20 | SDQ20 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE4 | SDQ21 | SDQ21 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD4 | SDQ22 | SDQ22 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC4 | SDQ23 | SDQ23 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD3 | SDQ24 | SDQ24 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD2 | SDQ25 | SDQ25 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC3 | SDQ26 | SDQ26 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC2 | SDQ27 | SDQ27 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AB3 | SDQ28 | SDQ28 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AB2 | SDQ29 | SDQ29 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AA3 | SDQ30 | SDQ30 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AA2 | SDQ31 | SDQ31 | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD13 | SDQM0 | SDQM0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AC18 | SDQM1 | SDQM1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AD8 | SDQM2 | SDQM2 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AE3 | SDQM3 | SDQM3 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AD11 | SDQS0P[(5)] | SDQS0P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE15 | SDQS1P[(5)] | SDQS1P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD5 | SDQS2P[(5)] | SDQS2P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AB1 | SDQS3P[(5)] | SDQS3P | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC11 | SDQS0N[(5)] | SDQS0N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AE16 | SDQS1N[(5)] | SDQS1N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AD6 | SDQS2N[(5)] | SDQS2N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |
| AC1 | SDQS3N[(5)] | SDQS3N | NA | NA | I/O | Z | NA | NA | VCC-DRAM |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| AB6 | SBA0 | SBA0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y15 | SBA1 | SBA1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W7 | SBA2 | SBA2 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AE9 | SCKP(5) | SCKP | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AE8 | SCKN(5) | SCKN | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y10 | SCKE0 | SCKE0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA9 | SCKE1 | SCKE1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y4 | SWE | SWE | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA5 | SCAS | SCAS | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y6 | SRAS | SRAS | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W9 | SCS0 | SCS0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA10 | SCS1 | SCS1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| Y9 | SODT0 | SODT0 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AB10 | SODT1 | SODT1 | NA | NA | O | Z | NA | NA | VCC-DRAM |
| W4 | SRST(7) | SRST | NA | NA | O | Z | NA | NA | VCC-DRAM |
| AA16 | SZQ(8) | SZQ | NA | NA | AI | Z | NA | NA | VCC-DRAM |
| Y1 | SVREF(9) | SVREF | NA | NA | P | Z | NA | NA | VCC-DRAM |
| V8,V9,V10, V11,V13,V14, V15 | VCC-DRAM | VCC-DRAM | NA | NA | P | NA | NA | NA | NA |
| **GPIOB**(16) | | | | | | | | | |
| W1 | PB0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART2_TX | 2 | | O | | | | |
| | | PCM2_BCLK | 3 | | I/O | | | | |
| | | JTAG_MS0 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W2 | PB1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART2_RX | 2 | | I | | | | |
| | | PCM2_DOUT | 3 | | O | | | | |
| | | JTAG_CK0 | 4 | | I | | | | |
| | | SIM_PWREN | 5 | | O | | | | |
| | | PB_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W3 | PB2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART2_RTS | 2 | | O | | | | |
| | | PCM2_DIN | 3 | | I | | | | |
| | | JTAG_DO0 | 4 | | O | | | | |
| | | SIM_VPPEN | 5 | | O | | | | |
| | | PB_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V6 | PB3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART2_CTS | 2 | | I | | | | |
| | | I2S0_MCLK | 3 | | O | | | | |
| | | JTAG_DI0 | 4 | | I | | | | |
| | | SIM_VPPPP | 5 | | O | | | | |
| | | PB_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V5 | PB4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | CPUBIST0 | 2 | | O | | | | |
| | | PCM0_SYNC | 3 | | I/O | | | | |
| | | UART4_RTS | 4 | | O | | | | |
| | | SIM_CLK | 5 | | O | | | | |
| | | PB_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V4 | PB5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | CPUBIST1 | 2 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | PCM0_BCLK | 3 | | I/O | | | | |
| | | UART4_CTS | 4 | | I | | | | |
| | | SIM_DATA | 5 | | I/O | | | | |
| | | PB_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T5 | PB6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | CPUBIST2 | 2 | | O | | | | |
| | | PCM0_DOUT | 3 | | O | | | | |
| | | UART4_TX | 4 | | O | | | | |
| | | SIM_RST | 5 | | O | | | | |
| | | PB_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T6 | PB7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | CPUBIST3 | 2 | | O | | | | |
| | | PCM0_DIN | 3 | | I | | | | |
| | | UART4_RX | 4 | | I | | | | |
| | | SIM_DET | 5 | | I | | | | |
| | | PB_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T4 | PB8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | PCM2_SYNC | 3 | | I/O | | | | |
| | | UART0_TX | 4 | | O | | | | |
| | | TWI2_SCK | 5 | | I/O,OD | | | | |
| | | PB_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T3 | PB9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | I2S2_MCLK | 3 | | O | | | | |
| | | UART0_RX | 4 | | I | | | | |
| | | TWI2_SDA | 5 | | I/O,OD | | | | |
| | | PB_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOC**[16] | | | | | | | | | |
| B12 | PC0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_WE | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | SPI0_CLK[12] | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C11 | PC1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_ALE | 2 | | O | | | | |
| | | SDC2_DS[13] | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D9 | PC2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_CLE | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | SPI0_MOSI | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C13 | PC3 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | NAND_CE0 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | SPI0_MISO | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B11 | PC4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_RE | 2 | | O | | | | |
| | | SDC2_CLK(15) | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C12 | PC5 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_RB0 | 2 | | I | | | | |
| | | SDC2_CMD(14) | 3 | | I/O,OD | | | | |
| | | SPI0_CS(10) | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C10 | PC6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ0 | 2 | | I/O | | | | |
| | | SDC2_D0 | 3 | | I/O | | | | |
| | | SPI0_HOLD(11) | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C9 | PC7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ1 | 2 | | I/O | | | | |
| | | SDC2_D1 | 3 | | I/O | | | | |
| | | SPI0_WP | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A8 | PC8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ2 | 2 | | I/O | | | | |
| | | SDC2_D2 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A10 | PC9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ3 | 2 | | I/O | | | | |
| | | SDC2_D3 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B10 | PC10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ4 | 2 | | I/O | | | | |
| | | SDC2_D4 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| B9 | PC11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ5 | 2 | | I/O | | | | |
| | | SDC2_D5 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B8 | PC12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ6 | 2 | | I/O | | | | |
| | | SDC2_D6 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C8 | PC13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQ7 | 2 | | I/O | | | | |
| | | SDC2_D7 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A11 | PC14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_DQS | 2 | | I/O | | | | |
| | | SDC2_RST | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D7 | PC15 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_CE1 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B7 | PC16 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-PC |
| | | Output | 1 | | O | | | | |
| | | NAND_RB1 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| H10 | VCC-PC | VCC-PC | NA | NA | P | NA | NA | NA | NA |
| **GPIOD**[16] | | | | | | | | | |
| V25 | PD0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D2 | 2 | | O | | | | |
| | | LVDS0_VP0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V24 | PD1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D3 | 2 | | O | | | | |
| | | LVDS0_VN0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W25 | PD2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D4 | 2 | | O | | | | |
| | | LVDS0_VP1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W24 | PD3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D5 | 2 | | O | | | | |
| | | LVDS0_VN1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y25 | PD4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D6 | 2 | | O | | | | |
| | | LVDS0_VP2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| Y24 | PD5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D7 | 2 | | O | | | | |
| | | LVDS0_VN2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA25 | PD6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D10 | 2 | | O | | | | |
| | | LVDS0_VPC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AA24 | PD7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D11 | 2 | | O | | | | |
| | | LVDS0_VNC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB25 | PD8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D12 | 2 | | O | | | | |
| | | LVDS0_VP3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AB24 | PD9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D13 | 2 | | O | | | | |
| | | LVDS0_VN3 | 3 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V22 | PD10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D14 | 2 | | O | | | | |
| | | LVDS1_VP0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V21 | PD11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D15 | 2 | | O | | | | |
| | | LVDS1_VN0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W23 | PD12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D18 | 2 | | O | | | | |
| | | LVDS1_VP1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| W22 | PD13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D19 | 2 | | O | | | | |
| | | LVDS1_VN1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC25 | PD14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D20 | 2 | | O | | | | |
| | | LVDS1_VP2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC24 | PD15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D21 | 2 | | O | | | | |
| | | LVDS1_VN2 | 3 | | O | | | | |
| | | PWM7 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AC23 | PD16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D22 | 2 | | O | | | | |
| | | LVDS1_VPC | 3 | | O | | | | |
| | | PWM6 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD24 | PD17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_D23 | 2 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | LVDS1_VNC | 3 | | O | | | | |
| | | PWM5 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AD23 | PD18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_CLK | 2 | | O | | | | |
| | | LVDS1_VP3 | 3 | | O | | | | |
| | | PWM4 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| AE23 | PD19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_DE | 2 | | O | | | | |
| | | LVDS1_VN3 | 3 | | O | | | | |
| | | PWM3 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T21 | PD20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_HSYNC | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | PWM2 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U22 | PD21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | LCD_VSYNC | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | PWM1 | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U23 | PD22 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PD |
| | | Output | 1 | | O | | | | |
| | | PWM0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T19,T20 | VCC-PD | VCC-PD | NA | NA | P | NA | NA | NA | NA |
| **GPIOE**[16] | | | | | | | | | |
| A3 | PE0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_PCLK | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_CLK | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B2 | PE1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_MCLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_ERR | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| B3 | PE2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_HSYNC | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_SYNC | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A4 | PE3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_VSYNC | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_DVLD | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| E6 | PE4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D0 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D0 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C7 | PE5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D1 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D6 | PE6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D2 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D2 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D5 | PE7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D3 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D3 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C5 | PE8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D4 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D4 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C2 | PE9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D5 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D5 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | IO Disable | 7 | | OFF | | | | |
| F6 | PE10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D6 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D6 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C1 | PE11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D7 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | TS_D7 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G7 | PE12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D8 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C6 | PE13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D9 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F7 | PE14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D10 | 2 | | I | | | | |
| | | TWI0_SCK | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F5 | PE15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D11 | 2 | | I | | | | |
| | | TWI0_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B6 | PE16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D12 | 2 | | I | | | | |
| | | TWI1_SCK | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B4 | PE17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D13 | 2 | | I | | | | |
| | | TWI1_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G5 | PE18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D14 | 2 | | I | | | | |
| | | TWI2_SCK | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| E5 | PE19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_D15 | 2 | | I | | | | |
| | | TWI2_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B5 | PE20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_SCK | 2 | | O,OD | | | | |
| | | TWI3_SCK | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | PLL_LOCK_DBG | 5 | | I/O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A5 | PE21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | NCSI0_SDA | 2 | | I/O,OD | | | | |
| | | TWI3_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G6 | PE22 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PE |
| | | Output | 1 | | O | | | | |
| | | CSI_FSIN0 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| H8 | VCC-PE | VCC-PE | NA | NA | P | NA | NA | NA | NA |
| **GPIOF**[16] | | | | | | | | | |
| T2 | PF0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D1 | 2 | | I/O | | | | |
| | | JTAG_MS1 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| T1 | PF1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D0 | 2 | | I/O | | | | |
| | | JTAG_DI1 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U3 | PF2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_CLK[15] | 2 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | UART0_TX | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U2 | PF3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_CMD(14) | 2 | | I/O,OD | | | | |
| | | JTAG_DO1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V3 | PF4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D3 | 2 | | I/O | | | | |
| | | UART0_RX | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| V2 | PF5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D2 | 2 | | I/O | | | | |
| | | JTAG_CK1 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| U1 | PF6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOG**(16) | | | | | | | | | |
| D12 | PG0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | SDC1_CLK(15) | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F12 | PG1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | SDC1_CMD(14) | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D13 | PG2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | SDC1_D0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F13 | PG3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | SDC1_D1 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| E13 | PG4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | SDC1_D2 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| E12 | PG5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | SDC1_D3 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| E9 | PG6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | UART1_TX | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F9 | PG7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | UART1_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D10 | PG8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | UART1_RTS | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G9 | PG9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | UART1_CTS | 2 | | I | | | | |
| | | DMIC_DATA2 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F10 | PG10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | PCM1_SYNC | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT10 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| G10 | PG11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | PCM1_BCLK | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT11 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| E10 | PG12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | PCM1_DOUT | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT12 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G13 | PG13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | PCM1_DIN | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT13 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G12 | PG14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PG |
| | | Output | 1 | | O | | | | |
| | | I2S1_MCLK | 2 | | O | | | | |
| | | DMIC_DATA3 | 3 | | I | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT14 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| H12 | VCC-PG | VCC-PG | NA | NA | P | NA | NA | NA | NA |
| **GPIOH**[16] | | | | | | | | | |
| J2 | PH0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI0_SCK | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J1 | PH1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI0_SDA | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J3 | PH2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI1_SCK | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J4 | PH3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI1_SDA | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N5 | PH4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI5_SCK | 2 | | I/O,OD | | | | |
| | | MCSIA_SCK | 3 | | O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N6 | PH5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI5_SDA | 2 | | I/O,OD | | | | |
| | | MCSIA_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L1 | PH6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI6_SCK | 2 | | I/O,OD | | | | |
| | | MCSIB_SCK | 3 | | O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K1 | PH7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI6_SDA | 2 | | I/O,OD | | | | |
| | | MCSIB_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J6 | PH8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | MCSIA_MCLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K2 | PH9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | MCSIB_MCLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K5 | PH10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART3_TX | 2 | | O | | | | |
| | | NCSI1_D12 | 3 | | I | | | | |
| | | SPI1_CLK(12) | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT10 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L3 | PH11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART3_RX | 2 | | I | | | | |
| | | NCSI1_D13 | 3 | | I | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | SPI1_CS(10) | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT11 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K4 | PH12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART3_RTS | 2 | | O | | | | |
| | | NCSI1_D14 | 3 | | I | | | | |
| | | SPI1_MOSI | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT12 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K6 | PH13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART3_CTS | 2 | | I | | | | |
| | | NCSI1_D15 | 3 | | I | | | | |
| | | SPI1_MISO | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT13 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N7 | PH14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | OWA_OUT | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT14 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M6 | PH15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | OWA_IN | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT15 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K7 | PH16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | DMIC_DATA1 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT16 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J5 | PH17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | DMIC_DATA0 | 2 | | I | | | | |
| | | TWI4_SCK | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT17 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J7 | PH18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | DMIC_CLK | 2 | | O | | | | |
| | | TWI4_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PH_EINT18 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOJ**(16) | | | | | | | | | |
| R2 | PJ0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | NCSI1_PCLK | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_RXD3/ MII_RXD3/ RMII_NULL | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R3 | PJ1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_MCLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_RXD2/ MII_RXD2/ RMII_NULL | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P2 | PJ2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_HSYNC | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_RXD1/ MII_RXD1/ RMII_RXD1 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P1 | PJ3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_VSYNC | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_RXD0/ MII_RXD0/ RMII_RXD0 | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N3 | PJ4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D0 | 2 | | I | | | | |
| | | SDC3_D1 | 3 | | I/O | | | | |
| | | RGMII_RXCK/ MII_RXCK/ RMII_NULL | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| P3 | PJ5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D1 | 2 | | I | | | | |
| | | SDC3_D0 | 3 | | I/O | | | | |
| | | RGMII_RXCTL/ MII_RXDV/ RMII_CRS_DV | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M2 | PJ6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D2 | 2 | | I | | | | |
| | | SDC3_CLK(15) | 3 | | O | | | | |
| | | RGMII_NULL/ MII_RXERR/ RMII_RXER | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT6 | 6 | | I | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | IO Disable | 7 | | OFF | | | | |
| T7 | PJ7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D3 | 2 | | I | | | | |
| | | SDC3_CMD(14) | 3 | | I/O,OD | | | | |
| | | RGMII_TXD3/ MII_TXD3/ RMII_NULL | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R7 | PJ8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D4 | 2 | | I | | | | |
| | | SDC3_D3 | 3 | | I/O | | | | |
| | | RGMII_TXD2/ MII_TXD2/ RMII_NULL | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R6 | PJ9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D5 | 2 | | I | | | | |
| | | SDC3_D2 | 3 | | I/O | | | | |
| | | RGMII_TXD1/ MII_TXD1/ RMII_TXD1 | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N1 | PJ10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D6 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_TXD0/ MII_TXD0/ RMII_TXD0 | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT10 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M4 | PJ11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D7 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_NULL/ MII_CRS/ RMII_NULL | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT11 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R4 | PJ12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D8 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_TXCK/ MII_TXCK/ RMII_TXCK | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT12 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N2 | PJ13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D9 | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | RGMII_TXCTL/ MII_TXEN/ | 4 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | RMII_TXEN | | | | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT13 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R5 | PJ14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D10 | 2 | | I | | | | |
| | | TWI3_SCK | 3 | | I/O,OD | | | | |
| | | RGMII_NULL/ MII_TXERR/ RMII_NULL | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT14 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L2 | PJ15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_D11 | 2 | | I | | | | |
| | | TWI3_SDA | 3 | | I/O,OD | | | | |
| | | RGMII_CLKIN/ MII_COL/ RMII_NULL | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT15 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M3 | PJ16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_SCK | 2 | | O,OD | | | | |
| | | TWI4_SCK | 3 | | I/O,OD | | | | |
| | | MDC | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT16 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M5 | PJ17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | NCSI1_SDA | 2 | | I/O,OD | | | | |
| | | TWI4_SDA | 3 | | I/O,OD | | | | |
| | | MDIO | 4 | | I/O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT17 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N4 | PJ18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PJ |
| | | Output | 1 | | O | | | | |
| | | CSI_FSIN1 | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PJ_EINT18 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J8 | VCC-PJ | VCC-PJ | NA | NA | P | NA | NA | NA | NA |
| **PL** | | | | | | | | | |
| B22 | PL0 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-RTC |
| | | Output | 1 | | O | | | | |
| | | S_RSB_SCK | 2 | | O | | | | |
| | | S_TWI0_SCK | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A22 | PL1 | Input | 0 | Function7 | I | PU | PU/PD | 6 | VCC-RTC |
| | | Output | 1 | | O | | | | |
| | | S_RSB_SDA | 2 | | I/O | | | | |
| | | S_TWI0_SDA | 3 | | I/O,OD | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | S_PL_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B23 | PL2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | S_UART0_TX | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| A23 | PL3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | S_UART0_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| B24 | PL4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | S_JTAG_MS | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C22 | PL5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | S_JTAG_CK | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C23 | PL6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | S_JTAG_DO | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D20 | PL7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | S_JTAG_DI | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D23 | PL8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D22 | PL9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PL |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Reserved | 5 | | NA | | | | |
| | | S_PL_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K18 | VCC-PL | VCC-PL | NA | NA | P | NA | NA | NA | NA |
| **PM** | | | | | | | | | |
| K20 | PM0 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_PWM0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K19 | PM1 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_SPI_CLK(12) | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J19 | PM2 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_SPI_CS(10) | 2 | | I/O | | | | |
| | | S_PWM1 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J20 | PM3 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_SPI_MOSI | 2 | | I/O | | | | |
| | | S_PWM2 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J21 | PM4 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_SPI_MISO | 2 | | I/O | | | | |
| | | S_PWM3 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| C25 | PM5 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART1_TX | 2 | | O | | | | |
| | | S_PWM4 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| D24 | PM6 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART1_RX | 2 | | I | | | | |
| | | S_PWM5 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G22 | PM7 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | S_UART1_RTS | 2 | | O | | | | |
| | | S_PWM6 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F21 | PM8 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART1_CTS | 2 | | I | | | | |
| | | S_PWM7 | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J23 | PM9 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART2_TX | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K23 | PM10 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART2_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT10 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K22 | PM11 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART2_RTS | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT11 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F22 | PM12 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART2_CTS | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT12 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F20 | PM13 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT13 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G20 | PM14 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT14 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| J22 | PM15 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | S_CIR_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT15 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| F23 | PM16 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART3_TX | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT16 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G21 | PM17 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART3_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT17 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M20 | PM18 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART3_RTS | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT18 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M22 | PM19 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART3_CTS | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT19 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| G23 | PM20 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART4_TX | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT20 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| K21 | PM21 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_UART4_RX | 2 | | I | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT21 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M23 | PM24 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_TWI0_SCK | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT24 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| N21 | PM25 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_TWI0_SDA | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT25 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R23 | PM26 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_TWI1_SCK | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT26 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| R22 | PM27 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_TWI1_SDA | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT27 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N23 | PM28 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_TWI2_SCK | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT28 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N20 | PM29 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | S_TWI2_SDA | 2 | | I/O,OD | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT29 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| M21 | PM30 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | WATCHDOG_SIG | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT30 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| N22 | PM31 | Input | 0 | Function7 | I | Z | PU/PD | 6 | VCC-PM |
| | | Output | 1 | | O | | | | |
| | | R_WATCHDOG_SIG | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | S_PM_EINT31 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| L19 | VCC-PM | VCC-PM | NA | NA | P | NA | NA | NA | NA |
| **System** | | | | | | | | | |
| D19 | NMI(17) | NMI | NA | NA | I/O,OD | Z | PU/PD | NA | VCC-RTC |
| C24 | RESET(18) | RESET | NA | NA | I | Z | PU/PD | NA | VCC-RTC |
| K17 | TEST(19) | TEST | NA | NA | I | PD | PU/PD | NA | VCC-RTC |
| V23 | FEL | FEL | NA | NA | I | PU | PU/PD | NA | VCC-IO |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| T8 | JTAG-SEL0 | JTAG-SEL0 | NA | NA | I | PU | PU/PD | NA | VCC-IO |
| T9 | JTAG-SEL1 | JTAG-SEL1 | NA | NA | I | PU | PU/PD | NA | VCC-IO |
| M18 | BOOT-MODE0 | BOOT-MODE0 | NA | NA | I | PU | PU/PD | NA | VCC-IO |
| M19 | BOOT-MODE1 | BOOT-MODE1 | NA | NA | I | PU | PU/PD | NA | VCC-IO |
| **HSIC** | | | | | | | | | |
| E25 | HSIC-STR | HSIC-STR | NA | NA | A I/O | NA | NA | NA | VCC-HSIC |
| D25 | HSIC-DAT | HSIC-DAT | NA | NA | A I/O | NA | NA | NA | VCC-HSIC |
| P18 | VCC-HSIC | VCC-HSIC | NA | NA | P | NA | NA | NA | NA |
| **LRADC** | | | | | | | | | |
| D15 | LRADC0 | LRADC0 | NA | NA | AI | NA | NA | NA | AVCC |
| D16 | LRADC1 | LRADC1 | NA | NA | AI | NA | NA | NA | AVCC |
| **GPADC** | | | | | | | | | |
| E16 | GPADC0 | GPADC0 | NA | NA | AI | NA | NA | NA | AVCC |
| F16 | GPADC1 | GPADC1 | NA | NA | AI | NA | NA | NA | AVCC |
| F15 | GPADC2 | GPADC2 | NA | NA | AI | NA | NA | NA | AVCC |
| E15 | GPADC3 | GPADC3 | NA | NA | AI | NA | NA | NA | AVCC |
| G15 | GPADC4 | GPADC4 | NA | NA | AI | NA | NA | NA | AVCC |
| G16 | GPADC5 | GPADC5 | NA | NA | AI | NA | NA | NA | AVCC |
| **TV-OUT** | | | | | | | | | |
| R24 | TVOUT | TVOUT | NA | NA | AO | NA | NA | NA | VCC-TVOUT |
| P20 | VCC-TVOUT | VCC-TVOUT | NA | NA | P | NA | NA | NA | NA |
| **TV-IN** | | | | | | | | | |
| A14 | TVIN0 | TVIN0 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| B14 | TVIN1 | TVIN1 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| A13 | TVIN2 | TVIN2 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| B13 | TVIN3 | TVIN3 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| H17 | TVIN-VRP | TVIN-VRP | NA | NA | P | NA | NA | NA | VCC-TVIN |
| H16 | TVIN-VRN | TVIN-VRN | NA | NA | P | NA | NA | NA | VCC-TVIN |
| H13 | VCC-TVIN | VCC-TVIN | NA | NA | P | NA | NA | NA | NA |
| C14 | GND-TVIN | GND-TVIN | NA | NA | G | NA | NA | NA | NA |
| **MIPI_CSI_A** | | | | | | | | | |
| H3 | MCSIA-D0N | MCSIAD0N | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| H4 | MCSIA-D0P | MCSIA-D0P | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| G3 | MCSIA-D1N | MCSIA-D1N | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| G4 | MCSIA-D1P | MCSIA-D1P | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| D3 | MCSIA-D2N | MCSIA-D2N | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| D4 | MCSIA-D2P | MCSIA-D2P | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| C3 | MCSIA-D3N | MCSIA-D3N | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| C4 | MCSIA-D3P | MCSIA-D3P | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| F3 | MCSIA-CKN | MCSIA-CKN | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| F4 | MCSIA-CKP | MCSIA-CKP | NA | NA | AI | NA | NA | NA | VCC-MCSIA |
| K9 | VCC-MCSIA | VCC-MCSIA | NA | NA | P | NA | NA | NA | NA |
| **MIPI_CSI_B** | | | | | | | | | |
| H1 | MCSIB-D0N | MCSIB-D0N | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| H2 | MCSIB-D0P | MCSIB-D0P | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| G1 | MCSIB-D1N | MCSIB-D1N | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| G2 | MCSIB-D1P | MCSIB-D1P | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| E2 | MCSIB-D2N | MCSIB-D2N | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| E3 | MCSIB-D2P | MCSIB-D2P | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| D1 | MCSIB-D3N | MCSIB-D3N | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| D2 | MCSIB-D3P | MCSIB-D3P | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| F1 | MCSIB-CKN | MCSIB-CKN | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| F2 | MCSIB-CKP | MCSIB-CKP | NA | NA | AI | NA | NA | NA | VCC-MCSIB |
| J9 | VCC-MCSIB | VCC-MCSIB | NA | NA | P | NA | NA | NA | NA |
| **MIPI DSI** | | | | | | | | | |
| K25 | DSI-D0P | DSI-D0P | NA | NA | A I/O | NA | NA | NA | VCC-DSI |
| K24 | DSI-D0N | DSI-D0N | NA | NA | A I/O | NA | NA | NA | VCC-DSI |
| L25 | DSI-D1P | DSI-D1P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| L24 | DSI-D1N | DSI-D1N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| N25 | DSI-D2P | DSI-D2P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| N24 | DSI-D2N | DSI-D2N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| P25 | DSI-D3P | DSI-D3P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| P24 | DSI-D3N | DSI-D3N | NA | NA | AO | NA | NA | NA | VCC-DSI |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| M25 | DSI-CKP | DSI-CKP | NA | NA | AO | NA | NA | NA | VCC-DSI |
| M24 | DSI-CKN | DSI-CKN | NA | NA | AO | NA | NA | NA | VCC-DSI |
| P19 | VCC-DSI | VCC-DSI | NA | NA | P | NA | NA | NA | NA |
| **USB** | | | | | | | | | |
| F25 | USB0-DM(20) | USB0-DM | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| F24 | USB0-DP(20) | USB0-DP | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| G25 | USB1-DM(20) | USB1-DM | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| G24 | USB1-DP(20) | USB1-DP | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| H25 | USB2-DM(20) | USB2-DM | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| H24 | USB2-DP(20) | USB2-DP | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| J25 | USB3-DM(20) | USB3-DM | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| J24 | USB3-DP(20) | USB3-DP | NA | NA | A I/O | NA | NA | NA | VCC3V3-USB |
| N18 | VDD-USB | VDD-USB | NA | NA | P | NA | NA | NA | NA |
| R21 | VCC3V3-USB | VCC3V3-USB | NA | NA | P | NA | NA | NA | NA |
| **Audio Codec** | | | | | | | | | |
| E19 | MBIAS | MBIAS | NA | NA | AO | NA | NA | NA | AVCC |
| B16 | MICIN3N(21) | MICIN3N | NA | NA | AI | NA | NA | NA | AVCC |
| A17 | MICIN3P(21) | MICIN3P | NA | NA | AI | NA | NA | NA | AVCC |
| B17 | MICIN2N(21) | MICIN2N | NA | NA | AI | NA | NA | NA | AVCC |
| C18 | MICIN2P(21) | MICIN2P | NA | NA | AI | NA | NA | NA | AVCC |
| C16 | MICIN1N(21) | MICIN1N | NA | NA | AI | NA | NA | NA | AVCC |
| A16 | MICIN1P(21) | MICIN1P | NA | NA | AI | NA | NA | NA | AVCC |
| C19 | PHONEOUTN | PHONEOUTN | NA | NA | AO | NA | NA | NA | AVCC |
| B18 | PHONEOUTP | PHONEOUTP | NA | NA | AO | NA | NA | NA | AVCC |
| F18 | VRA1(24) | VRA1 | NA | NA | AO | NA | NA | NA | AVCC |
| E18 | VRA2(22) (24) | VRA2 | NA | NA | AO | NA | NA | NA | AVCC |
| A19 | LINEOUTR | LINEOUTR | NA | NA | AO | NA | NA | NA | AVCC |
| B19 | LINEOUTL | LINEOUTL | NA | NA | AO | NA | NA | NA | AVCC |
| B15 | LINEINR | LINEINR | NA | NA | AI | NA | NA | NA | AVCC |
| C15 | LINEINL | LINEINL | NA | NA | AI | NA | NA | NA | AVCC |
| D18 | AVCC(23)(24) | AVCC | NA | NA | P | NA | NA | NA | NA |
| G18 | VRP(24) | VRP | NA | NA | AO | NA | NA | NA | AVCC |
| D17 | AGND | AGND | NA | NA | G | NA | NA | NA | NA |
| **PLL&RTC** | | | | | | | | | |
| B21 | X32KIN(25) | X32KIN | NA | NA | AI | NA | NA | NA | VCC-RTC |
| A20 | X32KOUT(25)(26) | X32KOUT | NA | NA | AO | NA | NA | NA | VCC-RTC |
| C20 | X32KFOUT | X32KFOUT | NA | NA | AO,OD | NA | NA | NA | VCC-RTC |
| D21 | VCC-RTC | VCC-RTC | NA | NA | P | NA | NA | NA | NA |
| U25 | X24MIN | X24MIN | NA | NA | AI | NA | NA | NA | VCC-PLL |
| T25 | X24MOUT(27) | X24MOUT | NA | NA | AO | NA | NA | NA | VCC-PLL |
| T24 | X24MFOUT | X24MFOUT | NA | NA | AO | NA | NA | NA | VCC-PLL |
| T22 | VCC-PLL | VCC-PLL | NA | NA | P | NA | NA | NA | NA |
| **Efuse** | | | | | | | | | |
| V20 | VDDBP-EFUSE(28) | VDDBP-EFUSE | NA | NA | P | NA | NA | NA | NA |
| **Power** | | | | | | | | | |
| AC20,AC21, AC22,AD20, AD21,AD22, AE20,AE21, AE22 | VDD-CPUA | VDD-CPUA | NA | NA | P | NA | NA | NA | NA |
| Y21,Y22,Y23, AA21,AA22, AA23,AB21, AB22,AB23 | VDD-CPUB | VDD-CPUB | NA | NA | P | NA | NA | NA | NA |
| L8,L9,L10, M8,M9,M10 | VDD-SYS | VDD-SYS | NA | NA | P | NA | NA | NA | NA |
| K12,K13,K14, L12,L13,L14, M12,M13, M14 | VDD-GPU(29)(30) | VDD-GPU | NA | NA | P | NA | NA | NA | NA |
| M17,N17 | VDD-CPUS | VDD-CPUS | NA | NA | P | NA | NA | NA | NA |
| R8,R9,R10 | VCC-IO | VCC-IO | NA | NA | P | NA | NA | NA | NA |
| N8,N9 | VDD-VE(31) | VDD-VE | NA | NA | P | NA | NA | NA | NA |
| AE19 | VDD-CPUAFB | VDD-CPUAFB | NA | NA | P | NA | NA | NA | NA |
| Y20 | VDD-CPUBFB | VDD-CPUBFB | NA | NA | P | NA | NA | NA | NA |
| K15 | VDD-GPUFB | VDD-GPUFB | NA | NA | P | NA | NA | NA | NA |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| **GND** | | | | | | | | | |
| A1,A2,A7, A24, A25,B1, B20,B25,C17, D11,E4,E7, E24,F19,H9, H18,H19, J10,J11,J12, J13,J14,J15, J16,J17,J18, K3,K8,K10, K11,K16,L11, L15,L16,L17, L18,L23,M7, M11,M15, M16,N10, N11,N12, N13,N14,N15 ,N16,N19,P8, P9,P10,P11, P12,P13,P14, P15,P16,P17, P22,P23,R11, R12,R13,R14, R15,R16,R17, R18,R19,R20, R25,T10,T11, T12,T13,T14, T15,T16,T17, T18,T23,U4, U8,U9,U10, U11,U12,U13 ,U14,U15, U16,U17,U18 ,U19,U24,V7, V12,V16,V17, V18,V19,W5, W10,W18, W19,W20, W21,Y2,Y3, Y12,Y16,Y18, Y19,AA4,AA7 , AA13,AA19, AA20,AB9, AB5,AA18, AB15,AB11, AB18,AB19, AB20,AC7, AC8,AC13, AC19,AD16, AD1,AD9, AD19,AE2, AD25,AE1, AE24,AE25 | GND | GND | NA | NA | G | NA | NA | NA | NA |

(1).NA: No Application.
(2).OFF: Disable IO function of GPIO.
(3).32 data lines(SDQ[31:0]), 4 data masks(SDQM[3:0]), 4 data strobes differential signals(SDQS[3:0]P/SDQS[3:0]N), can be divided to 4 groups. The data lines can swap each other intra-group or inter-group, but for inter-group swap, data masks and data strobes differential signals also need to swap.
(4).For SDQ[31:0], SDQM[3:0], SA[15:0], SBA[2:0],SCS[1:0],SCKE[1:0],SODT[1:0],SRAS,SCAS,SWE,SCKP,SCKN, every single-ended characteristics impedance is within (50Ω ±20%).
(5).The differential characteristics impedance of each pair of differential signals (SCKP/SCKN, SDQS[3:0]P/ SDQS[3:0]N) is within (100Ω±20%).
(6).For LPDDR2 and LPDDR3, SA[15:0] is undefined, SA[15:0] can be floated or connected to GND.
(7).SRST is only used for DDR3/DDR3L, it can be floated for DDR2/LPDDR2/LPDDR3.
(8).SZQ is an analog input signal that connects to an external 240Ω -1% grounded resistor which is used to calibrate the DDR PHY impedance.
(9).SVREF is a reference voltage input used to set the electric level of IO input buffers. For DDR2/DDR3/DDR3L/LPDDR2/LPDDR3, the reference electric level is (VCC-DRAM/2).
(10).SPI_CS is low active and has an internal pull-up. The signal is suggested to connect to an external pull-up resistor.
(11).SPI_HOLD is low active . For some SPI flash devices, their SPI_HOLD and Reset signals are multiplexed, in order to compatibility, SPI_HOLD needs an external pull-up resistor.
(12).SPI_CLK is used to output clock to SPI flash. Suggest that connect to a 33Ω resistor in series to offer impedance matching and reduce high-frequency radiation.
(13).SDC2_DS must connect to a 10kΩ external pull-down resistor when eMMC5.0 HS400 mode is used.
(14).SDC[3:0]_CMD is SD/TF/SDIO/eMMC command signal that must connect to an external pull-up resistor.
(15).SDC[3:0]_CLK is used to output clock to SD/TF/SDIO/eMMC device. SDC[3:0]_CLK needs to connect to 33Ω resistor in series to offer impedance matching and reduce high-frequency radiation.
(16).If all IOs of a GPIO port are unused, we suggest that the GPIO port has normal power supply, all IOs shall be floated or connected to GND, and the corresponding register of all IOs can be set to Disable.
(17).NMI is PMU interrupt input/output signal, and trigger at low level by default. NMI needs to connect to an external pull-up resistor and then connect to VCC-RTC. Suggest that NMI connects to a 1nF capacitor to restrain ESD.
(18).RESET needs ESD protection and is suggested to connect to a 10kΩ external pull-up resistor.
(19).TEST is CP test signal that shall be floated.
(20).The differential characteristics impedance of each pair of differential signals (USB0-DP, USB0-DN, USB1-DP, USB1-DN, USB2-DP, USB2-DN, USB3-DP, USB3-DN) must be within (90Ω±20%).
(21).MICIN[3:1]P/[3:1]N is analog differential input signals that shall be far away from interference signals.

(22).VRA2 connects to a 200kΩ±1% external resistor which is used to calibrate internal circuit.
(23).AVCC is as the reference voltage of the internal analog circuit, so ACC shall be ensured ±2% voltage accuracy.
(24).The external capacitors of AVCC, VRP, VRA1, VRA2 shall be placed near the T7 chip, and in order to reduce loop area, the negative terminals of these capacitors shall be placed near AGND.
(25).A 10MΩ resister is connected in parallel between X32KOUT and X32KIN, the resistor can create negative feedback in an inverter to ensure amplifier in linear amplifier region.
(26).32KFOUT can output 32.768kHz clock by software configuration to provide external Bluetooth to use. The 32KFOUT is open-drain output that connects to a pull-up resistor and then connects to working voltage.
(27).X24MOUT connects to a 0Ω resistor in series by default, changing the resistor value can adjust clock buffer strength to restrain EMI.
(28).VDDBP-EFUSE must connect to a 4.7uF external filter capacitor.
(29).Ensure that VDD-GPU has completed power-on before RESET starts to power on.
(30).If product scheme needs to enable GPU DVFS and Idle function, then GPU must be ensured independent power supply. The power accuracy of GPU is 3%, and power transient drop (Vdrop) is within 40mV.
(31).Ensure that VDD-VE has completed power-on before RESET starts to power on.
(32).The maximum buffer strength of each GPIO is 6mA.

For details about schematic diagram and PCB design recommendations, see the ***Allwinner T7 Hardware Design Guide***.

## 4.3. Signal Descriptions

T7 contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 4-2. Table 4-3 shows the detailed function description of every signal based on the different interface.

**[1].Signal Name**: The name of every signal.

**[2].Description**: The detailed function description of every signal.

**[3].Type**: Denotes the signal direction.

I (Input),
O (Output),
I/O (Input / Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
A I/O (Analog Input/Output),
P (Power),
G (Ground)

**Table 4-3. Signal Descriptions**

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| **DRAM** | | |
| SDQ[31:0] | DRAM Bidirectional Data Line to the Memory Device | I/O |
| SDQS[3:0]P | DRAM Active-High Bidirectional Data Strobes to the Memory Device | I/O |
| SDQS[3:0]N | DRAM Active-Low Bidirectional Data Strobes to the Memory Device | I/O |
| SDQM[3:0] | DRAM Data Mask Signal to the Memory Device | O |
| SCKP | DRAM Active-High Clock Signal to the Memory Device | O |
| SCKN | DRAM Active-Low Clock Signal to the Memory Device | O |
| SCKE[1:0] | DRAM Clock Enable Signal to the Memory Device | O |
| SA[15:0] | DRAM Address Signal to the Memory Device | O |
| SBA[2:0] | DRAM Bank Address Signal to the Memory Device | O |
| SWE | DRAM Write Enable Strobe to the Memory Device | O |
| SCAS | DRAM Column Address Strobe to the Memory Device | O |
| SRAS | DRAM Row Address Strobe to the Memory Device | O |
| SCS[1:0] | DRAM Chip Select Signal to the Memory Device | O |
| SODT[1:0] | DRAM On-Die Termination Output Signal | O |
| SZQ | DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer) | AI |
| SRST | DRAM Reset Signal to the Memory Device | O |
| SVREF | DRAM Reference Power | P |
| VCC-DRAM | DRAM Power Supply | P |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| **System Control** | | |
| FEL | Boot Select<br>Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process.<br>For more details, see section 3.4 “BROM System” in the ***Allwinner T7 User Manual***. | I |
| JTAG-SEL[1:0] | JTAG Mode Select<br>The signal is used to select the port from which JTAG function outputs.<br>00: Software selects GPIOB<br>01: Mandatory output from GPIOB<br>10: Mandatory enter into pin daisy-chain testing mode<br>11: Software selects GPIOF or GPIOB | I |
| TEST | Test Signal | I |
| NMI | Non-Maskable Interrupt | I/O,OD |
| RESET | System Reset Signal(active low) | I |
| BOOT-MODE[1:0] | Pin BOOT Select<br>00: SMHC0-> NAND FLASH<br>01: SMHC0-> SMHC2<br>10: SMHC0-> SPI NAND->SPI NOR<br>11: SMHC0->SMHC2->NAND FLASH->SPI NAND->SPI NOR<br>For more details, see section 3.4 “BROM System” in the ***Allwinner T7 User Manual***. | I |
| **Interrupt** | | |
| PB_EINT[9:0] | GPIO B External Interrupt Input | I |
| PF_EINT[6:0] | GPIO F External Interrupt Input | I |
| PG_EINT[14:0] | GPIO G External Interrupt Input | I |
| PH_EINT[18:0] | GPIO H External Interrupt Input | I |
| PJ_EINT[18:0] | GPIO J External Interrupt Input | I |
| **JTAG** | | |
| JTAG_DO[1:0] | JTAG Data Output | O |
| JTAG_DI[1:0] | JTAG Data Input | I |
| JTAG_MS[1:0] | JTAG Mode Select Input | I |
| JTAG_CK[1:0] | JTAG Clock Input | I |
| **PWM** | | |
| PWM[7:0] | Pulse Width Modulation Channel | I/O |
| **CLOCK** | | |
| X32KIN | 32768Hz Crystal Input | AI |
| X32KOUT | 32768Hz Crystal Drive Output | AO |
| X32KFOUT | 32768Hz Clock Fanout | AO,OD |
| VCC-RTC | RTC Power Supply | P |
| RTC-VIO | Internal LDO Output Bypass | AO |
| X24MIN | 24MHz Crystal Input | AI |
| X24MOUT | 24MHz Crystal Drive Output | AO |
| X24MFOUT | 24MHz Clock Fanout | AO |
| VCC-PLL | PLL Power Supply | P |
| **NAND FLASH** | | |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| NAND_DQ[7:0] | Nand Flash Data Bit | I/O |
| NAND_CE[1:0] | Nand Flash Chip Select | O |
| NAND_WE | Nand Flash Write Enable | O |
| NAND_ALE | Nand Flash Address Latch Enable | O |
| NAND_CLE | Nand Flash Command Latch Enable | O |
| NAND_RE | Nand Flash Read Enable | O |
| NAND_RB[1:0] | Nand Flash Ready/Busy Status Indicator Signal | I |
| NAND_DQS | Nand Flash Data Strobe | I/O |
| **LCD** | | |
| LCD_D[7:2], LCD_D[15:10], LCD_D[23:18] | LCD Data Bit | O |
| LCD_CLK | LCD Clock Signal | O |
| LCD_DE | LCD Data Enable | O |
| LCD_HSYNC | LCD Horizontal Sync | O |
| LCD_VSYNC | LCD Vertical Sync | O |
| **MIPI DSI** | | |
| DSI-CKN | MIPI DSI Differential Clock Negative | AO |
| DSI-CKP | MIPI DSI Differential Clock Positive | AO |
| DSI-D0N | MIPI DSI Differential Data0 Negative | A I/O |
| DSI-D0P | MIPI DSI Differential Data0 Positive | A I/O |
| DSI-D1N | MIPI DSI Differential Data1 Negative | AO |
| DSI-D1P | MIPI DSI Differential Data1 Positive | AO |
| DSI-D2N | MIPI DSI Differential Data2 Negative | AO |
| DSI-D2P | MIPI DSI Differential Data2 Positive | AO |
| DSI-D3N | MIPI DSI Differential Data3 Negative | AO |
| DSI-D3P | MIPI DSI Differential Data3 Positive | AO |
| VCC-DSI | MIPI DSI Power Supply | P |
| **TV-OUT** | | |
| TVOUT | TV-out Output | AO |
| VCC-TVOUT | TV-out Power Supply | P |
| **CSI(x=[1:0])** | | |
| NCSIx_D[15:0] | CSI Data Bit | I |
| NCSIx_PCLK | CSI Pixel Clock | I |
| NCSIx_MCLK | CSI Master Clock | O |
| NCSIx_HSYNC | CSI Horizontal Sync | I |
| NCSIx_VSYNC | CSI Vertical Sync | I |
| CSI_FSINx | Frame SYNC Input | O |
| NCSIx_SCK | CCI Control Clock | O,OD |
| NCSIx_SDA | CCI Control Data | I/O,OD |
| **MIPI CSI** | | |
| MCSIA-D0N | MIPI CSI Controller A Data0 Negative Signal | AI |
| MCSIA-D0P | MIPI CSI Controller A Data0 Positive Signal | AI |
| MCSIA-D1N | MIPI CSI Controller A Data1 Negative Signal | AI |
| MCSIA-D1P | MIPI CSI Controller A Data1 Positive Signal | AI |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| MCSIA-D2N | MIPI CSI Controller A Data2 Negative Signal | AI |
| MCSIA-D2P | MIPI CSI Controller A Data2 Positive Signal | AI |
| MCSIA-D3N | MIPI CSI Controller A Data3 Negative Signal | AI |
| MCSIA-D3P | MIPI CSI Controller A Data3 Positive Signal | AI |
| MCSIA-CKN | MIPI CSI Controller A Clock Negative Signal | AI |
| MCSIA-CKP | MIPI CSI Controller A Clock Positive Signal | AI |
| VCC-MCSIA | MIPI CSI Controller A Power Supply | P |
| MCSIA_MCLK | MIPI CSI Controller A Master Clock | O |
| MCSIA_SCK | MIPI CSI Controller A CCI Control Clock | O,OD |
| MCSIA_SDA | MIPI CSI Controller A CCI Control Data | I/O,OD |
| MCSIB-D0N | MIPI CSI Controller B Data0 Negative Signal | AI |
| MCSIB-D0P | MIPI CSI Controller B Data0 Positive Signal | AI |
| MCSIB-D1N | MIPI CSI Controller B Data1 Negative Signal | AI |
| MCSIB-D1P | MIPI CSI Controller B Data1 Positive Signal | AI |
| MCSIB-D2N | MIPI CSI Controller B Data2 Negative Signal | AI |
| MCSIB-D2P | MIPI CSI Controller B Data2 Positive Signal | AI |
| MCSIB-D3N | MIPI CSI Controller B Data3 Negative Signal | AI |
| MCSIB-D3P | MIPI CSI Controller B Data3 Positive Signal | AI |
| MCSIB-CKN | MIPI CSI Controller B Clock Negative Signal | AI |
| MCSIB-CKP | MIPI CSI Controller B Clock Positive Signal | AI |
| VCC-MCSIB | MIPI CSI Controller B Power Supply | P |
| MCSIB_MCLK | MIPI CSI Controller B Master Clock | O |
| MCSIB_SCK | MIPI CSI Controller B CCI Control Clock | O,OD |
| MCSIB_SDA | MIPI CSI Controller B CCI Control Data | I/O,OD |
| **TV-IN** | | |
| TVIN[3:0] | TV-in Input | AI |
| TVIN-VRP | TV-in Reference Voltage Positive | P |
| TVIN-VRN | TV-in Reference Voltage Negative | P |
| VCC-TVIN | TV-in Power Supply | P |
| GND-TVIN | TV-in Ground | G |
| **USB** | | |
| USB0-DM | USB0 D- Signal | A I/O |
| USB0-DP | USB0 D+ Signal | A I/O |
| USB1-DM | USB1 D- Signal | A I/O |
| USB1-DP | USB1 D+ Signal | A I/O |
| USB2-DM | USB2 D- Signal | A I/O |
| USB2-DP | USB2 D+ Signal | A I/O |
| USB3-DM | USB3 D- Signal | A I/O |
| USB3-DP | USB3 D+ Signal | A I/O |
| VDD-USB | USB Power Supply | P |
| VCC3V3-USB | USB Power Supply | P |
| **HSIC** | | |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| HSIC-STR | HSIC Strobe Signal | A I/O |
| HSIC-DAT | HSIC Data Signal | A I/O |
| VCC-HSIC | HSIC Power Supply | P |
| **Audio Codec** | | |
| PHONEOUTP | Phone Positive Differential Output | AO |
| PHONEOUTN | Phone Negative Differential Output | AO |
| MICIN[3:1]P | Microphone Positive Differential Input | AI |
| MICIN[3:1]N | Microphone Negative Differential Input | AI |
| VRA1 | Internal Reference Voltage | AO |
| VRA2 | Internal Reference Voltage | AO |
| VRP | Internal Reference Voltage | AO |
| AVCC | Analog Power Supply | P |
| LINEINR | Right Single-ended Input for Line-in | AI |
| LINEINL | Left Single-ended Input for Line-in | AI |
| LINEOUTR | Right Single-ended Output for Line-out | AO |
| LIINEOUTL | Left Single-ended Output for Line-out | AO |
| MBIAS | First Bias Voltage Output for Main Microphone | AO |
| AGND | Analog Ground | G |
| **LRADC** | | |
| LRADC[1:0] | ADC Input for Key | AI |
| **GPADC** | | |
| GPADC[5:0] | Analog Input | AI |
| **EMAC** | | |
| RGMII_RXD3/MII_RXD3/RMII_NULL | RGMII/MII Receive Data | I |
| RGMII_RXD2/MII_RXD2/RMII_NULL | RGMII/MII Receive Data | I |
| RGMII_RXD1/MII_RXD1/RMII_RXD1 | RGMII/MII/RMII Receive Data | I |
| RGMII_RXD0/MII_RXD0/RMII_RXD0 | RGMII/MII/RMII Receive Data | I |
| RGMII_RXCK/MII_RXCK/RMII_NULL | RGMII/MII Receive Clock | I |
| RGMII_RXCTL/MII_RXDV/RMII_CRS_DV | RGMII Receive Control /MII Receive Data Valid /RMII Carrier Sense Receive Data Valid | I |
| RGMII_NULL/MII_RXERR/RMII_RXER | MII/RMII Receive Error | I |
| RGMII_TXD3/MII_TXD3/RMII_NULL | RGMII/MII Transmit Data | O |
| RGMII_TXD2/MII_TXD2/RMII_NULL | RGMII/MII Transmit Data | O |
| RGMII_TXD1/MII_TXD1/RMII_TXD1 | RGMII/MII/RMII Transmit Data | O |
| RGMII_TXD0/MII_TXD0/RMII_TXD0 | RGMII/MII/RMII Transmit Data | O |
| RGMII_TXCK/MII_TXCK/RMII_TXCK | RGMII/MII/RMII Transmit Clock<br>For RGMII,IO type is output;<br>For MII/RMII,IO type is input | I/O |
| RGMII_TXCTL/MII_TXEN/RMII_TXEN | RGMII Transmit Control /MII Transmit Enable /RMII Transmit Enable | O |
| RGMII_CLKIN/MII_COL/RMII_NULL | RGMII Transmit Clock from External /MII Collision Detect | I |
| RGMII_NULL/MII_CRS/RMII_NULL | MII Carrier Sense | I |
| RGMII_NULL/MII_TXERR/RMII_NULL | MII Transmit Error | O |
| MDC | RGMII/RMII Management Data Clock | O |
| MDIO | RGMII/RMII Management Data Input/Output | I/O |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| **SPI** | | |
| SPI0_CS | SPI Chip Select Signal(active low) | I/O |
| SPI0_CLK | SPI Clock Signal | I/O |
| SPI0_MOSI | SPI Master Data Out, Slave Data In | I/O |
| SPI0_MISO | SPI Master Data In, Slave Data Out | I/O |
| SPI0_HOLD | Temporarily Pause Serial Communication without Deselecting or Resetting the Device | I/O |
| SPI0_WP | SPI Write Protection(active low) or Serial Data | I/O |
| SPI1_CS | SPI Chip Select Signal(active low) | I/O |
| SPI1_CLK | SPI Clock Signal | I/O |
| SPI1_MOSI | SPI Master Data Out, Slave Data In | I/O |
| SPI1_MISO | SPI Master Data In, Slave Data Out | I/O |
| **UART** | | |
| UART0_TX | UART0 Data Transmit | O |
| UART0_RX | UART0 Data Receive | I |
| UART1_TX | UART1 Data Transmit | O |
| UART1_RX | UART1 Data Receive | I |
| UART1_RTS | UART1 Data Request to Send | O |
| UART1_CTS | UART1 Data Clear to Send | I |
| UART2_TX | UART2 Data Transmit | O |
| UART2_RX | UART2 Data Receive | I |
| UART2_RTS | UART2 Data Request to Send | O |
| UART2_CTS | UART2 Data Clear to Send | I |
| UART3_TX | UART3 Data Transmit | O |
| UART3_RX | UART3 Data Receive | I |
| UART3_RTS | UART3 Data Request to Send | O |
| UART3_CTS | UART3 Data Clear to Send | I |
| UART4_TX | UART4 Data Transmit | O |
| UART4_RX | UART4 Data Receive | I |
| UART4_RTS | UART4 Data Request to Send | O |
| UART4_CTS | UART4 Data Clear to Send | I |
| **TWI(x=[6:0])** | | |
| TWIx_SCK | TWI Clock | I/O,OD |
| TWIx_SDA | TWI Data/Address | I/O,OD |
| **SMHC** | | |
| SDC0_D[3:0] | SDC0 Data Bit | I/O |
| SDC0_CLK | SDC0 Clock | O |
| SDC0_CMD | SDC0 Command Signal | I/O,OD |
| SDC1_D[3:0] | SDC1 Data Bit | I/O |
| SDC1_CLK | SDC1 Clock | O |
| SDC1_CMD | SDC1 Command Signal | I/O,OD |
| SDC2_D[7:0] | SDC2 Data Bit | I/O |
| SDC2_CLK | SDC2 Clock | O |
| SDC2_CMD | SDC2 Command Signal | I/O,OD |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| SDC2_DS | SDC2 Data Strobe | I |
| SDC2_RST | SDC2 Reset | O |
| SDC3_D[3:0] | SDC3 Data Bit | I/O |
| SDC3_CLK | SDC3 Clock | O |
| SDC3_CMD | SDC3 Command Signal | I/O,OD |
| **I2S/PCM(x=[2:0])** | | |
| I2Sx_MCLK | I2S Master Clock | O |
| PCMx_DOUT | I2S/PCM Data Output | O |
| PCMx_DIN | I2S/PCM Data Input | I |
| PCMx_BCLK | I2S/PCM Bit Clock | I/O |
| PCMx_SYNC | I2S Sample Rate Left and Right Channel Select Clock/PCM Sync | I/O |
| **OWA** | | |
| OWA_OUT | OWA Output | O |
| OWA_IN | OWA Input | I |
| **DMIC** | | |
| DMIC_CLK | Digital Microphone Clock Output | O |
| DMIC_DATA[3:0] | Digital Microphone Data Input | I |
| **TSC** | | |
| TS_D[7:0] | Transport Stream Data | I |
| TS_CLK | Transport Stream Clock | I |
| TS_ERR | Transport Stream Error Indicate | I |
| TS_SYNC | Transport Stream Sync | I |
| TS_DVLD | Transport Stream Data Valid | I |
| **LVDS** | | |
| LVDS0_VP[3:0] | LVDS0 Data Positive Signal Output | AO |
| LVDS0_VN[3:0] | LVDS0 Data Negative Signal Output | AO |
| LVDS0_VPC | LVDS0 Clock Positive Signal Output | AO |
| LVDS0_VNC | LVDS0 Clock Negative Signal Output | AO |
| LVDS1_VP[3:0] | LVDS1 Data Positive Signal Output | AO |
| LVDS1_VN[3:0] | LVDS1 Data Negative Signal Output | AO |
| LVDS1_VPC | LVDS1 Clock Positive Signal Output | AO |
| LVDS1_VNC | LVDS1 Clock Negative Signal Output | AO |
| **Smart Card** | | |
| SIM_PWREN | Smart Card Power Enable | O |
| SIM_VPPEN | Smart Card Program Voltage Enable | O |
| SIM_VPPPP | Smart Card Program Control | O |
| SIM_CLK | Smart Card Clock | O |
| SIM_DATA | Smart Card Data | I/O |
| SIM_RST | Smart Card Reset | O |
| SIM_DET | Smart Card Detect | I |
| **CPUS Domain** | | |
| **S_RSB** | | |
| S_RSB_SCK | RSB Clock Signal | O |

| Pin/Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| S_RSB_SDA | RSB Serial Data | I/O |
| **S_CIR** | | |
| S_CIR_RX | Consumer Infrared Receiver | I |
| **S_UART** | | |
| S_UART0_TX | UART Data Transmit | O |
| S_UART0_RX | UART Data Receive | I |
| S_UART1_TX | UART Data Transmit | O |
| S_UART1_RX | UART Data Receive | I |
| S_UART1_CTS | UART Data Clear to Send | I |
| S_UART1_RTS | UART Data Request to Send | O |
| S_UART2_TX | UART Data Transmit | O |
| S_UART2_RX | UART Data Receive | I |
| S_UART2_CTS | UART Data Clear to Send | I |
| S_UART2_RTS | UART Data Request to Send | O |
| S_UART3_TX | UART Data Transmit | O |
| S_UART3_RX | UART Data Receive | I |
| S_UART3_CTS | UART Data Clear to Send | I |
| S_UART3_RTS | UART Data Request to Send | O |
| S_UART4_TX | UART Data Transmit | O |
| S_UART4_RX | UART Data Receive | I |
| **S_TWI(x=[2:0])** | | |
| S_TWIx_SCK | TWI Clock | I/O,OD |
| S_TWIx_SDA | TWI Data/Address | I/O,OD |
| **S_PWM** | | |
| S_PWM[7:0] | Pulse Width Modulation Channel | I/O |
| **S_SPI** | | |
| S_SPI_CLK | SPI Clock Signal | I/O |
| S_SPI_CS | SPI Chip Select Signal(active low) | I/O |
| S_SPI_MOSI | SPI Master Data Out, Slave Data In | I/O |
| S_SPI_MISO | SPI Master Data In, Slave Data Out | I/O |
| **S_JTAG** | | |
| S_JTAG_MS | JTAG Mode Select Input | I |
| S_JTAG_CK | JTAG Clock Input | I |
| S_JTAG_DO | JTAG Data Output | O |
| S_JTAG_DI | JTAG Data Input | I |
| **Watchdog** | | |
| WATCHDOG_SIG | Watchdog Signal | O |
| R_WATCHDOG_SIG | R_Watchdog Signal | O |
| **S_Interrupt** | | |
| S_PL_EINT[9:0] | GPIO L External Interrupt Input | I |
| S_PM_EINT[21:0] | GPIO M External Interrupt Input | I |
| S_PM_EINT[31:24] | GPIO M External Interrupt Input | I |

# 5. Electrical Characteristics

## 5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

**CAUTION**

**Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.**

**Table 5-1. Absolute Maximum Ratings**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| Tstg | Storage Temperature | | -40 | 150 | °C |
| Tj | Limiting Working Junction Temperature | | -40 | 125 | °C |
| VCC-IO | Power Supply for 3.3V Digital Part | | -0.3 | 3.96 | V |
| VCC-PC | Power Supply for Port C | | -0.3 | 3.96 | V |
| VCC-PD | Power Supply for Port D | | -0.3 | 3.96 | V |
| VCC-PE | Power Supply for Port E | | -0.3 | 3.96 | V |
| VCC-PG | Power Supply for Port G | | -0.3 | 3.96 | V |
| VCC-PL | Power Supply for Port L | | -0.3 | 3.96 | V |
| VCC-PM | Power Supply for Port M | | -0.3 | 3.96 | V |
| VCC-PJ | Power Supply for Port J | | -0.3 | 3.96 | V |
| AVCC | DC Supply Voltage for Analog Part | | -0.3 | 3.6 | V |
| VCC-DRAM | Power Supply for DRAM | | -0.3 | 1.98 | V |
| VCC3V3-USB | High Power Supply for USB | | -0.3 | 3.96 | V |
| VDD-USB | Low Power Supply for USB | | -0.3 | 1.32 | V |
| VCC-HSIC | Power Supply for HSIC | | -0.3 | 1.44 | V |
| VCC-TVOUT | Power Supply for TV-OUT | | -0.3 | 3.96 | V |
| VCC-TVIN | Power Supply for TV-IN | | -0.3 | 3.96 | V |
| VCC-MCSIA | Power Supply for MIPI-CSIA | | -0.3 | 3.96 | V |
| VCC-MCSIB | Power Supply for MIPI-CSIB | | -0.3 | 3.96 | V |
| VCC-DSI | Power Supply for MIPI DSI | | -0.3 | 3.96 | V |
| VCC-PLL | Power Supply for PLL | | -0.3 | 3.6 | V |
| VCC-RTC | Power Supply for RTC | | -0.3 | 3.96 | V |
| VDD-VE | Power Supply for Video Engine | | -0.3 | 1.32 | V |
| VDD-CPUA | Power Supply for CPUA | | -0.3 | 1.32 | V |
| VDD-CPUB | Power Supply for CPUB | | -0.3 | 1.32 | V |
| VDD-CPUS | Power Supply for CPUS | | -0.3 | 1.32 | V |
| VDD-GPU | Power Supply for GPU | | -0.3 | 1.32 | V |
| VDD-SYS | Power Supply for System | | -0.3 | 1.32 | V |
| $V_{ESD}$ | Electrostatic Discharge | Human Body Model(HBM)(1) | - | 2000 | V |

| | | | | | |
|---|---|---|---|---|---|
| | | Charged Device Model(CDM)[2] | - | 500 | V |
| $I_{Latch-up}$ | Latch-up I-test performance current-pulse injection on each IO pin[3] | | Pass | | |
| | Latch-up over-voltage performance voltage injection on each IO pin[4] | | Pass | | |

(1). Reference document: AEC-Q100-002.
(2). Reference document: AEC-Q100-011.
(3). Current test performance: AEC-Q100-004-REV-C (Class II); trigger current: ±200mA; temperature: 85°C ambient temperature.
(4). Over-voltage performance: AEC-Q100-004-REV-C (Class II); trigger voltage: each Vdd pin, stress at 1.5 x VddMax; temperature: 85°C ambient temperature.

## 5.2. Recommended Operating Conditions

All T7 modules are used under the operating conditions contained in Table 5-2.

**NOTE**

- **Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.**
- **The junction temperature is proportional to the chip power consumption. Ensure that the junction temperature is appropriate to match power supplies.**

**Table 5-2. Recommended Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ta | Ambient Operating Temperature | -40 | - | 85 | °C |
| Tj | Working Junction Temperature | -40 | - | 120 | °C |
| VCC-IO | Power Supply for 3.3V Digital Part | 2.97 | 3.3 | 3.63 | V |
| VCC-PC | Power Supply for Port C | 1.62 | 1.8 | 1.98 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| VCC-PD | Power Supply for Port D | 2.97 | 3.3 | 3.63 | V |
| VCC-PE | Power Supply for Port E | 1.62 | 1.8 | 1.98 | V |
| | | 2.52 | 2.8 | 3.08 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| VCC-PG | Power Supply for Port G | 1.62 | 1.8 | 1.98 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| VCC-PL | Power Supply for Port L | 1.62 | 1.8 | 1.98 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| VCC-PM | Power Supply for Port M | 1.62 | 1.8 | 1.98 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| VCC-PJ | Power Supply for Port J | 1.62 | 1.8 | 1.98 | V |
| | | 2.52 | 2.8 | 3.08 | V |
| | | 2.97 | 3.3 | 3.63 | V |
| VCC-DRAM | Power Supply for DDR3/DDR3L | 1.425 | 1.5 | 1.575 | V |
| | Power Supply for LPDDR2 | 1.14 | 1.2 | 1.3 | V |
| | Power Supply for LPDDR3 | 1.14 | 1.2 | 1.3 | V |
| AVCC | DC Supply Voltage for Analog Part | 2.94 | 3.0 | 3.06 | V |
| VCC3V3-USB | High Power Supply for USB | 2.97 | 3.3 | 3.63 | V |
| VDD-USB | Low Power Supply for USB | 0.99 | 1.1 | 1.21 | V |

| | | | | | |
|---|---|---|---|---|---|
| VCC-HSIC | Power Supply for HSIC | 1.14 | 1.2 | 1.26 | V |
| VCC-TVOUT | Power Supply for TV-OUT | 3.135 | 3.3 | 3.465 | V |
| VCC-TVIN | Power Supply for TV-IN | 3.135 | 3.3 | 3.465 | V |
| VCC-MCSIA | Power Supply for MIPI-CSIA | 2.97 | 3.3 | 3.63 | V |
| VCC-MCSIB | Power Supply for MIPI-CSIB | 2.97 | 3.3 | 3.63 | V |
| VCC-DSI | Power Supply for MIPI DSI | 2.97 | 3.3 | 3.63 | V |
| VCC-PLL | Power Supply for PLL | 2.7 | 3.0 | 3.3 | V |
| VCC-RTC | Power Supply for RTC | 2.97 | 3.3 | 3.63 | V |
| VDD-VE | Power Supply for Video Engine | 1.0 | 1.1 | 1.2 | V |
| VDD-CPUA | Power Supply for CPUA | 1.0 | - | 1.32 | V |
| VDD-CPUB | Power Supply for CPUB | 1.0 | - | 1.32 | V |
| VDD-CPUS | Power Supply for CPUS | 0.99 | 1.1 | 1.21 | V |
| VDD-GPU | Power Supply for GPU | 1.0 | 1.1 | 1.2 | V |
| VDD-SYS | Power Supply for System | 0.99 | 1.1 | 1.21 | V |

## 5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of T7.

**Table 5-3. DC Electrical Characteristics**
**(VCC-IO/VCC-PC/VCC-PD/VCC-PE/VCC-PG/VCC-PL/VCC-PM/VCC-PJ)**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital GPIO | High-Level Input Voltage | $V_{IH}$ | 0.7 *VCC-IO | - | VCC-IO + 0.3 | V |
| | Low-Level Input Voltage | $V_{IL}$ | -0.3 | - | 0.3 * VCC-IO | V |
| | Input Pull-up Resistance | $R_{PU}$ | 50 | 100 | 150 | kΩ |
| | Input Pull-down Resistance | $R_{PD}$ | 50 | 100 | 150 | kΩ |
| | High-Level Input Current | $I_{IH}$ | - | - | 10 | uA |
| | Low-Level Input Current | $I_{IL}$ | - | - | 10 | uA |
| | High-Level Output Voltage | $V_{OH}$ | VCC-IO – 0.3 | - | VCC-IO | V |
| | Low-Level Output Voltage | $V_{OL}$ | 0 | - | 0.2 | V |
| | Tri-State Output Leakage Current | $I_{OZ}$ | -10 | - | 10 | uA |
| | Input Capacitance | $C_{IN}$ | - | - | 5 | pF |
| | Output Capacitance | $C_{OUT}$ | - | - | 5 | pF |

## 5.4. SDRAM I/O DC Electrical Characteristics

The SDRAM I/O pads support DDR3,DDR3L,LPDDR2,and LPDDR3 operational modes. The SDRAM Controller(DRAMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DRAMC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3E DDR3 JEDEC standard release July, 2010
- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

**Table 5-4. DC Input Logic Level**

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DC input logic high | $V_{IH(DC)}$ | VREF + 100 | - | - | mV |
| DC input logic low | $V_{IL(DC)}$ | - | - | VREF – 100 | mV |
| Input reference voltage | Vref | 0.49 * VDDQ | - | 0.51 * VDDQ | V |

| | | | | | |
|---|---|---|---|---|---|
| Input termination resistance(ODT) to $V_{DDQ}/2$ | $R_{TT}$ | 60 | 120 | Open | Ω |

**Table 5-5. Output DC Current Drive**

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DC output high voltage | $V_{OH}$ | 0.9 * VDDQ | - | V |
| DC output low voltage | $V_{OL}$ | - | 0.1 * VDDQ | V |

# 5.5. PLL Electrical Characteristics

## 5.5.1. CPU PLL Electrical Parameters

**Table 5-6. CPU PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 60MHz ~ 2.1GHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 3ms |
| Max. Peak-to-Peak Supply Noise | 200ps |

## 5.5.2. Audio PLL Electrical Parameters

**Table 5-7. Audio PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 24.576MHz, 22.5792MHz,(24.576 * 8) MHz, (22.5792 * 8) MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 1500ps |

## 5.5.3. GPU PLL Electrical Parameters

**Table 5-8. GPU PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 144MHz ~ 1000MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 200ps |

## 5.5.4. Peripheral0/1 PLL Electrical Parameters

**Table 5-9. Peripheral0/1 PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 504MHz ~ 1.4GHz |

| | |
|---|---|
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.5.5. MIPI PLL Electrical Parameters

**Table 5-10. MIPI PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 500MHz ~ 1.4GHz |
| Reference Clock | Video0 PLL |
| Max. Lock Time | 5ms |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.5.6. DDR0/1 PLL Electrical Parameters

**Table 5-11. DDR0/1 PLL Electrical Parameters**

| Parameter | Value | |
|---|---|---|
| Clock Output Range | 192MHz ~ 1.6GHz | |
| Reference Clock | 24MHz | |
| Max. Lock Time | 1ms | |
| Max. Peak-to-Peak Supply Noise | 192MHz ~800MHz | 200ps |
| | 800MHz ~1.3GHz | 140ps |
| | 1.3GHz ~1.6GHz | 100ps |

### 5.5.7. Video0/1 PLL Electrical Parameters

**Table 5-12. Video0/1 PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~ 600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.5.8. VE PLL Electrical Parameters

**Table 5-13. VE PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~ 600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.5.9. DE PLL Electrical Parameters

**Table 5-14. DE PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~ 600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 200ps |

### 5.5.10. HSIC PLL Electrical Parameters

**Table 5-15. HSIC PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192MHz ~ 600MHz |
| Reference Clock | 24MHz |
| Max. Lock Time | 100us |
| Max. Peak-to-Peak Supply Noise | 200ps |

## 5.6. LRADC Electrical Characteristics

LRADC is one analog-to-digital(ADC) converter for key application. Table 5-16 lists LRADC electrical characteristics.

**Table 5-16. LRADC Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ADC Resolution | - | 6 | - | bits |
| Full-scale Input Range | 0 | - | 0.667*AVCC | V |
| Quantizing Error | - | 1 | - | LSB |
| Clock Frequency | - | - | 250 | Hz |
| Conversion Time | - | 14 | - | ADC Clock Cycles |

## 5.7. SDIO Electrical Parameters

The SDIO electrical parameters are related to different supply voltage.

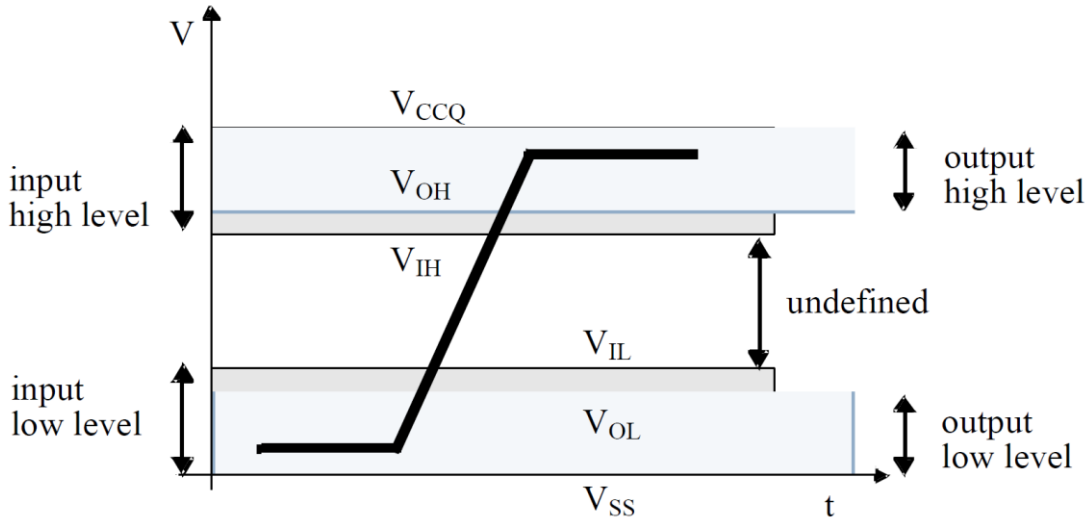



**Figure 5-1. SDIO Voltage Waveform**

Table 5-17 shows 3.3V SDIO electrical parameters.

**Table 5-17. 3.3V SDIO Electrical Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD | Power voltage | 2.7 | - | 3.6 | V |
| $V_{CCQ}$ | I/O voltage | 2.7 | | 3.6 | V |
| $V_{OH}$ | Output high-level voltage | 0.75 * $V_{CCQ}$ | - | - | V |
| $V_{OL}$ | Output low-level voltage | - | - | 0.125 * $V_{CCQ}$ | V |
| $V_{IH}$ | Input high-level voltage | 0.625 * $V_{CCQ}$ | - | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input low-level voltage | $V_{SS}$ - 0.3 | - | 0.25 * $V_{CCQ}$ | V |

Table 5-18 shows 1.8V SDIO electrical parameters.

**Table 5-18. 1.8V SDIO Electrical Parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD | Power voltage | 2.7 | - | 3.6 | V |
| $V_{CCQ}$ | I/O voltage | 1.7 | | 1.95 | V |
| $V_{OH}$ | Output HIGH voltage | $V_{CCQ}$ -0.45 | - | - | V |
| $V_{OL}$ | Output LOW voltage | - | - | 0.45 | V |
| $V_{IH}$ | Input HIGH voltage | 0.625 * $V_{CCQ}$ (1) | - | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input LOW voltage | $V_{SS}$ - 0.3 | - | 0.35 * $V_{CCQ}$ (2) | V |

**NOTE**

**0.7 * VDD for MMC4.3 or lower. 0.3 * VDD for MMC4.3 or lower.**

## 5.8. Audio Codec Electrical Parameters

Table 5-19 to Table 5-21 show audio codec electrical parameters.

VDD-SYS = 1.1V, AVCC=3.0V, Ta=25°C , 1kHz sinusoid signal, fs = 48kHz, input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

**Table 5-19. Audio Codec Typical Performance**

| Parameter | Test Conditions | Min | Typ(L/R) | Max | Unit |
|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| DAC Path | **DAC to Line-out signal on LINEOUTL or LINEOUTR(R=10kΩ)** | | | | | |
| | Full-scale Level | 0dBFS 1kHz | | 915 | | mVrms |
| | SNR(A-weighted) | 0dB 1kHz | | 98 | | dB |
| | THD+N | 0dB 1kHz | | -80 | | dB |
| | Crosstalk | R_0dB_L_0data 1kHz/ L_0dB_R_0data 1kHz | | -90 | | dB |
| | **DAC to Speaker signal on PHONEOUTP/N(R=10kΩ)** | | | | | |
| | Full-scale Level | 0dB 1kHz | | 1.8 | | Vrms |
| | SNR(A-weighted) | 0dB 1kHz | | 98 | | dB |
| | THD+N | 0dB 1kHz | | -80 | | dB |
| ADC Path | **MIC1P/N to ADC via ADC mixer** | | | | | |
| | Full-scale Level | 2.5Vpp 1kHz 0dB | | 820 | | mFFS |
| | SNR(A-weighted) | 2.5Vpp 1kHz 0dB | | 95 | | dB |
| | THD+N | 2.5Vpp 1kHz 0dB | | -80 | | dB |
| | SNR(A-weighted) | 55mVpp 1kHz 33dB | | 77 | | dB |
| | THD+N | 55mVpp 1kHz 33dB | | -70 | | dB |
| | **MIC2 to ADC via ADC mixer** | | | | | |
| | Full-scale Level | 2.5Vpp 1kHz 0dB | | 820 | | mFFS |
| | SNR(A-weighted) | 2.5Vpp 1kHz 0dB | | 95 | | dB |
| | THD+N | 2.5Vpp 1kHz 0dB | | -80 | | dB |
| | SNR(A-weighted) | 55mVpp 1kHz 33dB | | 77 | | dB |
| | THD+N | 55mVpp 1kHz 33dB | | -70 | | dB |
| | **MIC3 to ADC via ADC mixer** | | | | | |
| | Full-scale Level | 2.5Vpp 1kHz 0dB | | 820 | | mFFS |
| | SNR(A-weighted) | 2.5Vpp 1kHz 0dB | | 95 | | dB |
| | THD+N | 2.5Vpp 1kHz 0dB | | -80 | | dB |
| | SNR(A-weighted) | 55mVpp 1kHz 33dB | | 77 | | dB |
| | THD+N | 55mVpp 1kHz 33dB | | -70 | | dB |
| | **LINEINL/R to ADC via ADC mixer** | | | | | |
| | Full-scale Level | 2.5Vpp 1kHz 0dB | | 830 | | mFFS |
| | SNR(A-weighted) | 2.5Vpp 1kHz 0dB | | 98 | | dB |
| | THD+N | 2.5Vpp 1kHz 0dB | | -80 | | dB |
| Bypass Path Performance | **LINEINL/R to LINEOUTL/R via output mixer** | | | | | |
| | Full-scale Level | 2.8Vpp 1kHz 0dB | | 930 | | mVrms |
| | SNR(A-weighted) | 2.8Vpp 1kHz 0dB | | 100 | | dB |
| | THD+N | 2.8Vpp 1kHz 0dB | | -90 | | dB |

**Table 5-20. Audio Input Interface Parameters**

| Input Interface | Input Amplitude | Interface Type | Voltage Range | Performance |
|---|---|---|---|---|
| MICIN1P/N<br>MICIN2P/N<br>MICIN3P/N | 55mVpp(MIC differential input, 33dB Gain) | Mono differential input | AVCC: 0~3.0V | SNR: 77dB<br>THD:-70dB |
| LINEINL/R | 2.5Vpp(linear input) | Stereo single-ended input | AVCC: 0~3.0V | SNR: 98dB<br>THD:-80dB |

(1). Note that acceptable input amplitude is relevant with internal gain.
(2). Must block capacitor, the chip-end has 1.5V DC bias voltage.

**Table 5-21. Audio Output Interface Parameters**

| Output Interface | Output Amplitude | Interface Type | Voltage Range | Performance |
|---|---|---|---|---|
| LINEOUTL/R | 0.9Vrms | Stereo single-ended linear output | AVCC: 0~3.0V | SNR:98dB<br>THD:-80dB |
| PHONEOUTP/N | 1.8Vrms | Mono differential linear output | AVCC: 0~3.0V | SNR:98dB<br>THD:-80dB |

(1). L/R : left and right channel; P/N : differential pair.
(2). L/R can transform into P/N by certain way, but not the opposite.
(3). The noise of AVCC cannot be solved by differential way.
(4). The external circuit can eliminate power, ground and electromagnetic interference by differential way.

## 5.9. Oscillator Electrical Characteristics

T7 contains two external input clocks: X24MIN and X32KIN, two output clocks: X24MOUT and X32KOUT.

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN. Table 5-22 lists the 24MHz crystal specifications.

**Table 5-22. 24MHz Crystal Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | - | 24.000 | - | MHz |
| $t_{ST}$ | Startup Time | - | - | 2 | ms |
| | Frequency Tolerance at 25 °C | -50 | - | +50 | ppm |
| | Oscillation Mode | Fundamental | | | - |
| | Maximum Change Over Temperature Range | -50 | - | +50 | ppm |
| $P_{ON}$ | Drive Level | - | - | 300 | uW |
| $C_L$ | Equivalent Load Capacitance | 12 | 18 | 22 | pF |
| $R_S$ | Series Resistance(ESR) | - | 25 | 50 | Ω |
| | Duty Cycle | 30 | 50 | 70 | % |
| $C_I$ | Motional Capacitance | - | 4.72 | - | pF |
| $C_O$ | Shunt Capacitance | 5 | 6.5 | 7.5 | pF |
| $R_I$ | Insulation Resistor | 500MΩ Minimum at D.C.100V | | | |

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. Table 5-23 lists the 32768Hz crystal specifications.

**Table 5-23. 32768Hz Crystal Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | - | 32768 | - | Hz |
| $t_{ST}$ | Startup Time | - | - | - | ms |
| | Frequency Tolerance at 25 °C | -20 | - | +20 | ppm |
| | Oscillation Mode | Fundamental | | | - |
| | Maximum Change Over Temperature Range | -20 | - | +20 | ppm |
| $P_{ON}$ | Drive Level | - | - | 1.0 | uW |
| $C_L$ | Equivalent Load Capacitance | - | 18 | - | pF |
| $R_S$ | Series Resistance(ESR) | - | - | 70 | kΩ |
| | Duty Cycle | 30 | 50 | 70 | % |
| $C_I$ | Motional Capacitance | - | 2 | - | fF |
| $C_O$ | Shunt Capacitance | - | 1.1 | - | pF |
| $R_I$ | Insulation Resistor | 500MΩ Minimum at D.C.100V | | | |

# 5.10. Maximum Current Consumption

If you have questions about power consumption parameters, contact with Allwinner FAE.

# 5.11. External Memory Electrical Characteristics

## 5.11.1. SDRAM AC Electrical Characteristics

### 5.11.1.1. DDR3/DDR3L Parameters

Figure 5-2 shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 5-24.

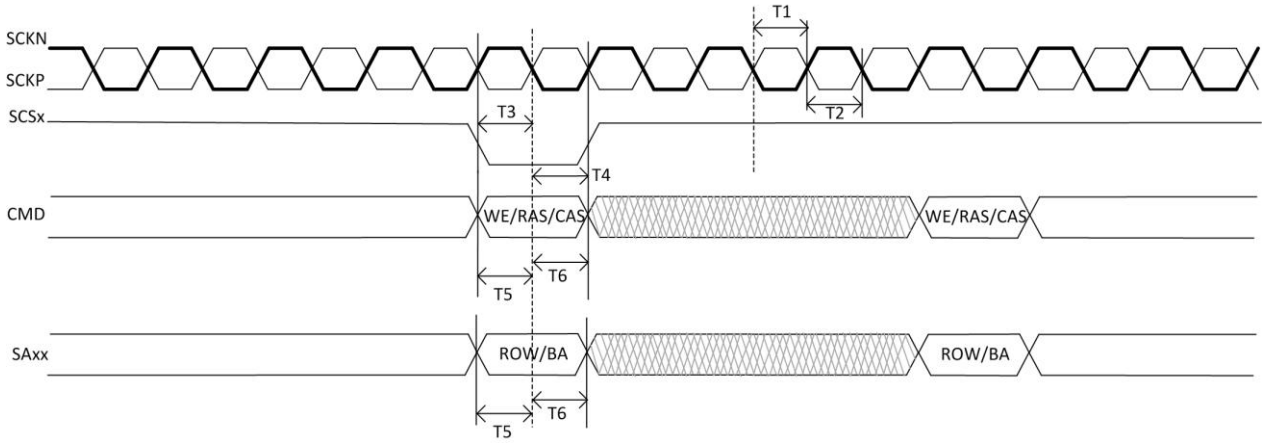



**Figure 5-2. DDR3/DDR3L Command and Address Timing**

**Table 5-24. DDR3/DDR3L Timing Parameters**

| ID | Parameter | Symbol | Clock = 800 MHz | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Suggest | Max | |
| T1 | SCKP clock high-level width | $t_{CH}$ | 0.47 | - | 0.53 | tck |
| T2 | SCKP clock low-level width | $t_{CL}$ | 0.47 | - | 0.53 | tck |
| T3 | CS setup time | $t_{IS}$ | 170 | 295 | - | ps |
| T4 | CS hold time | $t_{IH}$ | 120 | 245 | - | ps |
| T5 | Command and Address setup time to Clock edge | $t_{IS}$ | 170 | 295 | - | ps |
| T6 | Command and Address hold time to Clock edge | $t_{IH}$ | 120 | 245 | - | ps |

T1 and T2 are in reference to Vref level.
T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-3 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 5-25.

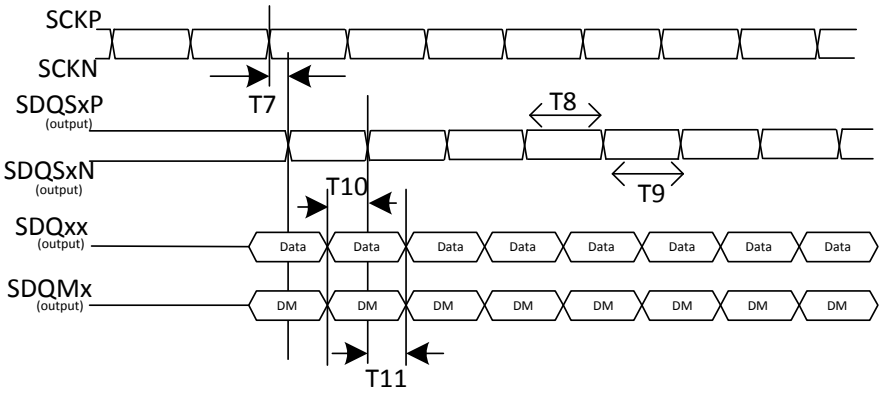



**Figure 5-3. DDR3/DDR3L Write Cycle**

**Table 5-25. DDR3/DDR3L Write Cycle Parameters**

| ID | Parameter | Symbol | Clock = 800 MHz | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Suggest | Max | |
| T7 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSS}$ | -0.27 | - | 0.27 | $t_{CK}$ |
| T8 | SDQSxP high level width | $t_{DQSH}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T9 | SDQSxP low level width | $t_{DQSL}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T10 | Data setup time to SDQSxP/SDQSxN | $t_{DS}$ | 10 | 145 | - | ps |
| T11 | Data hold time to SDQSxP/SDQSxN | $t_{DH}$ | 45 | 180 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7,T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-4 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 5-26.

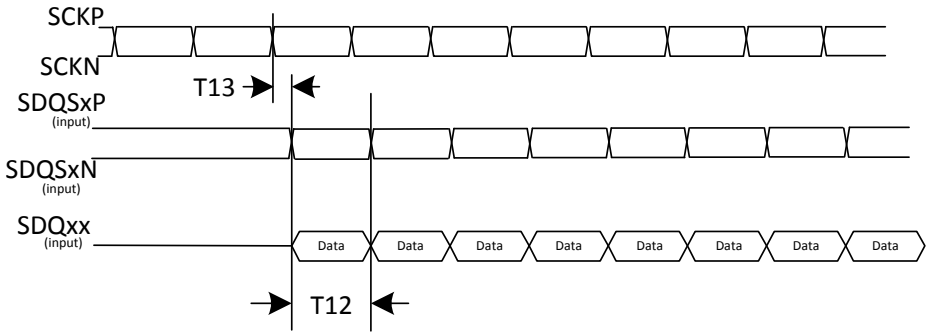



**Figure 5-4. DDR3/DDR3L Read Cycle**

**Table 5-26. DDR3/DDR3L Read Cycle Parameters**

| ID | Parameter | Symbol | Clock = 800 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T12 | Read Data valid width | $t_{Data}$ | 200 | - | ps |
| T13 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSCK}$ | -225 | 225 | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 and T13 are in reference to Vref level.

#### 5.11.1.2. LPDDR3 Parameters

Figure 5-5 shows the LPDDR3 command and address timing diagram. The timing parameters for this diagram shows in

Table 5-27.

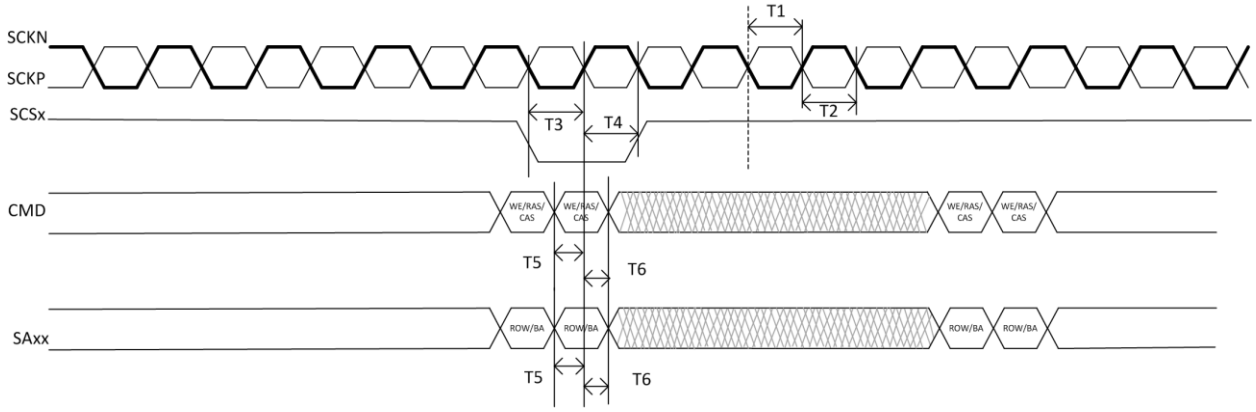



**Figure 5-5. LPDDR3 Command and Address Timing Diagram**

**Table 5-27. LPDDR3 Command and Address Timing Parameters**

| ID | Parameter | Symbol | Clock = 667 MHz | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Suggest | Max | |
| T1 | Clock high pulse width | $t_{CH}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T2 | Clock low pulse width | $t_{CL}$ | 0.45 | - | 0.55 | $t_{CK}$ |
| T3 | SCSx input setup time | $t_{ISCS}$ | 215 | 370.5 | - | ps |
| T4 | SCSx input hold time | $t_{IHCS}$ | 240 | 392.5 | - | ps |
| T5 | Address and control input setup time | $t_{IAS}$ | 100 | 177.5 | - | ps |
| T6 | Address and control input hold time | $t_{IAH}$ | 125 | 202.5 | - | ps |

T1 and T2 are in reference to Vref level.
T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-6 shows the LPDDR3 write timing diagram. The timing parameters for this diagram shows in Table 5-28.

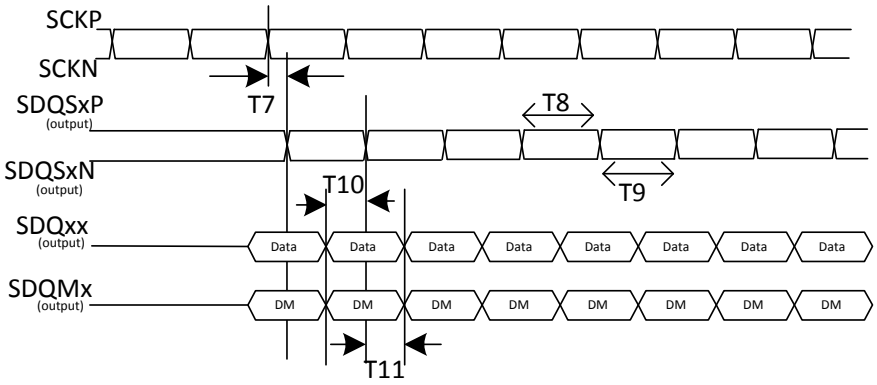



**Figure 5-6. LPDDR3 Write Cycle**

**Table 5-28. LPDDR3 Write Cycle Parameters**

| ID | Parameter | Symbol | Clock = 667 MHz | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Suggest | Max | |
| T7 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSS}$ | 0.75 | - | 1.25 | $t_{CK}$ |
| T8 | SDQSx input high-level width | $t_{DQSH}$ | 0.4 | - | - | $t_{CK}$ |
| T9 | SDQSx input low-level width | $t_{DQSL}$ | 0.4 | - | - | $t_{CK}$ |
| T10 | SDQxx and SDQMx input setup time | $t_{DS}$ | 100 | 177.5 | - | ps |
| T11 | SDQxx and SDQMx input hold time | $t_{DH}$ | 125 | 202.5 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7, T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-7 shows the LPDDR3 read timing diagram. The timing parameters for this diagram shows in Table 5-29.

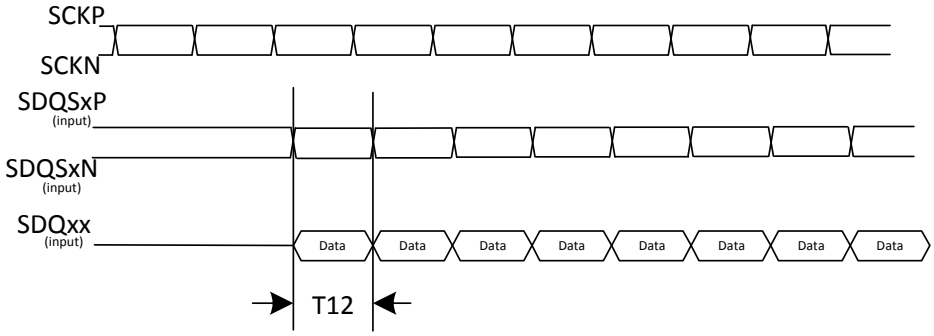



**Figure 5-7. LPDDR3 Read Cycle**

**Table 5-29. LPDDR3 Read Cycle Parameters**

| ID | Parameter | Symbol | Clock = 667 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T12 | Read Data valid width | $t_{DATA}$ | 200 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 is in reference to Vref level.

### 5.11.1.3. LPDDR2 Parameters

Figure 5-8 shows the LPDDR2 command and address timing diagram. The timing parameters for this diagram shows in Table 5-30.

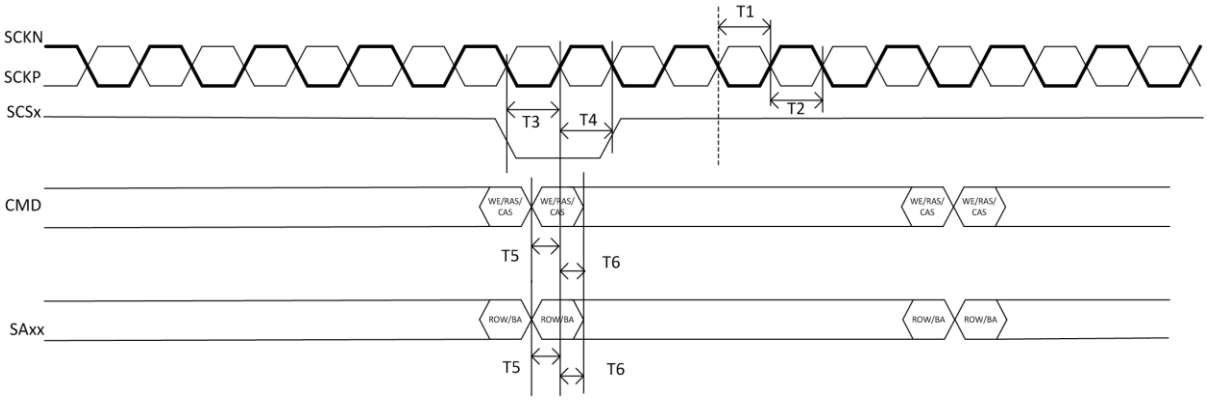



**Figure 5-8. LPDDR2 Command and Address Timing Diagram**

**Table 5-30. LPDDR2 Command and Address Timing Parameters**

| ID | Parameter | Symbol | Clock = 533 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T1 | Clock high pulse width | $t_{CH}$ | 0.45 | 0.55 | $t_{CK}$ |
| T2 | Clock low pulse width | $t_{CL}$ | 0.45 | 0.55 | $t_{CK}$ |
| T3 | SCSx input setup time | $t_{IS}$ | 220 | - | ps |
| T4 | SCSx input hold time | $t_{IH}$ | 220 | - | ps |
| T5 | Address and control input setup time | $t_{IS}$ | 220 | - | ps |
| T6 | Address and control input hold time | $t_{IH}$ | 220 | - | ps |

All measurements are in reference to Vref level.

Figure 5-9 shows the LPDDR2 write timing diagram. The timing parameters for this diagram shows in Table 5-31.

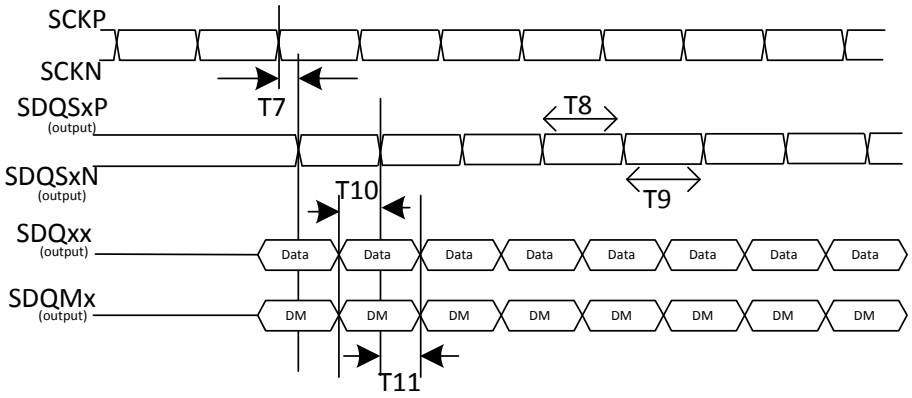



**Figure 5-9. LPDDR2 Write Cycle**

**Table 5-31. LPDDR2 Write Cycle Parameters**

| ID | Parameter | Symbol | Clock = 533 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T7 | SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge | $t_{DQSS}$ | 0.75 | 1.25 | $t_{CK}$ |
| T8 | SDQSx input high-level width | $t_{DQSH}$ | 0.4 | - | $t_{CK}$ |
| T9 | SDQSx input low-level width | $t_{DQSL}$ | 0.4 | - | $t_{CK}$ |
| T10 | SDQxx and SDQMx input setup time | $t_{DS}$ | 210 | - | ps |
| T11 | SDQxx and SDQMx input hold time | $t_{DH}$ | 210 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
All measurements are in reference to Vref level.

Figure 5-10 shows the LPDDR2 read timing diagram. The timing parameters for this diagram shows in Table 5-32.

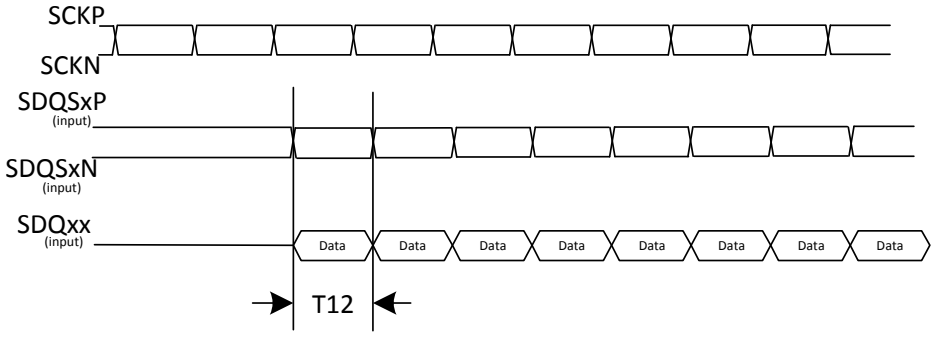



**Figure 5-10. LPDDR2 Read Cycle**

**Table 5-32. LPDDR2 Read Cycle Parameters**

| ID | Parameter | Symbol | Clock = 533 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| T12 | Read Data valid width | $t_{DATA}$ | 300 | - | ps |

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 is in reference to Vref level.

### 5.11.2. Nand AC Electrical Characteristics

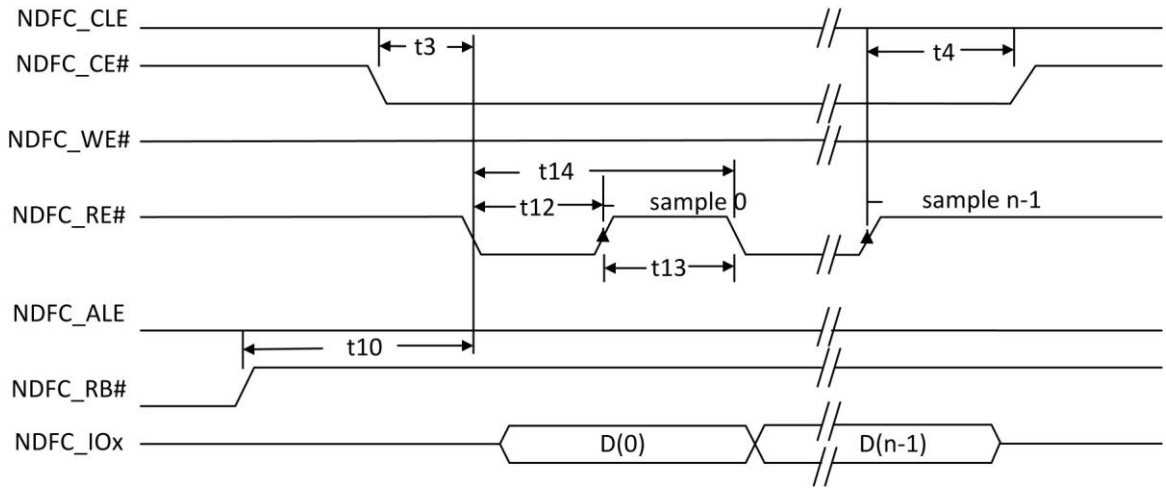



**Figure 5-11. Conventional Serial Access Cycle Timing (SAM0)**

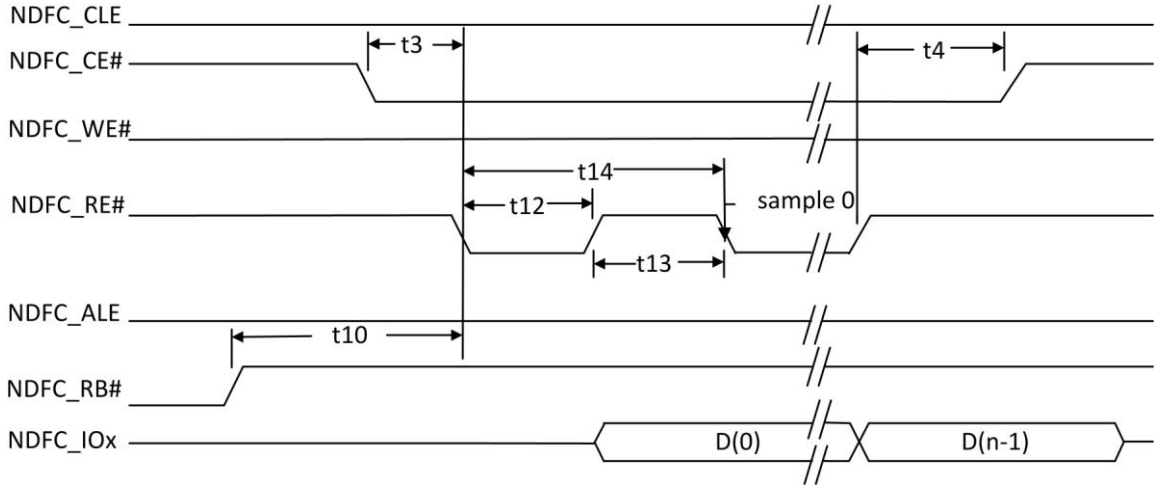



**Figure 5-12. EDO Type Serial Access after Read Cycle Timing (SAM1)**

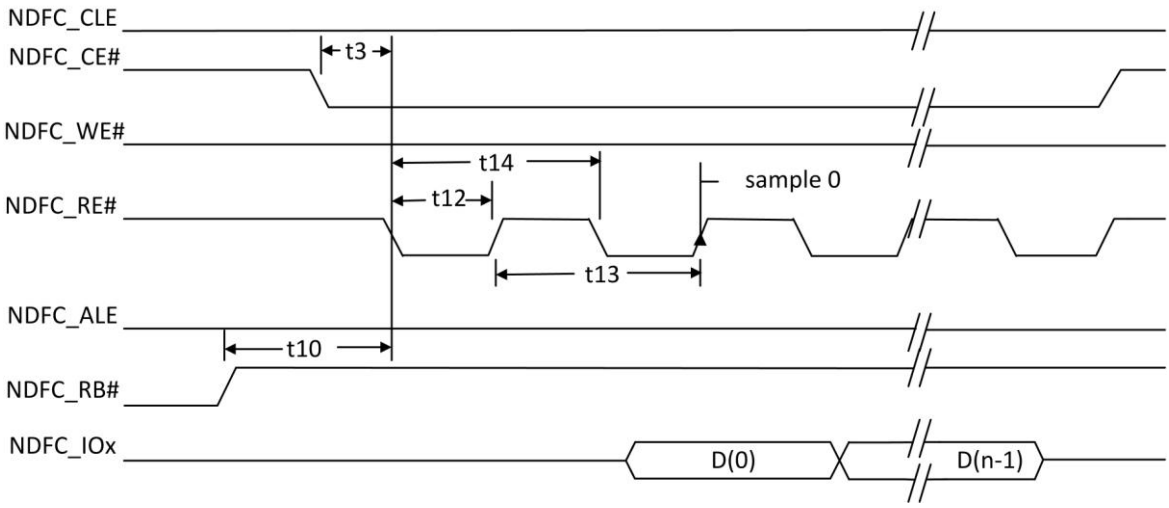



**Figure 5-13. Extending EDO Type Serial Access Mode Timing (SAM2)**

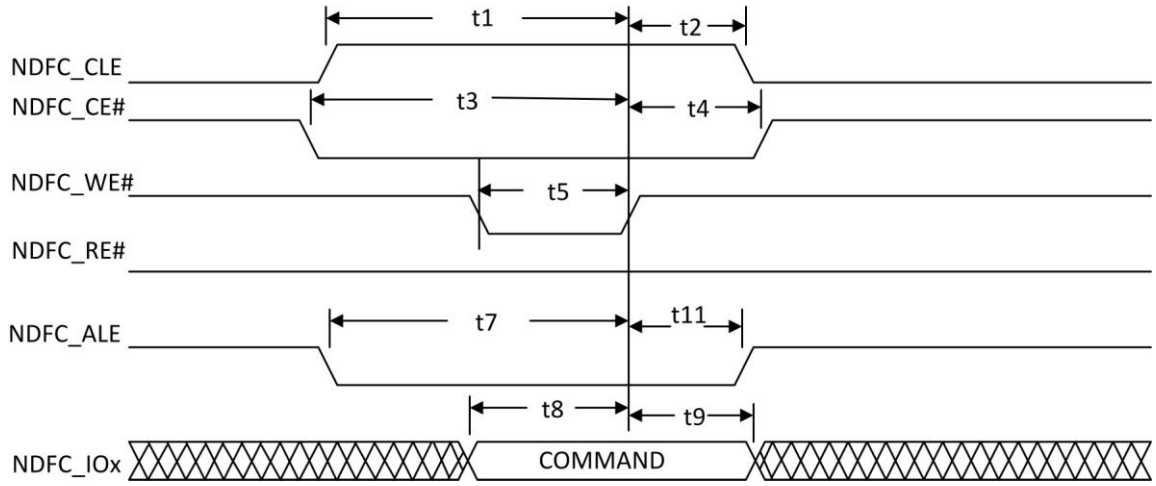



**Figure 5-14. Command Latch Cycle Timing**

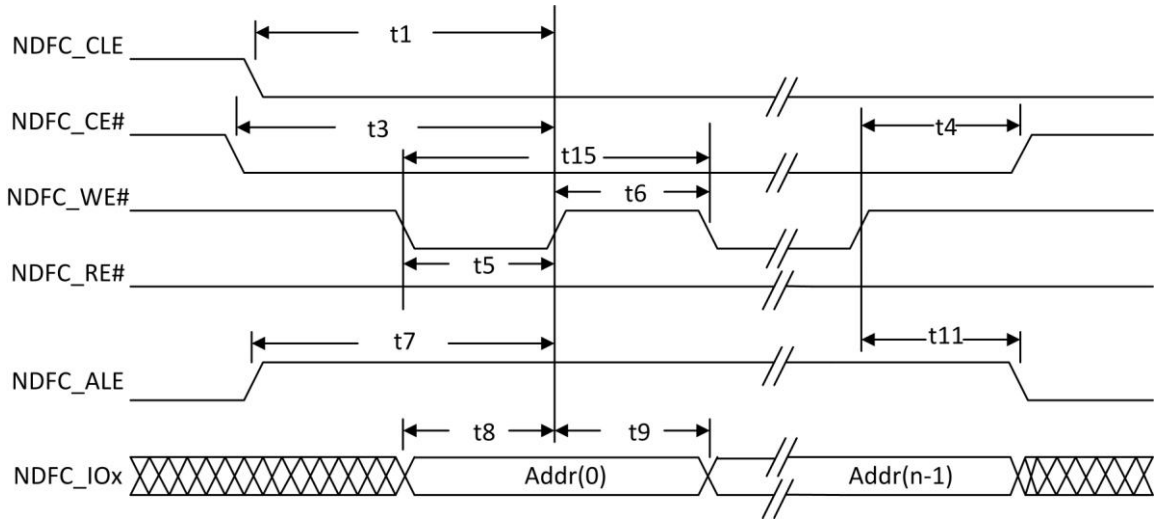



**Figure 5-15. Address Latch Cycle Timing**

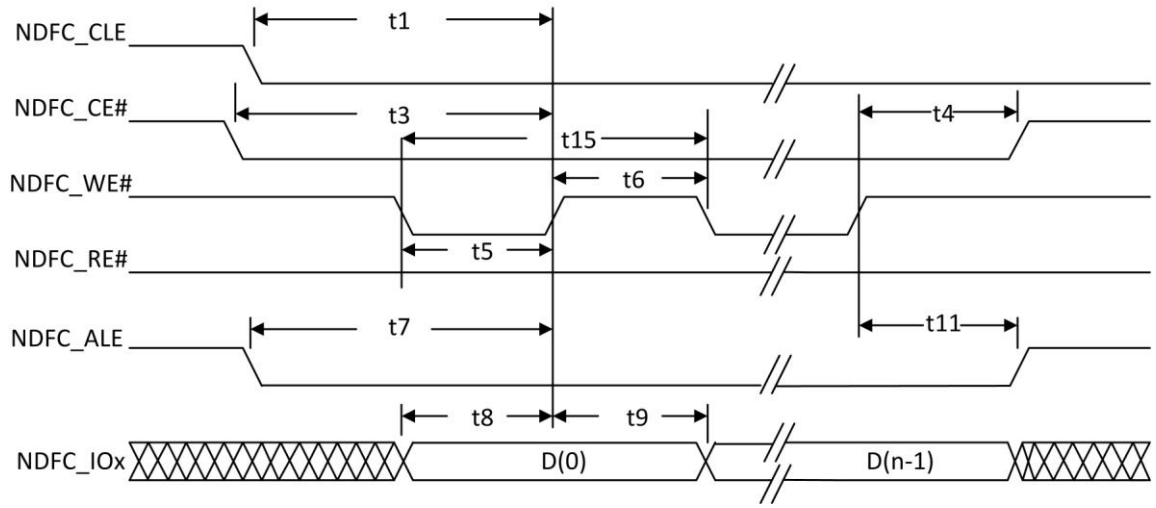



**Figure 5-16. Write Data to Flash Cycle Timing**

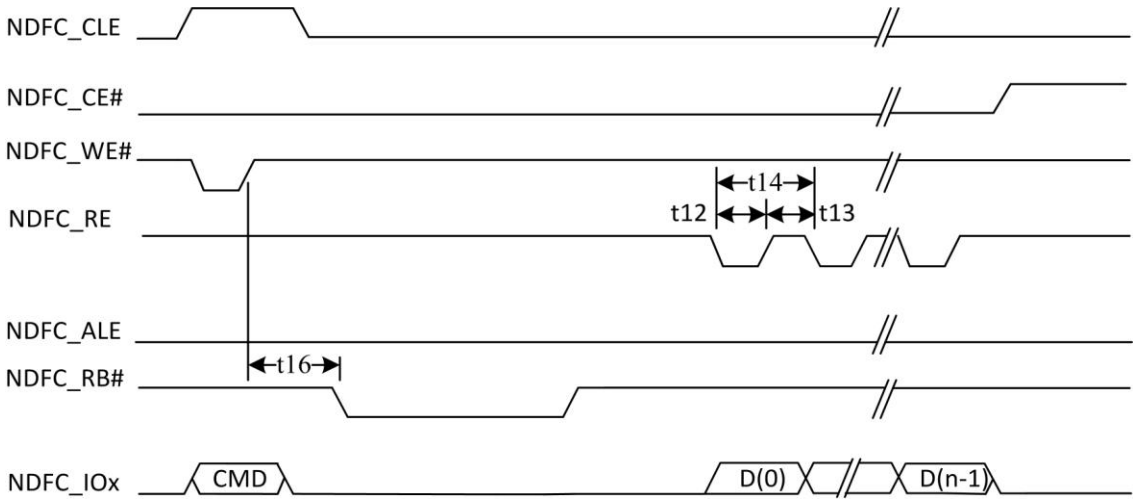



**Figure 5-17. Waiting R/B# Ready Timing**

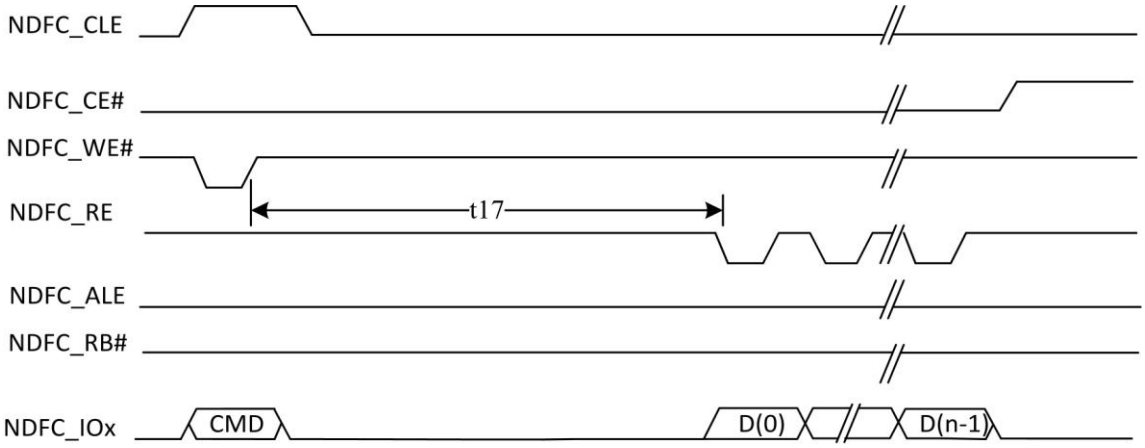



**Figure 5-18. WE# High to RE# Low Timing**

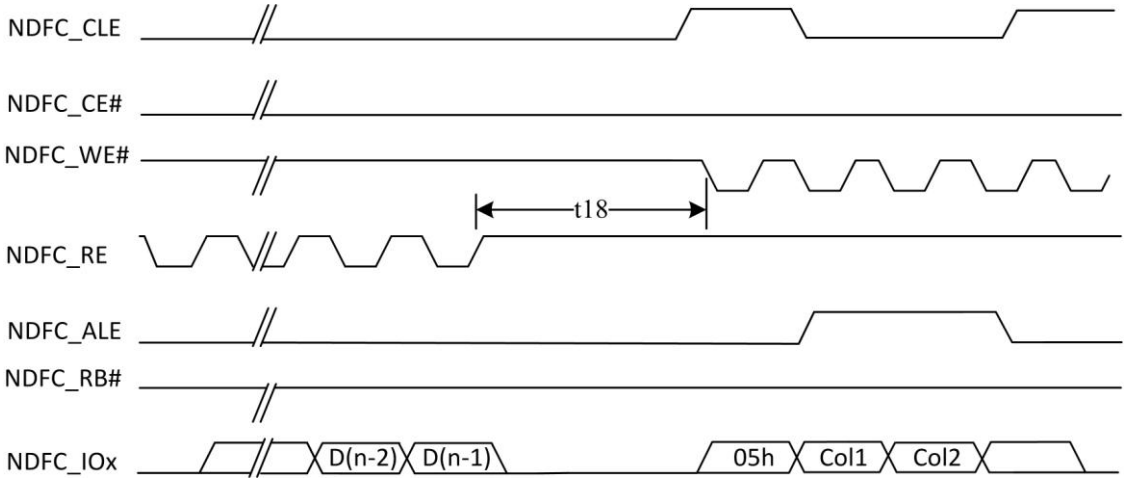



**Figure 5-19. RE# High to WE# Low Timing**

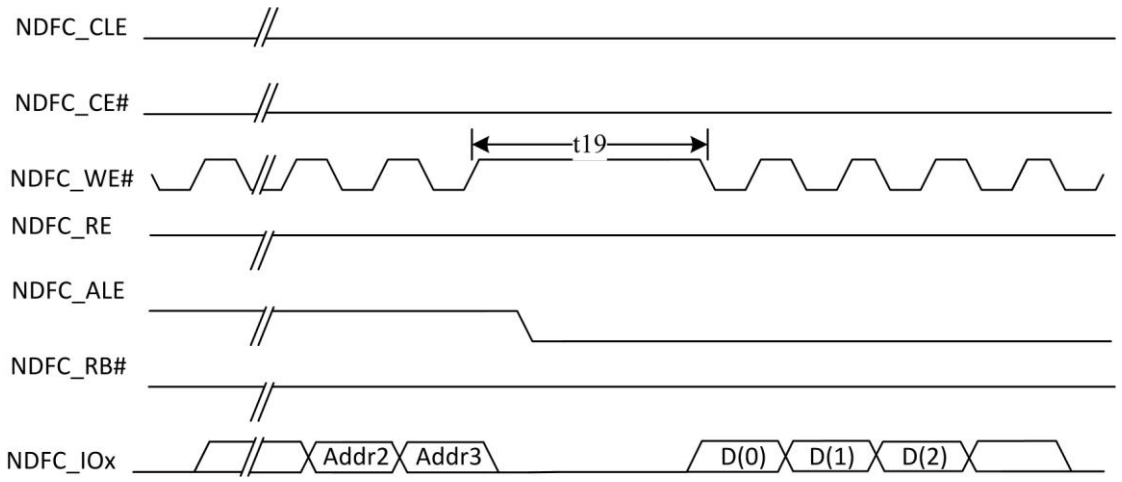



**Figure 5-20. Address to Data Loading Timing**

**Table 5-33. NAND Timing Constants**

| Parameter | Symbol | Timing | Unit |
|---|---|---|---|
| NDFC_CLE setup time | t1 | 2T | ns |
| NDFC_CLE hold time | t2 | 2T | ns |
| NDFC_CE setup time | t3 | 2T | ns |
| NDFC_CE hold time | t4 | 2T | ns |
| NDFC_WE# pulse width | t5 | T[1] | ns |
| NDFC_WE# hold time | t6 | T | ns |
| NDFC_ALE setup time | t7 | 2T | ns |
| Data setup time | t8 | T | ns |
| Data hold time | t9 | T | ns |
| Ready to NDFC_RE# low | t10 | 3T | ns |
| NDFC_ALE hold time | t11 | 2T | ns |
| NDFC_RE# pulse width | t12 | T | ns |
| NDFC_RE# hold time | t13 | T | ns |
| Read cycle time | t14 | 2T | ns |
| Write cycle time | t15 | 2T | ns |
| NDFC_WE# high to R/B# busy | t16 | T_WB[2] | ns |
| NDFC_WE# high to NDFC_RE# low | t17 | T_WHR[3] | ns |
| NDFC_RE# high to NDFC_WE# low | t18 | T_RHW[4] | ns |
| Address to data loading time | t19 | T_ADL[5] | ns |
| The following values are configurable in Nand Flash controller.<br>(1) T is the cycle of clock.<br>(2) The value of T_WB could be 14*2T/22*2T/30*2T/38*2T.<br>(3) The value of T_WHR could be 8*2T/16*2T/24*2T/32*2T.<br>(4) The value of T_RHW could be 4*2T/8*2T/12*2T/20*2T.<br>(5) The value of T_ADL could be 0*2T/8*2T/16*2T/24*2T. | | | |

## 5.11.3. SMHC AC Electrical Characteristics

### 5.11.3.1. SMHC0 and SMHC3

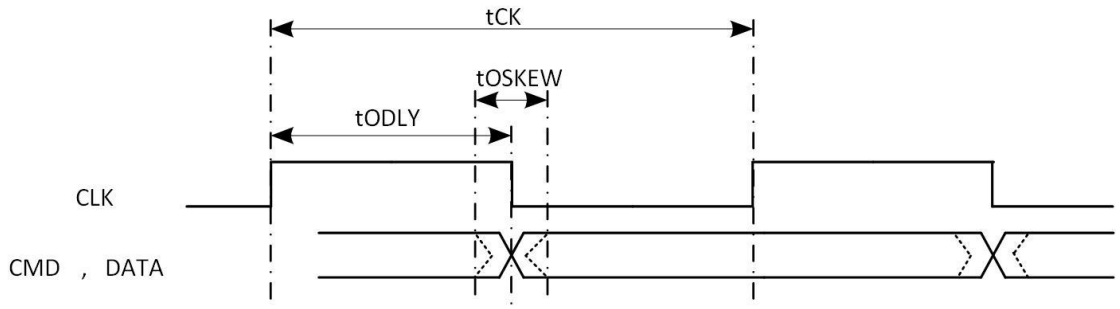



**Figure 5-21. SMHC0/3 SDR Mode Output Timing**

**Table 5-34. SMHC0/3 SDR Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI[1] |
| Data output delay skew time | tOSKEW | - | - | 2.0 | ns |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz.<br>(2) The GPIO's driver strength level is 2 for test. | | | | | |

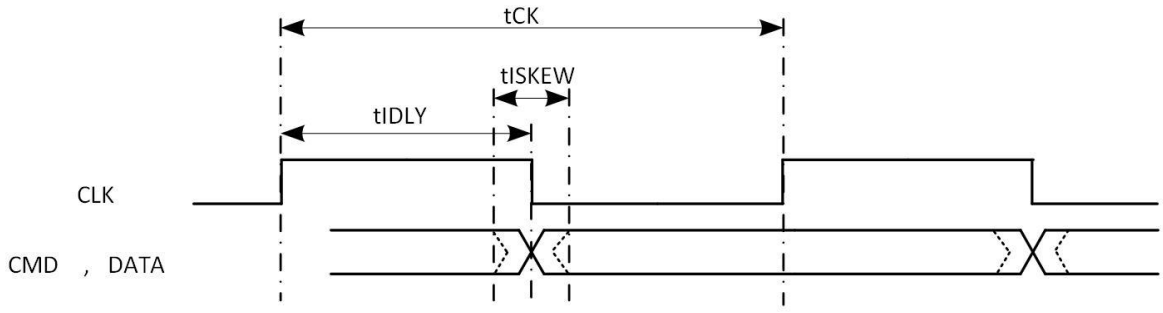



**Figure 5-22. SMHC0/3 SDR Mode Input Timing**

**Table 5-35. SMHC0/3 SDR Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Input CMD, DATA(referenced to CLK 50MHz)** | | | | | |
| Data input delay in SDR mode. It includes clock's PCB delay time, data's PCB delay time and device's data output delay | tIDLY | - | - | 20 | ns |
| Data input skew time in SDR mode | tISKEW | - | - | 2.0 | ns |
| (1) The GPIO's driver strength level is 2 for test. | | | | | |

#### 5.11.3.2. SMHC1

**(1) SDR Mode**

It is used for DS,HS(<100MHz).

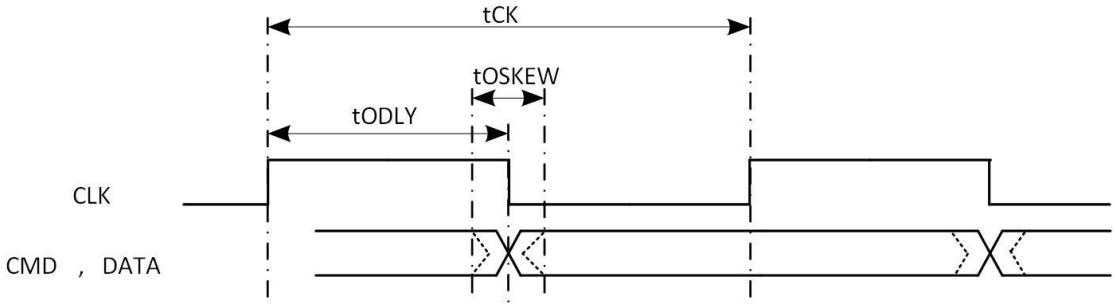



**Figure 5-23. SMHC1 SDR Mode Output Timing**

**Table 5-36. SMHC1 SDR Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI[1] |
| Data output delay skew time | tOSKEW | - | - | 1.33 | ns |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz.<br>(2) The GPIO's driver strength level is 2 for test. | | | | | |

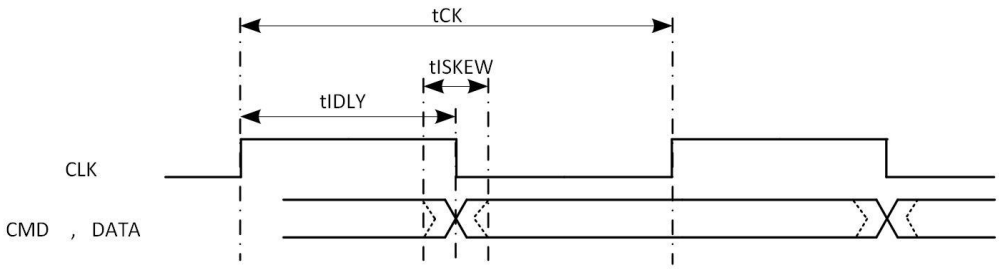



**Figure 5-24. SMHC1 SDR Mode Input Timing**

**Table 5-37. SMHC1 SDR Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Input CMD, DATA(referenced to CLK 50MHz)** | | | | | |
| Data input delay in SDR mode. It includes clock's PCB delay time, data's PCB delay time and device's data output delay | tIDLY | - | - | 20 | ns |
| Data input skew time in SDR mode | tISKEW | - | - | 1.33 | ns |
| (1) The GPIO's driver strength level is 2 for test. | | | | | |

**(2) DDR50 Mode**

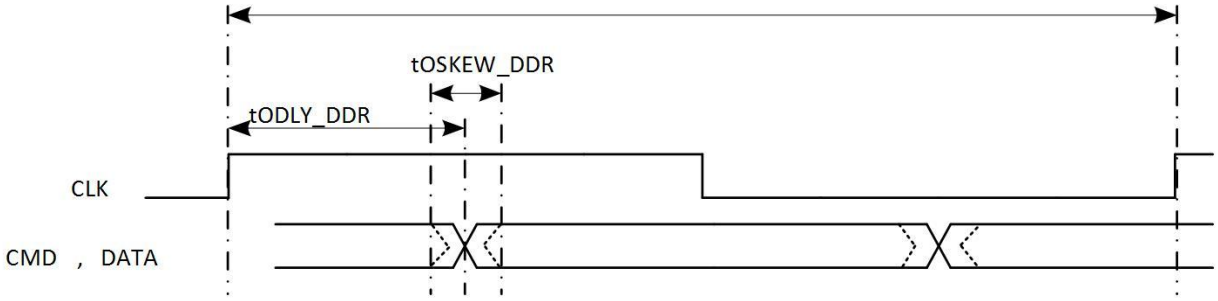



**Figure 5-25. SMHC1 DDR50 Mode Output Timing**

**Table 5-38. SMHC1 DDR50 Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time in DDR mode | tODLY_DDR | - | 0.25 | 0.25 | UI[1] |
| Data output delay skew time | tOSKEW_DDR | - | - | 1.33 | ns |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz.<br>(2) The GPIO's driver strength level is 2 for test. | | | | | |

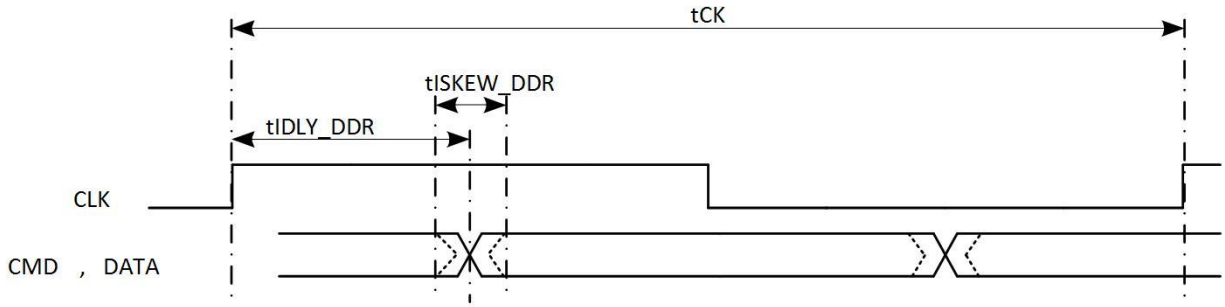



**Figure 5-26. SMHC1 DDR50 Mode Input Timing**

**Table 5-39. SMHC1 DDR50 Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Input CMD, DATA(referenced to CLK 50MHz)** | | | | | |
| Data input delay in DDR mode. It includes clock's PCB delay time, data's PCB delay time and device's data output delay | tIDLY_DDR | 8.55 | - | 22.95 | ns |
| Data input skew time in DDR mode | tISKEW_DDR | - | - | 2 | ns |
| (1) The GPIO's driver strength level is 2 for test. | | | | | |

**(3) SDR104 Mode(>100MHz)**

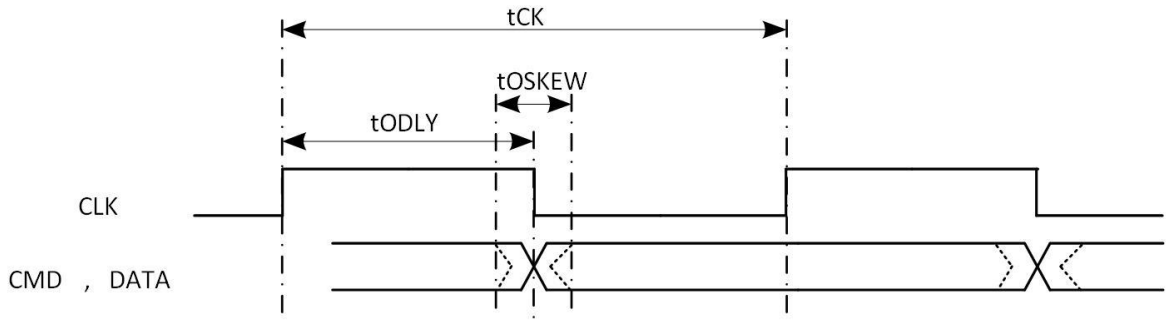



**Figure 5-27. SMHC1 SDR104 Mode Output Timing**

**Table 5-40. SMHC1 SDR104 Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | - | 150 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI[1] |
| Data output delay skew time | tOSKEW | - | - | 1.33 | ns |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz.<br>(2) The GPIO's driver strength level is 2 for test. | | | | | |

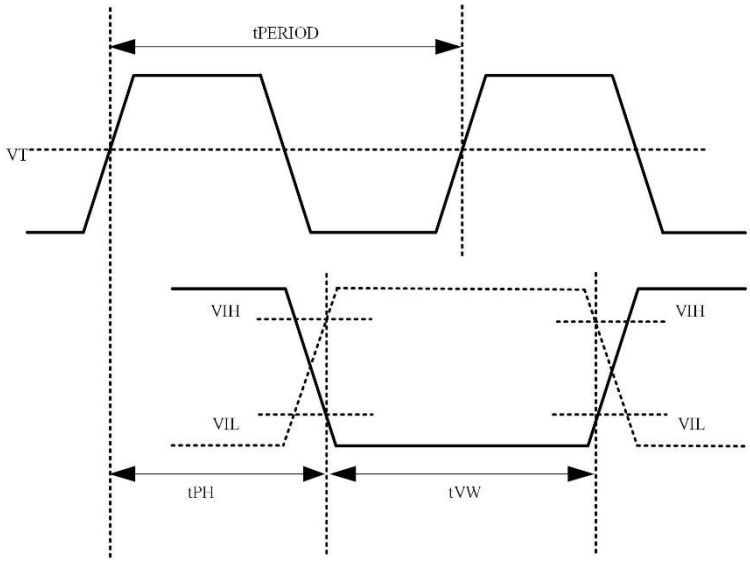



**Figure 5-28. SMHC1 SDR104 Mode Input Timing**

**Table 5-41. SMHC1 SDR104 Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock period | tPERIOD | 6.66 | - | - | ns |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Rise time, fall time | tTLH, tTHL | - | - | 0.2 | UI[1] |
| **Input CMD, DATA(referenced to CLK)** | | | | | |
| Input delay | tPH | 0 | - | 2 | UI[1] |
| Input delay variation due to temperature change after tuning | dPH | -350[3] | - | 1550[4] | ps |
| CMD, Data valid window | tVW | 0.575 | - | - | UI[1] |

(1) Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz.
(2) The GPIO's driver strength level is 3 for test.
(3) Temperature variation: -20°C
(4) Temperature variation: 90°C

#### 5.11.3.3. SMHC2

**(1) HS-SDR/HS-DDR Mode**

The IO voltage is 1.8V or 3.0V.

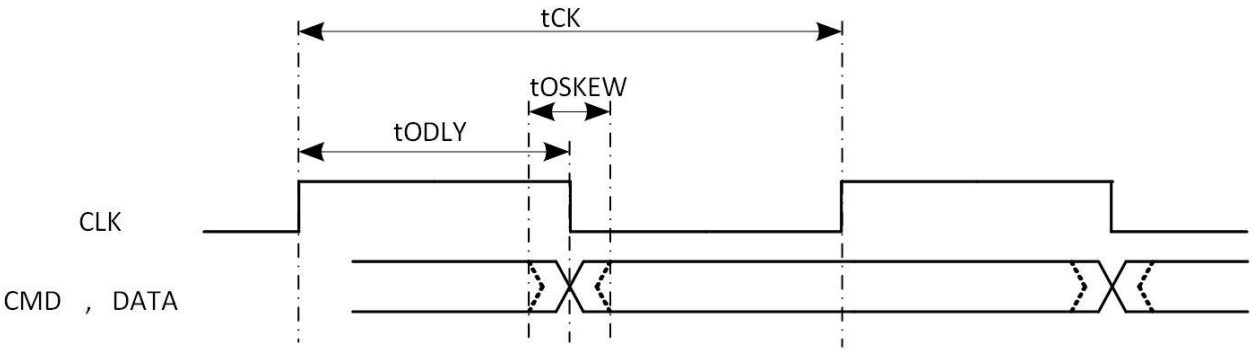



**Figure 5-29. SMHC2 HS-SDR Mode Output Timing**

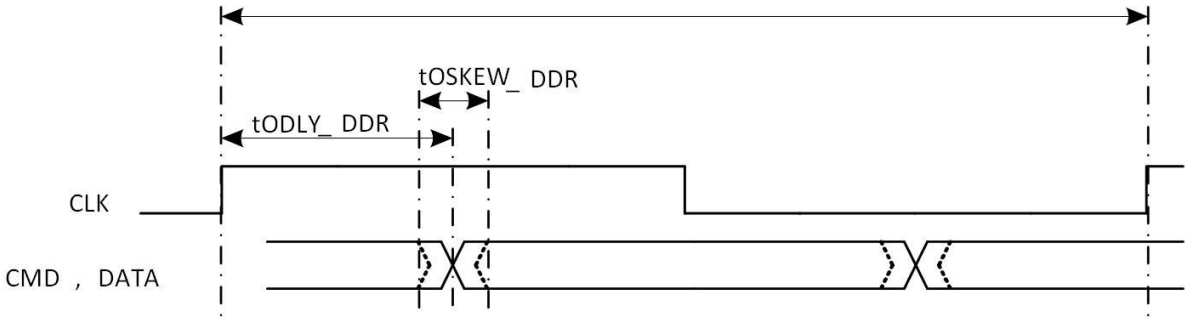



**Figure 5-30. SMHC2 HS-DDR Mode Output Timing**

**Table 5-42. SMHC2 HS-SDR/HS-DDR Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI[1] |
| CMD, Data output delay time in DDR mode | tODLY_DDR | - | 0.25 | 0.25 | UI[1] |
| Data output delay skew time | tOSKEW | - | - | 1.33 | ns |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz.<br>(2) The GPIO's driver strength level is 2 for test. | | | | | |

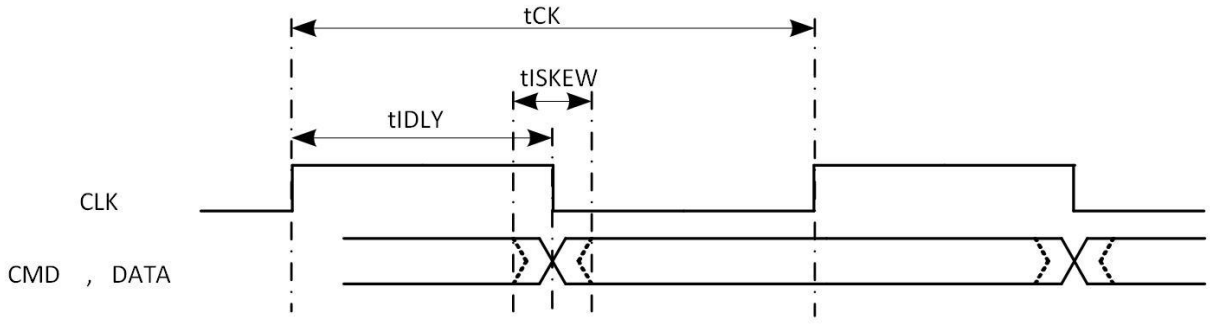



**Figure 5-31. SMHC2 HS-SDR Mode Input Timing**

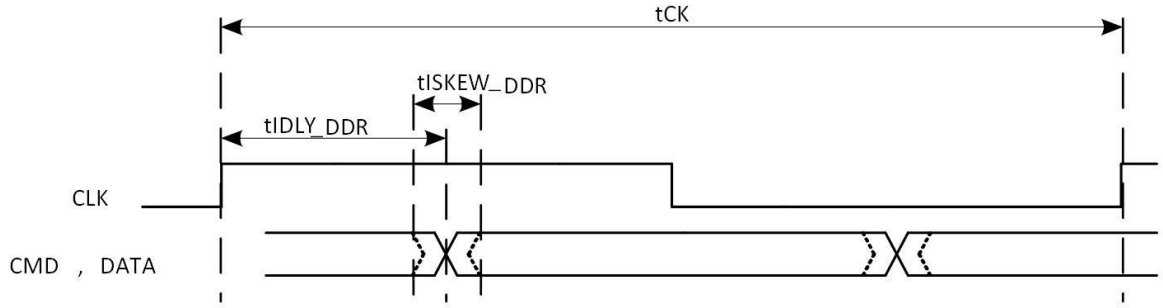



**Figure 5-32. SMHC2 HS-DDR Mode Input Timing**

**Table 5-43. SMHC2 HS-SDR/HS-DDR Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| **Input CMD, DATA(referenced to CLK 50MHz)** | | | | | |
| Data input delay in SDR mode. It includes clock's PCB delay time, data's PCB delay time and device's data output delay | tIDLY | - | - | 20 | ns |
| Data input delay in DDR mode. It includes clock's PCB delay time, data's PCB delay time and device's data output delay | tIDLY_DDR | - | - | 24.4 | ns |
| Data input skew time in SDR mode | tISKEW | - | - | 1.33 | ns |
| Data input skew time in DDR mode | tISKEW_DDR | - | - | 1.33 | ns |
| (1) The GPIO's driver strength level is 2 for test. | | | | | |

**(2) HS200 Mode**

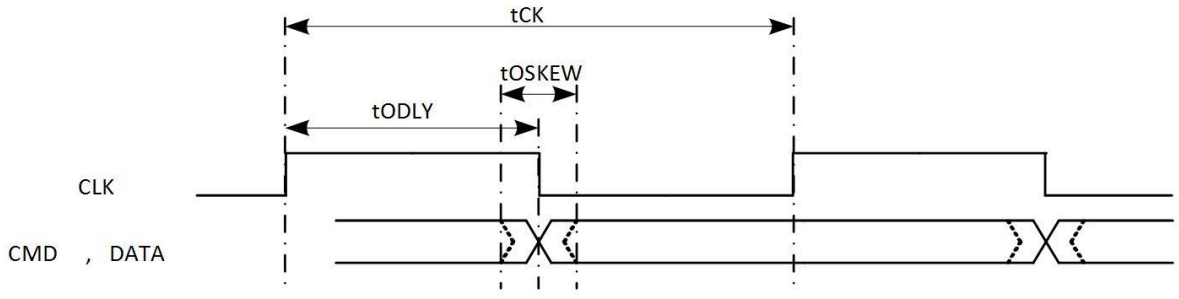



**Figure 5-33. SMHC2 HS200 Mode Output Timing**

**Table 5-44. SMHC2 HS200 Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | - | - | TBD | MHz |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Rise time, fall time | tTLH, tTHL | - | - | 0.2 | UI[1] |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI[1] |
| Data output delay skew time | tOSKEW | - | - | 1.33 | ns |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz.<br>(2) The GPIO's driver strength level is 3 for test. | | | | | |

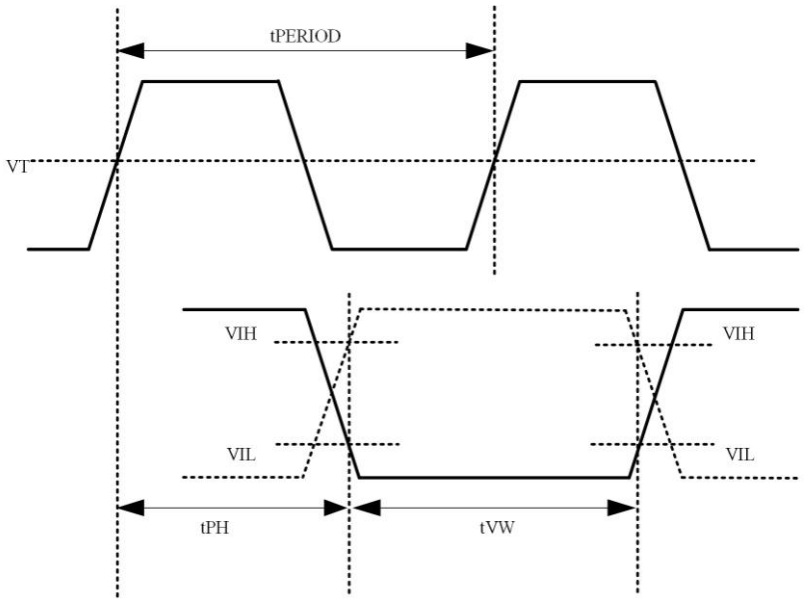



**Figure 5-34. SMHC2 HS200 Mode Input Timing**

**Table 5-45. SMHC2 HS200 Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock period | tPERIOD | TBD | - | - | ns |
| Duty cycle | DC | 45 | 50 | 55 | % |
| Rise time, fall time | tTLH, tTHL | - | - | 0.2 | UI[1] |
| **Input CMD, DATA(referenced to CLK)** | | | | | |
| Input delay | tPH | 0 | - | 2 | UI[1] |
| Input delay variation due to temperature change after tuning | dPH | -350[2] | - | 1550[3] | ps |
| CMD, Data valid window | tVW | 0.575 | - | - | UI[1] |
| (1) Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz.<br>(2) Temperature variation: -20°C.<br>(3) Temperature variation: 90°C.<br>(4) The GPIO's driver strength level is 3 for test. | | | | | |

**(3) HS400 Mode**

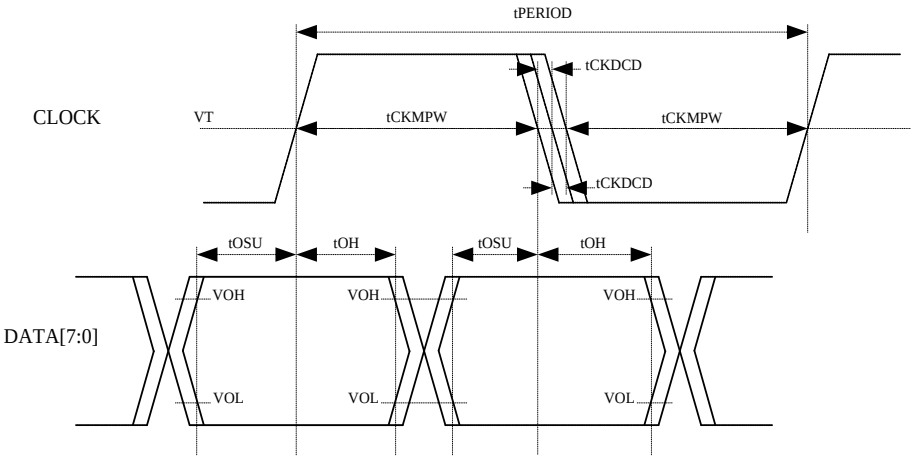



**Figure 5-35. SMHC2 HS400 Mode Output Timing**

**Table 5-46. SMHC2 HS400 Mode Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock period | tPERIOD | 10 | - | - | ns |
| Clock slew rate | SR | 1.125 | - | - | V/ns |
| Clock duty cycle distortion | tCKDCD | 0 | - | 0.5 | ns |
| Clock minimum pulse width | tCKMPW | 2.2 | - | - | ns |
| **Output DATA(referenced to CLK)** | | | | | |
| Data output setup time | tOSU | 0.4 | - | - | ns |
| Data output hold time | tOH | 0.4 | - | - | ns |
| Data output slew rate | SR | 0.9 | - | - | ns |
| (1) The GPIO's driver strength level is 3 for test. | | | | | |

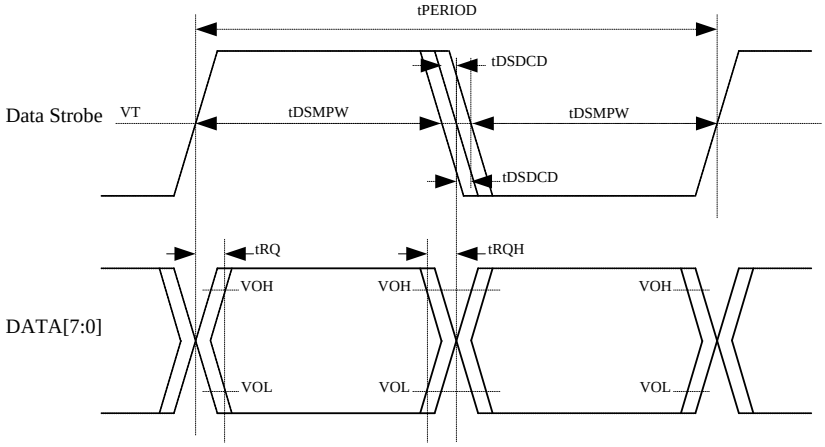



**Figure 5-36. SMHC2 HS400 Mode Input Timing**

**Table 5-47. SMHC2 HS400 Mode Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| DS period | tPERIOD | 10 | - | - | ns |
| DS slew rate | SR | 1.125 | - | - | V/ns |
| DS duty cycle distortion | tDSDCD | 0.0 | - | 0.4 | ns |
| DS minimum pulse width | tDSMPW | 2.0 | - | - | ns |
| **Input DATA(referenced to CLK)** | | | | | |

| | | | | | |
|---|---|---|---|---|---|
| Data input skew | tRQ | - | - | 0.4 | ns |
| Data input hold skew | tRQH | - | - | 0.4 | ns |
| Data input slew rate | SR | 0.85 | - | - | V/ns |
| (1) The GPIO's driver strength level is 3 for test. | | | | | |

# 5.12. External Peripherals Electrical Characteristics

## 5.12.1. LCD AC Electrical Characteristics

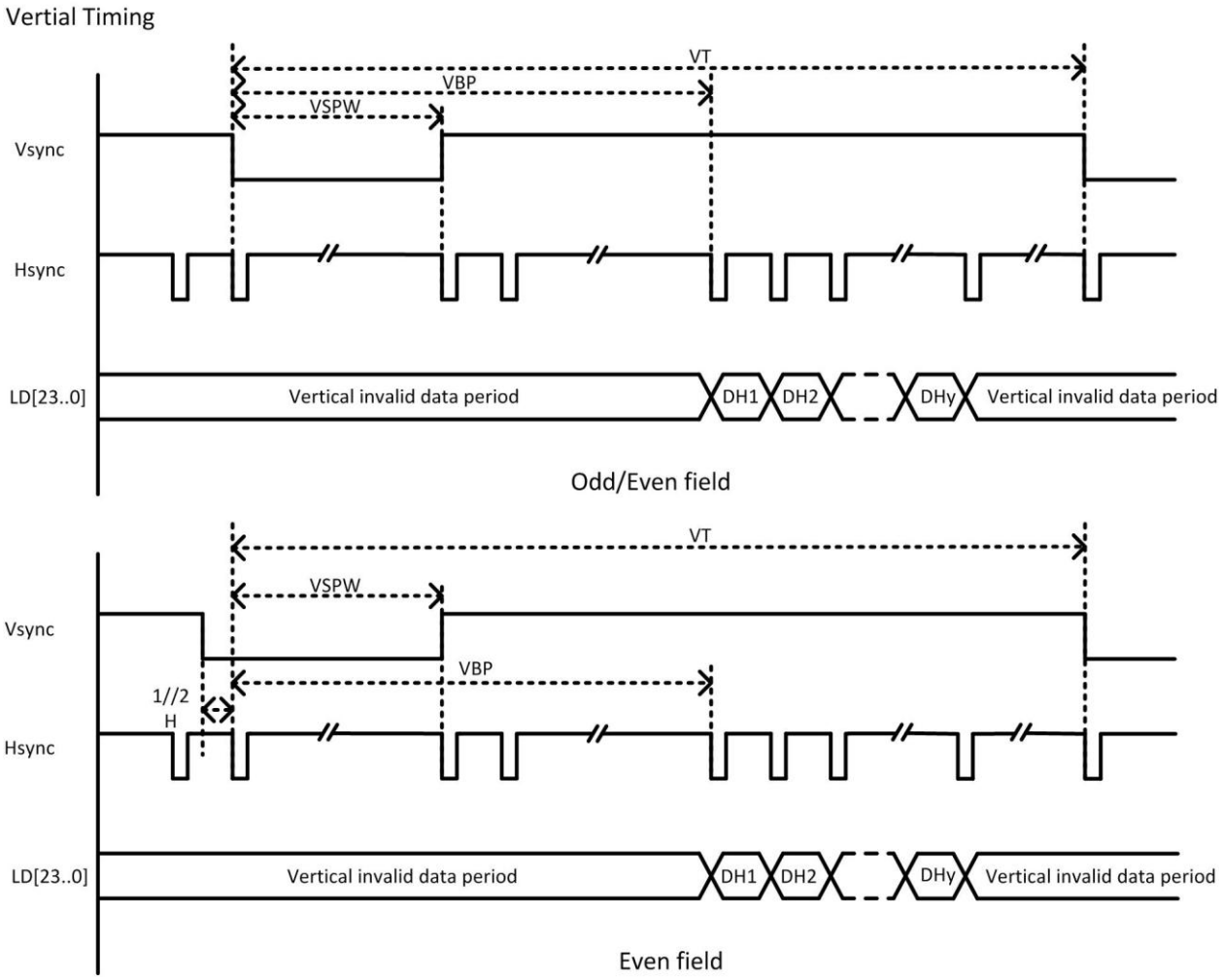



**Figure 5-37. HV_IF Interface Vertical Timing**

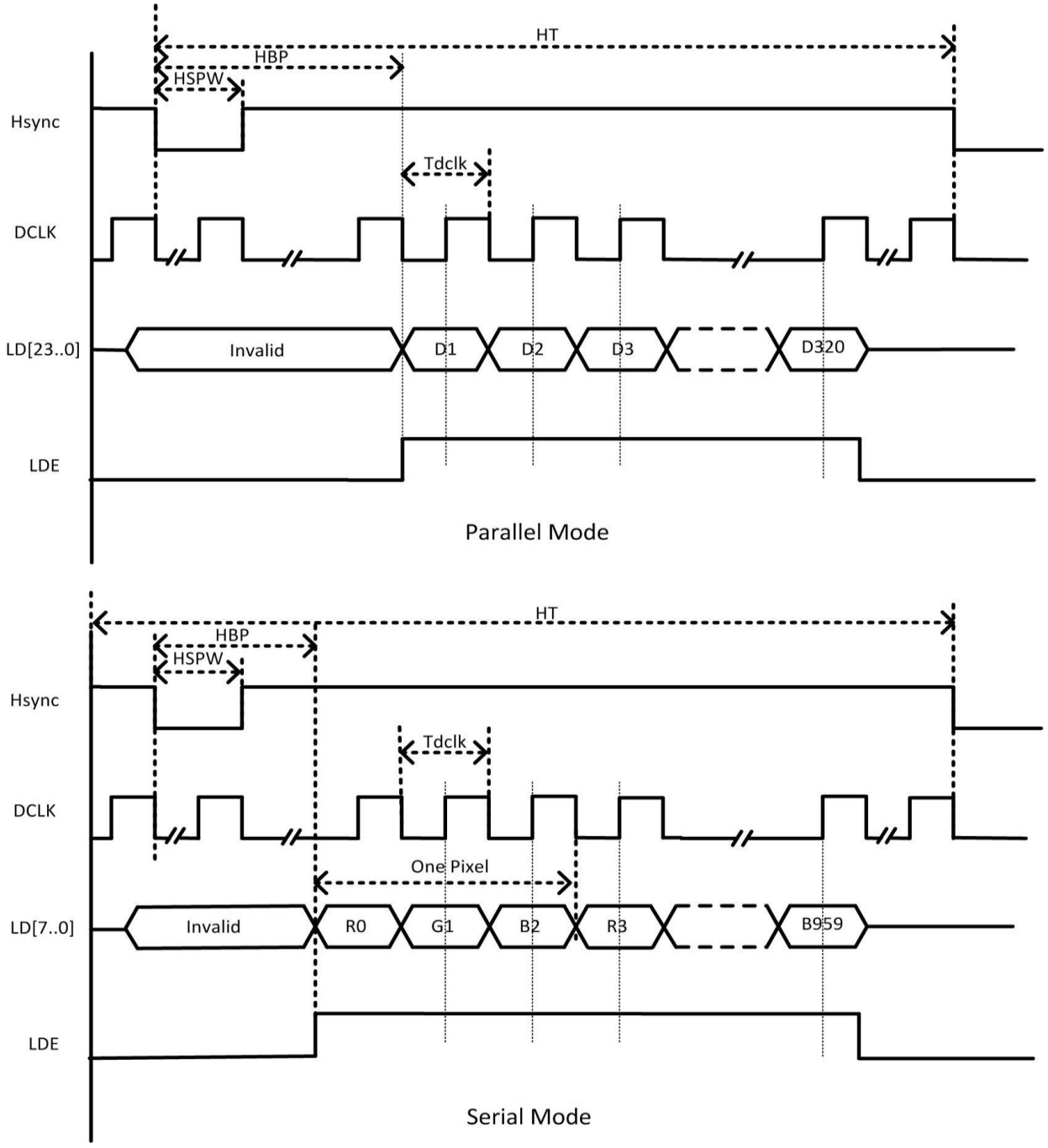



**Figure 5-38. HV_IF Interface Horizontal Timing**

**Table 5-48. LCD HV_IF Interface Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DCLK cycle time | tDCLK | 5 | - | - | ns |
| Hsync period time | tHT | - | HT+1 | - | tDCLK |
| Hsync width | tHSPW | - | HSPW+1 | - | tDCLK |
| Hsync back porch | tHBP | - | HBP+1 | - | tDCLK |
| Vsync period time | tVT | - | VT/2 | - | tHT |
| Vsync width | tVSPW | - | VSPW+1 | - | tHT |
| Vsync back porch | tVBP | - | VBP+1 | - | tHT |
| (1) Vsync: Vertical sync, indicates one new frame.<br>(2) Hsync: Horizontal sync, indicate one new scan line.<br>(3) DCLK: Dot clock, pixel data are sync by this clock.<br>(4) LDE: LCD data enable. | | | | | |

(5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

### 5.12.2. CSI AC Electrical Characteristics

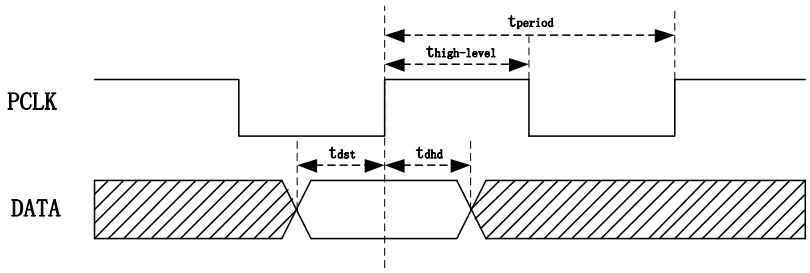



**Figure 5-39. CSI Data Sample Timing**

**Table 5-49. CSI Interface Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Pclk period | $t_{period}$ | 6.7 | - | - | ns |
| Pclk frequency | $1/t_{period}$ | - | - | 148.5 | MHz |
| Pclk duty | $t_{high-level}/t_{period}$ | 40 | 50 | 60 | % |
| Data input setup time | $t_{dst}$ | 0.6 | - | - | ns |
| Data input hold time | $t_{dhd}$ | 0.6 | - | - | ns |

### 5.12.3. EMAC AC Electrical Characteristics

#### 5.12.3.1. MII

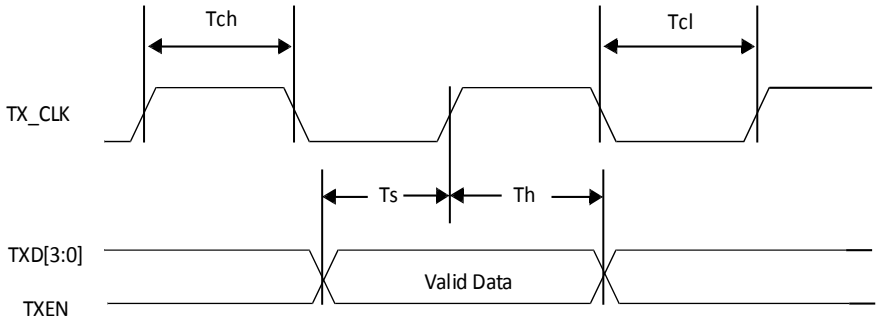



**Figure 5-40. MII Interface Transmit Timing**

**Table 5-50. MII Transmit Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transmit clock high time,100MHz mode | Tch | 40 | - | 40 | ns |
| Transmit clock low time,100MHz mode | Tcl | 40 | - | 40 | ns |
| TXEN/TXD setup time to TX_CLK | Ts | 10 | - | - | ns |
| TXEN/TXD hold time to TX_CLK | Th | 10 | - | - | ns |

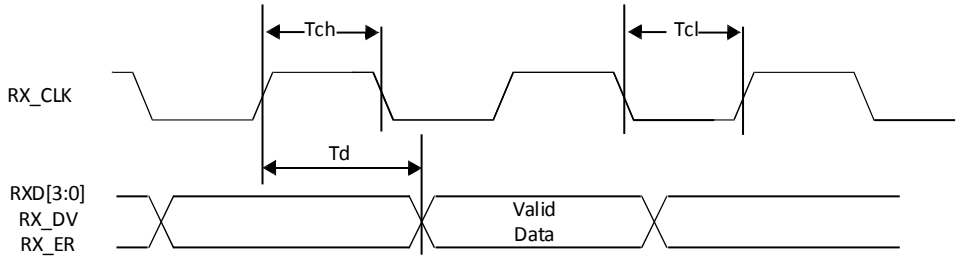



**Figure 5-41. MII Interface Receive Timing**

**Table 5-51. MII Receive Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Receive clock high time,100MHz mode | Tch | 40 | - | 40 | ns |
| Receive clock low time,100MHz mode | Tcl | 40 | - | 40 | ns |
| RX_CLK to RXD[3:0]/RX_DV/RX_ER Delay | Td | 10 | - | 30 | ns |

### 5.12.3.2. RMII

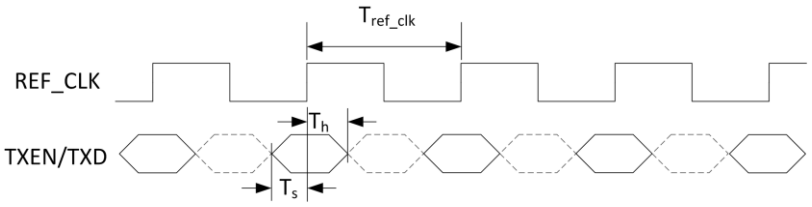



**Figure 5-42. RMII Interface Transmit Timing**

**Table 5-52. RMII Transmit Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Reference clock period | $T_{ref\_clk}$ | - | 20 | - | ns |
| TXD/TXEN to REF_CLK setup time | Ts | 4 | - | - | ns |
| TXD/TXEN to REF_CLK hold time | Th | 2 | - | - | ns |

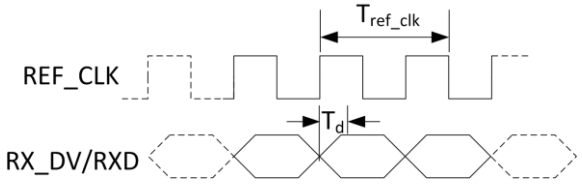



**Figure 5-43. RMII Interface Receive Timing**

**Table 5-53. RMII Receive Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Reference clock period | $T_{ref\_clk}$ | - | 20 | - | ns |
| REF_CLK rising edge to RX_DV/RXD | Td | - | 10 | 12 | ns |

### 5.12.3.3. RGMII

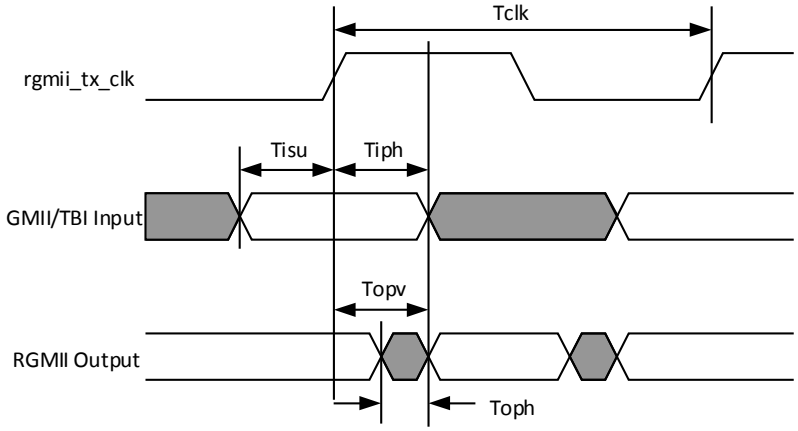



**Figure 5-44. RGMII Interface Transmit Timing**

**Table 5-54. RGMII Transmit Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| rgmii_tx_clk clock period | Tclk | 8 | - | DC | ns |
| RGMII/TBI input set up prior to rgmii_tx_clk | Tisu | 2.8 | - | - | ns |
| RGMII/TBI input data hold after rgmii_tx_clk | Tiph | 0.1 | - | - | ns |
| RGMII output data valid after rgmii_tx_clk | Topv | - | - | 0.85 | ns |
| RGMII output data hold after rgmii_tx_clk | Toph | 0 | - | - | ns |

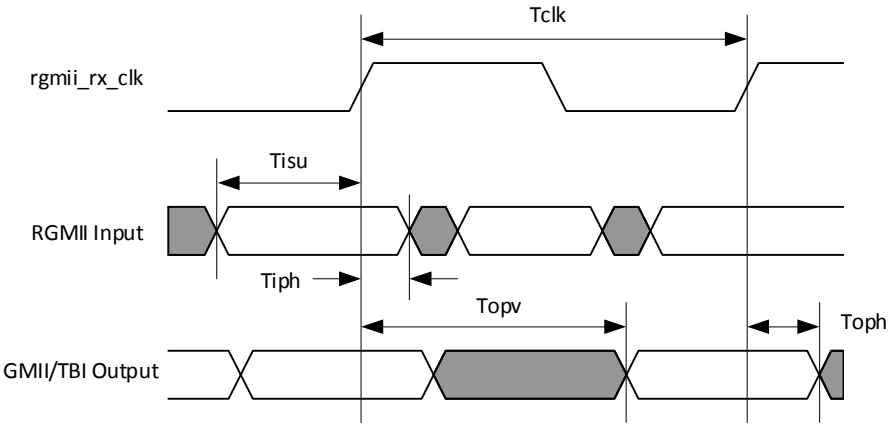



**Figure 5-45. RGMII Interface Receive Timing**

**Table 5-55. RGMII Receive Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| rgmii_rx_clk clock period | Tclk | 8 | - | DC | ns |
| RGMII input set up prior to rgmii_rx_clk | Tisu | 2.6 | - | - | ns |
| RGMII input data hold after rgmii_rx_clk | Tiph | 0.8 | - | - | ns |
| GMII/TBI input data valid after rgmii_rx_clk | Topv | - | - | 5.2 | ns |
| GMII output data hold after rgmii_rx_clk<br>TBI output data hold after rgmii_rx_clk | Toph | 0.1<br>0.5 | - | - | ns |

### 5.12.4. CIR-RX AC Electrical Characteristics

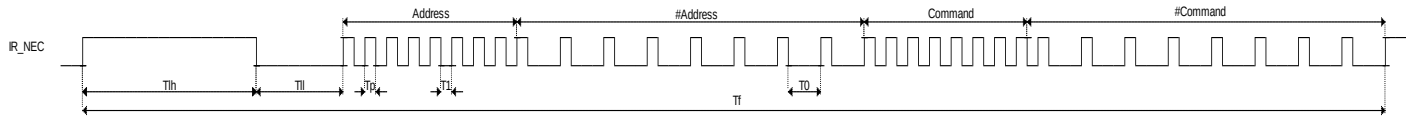



**Figure 5-46. CIR-RX Timing**

**Table 5-56. CIR-RX Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frame period | Tf | - | 67.5 | - | ms |
| Lead code high time | Tlh | - | 9 | - | ms |
| Lead code low time | Tll | - | 4.5 | - | ms |
| Pulse time | Tp | - | 560 | - | us |
| Logical 1 low time | T1 | - | 1680 | - | us |
| Logical 0 low time | T0 | - | 560 | - | us |

### 5.12.5. SPI AC Electrical Characteristics

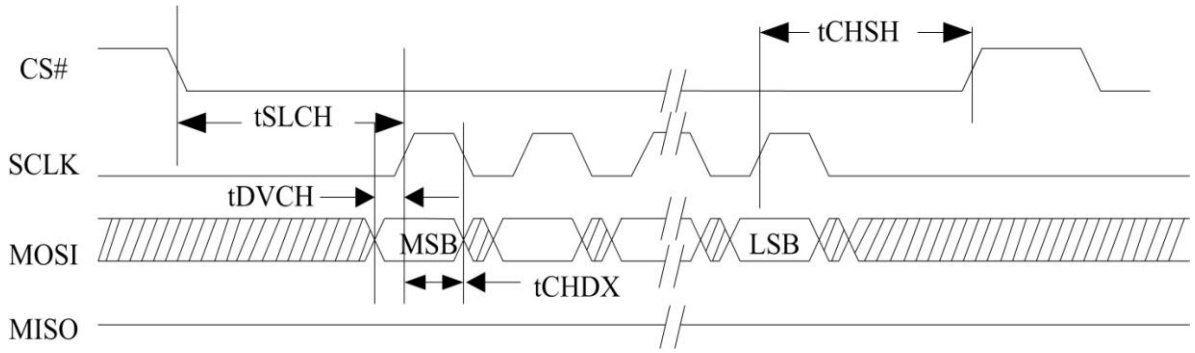



**Figure 5-47. SPI MOSI Timing**

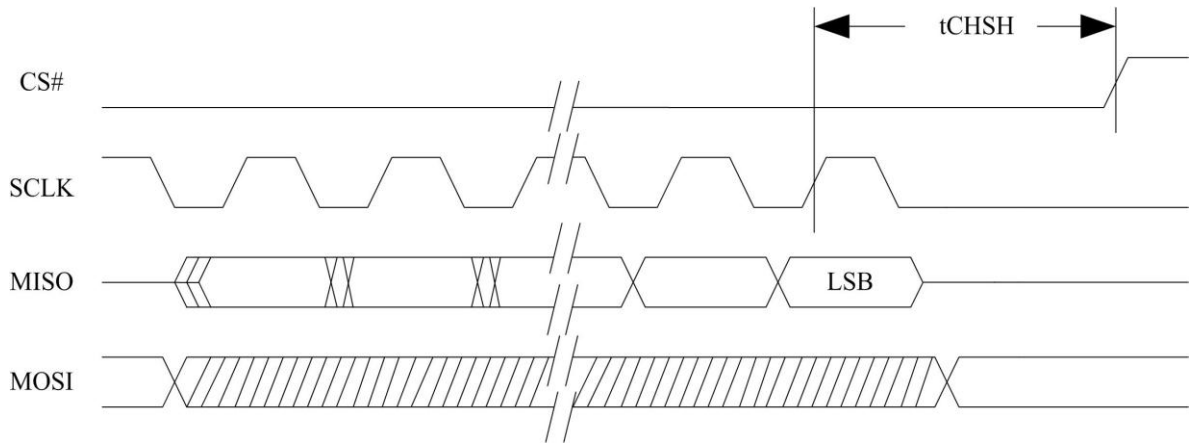



**Figure 5-48. SPI MISO Timing**

**Table 5-57. SPI Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CS# active setup time | tSLCH | - | 2T[1] | - | ns |
| CS# active hold time | tCHSH | - | 2T[1] | - | ns |

| | | | | | |
|---|---|---|---|---|---|
| Data in setup time | tDVCH | - | T[1]/2-3 | - | ns |
| Data in hold time | tCHDX | - | T[1]/2-3 | - | ns |
| (1) T is the cycle of clock. | | | | | |

## 5.12.6. UART AC Electrical Characteristics

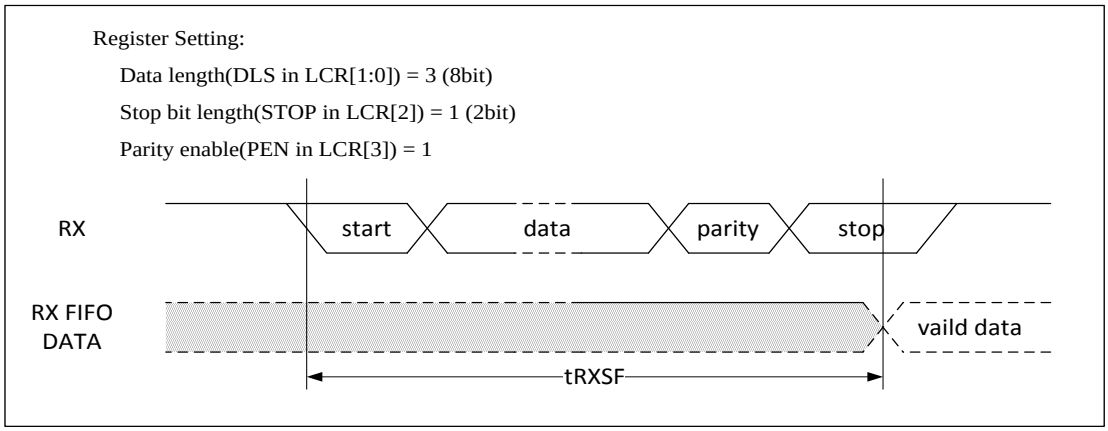



**Figure 5-49. UART RX Timing**

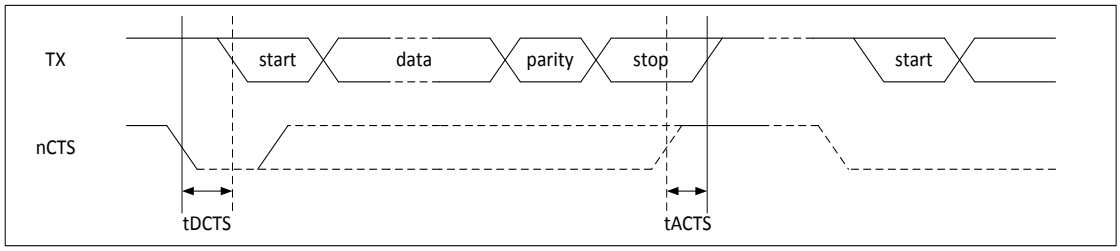



**Figure 5-50. UART nCTS Timing**

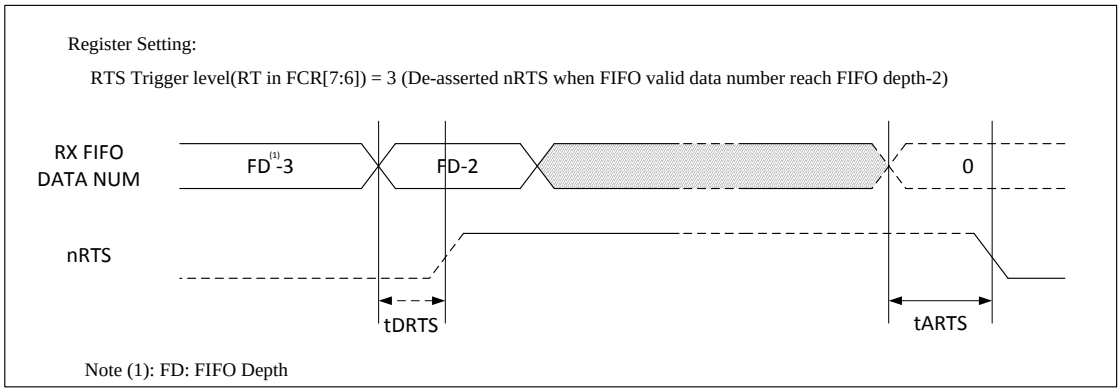



**Figure 5-51. UART nRTS Timing**

**Table 5-58. UART Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX start to RX FIFO | tRXSF | 10.5× BRP[1] | - | 11× BRP[1] | ns |
| Delay time of de-asserted nCTS to TX start | tDCTS | - | - | BRP[1] | ns |
| Step time of asserted nCTS to stop next transmission | tACTS | BRP[1]/4 | - | - | ns |

| | | | | | |
|---|---|---|---|---|---|
| Delay time of de-asserted nRTS | tDRTS | - | - | BRP[1] | ns |
| Delay time of asserted nRTS | tARTS | - | - | BRP[1] | ns |
| (1) BRP: Baud-Rate Period. | | | | | |

### 5.12.7. TWI AC Electrical Characteristics

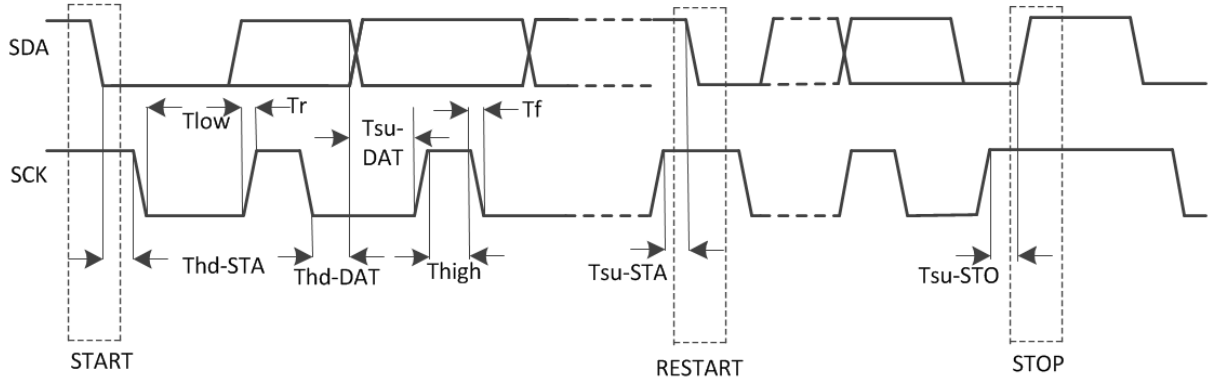



**Figure 5-52. TWI Timing**

**Table 5-59. TWI Timing Constants**

| Parameter | Symbol | Standard mode | | | Fast mode | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| SCK clock frequency | Fsck | 0 | - | 100 | 0 | - | 400 | kHz |
| Setup time in start | Tsu-STA | 4.7 | - | - | 0.6 | - | | us |
| Hold time in start | Thd-STA | 4.0 | - | - | 0.6 | - | | us |
| Setup time in data | Tsu-DAT | 250 | - | - | 100 | - | | ns |
| Hold time in data | Thd-DAT | 5.0 | - | - | - | - | | ns |
| Setup time in stop | Tsu-STO | 4.0 | - | - | 6.0 | - | - | us |
| SCK low level time | Tlow | 4.7 | - | - | 1.3 | - | - | us |
| SCK high level time | Thigh | 4.0 | - | - | 0.6 | - | - | ns |
| SCK/SDA falling time | Tf | - | - | 300 | 20 | - | 300 | ns |
| SCK/SDA rising time | Tr | - | - | 1000 | 20 | - | 300 | ns |

### 5.12.8. TSC AC Electrical Characteristics

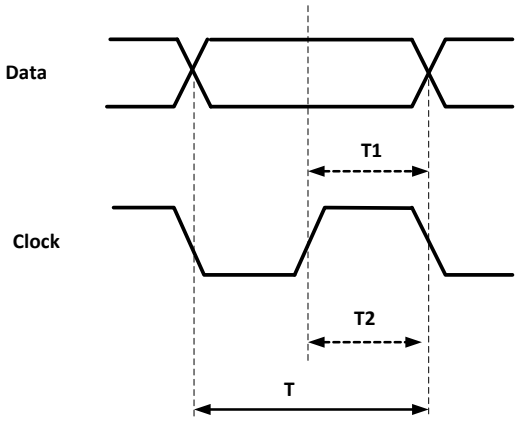



**Figure 5-53. TSC Data and Clock Timing**

**Table 5-60. TSC Timing Constants**

| Parameter | Symbol | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| Data hold time | T1 | $T^{[1]}/2-T^{[1]}/10$ | $T^{[1]}/2$ | $T^{[1]}/2+T^{[1]}/10$ | us |
| Clock pulse width | T2 | $T^{[1]}/2-T^{[1]}/10$ | $T^{[1]}/2$ | $T^{[1]}/2+T^{[1]}/10$ | us |
| (1) T is the cycle of clock. | | | | | |

## 5.12.9. I2S/PCM AC Electrical Characteristics

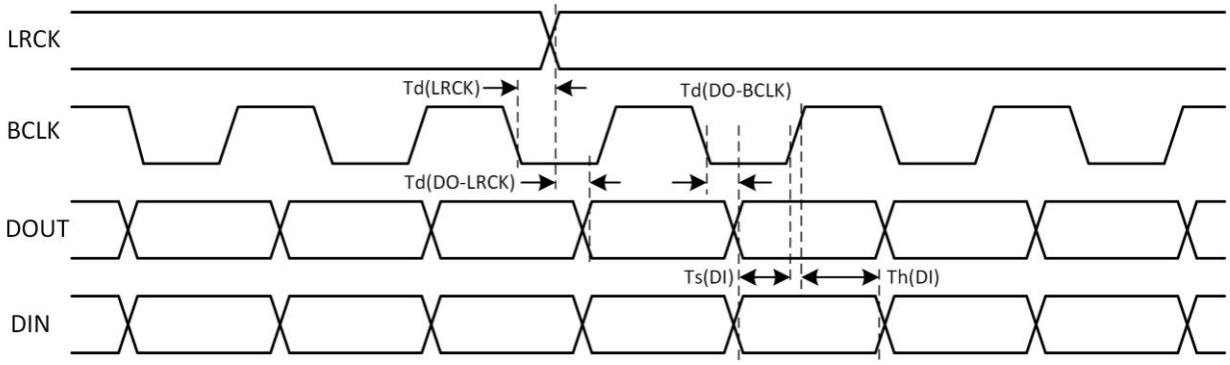



**Figure 5-54. I2S/PCM Timing in Master Mode**

**Table 5-61. I2S/PCM Timing Constants in Master Mode**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LRCK delay | Td(LRCK) | - | - | 10 | ns |
| LRCK to DOUT delay(For LJF) | Td(DO-LRCK) | - | - | 10 | ns |
| BCLK to DOUT delay | Td(DO-BCLK) | - | - | 10 | ns |
| DIN setup | Ts(DI) | 4 | - | - | ns |
| DIN hold | Th(DI) | 4 | - | - | ns |
| BCLK rise time | Tr | - | - | 8 | ns |
| BCLK fall time | Tf | - | - | 8 | ns |

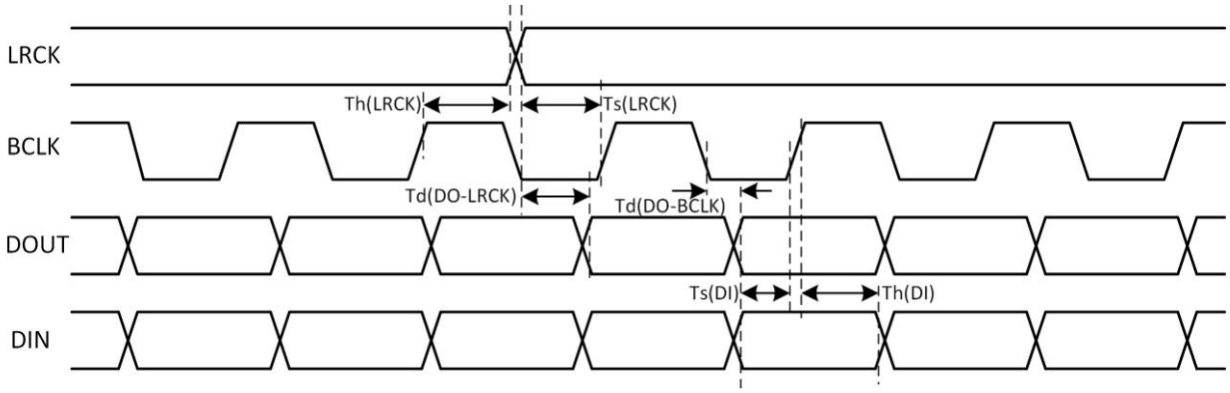



**Figure 5-55. I2S/PCM Timing in Slave Mode**

**Table 5-62. I2S/PCM Timing Constants in Slave Mode**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LRCK setup | Ts(LRCK) | 4 | - | - | ns |
| LRCK hold | Th(LRCK) | 4 | - | - | ns |
| LRCK to DOUT delay(For LJF) | Td(DO-LRCK) | - | - | 10 | ns |
| BCLK to DOUT delay | Td(DO-BCLK) | - | - | 10 | ns |
| DIN setup | Ts(DI) | 4 | - | - | ns |
| DIN hold | Th(DI) | 4 | - | - | ns |
| BCLK rise time | Ts(LRCK) | - | - | 4 | ns |
| BCLK fall time | Th(LRCK) | - | - | 4 | ns |

### 5.12.10. DMIC AC Electrical Characteristics

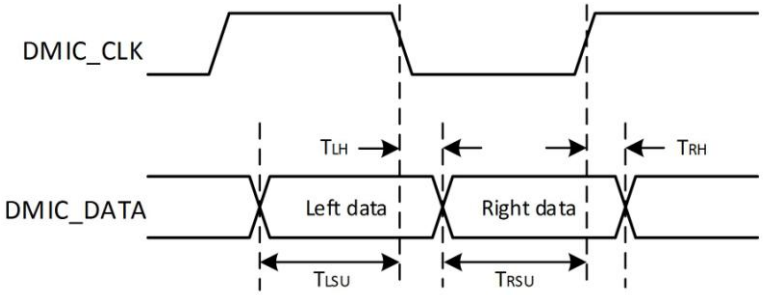



**Figure 5-56. DMIC Timing**

**Table 5-63. DMIC Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DMIC_DATA(Left) setup time to falling edge of DMIC_CLK | Tlsu | 15 | - | - | ns |
| DMIC_DATA(Left) hold time from falling edge of DMIC_CLK | Tlh | 0 | - | - | ns |
| DMIC_DATA(Right) setup time to rising edge of DMIC_CLK | Trsu | 15 | - | - | ns |
| DMIC_DATA(Right) hold time from rising edge of DMIC_CLK | Trh | 0 | - | - | ns |

### 5.12.11. OWA AC Electrical Characteristics

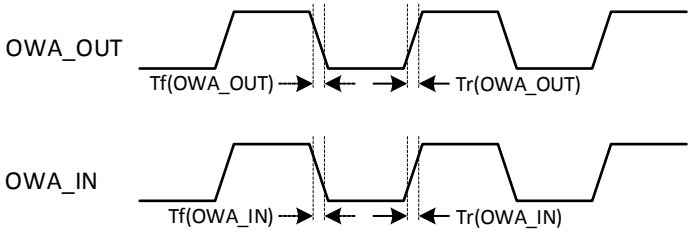



**Figure 5-57. OWA Timing**

**Table 5-64. OWA Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OWA_OUT rise time | Tr(OWA_OUT) | - | - | 8 | ns |
| OWA_OUT fall time | Tf(OWA_OUT) | - | - | 8 | ns |
| OWA_IN rise time | Tr(OWA_IN) | - | - | 4 | ns |
| OWA_IN fall time | Tf(OWA_IN) | - | - | 4 | ns |

### 5.12.12. SCR AC Electrical Characteristics

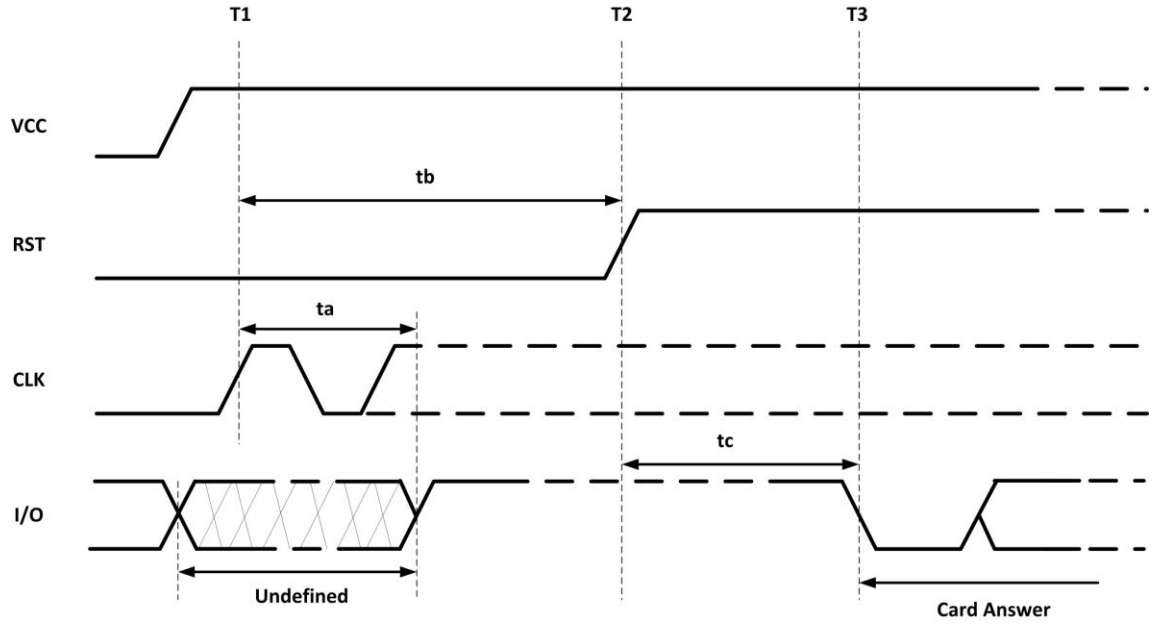



**Figure 5-58. SCR Activation and Cold Reset Timing**

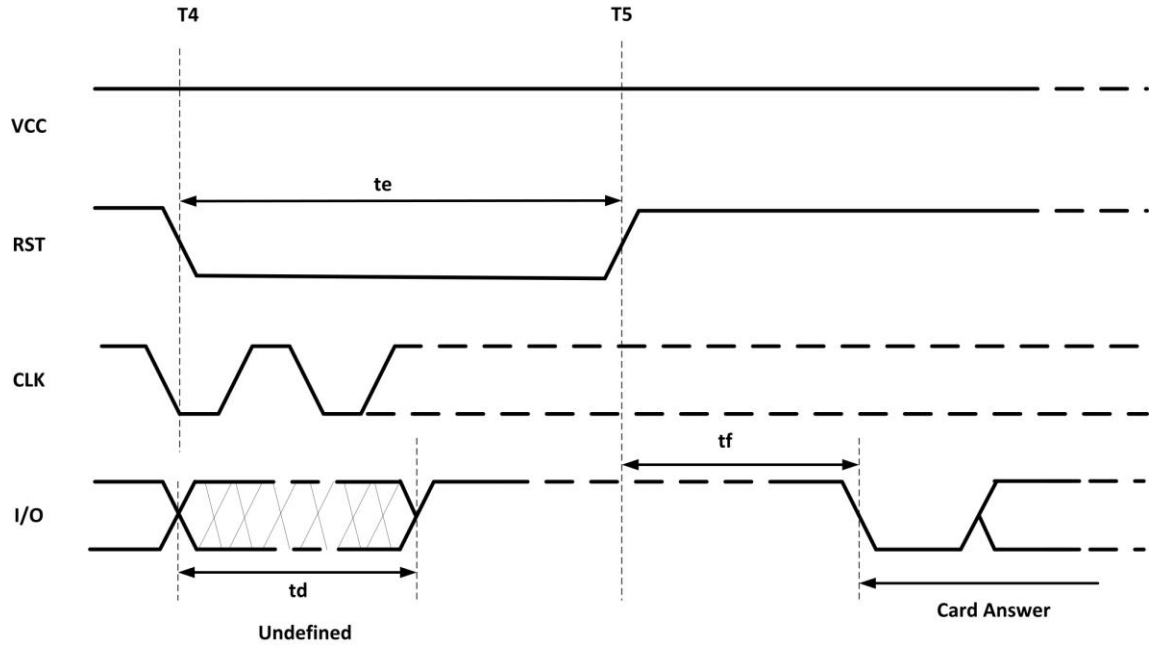



**Figure 5-59. SCR Warm Reset Timing**

**Table 5-65. SCR Timing Constants**

| Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ta | - | - | 200/f | us |
| tb | 400/f | - | - | us |
| tc | 400/f | - | 40000/f | us |
| td | - | - | 200/f | us |
| te | 400/f | - | - | us |
| tf | 400/f | - | 40000/f | us |
| (1) Activation: Before time T1<br>(2) Cold Reset: After time T1<br>(3) T1: The clock signal is applied to CLK at time T1.<br>(4) T2: The RST is put to state H. | | | | |

(5) T3: The card begin answer at time T3.
(6) ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
(7) tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
(8) tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
(9) td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
(10) te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11) tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12) f is the frequency of clock.

### 5.12.13. RSB AC Electrical Characteristics

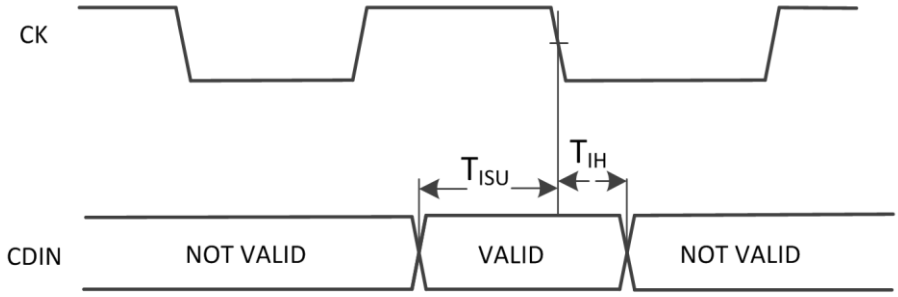



**Figure 5-60. RSB Module Input Timing**

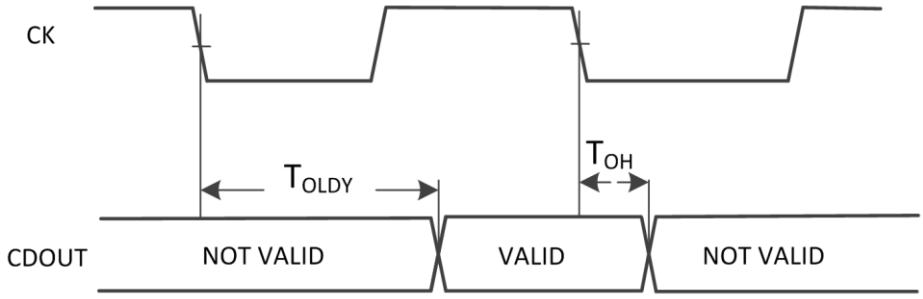



**Figure 5-61. RSB Module Output Timing**

**Table 5-66. RSB Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Clock CK (All values are referred to min ($V_{IH}$) and max ($V_{IL}$))** | | | | | |
| Clock frequency data Transfer mode | $F_P$ | 0 | - | 20 | MHz |
| **Inputs CD(referenced to CK)** | | | | | |
| Input set-up time | $T_{ISU}$ | 6 | - | - | ns |
| Input hold time | $T_{IH}$ | 3 | - | - | ns |
| **Outputs CD (referenced to CK)** | | | | | |
| Output delay time during data transfer mode | $T_{ODLY}$ | - | - | - | ns |
| Output hold time | $T_{OH}$ | 3 | - | - | ns |

# 5.13. Power-On and Power-Off Sequence

The section provides information about the T7 power on and power off sequence requirements.

## 5.13.1. Power-On Sequence

Figure 5-62 shows an example of the power on sequence for the T7 device. The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- VCC-RTC should remain powered on continuously, to maintain internal real-time clock status. Otherwise, it has to be powered on together with VDD-SYS and VDD-CPUS, or preceding VDD-SYS and VDD-CPUS.
- VDD-SYS should be powered on together, or any time after VCC-RTC.
- VDD-CPUS should be powered on together, or any time after VCC-RTC.
- After VCC-PLL powered on, the 24MHz clock need to start oscillating and be stable .
- IO power domains(VCC-IO,VCC-PC,VCC-PD,VCC-PL and VCC-PM) can ramp after VDD-SYS and VDD-CPUS are stabilized.
- VDD-CPUA, VDD-CPUB, VCC-DRAM, VDD-GPU, VDD-VE, VCC-PLL, AVCC, VDD-USB and VCC3V3-USB can ramp at any time from VDD-SYS to VCC-IO.
- During the entire power on sequence, the RESET pin must be held on low until 24MHz clock and all power domains are stable.

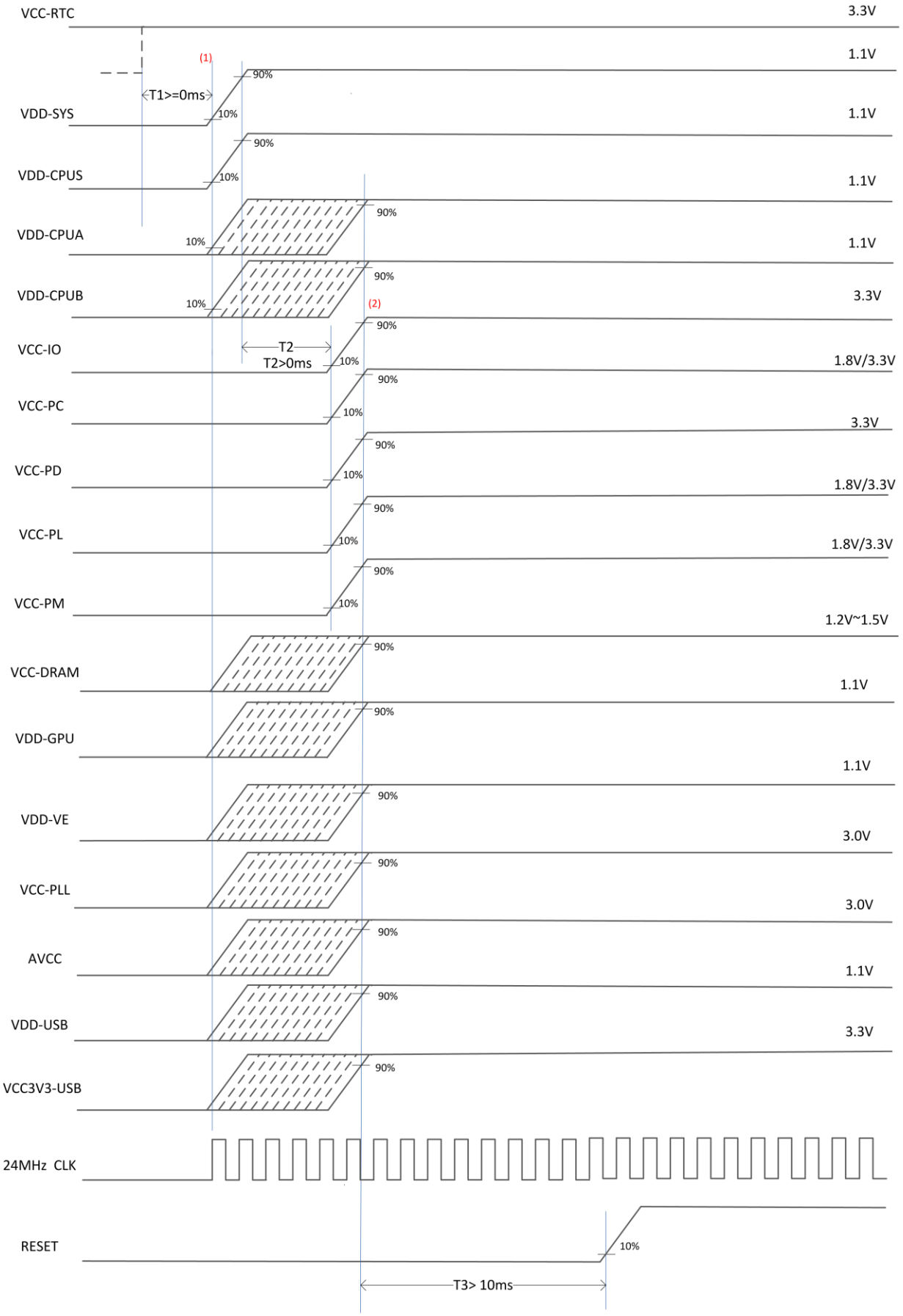



**Figure 5-62. T7 Power On Sequence**

### 5.13.2. Power-Off Sequence

The following steps give an example of the power off sequence supported by the T7 device. Figure 5-63 shows an example of the device power off sequence.

- Reset T7 device.
- VCC-RTC holds high.
- After PMIC receives the power-down command, pull-down RESET.
- After T4, other powers ramp down at the same time, and the ramp rate of each power rail is generally determined by the load on that power.

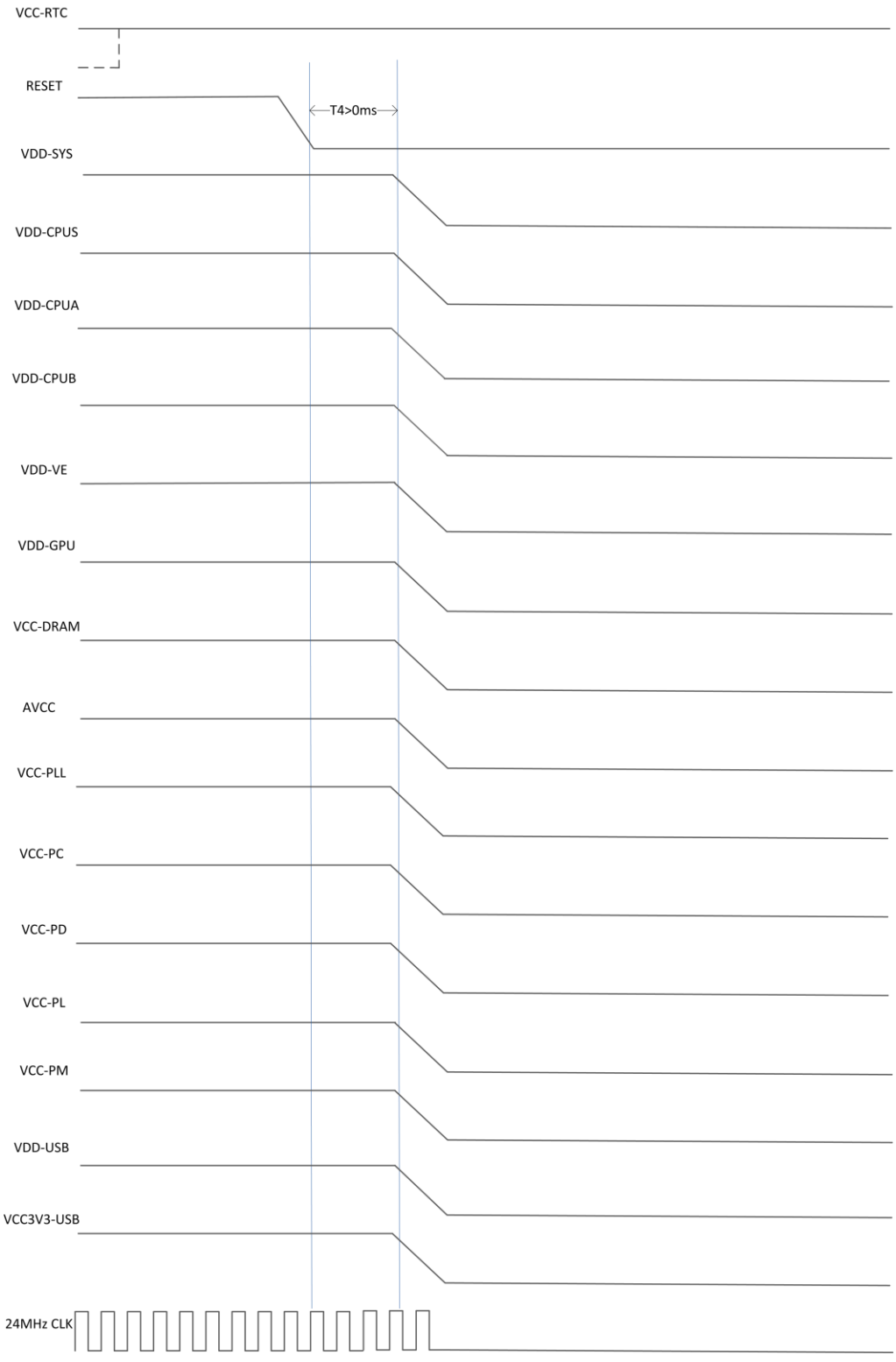



**Figure 5-63. T7 Power Off Sequence**

# 6. Package Thermal Characteristics

Table 6-1 shows thermal resistance parameters of the T7. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51 , the simulating result data is a reference only, please prevail in the actual application condition test.

**NOTE**

- **Test condition: four-layer board(2s2p),natural convection, no air flow.**
- **Design heat dissipation by following the *Allwinner T7 Hardware Design Guide*.**

**Table 6-1. T7 Thermal Resistance Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance | - | 23.4 | - | °C/W |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | - | 8.12 | - | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | - | 6.71 | - | °C/W |

# 7. Pin Assignment

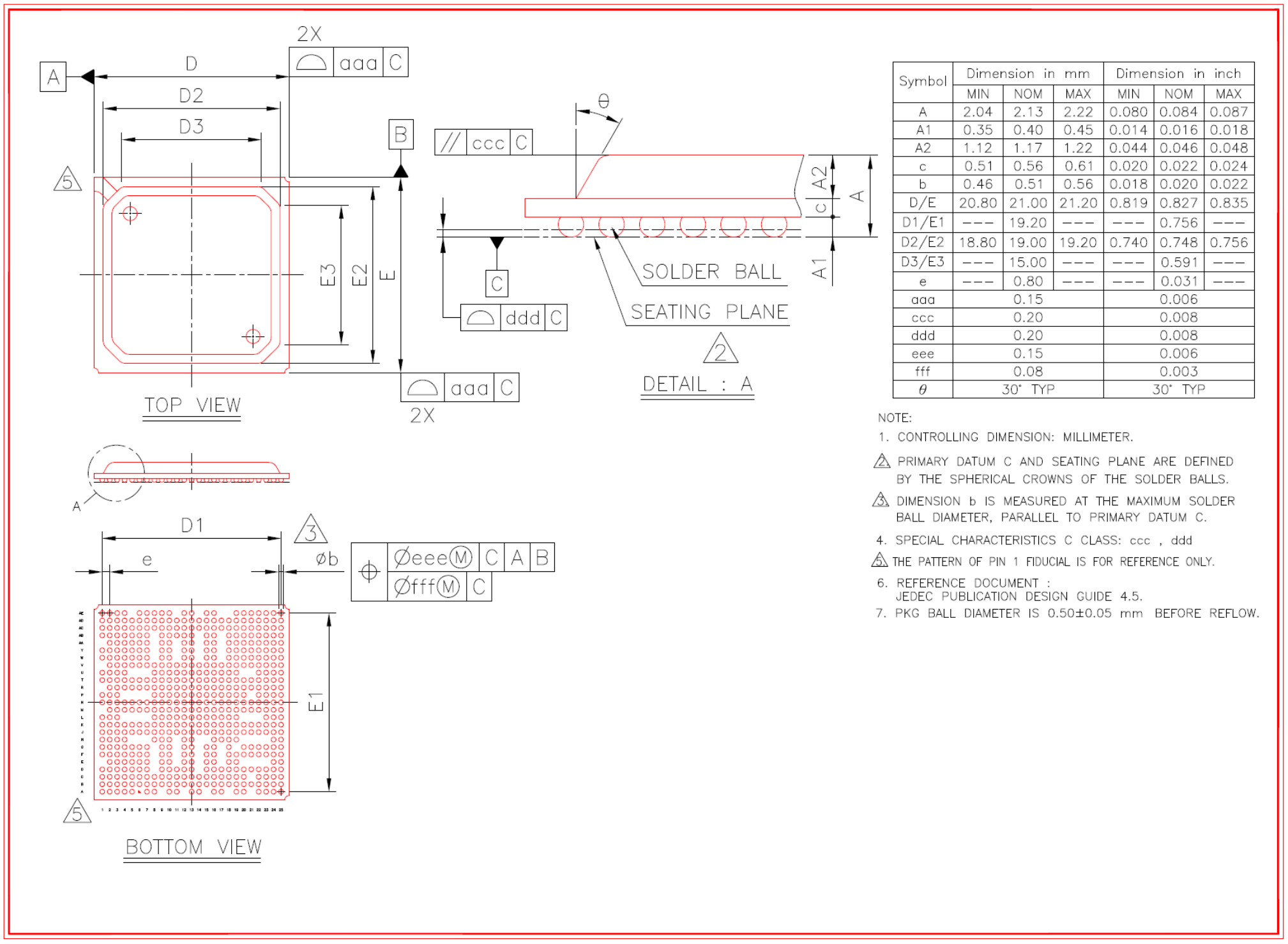
## 7.1. Pin Map

The following figure shows the pin maps of the 547-pin PBGA package of the T7 processor.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | GND | PE0 | PE3 | PE21 | | GND | PC8 | | PC9 | PC14 | | TVIN2 | TVIN0 | | MICIN1P | MICIN3P | | LINEOUTR | X32KOUT | | PL1 | PL3 | GND | GND | A |
| B | GND | PE1 | PE2 | PE17 | PE20 | PE16 | PC16 | PC12 | PC11 | PC10 | PC4 | PC0 | TVIN3 | TVIN1 | LINEINR | MICIN3N | MICIN2N | PHONEOUTP | LINEOUTL | GND | X32KIN | PL0 | PL2 | PL4 | GND | B |
| C | PE11 | PE9 | MCSIA-D3N | MCSIA-D3P | PE8 | PE13 | PE5 | PC13 | PC7 | PC6 | PC1 | PC5 | PC3 | GND-TVIN | LINEINL | MICIN1N | GND | MICIN2P | PHONEOUTN | X32KFOUT | | PL5 | PL6 | RESET | PM5 | C |
| D | MCSIB-D3N | MCSIB-D3P | MCSIA-D2N | MCSIA-D2P | PE7 | PE6 | PC15 | | PC2 | PG8 | GND | PG0 | PG2 | | LRADC0 | LRADC1 | AGND | AVCC | NMI | PL7 | VCC-RTC | PL9 | PL8 | PM6 | HSIC-DAT | D |
| E | | MCSIB-D2N | MCSIB-D2P | GND | PE19 | PE4 | GND | | PG6 | PG12 | | PG5 | PG4 | | GPADC3 | GPADC0 | | VRA2 | MBIAS | | | | | GND | HSIC-STR | E |
| F | MCSIB-CKN | MCSIB-CKP | MCSIA-CKN | MCSIA-CKP | PE15 | PE10 | PE14 | | PG7 | PG10 | | PG1 | PG3 | | GPADC2 | GPADC1 | | VRA1 | GND | PM13 | PM8 | PM12 | PM16 | USB0-DP | USB0-DM | F |
| G | MCSIB-D1N | MCSIB-D1P | MCSIA-D1N | MCSIA-D1P | PE18 | PE22 | PE12 | | PG9 | PG11 | | PG14 | PG13 | | GPADC4 | GPADC5 | | VRP | | PM14 | PM17 | PM7 | PM20 | USB1-DP | USB1-DM | G |
| H | MCSIB-D0N | MCSIB-D0P | MCSIA-D0N | MCSIA-D0P | | | | VCC-PE | GND | VCC-PC | | VCC-PG | VCC-TVIN | | | TVIN-VRN | TVIN-VRP | GND | GND | | | | | USB2-DP | USB2-DM | H |
| J | PH1 | PH0 | PH2 | PH3 | PH17 | PH8 | PH18 | VCC-PJ | VCC-MCSIB | GND | GND | GND | GND | GND | GND | GND | GND | GND | PM2 | PM3 | PM4 | PM15 | PM9 | USB3-DP | USB3-DM | J |
| K | PH7 | PH9 | GND | PH12 | PH10 | PH13 | PH16 | GND | VCC-MCSIA | GND | GND | VDD-GPU | VDD-GPU | VDD-GPU | VDD-GPUFB | GND | TEST | VCC-PL | PM1 | PM0 | PM21 | PM11 | PM10 | DSI-D0N | DSI-D0P | K |
| L | PH6 | PJ15 | PH11 | | | | | VDD-SYS | VDD-SYS | VDD-SYS | GND | VDD-GPU | VDD-GPU | VDD-GPU | GND | GND | GND | GND | VCC-PM | | | | GND | DSI-D1N | DSI-D1P | L |
| M | | PJ6 | PJ16 | PJ11 | PJ17 | PH15 | GND | VDD-SYS | VDD-SYS | VDD-SYS | GND | VDD-GPU | VDD-GPU | VDD-GPU | GND | GND | VDD-CPUS | BOOT-MODE0 | BOOT-MODE1 | PM18 | PM30 | PM19 | PM24 | DSI-CKN | DSI-CKP | M |
| N | PJ10 | PJ13 | PJ4 | PJ18 | PH4 | PH5 | PH14 | VDD-VE | VDD-VE | GND | GND | GND | GND | GND | GND | GND | VDD-CPUS | VDD-USB | GND | PM29 | PM25 | PM31 | PM28 | DSI-D2N | DSI-D2P | N |
| P | PJ3 | PJ2 | PJ5 | | | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | VCC-HSIC | VCC-DSI | VCC-TVOUT | | GND | GND | DSI-D3N | DSI-D3P | P |
| R | | PJ0 | PJ1 | PJ12 | PJ14 | PJ9 | PJ8 | VCC-IO | VCC-IO | VCC-IO | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | VCC3V3-USB | PM27 | PM26 | TVOUT | GND | R |
| T | PF1 | PF0 | PB9 | PB8 | PB6 | PB7 | PJ7 | JTAG-SEL0 | JTAG-SEL1 | GND | GND | GND | GND | GND | GND | GND | GND | GND | VCC-PD | VCC-PD | PD20 | VCC-PLL | GND | X24MFOUT | X24MOUT | T |
| U | PF6 | PF3 | PF2 | GND | | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | PD21 | PD22 | GND | X24MIN | U |
| V | | PF5 | PF4 | PB5 | PB4 | PB3 | GND | VCC-DRAM | VCC-DRAM | VCC-DRAM | VCC-DRAM | GND | VCC-DRAM | VCC-DRAM | VCC-DRAM | GND | GND | GND | GND | VDDBP-EFUSE | PD11 | PD10 | FEL | PD1 | PD0 | V |
| W | PB0 | PB1 | PB2 | SRST | GND | SA7 | SBA2 | | SCS0 | GND | | SA12 | SA10 | | SA15 | SA3 | | GND | GND | GND | GND | PD13 | PD12 | PD3 | PD2 | W |
| Y | SVREF | GND | GND | SWE | SA13 | SRAS | SA6 | | SODT0 | SCKE0 | | GND | SA4 | | SBA1 | GND | | GND | GND | VDD-CPUBFB | VDD-CPUB | VDD-CPUB | VDD-CPUB | PD5 | PD4 | Y |
| AA | | SDQ31 | SDQ30 | GND | SCAS | SA8 | GND | | SCKE1 | SCS1 | | SA11 | GND | | SA2 | SZQ | | GND | GND | GND | VDD-CPUB | VDD-CPUB | VDD-CPUB | PD7 | PD6 | AA |
| AB | SDQS3P | SDQ29 | SDQ28 | SA9 | GND | SBA0 | SA5 | | GND | SODT1 | GND | SA14 | SA0 | | GND | SA1 | | GND | GND | GND | VDD-CPUB | VDD-CPUB | VDD-CPUB | PD9 | PD8 | AB |
| AC | SDQS3N | SDQ27 | SDQ26 | SDQ23 | SDQ20 | SDQ19 | GND | GND | SDQ7 | SDQ4 | SDQS0N | SDQ1 | GND | SDQ15 | SDQ13 | SDQ11 | SDQ9 | SDQM1 | GND | VDD-CPUA | VDD-CPUA | VDD-CPUA | PD16 | PD15 | PD14 | AC |
| AD | GND | SDQ25 | SDQ24 | SDQ22 | SDQS2P | SDQS2N | SDQ16 | SDQM2 | GND | SDQ5 | SDQS0P | SDQ3 | SDQM0 | SDQ14 | SDQ12 | GND | SDQ10 | SDQ8 | GND | VDD-CPUA | VDD-CPUA | VDD-CPUA | PD18 | PD17 | GND | AD |
| AE | GND | GND | SDQM3 | SDQ21 | | SDQ18 | SDQ17 | SCKN | SCKP | SDQ6 | | SDQ2 | SDQ0 | | SDQS1P | SDQS1N | | | VDD-CPUAFB | VDD-CPUA | VDD-CPUA | VDD-CPUA | PD19 | GND | GND | AE |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | |

## 7.2. Package Dimension

The following diagram shows the package dimension of the T7 processor, includes the top, bottom, side views and details of the 21mmx21mm package.




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 2.04 | 2.13 | 2.22 | 0.080 | 0.084 | 0.087 |
| A1 | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| A2 | 1.12 | 1.17 | 1.22 | 0.044 | 0.046 | 0.048 |
| c | 0.51 | 0.56 | 0.61 | 0.020 | 0.022 | 0.024 |
| b | 0.46 | 0.51 | 0.56 | 0.018 | 0.020 | 0.022 |
| D/E | 20.80 | 21.00 | 21.20 | 0.819 | 0.827 | 0.835 |
| D1/E1 | --- | 19.20 | --- | --- | 0.756 | --- |
| D2/E2 | 18.80 | 19.00 | 19.20 | 0.740 | 0.748 | 0.756 |
| D3/E3 | --- | 15.00 | --- | --- | 0.591 | --- |
| e | --- | 0.80 | --- | --- | 0.031 | --- |
| aaa | 0.15 | | | 0.006 | | |
| ccc | 0.20 | | | 0.008 | | |
| ddd | 0.20 | | | 0.008 | | |
| eee | 0.15 | | | 0.006 | | |
| fff | 0.08 | | | 0.003 | | |
| θ | 30° TYP | | | 30° TYP | | |

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. REFERENCE DOCUMENT : JEDEC PUBLICATION DESIGN GUIDE 4.5.
7. PKG BALL DIAMETER IS 0.50±0.05 mm BEFORE REFLOW.

# 8. Carrier, Storage and Baking Information

## 8.1. Carrier

### 8.1.1. Matrix Tray Information

Table 8-1 shows the T7 matrix tray carrier information.

**Table 8-1. Matrix Tray Carrier Information**

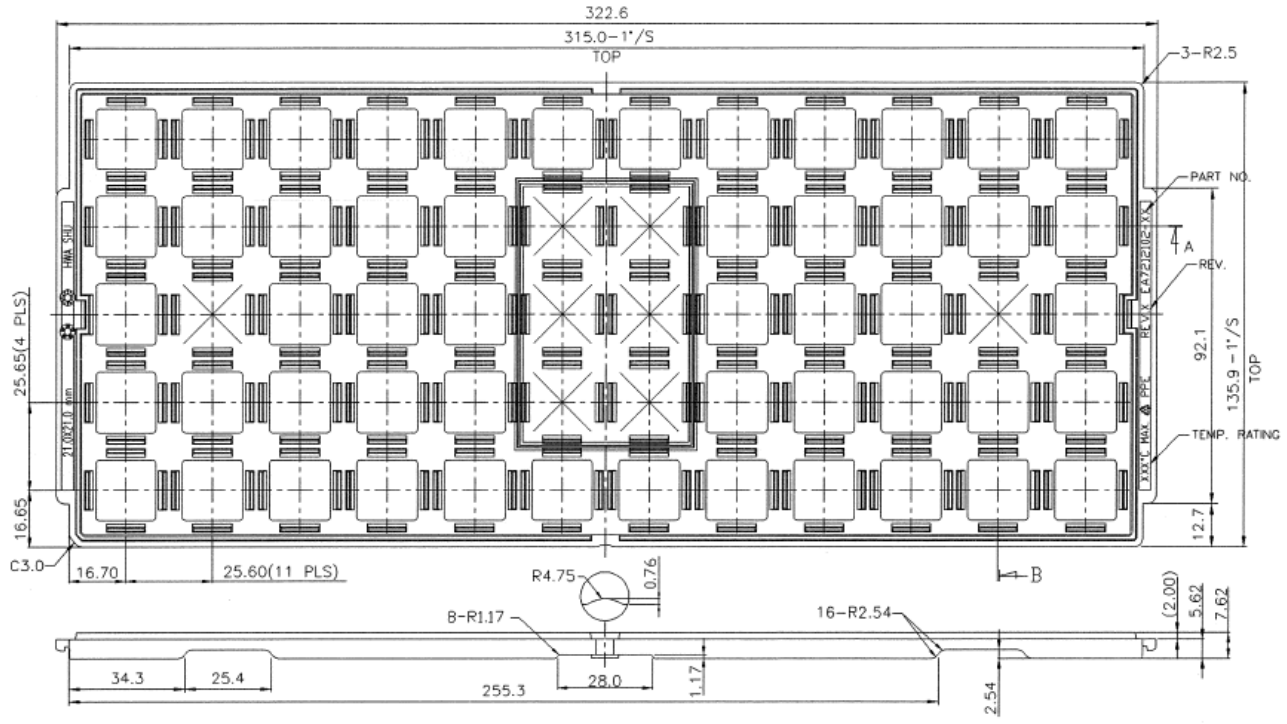
| Item | Color | Size | Note |
|---|---|---|---|
| Tray | Black | 315mm x 136mm x 7.62mm | 60 Qty/Tray |
| Aluminum foil bags | Silvery white | 540mm x 300mm x 0.14mm | Surface impedance:$10^9\Omega$<br>Vacuum packing<br>Including HIC and desiccant<br>Printing: RoHS symbol |
| Pearl cotton cushion(Vacuum bag) | White | 12mm x 680mm x 185mm | |
| Pearl cotton cushion (The Gap between vacuum bag and inner box) | White | Left-Right:12mm x 180mm x 85mm<br>Front-Back:12mm x 350mm x 70mm | |
| Inner box | White | 396mm x 196mm x 96mm | Printing: RoHS symbol |
| Carton | White | 420mm x 410mm x 320mm | |

Table 8-2 shows the T7 packing quantity.

**Table 8-2. Packing Quantity Information**

| Sample | Size(mm) | Qty/Tray | Tray/Inner Box | Full Inner Box Qty | Inner Box/Carton | Full Carton Qty |
|---|---|---|---|---|---|---|
| T7 | 21 x 21 | 60 | 10 | 600 | 6 | 3600 |

Figure 8-1 shows tray dimension drawing of the T7.



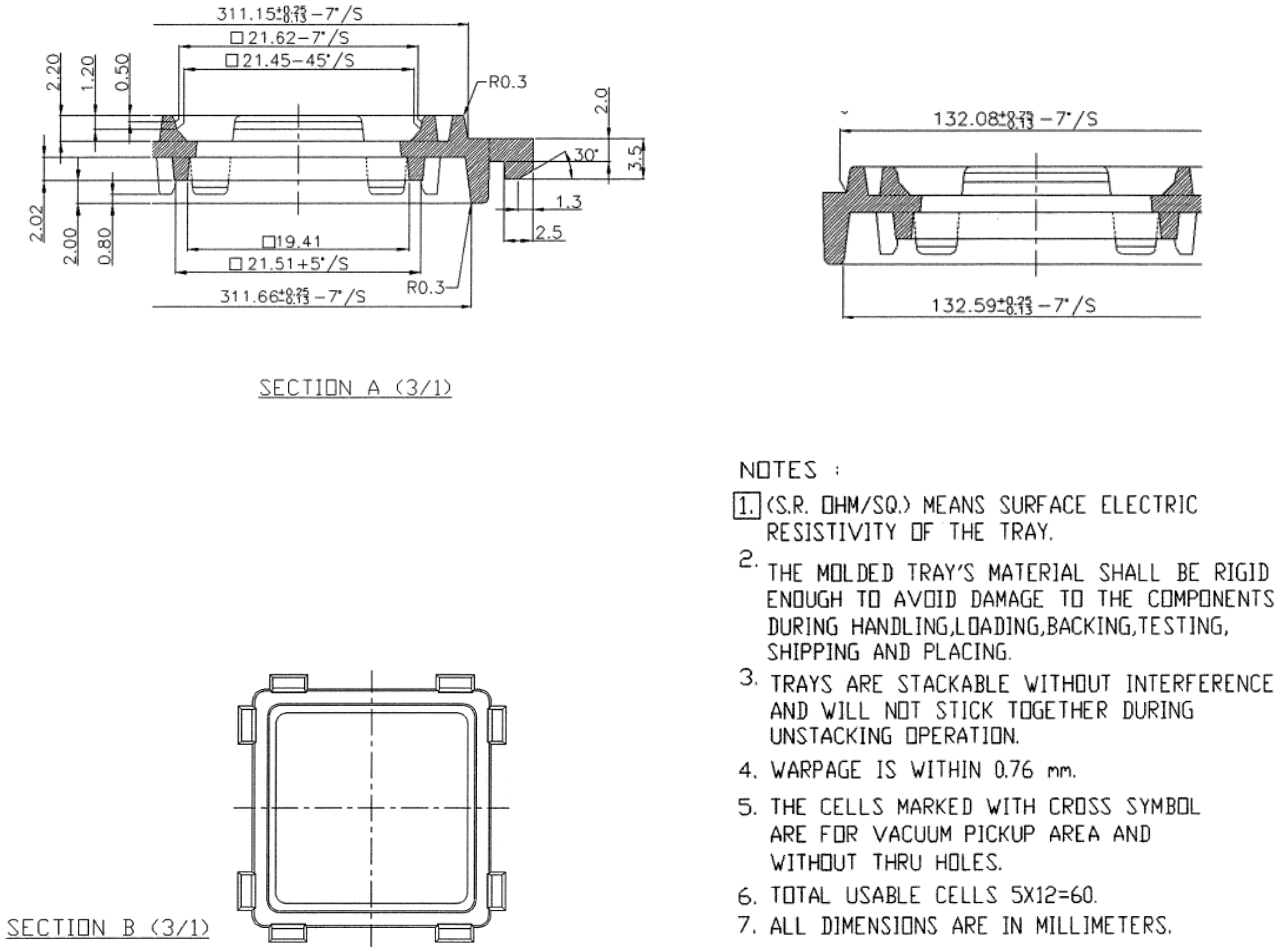



**Figure 8-1. Tray Dimension Drawing**

## 8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

### 8.2.1. Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in Table 8-3.

**Table 8-3. MSL Summary**

| MSL | Out-of-bag floor life | Comments |
|---|---|---|
| 1 | Unlimited | ≤30°C / 85%RH |
| 2 | 1 year | ≤30°C / 60%RH |
| 2a | 4 weeks | ≤30°C / 60%RH |
| 3 | 168 hours | ≤30°C / 60%RH |
| 4 | 72 hours | ≤30°C / 60%RH |
| 5 | 48 hours | ≤30°C / 60%RH |
| 5a | 24 hours | ≤30°C / 60%RH |
| 6 | Time on Label(TOL) | ≤30°C / 60%RH |

**NOTE**

**The T7 device samples are classified as MSL3.**

### 8.2.2. Bagged Storage Conditions

The shelf life of the T7 device samples are defined in Table 8-4.

**Table 8-4. Bagged Storage Conditions**

| | |
|---|---|
| **Packing mode** | Vacuum packing |
| **Storage temperature** | 20°C ~26°C |
| **Storage humidity** | 40%~60%RH |
| **Shelf life** | 12 months |

### 8.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the T7 are as follows.

**Table 8-5. Out-of-bag Duration**

| | |
|---|---|
| **Storage temperature** | 20°C~26°C |
| **Storage humidity** | 40%~60%RH |
| **Moisture sensitive level(MSL)** | 3 |
| **Floor life** | 168 hours |

SMT: Should finish the SMT process within 168 hours.
After open the vacuum bag, check the humidity indicator card (HIC):

- If 10%RH dot of HIC is not wheat, it means the chip has got moisture and must be re-baked through Table 8-6.
- If 10%RH dot of HIC is wheat, it means the chip is dry and can produce normally.

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

## 8.3. Baking

It is not necessary to bake the T7 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded.
It is necessary to bake the T7 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary bake the T7 if the storage humidity condition has been exceeded. We recommend that the device sample removed from its vacuum bag more than 2 days should be baked to guarantee production.

Note that baking should not exceed 3 times.

**Table 8-6. Baking Conditions**

| Body thickness | Surrounding | Level | Bake@125°C | Bake@90°C≤5%RH | Bake@40°C≤5%RH |
|---|---|---|---|---|---|
| 1.73mm | nitrogen protection | 3 | 17 hours | 2 days | 23 days |

# 9. Reflow Profile

All Allwinner chips provided for clients are Lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

Reflow profile conditions of the T7 device sample are given in Table 9-1.

**Table 9-1. T7 Reflow Profile Conditions**

| Profile Stage | Description | Symbol | High Temperature Condition Limits |
|---|---|---|---|
| Preheat | Initial ramp temperature range | A | 25°C to 150°C |
| | Initial ramp rate | B | < 3°C/s |
| Soak | Soak temperature range | C | 150°C to 180°C |
| | Soak time | D | 40s to 60s |
| Reflow | Liquidus temperature | E | 217°C |
| | Time above liquidus | F | 60s to 90s |
| | Peak temperature | G | 235°C to 250°C |
| Cool down | Cool down temperature rate | H | < 4°C/s |

Figure 9-1 shows the typical reflow profile of the T7 device sample.

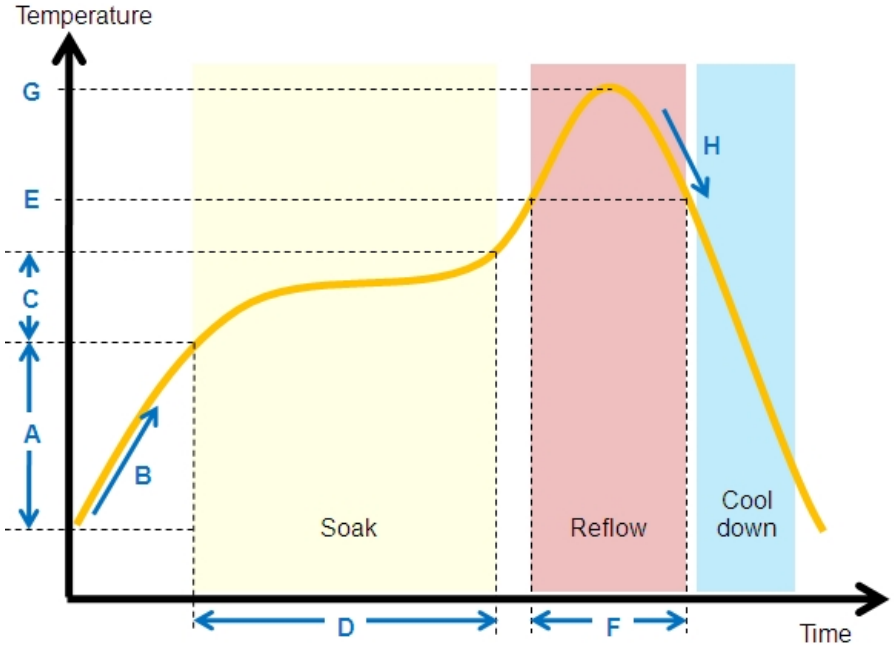



**Figure 9-1. T7 Typical Reflow Profile**

**NOTE**

**The above reflow profile is solder joint testing result, it is for reference only, please adjust depending on actual production conditions.**

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe.

See Figure 9-2.

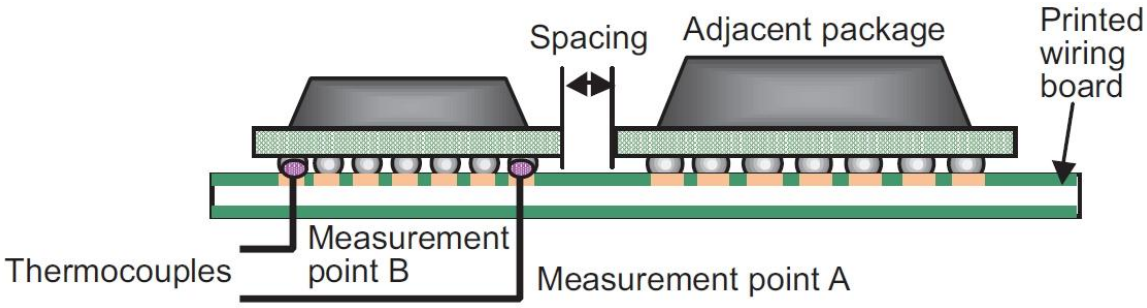



**Figure 9-2. Measuring the Reflow Soldering Process**

**NOTE**

**To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.**

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

# 10. Part Marking

Figure 10-1 shows the T7 marking.

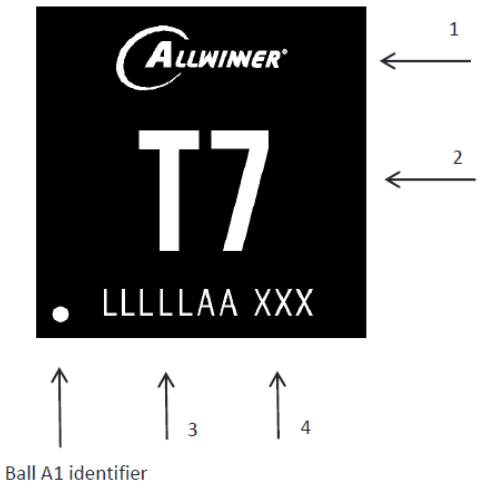



**Figure 10-1. T7 Marking**

Table 10-1 describes the T7 marking definitions.

**Table 10-1. T7 Marking Definitions**

| No. | Marking | Description | Fixed/Dynamic |
|---|---|---|---|
| 1 | ALLWINNER | Allwinner logo or name | Fixed |
| 2 | T7 | Product name | Fixed |
| 3 | LLLLLAA | Lot number | Dynamic |
| 4 | XXX | Data code | Dynamic |

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