A523
User Manual

Revision 1.1

Jul.5, 2023

Revision History

Revision	Date	Author	Description
1.0	April 3, 2023	AWA1896	Initial Release Version
1.0.1	May 12, 2023	AWA1896	Update the performace of the video decoding.
1.1	Jul.5, 2023	AWA1896	**About this document** Add revision number definition **Chapter 1 Production Description** Update the features of some modules. **Chapter 2 System** 1. Update PLL distribution and some registers in section 2.5 2. Update IOMMU TLB enbale register (offset: 0x0060) in section 2.9. 3. Update features in section 2.14.1 and add THS Temperature Conversion Formula in section 2.14.3.4. **Chapter 3 Memory** SMHC module is updated. **Chapter 4 Audio** Update the features of Audio Codec and I2S/PCM. **Chapter 7 Video Input Interfaces** CSIC module is updated. **Chapter 8 Interfaces** 1. Update the Global Core Control Register (offset: 0xC110) in section 8.11.6.5 2. Update the features of the PCIe2.1 module and SPIFC module. 3. Update the block digram of the PCIe2.1 module. 4. Update the PCIE SII Interrupt Mask Register1 (offset: 0x0E04) and the PCIE SII Interrupt Register1 (offset: 0x0E0C) in section 8.12.5.

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About This Document

Purpose and Scope

This document describes the features, logical structures, functions, operating modes, and related registers of each module about A523. For details about the interface timings and related parameters, the pins, pin usages, performance parameters, and package dimension, please refer to the *A523_Datasheet*.

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Programmers in writing code or modifying the Allwinner provided code

Revision Number Definiton

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

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Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

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Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Reset Value Conventions

In the register definition tables:

If other column value in the row of a bit or multiple bits is "/", this bit of these multiple bits are unused.

If the default value of a bit or multiple bits is "UDF", this default value is undefined.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

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The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression, X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

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1 Product Description

1.1 Overview

A523 series features high-performance platform processors for medium- and high-end tablets and interactive display applications. It integrates octa-core Cortex™-A55 CPU and G57 MC01 GPU to ensure rapid response and smooth running for daily applications, such as on-line video, web browsing, 3D game, and so on. A523 series also supports DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X, eMMC, NAND, SPI NAND, high-speed interfaces (PCIe2.1 and USB3.1 GEN1), multi video output interfaces (RGB/Dual-LVDS/2xMIPI-DSI/eDP), and video input interfaces (MIPI CSI). In addition, this chip family supports 4K@60fps H.265 decoder, 4K@25fps H.264 encoder, DI, and SmartColor system to provide users with outstanding experience. A523 series can be applied in the tablet PC market and the interactive terminal market.

1.2 Device Differences

The A523 series is configured with different sets of features in different devices. The feature differences across different devices are shown in the following table.

Table 1-1 Device Feature Differences

Device	Cortex™-A55 Speed Grade	Maximum Video Decoding Rate	
		H.265	VP9
A523H00X0000	2.0 GHz	4K@60fps, 10 bits	4K@60fps, 10 bits
A523M00X0000	1.8 GHz	4K@30fps, 8bits	4K@30fps, 8bits

NOTE

The terms “A523”and “A523 Series” are used in the following document to refer to the all devices listed in Table 1-1.

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1.3 Features

1.3.1 CPU Architecture

- Octa-core ARM Cortex™-A55 in a DynamIQ big.LITTLE configuration, up to 2.0 GHz
  - 32 KB L1 I-cache and 32 KB L1 D-cache per A55 core
  - Optional 64KB L2 cache per “LITTLE” core
  - Optional 128KB L2 cache per “big” core
- Single-core RISC-V, up to 200 MHz
  - 16 KB I-cache and 16 KB D-cache
  - RV32IMAFC instructions

1.3.2 GPU Architecture

- ARM G57 MC01 GPU
- Supports OpenGL ES 3.2/2.0/1.1, Vulkan1.1/1.2/1.3, and OpenCL2.2
- Output and input format: 8-bit, 10-bit, and 16-bit YUV
- Anti-aliasing algorithm
- High memory bandwidth and low power consumption in 3D graphics processing
- AMBA4 AXI slave interface
- Latency tolerance
- Texture compression
- Configurable power management
- AFBC1.3
- Supports Digital Rights Management (DRM)

1.3.3 Memory Subsystem

1.3.3.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
  - SD Card
  - eMMC
  - RAW NAND Flash
  - SPI NOR Flash (Single Mode and Quad Mode)

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- SPI NAND Flash

- Supports mandatory upgrade process through USB or SD card
- Supports GPADC0 pin and eFuse module to select the boot media type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Secure BROM ensures that the secure boot is a trusted environment

1.3.3.2 RAW NAND Flash

- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports SLC/MLC/TLC flash and EF-NAND
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0, and Toggle DDR2.0 RAW NAND FLASH

1.3.3.3 SDRAM

- 32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X interface
- Memory capacity up to 4GB
- 4 chip select lines for for LPDDR3, LPDDR4, and LPDDR4X (especially the 64-bit LPDDR3, LPDDR4, and LPDDR4X)
- Clock frequency up to 1066 MHz for DDR3, DDR3L, and LPDDR3
- Clock frequency up to 1200 MHz for DDR4, LPDDR4, and LPDDR4x

1.3.3.4 SMHC

- Three SD/MMC host controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (SD3.0)
  - SMHC1, compliant with the protocol Secure Digital I/O (SDIO3.0)
  - SMHC2, compliant with the protocol Multimedia Card (eMMC5.1)
- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad

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  - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 supports the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Supports HS400 mode and HS200 mode
  - Maximum performance
    - SDR mode 200MHz@1.8V IO pad
    - DDR mode 200MHz@1.8V IO pad
    - SDR mode 50MHz@3.3V IO pad
    - DDR mode 50MHz@3.3V IO pad
- Support block size of 1 to 65535 bytes
- Support hardware CRC generation and error detection

1.3.4 Video and Graphics

1.3.4.1 Display Engine (DE)

- Output size up to 4096 x 2048
- Supports seven alpha blending channels for main display and two display outputs
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports AFBC buffer decoder
- Supports vertical keystone correction
- Input format
  - Semi-planar of YUV422/YUV420/YUV411/P010/P210
  - Planar of YUV422/YUV420/ YUV411
  - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Output format: 8-bit or 10-bit YUV444/YUV422/YUV420/RGB444
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- 10-bit processing path for HDR video
- SmartColor5.0 for excellent display experience
  - Adaptive de-noising for compression noise or mosquito noise with yuv420/422 input
  - Adaptive super resolution scaler
  - Adaptive local dynamic contrast enhancement
  - Adaptive detail/edge enhancement

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- Adaptive color enhancement (blue-stretch, green-stretch, and fresh tone correction) and skin tone protection
- Hue gain, saturation gain, and value gain controller
- Fully programmable color matrix
- Dynamic gamma

- Supports write back for high efficient dual display and miracast
- Supports register configuration queue for register update function

1.3.4.2 De-interlacer (DI)

- Only off-line processing mode
- Video resolution from 32x32 to 2048x1280 pixel
- Input data format: 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined
- Output data format
  - 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined for DIT
  - YV12/planar YUV422 for TNR
- Weave/pixel-motion-adaptive de-interlace method
- Temporal noise reduction
- Film mode detection with video-on-film detection
- Performance
  - Module clock 120MHz for 1080P@60Hz YUV420 with all functions enable
  - Module clock 150MHz for 1080P@60Hz YUV422 with all functions enable

1.3.4.3 Graphic 2D (G2D)

- Layer size up to 2048x2048 pixels
- Input format and output format contain the following:
  - YUV422 (semi-planar and planar format)
  - YUV420 (semi-planar and planar format)
  - P010, P210, P410, and Y8
  - ARGB8888, XRGB8888, RGB888, ARGB4444, ARGB1555, ARGB2101010, and RGB565
- Multiple rotation types
  - Horizontal flip and vertical flip
  - 0, 90, 180, or 270 degrees' rotation in clockwise direction

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1.3.4.4 Video Engine

Video Decoding

- Supports ITU-T H.265 Main/Main10, level 6.1
  - Maximum video resolution:8192x4320
  - Maximum decoding rate: 3840x2160@60fps, 10 bits
- Supports VP9 Profile0/ Profile2, level 6.1
  - Maximum video resolution: 8192 x 4320
  - Maximum decoding rate: 3840x2160@60fps, 10 bits
- Supports ITU-T H.264 Base/Main/High Profile@Level 4.2
  - Maximum video resolution: 3840 x 2160
  - Maximum decoding rate: 3840x2160@30fps, 8 bits

Video Encoding

- H.264 BP/MP/HP encoding
  - Supports 4K@25fps@8bits
  - Maximum resolution: 4096 x 4096 (16 megapixels)
  - Supports I/P frame type
  - Supports CBR, VBR and FIXEDQP modes
  - Supports region of interest(ROI) encoding, a maximum of eight ROIs
- JPEG baseline encoding
  - JPEG encoder supports 4K@15fps
  - JPEG encoder supports YUV420, YUV422 and YUV444 format
- MJPEG baseline encoding up to 4K@15fps

1.3.5 Video Output

1.3.5.1 eDP1.3

- Up to 2.5K@60fps
- 1-lane, 2-lane, or 4-lane transmission, up to 2.7 Gbit/s per lane
- Video formats: RGB, YCbCr4:4:4, and YCbCr4:2:2
- Color depth: 8-bit and 10-bit per channel
- Supports I2S interface
  - Supports mono sound, stereo sound, and 7.1 surround sound

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- Maximum sampling rate: 192 KHz

- Full link training
- Hot plug detection
- AUX channel
  - Maximum working frequency: 1MHz
  - Adopts Manchester-II encoding
- Clock spread spectrum
- Programmable voltage swing and pre-emphasis
- Embedded ESD

1.3.5.2 MIPI DSI

- Compliance with MIPI DSI V1.02
- Up to 1.5 Gbit/s for each lane
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports 4+4-lane MIPI DSI, up to 2560 x 1600@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous and non-continuous lane clock modes
- Generic commands support bidirectional communication in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Supports hardware checksum

1.3.5.3 TCON LCD

- Two TCON LCD controllers: TONC_LCD0 and TCON_LCD1
- TCON_LCD0 supports the following
  - Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
  - Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
  - Supports LVDS interface with dual link, up to 1920 x 1080@60fps
  - Supports LVDS interface with single link, up to 1366 x 768@60fps
  - Dither function for RGB888, RGB666, and RGB565
  - Supports i8080 interface, up to 800 x 480@60fps

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- Supports BT656 interface for NTSC and PAL
- Supports MIPI DSI interface with dual link, up to 2560x1600@60fps
- Supports MIPI DSI interface with single link, up to 1920x1200@60fps

- TCON_LCD1 supports MIPI DSI interface with single link, up to 1920x1200@60fps

1.3.5.4 TCON TV

- One TCON TV controller (TCON_TV1) for eDP1.3
- Up to 2.5K@60Hz
- Output format:
  - 8-bit or 10-bit pixel depth
  - HV

1.3.6 Video Input

1.3.6.1 ISP

- Supports one individual image signal processor(ISP), with maximum resolution of 3264x4224 in online mode
- Maximum frame rate of 8M@30fps 2F-WDR
- Supports off-line mode
- Supports WDR spilt, 2F-WDR line-based stitch, dynamic range compression (DRC), tone mapping, digital gain, gamma correction, defect pixel correction (DPC), cross talk correction (CTC), and chromatic aberration correction (CAC)
- Supports 2D/3D noise reduction, bayer interpolation, sharpen, white balance, and color enhancement
- Adjustable 3A functions: automatic white balance (AWB), automatic exposure (AE), and automatic focus (AF)
- Supports anti-flick detection statistics, and histogram statistics

1.3.6.2 VIPP

- Four VIPP YUV422 or YUV420 outputs
- Maximum resolution of 3264x4224
- Each VIPP has one sub-VIPP in online mode
- Each VIPP has maximum four sub-VIPPs for time division multiplexing in offline mode
- Each Sub-VIPP supports the following:

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- Crop
- 1 to 1/16 scaling for height and width
- 16 ORLs

- Supports graphics mirror and flip

1.3.6.3 MIPI CSI

- 8M@30fps RAW12 2F-WDR, size up to 3264(H) x 2448(V)
- 4+4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI Interface
  - MIPI CSI2 V1.1
  - MIPI DPHY V1.1
  - 2.0 Gbit/s per lane
- Crop function
- Frame-rate decreasing via software
- 4 DMA controllers for 4 video stream storage
  - Conversion of interlaced input to progressive output (anti-aliasing and noise reduction are not supported)
  - Data conversion supports: YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
  - Horizontal and vertical flip

1.3.6.4 Parallel CSI

- 16-bit digital camera interface
- Supports 8/10/12/16-bit width
- Supports BT.656, BT.601, BT.1120 interface
- Dual Data Rate (DDR) sample mode with pixel clock up to 148.5MHz
- Supports ITU-R BT.656 up to 4*720P@30fps
- Supports ITU-R BT.1120 up to 4*1080P@30fps

1.3.7 System Peripherals

1.3.7.1 Clock Controller Unit (CCU)

- 10 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator

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- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

1.3.7.2 DMAC

- Up to 16-ch DMA in CPUX domain and 16-ch DMA in CPUS domain
- Provides 53 peripheral DMA requests for data reading and 53 peripheral DMA requests for data writing
- Transferring data with linked list
- Flexible data width: 8 bits, 16 bits, or 32 bits
- Programmable DMA burst length
- DRQ response includes waiting mode and handshake mode
- Supports non-aligned transform for memory devices
- DMA channels that support the following:
  - Pausing DMA
  - BMODE and I/O speed mode
  - DMA timeout

1.3.7.3 I/O Memory Management Unit (IOMMU)

- Supports virtual address to physical address mapping by hardware implementation
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI parallel address mapping
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI bypass function independently
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI pre-fetch independently
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

1.3.7.4 Message Box (MSGBOX)

- Supports communication between two CPUs through one way channels. Each CPU has one MSGBOX and can only read or write in one communication

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- CPUX_MSGBOX: CPUS/RISC-V write; ARM CPU read
- CPUS_MSGBOX: ARM CPU/RISC-V write; CPUS read
- RISCV_MSGBOX: ARM CPU/CPUS write; RISC-V read

- The channel between two CPU has 4 channels, and the FIFO depth of a channel is 8 x 32 bits
- Supports interrupts

1.3.7.5 Power Reset Clock Management (PRCM)

- Two PRCMs in CPUS domain: PRCM and MCU_PRCM
- 1 PLL
- CPUS Clock Configuration
- APBS Clock Configuration
- CPUS Module Clock Configuration
- CPUS Module BUS Gating and Reset
- RAM configure Control for PRCM

1.3.7.6 RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports fanout function of internal 32K clock
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing power-off information in AON domain

1.3.7.7 Spinlock

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

1.3.7.8 Thermal Sensor Controller (THS)

- Two THS controllers
  - THS0, including TSENSOR4

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- THS1, including TSENSOR0, TSENSOR1, and TSENSOR2

- Temperature accuracy: ±5°C from -40°C to 60°C, ±3°C from -60°C to +125°C
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

1.3.7.9 Timer

- Configurable counting clock: 32KHz, 24MHz, 16MHz, or 200MHz
- Programmable 56-bit down timer
- Two working modes: periodic mode and single count mode
- Generates an interrupt when the count is decreased to 0

1.3.7.10 Watchdog Timer (WDT)

- Supports 12 initial values
- Supports the generation of timeout interrupts
- Supports the generation of reset signals
- Supports Watchdog Restart

1.3.8 Audio Subsystem

1.3.8.1 Audio Codec

- Two audio digital-to-analog converter (DAC) channels
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 100 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- Three audio outputs
  - One stereo headphone output: HPOUTL/R
  - Two differential lineout outputs: LINEOUTLP/N and LINEOUTRP/N
- Three audio analog-to-digital converter (ADC) channels
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95 ± 3 dB SNR@A-weight, -80 ± 3 dB THD+N
- Three differential microphone inputs: MICIN1P/1N, MICIN2P/2N, and MICIN3P/3N (for echo reduction)

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- Two low-noise analog microphone bias outputs: MBIAS and HBIAS
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA
- Internal ALDO output for AVCC

1.3.8.2 I2S/PCM

- Four I2S/PCM external interfaces (I2S0, I2S1, I2S2, and I2S3) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- FIFOs for transmitting and receiving data
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width $\leqslant$ 24.576 MHz)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

1.3.8.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

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1.3.8.4 One Wire Audio (OWA)

- One OWA TX and One OWA RX
- Compliance with S/PDIF interface
- IEC-60958 and IEC-61937 transmitter and receiver functionality
- IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- TXFIFO and RXFIFO
  - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
  - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Multiple function clock
  - Separate clock for OWA TX and OWA RX
  - The clock of TX function includes 24.576 MHz and 22.5792 MHz
  - The clock of RX function includes 24.576*8 MHz
- Supports Hardware Parity On TX/RX
  - Hardware Parity generation on the transmitter
  - Hardware Parity checking on the receiver
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter

1.3.9 Security System

1.3.9.1 Crypto Engine (CE)

- Symmetrical algorithm:
  - AES symmetrical algorithm
    - Key size: 128/192/256 bits
    - CFB mode includes: CFB1, CFB8, CFB64, and CFB128
    - CTR mode includes: CTR16, CTR32, CTR64, and CTR128
    - Supports ECB, CBC, CTS, OFB, CBC-MAC, and GCM modes
  - DES symmetrical algorithm
    - CTR mode, includes: CTR16, CTR32, and CTR64

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  - Supports ECB, CBC, and CBC-MAC mode
- Supports 3DES
- SM4 symmetrical algorithm supports ECB and CBC mode

- Hash algorithms
  - Support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
  - Support HMAC-SHA1, HMAC-SHA256
- Random bit generator algorithms
  - Support PRNG, 175 bits seed width, and output with multiple of 5 words
  - Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words
- Public key algorithms
  - Support RSA public key algorithms: 512/1024/2048/3072/4096-bit width
  - Support ECC public key algorithms: 160/224/256/384/521-bit width
  - Support SM2 algorithms

1.3.9.2 Security ID (SID)

- 4 Kbits eFuse
- Supports secure and non-secure world in eFuse
- The register configuration of SID is always in non-secure world
- Backup eFuse information by using SID_SRAM
- One-time programming
- Selecting double-bit check by parameter definition
- Data scrambling
- Reading and writing protection

1.3.9.3 Secure Memory Control (SMC)

- The SMC is always secure, only secure CPUX can access the SMC
- Sets secure area of DRAM
- Supports Master and address protection
- Sets secure property that Master accesses to DRAM
- Sets DRM area
- Maximum 16 regions and Master has access to each region

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1.3.9.4 Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Sets secure property of peripherals

1.3.10 External Peripherals

1.3.10.1 CIR Receiver (CIR_RX)

- One CIR_RX interface in CPUX domain and one CIR_RX interface in CPUS domain
- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

1.3.10.2 CIR Transmitter (CIR_TX)

- One CIR_TX interface in CPUX domain
- Full physical layer implementation
- Arbitrary wave generator
- Configurable carrier frequency
- Handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer
- Supports Interrupts and DMA

1.3.10.3 GMAC

- One GMAC interface (GMAC) for connecting external Ethernet PHY
- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operations
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters

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- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors

- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies

1.3.10.4 General Purpose ADC (GPADC)

- 4-ch successive approximation register (SAR) analog-to-digital converter (ADC)
- 64 FIFO depth of data register
- 12-bit sampling resolution and 10-bit precision
- Power reference voltage: AVCC, analog input voltage range: 0 to AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

1.3.10.5 LEDC

- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- Configurable interval time between data packets and frame data
- Configurable RGB display mode

1.3.10.6 Low Rate ADC (LRADC)

- 2-ch LRADC input
- 6-bit resolution
- Sampling rate up to 2 KHz
- Supports hold key and general key
- Supports normal, continue and single work mode
- Power supply voltage:1.8V, power reference voltage:1.35V

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1.3.10.7 USB2.0 DRD

- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- USB Host that supports the following:
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root port shared between EHCI and OHCI
- USB Device that supports the following:
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
  - Supports bi-directional endpoint0 (EP0) for Control transfer
  - Up to 10 user-configurable endpoints (EP1 IN/OUT, EP2 IN/OUT, EP3 IN/OUT, EP4 IN/OUT, EP5 IN/OUT) for Bulk transfer, Isochronous transfer and Interrupt transfer
  - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
  - Supports interface to an external Normal DMA controller for every EP
- Supports an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral modes
- Includes automatic PING capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Device and host controller share an 8K SRAM and a physical PHY

1.3.10.8 USB2.0 HOST

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Industry-standard AMBA High-Performance Bus (AHB), fully compliant with the AMBA Specification, Revision 2.0
- 32-bit Little Endian AMBA AHB Slave Bus for Register Access
- 32-bit Little Endian AMBA AHB Master Bus for Memory Access
- An internal DMA Controller for data transfer with memory

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- Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
- Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
- Supports the UTMI+ Level 3 interface and 8-bit bidirectional data buses
- Supports only 1 USB Root port shared between EHCI and OHCI

1.3.10.9 PCIe2.1&USB3.1 System

PCIe2.1&USB3.1 system contains 1 PCIe2.1&USB3.1 combo PHY, 1 PCIe2.1 controller and 1 USB3.1 GEN1 DRD controller.

PCIe2.1

- Complies with PCI Express Base 2.1 Specification
- Only supports Root Complex (RC) mode
- Embedded PCI Express PHY, supports x1 Gen2 (5.0 Gbit/s) lane
- Maximum payload size: 1024 bytes
- Supports 8 Inbound windows and 8 Outbound window
- 4 writing channels and 4 reading channels for embedded DMA
- Supports Message Signaled Interrupts (MSI)

USB3.1 DRD

NOTE

USB2.0 PHY and USB3.1 PHY share the same controller. They cannot be used simultaneously.

- Compliant with USB3.1 GEN1 Specification
- One USB 2.0 UTMI+ PHY (USB2)
- One USB3.1 PIPE PHY (USB3)
- USB3.1 DRD Device mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s) and Full-Speed (FS, 12-Mbit/s) for USB2.0 PHY
- USB3.1 DRD HOST mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) for USB2.0 PHY

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- Supports Device or Host operation at a time
- AXI interface for DMA operation
- Reading and writing access to Control and Status Registers (CSRs) through AHB Slave interface
- Up to 10 Endpoints, including bi-directional control Endpoint 0 in Device mode:
  - 5 IN Endpoints: User EP1 IN, EP2 IN, EP3 IN, EP4 IN, Control EP0 IN
  - 5 OUT Endpoints: User EP1 OUT, EP2 OUT, EP3 OUT, EP4 OUT, Control EP0 OUT
- Simultaneous IN and OUT transfer in Super-Speed mode
- Dual-port interfaces for TX data buffering, RX data prefetching, descriptor caching, and register caching
- Three RAMs: Rx data FIFO RAM, TX data FIFO RAM, and descriptor/register Cache RAM
- Hardware handles all data transfer
- Implements both static and dynamic power reduction techniques at multiple levels

1.3.10.10 PWM

- Up to 30 PWM channels and 4 PWM controllers: PWM [19:0] in CPUX domain, S-PWM [9:0] in CPUS domain
  - PWM [15:0] for PWMCTRL0 controller
  - PWM [19:16] for PWMCTRL1 controller
  - S-PWM [1:0] for S_PWMCTRL controller
  - S-PWM [9:2] for MCU_PWMCTRL controller
- Maximum 16 independent PWM channels for PWM controller
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz (when the clock source is DCXO24M)
    - 0 to 100 MHz (when the clock source is APB1 clock)
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Maximum 8 complementary pairs output
  - The pairing methods for each PWM controller are as follows. The components are internal PWM channels:
    - Maximum 8 pairs for PWMCTRL0:

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PWM0 + PWM1, PWM2 + PWM3, PWM4 + PWM5, PWM6 + PWM7, PWM8 + PWM9, PWM10 + PWM11, PWM12 + PWM13, PWM14 + PWM15

- Maximum 2 pairs for PWMCTRL1:

  PWM0+PWM1, PWM2+PWM3

- Maximum 1 pair for S_PWMCTRL:

  PWM0+PWM1

- Maximum 4 pairs for MCU_PWMCTRL:

  PWM0+PWM1, PWM2+PWM3, PWM4+PWM5, PWM6+PWM7

  - Supports dead-zone generator, and the dead-zone time is configurable

- Maximum 4 group of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Maximum 16 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

1.3.10.11 SPI and SPI_DBI

- Up to 4 SPI controllers
  - SPI0, SPI1, and SPI2 in CPUX Domain
  - S-SPI0 in CPUS Domain
- The SPI0, SPI2, and S-SPI0 support SPI mode; The SPI1 supports SPI mode and display bus interface (DBI) mode

SPI mode

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmmable serial data frame length of 1 bit to 32 bits
- Maximum clock frequency: 100MHz
- TX/RX DMA slave interface
- 8-bit wide by 64-entry FIFO for both transmitting and receiving data

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- Supports mode0, mode1, mode2, and mode3
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

DBI mode

- DBI Type C 3 Line/4 Line Interface Mode
- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

1.3.10.12 SPI Flash Controller (SPIFC)

- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports STR mode and DTR mode, and DTR mode supports DQS signal
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Software Write Protection
  - Write protection for all/portion of memory via software
  - Top/Bottom Block protection
- Programmable delay between transactions
- Supports Mode0, Mode1, Mode2 and Mode3
- Supports control signal configuration
  - Up to four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

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1.3.10.13 Two Wire Interface (TWI)

- Up to 9 TWI controllers
  - 6 TWI controllers in CPUX domain: TWI0, TWI1, TWI2, TWI3, TWI4, and TWI5
  - 3 TWI controllers in CPUS domain: S_TWI0, S_TWI1, and S_TWI2
- Compliant with I2C bus standard
- 7-bit and 10-bit device addressing modes
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports general call and start byte
- Master mode supports the following:
  - Bus arbitration in the case of multiple master devices
  - Clock synchronization and bit and byte waiting
  - Packet transmission and DMA
- Slave mode supports Interrupt on address detection

1.3.10.14 UART

- Up to 10 UART controllers
  - 8 UART controllers in CPUX domain: UART0, UART1, UART2, UART3, UART4, UART5, UART6, and UART7
  - 2 UART controllers in CPUS domain: S_UART0 and S_UART1
- Compatible with industry-standard 16450/16550 UARTs
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes for UART0, S_UART0, and S_UART1
  - Each of them is 128 bytes for UART1, UART2, UART3, UART4, UART5, UART6, and UART7
- The working reference clock is from the APB bus clock
  - Speed up to 10 Mbit/s with 160 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 5 Mbit/s with 80 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 3.75 Mbit/s with 60 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 format, or 9 bits RS-485 format
- 1, 1.5 or 2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface

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- Supports software/hardware flow control
- Supports IrDA-compatible slow infrared (SIR) format
- Supports auto-flow by using CTS & RTS (excluding UART0, S_UART0, and S_UART1)

1.3.11 Package

FCCSP 522 balls, 15 mm x 15 mm body size, 0.5 mm ball pitch, 0.3 mm ball size

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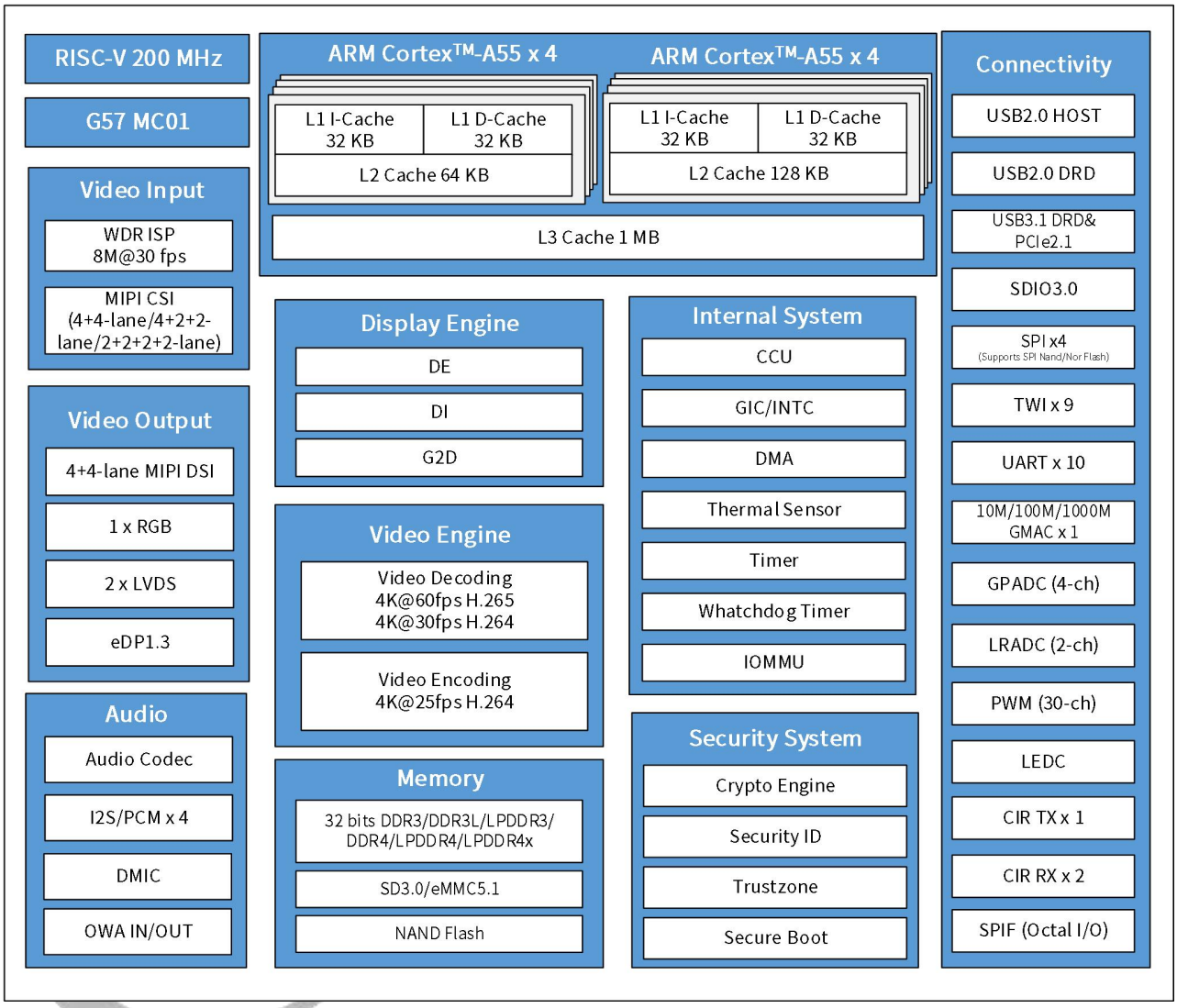
1.4 Block Diagram

The following figure shows the system block diagram of the A523.

Figure 1-1 A523 System Block Diagram



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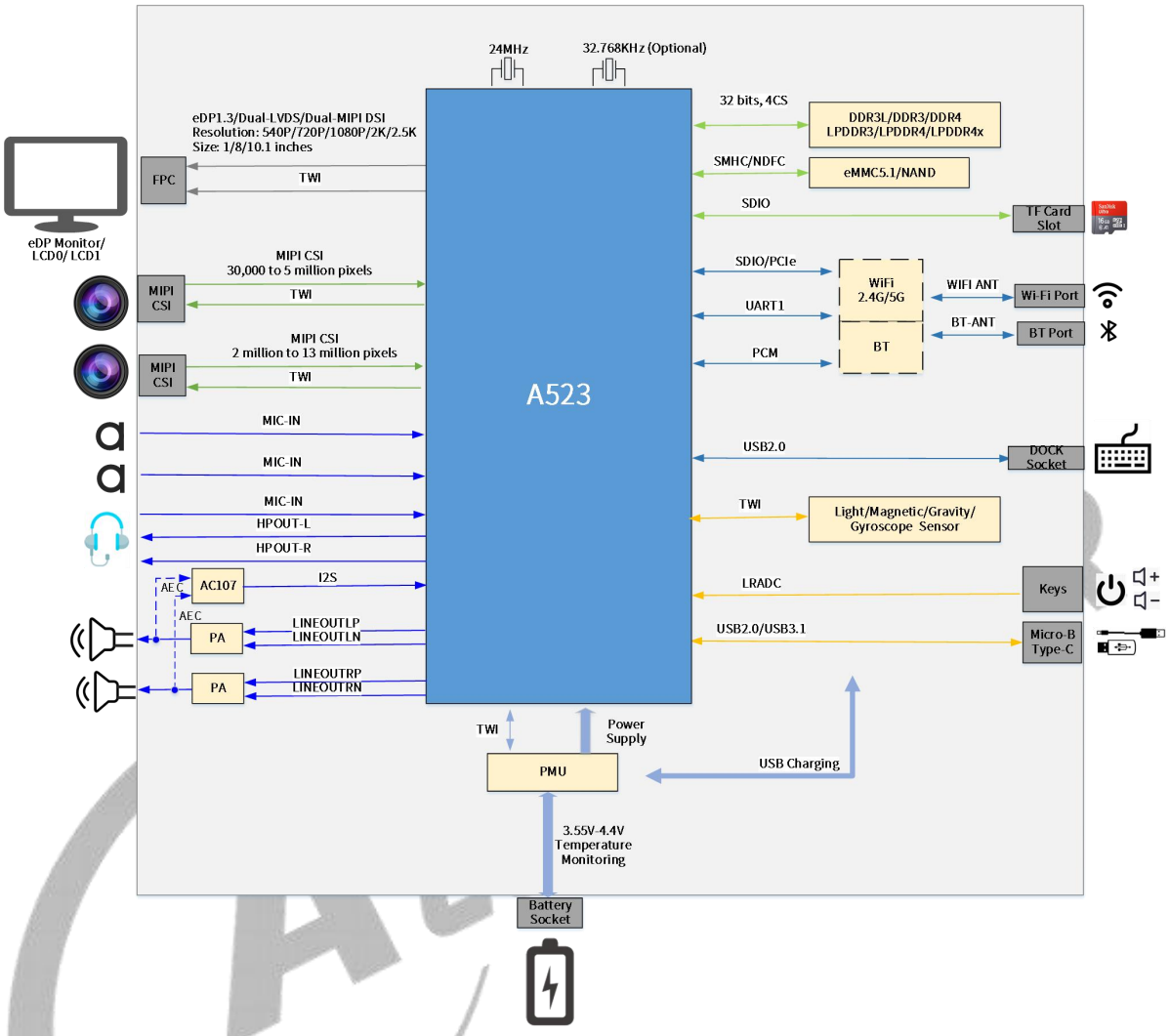
The following figure shows the medium- and high-end tablet solution of the A523.

Figure 1-2 Medium and High-End Tablet Solution



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Figures

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Tables

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2 System

2.1 Memory Mapping

Module	Address	Size(Bytes)
BROM & SRAM		
S_BROM	0x0000 0000---0x0000 AFFF	44 KB
M_BROM	0x0001 0000---0x0001 8FFF	36 KB
MCU0 SRAM	0x0002 0000---0x0003 FFFF	128 KB The local SRAM is switched to system boot.
SRAM A2	0x0004 0000---0x0006 3FFF	16 KB+128 KB
GPU_SYS		
GPU	0x0180 0000---0x0183 FFFF	256 KB
VE_SYS		
VE	0x01C0 E000---0x01C0 EFFF	4 KB
SP0		
GPIO	0x0200 0000---0x0200 07FF	2 KB
SPC	0x0200 0800---0x0200 0BFF	1 KB
PWMCTRL0	0x0200 0C00---0x0200 0FFF	1 KB
CCU	0x0200 1000---0x0200 1FFF	4 KB
CIR_TX	0x0200 3000---0x0200 33FF	1 KB
CIR_RX	0x0200 5000---0x0200 53FF	1 KB
LEDC	0x0200 8000---0x0200 83FF	1 KB
GPADC	0x0200 9000---0x0200 93FF	1 KB
THS1	0x0200 9400---0x0200 97FF	1 KB
LRADC	0x0200 9800---0x0200 9BFF	1 KB
THS0	0x0200 A000---0x0200 A3FF	1 KB
IOMMU	0x0201 0000---0x0201 FFFF	64 KB
NSI	0x0202 0000---0x0202 FFFF	64 KB
CPUX_WDT	0x0205 0000---0x0205 0FFF	4 KB
PWMCTRL1	0x0205 1000---0x0205 13FF	1 KB
NSI_CPU	0x0207 1000---0x0207 13FF	1 KB
SP1		
UART0	0x0250 0000---0x0250 03FF	1 KB
UART1	0x0250 0400---0x0250 07FF	1 KB
UART2	0x0250 0800---0x0250 0BFF	1 KB
UART3	0x0250 0C00---0x0250 0FFF	1 KB

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Module	Address	Size(Bytes)
UART4	0x0250 1000---0x0250 13FF	1 KB
UART5	0x0250 1400---0x0250 17FF	1 KB
UART6	0x0250 1800---0x0250 1BFF	1 KB
UART7	0x0250 1C00---0x0250 1FFF	1 KB
TWI0	0x0250 2000---0x0250 23FF	1 KB
TWI1	0x0250 2400---0x0250 27FF	1 KB
TWI2	0x0250 2800---0x0250 2BFF	1 KB
TWI3	0x0250 2C00---0x0250 2FFF	1 KB
TWI4	0x0250 3000---0x0250 33FF	1 KB
TWI5	0x0250 3400---0x0250 37FF	1 KB
SH0		
SYSCTRL	0x0300 0000---0x0300 0FFF	4 KB
CPUX_TIMER	0x0300 8000---0x0300 83FF	1 KB
DMAC	0x0300 2000---0x0300 2FFF	4 KB
CPUX_MSGBOX	0x0300 3000---0x0300 3FFF	4 KB
SPINLOCK	0x0300 5000---0x0300 5FFF	4 KB
SID	0x0300 6000---0x0300 6FFF	4 KB
CE_NS	0x0304 0000---0x0304 07FF	2 KB
CE_S	0x0304 0800---0x0304 0FFF	2 KB
MEMC	0x0310 2000---0x0330 1FFF	2 M
MEMC_SMC	0x0311 0000---0x0311 FFFF	64 KB
MEMC_COMMON	0x0312 0000---0x0312 FFFF	64 KB
MEMC_DDRC	0x0313 0000---0x0313 FFFF	64 KB
MEMC_PHY	0x0314 0000---0x0314 FFFF	64 KB
GIC	0x0340 0000---0x034E FFFF	15*64 KB
SH2		
NDFC	0x0401 1000---0x0401 1FFF	4 KB
SMHC0	0x0402 0000---0x0402 0FFF	4 KB
SMHC1	0x0402 1000---0x0402 1FFF	4 KB
SMHC2	0x0402 2000---0x0402 2FFF	4 KB
SPI0	0x0402 5000---0x0402 5FFF	4 KB
SPI1	0x0402 6000---0x0402 6FFF	4 KB
SPI2	0x0402 7000---0x0402 7FFF	4 KB
USB0	0x0410 0000---0x041F FFFF	1 MB
USB1	0x0420 0000---0x042F FFFF	1 MB
GMAC	0x0450 0000---0x0450 FFFF	64 KB
SPIFC	0x047F 0000---0x047F 0FFF	4 KB
PCIE	0x0480 0000---0x04CF FFFF	5 MB
USB3	0x04D0 0000---0x04EF FFFF	2 MB
PCIE_USB3_TOP_AP	0x04F0 0000---0x04F7 FFFF	512 KB

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Module	Address	Size(Bytes)
P		
DE_SYS		
DE	0x0500 0000---0x053F FFFF	4 MB
DI	0x0540 0000---0x0543 FFFF	256 KB
G2D	0x0544 0000---0x0547 FFFF	256 KB
VIDEO0_OUT_SYS		
DISPLAY0_TOP	0x0550 0000---0x0550 0FFF	4 KB
TCON_LCD0	0x0550 1000---0x0550 1FFF	4 KB
TCON_LCD1	0x0550 2000---0x0550 2FFF	4 KB
TCON_TV1	0x0550 4000---0x0550 4FFF	4 KB
COMBOPHY_DSI0	0x0550 6000---0x0550 7FFF	8 KB
COMBOPHY_DSI1	0x0550 8000---0x0550 9FFF	8 KB
EDP	0x0572 0000---0x0572 3FFF	16 KB
VIDEO_IN_SYS		
CSI	0x0580 0000---0x058F FFFF	1 MB
ISP	0x0590 0000---0x05CF FFFF	4 MB
APBS0		
S_PPU1	0x0700 1400---0x0700 17FF	1 KB
S_SPC	0x0700 2000---0x0700 23FF	1 KB
PRCM	0x0701 0000---0x0701 FFFF	64 KB
CPUS_WDT	0x0702 0400---0x0702 07FF	1 KB
S_TWD	0x0702 0800---0x0702 0BFF	1 KB
S_PWMCTRL	0x0702 0C00---0x0702 0FFF	1 KB
S_INTC	0x0702 1000---0x0702 13FF	1 KB
S_GPIO	0x0702 2000---0x0702 27FF	2 KB
CPUS_CFG	0x0703 1000---0x0703 1FFF	4 KB
S_CIRRX	0x0704 0000---0x0704 03FF	1 KB
PCK600_CPU	0x0705 0000---0x0705 FFFF	64 KB
PCK600_QCHANNEL(S_PPU)	0x0706 0000---0x0706 7FFF	32 KB
APBS1		
S_UART0	0x0708 0000---0x0708 03FF	1 KB
S_UART1	0x0708 0400---0x0708 07FF	1 KB
S_TWI0	0x0708 1400---0x0708 17FF	1 KB
S_TWI1	0x0708 1800---0x0708 1BFF	1 KB
S_TWI2	0x0708 1C00---0x0708 1FFF	1 KB
AHBS		
RTC	0x0709 0000---0x0709 03FF	1 KB
CPUS_TIMER	0x0709 0400---0x0709 07FF	1 KB
S_SPI0	0x0709 2000---0x0709 2FFF	4 KB
S_SPINLOCK	0x0709 3000---0x0709 3FFF	4 KB

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Module	Address	Size(Bytes)
CPUS_MSGBOX	0x0709 4000---0x0709 4FFF	4 KB
MCU_APB0		
MCU_PRCM	0x0710 2000---0x0710 2FFF	4 KB
MCU_PWMCTRL	0x0710 3000---0x0710 33FF	1 KB
AUDIO CODEC	0x0711 0000---0x0711 0FFF	4 KB
DMIC	0x0711 1000---0x0711 13FF	1 KB
I2S0	0x0711 2000---0x0711 2FFF	4 KB
I2S1	0x0711 3000---0x0711 3FFF	4 KB
I2S2	0x0711 4000---0x0711 4FFF	4 KB
I2S3	0x0711 5000---0x0711 5FFF	4 KB
OWA	0x0711 6000---0x0711 63FF	1 KB
MCU_AHB		
MCU_DMAC	0x0712 1000---0x0712 1FFF	4 KB
MCU_TIMER	0x0712 3000---0x0712 33FF	1 KB
RISCV_SYS		
RISCV_CFG	0x0713 0000---0x0713 0FFF	4 KB
RISCV_WDT	0x0713 2000---0x0713 2FFF	4 KB
RISCV_LCNT	0x0713 4000---0x0713 4FFF	4 KB
RISCV_MSGBOX	0x0713 6000---0x0713 6FFF	4 KB
MCU_SRAM		
SRAMA3_0	0x0728 0000---0x072B FFFF	256 KB (SRAMA3_0 can not be used cross 256 KB boundary)
SRAMA3_1	0x072C 0000---0x072F FFFF	256 KB (SRAMA3_1 can not be used cross 256 KB boundary)
SRAMA3_2	0x0730 0000---0x0737 FFFF	512 KB
CPUX Related		
CPU_SUBSYS_CTRL	0x0800 0000---0x0800 0FFF	4 KB
TIMESTAMP_STA	0x0801 0000---0x0801 0FFF	4 KB
TIMESTAMP_CTRL	0x0802 0000---0x0802 0FFF	4 KB
APB_ROM1	0x0880 1000---0x0880 1FFF	4 KB
CTI	0x0880 3000---0x0880 3FFF	4 KB
CS_TS_CTRL	0x0880 5000---0x0880 5FFF	4 KB
CS_TS_READ	0x0880 7000---0x0880 7FFF	4 KB
TPIU	0x0880 9000---0x0880 9FFF	4 KB
ETB	0x0880 B000---0x0880 BFFF	4 KB
APB_ROM2	0x0881 1000---0x0881 1FFF	4 KB
ATB_FUNNEL	0x0881 3000---0x0881 3FFF	4 KB
CLUSTER_CFG	0x0881 5000---0x0881 5FFF	4 KB
CPU_PLL_CFG	0x0881 7000---0x0881 7FFF	4 KB
CLUSTER_DBUG	0x0980 0000---0x09BF FFFF	4 MB

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Module	Address	Size(Bytes)
PCIE		
PCIE_SLV	0x2000 0000---0x2FFF FFFF	256 MB
RISCV Related (Only RISC-V access)		
RISCV_CLINT	0xE000 0000---0xE000 FFFF	64 KB
RISCV_CLIC	0xE080 0000---0xE080 4FFF	20 KB
RISCV_SYSMAP	0xEFFF F000---0xEFFF FFFF	4 KB
DRAM Space		
DRAM SPACE	0x4000 0000---0x13FFF FFFF	4 GB RISC-V core accesses the DRAM address: 0x4004 0000---0x7FFF FFFF

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2.2 ARM Cortex™-A55 System(CPUX)

2.2.1 Overview

A523 CPU architecture adopts DynamIQ technology. The CPUX system includes DynamIQ Shared Unit (DSU), DynamIQ cluster, GIC600 distributor, coresight subsystem, and timestamp module. The features of the CPUX cores and DSU in DynamIQ cluster are as follows.

CPUX Cores

- Two sets of ARM Cortex™-A55 cores in a DynamIQ big. LITTLE configuration
- Memory subsystem features
  - 32 KB L1 I-cache and D-cache
  - Optional 64KB L2 cache for 'LITTLE' cores
  - Optional 128KB L2 cache for 'big' cores
  - Separate L1 instruction side memory subsystem with a Memory Management Unit (MMU)
- A64, A32, and T32 instruction sets running on ARMv8-A architecture ISA
- Both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3).
- In-order pipeline with direct and indirect branch prediction.
- Optional Data Engine Unit implementing the advanced Single Instruction Multiple Data (SIMD) and floating-point architecture
- Optional Cryptography extensions
- Separate L1 instruction side memory system with a Memory Management Unit (MMU)
- ARM TrustZone® technology
- Generic Interrupt Controller (GIC) interface connecting an external distributor
- Generic Timers interface supporting 64-bit count input from an external system counter
- Reliability, Availability, and Serviceability (RAS) extension
- Debug and trace capabilities

NOTE

Cryptography extensions are available only when Data Engine unit is present.

DSU

DSU comprises the L3 cache, the Snoop Control Unit (SCU), internal interfaces to the cores, and external interfaces to the SoC.

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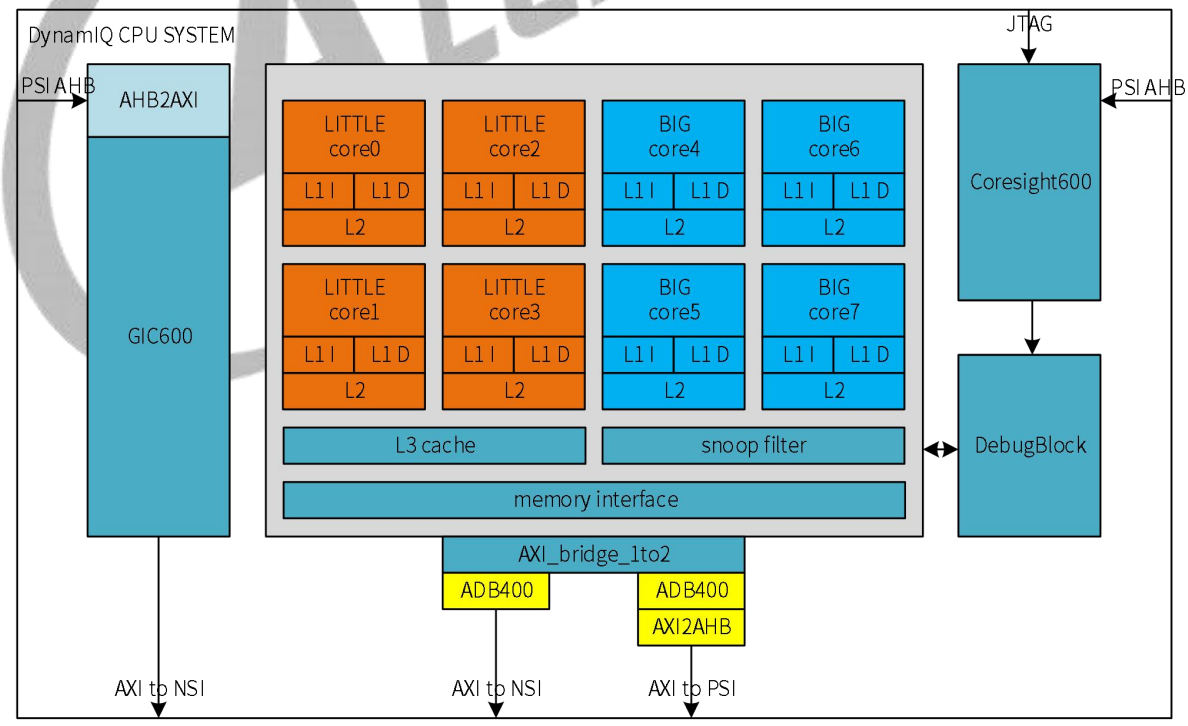
- Memory subsystem features
  - 1024 KB L3 cache
  - Optional 16-way set-associative L3 cache, 64-byte cache line
  - L3 memory system can be clocked at a rate synchronous to the external system interconnect or at integer multiples.
  - L3 cache partial power down
  - Optional cache protection in the form of Error Correcting Code (ECC) on L3 cache RAM instances
  - 40-bit, 44-bit, and 48-bit physical addresses
- Main bus interface adopting AMBA 5 ACE protocol or AMBA 5 CHI protocol
- Optional 128-bit wide and I/O-coherent Accelerator Coherency Port (ACP)
- Optional 64-bit wide peripheral port
- ARMv8.2 debug logic
- Supports RAS

2.2.2 Block diagram

The following figure shows the block diagram of CPUX system.

Figure 2-1 CPUX System Block Diagram



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The following table describes the components of A523 DynamIQ big. LITTLE cluster.

Table 2-1 CPUX DynamIQ Cluster Components

Components	Description
CPU bridges	For communication between cores and DSU buffers.
SCU	The SCU maintains coherency and cache-to-cache transmission for all CPUX cores.
Debug and trace components	Each core allows tracing supported by Embedded Trace Macrocell (ETM). The trigger events from CPUX cores are transmitted through debug APB master/slave interface.
Clock and power management	The cluster supports low power mode and is controlled by a low power control module outside the cluster power-down domain. DSU and each CPUX core has independent P-channels. They could control the power mode through P-channels.
L3 memory interfaces	To access memory and peripherals.
DSU system control registers	Include information related to CPUX core configuration, such as: • Power management of the cluster • QOS and ID control of CHI bus • DSU hardware configuration information • L3 cache hit and miss count information

2.2.3 Functional Descriptions

2.2.3.1 Power Block System

Power Domain

The following table describes the power domain of the CPUX.

Table 2-2 CPUX Power domain

Power Domain	Power Switch	Description
VDD-CPUB	Yes	Power source of Core4-Core7. It is controlled by the PPU for each core.
VDD-CPUL	Yes	Power source of the cluster top and Core0-Core3. It is controlled by the PPU for the cluster top and each core.
VDD-SYS	No	Power source of CPUX system excluding the cluster top and CPUX cores. It is the same power supply of the SoC system.

Power Mode

CPUX cores support four power modes:

- Debug Recovery
- ON

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- OFF (emulated)
- OFF

DSU supports the following power modes

- ON: SFONLY_ON、1/4 ON、1/2 ON、3/4 ON、FULL ON
- Functional Retention: SFONLY FUNC_RET, ¼FUNC_RET, ½FUNC_RET, ¾FUNC_RET, FULL FUNC_RET
- OFF and OFF_EMU

2.2.3.2 CPU PLL Distribution and Clock Sources

The CPUX system contains three linear frequency modulation PLLs: CPU_L_PLL, CPU_DSU_PLL, and CPU_B_PLL. The following table shows the clock sources of CPUX cores and DSU.

Table 2-3 Clock Sources of CPUX Cores and DSU

CPUX Cores	Clock Sources	Description
Core0-Core3	CLK32K	• Generally, CPU_L_PLL is the main clock source of Core0-Core3. For all clock sources of Core0-Core3, refer to CPUA_CLK_REG register. • Generally, CPU_B_PLL is the main clock source of Core4-Core7. For all clock sources of Core4-Core7, refer to CPUB_CLK_REG register. • Generally, CPU_DSU_PLL is the main clock source of DSU. For all clock sources of DSU, refer to DSU_CLK_REG register.
	CLK16M_RC	
	HOSC	
	PERI0_600M	
	CPU_L_PLL	
Core4-Core7	CLK32K	
	CLK16M_RC	
	HOSC	
	PERI0_600M	
	CPU_PLL3CPU_B_PLL	
DSU	CLK32K	
	CLK16M_RC	
	HOSC	
	PERI0_600M	
	PLL_PERI0(2X)	
	CPU_DSU_PLL	

2.2.3.3 CPUX Reset System

The following table shows the input reset signal of the whole CPUX system.

Table 2-4 Reset signal description of CPUX System

Reset signal	Source	Description
DBGSYS_RST	CCU	For detailed information, please refer to the description of DBGSYS_RST in section 2.5.6.70 0x078C DBGSYS Bus Gating Reset

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Reset signal	Source	Description
		Register (Default Value: 0x0000_0000).
DSU_RSTN	PPU	Whether to reset is controlled by PPU according to the power mode.
CORE_RSTN	PPU	Whether to reset is controlled by PPU according to the power mode.

2.2.4 Programming Guidelines

The following takes CPU_L_PLL as an example, CPU_DSU_PLL and CPU_B_PLL are the same.

NOTE

It is not suggested to enable or disable the PLLs during usage. When the clock is not required, it is recommended to configure the PLL_OUTPUT_EN bit of PLL control register as 0.

2.2.4.1 Enabling the Linear Frequency Modulation PLLs

Step 1 Write 1 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

Step 2 Configure the N, M, and P factors of the CPU_L_PLL_CTRL_REG register.

Step 3 Write 1 to the PLL_PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the CPU_L_PLL_CTRL_REG register.

Step 4 Write 1 to the LOCK_ENABLE bit (bit [29]) of the CPU_L_PLL_CTRL_REG register.

Step 5 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register.

Step 6 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 7 Wait for the status of the Lock to change to 1.

Step 8 Delay 10 ms.

Step 9 Write 0 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

2.2.4.2 Configuring the Frequency of Linear Frequency Modulation PLLs

Step 1 Configure the PLL_SSC_STEP bit (bit [3:0]) of the CPU_L_PLL_SSC_REG register to select required frequency modulation slope.

Step 2 Configure the PLL_SSC bit (bit [28:12]) of the CPU_L_PLL_SSC_REG register to set the SSC ampltitude.

Step 3 Write 1 to the PLL_SSC_MODE bit (bit [31]) of the CPU_L_PLL_SSC_REG register to enable linear frequency modulation.

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Step 4 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register to update PLL configuration parameters.

Step 5 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 6 Configure the N factor of the CPU_L_PLL_CTRL_REG register.

Step 7 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register to update PLL configuration parameters.

Step 8 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 9 Write 0 to the PLL_SSC_MODE bit (bit [31]) of the CPU_L_PLL_SSC_REG register to disable linear frequency modulation.

Step 10 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register to update PLL configuration parameters.

Step 11 Wait for the value of the PLL_UPDATE bit to change to 0.

2.2.4.3 Disabling the Linear Frequency Modulation PLLs

Follow the steps below to disable the PLL:

Step 1 Write 0 to the PLL_PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the CPU_L_PLL_CTRL_REG register.

Step 2 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register.

Step 3 Write 1 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

Step 4 Write 1 to the PLL_UPDATE bit (bit [26]) of the CPU_L_PLL_CTRL_REG register.

Step 5 Wait for the value of the PLL_UPDATE bit to change to 0.

Step 6 Write 0 to the PLL_SSC_CLK_SEL bit (bit [29]) of CPU_L_PLL_SSC_REG register.

2.2.5 Register list

Module Name	Base Address	Description
CPU_SUBSYS_CTRL	0x08000000	CPU Subsystem Control (4KB)
TIMESTAMP_STA	0x08010000	Timestamp Status Registers (4KB)
TIMESTAMP_CTRL	0x08020000	Timestamp Control Registers (4KB)
CPU_PLL_CFG	0x08817000	Cluster PLL configure (4KB)

2.2.5.1 CPU_SUBSYS_CTRL Register List

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0

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Register Name	Offset	Description
GIC_JTAG_RST_CTRL	0x000C	GIC and JTAG reset control Register
DBG_STATE	0x001C	Debug State Register
CPU0_CTRL_REG	0x0020	CPU0 Control Register
CPU1_CTRL_REG	0x0024	CPU1 Control Register
CPU2_CTRL_REG	0x0028	CPU2 Control Register
CPU3_CTRL_REG	0x002C	CPU3 Control Register
CPU4_CTRL_REG	0x0030	CPU4 Control Register
CPU5_CTRL_REG	0x0034	CPU5 Control Register
CPU6_CTRL_REG	0x0038	CPU6 Control Register
CPU7_CTRL_REG	0x003C	CPU7 Control Register
RVBARADDR0_L	0x0040	Reset Vector Base Address Register0_L
RVBARADDR0_H	0x0044	Reset Vector Base Address Register0_H
RVBARADDR1_L	0x0048	Reset Vector Base Address Register1_L
RVBARADDR1_H	0x004c	Reset Vector Base Address Register1_H
RVBARADDR2_L	0x0050	Reset Vector Base Address Register2_L
RVBARADDR2_H	0x0054	Reset Vector Base Address Register2_H
RVBARADDR3_L	0x0058	Reset Vector Base Address Register3_L
RVBARADDR3_H	0x005C	Reset Vector Base Address Register3_H
RVBARADDR4_L	0x0060	Reset Vector Base Address Register4_L
RVBARADDR4_H	0x0064	Reset Vector Base Address Register4_H
RVBARADDR5_L	0x0068	Reset Vector Base Address Register5_L
RVBARADDR5_H	0x006c	Reset Vector Base Address Register5_H
RVBARADDR6_L	0x0070	Reset Vector Base Address Register6_L
RVBARADDR6_H	0x0074	Reset Vector Base Address Register6_H
RVBARADDR7_L	0x0078	Reset Vector Base Address Register7_L
RVBARADDR7_H	0x007C	Reset Vector Base Address Register7_H
PLL_CTRL_REG0	0x0140	PLL control register 0
PLL_CTRL_REG1	0x0144	PLL control register 1

2.2.5.2 TIMESTAMP_STA Register List

Register Name	Offset	Description
CNTCVLREAD	0x0000	Current value of Counter[31:0]
CNTCVUREAD	0x0004	Current value of Counter[63:32]
PIDR4	0x0FD0	Peripheral Identification Register 4
PIDR5	0x0FD4	Peripheral Identification Register 5
PIDR6	0x0FD8	Peripheral Identification Register 6
PIDR7	0x0FDC	Peripheral Identification Register 7
PIDR0	0x0FE0	Peripheral Identification Register 0
PIDR1	0x0FE4	Peripheral Identification Register 1
PIDR2	0x0FE8	Peripheral Identification Register 2

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Register Name	Offset	Description
PIDR3	0x0FEC	Peripheral Identification Register 3
CIDR0	0x0FF0	Component Identification Register 0
CIDR1	0x0FF4	Component Identification Register 1
CIDR2	0x0FF8	Component Identification Register 2
CIDR3	0x0FFc	Component Identification Register 3

2.2.5.3 TIMESTAMP_CTRL Register List

Register Name	Offset	Description
CNTCR	0x0000	Counter Control Register
CNTSR	0x0004	Counter Status Register
CNTCVL	0x0008	Current value of Counter[31:0]
CNTCVU	0x000c	Current value of Counter[63:32]
CNTFID0	0x0020	Base Frequency ID register
ITSTAT	0x0EF8	Integration Test Status Register
ITCTRL	0x0F00	Integration Mode Control Register
PIDR4	0x0FD0	Peripheral Identification Register 4
PIDR5	0x0FD4	Peripheral Identification Register 5
PIDR6	0x0FD8	Peripheral Identification Register 6
PIDR7	0x0FDC	Peripheral Identification Register 7
PIDR0	0x0FE0	Peripheral Identification Register 0
PIDR1	0x0FE4	Peripheral Identification Register 1
PIDR2	0x0FE8	Peripheral Identification Register 2
PIDR3	0x0FEC	Peripheral Identification Register 3
CIDR0	0x0FF0	Component Identification Register 0
CIDR1	0x0FF4	Component Identification Register 1
CIDR2	0x0FF8	Component Identification Register 2
CIDR3	0x0FFc	Component Identification Register 3

2.2.5.4 CPU_PLL_CTRL Register List

Register Name	Offset	Description
CPU_L_PLL_CTRL_REG	0x0004	CPU_L_PLL Control Register
CPU_DSU_PLL_CTRL_REG	0x0008	CPU_DSU_PLL Control Register
CPU_B_PLL_CTRL_REG	0x000c	CPU_B_PLL Control Register
CPU_L_PLL__PAT0_CTRL_REG	0x0010	CPU_L_PLL Pattern0 Control Register
CPU_L_PLL__PAT1_CTRL_REG	0x0014	CPU_L_PLL Pattern1 Control Register
CPU_DSU_PLL__PAT0_CTRL_REG	0x0018	CPU_DSU_PLL Pattern0 Control Register
CPU_DSU_PLL__PAT1_CTRL_REG	0x001c	CPU_DSU_PLL Pattern1 Control Register
CPU_B_PLL__PAT0_CTRL_REG	0x0020	CPU_B_PLL Pattern0 Control Register
CPU_B_PLL__PAT1_CTRL_REG	0x0024	CPU_B_PLL Pattern1 Control Register

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Register Name	Offset	Description
CPU_L_PLL_BIAS_REG	0x002c	CPU_L_PLL Bias Register
CPU_DSU_PLL_BIAS_REG	0x0030	CPU_DSU_PLL Bias Register
CPU_B_PLL_BIAS_REG	0x0034	CPU_B_PLL Bias Register
CPU_L_PLL_TUN0_REG	0x003C	CPU_L_PLL Tuning0 Control Register
CPU_L_PLL_TUN1_REG	0x0040	CPU_L_PLL Tuning1 Control Register
CPU_DSU_PLL_TUN0_REG	0x0044	CPU_DSU_PLL Tuning0 Control Register
CPU_DSU_PLL_TUN1_REG	0x0048	CPU_DSU_PLL Tuning1 Control Register
CPU_B_PLL_TUN0_REG	0x004C	CPU_B_PLL Tuning0 Control Register
CPU_B_PLL_TUN1_REG	0x0050	CPU_B_PLL Tuning1 Control Register
CPU_L_PLL_SSC_REG	0x0054	CPU_L_PLL SSC Register
CPU_DSU_PLL_SSC_REG	0x0058	CPU_DSU_PLL SSC Register
CPU_B_PLL_SSC_REG	0x005c	CPU_B_PLL SSC Register
CPUA_CLK_REG	0x0060	CPUA Clock Register
CPUB_CLK_REG	0x0064	CPUB Clock Register
CPU_GATING_REG	0x0068	CPU Gating Configuration Register
DSU_CLK_REG	0x006c	DSU Clock Register
PLL_TEST_CLK_SEL	0x0070	PLL Test Clock Selection Register

2.2.6 CPU_SUBSYS_CTRL Register Description

2.2.6.1 0x0000 General Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GENER_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	GICCDISABLE DEBUGBLOCK Control
0	R/W	0x0	CDBGRSTACK Debug Reset ACK

2.2.6.2 0x000C GIC and JTAG Reset Control Register (Default Value: 0x0000_003F)

Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	EXM_CLR [3:0] Clear the status of interface, for debug
15:7	/	/	/
6	R/W	0x1	GIC_DBG_RSTN GIC OUTRE Reset 0: Assert

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Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	Read/Write	Default/Hex	Description
			1: De-assert.
5	R/W	0x1	GIC_OUT_RSTN GIC OUTRE Reset 0: Assert 1: De-assert.
4	R/W	0x1	GIC_OUT_MBIST_RSTN GIC OUTER MBIST Reset 0: Assert 1: De-assert.
3	R/W	0x1	COREPLL_RST COREPLL Reset 0: Assert 1: De-assert.
2	R/W	0x1	CS_RST CoreSight Reset 0: Assert 1: De-assert.
1	R/W	0x1	PORTRST JTAG Portrst 0: Assert 1: De-assert.
0	R/W	0x1	TRST Jtag TRST 0: Assert 1: De-assert.

2.2.6.3 0x001C Debug State Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DBG_STATE
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CLU_PWRSW_STA
23:0	/	/	/

2.2.6.4 0x0020 CPU0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CPU0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU0 AA64NAA32 Register Width State

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Offset: 0x0020			Register Name: CPU0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.5 0x0024 CPU1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CPU1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU1 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor

2.2.6.6 0x0028 CPU2 Control Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CPU2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU2 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.7 0x002C CPU3 Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CPU3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU3 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

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2.2.6.8 0x0030 CPU4 Control Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CPU4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU4 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.9 0x0034 CPU5 Control Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CPU5_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU5 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.10 0x0038 CPU6 Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CPU6_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU6 AA64NAA32 Register Width State: 0: AArch32 1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.11 0x003C CPU7 Control Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	Cluster 0 CPU7 AA64NAA32 Register Width State: 0: AArch32

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Offset: 0x003C			Register Name: CPU7_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			1: AArch64 This pin is sampled only during reset of the processor.

2.2.6.12 0x0040 Reset Vector Base Address Register0_L (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: RVBARADDR0_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU0.
1:0	/	/	/

2.2.6.13 0x0044 Reset Vector Base Address Register0_H (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: RVBARADDR0_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU0.

2.2.6.14 0x0048 Reset Vector Base Address Register1_L (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: RVBARADDR1_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU1.
1:0	/	/	/

2.2.6.15 0x004C Reset Vector Base Address Register1_H (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: RVBARADDR1_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU1.

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2.2.6.16 0x0050 Reset Vector Base Address Register2_L (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: RVBARADDR2_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU2.
1:0	/	/	/

2.2.6.17 0x0054 Reset Vector Base Address Register2_H (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: RVBARADDR2_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU2.

2.2.6.18 0x0058 Reset Vector Base Address Register3_L (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: RVBARADDR3_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU3.
1:0	/	/	/

2.2.6.19 0x005C Reset Vector Base Address Register3_H (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: RVBARADDR3_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU3.

2.2.6.20 0x0060 Reset Vector Base Address Register4_L (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: RVBARADDR4_L
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0060			Register Name: RVBARADDR4_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU4.
1:0	/	/	/

2.2.6.21 0x0064 Reset Vector Base Address Register4_H (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: RVBARADDR4_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU4.

2.2.6.22 0x0068 Reset Vector Base Address Register5_L (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: RVBARADDR5_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU5.
1:0	/	/	/

2.2.6.23 0x006C Reset Vector Base Address Register5_H (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: RVBARADDR5_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU5.

2.2.6.24 0x0070 Reset Vector Base Address Register6_L (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: RVBARADDR6_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU6.

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Offset: 0x0070			Register Name: RVBARADDR6_L
Bit	Read/Write	Default/Hex	Description
1:0	/	/	/

2.2.6.25 0x0074 Reset Vector Base Address Register6_H (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: RVBARADDR6_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU6.

2.2.6.26 0x0078 Reset Vector Base Address Register7_L (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: RVBARADDR7_L
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	RVBARADDR [31:2] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU7.
1:0	/	/	/

2.2.6.27 0x007C Reset Vector Base Address Register7_H (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: RVBARADDR7_H
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	RVBARADDR [39:32] Reset Vector Base Address [39:2] for executing in 64-bit state (AArch64) of CPU7.

2.2.6.28 0x0140 PLL Control Register 0 (Default: 0x0000_0007)

Offset: 0x0140			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL Test Clock Selection 0: XTAL. 1: External Clock
23:3	/	/	/

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Offset: 0x0140			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
2	R/W	0x1	GM1 XTAL Gain Control Bit1
1	R/W	0x1	GM0 XTAL Gain Control Bit0
0	R/W	0x1	PLL_BIAS_EN PLL Bias Enable 0: Disable 1: Enable.

2.2.6.29 0x0144 PLL Control Register 1 (Default: 0x00040005)

Offset: 0x0144			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD Key Field for LDO Enable bit If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/
18:16	R/W	0x4	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control 000: 0.90 V 001: 0.94 V 010: 0.98 V 011: 1.02 V 100: 1.06 V 101: 1.10 V 110: 1.14 V 111: 1.18 V
15:5	/	/	/
4	R/W	0x0	MBIAS_EN Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias
3	R/W	0x0	PLLTEST_EN. PLLTEST pin enable For Verify (Back door clock PLLTEST enable). 0：Output clock is gated off. 1：Clock Output. The clock is the clock output to the PLL and the clock after frequency division through PLLTEST pin.
2:1	/	/	/
0	R/W	0x1	LDO_EN. PLL Power Enable

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Offset: 0x0144			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
			(The power source is VCC_PLL) 0: Disable 1: Enable

2.2.7 TIMESTAMP_STA Register Description

2.2.7.1 0x0000 Current value of Counter [31:0] Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CNTCVLREAD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNTCVL32 The lower 32 bits of the current timestamp counter value.

2.2.7.2 0x0004 Current value of Counter [63:32] Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CNTCVUREAD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNTCVU32 The upper 32 bits of the current timestamp counter value.

2.2.7.3 0x0FD0 Peripheral Identification Register 4 Register (Default Value:0x0000_0004)

Offset: 0x0FD0			Register Name: PIDR4
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	SIZE Indicates the memory size that is used by this component. Returns 0 indicating that the component uses an UNKNOWN number of 4KB blocks. Using the SIZE field to indicate the size of the component is deprecated.
3:0	R	0x4	DES_2 JEP106 continuation code. Together, with PIDR2.DES_1 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

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2.2.7.4 0x0FD4 Peripheral Identification Register 5 Register (Default Value:0x0000_0000)

Offset: 0x0FD4			Register Name: PIDR5
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR5 Reserved

2.2.7.5 0x0FD8 Peripheral Identification Register 6 Register (Default Value:0x0000_0000)

Offset: 0x0FD8			Register Name: PIDR6
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR6 Reserved

2.2.7.6 0x0FDC Peripheral Identification Register 7 Register (Default Value:0x0000_0000)

Offset: 0x0FDC			Register Name: PIDR7
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR7 Reserved

2.2.7.7 0x0FE0 Peripheral Identification Register 0 Register (Default Value:0x0000_0093)

Offset: 0x0FE0			Register Name: PIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x93	PART_0 Part number, bits [7:0]. Taken together with PIDR1.PART_1 it indicates the component. The Part Number is selected by the designer of the component.

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2.2.7.8 0x0FE4 Peripheral Identification Register 1 Register (Default Value:0x0000_00B1)

Offset: 0x0FE4			Register Name: PIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xB	DES_0 JEP106 identification code, bits [3:0]. Together, with PIDR4.DES_2 and PIDR2.DES_1, they indicate the designer of the component and not the implementer, except where the two are the same.
3:0	R	0x1	PART_1 Part number, bits [11:8]. Taken together with PIDR0.PART_0 it indicates the component. The Part Number is selected by the designer of the component.

2.2.7.9 0x0FE8 Peripheral Identification Register 2 Register (Default Value:0x0000_000B)

Offset: 0x0FE8			Register Name: PIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVISION Revision. It is an incremental value starting at 0x0 for the first design of a component. See the css600 Component list in Chapter 1 for information on the RTL revision of the component.
3	R	0x1	JEDEC 1 - Always set. Indicates that a JEDEC assigned value is used.
2:0	R	0x3	DES_1 JEP106 identification code, bits [6:4]. Together, with PIDR4.DES_2 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

2.2.7.10 0x0FEC Peripheral Identification Register 3 Register (Default Value:0x0000_0000)

Offset: 0x0FEC			Register Name: PIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0

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Offset: 0x0FEC			Register Name: PIDR3
Bit	Read/Write	Default/Hex	Description
			Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVAND This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is 0x0.
3:0	R	0x0	CMOD Customer Modified. Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is 0x0.

2.2.7.11 0x0FF0 Component Identification Register 0 Register (Default Value:0x0000_000D)

Offset: 0x0FF0			Register Name: CIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0D	PRMBL_0 Preamble. Returns 0x0D.

2.2.7.12 0x0FF4 Component Identification Register 1 Register (Default Value:0x0000_00F0)

Offset: 0x0FF4			Register Name: CIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xF	CLASS Component class. Returns 0xF, indicating CoreLink, PrimeCell, or system component.
3:0	R	0x0	PRMBL_1 Preamble. Returns 0x0.

2.2.7.13 0x0FF8 Component Identification Register 2 Register (Default Value:0x0000_0005)

Offset: 0x0FF8			Register Name: CIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0

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Offset: 0x0FF8			Register Name: CIDR2
Bit	Read/Write	Default/Hex	Description
			Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x05	PRMBL_2 Preamble. Returns 0x05.

2.2.7.14 0x0FFC Component Identification Register 3 Register (Default Value:0x0000_00B1)

Offset: 0x0FFC			Register Name: CIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0xB1	PRMBL_3 Preamble. Returns 0xB1.

2.2.8 TIMESTAMP_CTRL Register Description

2.2.8.1 0x0000 Counter Control Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CNTCR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	HDBG Halt On Debug 0 Do not halt on debug. The HALT_REQ signal into the counter has no effect. 1 Halt on debug. When the HALT_REQ pulse is received, the count value is held static.
0	R/W	0x0	EN Enable Bit 0 The counter is disabled. Count is not incrementing. 1 The counter is enabled. Count is incrementing.

2.2.8.2 0x0004 Counter Status Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CNTSR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x0	DBGH

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Offset: 0x0004			Register Name: CNTSR
Bit	Read/Write	Default/Hex	Description
			Debug status. 0 Debug is halted 1 Debug is not halted.
0	/	/	/

2.2.8.3 0x0008 Current value of Counter [31:0] Register (Default Value:0x0000_0000)

Offset: 0x0008			Register Name: CNTCVL
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNTCVL32 Reads to this register return the lower 32 bits of the current timestamp counter value. To change the current timestamp value, write the lower 32 bits of the new value to this register before writing the upper 32 bits to CNTCVU. The timestamp value is not changed until the CNTCVU register is written to.

2.2.8.4 0x000C Current value of Counter [63:32] Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CNTCVU
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CNTCVU32 Reads to this register return the upper 32 bits of the current timestamp counter value. To change the current timestamp value, write the lower 32 bits of the new value to CNTCVL before writing the upper 32 bits to this register. The 64-bit timestamp value is updated with the value from both writes when this register is written to.

2.2.8.5 0x0020 Base Frequency ID Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name:CNTFID0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	Freq Frequency in number of ticks per second. Up to 4GHz can be specified.

2.2.8.6 0x0EF8 Integration Test Status Register (Default Value:0x0000_0000)

Offset: 0x0EF8	Register Name: ITSTAT

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Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x0	ITTRESTARTREQ Integration Test Restart Request status of the RESTART_REQ input. Integration testing mode:Behaves as a sticky bit and latches to 1 when TSGEN receives restart request. Cleared onreading this register. If RESTART_REQ is asserted in the same cycle as an APB read of this register, the read takes priority and the register is cleared as a result. Always returns 0 in normal functional mode.
0	R	0x0	ITHALTREQ Integration Test Halt Request status of the HALT_REQ input. Integration testing mode: Behaves as a sticky bit and latches to 1 when TSGEN receives halt request. Cleared on reading this register. If HALT_REQ is asserted in the same cycle as an APB read of this register, the read takes priority and the register is cleared as a result. Always returns 0 in normal functional mode.

2.2.8.7 0x0F00 Integration Mode Control Register (Default Value:0x0000_0000)

Offset: 0x0F00			Register Name: ITCTRL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	IME Integration Mode Enable. When set, the component enters integration mode, enabling topology detection or integration testing to be performed.

2.2.8.8 0x0FD0 Peripheral Identification Register 4 Register (Default Value:0x0000_0004)

Offset: 0x0FD0			Register Name:PIDR4
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	SIZE Indicates the memory size that is used by this component. Returns 0 indicating that the component uses an UNKNOWN number of 4KB blocks. Using the SIZE field to indicate the size of the component is deprecated.
3:0	R	0x4	DES_2

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Offset: 0x0FD0			Register Name:PIDR4
Bit	Read/Write	Default/Hex	Description
			JEP106 continuation code. Together, with PIDR2.DES_1 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

2.2.8.9 0x0FD4 Peripheral Identification Register 5 Register (Default Value:0x0000_0000)

Offset: 0x0FD4			Register Name:PIDR5
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR5 Reserved

2.2.8.10 0x0FD8 Peripheral Identification Register 6 Register (Default Value:0x0000_0000)

Offset: 0x0FD8			Register Name:PIDR6
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR6 Reserved

2.2.8.11 0x0FDC Peripheral Identification Register 7 Register (Default Value:0x0000_0000)

Offset: 0x0FDC			Register Name:PIDR7
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0	PIDR7 Reserved

2.2.8.12 0x0FE0 Peripheral Identification Register 0 Register (Default Value:0x0000_0093)

Offset: 0x0FE0			Register Name:PIDR0
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0FE0			Register Name:PIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x93	PART_0 Part number, bits [7:0]. Taken together with PIDR1.PART_1 it indicates the component. The Part Number is selected by the designer of the component.

2.2.8.13 0x0FE4 Peripheral Identification Register 1 Register (Default Value:0x0000_00B1)

Offset: 0x0FE4			Register Name:PIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0xB	DES_0 JEP106 identification code, bits [3:0]. Together, with PIDR4.DES_2 and PIDR2.DES_1, they indicate the designer of the component and not the implementer, except where the two are the same.
3:0	R	0x1	PART_1 Part number, bits [11:8]. Taken together with PIDR0.PART_0 it indicates the component. The Part Number is selected by the designer of the component.

2.2.8.14 0x0FE8 Peripheral Identification Register 2 Register (Default Value:0x0000_000B)

Offset: 0x0FE8			Register Name:PIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVISION Revision. It is an incremental value starting at 0x0 for the first design of a component. For information on the RTL revision of the component, see the css600 Component list in chapter 1 of *coresight_soc600_technical_reference_manual_100806_0300_00_en.pdf*
3	R	0x1	JEDEC

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Offset: 0x0FE8			Register Name:PIDR2
Bit	Read/Write	Default/Hex	Description
			1: Always set. Indicates that a JEDEC assigned value is used.
2:0	R	0x3	DES_1 JEP106 identification code, bits [6:4]. Together, with PIDR4.DES_2 and PIDR1.DES_0, they indicate the designer of the component and not the implementer, except where the two are the same.

2.2.8.15 0x0FEC Peripheral Identification Register 3 Register (Default Value:0x0000_0000)

Offset: 0x0FEC			Register Name:PIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:4	R	0x0	REVAND This field indicates minor errata fixes specific to this design, for example metal fixes after implementation. In most cases this field is 0x0.
3:0	R	0x0	CMOD Customer Modified. Where the component is reusable IP, this value indicates if the customer has modified the behavior of the component. In most cases this field is 0x0.

2.2.8.16 0x0FF0 Component Identification Register 0 Register (Default Value:0x0000_000D)

Offset: 0x0FF0			Register Name:CIDR0
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x0D	PRMBL_0 Preamble. Returns 0x0D.

2.2.8.17 0x0FF4 Component Identification Register 1 Register (Default Value:0x0000_00F0)

Offset: 0x0FF4			Register Name:CIDR1
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved

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Offset: 0x0FF4			Register Name:CIDR1
Bit	Read/Write	Default/Hex	Description
			(SBZP) behavior.
7:4	R	0xF	CLASS Component class. Returns 0xF, indicating CoreLink, PrimeCell, or system component.
3:0	R	0x0	PRMBL_1 Preamble. Returns 0x0.

2.2.8.18 0x0FF8 Component Identification Register 2 Register (Default Value:0x0000_0005)

Offset: 0x0FF8			Register Name:CIDR2
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0x05	PRMBL_2 Preamble. Returns 0x05.

2.2.8.19 0x0FFC Component Identification Register 3 Register (Default Value:0x0000_00B1)

Offset: 0x0FFC			Register Name:CIDR3
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	RES0 Reserved bit or field with Should-Be-Zero-or-Preserved (SBZP) behavior.
7:0	R	0xB1	PRMBL_3 Preamble. Returns 0xB1.

2.2.9 CPU_PLL_CFG Register Description

2.2.9.1 0x0004 CPU_L_PLL Control Register (Default Value: 0x4880_1400)

Offset: 0x0004			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable The CPU_L_PLL= InputFreq*N/P/(M0*M1). Note: The CPU_L_PLL output frequency must be in the

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Offset: 0x0004			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			range from 480 MHz to 2.6 GHz. And the default value of CPU_L_PLL is 480 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO Enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock INFO. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26	R/WAC	0x0	PLL_UPDATE Write q update the CFG to PLL, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 3.
19:16	R/W	0x0	PLL_P PLL PREDIV P P = PLL_P + 1
15:8	R/W	0x14	PLL_N PLL N N= PLL_N
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles

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Offset: 0x0004			Register Name: CPU_L_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1 PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

2.2.9.2 0x0008 CPU_DSU_PLL Control Register (Default Value: 0x4880_1400)

Offset: 0x0008			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The CPU_DSU_PLL= InputFreq*N/P/(M0*M1). Note: The CPU_DSU_PLL output frequency must be in the range from 200 MHz to 3 GHz. And the default value of CPU_DSU_PLL is 408 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0: Disable 1: Enable The bit is used to control the output enable of the PLL.

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Offset: 0x0008			Register Name: CPU_DSU_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26	R/WAC	0x0	PLL_UPDATE Write q update the CFG to PLL, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 15.
19:16	R/W	0x0	PLL_P PLL PREDIV P P = PLL_P + 1
15:8	R/W	0x14	PLL_N PLL N N= PLL_N
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15.

2.2.9.3 0x000C CPU_B_PLL Control Register (Default Value: 0x4880_1400)

Offset: 0x000C			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The CPU_B_PLL= InputFreq*N/P/(M0*M1). Note: The CPU_B_PLL output frequency must be in the range from 480 MHz to 2.6 GHz. And the default value of CPU_B_PLL is 480 MHz when the crystal oscillator is 24

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Offset: 0x000C			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			MHz.
30	R/W	0x1	PLL_LDO_EN. LDO Enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock INFO 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26	R/WAC	0x0	PLL_UPDATE Write q update the CFG to PLL, auto clear.
25:24	/	/	/
23	R/W	0x1	PLL_NDET
22	R/W	0x0	PLL_TDIV
21:20	R/W	0x0	PLL_M0 M0 = PLL_M0 + 1 PLL_FACTOR_M0 is from 0 to 15.
19:16	R/W	0x0	PLL_P P = PLL_P + 1
15:8	R/W	0x14	PLL_N N= PLL_N
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level

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Offset: 0x000C			Register Name: CPU_B_PLL_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4	/	/	/
3:0	R/W	0x0	PLL_M1 M1 = PLL_M1 + 1 PLL_M1 is from 0 to 15

2.2.9.4 0x0010 CPU_L_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CPU_L_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular (1bit) 11: Triangular (n bit)
28:17	R/W	0x0	WAVE_STEP Wave Step
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.2.9.5 0x0014 CPU_L_PLL Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CPU_L_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	SDM_CYCLE SDM Cycle SDM_CYCLE=SDM_FRE/CLK_SDM/2
21	/	/	/
20	R/W	0x0	SDM_DIRECTION SDM direction 0: UP 1: DOWM
19	/	/	/
18	R/W	0x0	DITHER_EN Dither Enable
17	R/W	0x0	FRAC_EN

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Offset: 0x0014			Register Name: CPU_L_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			Fraction Enable
16:0	R/W	0x0	FRAC_IN Fraction In

2.2.9.6 0x0018 CPU_DSU_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CPU_DSU_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular (1bit) 11: Triangular (n bit)
28:17	R/W	0x0	WAVE_STEP Wave Step
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.2.9.7 0x001C CPU_DSU_PLL Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: CPU_DSU_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	SDM_CYCLE SDM Cycle SDM_CYCLE=SDM_FRE/CLK_SDM/2
21	/	/	/
20	R/W	0x0	SDM_DIRECTION. SDM direction. 0: UP 1: DOWM
19	/	/	/
18	R/W	0x0	DITHER_EN Dither Enable
17	R/W	0x0	FRAC_EN Fraction Enable
16:0	R/W	0x0	FRAC_IN Fraction In

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2.2.9.8 0x0020 CPU_B_PLL Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CPU_B_PLL_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular (1 bit) 11: Triangular (n bit)
28:17	R/W	0x0	WAVE_STEP Wave Step
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.2.9.9 0x0024 CPU_B_PLL Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CPU_B_PLL_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x0	SDM_CYCLE SDM Cycle SDM_CYCLE=SDM_FRE/CLK_SDM/2
21	/	/	/
20	R/W	0x0	SDM_DIRECTION SDM direction 0: UP 1: DOWM
19	/	/	/
18	R/W	0x0	DITHER_EN Dither Enable
17	R/W	0x0	FRAC_EN Fraction Enable
16:0	R/W	0x0	FRAC_IN Fraction In

2.2.9.10 0x002C CPU_L_PLL Bias Register (Default Value: 0x0010_0000)

Offset: 0x002C			Register Name: CPU_L_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

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Offset: 0x002C			Register Name: CPU_L_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
20:16	R/W	0x10	PLL_CP PLL Current Bias Control
15:0	/	/	/

2.2.9.11 0x0030 CPU_DSU_PLL Bias Register (Default Value: 0x0010_0000)

Offset: 0x0030			Register Name: CPU_DSU_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x10	PLL_CP PLL Current Bias Control
15:0	/	/	/

2.2.9.12 0x0034 CPU_B_PLL Bias Register (Default Value: 0x0010_0000)

Offset: 0x0034			Register Name: CPU_B_PLL_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x10	PLL_CP PLL Current Bias Control
15:0	/	/	/

2.2.9.13 0x003C CPU_L_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CPU_L_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR

2.2.9.14 0x0040 CPU_L_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x0040			Register Name: CPU_L_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN
30	R/W	0x0	PLL_FF_EN
29	R/W	0x0	PLL_SS_EN

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Offset: 0x0040			Register Name: CPU_L_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
28:20	R/W	0x0	PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC

2.2.9.15 0x0044 CPU_DSU_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CPU_DSU_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR

2.2.9.16 0x0048 CPU_DSU_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x0048			Register Name: CPU_DSU_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN
30	R/W	0x0	PLL_FF_EN.
29	R/W	0x0	PLL_SS_EN
28:20	R/W	0x0	PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC

2.2.9.17 0x004C CPU_B_PLL Tuning0 Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CPU_B_PLL_TUN0_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	PLL_LPF_SW
4:2	/	/	/
1:0	R/W	0x0	PLL_FF_SR

2.2.9.18 0x0050 CPU_B_PLL Tuning1 Register (Default Value: 0x0003_2800)

Offset: 0x0050			Register Name: CPU_B_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SDM_EN.

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Offset: 0x0050			Register Name: CPU_B_PLL_TUN1_REG
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	PLL_FF_EN
29	R/W	0x0	PLL_SS_EN
28:20	R/W	0x0	PLL_SS_FRAC
19:12	R/W	0x32	PLL_SS_INT
11:0	R/W	0x800	PLL_FRAC

2.2.9.19 0x0054 CPU_L_PLL SSC Register (Default Value: 0x4CCC_A000)

Offset: 0x0054			Register Name: CPU_L_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SSC_MODE 0: Normal Mode 1:Continuously Frequency Scale
30	R/W	0x1	PLL_SSC_RSTN SSC RSTN Bake Up
29	R/W	0x0	PLL_SSC_CLK_SEL SSC CLK Selection 0: REF_CLK 1: PLL_CLK_SDM
28:12	R/W	0xCCCA	PLL_SSC SSC amplitude must be an integer multiple of 2^step. spread spectrum amplitude = (SSC amplitude + 2^step) *24/(2^17), unit: MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_PHASE_COMPENSATE The value of bit[6:4] is based on 24M clock, then the default PLL phase compensate is (3/24000000)s.
3:0	R/W	0x0	PLL_SSC_STEP 0000:0.00439MHz/us (576/2^17) 0001:0.00879MHz/us (576/2^16) 0010:0.01758MHz/us (576/2^15) 0011:0.03516MHz/us (576/2^14) 0100:0.07031MHz/us (576/2^13) 0101:0.14062MHz/us (576/2^12) 0110:0.28125MHz/us (576/2^11) 0111:0.56250MHz/us (576/2^10) 1000:1.12500MHz/us (576/2^9) 1001:2.25000MHz/us (576/2^8) 1010:4.50000MHz/us (576/2^7) 1011:9.00000MHz/us (576/2^6)

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Offset: 0x0054			Register Name: CPU_L_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
			Others:0.00439MHz/us (576/2^17)

2.2.9.20 0x0058 CPU_DSU_PLL SSC Register (Default Value: 0x4CCC_A000)

Offset: 0x0058			Register Name: CPU_DSU_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SSC_MODE 0: Normal Mode 1:Continuously Frequency Scale
30	R/W	0x1	PLL_SSC_RSTN SSC RSTN Bake Up
29	R/W	0x0	PLL_SSC_CLK_SEL SSC CLK Selection 0: REF_CLK 1: PLL_CLK_SDM
28:12	R/W	0xCCCA	PLL_SSC SSC amplitude must be an integer multiple of 2^step. spread spectrum amplitude = (SSC amplitude + 2^step) *24/(2^17), unit: MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_PHASE_COMPENSATE The value of bit[6:4] is based on 24M clock, then the default PLL phase compensate is (3/24000000)s.
3:0	R/W	0x0	PLL_SSC_STEP 0000:0.00439MHz/us (576/2^17) 0001:0.00879MHz/us (576/2^16) 0010:0.01758MHz/us (576/2^15) 0011:0.03516MHz/us (576/2^14) 0100:0.07031MHz/us (576/2^13) 0101:0.14062MHz/us (576/2^12) 0110:0.28125MHz/us (576/2^11) 0111:0.56250MHz/us (576/2^10) 1000:1.12500MHz/us (576/2^9) 1001:2.25000MHz/us (576/2^8) 1010:4.50000MHz/us (576/2^7) 1011:9.00000MHz/us (576/2^6) Others:0.00439MHz/us (576/2^17)

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2.2.9.21 0x005C CPU_B_PLL SSC Register (Default Value: 0x4CCC_A000)

Offset: 0x005C			Register Name: CPU_B_PLL_SSC_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_SSC_MODE 0: Normal Mode 1:Continuously Frequency Scale
30	R/W	0x1	PLL_SSC_RSTN SSC RSTN Bake Up
29	R/W	0x0	PLL_SSC_CLK_SEL SSC CLK Selection 0: REF_CLK 1: PLL_CLK_SDM
28:12	R/W	0xCCCA	PLL_SSC SSC amplitude must be an integer multiple of 2^step. spread spectrum amplitude = (SSC amplitude + 2^step) *24/(2^17), unit: MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_PHASE_COMPENSATE The value of bit[6:4] is based on 24M clock, then the default PLL phase compensate is (3/24000000)s.
3:0	R/W	0x0	PLL_SSC_STEP 0000:0.00439MHz/us (576/2^17) 0001:0.00879MHz/us (576/2^16) 0010:0.01758MHz/us (576/2^15) 0011:0.03516MHz/us (576/2^14) 0100:0.07031MHz/us (576/2^13) 0101:0.14062MHz/us (576/2^12) 0110:0.28125MHz/us (576/2^11) 0111:0.56250MHz/us (576/2^10) 1000:1.12500MHz/us (576/2^9) 1001:2.25000MHz/us (576/2^8) 1010:4.50000MHz/us (576/2^7) 1011:9.00000MHz/us (576/2^6) Others:0.00439MHz/us (576/2^17)

2.2.9.22 0x0060 CPUA Clock Register (Default Value: 0x0000_0305)

Offset: 0x0060			Register Name: CPUA_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

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Offset: 0x0060			Register Name: CPUA_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CPUA_CLK_SEL Clock Source Selection 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPU1PLL/P 100: PERI0_600M 101: CPU0PLL CPUA_CLK = Clock Source The clock MUX supports glitch-free switch and dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	CPU_L_PLL_OUT_EXT_DIVP Factor P 00: 1 01: 2 10: 4 11: \ When the output clock is less than 288 MHz, it can divide P to get the required clock frequency.
15:10	/	/	/
9:8	R/W	0x3	CPU_APB_DIV_CFG. Factor N. (N = FACTOR_N +1) FACTOR_N is 1 or 3. The clock division is no-burr switch, and supports dynamic configuration.
7:4	/	/	/
3:2	R/W	0x1	CPU_PERI_DIV_CFG. Factor M1:(M= FACTOR_M1 +1) FACTOR_M1 is 0, 1, or 3. The clock division is no-burr switch, and supports dynamic configuration.
1:0	R/W	0x1	CPU_AXI_DIV_CFG. Factor M:(M= FACTOR_M +1) FACTOR_M is from 1 to 3 The clock division is no-burr switch, and supports dynamic configuration.

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2.2.9.23 0x0064 CPUB Clock Register (Default Value: 0x0000_0305)

Offset: 0x0064			Register Name: CPUB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CPUB_CLK_SEL. Clock Source Selection. 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPU3PLL/P 100: PERI0_600M 101: CPU0PLL CPU_CLK = Clock Source. The clock MUX supports glitch-free switch and dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	CPU_B_PLL_OUT_EXT_DIVP. Factor P 00: 1 01: 2 10: 4 11: \ When the output clock is less than 288 MHz, it can divide P to get the required clock frequency.
15:0	/	/	/

2.2.9.24 0x0068 CPU Gating Configuration Register (Default Value: 0x0000_0007)

Offset: 0x0068			Register Name: CPU_GATING_REG:
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD CPU Gating Field If CPU_GATING_FIELD==16’h16AA，the bit [15:0] can be configured.
15:4	/	/	/
3	R/W	0x0	DSU_PPU_SW_GATE_EN DSU PPU Control Enable 0: Disable 1: Enable
2	R/W	0x1	DSU_CLK_GATING Gating Clock

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Offset: 0x0068			Register Name: CPU_GATING_REG:
Bit	Read/Write	Default/Hex	Description
			0: Clock is OFF 1: Clock is ON
1	R/W	0x1	CPUB_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON
0	R/W	0x1	CPUA_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON

2.2.9.25 0x006C DSU Clock Register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: DSU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	DSU_CLK_SEL Clock Source Selection 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPU2PLL/P 100: PERI0PLL2X 101: PERI0_600M DSU_CLK = Clock Source. CPU_AXI Clock = DSU_CLK/M. CPU_APB Clock= DSU_CLK/N. CPU_GIC Clock=DSU_CLK/M1. The clock MUX supports glitch-free switch and dynamic configuration.
23:18	/	/	/
17:16	R/W	0x0	CPU_DSU_PLL_OUT_EXT_DIVP Factor P 00: 1 01: 2 10: 4 11: \ When the output clock is less than 288 MHz, it can divide P to get the required clock frequency.
15:0	/	/	/

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2.2.9.26 0x0070 PLL Test Clock Selection Register (Default Value: 0x0000_0300)

Offset: 0x0070			Register Name: PLL_TEST_CLK_SEL
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
9:8	R/W	0x3	PLL_CFG_CLK_DIV PLL Config Clock Div
7:1	/	/	/
0	R/W	0x0	CLK_SEL Clock Selection 0: COREPLLA 1: DSU_CLK

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2.3 RISC-V System (RISCV)

2.3.1 Overview

The RISC-V system includes RISC IP core and related peripheral devices (AHB_Decoder, AHB2APB, RISCV_CFG, RISC_TIMESTAMP, and so on), which is able to be interconnected to MCU system by MCU AHB Matrix.

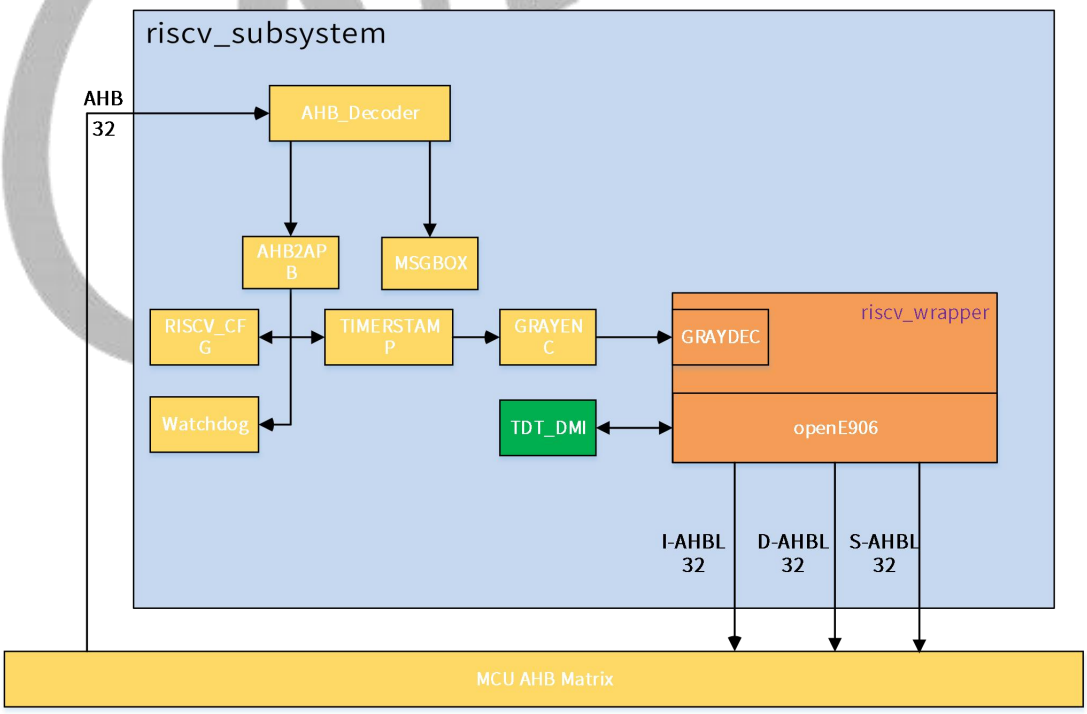
The RISC-V system has the following features:

- Configurable start address via software
- Combined with PPU module, supporting standby in low-power mode and wake-up through external interrupts
- Separate TIMERSTAMP supports timing immediately after reset is released
- Separate watchdog supports to reset the SoC system when the RISC-V system malfunctions
- Separate message box supports communicating with other modules
- Supports separate PMU check module

2.3.2 Block Diagram

The following figure shows the block diagram of RISC-V system.

Figure 2-2 RISC-V System Block Diagram



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2.3.3 Register List

Module Name	Base Address
RISCV_CFG	0x0713_0000

Register Name	Offset	Description
RF1P_CFG_REG	0x0010	RF1P Configuration Register
TS_TMODE_SEL_REG	0x0040	Timestamp Test Mode Selection Register
RISCV_STA_ADD_REG	0x0204	RISC-V Start Address Register
RISCV_WAKEUP_EN_REG	0x0220	RISC-V Wakeup Enable Register
RISCV_WAKEUP_MASK0_REG	0x0224	RISC-V Wakeup Mask0 Register
RISCV_WAKEUP_MASK1_REG	0x0228	RISC-V Wakeup Mask1 Register
RISCV_WAKEUP_MASK2_REG	0x022C	RISC-V Wakeup Mask2 Register
RISCV_WAKEUP_MASK3_REG	0x0230	RISC-V Wakeup Mask3 Register
RISCV_WORK_MODE_REG	0x0248	RISC-V Work Mode Register

2.3.4 Register Description

2.3.4.1 0x0010 RF1P Configuration Register (Default Value: 0x0000_0400)

Offset: 0x0010			Register Name: RF1P_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x400	RF1P_CFG RF1P Configuration

2.3.4.2 0x0040 Timestamp Test Mode Selection Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TS_TMODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	RISCV_TS_TEST_MODE_EN RISCV Timestamp Test Mode Enable 0: Normal Mode 1: Test Mode In Test Mode, this Counter Low/Hi registers will count simultaneously.
0	/	/	/

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2.3.4.3 0x0204 RISCV Start Address Register (Default Value: 0x3FFC_0000)

this register is the running PC address after RISCV releases reset. Before releasing reset, this register should be configured. This register does support dynamic configuration.

Offset: 0x0204			Register Name: RISCV_STA_ADD0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x3FFC0000	STA_ADD Start Address The bit 0 is fixed as 0 and could not be written.

2.3.4.4 0x0220 RISCV Wakeup Enable Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: RISCV_WAKEUP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WP_EN Wakeup Enable To wake up the enable bit of RISC-V, when RISC-V is in low power mode.

2.3.4.5 0x0224 RISCV Wakeup Mask0 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0230 registers corresponds to the wakeup enable bits of 128 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1. For detailed interrupt sources, please refer to section 2.8 Core-Local Interrupt Controller (CLIC)

Offset: 0x0224			Register Name: RISCV_WAKEUP_MASK0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK0 Wakeup Mask0

2.3.4.6 0x0228 RISCV Wakeup Mask1 Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: RISCV_WAKEUP_MASK1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK1 Wakeup Mask1

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2.3.4.7 0x022C RISCV Wakeup Mask2 Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: RISCV_WAKEUP_MASK2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK2 Wakeup Mask2

2.3.4.8 0x00230 RISCV Wakeup Mask3 Register (Default Value: 0x0000_0000)

Offset: 0x00230			Register Name: RISCV_WAKEUP_MASK3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK3 Wakeup Mask3

2.3.4.9 0x0248 RISCV Work Mode Register (Default Value: 0x0000_0003)

Offset: 0x0248			Register Name: RISCV_WORK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	LOCKUP_STA Lockup Status 0: Not Lockup 1: Lockup If CPU has a lockup, CPU will stop accessing data and fetching, and clear the pipeline. Reset processor unit and debug unit to unlock.
2	R	0x0	DM_STA Debug Mode Status 0: Normal Mode 1: Debug Mode
1:0	R	0x3	LP_STA Low Power Status 00: Deep Sleep Low Power Mode 01: Light Sleep Low Power Mode 10: Reserved 11: Normal Mode

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2.4 BROM System

2.4.1 Overview

The system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) that is considered the primary program-loader. On the startup process, the A523 starts to fetch the first instruction from address 0x0, where is the BROM located at.

The BROM system is divided into two parts: the firmware exchange launch (FEL) module and the Medium Boot module. FEL is responsible for writing the external data to the local NVM, and Medium Boot is responsible for loading an effective and legitimate BOOT0 from NVM and running.

The BROM system includes the following features:

- Supports CPU0 boot process
- Supports mandatory upgrade process through USB and SD card
- Supports GPADC0 pin and eFuse module to select the boot media type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Ensures that the secure boot is in a trusted environment

2.4.2 Functional Description

2.4.2.1 Selecting the Boot Medium

The BROM system supports the following boot media:

- SD Card
- eMMC
- RAW NAND Flash
- SPI NOR Flash (Quad Mode and Single Mode)
- SPI NAND Flash

There are two ways to select the boot medium: GPADC Pin Select and eFuse Select. The BROM will read the state of BOOT_MODE first, and then select the boot medium according to the state of BOOT_MODE. The BOOT_MODE is the BROM_Config in the eFuse mapping.

The following table shows the BOOT_MODE setting:

Table 2-5 BOOT_MODE Setting

BOOT_MODE[0]	Boot Select type
0	GPADC Selection
1	eFuse Selection

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NOTE

The BOOT_MODE BIT is bit [0] of the eFuse register 0x03006210.

GPADC Boot Selection

If the state of the BOOT_MODE is 0, choose the GPADC Boot Selection.

If BROM failed to boot from the selected medium, it will try other media with the following priority:

EMMC_USR -> EMMC_BOOT -> SLC_NAND -> MLC_NAND -> SPI_NOR -> SPI_NAND

And the medium selected by GPADC will be skipped.

For example, when BROM failed to boot from SPI NOR, it will try other media with the following priority:

SPI NOR (selected by GPADC) -> EMMC_USR -> EMMC_BOOT -> SLC_NAND -> MLC_NAND -> SPI_NOR (try at first, skipped) -> SPI_NAND

The following table shows GPADC Boot Select setting.

Table 2-6 GPADC Boot Select Setting

KEY_VALUE	Boot Select type
0x00-0xB6	SD Card->MLC NAND->SLC NAND->try (except SPI in PJ)
0xB7-0x22B	SD Card->SLC NAND->MLC NAND->try (except SPI in PJ)
0x22C-0x3AF	SD Card->EMMC_USER->EMMC_BOOT->try (except SPI in PJ)
0x3B0-0x57B	SD Card->EMMC_BOOT->EMMC_USER->try (except SPI in PJ)
0x57C-0x73C	SD Card->SPI NOR->try (except SPI in PJ)
0x73D-0x8CC	SD Card->SPI NAND->try (except SPI in PJ)
0x8CD-0xB49	SD Card->SPI NOR in PJ->try
0xB4A-0xE7C	SD Card->SPI NAND in PJ->try
0x8CD-0xFFF	Reserved

NOTE

When trying SPI NOR, BROM try 4 wire mode first, then 1 wire mode.

eFuse Boot Selection

If the state of the BOOT_MODE is 1, choose the eFuse Boot Selection.

The eFuse_Boot_Select_Cfg is divided into 3 groups and each group is 3-bit. The following table shows the groups of eFuse_Boot_Select.

Table 2-7 Groups of eFuse_Boot_Select

eFuse_Boot_Select_Cfg [11:0]	Description

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eFuse_Boot_Select_Cfg [11:0]	Description
eFuse_Boot_Select[3:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[7:4]	eFuse_Boot_Select_2
eFuse_Boot_Select[11:8]	eFuse_Boot_Select_3

These three groups take effect with the following priority:

eFuse_Boot_Select_1 -> eFuse_Boot_Select_2 -> eFuse_Boot_Select_3

For example, eFuse_Boot_Select_2 will not take effect unless eFuse_Boot_Select_1 is set as 0b1111(skip), eFuse_Boot_Select_3 will not take effect unless eFuse_Boot_Select_2 is set as 0b1111(skip), etc. If all three groups are set to 0b1111, no other groups can be used for boot select, BROM assume "try" is selected.

In the Try mode, the BROM follows the order below to select the boot medium:

SD Card -> eMMC -> NAND FLASH -> SPI NOR -> SPI NAND

The following table shows the boot medium priority for the different values of eFuse_Boot_Select_n, where n = [4:1].

Table 2-8 eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot media
0000	Try (except SPI in PJ)
0001	SLC NAND -> MLC NAND
0010	EMMC_USER -> EMMC_BOOT
0011	SPI NOR
0100	SPI NAND
0101	MLC NAND -> SLC NAND
0110	MMC_BOOT -> EMMC_USER
1011	SPI NOR in PJ
1100	SPI NAND in PJ
1111	When n is 1 or 2: The boot medium is decided by the value of **eFuse_Boot_Select_ (n + 1)**. When n is 4: Select the boot medium in Try mode.

NOTE

The status of the eFuse boot select pin is the bit [11:0] of the eFuse register 0x03006212.

2.4.2.2 Selecting the Boot Mode

For SoCs that have implemented and enabled the ARM TrustZone technology, there are two boot modes: Normal BROM Mode and Secure BROM Mode.

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Secure BROM Mode is designed to protect against attackers modifying the code or data areas in the programmable memory.

During the startup process, the BROM will select the boot mode according to the value of the Secure Enable bit. If the value of Secure Enable bit is 0, the system will boot in Normal BROM Mode. Otherwise, it will boot in Secure BROM Mode.

NOTE

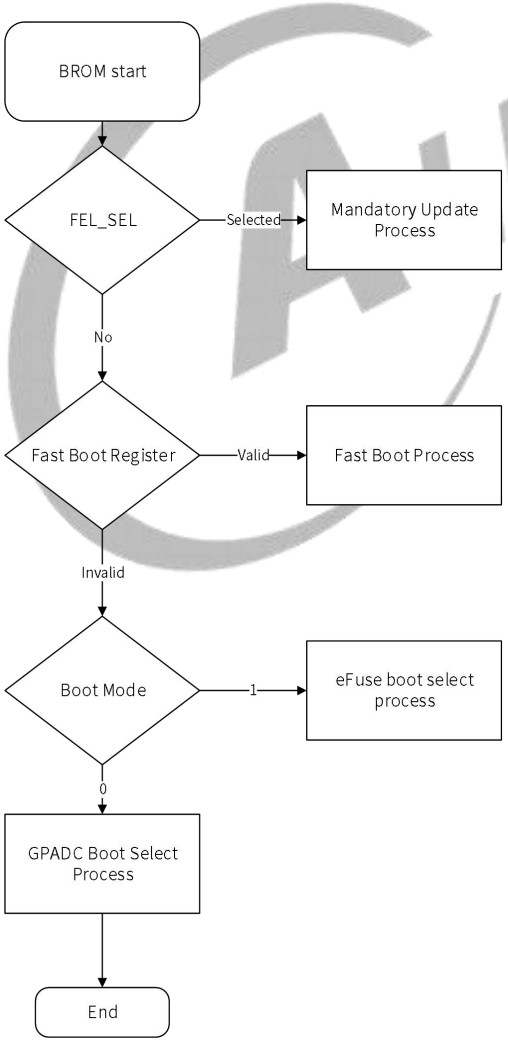
The System on Chip (SoC) supports the ARM TrustZone technology. If the Secure Enable Bit is enabled, the BROM will be safely booted based on this ARM TrustZone technology.

Normal BROM Mode

In Normal BROM Mode, the system boot starts from CPU0, and then the BROM will read the state of the FEL pin. If the FEL pin is high, the system will jump to the fast boot process. If it is low, the system will jump to the mandatory upgrade process.

The following figure shows the boot process in Normal BROM Mode.

Figure 2-3 Boot Process in Normal BROM Mode



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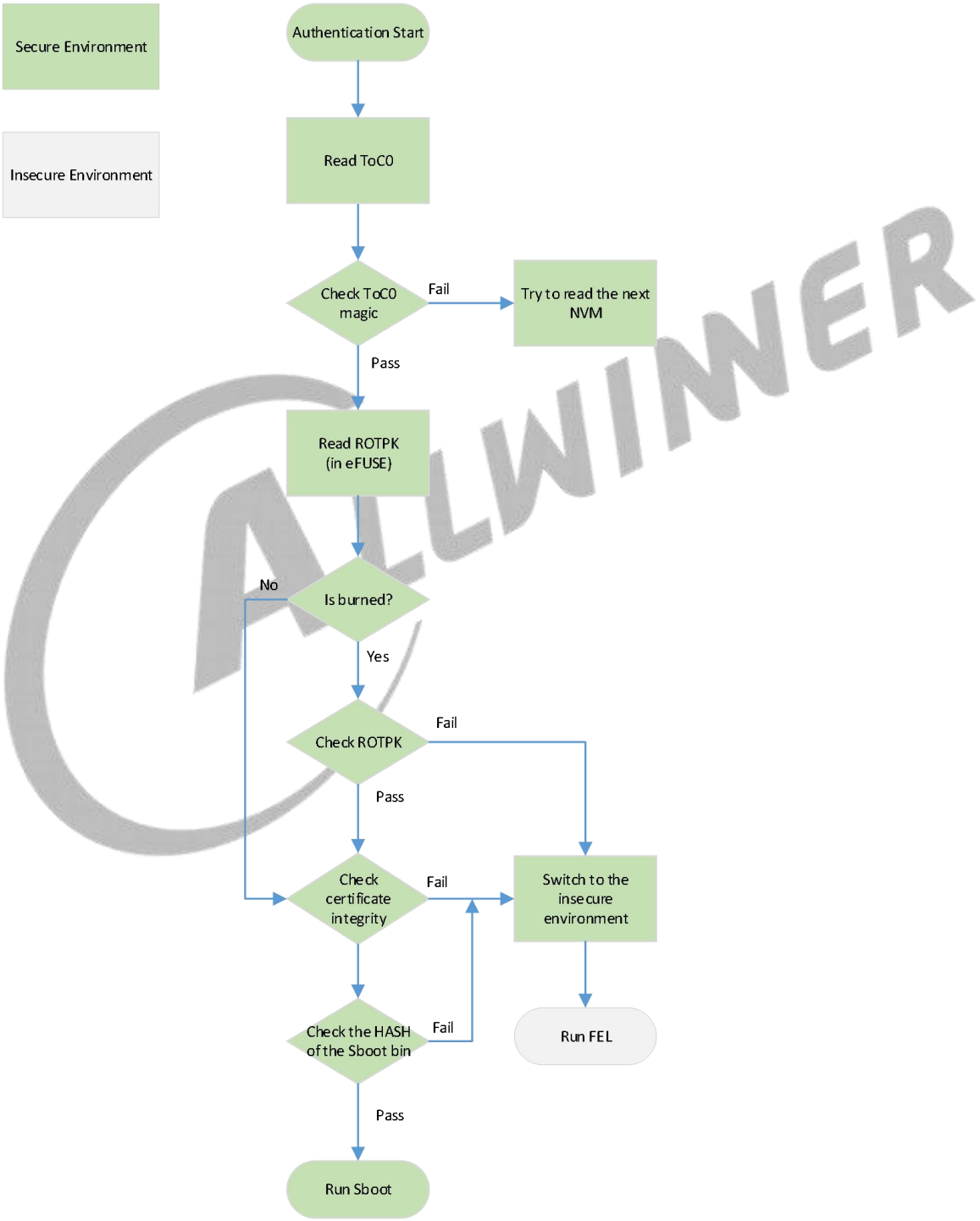
Secure BROM Mode

The process of selecting the boot medium in Secure Boot Mode is the same as that in Normal Boot Mode.

In Secure Boot Mode, after the boot medium is selected, the system additionally runs the Security Boot software to authenticate the Sboot bin file.

The following figure shows the authentication process.

Figure 2-4 Authentication Process in Secure BROM Mode



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Secure BROM Requirements

The Secure Boot has the following some requirement:

- Supports X509 certificate

  The certificate is used to check whether the Security Boot software is modified or replaced. Before running the Security Boot software, the system checks the integrity of the certificate make sure the software has not been modified or replaced.

- Supports cryptographic algorithms
  - AES-128
  - SHA-256
  - RSA-2048
  - AES, DES

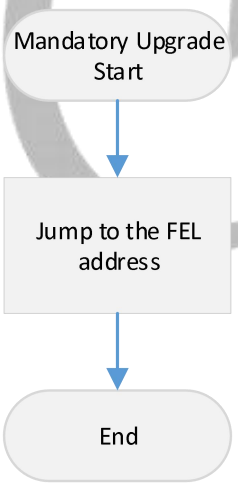
  The system uses the Crypto Engine (CE) hardware module to accelerate the speed of encryption and decryption. The standard cryptography ensures the reliability of the firmware images. The reliable firmware image ensures that the system security state can be as expected.

- Support OTP/eFuse

2.4.2.3 Mandatory Upgrade Process

If the FEL pin is detected to pull low, the system will jump to the mandatory upgrade process. The following figure shows the mandatory upgrade process.

Figure 2-5 Mandatory Upgrade Process



NOTE

The FEL address of the Normal BROM is 0x20.

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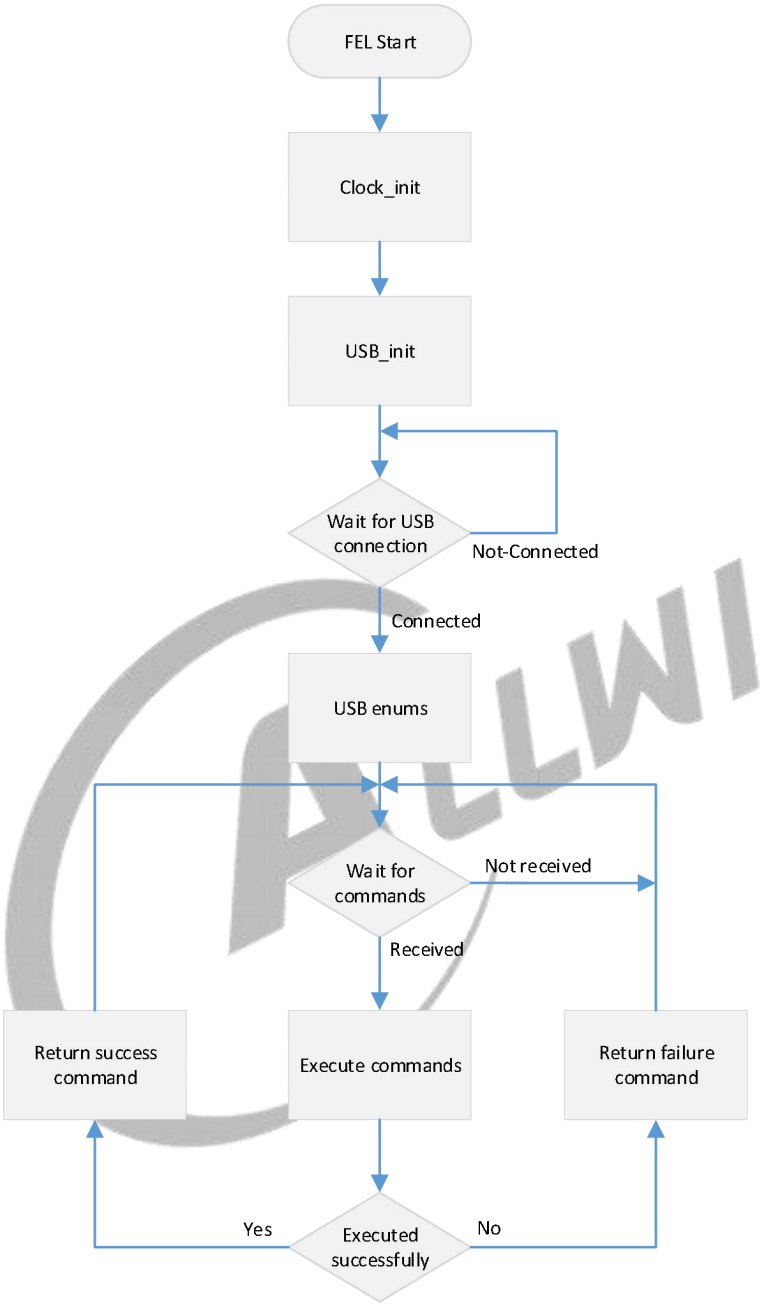
FEL Process

When the system enters mandatory upgrade process, it will jump to the FEL process.

The following figure shows the FEL upgrade process.

Figure 2-6 USB FEL Process



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2.4.2.4 Fast Boot Process

If the value of the Fast Boot register (0x07090120) in RTC module is not zero, the system will enter the fast boot process. The following table shows the boot medium priority for different values of the Fast Boot register.

Table 2-9 Fast Boot Select Setting

Reg_bit[31:28]	Boot Select type
1	SD Card->MLC NAND -> SLC NAND -> TRY
2	SD Card->EMMC_USER -> EMMC_BOOT -> TRY
3	SD Card->SPI NOR(1 wire)-> SPI NOR(4 wire)-> TRY
4	SD Card->SPI NAND -> TRY
5	SD Card->EMMC_BOOT -> EMMC_USER -> TRY
6	SD Card->SLC NAND -> MLC NAND -> TRY
7	Reserved
8	SD Card->SPI NOR(4 wire)-> SPI NOR(1 wire)-> TRY
10	SD Card->SPI NOR(4 wire) in PJ -> TRY
11	SD Card->SPI NAND in PJ-> TRY

NOTE

- The Fast Boot register bit [27:0] is used record the media information.
- Unused value like 7 regarded as “TRY”.

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2.5 Clock Controller Unit (CCU)

2.5.1 Overview

The clock controller unit (CCU) controls the PLL configurations and most of the clock generation, division, distribution, synchronization, and gating. The input signals of the CCU include the external clock for the reference frequency (24 MHz). The outputs from the CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 10 PLLs
- Bus source and divisions
- Clock output control
- Configuring modules clock
- Bus clock gating
- Bus software reset

NOTE

- There are 15 PLLs in A523. 10 PLLs in CCU, 4 PLLs in CPUX system, and 1 PLL in MCU_PRCM.
- CCU describes module clocks in CPUX domain excluding the clock of CPUX system.
- For clock description of CPUX system, please refer to section 2.2.3.2 CPU PLL Distribution and Clock Sources.
- For module clocks in CPUS domain, please refer to section 2.11 Power Reset Clock Management (PRCM).

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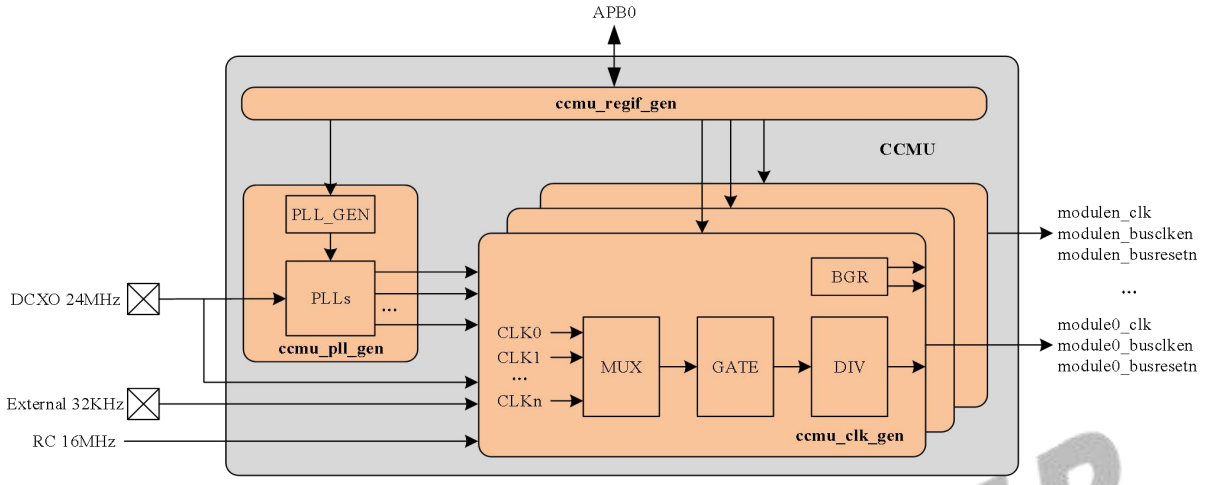
2.5.2 Block Diagram

The following figure shows the functional block diagram of the CCU.

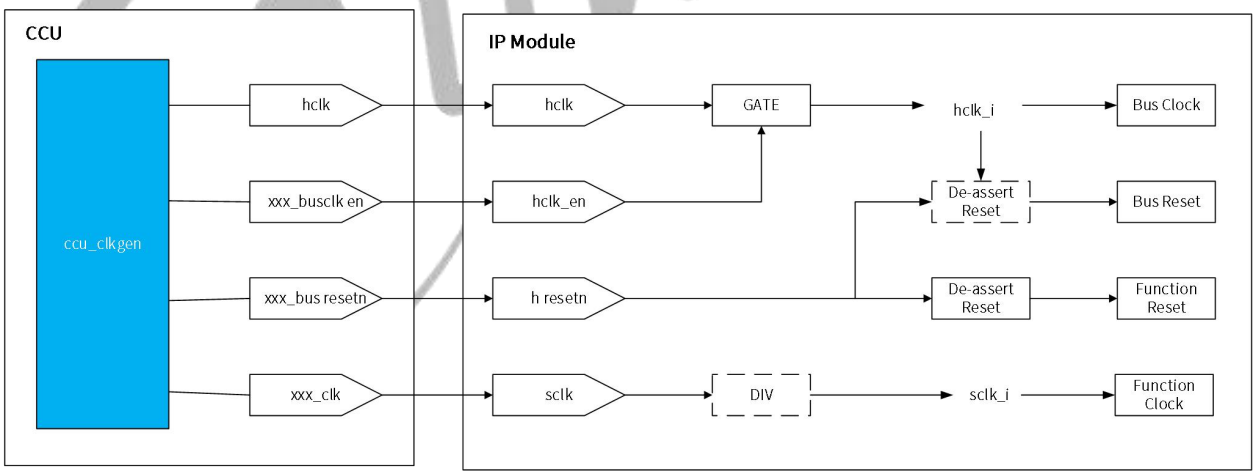
Figure 2-7 CCU Block Diagram



2.5.3 Functional Description

2.5.3.1 Typical Application

Figure 2-8 CCU Typical Application Diagram



CCU outputs bus clock, bus reset, function clock, and function reset to each IP module.

It is needed to enable the bus clock gating signal before using the bus clock. For some subsystems, CCU outputs special bus clock which has been added clock gating. When using the special bus clock, you also need to enable the bus clock gating signal.

The IP reset is from the synchronous release of the input reset signal. To ensure the implement of synchronous release in every module, you need to release the reset signal before enbling the clock gating signal of the function clock.

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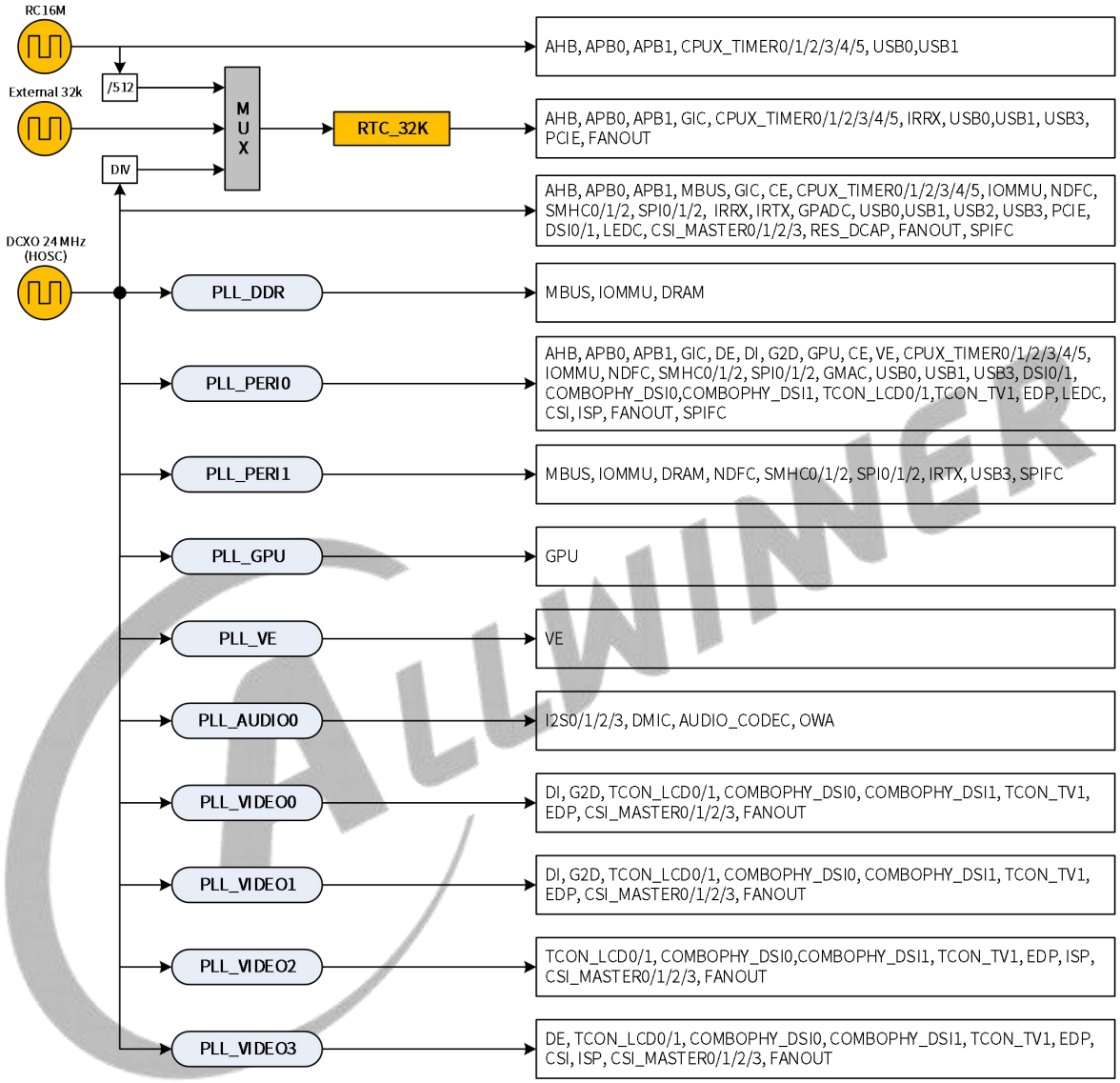
2.5.3.2 PLL Distribution

The following figure shows the block diagram of the PLL distribution.

Figure 2-9 PLL Distribution



2.5.3.3 PLL Features

The following table shows the PLL features.

Table 2-10 PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Pk-Pk	Lock Time
PLL_DDR	1.26 GHz～2.52 GHz	< 2.5 GHz	Yes	No	< 200ps	500us

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PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Pk-Pk	Lock Time
PLL_GPU	1.26 GHz～2.52 GHz	< 1.5 GHz	Yes	No	< 200ps	500us
PLL_PERI0	1.26 GHz～2.52 GHz	2x：1.2 GHz 3x：800 MHz 5x：480 MHz	Yes	No	< 200ps	500us
PLL_PERI1	1.26 GHz～2.52 GHz	2x：1.248 GHz/1.2 GHz 3x：832 MHz/800 MHz 5x：499.2 MHz/480 MHz	Yes	No	< 200ps	500us
PLL_VE	1.26 GHz～2.52 GHz	< 1.5 GHz	Yes	No	< 200ps	500us
PLL_AUDIO0	1.26 GHz～2.52 GHz	1x：22.5792 MHz 4x：22.5792*4 MHz	Yes	No	< 200ps	500us
PLL_VIDEO	1.26 GHz～2.52 GHz	3x:792 MHz 4x:1188 MHz	Yes	No	< 200ps	500us

2.5.4 Programming Guidelines

NOTE

It is not suggested to enable or disable the PLLs frequently during usage. Because the enabling and disabling of PLL will cause a mutual interference between PLLs, which will affect system stability. When the clock is not required, it is recommended to configure the PLL_OUTPUT_GATE bit of PLL control register as 0 instead of writing 0 to the enable bit.

2.5.4.1 Enabling the PLL

Follow the steps below to enable the PLL:

Step 1 Configure the N, M, and P factors of the PLL control register.

Step 2 Write 1 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register, write 0 to the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register.

Step 3 Write 1 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

Step 4 Wait for the status of the Lock to change to 1.

Step 5 Delay 20 us.

Step 6 Write the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register to 1 and then the PLL will be available.

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2.5.4.2 Configuring the Frequency of General PLLs

Step 1 Make sure the PLL is enabled. If not, refer to section 2.5.4.1 Enabling the PLL to enable the PLL.

Step 2 Configure the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register as 0 to disable the output gate of the PLL. Because, general PLLs are unavailable in the process of frequency modulation.

Step 3 Configure the N and M factors. (It is not suggested to configure M1 factor)

Step 4 Write 0 and then write 1 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

Step 5 Wait for the LOCK bit (bit [28]) of the PLL control register to 1.

Step 6 Configure PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register to 1.

2.5.4.3 Configuring the Frequency of PLL_AUDIO0

The frequency configuration formula of PLL_AUDIO0:

PLL_AUDIO0 = 24 MHz*N/M0/M1/P

PLL_AUDIO0 does not support dynamic adjustment because changing any parameter of N, M0, M1, and P will affect the normal work of PLL, and the PLL will need to be relocked.

Generally, PLL_AUDIO0 only needs two frequency points: 24.576*4 MHz or 22.5792*4 MHz. For these two frequencies, there are usually special recommended matching factors. To implement the desired frequency point of PLL_AUDIO0, you need to use the decimal frequency-division function, so follow the steps below:

Step 1 Configure the N, M0, M1 and P factors.

Step 2 Write 1 to the PLL_SDM_EN bit (bit [24]) of PLL_AUDIO0_CTRL register.

Step 3 Configure PLL_AUDIO0_PAT0_CTRL register to enable the digital spread spectrum.

Step 4 Write 0 and then write 1 to the LOCK ENABLE bit (bit [29]) of PLL_AUDIO0_CTRL register.

Step 5 Write 1 to the LOCK bit (bit [28]) of PLL_AUDIO0_CTRL register.

NOTE

- When the P factor of PLL_AUDIO0 is an odd number, the clock output is an unequal-duty-cycle signal.
- A523 includes PLL_AUDIO0 and PLL_AUDIO1. For detailed description of PLL_AUDIO1, please refer to section 2.11 Power Reset Clock Management (PRCM).

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2.5.4.4 Disabling the PLL

Follow the steps below to disable the PLL:

Step 1 Write 0 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register.

Step 2 Write 0 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

2.5.4.5 Implementing Spread Spectrum

The spread spectrum technology is to convert a narrowband signal into a wideband signal. It helps to reduce the effect of electromagnetic interference (EMI) associated with the fundamental frequency of the signal.

For the general PLL frequency, the calculation formula is as follows:

$$f = \frac{N+1+X}{P\cdot(M0+1)\cdot(M1+1)}\cdot 24MHz, 0<X<1$$

Where,

P is the frequency division factor of module or PLL;

M0 is the post-frequency division factor of PLL;

M1 is the pre-frequency division factor of PLL;

N is the frequency doubling factor of PLL;

X is the amplitude coefficient of the spread spectrum.

The parameters N, P, M1, and M0 are for the frequency division.

When M1 = 0, M0 = 0, and P = 1 (no frequency division), the calculation formula of PLL frequency can be simplified as follows:

$$f = (N+1+X)\cdot 24MHz, 0<X<1$$

$$[f_1, f_2] = (N+1+[X_1, X_2])\cdot 24MHz$$

$$SDM\_BOT = 2^{17}\cdot X_1$$

$$\text{WAVE\_STEP} = 2^{17}\cdot(X_2 - X_1)/(24\,\text{MHz}/PREQ)\cdot 2$$

Where, SDM_BOT and WAVE_STEP are bits of the PLL pattern control register, and PREQ is the frequency of the spread spectrum.

NOTE

Different PLLs have different calculate formulas, refer to the CTRL register of the corresponding PLL in section 2.5.6 Register Description.

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Follow the steps below to implement the spread spectrum:

Step 1 Configure the control register of the corresponding PLL

a) Calculate the factor N and decimal value X according to the PLL frequency and PLL frequency formula. Refer to the control register of the corresponding PLL (named PLL_xxx_CTRL_REG, where xxx is the module name) in 2.5.6 Register Description for the corresponding PLL frequency formula.

b) Write M0, M1, N, and PLL frequency to the PLL control register.

c) Configure the PLL_SDM_EN bit (bit [24]) of the PLL control register to 1 to enable the spread spectrum function.

Step 2 Configure the pattern control register of the corresponding PLL

a) Calculate the SDM_BOT and WAVE_STEP of the pattern control register according to decimal value X and spread spectrum frequency (the bit [18:17] of the PLL pattern register)

b) Configure the spread spectrum mode (SPR_FREQ_MODE) to 2 or 3.

c) If the PLL_INPUT_DIV2 of the PLL control register is 1, configure the spread spectrum clock source select bit (SDM_CLK_SEL) of the PLL pattern control register to 1. Otherwise, configure SDM_CLK_SEL to the default value 0.

d) Write SDM_BOT, WAVE_STEP, PREQ, SPR_FREQ_MODE, and SDM_CLK_SEL to the PLL pattern control register, and configure the SIG_DELT_PAT_EN bit (bit [31]) of this register to 1.

Step 3 Delay 20 us

2.5.4.6 Configuring Bus Clock

The bus clock supports dynamic switching, but the process of switching needs to follow the following two rules.

- From a higher frequency to a lower frequency: switch the clock source first, and then set the frequency division factor;
- From a lower frequency to a higher frequency: configure the frequency division factor first, and then switch the clock source.

The bus frequency for each bus is as follows:

- AXI: It is suggested to be configured as the CPU clock frequency divided by 3. when the CPU clock frequency is less than 1.2 GHz, AXI frequency could be configured as the CPU clock frequency divided by 2.
- AHB: Maximum 200 MHz
- APB0: Maximum 100 MHz
- APB1: Maximum 160 MHz

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- MBUS: Maximum 700 MHz
- IOMMU: Maximum 600 MHz

2.5.4.7 Configuring Module Clock

For the Bus Gating Reset register of a module, the reset bit is de-asserted first, and then the clock gating bit is enabled to avoid potential problems caused by the asynchronous release of the reset signal.

For all module clocks except the DDR clock, configure the clock source and frequency division factor first, and then release the clock gating (that is, set to 1). For the configuration order of the clock source and frequency division factor, follow the rules below:

- With the increasing of the clock source frequency, configure the frequency division factor before the clock source;
- With the decreasing of the clock source frequency, configure the clock source before the frequency division factor.

2.5.5 Register List

NOTE

- Before switching the glitch-free MUX, ensure that
  - Every clock source is in use.
  - The switching time is longer than two clock periods of the slowest clock source.
- Before switching the normal MUX, ensure that the clock sources are closed.

Module Name	Base Address
CCU	0x0200 1000

Register Name	Offset	Description
PLL_DDR_CTRL_REG	0x0010	PLL_DDR Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register
PLL_PERI1_CTRL_REG	0x0028	PLL_PERI1 Control Register
PLL_GPU_CTRL_REG	0x0030	PLL_GPU Control Register
PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_VIDEO1_CTRL_REG	0x0048	PLL_VIDEO1 Control Register
PLL_VIDEO2_CTRL_REG	0x0050	PLL_VIDEO2 Control Register
PLL_VE_CTRL_REG	0x0058	PLL_VE Control Register
PLL_VIDEO3_CTRL_REG	0x0068	PLL_VIDEO3 Control Register
PLL_AUDIO0_CTRL_REG	0x0078	PLL_AUDIO0 Control Register

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Register Name	Offset	Description
PLL_DDR_PAT0_CTRL_REG	0x0110	PLL_DDR Pattern0 Control Register
PLL_DDR_PAT1_CTRL_REG	0x0114	PLL_DDR Pattern1 Control Register
PLL_PERI0_PAT0_CTRL_REG	0x0120	PLL_PERI0 Pattern0 Control Register
PLL_PERI0_PAT1_CTRL_REG	0x0124	PLL_PERI0 Pattern1 Control Register
PLL_PERI1_PAT0_CTRL_REG	0x0128	PLL_PERI1 Pattern0 Control Register
PLL_PERI1_PAT1_CTRL_REG	0x012C	PLL_PERI1 Pattern1 Control Register
PLL_GPU_PAT0_CTRL_REG	0x0130	PLL_GPU Pattern0 Control Register
PLL_GPU_PAT1_CTRL_REG	0x0134	PLL_GPU Pattern1 Control Register
PLL_VIDEO0_PAT0_CTRL_REG	0x0140	PLL_VIDEO0 Pattern0 Control Register
PLL_VIDEO0_PAT1_CTRL_REG	0x0144	PLL_VIDEO0 Pattern1 Control Register
PLL_VIDEO1_PAT0_CTRL_REG	0x0148	PLL_VIDEO1 Pattern0 Control Register
PLL_VIDEO1_PAT1_CTRL_REG	0x014C	PLL_VIDEO1 Pattern1 Control Register
PLL_VIDEO2_PAT0_CTRL_REG	0x0150	PLL_VIDEO2 Pattern0 Control Register
PLL_VIDEO2_PAT1_CTRL_REG	0x0154	PLL_VIDEO2 Pattern1 Control Register
PLL_VE_PAT0_CTRL_REG	0x0158	PLL_VE Pattern0 Control Register
PLL_VE_PAT1_CTRL_REG	0x015C	PLL_VE Pattern1 Control Register
PLL_VIDEO3_PAT0_CTRL_REG	0x0168	PLL_VIDEO3 Pattern0 Control Register
PLL_VIDEO3_PAT1_CTRL_REG	0x016C	PLL_VIDEO3 Pattern1 Control Register
PLL_AUDIO0_PAT0_CTRL_REG	0x0178	PLL_AUDIO0 Pattern0 Control Register
PLL_AUDIO0_PAT1_CTRL_REG	0x017C	PLL_AUDIO0 Pattern1 Control Register
PLL_DDR_BIAS_REG	0x0310	PLL_DDR Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_PERI1_BIAS_REG	0x0328	PLL_PERI1 Bias Register
PLL_GPU_BIAS_REG	0x0330	PLL_GPU Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_VIDEO1_BIAS_REG	0x0348	PLL_VIDEO1 Bias Register
PLL_VIDEO2_BIAS_REG	0x0350	PLL_VIDEO2 Bias Register
PLL_VE_BIAS_REG	0x0358	PLL_VE Bias Register
PLL_VIDEO3_BIAS_REG	0x0368	PLL_VIDEO3 Bias Register
PLL_AUDIO0_BIAS_REG	0x0378	PLL_AUDIO0 Bias Register
AHB_CLK_REG	0x0510	AHB Clock Register
APB0_CLK_REG	0x0520	APB0 Clock Register
APB1_CLK_REG	0x0524	APB1 Clock Register
MBUS_CLK_REG	0x0540	MBUS Clock Register
NSI_BGR_REG	0x054C	NSI Bus Gating Reset Register
GIC_CLK_REG	0x0550	GIC Clock Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
DI_CLK_REG	0x0620	DI Clock Register
DI_BGR_REG	0x062C	DI Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register

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Register Name	Offset	Description
DE_SYS_BGR_REG	0x064C	DE_SYS Bus Gating Reset Register
GPU_CLK_REG	0x0670	GPU Clock Register
GPU_GATING_REG	0x067C	GPU Gating Reset Configuration Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
DMAC_BGR_REG	0x070C	DMAC Bus Gating Reset Register
CPUX_MSGBOX_BGR_REG	0x071C	CPUX_MSGBOX Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	SPINLOCK Bus Gating Reset Register
CPUX_TIMER0_CLK_REG	0x0730	CPUX_TIMER0 Clock Register
CPUX_TIMER1_CLK_REG	0x0734	CPUX_TIMER1 Clock Register
CPUX_TIMER2_CLK_REG	0x0738	CPUX_TIMER2 Clock Register
CPUX_TIMER3_CLK_REG	0x073C	CPUX_TIMER3 Clock Register
CPUX_TIMER4_CLK_REG	0x0740	CPUX_TIMER4 Clock Register
CPUX_TIMER5_CLK_REG	0x0744	CPUX_TIMER5 Clock Register
CPUX_TIMER_BGR_REG	0x074C	CPUX_TIMER Bus Gating Reset Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PWMCTRL_BGR_REG	0x07AC	PWMCTRL Bus Gating Reset Register
IOMMU_CLK_REG	0x07B0	IOMMU Clock Register
IOMMU_BGR_REG	0x07BC	IOMMU Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MAT_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
NDFC_CLK0_CLK_REG	0x0810	NDFC CLK0 Clock Register
NDFC_CLK1_CLK_REG	0x0814	NDFC CLK1 Clock Register
NDFC_BGR_REG	0x082C	NDFC Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
SYSDAP_BGR_REG	0x088C	SYSDAP Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPIFC_CLK_REG	0x0950	SPIFC Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
GMAC_25M_CLK_REG	0x0970	GMAC_25M Clock Register
GMAC_BGR_REG	0x097C	GMAC Bus Gating Reset Register
IRRX_CLK_REG	0x0990	IRRX Clock Register

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Register Name	Offset	Description
IRRX_BGR_REG	0x099C	IRRX Bus Gating Reset Register
IRTX_CLK_REG	0x09C0	IRTX Clock Register
IRTX_BGR_REG	0x09CC	IRTX Bus Gating Reset Register
GPADC_24M_CLK_REG	0x09E0	GPADC_24M Clock Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
USB0_CLK_REG	0x0A70	USB0 Clock Register
USB1_CLK_REG	0x0A74	USB1 Clock Register
USB2_REF_CLK_REG	0x0A80	USB2_REF Clock Register
USB3_PCIE_REF_CLK_REG	0x0A84	USB3_PCIE Reference Clock Register
USB3_SUSPEND_CLK_REG	0x0A88	USB3_SUSPEND Clock Register
USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
LRADC_BGR_REG	0x0A9C	LRADC Bus Gating Reset Register
PCIE_AUX_CLK_REG	0x0AA0	PCIE_AUX Clock Register
PCIE_BGR_REG	0x0AAC	PCIE Bus Gating Reset Register
DISPLAY0_TOP_BGR_REG	0x0ABC	DISPLAY0_TOP Bus Gating Reset Register
DSI0_CLK_REG	0x0B24	DSI0 Clock Register
DSI1_CLK_REG	0x0B28	DSI1 Clock Register
DSI_BGR_REG	0x0B4C	DSI Bus Gating Reset Register
TCONLCD0_CLK_REG	0x0B60	TCONLCD0 Clock Register
TCONLCD1_CLK_REG	0x0B64	TCONLCD1 Clock Register
COMBOPHY_DSI0_CLK_REG	0x0B6C	COMBOPHY_DSI0 Clock Register
COMBOPHY_DSI1_CLK_REG	0x0B70	COMBOPHY_DSI1 Clock Register
TCONLCD_BGR_REG	0x0B7C	TCONLCD Bus Gating Reset Register
TCONTV1_CLK_REG	0x0B84	TCONTV1 Clock Register
TCONTV_BGR_REG	0x0B9C	TCONTV Bus Gating Reset Register
LVDS_BGR_REG	0x0BAC	LVDS Bus Gating Reset Register
EDP_CLK_REG	0x0BB0	EDP Clock Register
EDP_BGR_REG	0x0BBC	EDP Bus Gating Reset Register
VIDEO_OUT_BGR_REG	0x0BCC	Video out Bus Gating Reset Register
LEDC_CLK_REG	0x0BF0	LEDC Clock Register
LEDC_BGR_REG	0x0BFC	LEDC Bus Gating Reset Register
CSI_CLK_REG	0x0C04	CSI Clock Register
CSI_MASTER0_CLK_REG	0x0C08	CSI Master0 Clock Register
CSI_MASTER1_CLK_REG	0x0C0C	CSI Master1 Clock Register
CSI_MASTER2_CLK_REG	0x0C10	CSI Master2 Clock Register
CSI_MASTER3_CLK_REG	0x0C14	CSI Master3 Clock Register
CSI_BGR_REG	0x0C1C	CSI Bus Gating Reset Register
ISP_CLK_REG	0x0C20	ISP Clock Register
AHB_GATE_EN_REG	0x0E04	AHB Gate Enable Register
PERI0PLL_GATE_EN_REG	0x0E08	PERI0PLL Gate Enable Register
CLK24M_GATE_EN_REG	0x0E0C	CLK24M Gate Enable Register

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Register Name	Offset	Description
PERI1PLL_GATE_EN_REG	0x0E10	PERI1PLL Gate Enable Register
VIDEOPLL_GATE_EN_REG	0x0E14	VIDEOPLL Gate Enable Register
CM_GPU_CFG_REG	0x0E20	CM GPU Enable Configuration Register
CM_VE_CFG_REG	0x0E24	CM VE Enable Configuration Register
CM_DE_CFG_REG	0x0E28	CM DE Enable Configuration Register
CM_VI_CFG_REG	0x0E2C	CM VI Enable Configuration Register
CM_VO0_CFG_REG	0x0E30	CM VO0 Enable Configuration Register
CM_NDFC_CFG_REG	0x0E38	CM NDFC Enable Configuration Register
CM_PCIE_CFG_REG	0x0E3C	CM PCIE Enable Configuration Register
CCMU_SEC_SWITCH_REG	0x0F00	CCMU Security Switch Register
SYSDAP_REQ_CTRL_REG	0x0F08	SYSDAP REQ Control Register
CCMU_FAN_GATE_REG	0x0F30	CCMU FANOUT CLOCK GATE Register
CLK27M_FAN_REG	0x0F34	CLK27M FANOUT Register
CLK_FAN_REG	0x0F38	CLK FANOUT Register
CCMU_FAN_REG	0x0F3C	CCMU FANOUT Register
PLL_CFG0_REG	0x0F40	PLL Configuration0 Register
PLL_CFG1_REG	0x0F44	PLL Configuration1 Register
PLL_CFG2_REG	0x0F48	PLL Configuration2 Register

2.5.6 Register Description

2.5.6.1 0x0010 PLL_DDR Control Register (Default Value: 0x4800_2301)

Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The DDRPLL= InputFreq*N/M1/M0 The default value of PLL_DDR is 432 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK

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Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1:Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.5.6.2 0x0020 PLL_PERI0 Control Register (Default Value: 0x4821_6310)

Offset: 0x0020	Register Name: PLL_PERI0_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable PERI0PLL2X = 24MHz*N/M1/P0 PERI0_800M = 24MHz*N/M1/P1 PERI0_480M = 24MHz*N/M1/P2 PERI0_600M = PERI0PLL2X/2 PERI0_400M = PERI0PLL2X/3 PERI0_300M = PERI0_600M/2 PERI0_200M = PERI0_400M/2 PERI0_160M = PERI0_480M/3 PERI0_150M = PERI0_300M/2 When the crystal oscillator is 24 MHz, the default frequency of PERI0PLL2X is 1.2 GHz, the default frequency of PERI0_800M is 800 MHz, and the default frequency of PERI0_480M is 480 MHz. The output clock of PERI0PLL2X is fixed to 1.2 GHz and not suggested to change the parameter.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23	/	/	/

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Offset: 0x0020			Register Name: PLL_PERI0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
22:20	R/W	0x2	PLL_P1 PLL Output Div P1 P1=PLL_P1 + 1 PLL_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0 PLL Output Div P0 P0=PLL_P0 + 1 PLL_P0 is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_P2 PLL Output Div P2 P2=PLL_P2 + 1 PLL_P2 is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	/	/	/

2.5.6.3 0x0028 PLL_PERI1 Control Register (Default Value: 0x4821_6310)

Offset: 0x0028			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable

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Offset: 0x0028			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			PERI1PLL2X = 24MHz*N/M1/P0 PERI1_800M = 24MHz*N/M1/P1 PERI1_480M = 24MHz*N/M1/P2 PERI1_600M = PERI1PLL2X/2 PERI1_400M = PERI1PLL2X/3 PERI1_300M = PERI1_600M/2 PERI1_200M = PERI1_400M/2 PERI1_160M = PERI1_480M/3 PERI1_150M = PERI1_300M/2 When the crystal oscillator is 24 MHz, the default frequency of PERI1PLL2X is 1.2 GHz, the default frequency of PERI1_800M is 800 MHz, and the default frequency of PERI1_480M is 480 MHz. The output clock of PERI1PLL2X is fixed to 1.2 GHz and not suggested to change the parameter.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x2	PLL_P1 PLL Output Div P1

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Offset: 0x0028			Register Name: PLL_PERI1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			P1=PLL_P1 + 1 PLL_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0 PLL Output Div P0 P0=PLL_P0 + 1 PLL_P0 is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_P2 PLL Output Div P2 P2=PLL_P2 + 1 PLL_P2 is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	/	/	/

2.5.6.4 0x0030 PLL_GPU Control Register (Default Value: 0x4800_2301)

Offset: 0x0030			Register Name: PLL_GPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL_GPU = InputFreq*N/M1/M0 The default value of PLL_GPU is 432 MHz when the crystal

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Offset: 0x0030			Register Name: PLL_GPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable. 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL Factor N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1

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Offset: 0x0030			Register Name: PLL_GPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1

2.5.6.5 0x0040 PLL_VIDEO0 Control Register (Default Value: 0x4800_6201)

Offset: 0x0040			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable For application, VIDEO0PLL4X = InputFreq *N/M1/M0 VIDEO0PLL3X = InputFreq *N/M1/3 The default value of VIDEO0PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable 0: Disable

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Offset: 0x0040			Register Name: PLL_VIDEO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.5.6.6 0x0048 PLL_VIDEO1 Control Register (Default Value: 0x4800_6201)

Offset: 0x0048			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable For application, VIDEO1PLL4X = InputFreq *N/M1/M0 VIDEO1PLL3X = InputFreq *N/M1/3 The default value of VIDEO1PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable

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Offset: 0x0048			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2

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Offset: 0x0048			Register Name: PLL_VIDEO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.5.6.7 0x0050 PLL_VIDEO2 Control Register (Default Value: 0x4800_6201)

Offset: 0x0050			Register Name: PLL_VIDEO2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable For application, VIDEO2PLL4X = InputFreq *N/M1/M0. VIDEO2PLL3X = InputFreq *N/M1/3. The default value of VIDEO2PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N

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Offset: 0x0050			Register Name: PLL_VIDEO2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.5.6.8 0x0058 PLL_VE Control Register (Default Value: 0x4800_2301)

Offset: 0x0058			Register Name: PLL_VE_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL_VE = InputFreq*N/M1/M0 The default value of PLL_VE is 432 MHz when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable

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Offset: 0x0058			Register Name: PLL_VE_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

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2.5.6.9 0x0068 PLL_VIDEO3 Control Register (Default Value: 0x4800_6201)

Offset: 0x0068			Register Name: PLL_VIDEO3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable For application, VIDEO3PLL4X = InputFreq *N/M1/M0 VIDEO3PLL3X = InputFreq *N/M1/3 The default value of VIDEO3PLL4X is 1188MHz=24*99/2, when the crystal oscillator is 24 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level

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Offset: 0x0068			Register Name: PLL_VIDEO3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0 M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.5.6.10 0x0078 PLL_AUDIO0 Control Register (Default Value: 0x4814_5500)

Offset: 0x0078			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable AUDIO0PLL4X = 24MHz*N/M1/M0/P AUDIO0PLL2X = 24MHz*N/M1/M0/P/2 AUDIO0PLL1X = 24MHz*N/M1/M0/P/4 7.5≤N/M0/M1≤125 and 12≤N The working frequency range of 24MHz*N/M0/M1 is from 180 MHz to 3.0 GHz. The default frequency of PLL_AUDIO0PLL1X is 24.5714 MHz.
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK

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Offset: 0x0078			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) The bit is only valid when the bit29 is set to 1.
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23:22	/	/	/
21:16	R/W	0x14	PLL_P PLL Post Div P P= PLL_POST_DIV_P +1 PLL_POST_DIV_P is from 0 to 63.
15:8	R/W	0x55	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1 M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV2 PLL Output Div M0

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Offset: 0x0078			Register Name: PLL_AUDIO0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

2.5.6.11 0x0110 PLL_DDR Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.12 0x0114 PLL_DDR Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN

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Offset: 0x0114			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.13 0x0120 PLL_PERI0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PLL_PERI0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom.

2.5.6.14 0x0124 PLL_PERI0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable

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Offset: 0x0124			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.15 0x0128 PLL_PERI1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PLL_PERI1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.16 0x012C PLL_PERI1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/

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Offset: 0x012C			Register Name: PLL_PERI1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.17 0x0130 PLL_GPU Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PLL_GPU_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.18 0x0134 PLL_GPU Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0134	Register Name: PLL_GPU_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.19 0x0140 PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.20 0x0144 PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144	Register Name: PLL_VIDEO0_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.21 0x0148 PLL_VIDEO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_VIDEO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom.

2.5.6.22 0x014C PLL_VIDEO1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x014C	Register Name: PLL_VIDEO1_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.23 0x0150 PLL_VIDEO2 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PLL_VIDEO2_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.24 0x0154 PLL_VIDEO2 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0154	Register Name: PLL_VIDEO2_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.25 0x0158 PLL_VE Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PLL_VE_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.26 0x015C PLL_VE Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x015C	Register Name: PLL_VE_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.27 0x0168 PLL_VIDEO3 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PLL_VIDEO3_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.28 0x016C PLL_VIDEO3 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x016C	Register Name: PLL_VIDEO3_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.29 0x0178 PLL_AUDIO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO0_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: pulse swallow 01: Triangular(1bit) 10: Triangular(2bit) 11: Triangular(3bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24MHz 1: 12MHz When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.5.6.30 0x017C PLL_AUDIO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C	Register Name: PLL_AUDIO0_PAT1_CTRL_REG

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Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.5.6.31 0x0310 PLL_DDR Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.32 0x0320 PLL_PERI0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.33 0x0328 PLL_PERI1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0328			Register Name: PLL_PERI1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.34 0x0330 PLL_GPU Bias Register (Default Value: 0x0003_0000)

Offset: 0x0330	Register Name: PLL_GPU_BIAS_REG

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Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.35 0x0340 PLL_VIDEO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.36 0x0348 PLL_VIDEO1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0348			Register Name: PLL_VIDEO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL Bias Control
15:0	/	/	/

2.5.6.37 0x0350 PLL_VIDEO2 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0350			Register Name: PLL_VIDEO2_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL Bias Control
15:0	/	/	/

2.5.6.38 0x0358 PLL_VE Bias Register (Default Value: 0x0003_0000)

Offset: 0x0358			Register Name: PLL_VE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

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2.5.6.39 0x0368 PLL_VIDEO3 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0368			Register Name: PLL_VIDEO3_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.40 0x0378 PLL_AUDIO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL bias control
15:0	/	/	/

2.5.6.41 0x0510 AHB Clock Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: AHB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI0_600M_BUS The clock MUX supports glitch-free switch and dynamic configuration. AHB_CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31 The clock DIV supports glitch-free switch and dynamic configuration.

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2.5.6.42 0x0520 APB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI0_600M_BUS The clock MUX supports glitch-free switch and dynamic configuration. APB0_CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.5.6.43 0x0524 APB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: APB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK32K 010: CLK16M_RC 011: PERI0_600M_BUS 100: PERI0_480M_BUS The clock MUX supports glitch-free switch and dynamic configuration. APB1_CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic

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Offset: 0x0524			Register Name: APB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
			configuration.

2.5.6.44 0x0540 MBUS Clock Register (Default Value: 0xC000_0000)

Offset: 0x0540			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MBUS_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS CLK = Clock Source/M
30	R/W	0x1	MBUS_RST MBUS Reset 0: Assert 1: De-assert
29	/	/	/
28	R/W	0x0	MBUS_DFS_EN MBUS Clock Dynamic Frequency Scaling Enable 0: Disable 1: Enable
27	R/WAC	0x0	MBUS_UPD MBUS Clock Configuration 0 update 0: Invalid 1: Valid Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This register supports DRAM REQ/ACK signal. When MBUS_UPD is set to 1. MBUS_CLK_SEL and MBUS_CLK1 will be updated.
26:24	R/W	0x0	MBUS_CLK_SEL Clock Source Select 000: DDRPLL 001: PERI1_600M 010: PERI1_480M 011: PERI1_400M 100: PERI1_150M 101: HOSC The clock MUX supports glitch-free switch and dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	MBUS_DIV1

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Offset: 0x0540			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
			Factor M M= MBUS_DIV1 + 1 FACTOR M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.5.6.45 0x054C NSI Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x054C			Register Name: NSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	NSI_RST NSI Reset 0: Assert 1: De-assert
15:0	/	/	/

2.5.6.46 0x0550 GIC Clock Register (Default Value: 0x8000_0000)

Offset: 0x0550			Register Name: GIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	GIC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GIC_CLK = Clock Source/M
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK32K 010: PERI0_600M 011: PERI0_480M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.5.6.47 0x0600 DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DE_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DE_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO3PLL4X 011: VIDEO3PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.48 0x060C DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DE_RST DE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE_GATING Gating Clock for DE 0: Mask 1: Pass

2.5.6.49 0x0620 DI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0620			Register Name: DI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DI_CLK_GATING

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Offset: 0x0620			Register Name: DI_CLK_REG
Bit	Read/Write	Default/Hex	Description
			Gating Clock 0: Clock is OFF 1: Clock is ON DI_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO0PLL4X 011: VIDEO1PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.50 0x062C DI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x062C			Register Name: DI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DI_RST DI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DI_GATING Gating Clock for DI 0: Mask 1: Pass

2.5.6.51 0x0630 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	G2D_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON

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Offset: 0x0630			Register Name: G2D_CLK_REG
Bit	Read/Write	Default/Hex	Description
			G2D_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_400M 001: PERI0_300M 010: VIDEO0PLL4X 011: VIDEO1PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.52 0x063C G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	G2D_RST G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING Gating Clock for G2D 0: Mask 1: Pass

2.5.6.53 0x064C DE_SYS Bus Gating Reset Register (Default Value: 0x0001_0000)

Offset: 0x064C			Register Name: DE_SYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	DE_SYS_RST DE_SYS Reset 0: Assert 1: De-assert
15:0	/	/	/

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2.5.6.54 0x0670 GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x0670			Register Name: GPU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPU_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GPU_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: GPUPLL 001: PERI0_800M 010: PERI0_600M 011: PERI0_400M 100: PERI0_300M 101: PERI0_200M The clock selection supports glitch-free switch.
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M 0000: not mask 0001: mask 1 cycle at 16 cycles 0010: mask 2 cycles at 16 cycles 0011: mask 3 cycles at 16 cycles ..... 1111: mask 15 cycles at 16 cycles

2.5.6.55 0x067C GPU Gating Reset Configuration Register (Default Value: 0x0000_0000)

Offset: 0x067C			Register Name: GPU_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GPU_RST GPU Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPU_GATING Gating Clock for GPU 0: Mask

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Offset: 0x067C			Register Name: GPU_GATING_REG
Bit	Read/Write	Default/Hex	Description
			1: Pass

2.5.6.56 0x0680 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CE_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CE_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_480M 010: PERI0_400M 011: PERI0_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.5.6.57 0x068C CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG:
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CE_SYS_RST CE_SYS Reset 0: Assert 1: De-assert
16	R/W	0x0	CE_RST CE Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	CE_SYS_GATING Gating Clock for CE_SYS

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Offset: 0x068C			Register Name: CE_BGR_REG:
Bit	Read/Write	Default/Hex	Description
			0: Mask 1: Pass
0	R/W	0x0	CE_GATING Gating Clock for CE 0: Mask 1: Pass

2.5.6.58 0x0690 VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VE_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON VE_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VEPLL 001: PERI0_480M 010: PERI0_400M 011: PERI0_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.59 0x069C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	VE_RST VE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING

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Offset: 0x069C			Register Name: VE_BGR_REG
Bit	Read/Write	Default/Hex	Description
			Gating Clock for VE 0: Mask 1: Pass

2.5.6.60 0x070C DMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMAC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMAC_RST DMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMAC_GATING Gating Clock for DMAC 0: Mask 1: Pass

2.5.6.61 0x071C CPUX_MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: CPUX_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUX_MSGBOX_RST CPUX_MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUX_MSGBOX_GATING Gating Clock for CPUX_MSGBOX 0: Mask 1: Pass

2.5.6.62 0x072C SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

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Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	SPINLOCK_RST SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING Gating Clock for SPINLOCK 0: Mask 1: Pass

2.5.6.63 0x0730 CPUX_TIMER0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0730			Register Name: CPUX_TIMER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER0_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER0_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER0 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

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2.5.6.64 0x0734 CPUX_TIMER1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0734			Register Name: CPUX_TIMER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER1_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER1_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER1 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.5.6.65 0x0738 CPUX_TIMER2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0738			Register Name: CPUX_TIMER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER2_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER2_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select

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Offset: 0x0738			Register Name: CPUX_TIMER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
			00: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER2 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.5.6.66 0x073C CPUX_TIMER3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: CPUX_TIMER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER3_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER3_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER3 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1

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Offset: 0x073C			Register Name: CPUX_TIMER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
			001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.5.6.67 0x0740 CPUX_TIMER4 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: CPUX_TIMER4_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER4_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER4_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER4 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

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2.5.6.68 0x0744 CPUX_TIMER5 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0744			Register Name: CPUX_TIMER5_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CPUX_TIMER5_CLK_GATING Gating Clock 0: Disable 1: Enable CPUX_TIMER5_CLK=Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: CLK16M_RC 010: CLK32K 011: PERI0_200M CPUX_TIMER5 clock input, the clock source is 24MHz, RC 16 MHz, 32 kHz, or 200 MHz.
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128 Select the pre-scale of clock source.

2.5.6.69 0x074C CPUX_TIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x074C			Register Name: CPUX_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUX_TIMER_RST. CPUX_TIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUX_TIMER_GATING.

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Offset: 0x074C			Register Name: CPUX_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
			Gating Clock for CPUX_TIMER 0: Mask 1: Pass

2.5.6.70 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST DBGSYS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING Gating Clock for DBGSYS 0: Mask 1: Pass

2.5.6.71 0x07AC PWMCTRL Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	PWMCTRL1_RST PWMCTRL1 Reset 0: Assert 1: De-assert
16	R/W	0x0	PWMCTRL0_RST PWMCTRL0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	PWMCTRL1_GATING Gating Clock for PWMCTRL1 0: Mask 1: Pass
0	R/W	0x0	PWMCTRL0_GATING Gating Clock for PWMCTRL0 0: Mask

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Offset: 0x07AC			Register Name: PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
			1: Pass

2.5.6.72 0x07B0 IOMMU Clock Register (Default Value: 0x8000_0000)

Offset: 0x07B0			Register Name: IOMMU_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	IOMMU_CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON IOMMU_CLK = Clock Source/M
30:29	/	/	/
28	R/W	0x0	IOMMU_DFS_EN IOMMU CLK Dynamic Frequency Scaling Enable 0: Disable 1: Enable
27	R/WAC	0x0	IOMMU_UPD IOMMU Clock Configuration 0 update 0: Invalid 1: Valid Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This register supports DRAM REQ/ACK signal. When IOMMU_UPD is set to 1. IOMMU_CLK_SEL and IOMMU_CLK1 will be updated.
26:24	R/W	0x0	IOMMU_CLK_SEL Clock Source Select 000: PERI0_600M 001: DDRPLL 010: PERI1_480M 011: PERI1_400M 100: PERI1_150M 101: HOSC The clock MUX supports glitch-free switch and dynamic configuration.
23:5	/	/	/
4:0	R/W	0x0	IOMMU_DIV1 Factor M M= IOMMU_DIV1 + 1 FACTOR M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic

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Offset: 0x07B0			Register Name: IOMMU_CLK_REG
Bit	Read/Write	Default/Hex	Description
			configuration.

2.5.6.73 0x07BC IOMMU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07BC			Register Name: IOMMU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	IOMMU_GATING Gating Clock for IOMMU 0: Mask 1: Pass

2.5.6.74 0x0800 DRAM Clock Register (Default Value: 0x8000_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	DRAM_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DRAM_CLK = Clock Source/M
30:28	/	/	/
27	R/WAC	0x0	DRAM_UPD SDRCLK Configuration 0 update 0: Invalid 1: Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. This register supports DRAM REQ/ACK signal. When DRAM_UPD is set to 1, DRAM_CLK_GATING, DRAM_CLK_SEL, and DRAM_DIV1 will be updated.
26:24	R/W	0x0	DRAM_CLK_SEL Clock Source Select 000: DDRPLL 001: PERI1_600M 010: PERI1_480M 011: PERI1_400M 100: PERI1_150M The clock MUX supports glitch-free switch and dynamic configuration.

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Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:5	/	/	/
4:0	R/W	0x0	DRAM_DIV1 Factor M M= DRAM_DIV1 + 1 FACTOR M is from 0 to 31. The clock DIV supports glitch-free switch and dynamic configuration.

2.5.6.75 0x0804 MBUS Master Clock Gating Register (Default Value: 0x03D7_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x1	USB_SYS_MBUS_GATE_SW_CFG USB_SYS MBUS Clock Gate Enable 0: Disable 1:Enable
24	R/W	0x1	GPU_MBUS_GATE_SW_CFG GPU MBUS Clock Gate Enable 0: Disable 1:Enable
23	R/W	0x1	DE_SYS_MBUS_GATE_SW_CFG DE_SYS MBUS Clock Gate Enable 0: Disable 1:Enable
22	R/W	0x1	NDFC_MBUS_GATE_SW_CFG NDFC MBUS Clock Gate Enable 0: Disable 1:Enable
21	/	/	/
20	R/W	0x1	VID_IN_MBUS_GATE_SW_CFG VID_IN MBUS Clock Gate Enable 0: Disable 1:Enable
19	/	/	/
18	R/W	0x1	CE_MBUS_GATE_SW_CFG CE MBUS Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	VE_MBUS_GATE_SW_CFG

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Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	Read/Write	Default/Hex	Description
			VE MBUS Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	DMAC_MBUS_GATE_SW_CFG DMAC MBUS Clock Gate Enable 0: Disable 1:Enable
15:10	/	/	/
9	R/W	0x0	ISP_MCLK_EN Gating MBUS Clock for ISP 0: Mask 1: Pass
8	R/W	0x0	CSI_MCLK_EN Gating MBUS Clock for CSI 0: Mask 1: Pass
7	/	/	/
6	R/W	0x0	USB3_MCLK_EN Gating MBUS Clock for USB3 0: Mask 1: Pass
5	R/W	0x0	NDFC_MCLK_EN Gating MBUS Clock for NDFC 0: Mask 1: Pass
4:3	/	/	/
2	R/W	0x0	CE_MCLK_EN Gating MBUS Clock for CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_EN Gating MBUS Clock for VE 0: Mask 1: Pass
0	R/W	0x0	DMAC_MCLK_EN Gating MBUS Clock for DMAC 0: Mask 1: Pass

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2.5.6.76 0x080C DRAM Bus Gating Reset Register (Default Value: 0x0000_0001)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DRAM_RST DRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	DRAM_GATING Gating Clock for DRAM 0: Mask 1: Pass

2.5.6.77 0x0810 NDFC CLK0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0810			Register Name: NDFC_CLK0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NDFC_CLK0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON NDFC_CLK0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.5.6.78 0x0814 NDFC CLK1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: NDFC_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0814			Register Name: NDFC_CLK1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NDFC_CLK1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON NDFC_CLK1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.5.6.79 0x082C NDFC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: NDFC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	NDFC_RST NDFC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NDFC_GATING Gating Clock for NDFC 0: Mask 1: Pass

2.5.6.80 0x0830 SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC0_CLK_GATING Gating Clock

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Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
			0: Clock is OFF 1: Clock is ON SMHC0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.81 0x0834 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SMHC1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100: PERI1_300M
23:13	/	/	/

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Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.82 0x0838 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SMHC2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SMHC2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_800M 010: PERI0_600M 011: PERI1_800M 100: PERI1_600M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.5.6.83 0x084C SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST SMHC1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST SMHC0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING Gating Clock for SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING Gating Clock for SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING Gating Clock for SMHC0 0: Mask 1: Pass

2.5.6.84 0x088C SYSDAP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x088C			Register Name: SYSDAP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	SYSDAP_RST SYSDAP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SYSDAP_GATING

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Offset: 0x088C			Register Name: SYSDAP_BGR_REG
Bit	Read/Write	Default/Hex	Description
			Gating Clock for DRAM 0: Mask 1: Pass

2.5.6.85 0x090C UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	UART7_RST UART7 Reset 0: Assert 1: De-assert
22	R/W	0x0	UART6_RST UART6 Reset 0: Assert 1: De-assert
21	R/W	0x0	UART5_RST UART5 Reset 0: Assert 1: De-assert
20	R/W	0x0	UART4_RST UART4 Reset 0: Assert 1: De-assert
19	R/W	0x0	UART3_RST UART3 Reset 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST UART2 Reset 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST UART0 Reset 0: Assert 1: De-assert

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Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
15:8	/	/	/
7	R/W	0x0	UART7_GATING Gating Clock for UART7 0: Mask 1: Pass
6	R/W	0x0	UART6_GATING Gating Clock for UART6 0: Mask 1: Pass
5	R/W	0x0	UART5_GATING Gating Clock for UART5 0: Mask 1: Pass
4	R/W	0x0	UART4_GATING Gating Clock for UART4 0: Mask 1: Pass
3	R/W	0x0	UART3_GATING Gating Clock for UART3 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING Gating Clock for UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING Gating Clock for UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING Gating Clock for UART0 0: Mask 1: Pass

2.5.6.86 0x091C TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	TWI5_RST TWI5 Reset

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Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
			0: Assert 1: De-assert
20	R/W	0x0	TWI4_RST TWI4 Reset 0: Assert 1: De-assert
19	R/W	0x0	TWI3_RST TWI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST TWI0 Reset 0: Assert 1: De-assert
15:6	/	/	/
5	R/W	0x0	TWI5_GATING Gating Clock for TWI5 0: Mask 1: Pass
4	R/W	0x0	TWI4_GATING Gating Clock for TWI4 0: Mask 1: Pass
3	R/W	0x0	TWI3_GATING Gating Clock for TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING Gating Clock for TWI2 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING Gating Clock for TWI1

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Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
			0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING Gating Clock for TWI0 0: Mask 1: Pass

2.5.6.87 0x0940 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPI0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100:PERI1_200M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.88 0x0944 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI1_CLK_GATING

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Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
			Gating Clock 0: Clock is OFF 1: Clock is ON SPI1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100:PERI1_200M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.89 0x0948 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPI2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPI2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_300M 010: PERI0_200M 011: PERI1_300M 100:PERI1_200M
23:13	/	/	/

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Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	Read/Write	Default/Hex	Description
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.90 0x0950 SPIFC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0950			Register Name: SPIFC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPIFC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON SPIFC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_400M 010: PERI0_300M 011: PERI1_400M 100:PERI1_300M
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.5.6.91 0x096C SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	SPIFC_RST SPIFC Reset 0: Assert 1: De-assert
18	R/W	0x0	SPI2_RST SPI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST SPI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST SPI0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	SPIFC_GATING Gating Clock for SPIFC 0: Mask 1: Pass
2	R/W	0x0	SPI2_GATING Gating Clock for SPI2 0: Mask 1: Pass
1	R/W	0x0	SPI1_GATING Gating Clock for SPI1 0: Mask 1: Pass
0	R/W	0x0	SPI0_GATING Gating Clock for SPI0 0: Mask 1: Pass

2.5.6.92 0x0970 GMAC_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970	Register Name: GMAC_25M_CLK_REG

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GMAC_25M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GMAC_25M_CLK =PERI0_150M/6=25M
30	R/W	0x0	GMAC_25M_CLK_SRC_GATING Gating the Source Clock for Low Power Design 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

2.5.6.93 0x097C GMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: GMAC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GMAC_RST GMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GMAC_GATING Gating Clock for GMAC 0: Mask 1: Pass

2.5.6.94 0x0990 IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0990			Register Name: IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IRRX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON IRRX_CLK = Clock Source/M
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: CLK32K 1: HOSC
23:5	/	/	/

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Offset: 0x0990			Register Name: IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.95 0x099C IRRX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x099C			Register Name: IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	IRRX_RST IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRRX_GATING Gating Clock for IRRX 0: Mask 1: Pass

2.5.6.96 0x09C0 IRTX Clock Register (Default Value: 0x0000_0000)

Offset: 0x09C0			Register Name: IRTX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IRTX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON IRTX_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: HOSC 1: PERI1_600M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.5.6.97 0x09CC IRTX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09CC			Register Name: IRTX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	IRTX_RST IRTX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	IRTX_GATING Gating Clock for IRTX 0: Mask 1: Pass

2.5.6.98 0x09E0 GPADC_24M Clock Register (Default Value: 0x0000_0000)

Offset: 0x09E0			Register Name: GPADC_24M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	GPADC_24M_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON GPADC_24M_CLK = HOSC
30:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.99 0x09EC GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	GPADC_RST GPADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC_GATING Gating Clock for GPADC

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Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
			0: Mask 1: Pass

2.5.6.100 0x09FC THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			Register Name: THS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	THS_RST THS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING Gating Clock for THS 0: Mask 1: Pass

2.5.6.101 0x0A70 USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB0_CLKEN Gating Clock for OHCI0 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY0_RSTN USB PHY0 Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USB0_CLK12M_SEL OHCI0 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from HOSC 10: CLK32K 11: CLK16M_RC
23:0	/	/	/

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2.5.6.102 0x0A74 USB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A74			Register Name: USB1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB1_CLKEN Gating Clock for OHCI1 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY1_RSTN USB PHY1 Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USB1_CLK12M_SEL OHCI1 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from HOSC 10: CLK32K 11: CLK16M_RC
23:0	/	/	/

2.5.6.103 0x0A80 USB2_REF Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A80			Register Name: USB2_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB2_REF_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON USB2_REF_CLK = HOSC
30:0	/	/	/

2.5.6.104 0x0A84 USB3_PCIE_REF Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A84			Register Name: USB3_PCIE_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB3_PCIE_REF_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON USB3_REF_CLK = Clock Source
30:27	/	/	/

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Offset: 0x0A84			Register Name: USB3_PCIE_REF_CLK_REG
Bit	Read/Write	Default/Hex	Description
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: HOSC 01: PERI0_200M 10: PERI1_200M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.105 0x0A88 USB3_SUSPEND Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A88			Register Name: USB3_SUSPEND_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB3_SUSPEND_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON USB3_SUSPEND_CLK = Clock Source/M
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: CLK32K 1: HOSC
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.106 0x0A8C USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	USBDEVICE0_RST USBDEVICE0 Reset 0: Assert 1: De-assert

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Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21	R/W	0x0	USBEHCI1_RST USBEHCI1 Reset 0: Assert 1: De-assert
20	R/W	0x0	USBEHCI0_RST USBEHCI0 Reset 0: Assert 1: De-assert
19:18	/	/	/
17	R/W	0x0	USBOHCI1_RST USBOHCI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	USBOHCI0_RST USBOHCI0 Reset 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USBDEVICE0_GATING Gating Clock for USBDEVICE0 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	USBEHCI1_GATING Gating Clock for USBEHCI1 0: Mask 1: Pass
4	R/W	0x0	USBEHCI0_GATING Gating Clock for USBEHCI0 0: Mask 1: Pass
3:2	/	/	/
1	R/W	0x0	USBOHCI1_GATING Gating Clock for USBOHCI1 0: Mask 1: Pass
0	R/W	0x0	USBOHCI0_GATING Gating Clock for USBOHCI0 0: Mask 1: Pass

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2.5.6.107 0x0A9C LRADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A9C			Register Name: LRADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LRADC_RST LRADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LRADC_GATING Gating Clock for LRADC 0: Mask 1: Pass

2.5.6.108 0x0AA0 PCIE_AUX Clock Register (Default Value: 0x8000_0000)

Offset: 0x0AA0			Register Name: PCIE_AUX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	PCIE_AUX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON PCIE_REF_ALT_CLK = Clock Source/M
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: HOSC 1: CLK32K
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.109 0x0AAC PCIE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0AAC			Register Name:PCIE_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PCIE_USB3_SYS_RST PCIE POWER_UP Reset

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Offset: 0x0AAC			Register Name:PCIE_BGR_REG
Bit	Read/Write	Default/Hex	Description
			0: Assert 1: De-assert
15:0	/	/	/

2.5.6.110 0x0ABC DISPLAY0_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ABC			Register Name: DISPLAY0_TOP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DISPLAY0_TOP_RST DISPLAY0_TOP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DISPLAY0_TOP_GATING Gating Clock for DISPLAY0_TOP 0: Mask 1: Pass

2.5.6.111 0x0B24 DSI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: DSI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DSI0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_200M 010: PERI0_150M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.5.6.112 0x0B28 DSI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B28			Register Name: DSI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DSI1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DSI1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_200M 010: PERI0_150M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.113 0x0B4C DSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: DSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	DSI1_RST DSI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	DSI0_RST DSI0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	DSI1_GATING Gating Clock for DSI1 0: Mask 1: Pass
0	R/W	0x0	DSI0_GATING Gating Clock for DSI0 0: Mask

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Offset: 0x0B4C			Register Name: DSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
			1: Pass

2.5.6.114 0x0B60 TCONLCD0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCONLCD0_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONLCD0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.115 0x0B64 TCONLCD1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B64			Register Name: TCONLCD1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONLCD1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X

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Offset: 0x0B64			Register Name: TCONLCD1_CLK_REG
Bit	Read/Write	Default/Hex	Description
			001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 15.

2.5.6.116 0x0B6C COMBOPHY_DSI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B6C			Register Name: COMBOPHY_DSI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMBOPHY_DSI0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON COMBOPHY_DSI0_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.117 0x0B70 COMBOPHY_DSI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B70	Register Name: COMBOPHY_DSI1_CLK_REG

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COMBOPHY_DSI1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON COMBOPHY_DSI1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X 101: VIDEO0PLL3X 110:VIDEO1PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.118 0x0B7C TCONLCD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCONLCD_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	TCONLCD1_RST TCON LCD1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TCONLCD0_RST TCON LCD0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	TCONLCD1_GATING Gating Clock for TCON LCD1 0: Mask 1: Pass
0	R/W	0x0	TCONLCD0_GATING Gating Clock for TCON LCD0 0: Mask

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Offset: 0x0B7C			Register Name: TCONLCD_BGR_REG
Bit	Read/Write	Default/Hex	Description
			1: Pass

2.5.6.119 0x0B84 TCONTV1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B84			Register Name: TCONTV1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONTV1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON TCONTV1_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.120 0x0B9C TCONTV Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B9C			Register Name: TCONTV_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	TCONTV1_RST TCONTV1 Reset 0: Assert 1: De-assert
16:2	/	/	/
1	R/W	0x0	TCONTV1_GATING Gating Clock for TCONTV1 0: Mask 1: Pass
0	/	/	/

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2.5.6.121 0x0BAC LVDS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BAC			Register Name: LVDS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LVDS0_RST LVDS0 Reset 0: Assert 1: De-assert
15:0	/	/	/

2.5.6.122 0x0BB0 EDP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BB0			Register Name: EDP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EDP_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON EDP_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X 100: PERI0PLL2X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.123 0x0BBC EDP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BBC			Register Name: EDP_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EDP_RST EDP Reset 0: Assert

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Offset: 0x0BBC			Register Name: EDP_BGR_REG
Bit	Read/Write	Default/Hex	Description
			1: De-assert
15:1	/	/	/
0	R/W	0x0	EDP_GATING Gating Clock for EDP 0: Mask 1: Pass

2.5.6.124 0x0BCC Video Out Bus Gating Reset Register (Default Value: 0x0003_0000)

Offset: 0x0BCC			Register Name: VIDEO_OUT_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	VIDEO_OUT0_RST VIDEO_OUT0 Reset 0: Assert 1: De-assert
15:0	/	/	/

2.5.6.125 0x0BF0 LEDC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BF0			Register Name: LEDC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LEDC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON LEDC_CLK = Clock Source/M/N
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: PERI0_600M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

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2.5.6.126 0x0BFC LEDC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BFC			Register Name: LEDC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	LEDC_RST LEDC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	LEDC_GATING Gating Clock for LEDC 0: Mask 1: Pass

2.5.6.127 0x0C04 CSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: PERI0_480M 011: VIDEO3PLL4X 100: VIDEO3PLL3X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.128 0x0C08 CSI Master0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.129 0x0C0C CSI Master1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI_MASTER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X

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Offset: 0x0C0C			Register Name: CSI_MASTER1_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.130 0x0C10 CSI Master2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C10			Register Name: CSI_MASTER2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

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2.5.6.131 0x0C14 CSI Master3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C14			Register Name: CSI_MASTER3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_MASTER3_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON CSI_MASTER3_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: HOSC 001: VIDEO3PLL4X 010: VIDEO0PLL4X 011: VIDEO1PLL4X 100:VIDEO2PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.132 0x0C1C CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C1C			Register Name: CSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CSI_RST CSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING Gating Clock for CSI 0: Mask 1: Pass

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2.5.6.133 0x0C20 ISP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C20			Register Name: ISP_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ISP_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON ISP_CLK = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PERI0_300M 001: PERI0_400M 010: VIDEO2PLL4X 011: VIDEO3PLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.5.6.134 0x0E04 AHB Gate Enable Register (Default Value: 0x107F_0FFE)

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AHB_MONITOR_EN AHB bus auto clock gating function enable 1: enable auto clock gate 0: disable auto clock gate
30	/	/	/
29	R/W	0x0	SD_MONITOR_EN SD bus auto clock gating function enable 1: enable auto clock gate 0: disable auto clock gate
28	R/W	0x1	CPUS_HCLK_GATE_SW_CFG CPUS AHB Clock Gate Enable 0: Disable 1:Enable
27:23	/	/	/
22	R/W	0x1	SPIFC_MBUS_AHB_GATE_SW_CFG SPIFC MBUS_AHB Clock Gate Enable

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Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
21	/	/	/
20	R/W	0x1	GMAC_MBUS_AHB_GATE_SW_CFG GMAC MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
19	R/W	0x1	SMHC2_MBUS_AHB_GATE_SW_CFG SMHC2 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
18	R/W	0x1	SMHC1_MBUS_AHB_GATE_SW_CFG SMHC1 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
17	R/W	0x1	SMHC0_MBUS_AHB_GATE_SW_CFG SMHC0 MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
16	R/W	0x1	USB_MBUS_AHB_GATE_SW_CFG USB MBUS_AHB Clock Gate Enable 0: Disable 1: Enable
15:12	/	/	/
11	R/W	0x1	USB_SYS_AHB_GATE_SW_CFG USB_SYS AHB Clock Gate Enable 0: Disable 1: Enable
10	R/W	0x1	GPU_AHB_GATE_SW_CFG GPU AHB Clock Gate Enable 0: Disable 1: Enable
9	/	/	/
8	R/W	0x1	GMAC_AHB_GATE_SW_CFG GMAC AHB Clock Gate Enable 0: Disable 1: Enable
7	R/W	0x1	SMHC2_AHB_GATE_SW_CFG SMHC2 AHB Clock Gate Enable 0: Disable 1: Enable

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Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
6	R/W	0x1	SMHC1_AHB_GATE_SW_CFG SMHC1 AHB Clock Gate Enable 0: Disable 1: Enable
5	R/W	0x1	SMHC0_AHB_GATE_SW_CFG SMHC0 AHB Clock Gate Enable 0: Disable 1: Enable
4	R/W	0x1	USB_AHB_GATE_SW_CFG USB AHB Clock Gate Enable 0: Disable 1: Enable
3	R/W	0x1	VID_OUT_AHB_GATE_SW_CFG Video Out AHB Clock Gate Enable 0: Disable 1: Enable
2	R/W	0x1	VID_IN_AHB_GATE_SW_CFG Video in AHB Clock Gate Enable 0: Disable 1: Enable
1	R/W	0x1	VE_AHB_GATE_SW_CFG VE AHB Clock Gate Enable 0: Disable 1: Enable
0	/	/	/

2.5.6.135 0x0E08 PERI0PLL Gate Enable Register (Default Value: 0x8FFF_0FFF)

Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	PERI0PLL2X_GATE_SW_CFG PERI0PLL2X Clock Gate Enable 0: Disable 1:Enable
26	R/W	0x1	PERI0_800M_GATE_SW_CFG PERI0 800M Clock Gate Enable 0: Disable 1:Enable
25	R/W	0x1	PERI0_600M_GATE_SW_CFG PERI0 600M Clock Gate Enable

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Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
			0: Disable 1:Enable
24	R/W	0x1	PERI0_480M_GATE_ALL_CFG PERI0 480M Clock Gate Enable 0: Disable 1:Enable
23	R/W	0x1	PERI0_480M_GATE_SW_CFG PERI0 480M Clock Gate Enable 0: Disable 1:Enable
22	R/W	0x1	PERI0_160M_GATE_SW_CFG PERI0 160M Clock Gate Enable 0: Disable 1:Enable
21	R/W	0x1	PERI0_300M_GATE_ALL_CFG PERI0 300M Clock Gate Enable 0: Disable 1:Enable
20	R/W	0x1	PERI0_300M_GATE_SW_CFG PERI0 300M Clock Gate Enable 0: Disable 1:Enable
19	R/W	0x1	PERI0_150M_GATE_SW_CFG PERI0 150M Clock Gate Enable 0: Disable 1:Enable
18	R/W	0x1	PERI0_400M_GATE_ALL_CFG PERI0 400M Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	PERI0_400M_GATE_SW_CFG PERI0 400M Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	PERI0_200M_GATE_SW_CFG PERI0 200M Clock Gate Enable 0: Disable 1:Enable
15:12	/	/	/
11	R/W	0x1	PERI0PLL2X_AUTO_GATE_EN PERI0PLL2X Clock Auto Gate Enable

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Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
			0: Auto 1:No-Auto
10	R/W	0x1	PERI0_800M_AUTO_GATE_EN PERI0 800M Clock Auto Gate Enable 0: Auto 1:No-Auto
9	R/W	0x1	PERI0_600M_AUTO_GATE_EN PERI0 600M Clock Auto Gate Enable 0: Auto 1:No-Auto
8	R/W	0x1	PERI0_480M_AUTO_GATE_EN_ALL PERI0 480M Clock Auto Gate Enable 0: Auto 1:No-Auto
7	R/W	0x1	PERI0_480M_AUTO_GATE_EN PERI0 480M Clock Auto Gate Enable 0: Auto 1:No-Auto
6	R/W	0x1	PERI0_160M_AUTO_GATE_EN PERI0 160M Clock Auto Gate Enable 0: Auto 1:No-Auto
5	R/W	0x1	PERI0_300M_AUTO_GATE_EN_ALL PERI0 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
4	R/W	0x1	PERI0_300M_AUTO_GATE_EN PERI0 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
3	R/W	0x1	PERI0_150M_AUTO_GATE_EN PERI0 150M Clock Auto Gate Enable 0: Auto 1:No-Auto
2	R/W	0x1	PERI0_400M_AUTO_GATE_EN_ALL PERI0 400M Clock Auto Gate Enable All 0: Auto 1:No-Auto
1	R/W	0x1	PERI0_400M_AUTO_GATE_EN PERI0 400M Clock Auto Gate Enable 0: Auto

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Offset: 0x0E08			Register Name: PERI0PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
			1:No-Auto
0	R/W	0x1	PERI0_200M_AUTO_GATE_EN PERI0 200M Clock Auto Gate Enable 0: Auto 1:No-Auto

2.5.6.136 0x0E0C CLK24M Gate Enable Register (Default Value: 0x0000_0009)

Offset: 0x0E0C			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x1	RES_DCAP_24M_GATE_EN RES_DCAP 24M Clock Gate Enable 0: Disable 1:Enable
2:1	/	/	/
0	R/W	0x1	USB_24M_GATE_EN USB 24M Clock Gate Enable 0: Disable 1:Enable

2.5.6.137 0x0E10 PERI1PLL Gate Enable Register (Default Value: 0x8EBF_0EBF)

Offset: 0x0E10			Register Name: PERI1PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	PERI1_800M_GATE_SW_CFG PERI1 800M Clock Gate Enable 0: Disable 1:Enable
26	R/W	0x1	PERI1_600M_GATE_ALL_CFG PERI1 600M Clock Gate Enable 0: Disable 1:Enable
25	R/W	0x1	PERI1_600M_GATE_SW_CFG PERI1 600M Clock Gate Enable 0: Disable 1:Enable
24	/	/	/
23	R/W	0x1	PERI1_480M_GATE_SW_CFG

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Offset: 0x0E10			Register Name: PERI1PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
			PERI1 480M Clock Gate Enable 0: Disable 1:Enable
22	/	/	/
21	R/W	0x1	PERI1_300M_GATE_ALL_CFG PERI1 300M Clock Gate Enable 0: Disable 1:Enable
20	R/W	0x1	PERI1_300M_GATE_SW_CFG PERI1 300M Clock Gate Enable 0: Disable 1:Enable
19	R/W	0x1	PERI1_150M_GATE_SW_CFG PERI1 150M Clock Gate Enable 0: Disable 1:Enable
18	R/W	0x1	PERI1_400M_GATE_ALL_CFG PERI1 400M Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	PERI1_400M_GATE_SW_CFG PERI1 400M Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	PERI1_200M_GATE_SW_CFG PERI1 200M Clock Gate Enable 0: Disable 1:Enable
15:12	/	/	/
11	R/W	0x1	PERI1_800M_AUTO_GATE_EN PERI1 800M Clock Auto Gate Enable 0: Auto 1:No-Auto
10	R/W	0x1	PERI1_600M_AUTO_GATE_EN_ALL PERI1 600M Clock Auto Gate Enable 0: Auto 1:No-Auto
9	R/W	0x1	PERI1_600M_AUTO_GATE_EN PERI1 600M Clock Auto Gate Enable 0: Auto 1:No-Auto

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Offset: 0x0E10			Register Name: PERI1PLL_GATE_EN_REG:
Bit	Read/Write	Default/Hex	Description
8	/	/	/
7	R/W	0x1	PERI1_480M_AUTO_GATE_EN PERI1 480M Clock Auto Gate Enable 0: Auto 1:No-Auto
6	/	/	/
5	R/W	0x1	PERI1_300M_AUTO_GATE_EN_ALL PERI1 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
4	R/W	0x1	PERI1_300M_AUTO_GATE_EN PERI1 300M Clock Auto Gate Enable 0: Auto 1:No-Auto
3	R/W	0x1	PERI1_150M_AUTO_GATE_EN PERI1 150M Clock Auto Gate Enable 0: Auto 1:No-Auto
2	R/W	0x1	PERI1_400M_AUTO_GATE_EN_ALL PERI1 400M Clock Auto Gate Enable All 0: Auto 1:No-Auto
1	R/W	0x1	PERI1_400M_AUTO_GATE_EN PERI1 400M Clock Auto Gate Enable 0: Auto 1:No-Auto
0	R/W	0x1	PERI1_200M_AUTO_GATE_EN PERI1 200M Clock Auto Gate Enable 0: Auto 1:No-Auto

2.5.6.138 0x0E14 VIDEOPLL Gate Enable Register (Default Value: 0x00BF_00BF)

Offset: 0x0E14			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x1	VIDEO3PLL3X_GATE_SW_CFG VIDEO3PLL3X Clock Gate Enable 0: Disable 1:Enable

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Offset: 0x0E14			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
22	/	/	/
21	R/W	0x1	VIDEO1PLL3X_GATE_SW_CFG VIDEO1PLL3X Clock Gate Enable 0: Disable 1:Enable
20	R/W	0x1	VIDEO0PLL3X_GATE_SW_CFG VIDEO0PLL3X Clock Gate Enable 0: Disable 1:Enable
19	R/W	0x1	VIDEO3PLL4X_GATE_SW_CFG VIDEO3PLL4X Clock Gate Enable 0: Disable 1:Enable
18	R/W	0x1	VIDEO2PLL4X_GATE_SW_CFG VIDEO2PLL4X Clock Gate Enable 0: Disable 1:Enable
17	R/W	0x1	VIDEO1PLL4X_GATE_SW_CFG VIDEO1PLL4X Clock Gate Enable 0: Disable 1:Enable
16	R/W	0x1	VIDEO0PLL4X_GATE_SW_CFG VIDEO0PLL4X Clock Gate Enable 0: Disable 1:Enable
15:8	/	/	/
7	R/W	0x1	VIDEO3PLL3X_AUTO_GATE_EN VIDEO3PLL3X Clock Auto Gate Enable 0: Auto 1:No-Auto
6	/	/	/
5	R/W	0x1	VIDEO1PLL3X_AUTO_GATE_EN VIDEO1PLL3X Clock Auto Gate Enable 0: Auto 1:No-Auto
4	R/W	0x1	VIDEO0PLL3X_AUTO_GATE_EN VIDEO0PLL3X Clock Auto Gate Enable 0: Auto 1:No-Auto
3	R/W	0x1	VIDEO3PLL4X_AUTO_GATE_EN VIDEO3PLL4X Clock Auto Gate Enable

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Offset: 0x0E14			Register Name: VIDEOPLL_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Auto 1:No-Auto
2	R/W	0x1	VIDEO2PLL4X_AUTO_GATE_EN VIDEO2PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto
1	R/W	0x1	VIDEO1PLL4X_AUTO_GATE_EN VIDEO1PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto
0	R/W	0x1	VIDEO0PLL4X_AUTO_GATE_EN VIDEO0PLL4X Clock Auto Gate Enable 0: Auto 1:No-Auto

2.5.6.139 0x0E20 CM GPU Enable Configuration Register (Default Value: 0x0002_0000)

Offset: 0x0E20			Register Name: CM_GPU_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_GPU_STATUS CM GPU Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_GPU_MODULE_MODE CM GPU module mode 0: Disable 1: Enable

2.5.6.140 0x0E24 CM VE Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E24			Register Name: CM_VE_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VE_STATUS CM VE Status 01: Power OFF 10: Power ON
15:1	/	/	/

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Offset: 0x0E24			Register Name: CM_VE_CFG_REG
Bit	R/W	Default/Hex	Description
0	R/W	0x0	CM_VE_MODULE_MODE CM VE module mode 0: Disable 1: Enable

2.5.6.141 0x0E28 CM DE Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E28			Register Name: CM_DE_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_DE_STATUS CM DE Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_DE_MODULE_MODE CM DE module mode 0: Disable 1: Enable

2.5.6.142 0x0E2C CM VI Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E2C			Register Name: CM_VI_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VI_STATUS CM VI Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VI_MODULE_MODE CM VI module mode 0: Disable 1: Enable

2.5.6.143 0x0E30 CM VO0 Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E30			Register Name: CM_VO0_CFG_REG
Bit	R/W	Default/Hex	Description

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Offset: 0x0E30			Register Name: CM_VO0_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_VO0_STATUS CM VO0 Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_VO0_MODULE_MODE CM VO0 module mode 0: Disable 1: Enable

2.5.6.144 0x0E38 CM NDFC Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E38			Register Name: CM_NDFC_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_NDFC_STATUS CM NDFC Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_NDFC_MODULE_MODE CM NDFC module mode 0: Disable 1: Enable

2.5.6.145 0x0E3C CM PCIE Enable Configuration Register (Default Value:0x0002_0000)

Offset: 0x0E3C			Register Name: CM_PCIE_CFG_REG
Bit	R/W	Default/Hex	Description
31:18	/	/	/
17:16	R	0x2	CM_PCIE_STATUS CM PCIE Status 01: Power OFF 10: Power ON
15:1	/	/	/
0	R/W	0x0	CM_PCIE_MODULE_MODE CM PCIE module mode 0: Disable 1: Enable

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2.5.6.146 0x0F00 CCU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCU_SEC_SWITCH_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MBUS_SEC MBUS clock register security 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC Bus relevant registers security 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC PLL relevant registers security 0: Secure 1: Non-secure

2.5.6.147 0x0F08 SYSDAP REQ Control Register (Default Value: 0x0000_0001)

Offset: 0x0F08			Register Name: SYSDAP_REQ_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	SYSDAP_REQ_ENABLE 0：Disable 1：Enable By configuring this bit, SYSDAP REQ signal could be set to control the clock and reset of CE and DAPSYS.

2.5.6.148 0x0F30 CCU FANOUT CLOCK GATE Register (Default Value:0x0000_0000)

Offset: 0x0F30			Register Name: CCU_FAN_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	CLK50M_EN Gating for CLK50M 0: Clock is OFF 1: Clock is ON
3	R/W	0x0	CLK25M_EN Gating for CLK25M 0: Clock is OFF 1: Clock is ON

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Offset: 0x0F30			Register Name: CCU_FAN_GATE_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	CLK16M_EN Gating for CLK16M 0: Clock is OFF 1: Clock is ON
1	R/W	0x0	CLK12M_EN Gating for CLK12M 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	CLK24M_EN Gating for CLK24M 0: Clock is OFF 1: Clock is ON

2.5.6.149 0x0F34 CLK27M FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F34			Register Name: CLK27M_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CLK27M_EN Gating for CLK27M 0: Clock is OFF 1: Clock is ON SCLK=Clock Source/M/N
30:26	/	/	/
25:24	R/W	0x0	CLK27M_SCR_SEL Clock Source Select 000: VIDEO0PLL4X 001: VIDEO1PLL4X 010: VIDEO2PLL4X 011: VIDEO3PLL4X
23:13	/	/	/
12:8	R/W	0x0	CLK27M_DIV1 Factor N N= FACTOR_N +1 FACTOR_M is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	CLK27M_DIV0 Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

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2.5.6.150 0x0F38 CLK FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F38			Register Name: CLK_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCLK_DIV_EN Gating for PCLK 0: Clock is OFF 1: Clock is ON PCLK = APB0_CLK/M/N
30:10	/	/	/
9:5	R/W	0x0	PCLK_DIV1 Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
4:0	R/W	0x0	PCLK_DIV Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.5.6.151 0x0F3C CCU FANOUT Register (Default Value:0x0000_0007)

Offset: 0x0F3C			Register Name: CCU_FAN_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	Reserved
23	R/W	0x0	CLK_FANOUT2_EN Gating for CLK_FANOUT2 0: Clock is OFF 1: Clock is ON
22	R/W	0x0	CLK_FANOUT1_EN Gating for CLK_FANOUT1 0: Clock is OFF 1: Clock is ON
21	R/W	0x0	CLK_FANOUT0_EN Gating for CLK_FANOUT0 0: Clock is OFF 1: Clock is ON
20:18	/	/	/
17:9	R/W	0x0	Reserved
8:6	R/W	0x0	CLK_FANOUT2_SEL Clock Fanout2 Select 000: CLK32K_FANOUT (From SYSRTC)

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Offset: 0x0F3C			Register Name: CCU_FAN_REG
Bit	Read/Write	Default/Hex	Description
			001: CLK12M (From DCXO/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From DCXO) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK 111: CLK50M (From PERI0_150M/3) CLK_FANOUT2 can be selected to output from the above seven sources.
5:3	R/W	0x0	CLK_FANOUT1_SEL Clock Fanout1 Select 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From DCXO/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From DCXO) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK 111: CLK50M (From PERI0_150M/3) CLK_FANOUT1 can be selected to output from the above seven sources.
2:0	R/W	0x7	CLK_FANOUT0_SEL Clock Fanout0 Select 000: CLK32K_FANOUT (From SYSRTC) 001: CLK12M (From DCXO/2) 010: CLK16M (From PERI0_160M/10) 011: CLK24M (From DCXO) 100: CLK25M (From PERI0_150M/6) 101: CLK27M 110: PCLK 111: CLK50M (From PERI0_150M/3) CLK_FANOUT0 can be selected to output from the above seven sources.

2.5.6.152 0x0F40 PLL Configuration0 Register (Default Value: 0x0000_0000)

Offset: 0x0F40			Register Name: PLL_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG0 PLL Control Reserved Register

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2.5.6.153 0x0F44 PLL Configuration1 Register (Default Value: 0x0000_0000)

Offset: 0x0F44			Register Name: PLL_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG1 PLL Control Reserved Register

2.5.6.154 0x0F48 PLL Configuration2 Register (Default Value: 0x0000_0000)

Offset: 0x0F48			Register Name: PLL_CFG2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PLL_CONFIG2 PLL Control Reserved Register

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2.6 DMA Controller (DMAC)

2.6.1 Overview

The direct memory access (DMA) is a method of transferring data between peripherals and memories (including the SRAM and DRAM) without using the CPU. It is an efficient way to offload data transfer duties from the CPU. Without DMA, the CPU has to control all the data transfers. While with DMA, the DMAC directly transfers data between a peripheral and a memory, between peripherals, or between memories.

The DMAC has the following features:

- Up to 16-ch DMA in CPUX domain and 16-ch DMA in CPUS domain
- Provides 53 peripheral DMA requests for data reading and 53 peripheral DMA requests for data writing
- Transferring data with linked list
- Flexible data width: 8 bits, 16 bits, or, 32 bits
- Programmable DMA burst length
- DRQ response includes waiting mode and handshake mode
- Supports non-aligned transform for memory devices
- DMA channels that support the following:
  - Pausing DMA
  - BMODE and I/O speed mode
  - DMA timeout

NOTE

The following description focuses on the DMA of the CPUX domain.

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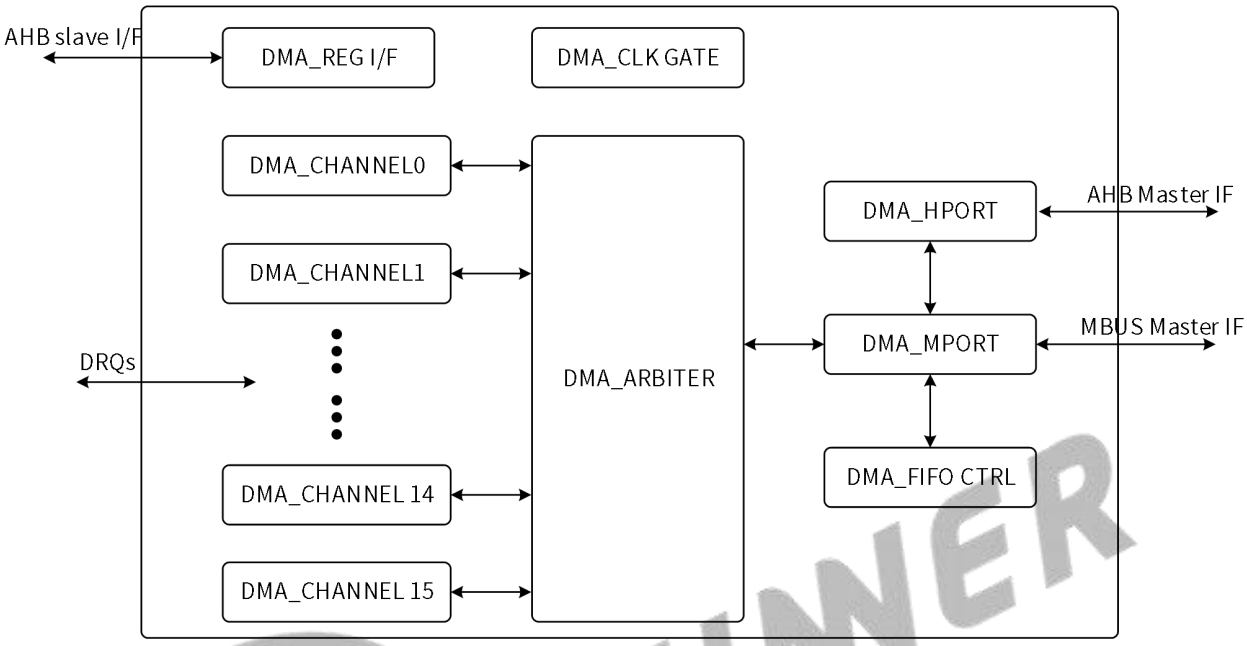
2.6.2 Block Diagram

The following figure shows a block diagram of DMAC.

Figure 2-10 DMAC Block Diagram



DMAC contains the following sub-blocks:

Table 2-11 DMAC Sub-blocks

Sub-block	Description
DMA_ARBITER	Arbitrates the DMA read/write requests from all channels, and converts the requests to the read/write requests of ports.
DMA_CHANNELs	DMA transfer engine. Each channel is independent. When the DMA requests from multiple peripherals are valid simultaneously, the channel with the highest priority starts data transfer first. The system uses the polling mechanism to decide the priorities of DMA channels. When DMA_ARBITER is idle, channel 0 has the highest priority, whereas channel 15 has the lowest priority. When DMA_ARBITER is busy processing the request from channel n, channel (n+1) has the highest priority. For n = 15, the channel (n + 1) should be channel 0.
DRQs	DMA requests. Peripherals use the DMA request signals to request a data transfer.
DMA_MPORT	Receives the read/write requests from DMA_ARBITER, and converts the requests to the corresponding MBUS access requests. It is mainly used for accessing the DRAM.
DMA_HPORT	The port for accessing the AHB Master. It is mainly used for accessing the SRAM and IO devices.
DMA_FIFO CTRL	Internal FIFO cell control module.

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Sub-block	Description
DMA_REG Interface	DMA_REG is the common register module that is mainly used to resolve AHB commands.
DMA_CLKGATE	The control module for hardware auto clock gating.

The DMAC integrates 16 independent DMA channels and each channel has an independent FIFO controller. When the DMA channel starts, the DMAC gets a DMA descriptor from the DMA_DESC_ADDR_REG and uses it as the configuration information for the data transfer of the current DMA package. Then the DMAC can transfer data between the specified devices. After transferring a DMA package, the DMAC judges if the current channel transfer is finished via the linked address in the descriptor. If the linked address shows all the packages are transferred, the DMAC will end the chain transmission and close the channel.

2.6.3 Functional Description

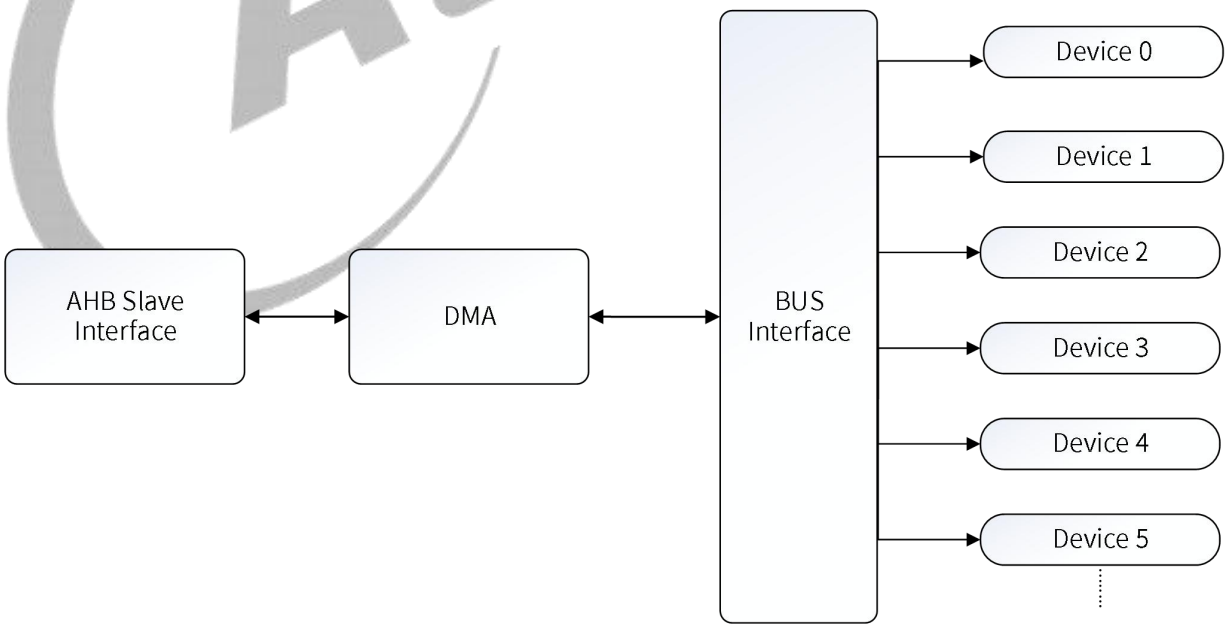
2.6.3.1 Clock

The DMAC is on AHB or MBUS. The clocks of AHB and MBUS influence the transfer efficiency of the DMAC.

2.6.3.2 Typical Application

The following figure shows a typical application of the DMAC.

Figure 2-11 DMAC Typical Application Diagram



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2.6.3.3 DRQ Port of Peripherals

The following tables show the source DRQ types and destination DRQ types of different ports.

Table 2-12 DMA DRQ Type

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2		port2	
port3		port3	
port4		port4	
port5		port5	
port6		port6	
port7		port7	
port8		port8	
port9		port9	
port10	NDFC	port10	NDFC
port11		port11	
port12	GPADC	Port12	
port13		port13	CIR_TX
port14	UART0_RX	port14	UART0_TX
port15	UART1_RX	port15	UART1_TX
port16	UART2_RX	port16	UART2_TX
port17	UART3_RX	port17	UART3_TX
port18	UART4_RX	port18	UART4_TX
port19	UART5_RX	port19	UART5_TX
port20	UART6_RX	Port20	UART6_TX
port21	UART7_RX	port21	UART7_TX
port22	SPI0_RX	port22	SPI0_TX
port23	SPI1_RX	port23	SPI1_TX
port24	SPI2_RX	port24	SPI2_TX
port25		port25	
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	USB0_EP1	Port30	USB0_EP1
Port31	USB0_EP2	Port31	USB0_EP2
Port32	USB0_EP3	Port32	USB0_EP3
Port33	USB0_EP4	Port33	USB0_EP4
Port34	USB0_EP5	Port34	USB0_EP5
Port35		Port35	
Port36		Port36	

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Source DRQ Type		Destination DRQ Type	
Port37		Port37	
Port38		Port38	
Port39		Port39	
Port40		Port40	
Port41		Port41	
Port42		Port42	LEDC
Port43	TWI0	Port43	TWI0
Port44	TWI1	Port44	TWI1
Port45	TWI2	Port45	TWI2
Port46	TWI3	Port46	TWI3
Port47	TWI4	Port47	TWI4
Port48	TWI5	Port48	TWI5
Port49	S_TWI0	Port49	S_TWI0
Port50	S_TWI1	Port50	S_TWI1
Port51	S_UART0	Port51	S_UART0
Port52	S_UART1	Port52	S_UART1
Port53	S_SPI0	Port53	S_SPI0

Table 2-13 DMA DRQ Type of MCU_DMAC

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2	OWA	port2	OWA
port3	I2S0_RX	port3	I2S0_TX
port4	I2S1_RX	port4	I2S1_TX
port5	I2S2_RX	port5	I2S2_TX
port6	I2S3_RX	port6	I2S3_TX
port7	AUDIO_CODEC	port7	AUDIO_CODEC
port8	DMIC	port8	
port9	S_TWI0	port9	S_TWI0
port10	S_TWI1	port10	S_TWI1
port11	S_UART0	port11	S_UART0
port12	S_UART1	port12	S_UART1
Port13	S_SPI0	Port13	S_SPI0
Port14	S_TWI2	Port14	S_TWI2

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2.6.3.4 DMA Descriptor

The DMAC descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words: Configuration, Source Address, Destination Address, Byte Counter, Parameter, and Link. The following figure shows the structure of the DMA descriptor.

Figure 2-12 DMA Descriptor

- **Configuration**: Configure the following information.
  - DRQ type: DRQ type of the source and destination devices.
  - Address counting mode: For both the source and destination devices, there are two address counting modes: the IO mode and linear mode. The IO mode is for IO devices whose address is fixed during the data transfer and the linear mode is for the memory whose address is increasing during the data transfer.
  - Transferred block length: How many times can non-memory peripherals transfer in a valid DRQ. The block length supports 1 time, 4 times, 8 times, and 16 times.
  - Transferred data width: The data width of operating the non-memory peripherals. The data width supports 8 bits, 16 bits, and 32 bits.

  NOTE

  The configuration supports BMODE mode. The BMODE is used in the following scenario: the source is an IO device, and the destination is a memory device. Setting the BMODE mode can limit the amount of block data transferred in DMA block transmission to the amount of data transferred when the DRQ threshold of the source IO device is 1.

- **Source Address**: Configure the address of the source device.
- **Destination Address**: Configure the address of the destination device.

  DMA reads data from the source address and then writes data to the destination address.

  Both the DMA source and destination addresses have 34 bits. In the descriptor, because there are only 32 bits in the Source/Destination Address field, another 2 bits are stored in the Parameter field.

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The following table shows the details of the related fields in the descriptor.

Table 2-14 Source/Destination Address Distribution

Descriptor Group	Bit	Description
Source Address	31:0	DMA transfers the lower 32 bits of the 34-bit source address
Destination Address	31:0	DMA transfers the lower 32 bits of the 34-bit destination address
Parameter	31	TIMEOUT Enable TIMEOUT only can be enabled in BMODE and IOspeed should be disabled when using this function.
	30:29	TIMEOUT Configuration 00: Not use sub-functions 01: Generate an interrupt and suspend the transmission after timeout. 10: Generate an interrupt and end the transmission after timeout. 11: Generate an interrupt and skip to the next descriptor after timeout.
	28:20	TIMEOUT Configuration Timer time of channels.
	19:18	DMA transfers the higher 2 bits of the 34-bit destination address
	17:16	DMA transfers the high 2 bits of the 34-bit source address
	15:9	Reserved
	8	I/O Speed Mode Enable If this bit is enabled, DMA will transmit the data of the I/O device from the source device or the destination device, or both of them at a faster speed. **Note: IOspeed and BMODE cannot be enabled at the same time.**
	7:0	Wait Clock Cycles Set the waiting time in DRQ mode
Link	31:2	The address of the next group descriptor, the lower 30 bits of the word address
	1:0	The address of the next group descriptor, the higher 2 bits of the word address

From the above table, you can get:

Real DMA source address (in byte mode) = {Parameter [17:16], Source Address [31:0]};

Real DMA destination address (in byte mode) = {Parameter [19:18], Destination Address [31:0]};

Real link address (in byte mode) = {Link [1:0], Link [31:2], 2'b00}.

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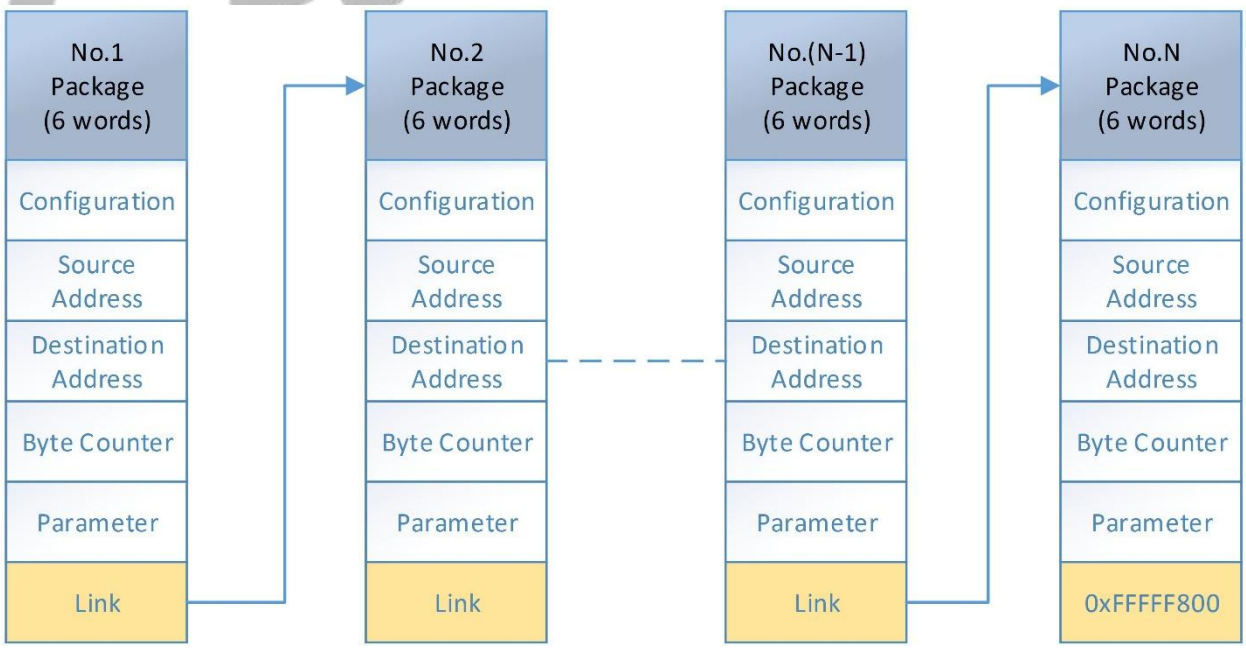
- **Byte counter**: Configure the data amount of a package. The maximum value is (2^25-1) bytes. If the data amount of the package reaches the maximum value, even if DRQ is valid, the DMA will stop the current transfer.
- **Parameter**: Configure the interval between the data block. The parameter is valid for non-memory peripherals. When DMA detects that the DRQ is high, the DMA transfers the data block and ignores the status changes of the DRQ until the data transfer finishes. After that, the DMA waits for certain clock cycles (WAIT_CYC) and executes the next DRQ detection. In addition, the Parameter is responsible for enabling and configuring TIMEOUT. In the case that the source device is an I/O device and the destination device is a memory device, the waiting time of a DRQ signal triggered by the source device can be set when TIMEOUT is enabled. When time is out, an interrupt signal of TIMEOUT will be generated by DMA. There are three sub-functions of TIMEOUT to be enabled (TIMEOUT will only generate interrupts if they are disabled): suspend the transmission of the current channel after an interrupt is generated; end the transmission of the current channel after an interrupt is generated; skip to the next descriptor for transmission after an interrupt is generated. (TIMEOUT only can be enabled in BMODE.)

  The Parameter also configures whether the IOspeed is enabled or not. If IOspeed is enabled, DMA will transmit the data of the I/O device from the source device or the destination device, or both of them at a faster speed. The larger block indicates a faster speed. However, when the block is 1, the speed won't change a lot even if the IO speed is enabled.
- **Link**: If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. The DMAC will stop the data transfer after transferring the package; otherwise, the value of the link is considered as the descriptor address of the next package.

Figure 2-13 DMA Chain Transfer



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2.6.3.5 Interrupts

There are four kinds of DMA interrupts: the half package interrupt, package end interrupt, and queue end interrupt.

- Half package interrupt

When enabled, the DMAC sends out a half package interrupt after transferring half of a package.

- Package end interrupt

When enabled, the DMAC sends out a package end interrupt after transferring a complete package.

- Queue end interrupt

When enabled, the DMAC sends out a queue end interrupt after transferring a complete queue.

- Timeout interrupt

When TIMEOUT is enabled, DMA will generate a timeout interrupt after timeout.

Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts are generated very closely, the later interrupt may override the former one. That is, from the perspective of the CPU, the DMAC has only a system interrupt source.

2.6.3.6 Clock Gating

The DMA_CLK_GATE module is a hardware module for controlling the clock gating automatically. It provides clock sources for sub-modules in DMAC and the module local circuits.

The DMA_CLK_GATE module consists of two parts: the channel clock gate and the common clock gate.

Channel clock gate: Controls the DMA clock of the DMA channels. When the system accesses the register of the current DMA channel and the DMA channel is enabled, the channel clock gate automatically opens the DMA clock. With a 16-HCLK-cycle delay after the system finishes accessing the register or the DMA data transfer is completed, the channel clock gate automatically closes the DMA clock. Also, the clock for the related circuits, such as for the channel control and FIFO control modules, will be closed.

Common clock gate: Controls the clocks of the DMA common circuits. The common circuits include the common circuit of the FIFO control module, MPORT module, and MBUS. When all the DMA channels are disabled, the common clock gate automatically closes the clocks for the above circuits.

The DMA clock gating can support all the functions stated above or not by software.

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2.6.3.7 Transfer Mode

The peripherals initiate data transfer by transmitting DMA request signals to the DMAC. After receiving the request signal, the DMAC converts it to the internal DRQ signal and controls the DMA data transfer.

The DMAC supports two data transfer modes: the waiting mode and handshake mode.

The principle of waiting mode

- When the DMAC detects a valid external request signal, the DMAC starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ pulls low automatically.
- The internal DRQ holds low for certain clock cycles (WAIT_CYC), and then the DMAC restarts to detect the external requests. If the external request signal is valid, then the next transfer starts.

The principle of handshake mode

- When the DMAC detects a valid external request signal, the DMAC starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ will be pulled down automatically. For the last data transfer of the block, the DMAC sends a DMA Last signal with the DMA commands to the peripheral device. The DMA Last signal will be packed as part of the DMA commands and transmitted on the bus. It is used to inform the peripheral device that it is the end of the data transfer for the current DRQ.
- When the peripheral device receives the DMA Last signal, it can judge that the data transfer for the current DRQ is finished. To continue the data transfer, it sends a DMA Active signal to the DMAC.

NOTE

One DMA Active signal will be converted to one DRQ signal in the DMA module. To generate multiple DRQs, the peripheral device needs to send out multiple DMA Active signals via the bus protocol.

- When the DMAC received the DMA Active signal, it sends back a DMA ACK signal to the peripheral device.
- When the peripheral device receives the DMA ACK signal, it waits for all the operations on the local device completed, and both the FIFO and DRQ status refreshed. Then it invalidates the DMA Active signal.

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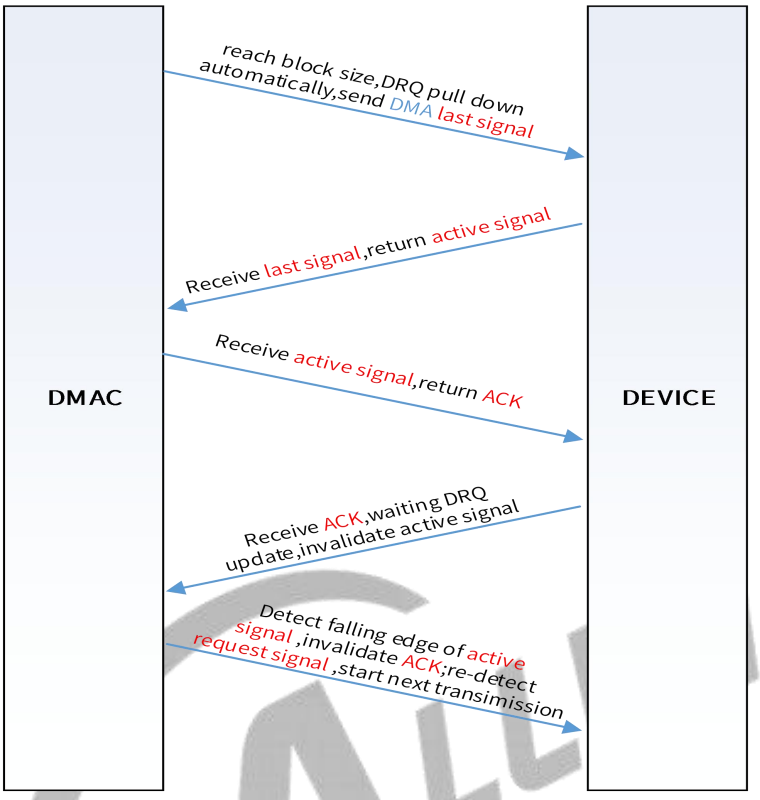
- When the DMAC detects the falling edge of the DMA Active signal, it invalidates the corresponding DMA ACK signal, and restarts to detect the external request signals. If a valid request signal is detected, the next data transfer starts.

The following figure shows the workflow of the handshake mode.

Figure 2-14 Workflow of the DMAC Handshake Mode



2.6.3.8 Address Auto-Alignment

For the non-IO devices whose start address is not 32-byte-aligned, the DMAC will adjust the address to 32-byte-aligned through the burst transfer within 32 bytes. Adjusting address to 32-byte-aligned improves the DRAM access efficiency.

The following example shows how the DMAC adjusts the address: when the peripheral device of a DMA channel is a non-IO device whose start address is 0x86 (not 32-byte-aligned), the DMAC firstly uses a 26-byte burst transfer to align the address to 0xA0 (32-byte-aligned), and then transfers data by 64-byte burst (the maximum transfer amount that MBUS allows).

The IO devices do not support address alignment, so the bit width of IO devices must match the address offset; otherwise, the DMAC will ignore the inconsistency and directly transmit data of the corresponding bit width to the address.

The address of the DMA descriptor does not support the address auto-alignment. Make sure the address is word-aligned; otherwise the DMAC cannot identify the descriptor.

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2.6.3.9 DMAC Clock Control

- The DMAC clock is synchronous with the AHB clock. Make sure that the DMAC gating bit of AHB clock is enabled before accessing the DMAC register.
- The reset input signal of the DMAC is asynchronous with AHB and is low valid by default. Make sure that the reset signal of the DMAC is de-asserted before accessing the DMA register.
- To avoid the indefinite state within registers, de-assert the reset signal first, and then open the gating bit of AHB.
- The DMAC supports Clock Auto Gating function to reduce power consumption, the system will automatically disable the DMAC clock in the DMAC idle state. Clock Auto Gating is enabled by default.

2.6.4 Programming Guidelines

2.6.4.1 Using DMAC Transfer Process

The DMAC transfer process is as follows.

Step 1 Configure DMAC_IRQ_CPU_EN_REG register and DMAC_IRQ_MCU_EN_REG register to select whether the channel interrupt siganl is transferred to CPU field or MCU field. If both of the two registers are not configured, the IRQ will be transferred to both CPU field and MCU field by default.

Step 2 Request DMA channel, and check if the DMA channel is idle by checking if it is enabled. A disabled channel indicates it is idle, while an enabled channel indicates it is busy.

Step 3 Write the descriptor with 6 words into the memory. The descriptor must be word-aligned. For more details, refer to section 2.6.3.4 DMA Descriptor.

Step 4 Write the start address of the descriptor to DMAC_DESC_ADDR_REG.

Step 5 Enable the DMA channel, and write the corresponding channel to DMAC_EN_REG.

Step 6 The DMA obtains the descriptor information.

Step 7 Start to transmit a package. When half of the package is completed, the DMA sends a Half Package Transfer Interrupt; when a total package is completed, the DMA sends a Package End Transfer Interrupt. This interrupt status can be read by DMAC_IRQ_PEND_REG0.

Step 8 Set DMAC_PAU_REG to pause or resume the data transfer.

Step 9 After completing a total package transfer, the DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; otherwise, the next package starts to transmit. When the transfer ends, the DMA sends a Queue End Transfer Interrupt.

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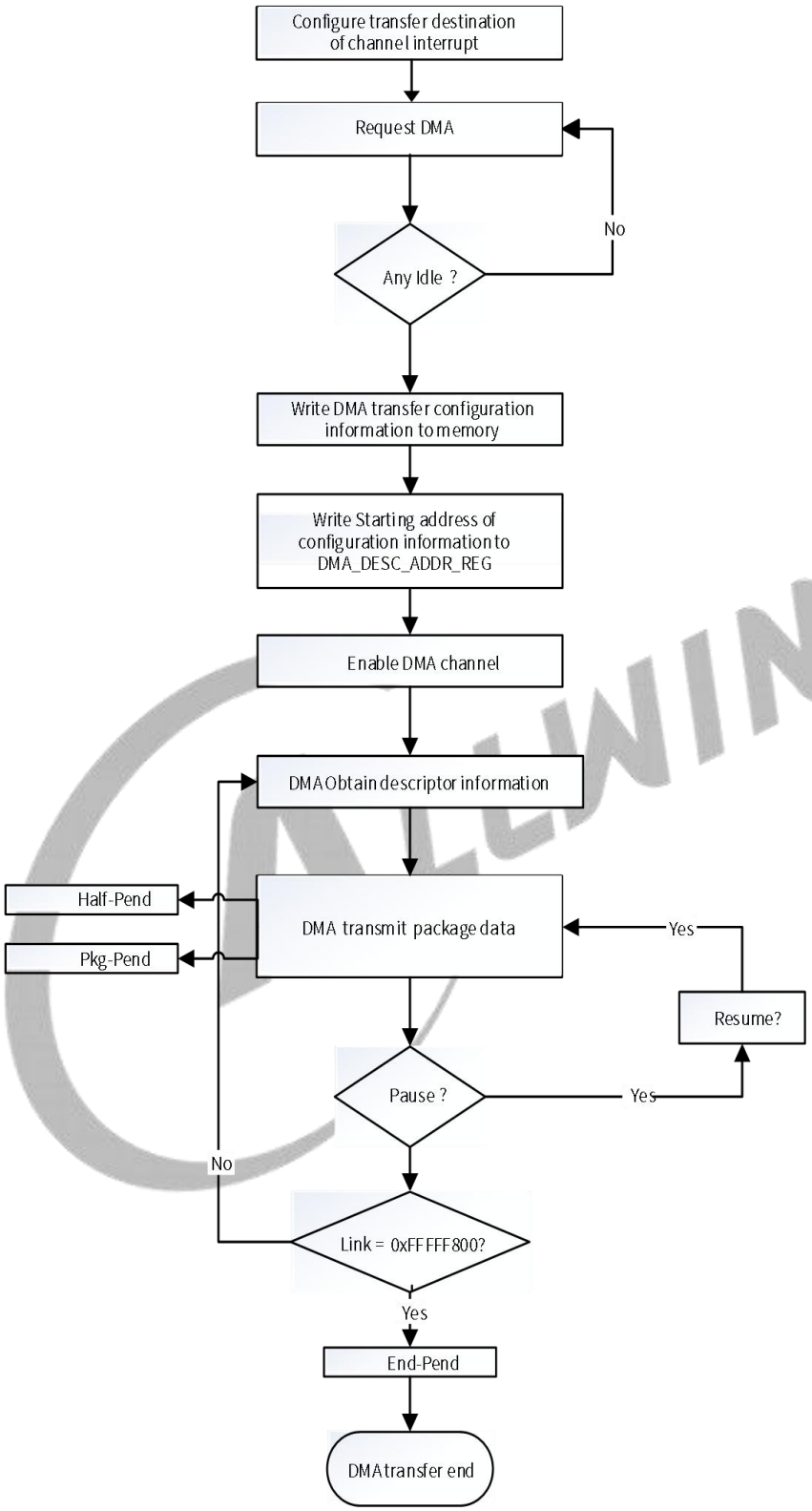
Step 10 Disable the DMA channel.

Figure 2-15 DMAC Transfer Process



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2.6.4.2 Processing DMAC Interrupt

Follow the steps below to process the DMAC interrupt:

Step 1 Enable interrupt: write the corresponding interrupt enable bit of DMAC_IRQ_EN_REG0. The system generates an interrupt when the corresponding condition is satisfied.

Step 2 After entering the interrupt process, write to clear the interrupt pending and execute the process of waiting for the interrupt.

Step 3 Resume the interrupt and continue to execute the interrupted process.

2.6.4.3 Configuring DMAC

To configure the DMAC, follow the guidelines below:

- Make sure the transfer bit width of IO devices is consistent with the offset of the start address.
- The MBUS protocol does not support the read operation of non-integer words. For the devices whose bit width is not word-aligned, after receiving the read command, they should resolve the read command according to their FIFO bit width instead of the command bit width, and ignore the redundant data caused by the inconsistency of the bit width.
- When the DMA transfer is paused, this is equivalent to invalid DRQ. Because there is a certain time delay between DMA transfer commands, the DMAC will not stop data transfer until the DMAC finishes processing the current command and the commands in Arbiter (at most 128 bytes' data).
- IOspeed and BMODE cannot be enabled at the same time.
- As DMA will transmit interrupts to DMAC_IRQ_CPU_EN_REG and DMAC_IRQ_MCU_EN_REG by default simultaneously, it should be configured which one receives interrupts before transmission, and the other one ought to be disabled.
- Timeout Programming Instruction
  - Similar to the register configuration of other channels, configure by descriptors and read through registers.
  - Enable BMODE before using TIMEOUT functions.
  - Before enabling TIMEOUT functions, if the source device configures the descriptor Config [7:6] as 0, set the DMAC_MODE_REG [4] as 1, and then start the DMA transfer.
  - After enabling the pause function of TIMEOUT, resume the data transfer by configuring the DMAC_PAU_REG.
  - After enabling the stop function of TIMEOUT, when TIMEOUT generates an interrupt, DMA will not generate the interrupt end signal of package and write-back. To restart the channel, configure the descriptors again.

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- After enabling the jump function of TIMEOUT, when TIMEOUT generates an interrupt, DMA will not generate the interrupt end signal of package and write-back but skip to the next descriptor. Whether to start the TIMEOUT functions is decided by the descriptor being executed at that time. If there is no descriptor, transmission ends.
- The entered count number= the time to be counted * clock frequency (DMA clock frequency)/4096
- Take an example of 200MHz clock frequency for DMA. If the step size of timer is 20.48 us, and the maximum count is 511, the longest counting time will be the maximum count*step size=10.46 ms, and the shortest counting time will be 1*step size=20.48 us.

DMAC application example:

```
writel(0x00000000, mem_address + 0x00);  //Set configurations. The mem_address must be word-aligned.
writel (0x00001000, mem_address + 0x04);    // Set the start address for the source device.
writel (0x20000000, mem_address + 0x08);  //Set the start address for the destination device.
writel (0x00000020, mem_address + 0x0C);  // Set the data package size.
writel (0x00000000, mem_address + 0x10);  //Set the parameters.
writel (0xFFFFF800, mem_address + 0x14);  //Set the start address for the next descriptor.
writel (mem_address, 0x03002000+ 0x100 + 0x08); //Set the start address for the DMA channel0 descriptor.
do {
If (mem_address == readl (0x03002000+ 0x100 + 0x08));
break;
} while (1);                  //Make sure that the writing operation is valid.
writel (0x000000001, 0x03002000+ 0x100 + 0x00);      // Enable DMA channel0 transfer.
```

The DMAC supports increasing data package in transfer, pay attention to the following points:

- The 0xFFFFF800 value of DMAC_FDESC_ADDR_REG indicates that the DMA channel has got back the descriptor of the last package. The DMA channel will automatically stop the data transfer after transferring the current package.
- To add a package during the data transfer, check if the DMA channel has got back the descriptor of the last package. If yes, you cannot add any package in the current queue. Request another DMA channel with a new DRQ to transfer the package. Otherwise, you can add the package by modifying the DMAC_FDESC_ADDR_REG of the last package from 0xFFFFF800 to the start address of the to-be-added package.

  To ensure that the modification is valid, read the value of DMAC_FDESC_ADDR_REG after the modification. The value 0xFFFFF800 indicates the modification fails and the other values indicate you have successfully added packages to the queue.

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Another problem is, the system needs some time to process the modification, during which the DMA channel may get back the descriptor of the last package. You can read DMAC_CUR_SRC_REG and DMAC_CUR_DEST_REG and check if the increasing memory address accords with the information of the added package. If yes, the package is added successfully; otherwise, the modification failed.

To ensure a higher rate of success, it is suggested that you add the package before the half package interrupt of the penultimate package.

2.6.5 Register List

Module Name	Base Address	Comments
DMAC	0x0300 2000	
MCU_DMAC	0x0712 1000	MCU_DMAC register is the same with DMAC

Register Name	Offset	Description
DMAC_IRQ_EN_REG0	0x0000	DMAC IRQ Enable Register 0
DMAC_IRQ_EN_REG1	0x0004	DMAC IRQ Enable Register 1
DMAC_IRQ_PEND_REG0	0x0010	DMAC IRQ Pending Status Register 0
DMAC_IRQ_PEND_REG1	0x0014	DMAC IRQ Pending Status Register 1
DMAC_SEC_REG	0x0020	DMAC Security Register
DMAC_AUTO_GATE_REG	0x0028	DMAC Auto Gating Register
DMAC_STA_REG	0x0030	DMAC Status Register
DMAC_IRQ_CPU_EN_REG	0x0034	DMAC IRQ Transfer to CPU Field Enable Register
DMAC_IRQ_MCU_EN_REG	0x0038	DMAC IRQ Transfer to MCU Field Enable Register
DMAC_EN_REG	0x0100+N*0x0040 (N=0-15)	DMAC Channel Enable Register
DMAC_PAU_REG	0x0104+N*0x0040 (N=0-15)	DMAC Channel Pause Register
DMAC_DESC_ADDR_REG	0x0108+N*0x0040 (N=0-15)	DMAC Channel Descriptor Address Register
DMAC_CFG_REG	0x010C+N*0x0040 (N=0-15)	DMAC Channel Configuration Register
DMAC_CUR_SRC_REG	0x0110+N*0x0040 (N=0-15)	DMAC Channel Current Source Address Register
DMAC_CUR_DEST_REG	0x0114+N*0x0040 (N=0-15)	DMAC Channel Current Destination Address Register
DMAC_BCNT_LEFT_REG	0x0118+N*0x0040 (N=0-15)	DMAC Channel Byte Counter Left Register
DMAC_PARA_REG	0x011C+N*0x0040 (N=0-15)	DMAC Channel Parameter Register

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Register Name	Offset	Description
DMAC_MODE_REG	0x0128+N*0x0040 (N=0-15)	DMAC Mode Register
DMAC_FDESC_ADDR_REG	0x012C+N*0x0040 (N=0-15)	DMAC Former Descriptor Address Register
DMAC_PKG_NUM_REG	0x0130+N*0x0040 (N=0-15)	DMAC Package Number Register

2.6.6 Register Description

2.6.6.1 0x0000 DMAC IRQ Enable Register 0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA7_TIMEOUT_IRQ_EN DMA 7 Timeout Interrupt Enable. 0: Disable 1: Enable
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	R/W	0x0	DMA6_TIMEOUT_IRQ_EN DMA 6 Timeout Interrupt Enable. 0: Disable 1: Enable
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN

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Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
			DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	R/W	0x0	DMA5_TIMEOUT_IRQ_EN DMA 5 Timeout Interrupt Enable. 0: Disable 1: Enable
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	R/W	0x0	DMA4_TIMEOUT_IRQ_EN DMA 4 Timeout Interrupt Enable. 0: Disable 1: Enable
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	R/W	0x0	DMA3_TIMEOUT_IRQ_EN DMA 3 Timeout Interrupt Enable. 0: Disable 1: Enable
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable.

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Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	R/W	0x0	DMA2_TIMEOUT_IRQ_EN DMA 2 Timeout Interrupt Enable. 0: Disable 1: Enable
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	R/W	0x0	DMA1_TIMEOUT_IRQ_EN DMA 1 Timeout Interrupt Enable. 0: Disable 1: Enable
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable

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Offset: 0x0000			Register Name: DMAC_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
			1: Enable
3	R/W	0x0	DMA0_TIMEOUT_IRQ_EN DMA 0 Timeout Interrupt Enable. 0: Disable 1: Enable
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

2.6.6.2 0x0004 DMAC IRQ Enable Register 1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA15_TIMEOUT_IRQ_EN DMA 15 Timeout Interrupt Enable. 0: Disable 1: Enable
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	R/W	0x0	DMA14_TIMEOUT_IRQ_EN DMA 14 Timeout Interrupt Enable. 0: Disable

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Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
			1: Enable
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	R/W	0x0	DMA13_TIMEOUT_IRQ_EN DMA 13 Timeout Interrupt Enable. 0: Disable 1: Enable
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	R/W	0x0	DMA12_TIMEOUT_IRQ_EN DMA 12 Timeout Interrupt Enable. 0: Disable 1: Enable
18	R/W	0x0	DMA12_QUEUE_IRQ_EN DMA 12 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable 1: Enable

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Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	R/W	0x0	DMA11_TIMEOUT_IRQ_EN DMA 11 Timeout Interrupt Enable. 0: Disable 1: Enable
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	R/W	0x0	DMA10_TIMEOUT_IRQ_EN DMA 10 Timeout Interrupt Enable. 0: Disable 1: Enable
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	R/W	0x0	DMA9_TIMEOUT_IRQ_EN DMA 9 Timeout Interrupt Enable. 0: Disable 1: Enable
6	R/W	0x0	DMA9_QUEUE_IRQ_EN

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Offset: 0x0004			Register Name: DMAC_IRQ_EN_REG1
Bit	Read/Write	Default/Hex	Description
			DMA9 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA9 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA9 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	R/W	0x0	DMA8_TIMEOUT_IRQ_EN DMA 8 Timeout Interrupt Enable. 0: Disable 1: Enable
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

2.6.6.3 0x0010 DMAC IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMA7_TIMEOUT_IRQ_PEND DMA 7 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	R/W1C	0x0	DMA6_TIMEOUT_IRQ_PEND DMA 6 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	R/W1C	0x0	DMA5_TIMEOUT_IRQ_PEND DMA 5 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it.

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
			0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	R/W1C	0x0	DMA4_TIMEOUT_IRQ_PEND DMA 4 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	R/W1C	0x0	DMA3_TIMEOUT_IRQ_PEND DMA 3 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
			bit will clear it. 0: No effect 1: Pending
11	R/W1C	0x0	DMA2_TIMEOUT_IRQ_PEND DMA 2 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	R/W1C	0x0	DMA1_TIMEOUT_IRQ_PEND DMA 1 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0010			Register Name: DMAC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
3	R/W1C	0x0	DMA0_TIMEOUT_IRQ_PEND DMA 0 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

2.6.6.4 0x0014 DMAC IRQ Pending Status Register 1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMA15_TIMEOUT_IRQ_PEND DMA 15 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND. DMA 15 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_PEND DMA 15 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Set 1 to the

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
			bit will clear it. 0: No effect 1: Pending
27	R/W1C	0x0	DMA14_TIMEOUT_IRQ_PEND DMA 14 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_PEND DMA 14 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	R/W1C	0x0	DMA13_TIMEOUT_IRQ_PEND DMA 13 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA13_PKG_IRQ_PEND DMA 13 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND. DMA 13 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it.

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
			0: No effect 1: Pending
19	R/W1C	0x0	DMA12_TIMEOUT_IRQ_PEND DMA 12 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_PEND DMA 12 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	R/W1C	0x0	DMA11_TIMEOUT_IRQ_PEND DMA 11 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
11	R/W1C	0x0	DMA10_TIMEOUT_IRQ_PEND DMA 10 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_PEND DMA 10 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	R/W1C	0x0	DMA9_TIMEOUT_IRQ_PEND DMA 9 Timeout Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_PEND DMA 9 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	R/W1C	0x0	DMA8_TIMEOUT_IRQ_PEND DMA 8 Timeout Interrupt Pending. Set 1 to the bit will clear it.

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Offset: 0x0014			Register Name: DMAC_IRQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
			0: No effect 1: Pending
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA8 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_PEND DMA 8 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA8 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

2.6.6.5 0x0020 DMAC Security Register (Default Value: 0x0000_FFFF)

Offset: 0x0020			Register Name: DMAC_SEC_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_SEC DMA channel 15 security. 0: Secure, 1: Non-secure.
14	R/W	0x1	DMA14_SEC DMA channel 14 security. 0: Secure, 1: Non-secure.
13	R/W	0x1	DMA13_SEC DMA channel 13 security. 0: Secure, 1: Non-secure.
12	R/W	0x1	DMA12_SEC DMA channel 12 security. 0: Secure, 1: Non-secure.
11	R/W	0x1	DMA11_SEC DMA channel 11 security.

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Offset: 0x0020			Register Name: DMAC_SEC_REG
Bit	Read/Write	Default/Hex	Description
			0: Secure, 1: Non-secure.
10	R/W	0x1	DMA10_SEC DMA channel 10 security. 0: Secure, 1: Non-secure.
9	R/W	0x1	DMA9_SEC DMA channel 9 security. 0: Secure, 1: Non-secure.
8	R/W	0x1	DMA8_SEC DMA channel 8 security. 0: Secure, 1: Non-secure.
7	R/W	0x1	DMA7_SEC DMA channel 7 security. 0: Secure, 1: Non-secure.
6	R/W	0x1	DMA6_SEC DMA channel 6 security. 0: Secure, 1: Non-secure.
5	R/W	0x1	DMA5_SEC DMA channel 5 security. 0: Secure, 1: Non-secure.
4	R/W	0x1	DMA4_SEC DMA channel 4 security. 0: Secure, 1: Non-secure.
3	R/W	0x1	DMA3_SEC DMA channel 3 security. 0: Secure, 1: Non-secure.
2	R/W	0x1	DMA2_SEC DMA channel 2 security. 0: Secure, 1: Non-secure.
1	R/W	0x1	DMA1_SEC DMA channel 1 security. 0: Secure,

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Offset: 0x0020			Register Name: DMAC_SEC_REG
Bit	Read/Write	Default/Hex	Description
			1: Non-secure.
0	R/W	0x1	DMA0_SEC DMA channel 0 security. 0: Secure, 1: Non-secure.

2.6.6.6 0x0028 DMAC Auto Gating Register (Default Value: 0x00000000)

Offset: 0x0028			Register Name: DMAC_AUTO_GATE_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, bit-2 should be set up.

2.6.6.7 0x0030 DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: DMAC_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0	MBUS_FIFO_STATUS MBUS FIFO Status 0: Empty 1: Not Empty
30:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status.

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Offset: 0x0030			Register Name: DMAC_STA_REG
Bit	Read/Write	Default/Hex	Description
			0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle

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Offset: 0x0030			Register Name: DMAC_STA_REG
Bit	Read/Write	Default/Hex	Description
			1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle 1: Busy

2.6.6.8 0x0034 DMAC IRQ Transfer to CPU Field Enable Register (Default Value: 0x0000_FFFF)

Offset: 0x0034			Register Name: DMAC_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_IRQ_CPU_EN Control whether the DMA Channel 15 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
14	R/W	0x1	DMA14_IRQ_CPU_EN Control whether the DMA Channel 14 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
13	R/W	0x1	DMA13_IRQ_CPU_EN Control whether the DMA Channel 13 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field

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Offset: 0x0034			Register Name: DMAC_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: can transfer to CPU field
12	R/W	0x1	DMA12_IRQ_CPU_EN Control whether the DMA Channel 12 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
11	R/W	0x1	DMA11_IRQ_CPU_EN Control whether the DMA Channel 11 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
10	R/W	0x1	DMA10_IRQ_CPU_EN Control whether the DMA Channel 10 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
9	R/W	0x1	DMA9_IRQ_CPU_EN Control whether the DMA Channel 9 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
8	R/W	0x1	DMA8_IRQ_CPU_EN Control whether the DMA Channel 8 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
7	R/W	0x1	DMA7_IRQ_CPU_EN Control whether the DMA Channel 7 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
6	R/W	0x1	DMA6_IRQ_CPU_EN Control whether the DMA Channel 6 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
5	R/W	0x1	DMA5_IRQ_CPU_EN Control whether the DMA Channel 5 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field

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Offset: 0x0034			Register Name: DMAC_IRQ_CPU_EN_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x1	DMA4_IRQ_CPU_EN Control whether the DMA Channel 4 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
3	R/W	0x1	DMA3_IRQ_CPU_EN Control whether the DMA Channel 3 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
2	R/W	0x1	DMA2_IRQ_CPU_EN Control whether the DMA Channel 2 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
1	R/W	0x1	DMA1_IRQ_CPU_EN Control whether the DMA Channel 1 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field
0	R/W	0x1	DMA0_IRQ_CPU_EN Control whether the DMA Channel 0 IRQ signal can transfer to CPU field or not. 0: can not transfer to CPU field 1: can transfer to CPU field

2.6.6.9 0x0038 DMAC IRQ Transfer to MCU Field Enable Register (Default Value: 0x0000_FFFF)

Offset: 0x0038			Register Name: DMAC_IRQ_MCU_EN_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x1	DMA15_IRQ_MCU_EN Control whether the DMA Channel 15 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
14	R/W	0x1	DMA14_IRQ_MCU_EN Control whether the DMA Channel 14 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field

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Offset: 0x0038			Register Name: DMAC_IRQ_MCU_EN_REG
Bit	Read/Write	Default/Hex	Description
13	R/W	0x1	DMA13_IRQ_MCU_EN Control whether the DMA Channel 13 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
12	R/W	0x1	DMA12_IRQ_MCU_EN Control whether the DMA Channel 12 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
11	R/W	0x1	DMA11_IRQ_MCU_EN Control whether the DMA Channel 11 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
10	R/W	0x1	DMA10_IRQ_MCU_EN Control whether the DMA Channel 10 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
9	R/W	0x1	DMA9_IRQ_MCU_EN Control whether the DMA Channel 9 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
8	R/W	0x1	DMA8_IRQ_MCU_EN Control whether the DMA Channel 8 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
7	R/W	0x1	DMA7_IRQ_MCU_EN Control whether the DMA Channel 7 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
6	R/W	0x1	DMA6_IRQ_MCU_EN Control whether the DMA Channel 6 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
5	R/W	0x1	DMA5_IRQ_MCU_EN

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Offset: 0x0038			Register Name: DMAC_IRQ_MCU_EN_REG
Bit	Read/Write	Default/Hex	Description
			Control whether the DMA Channel 5 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
4	R/W	0x1	DMA4_IRQ_MCU_EN Control whether the DMA Channel 4 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
3	R/W	0x1	DMA3_IRQ_MCU_EN Control whether the DMA Channel 3 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
2	R/W	0x1	DMA2_IRQ_MCU_EN Control whether the DMA Channel 2 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
1	R/W	0x1	DMA1_IRQ_MCU_EN Control whether the DMA Channel 1 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field
0	R/W	0x1	DMA0_IRQ_MCU_EN Control whether the DMA Channel 0 IRQ signal can transfer to MCU field or not. 0: can not transfer to MCU field 1: can transfer to MCU field

2.6.6.10 0x0100+N*0x0040 (N=0-15) DMAC Channel Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0040 (N=0-15)			Register Name: DMAC_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

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2.6.6.11 0x0104+N*0x0040 (N=0-15) DMAC Channel Pause Register (Default Value: 0x0000_0000)

Offset: 0x0104+N*0x0040 (N=0-15)			Register Name: DMAC_PAU_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

2.6.6.12 0x0108+N*0x0040 (N=0-15) DMAC Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x0108+N*0x0040 (N=0-15)			Register Name: DMAC_DESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	DMA_DESC_LOW_ADDR DMA Channel Descriptor Word Address, Low 30bits. The Descriptor Address must be word-aligned.
1:0	R/W	0x0	DMA_DESC_HIGH_ADDR DMA Channel Descriptor High Address, High 2bits The real address is as below: DMA Channel Descriptor Address = {bit[1:0],bit[31:2],2'b00};

2.6.6.13 0x010C+N*0x0040 (N=0-15) DMAC Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x010C+N*0x0040 (N=0-15)			Register Name: DMAC_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R	0x0	BMODE_SEL Mode select 0: Normal Mode 1: BMODE
29:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: Reserved

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Offset: 0x010C+N*0x0040 (N=0-15)			Register Name: DMAC_CFG_REG
Bit	Read/Write	Default/Hex	Description
24	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: Reserved
8	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

2.6.6.14 0x0110+N*0x0040 (N=0-15) DMAC Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x0040 (N=0-15)			Register Name: DMAC_CUR_SRC_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_SRC.

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Offset: 0x0110+N*0x0040 (N=0-15)			Register Name: DMAC_CUR_SRC_REG
Bit	Read/Write	Default/Hex	Description
			DMA Channel Current Source Address, read only.

2.6.6.15 0x0114+N*0x0040 (N=0-15) DMAC Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset: 0x0114+N*0x0040 (N=0-15)			Register Name: DMAC_CUR_DEST_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

2.6.6.16 0x0118+N*0x0040 (N=0-15) DMAC Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset: 0x0118+N*0x0040 (N=0-15)			Register Name: DMAC_BCNT_LEFT_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

2.6.6.17 0x011C+N*0x0040 (N=0-15) DMAC Channel Parameter Register (Default Value: 0x0000_0000)

NOTE

- The entered count number (bit [28:20], this number needs to be integer) = the time to be counted * clock frequency (DMA clock frequency)/4096
- Take an example of 200MHz clock frequency for DMAC. If the step size of timer is 20.48 us, the longest counting time will be the maximum count*step size=10.46 ms.

Offset: 0x011C+N*0x0040 (N=0-15)			Register Name: DMAC_PARA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_TO_EN. Timeout Function Enable Bit 1: Enable 0：Disable
30:29	R	0x0	DMA_TO_FUN. Timeout Function Configuration 01: Enabling pause channel transfer function after timeout

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Offset: 0x011C+N*0x0040 (N=0-15)			Register Name: DMAC_PARA_REG
Bit	Read/Write	Default/Hex	Description
			10: Enabling stop channel transfer function after timeout 11: Enabling jump next opcode function after timeout
28:20	R	0x0	DMA_TO_WAIT_CYC. The time cycle of waiting the start device to restart transferring data.
19:18	R	0x0	DMA Channel Current Destination Address[33:32], Read only.
17:16	R	0x0	DMA Channel Current Source Address[33:32], read only.
15:9	/	/	/
8	R	0x0	DMA_IOSPEED_EN. Accelerating DMA speed when transferring the data of IO device 1: Enable 0: Disable
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

2.6.6.18 0x0128+N*0x0040 (N=0-15) DMAC Mode Register (Default Value: 0x0000_0000)

Offset: 0x0128+N*0x0040 (N=0-15)			Register Name: DMAC_MODE_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	LAG_TIME_MODE In wait mode, enabling this bit, DMA will not timing wait cycle until DMA receive or transmit data successfully. It's recommend to enable this bit before using DMA when the DMA has enable more than one channel which access IO and memory equipment. 0: disable 1: enable
4	R/W	0x0	DMA_BLOCK_ZERO_EN Enable pre-read source DRQ when source block is configured 0. It needs to disable when opening timeout sub function (DMA Channel Parameter Register [30:29] =01, 10 or 11) and source block is configured 0. 0: enable 1: disable
3	R/W	0x0	DMA_DST_MODE. Destination communication Mode Select 0: Wait mode. 1: Handshake mode.

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Offset: 0x0128+N*0x0040 (N=0-15)			Register Name: DMAC_MODE_REG
Bit	R/W	Default/Hex	Description
2	R/W	0x0	DMA_SRC_MODE. Source communication Mode Select 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

2.6.6.19 0x012C+N*0x0040 (N=0-15) DMAC Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset: 0x012C+N*0x0040 (N=0-15)			Register Name: DMAC_FDESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to storing the former value of DMA Channel Descriptor Address Register.

2.6.6.20 0x0130+N*0x0040 (N=0-15) DMAC Package Number Register (Default Value: 0x0000_0000)

Offset: 0x0130+N*0x0040 (N=0-15)			Register Name: DMAC_PKG_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

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2.7 Generic Interrupt Controller (GIC)

2.7.1 Overview

The GIC-600 is a generic interrupt controller that handles interrupts from peripherals to the cores and interrupts between cores. The GIC-600 supports a distributed microarchitecture containing several individual blocks that are used to provide a flexible GIC implementation.

All the GIC-600 blocks communicate through fully credited AXI4-Stream interface channels. This means that the interface exerts transient backpressure only on their ic<xy>tready signals, enabling packets to be routed over any free-flowing interconnect. Channels can be routed over dedicated AXI4-Stream buses, or over any available free-flowing transport layer in the system. A channel is described as free-flowing if all transactions on that channel complete without a non-transient dependency on any other transaction.

The GIC-600 includes build scripts that can create appropriate levels of hierarchy for any particular configuration. In small configurations, the distribution can be hidden and internally optimized.

the GIC has the following features:

- Interrupt services and masking:
  - Supports the following interrupt types:
    - Up to 56000 LPIs. A peripheral generates these interrupts by writing to a memory-mapped register in the GIC-600.
    - Up to 960 SPIs in groups of 32.
    - Up to 16 PPIs that are independent for each core and can be programmed to support either edge triggered or level-sensitive interrupts.
    - Up to 16 SGIs that are generated through the GIC CPU interface of a core.
  - Up to 16 ITS modules that provide device isolation and ID translation for message-based interrupts and enable virtual machines to program devices directly.
  - Interrupt masking and prioritization with 32 priority levels, five bits per interrupt.
- Registers and programming
  - Flexible affinity routing, using the Multiprocessor Identification Register (MPIDR) addresses, including support for all four affinity levels.
  - Single ACE-Lite slave port on each chip for programming of all GIC Distributor (GICD) registers, GIC Interrupt Translation Service (GITS) registers, and GIC Redistributor (GICR) registers. Each ITS has an optional ACE-Lite slave port for programming the GITS_TRANSLATER register.
  - Coherent view of SPI register data across multiple chips.

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- Security
  - A global Disable Security (DS) bit. This bit enables support for systems without security.
  - The following interrupt groups allow interrupts to target different exception levels:
    - Group 0.
    - Non-secure Group 1.
    - Secure Group 1.
- Performance Monitoring Unit (PMU) counters with snapshot functionality.
- Error correction: ARMv8.2 Reliability Accessibility Serviceability (RAS) architecture-compliant error reporting for the following:
  - Software access errors
  - ITS command and translation errors
  - Error Correcting Code (ECC) errors

2.7.2 Functional Description

the following table describes the details of interrupt sources:

Table 2-15 Interrupt Source in CPUX Domain

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	CPUX_MSGBOX_R	0x0080	CPUX MSGBOX read IRQ for CPUX
33	CPUS _MSGBOX_W	0x0084	CPUS MSGBOX write IRQ for CPUX
34	UART0	0x0088	
35	UART1	0x008C	
36	UART2	0x0090	
37	UART3	0x0094	
38	UART4	0x0098	
39	UART5	0x009C	
40	UART6	0x00A0	
41	UART7	0x00A4	
42	TWI0	0x00A8	
43	TWI1	0x00AC	
44	TWI2	0x00B0	
45	TWI3	0x00B4	
46	TWI4	0x00B8	
47	TWI5	0x00BC	
48	SPI0	0x00C0	
49	SPI1	0x00C4	
50	SPI2	0x00C8	
51	PWMCTRL0	0x00CC	
52	SPIFC	0x00D0	
53		0x00D4	
54		0x00D8	
55		0x00DC	
56		0x00E0	
57		0x00E4	
58	CIR_TX	0x00E8	
59	CIR_RX	0x00EC	
60	LEDC	0x00F0	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
61	USB0_DEVICE	0x00F4	
62	USB0_EHCI	0x00F8	
63	USB0_OHCI	0x00FC	
64	USB1_EHCI	0x0100	
65	USB1_OHCI	0x0104	
66		0x0108	
67	USB2/USB3	0x010C	
68		0x0110	
69		0x0114	
70	NDFC	0x0118	
71	THS0	0x011C	
72	SMHC0	0x0120	
73	SMHC1	0x0124	
74	SMHC2	0x0128	
75	NSI	0x012C	
76	SMC	0x0130	
77		0x0134	
78	GMAC	0x0138	
79		0x013C	
80	CCU_FERR	0x0140	
81	AHB_HREADY_TIME_OUT	0x0144	
82	DMAC_CPUX_NS	0x0148	DMAC channel 0-15 non-secure interrupt
83	DMAC_ CPUX_S	0x014C	DMAC channel 0-15 secure interrupt
84	CE_NS	0x0150	
85	CE_S	0x0154	
86	SPINLOCK	0x0158	
87	CPUX_TIMER0	0x015C	
88	CPUX_TIMER1	0x0160	
89	CPUX_TIMER2	0x0164	
90	CPUX_TIMER3	0x0168	
91	CPUX_TIMER4	0x016C	
92	CPUX_TIMER5	0x0170	
93	GPADC	0x0174	
94	THS1	0x0178	
95	CPUX_WDT	0x017C	
96		0x0180	
97	IOMMU	0x0184	
98	LRADC	0x0188	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
99	GPIOA_NS	0x018C	
100	GPIOA_S	0x0190	
101	GPIOB_NS	0x0194	
102	GPIOB_S	0x0198	
103	GPIOC_NS	0x019C	
104	GPIOC_S	0x01A0	
105	GPIOD_NS	0x01A4	
106	GPIOD_S	0x01A8	
107	GPIOE_NS	0x01AC	
108	GPIOE_S	0x01B0	
109	GPIOF_NS	0x01B4	
110	GPIOF_S	0x01B8	
111	GPIOG_NS	0x01BC	
112	GPIOG_S	0x01C0	
113	GPIOH_NS	0x01C4	
114	GPIOH_S	0x01C8	
115		0x01CC	
116		0x01D0	
117		0x01D4	
118		0x01D8	
119	DE	0x01DC	
120	DI	0x01E0	
121		0x01E4	
122	TCON_LCD0	0x01E8	
123		0x01EC	
124	TCON_LCD1	0x01F0	
125		0x01F4	
126	DSI0	0x01F8	
127	DSI1	0x01FC	
128	TCON_TV1	0x0200	
129		0x0204	
130	PCIE_EDMA[0]	0x0208	
131	PCIE_EDMA[1]	0x020C	
132	PCIE_EDMA[2]	0x0210	
133	PCIE_EDMA[0]	0x0214	
134	PCIE_EDMA[4]	0x0218	
135	PCIE_EDMA[5]	0x021C	
136	PCIE_EDMA[6]	0x0220	
137	PCIE_EDMA[7]	0x0224	
138	PCIE_SII	0x0228	
139	PCIE_MSI	0x022C	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
140	PCIE_EDMA[8]	0x0230	
141	PCIE_EDMA[9]	0x0234	
142	PCIE_EDMA[10]	0x0238	
143	PCIE_EDMA[11]	0x023C	
144	PCIE_EDMA[12]	0x0240	
145	PCIE_EDMA[13]	0x0244	
146	PCIE_EDMA[14]	0x0248	
147	PCIE_EDMA[15]	0x024C	
148	GPU_EVENT	0x0250	
149	GPU_JOB	0x0254	
150	GPU_MMU	0x0258	
151	GPU	0x025C	
152	VE3	0x0260	
153	MEMC_DFS	0x0264	
154	CSI_DMA0	0x0268	
155	CSI_DMA1	0x026C	
156	CSI_DMA2	0x0270	
157	CSI_DMA3	0x0274	
158	CSI_VIPP0	0x0278	
159	CSI_VIPP1	0x027C	
160	CSI_VIPP2	0x0280	
161	CSI_VIPP3	0x0284	
162	CSI_PARSER0	0x0288	
163	CSI_PARSER1	0x028C	
164	CSI_PARSER2	0x0290	
165	CSI_ISP0	0x0294	
166	CSI_ISP1	0x0298	
167	CSI_ISP2	0x029C	
168	CSI_ISP3	0x02A0	
169	CSI_CMB	0x02A4	
170	CSI_TDM	0x02A8	
171	CSI_TOP_PKT	0x02AC	
172	GPIOK_NS	0x02B0	
173	GPIOK_S	0x02B4	
174	PWMCTRL1	0x02B8	
175	G2D	0x02BC	
176	EDP	0x02C0	
177		0x02C4	
178		0x02C8	
179	CSI_PARSER3	0x02CC	
180	NMI	0x02D0	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
181	S_PPU	0x02D4	
182	S_PPU1	0x02D8	
183	TWD	0x02DC	
184	CPUS_WDT	0x02E0	
185	CPUS_TIMER0	0x02E4	
186	CPUS_TIMER1	0x02E8	
187	CPUS_TIMER2	0x02EC	
188	S_TWI2	0x02F0	
189	ALARM	0x02F4	
190	GPIOL_S	0x02F8	
191	GPIOL_NS	0x02FC	
192	GPIOM_S	0x0300	
193	GPIOM_NS	0x0304	
194	S_UART0	0x0308	
195	S_UART1	0x030C	
196	S_TWI0	0x0310	
197	S_TWI1	0x0314	
198		0x0318	
199	S_CIRRX	0x031C	
200	S_PWMCTRL	0x0320	
201		0x0324	
202	AHBS_HREADY_TIME_OUT	0x0328	
203	CPUIDLE(PCK600_CPU)	0x032C	
204	S_SPI	0x0330	
205	S_SPINLOCK	0x0334	
206	CPUS_MSGBOX_CPUX	0x0338	
207		0x033C	
208		0x0340	
209		0x0344	
210		0x0348	
211		0x034C	
212	S_TWD	0x0350	
213		0x0354	
214		0x0358	
215		0x035C	
216		0x0360	
217	MCU_TIMER0	0x0364	
218	MCU_TIMER1	0x0368	
219	MCU_TIMER2	0x036C	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
220	MCU_AHB0_TO	0x0370	
221	MCU_AHB1_TO	0x0374	
222	AUDIO CODEC	0x0378	
223	DMIC	0x037C	
224	I2S0	0x0380	
225	I2S1D	0x0384	
226	I2S2	0x0388	
227	I2S3	0x038C	
228	OWA	0x0390	
229	MCU_DMAC_NS	0x0394	
230	MCU_DMAC_S	0x0398	
231		0x039C	
232		0x03A0	
233	MCU_TIMER3	0x03A4	
234	MCU_TIMER4	0x03A8	
235	MCU_TIMER5	0x03AC	
236		0x03B0	
237		0x03B4	
238	RISCV_WDT	0x03B8	
239	MCU_PWMCTRL	0x03BC	
240		0x03C0	
241		0x03C4	
242		0x03C8	
243		0x03CC	
244		0x03D0	
245		0x03D4	
246		0x03D8	
247		0x03DC	
248		0x03E0	
249		0x03E4	
250		0x03E8	
251		0x03EC	
252		0x03F0	
253		0x03F4	
254		0x03F8	
255		0x03FC	
CPUX Related			
256	nERRIRQ[0]	0x0400	L3 ECC error that causes potential data corruption or loss of coherency
257	nERRIRQ[1]	0x0404	Core0 ECC error that causes potential data

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
			corruption or loss of coherency
258	nERRIRQ[2]	0x0408	Core1 ECC error that causes potential data corruption or loss of coherency
259	nERRIRQ[3]	0x040C	Core2 ECC error that causes potential data corruption or loss of coherency
260	nERRIRQ[4]	0x0410	Core3 ECC error that causes potential data corruption or loss of coherency
261	nERRIRQ[5]	0x0414	Core4 ECC error that causes potential data corruption or loss of coherency
262	nERRIRQ[6]	0x0418	Core5 ECC error that causes potential data corruption or loss of coherency
263	nERRIRQ[7]	0x041C	Core6 ECC error that causes potential data corruption or loss of coherency
264	nERRIRQ[8]	0x0220	Core7 ECC error that causes potential data corruption or loss of coherency
265	nFAULTIRQ[0]	0x0424	L3 detected 1-bit or 2-bit ECC or Parity error in the RAMs
266	nFAULTIRQ[1]	0x0428	Core0 detected 1-bit or 2-bit ECC or Parity error in the RAMs
267	nFAULTIRQ[2]	0x042C	Core1 detected 1-bit or 2-bit ECC or Parity error in the RAMs
268	nFAULTIRQ[3]	0x0430	Core2 detected 1-bit or 2-bit ECC or Parity error in the RAMs

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
269	nFAULTIRQ[4]	0x0434	Core3 detected 1-bit or 2-bit ECC or Parity error in the RAMs
270	nFAULTIRQ[5]	0x0438	Core4 detected 1-bit or 2-bit ECC or Parity error in the RAMs
271	nFAULTIRQ[6]	0x043C	Core5 detected 1-bit or 2-bit ECC or Parity error in the RAMs
272	nFAULTIRQ[7]	0x0440	Core6 detected 1-bit or 2-bit ECC or Parity error in the RAMs
273	nFAULTIRQ[8]	0x0444	Core7 detected 1-bit or 2-bit ECC or Parity error in the RAMs
274	nCLUSTERPMUIRQ	0x0448	Cluster PMU interrupt request
275	GIC_FAULT_INT	0x044C	
276	GIC_ERR_INT	0x0450	
277	GIC_PMU_INT	0x0454	
278		0x0458	
279		0x045C	
280		0x0460	
281		0x0464	
282		0x0468	
283		0x046C	
284		0x0470	
285		0x0474	
286		0x0478	
287		0x047C	

2.7.3 Register List

Module Name	Base Address	Comments
GIC		
GIC600_MON_4	0x03400000	General interrupt controller(23*64KB)
GITS_TRANSLATER	0x03450000	

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NOTE

Offsets that are not shown are reserved and RAZ/WI. Accessing these offsets might be reported in error record 0 as a SYN_ACE_BAD access.

Register Name	Offset	Description
GICD_CTLR	0x00000	Distributor Control Register
GICD_TYPER	0x00004	Interrupt Controller Type Register
GICD_IIDR	0x00008	Distributor Implementer Identification Register
GICD_FCTLR	0x00020	Function Control Register
GICD_SAC	0x00024	Secure Access Control
GICD_SETSPI_NSR	0x00040	Non-secure SPI Set Register
GICD_CLRSPI_NSR	0x00048	Non-secure SPI Clear Register
GICD_CLRSPI_NSR	0x00050	Secure SPI Set Register
GICD_CLRSPI_SR	0x00058	Secure SPI Clear Register
GICD_IGROUPRn	0x4*N +0x00080 (N=0-31)	Interrupt Group Registers
GICD_ISENABLERn	0x4*N +0x00100 (N=0-31)	Interrupt Set-Enable Registers 0-N
GICD_ICENABLERn	0x4*N +0x00180 (N=0-31)	Interrupt Clear-Enable Registers 0-N
GICD_ISPENDRn	0x4*N +0x00200 (N=0-31)	Interrupt Set-Pending Registers
GICD_ICPENDRn	0x4*N +0x00280 (N=0-31)	Interrupt Clear-Pending Registers
GICD_ISACTIVERn	0x4*N +0x00300 (N=0-31)	Interrupt Set-Active Registers
GICD_ICACTIVERn	0x4*N +0x00380 (N=0-31)	Interrupt Clear-Active Registers
GICD_IPRIORITYRn	0x4*N +0x00400 (N=0-255)	Interrupt Priority Registers
GICD_ICFGRn	0x4*N +0x00C00 (N=0-63)	Interrupt Configuration Registers
GICD_IGRPMODRn	0x4*N +0x00D00 (N=0-63)	Interrupt Group Modifier Registers
GICD_NSACRn	0x4*N +0x00E00 (N=0-63)	Non-secure Access Control Registers
GICD_IROUTERn	0x8*N +0x06000 (N=32-1019)	Interrupt Routing Registers
GICD_CHIPSR	0x0C000	Chip Status Register
GICD_DCHIPR	0x0C004	Default Chip Register
GICD_CHIPRn	0x4*N +0x0C000	Chip Registers

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Register Name	Offset	Description
	(N=2-32)	
GICD_ICLARn	0x4*N +0x0E000 (N=2-63)	Interrupt Class Registers
GICD_IERRRn	0x4*N +0x0E100 (N=2-31)	Interrupt Error Registers
GICD_CFGID	0x0F000	Configuration ID Register
GICD_PIDR4	0x0FFD0	Peripheral ID4 Register
GICD_PIDR5	0x0FFD4	Peripheral ID5 Register
GICD_PIDR6	0x0FFD8	Peripheral ID6 Register
GICD_PIDR7	0x0FFDC	Peripheral ID7 Register
GICD_PIDR0	0x0FFE0	Peripheral ID0 Register
GICD_PIDR1	0x0FFE4	Peripheral ID1 Register
GICD_PIDR2	0x0FFE8	Peripheral ID2 Register
GICD_PIDR3	0x0FFEC	Peripheral ID3 Register
GICD_CIDR0	0x0FFF0	Component ID 0 Register
GICD_CIDR1	0x0FFF4	Component ID 1 Register
GICD_CIDR2	0x0FFF8	Component ID 2 Register
GICD_CIDR3	0x0FFFC	Component ID 3 Register
GICA_SETSPI_NSR	0x10040	Aliased Non-secure SPI Set Register
GICA_CLRSPI_NSR	0x10048	Aliased Non-secure SPI Clear Register
GICA_SETSPI_SR	0x10050	Aliased Secure SPI Set Register
GICA_CLRSPI_SR	0x10058	Aliased Secure SPI Clear Register
GICT_ERR<n>FR	0x10*N +0x20000 (N=0-2)	Error Record Feature Register
GICT_ERR<n>CTLR	0x10*N +0x20008 (N=0-2)	Error Record Control Register,
GICT_ERR<n>STATUS	0x10*N +0x20010 (N=0-2)	Error Record Primary Status Register
GICT_ERR<n>ADDR	0x10*N +0x20018 (N=0-2)	Error Record Address Register
GICT_ERR<n>MISC0	0x10*N +0x20020 (N=0-2)	Error Record Miscellaneous Register 0
GICT_ERR<n>MISC1	0x10*N +0x20028 (N=0-2)	Error Record Miscellaneous Register 1
GICT_ERRGSR	0x2E000	Error Group Status Register,
GICT_ERRIRQCR<n>	0x4*N +0x2E800 (N=0-2)	Error Interrupt Configuration Register
GICT_DEVARCH	0x2FFBC	Device Architecture register
GICT_ERRIDR	0x2FFC8	Error Record ID Register
GICT_PIDR4	0x2FFD0	Peripheral ID4 Register
GICT_PIDR5	0x2FFD4	Peripheral ID5 Register

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Register Name	Offset	Description
GICT_PIDR6	0x2FFD8	Peripheral ID6 Register
GICT_PIDR7	0x2FFDC	Peripheral ID7 Register
GICT_PIDR0	0x2FFE0	Peripheral ID0 Register
GICT_PIDR1	0x2FFE4	Peripheral ID1 Register
GICT_PIDR2	0x2FFE8	Peripheral ID2 Register
GICT_PIDR3	0x2FFEC	Peripheral ID3 Register
GICT_CIDR0	0x2FFF0	Component ID 0 Register
GICT_CIDR1	0x2FFF4	Component ID 1 Register
GICT_CIDR2	0x2FFF8	Component ID 2 Register
GICT_CIDR3	0x2FFFC	Component ID 3 Register
GICP_EVCNTRn	0x4*N +0x30000 (N=0-2)	Event Counter Registers
GICP_EVTYPERn	0x4*N +0x30400 (N=0-2)	Event Type Configuration Register
GICP_SVRn	0x4*N +0x30600 (N=0-2)	Shadow Value Registers
GICP_FRn	0x4*N +0x30A00 (N=0-2)	Filter Registers
GICP_CNTENSET0	0x30C00	Counter Enable Set Register
GICP_CNTENCLR0	0x30C20	Counter Enable Clear Register 0,
GICP_INTENSET0	0x30C40	Interrupt Contribution Enable Set Register 0
GICP_INTENCLR0	0x30C60	Interrupt Contribution Enable Clear Register 0,
GICP_OVSCLR0	0x30C80	Overflow Status Clear Register 0,
GICP_OVSSET0	0x30CC0	Overflow Status Set Register 0,
GICP_CAPR	0x30D88	Counter Shadow Value Capture Register
GICP_CFGR	0x30E00	Configuration Information Register
GICP_CR	0x30E04	Control Register
GICP_IRQCR	0x30E50	Interrupt Configuration Register
GICP_PMAUTHSTATUS	0x30FB8	
GICP_PMDEVARCH	0x30FBC	
GICP_PMDEVTYPE	0x30FCC	
GICP_PIDR4	0x30FD0	Peripheral ID4 Register
GICP_PIDR5	0x30FD4	Peripheral ID5 Register
GICP_PIDR6	0x30FD8	Peripheral ID6 Register
GICP_PIDR7	0x30FDC	Peripheral ID7 Register
GICP_PIDR0	0x30FE0	Peripheral ID0 Register
GICP_PIDR1	0x30FE4	Peripheral ID1 Register
GICP_PIDR2	0x30FE8	Peripheral ID2 Register
GICP_PIDR3	0x30FEC	Peripheral ID3 Register
GICP_CIDR0	0x30FF0	Component ID 0 Register
GICP_CIDR1	0x30FF4	Component ID 1 Register
GICP_CIDR2	0x30FF8	Component ID 2 Register

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Register Name	Offset	Description
GICP_CIDR3	0x30FFC	Component ID 3 Register
GITS_CTLR	0x40000	ITS Control Register
GITS_IIDR	0x40004	ITS Implementer Identification Register
GITS_TYPER	0x40008	Interrupt Controller Type Register
GITS_FCTLR	0x40020	Function Control Register
GITS_OPR	0x40028	Operations Register
GITS_OPSR	0x40030	Operation Status Register
GITS_CBASER	0x40080	Command Queue Control Register
GITS_CWRITER	0x40088	Command Queue Write Pointer Register
GITS_CREADR	0x40090	Command Queue Read Pointer Register
GITS_BASER0	0x40100	ITS Translation Table Descriptor Register0
GITS_BASER1	0x40108	ITS Translation Table Descriptor Register1
GITS_CFGID	0x4F000	Configuration ID Register
GITS_PIDR4	0x4FFD0	Peripheral ID4 Register
GITS_PIDR5	0x4FFD4	Peripheral ID5 Register
GITS_PIDR6	0x4FFD8	Peripheral ID6 Register
GITS_PIDR7	0x4FFDC	Peripheral ID7 Register
GITS_PIDR0	0x4FFE0	Peripheral ID0 Register
GITS_PIDR1	0x4FFE4	Peripheral ID1 Register
GITS_PIDR2	0x4FFE8	Peripheral ID2 Register
GITS_PIDR3	0x4FFEC	Peripheral ID3 Register
GITS_CIDR0	0x4FFF0	Component ID 0 Register
GITS_CIDR1	0x4FFF4	Component ID 1 Register
GITS_CIDR2	0x4FFF8	Component ID 2 Register
GITS_CIDR3	0x4FFFC	Component ID 3 Register
GITS_TRANSLATER	0x50040	ITS Translation Register
GICR_CTLR_C0	0x60000	Redistributor Control Register
GICR_IIDR_C0	0x60004	Redistributor Implementation Identification Register
GICR_TYPER_C0	0x60008	Interrupt Controller Type Register
GICR_WAKER_C0	0x60014	Power Management Control Register
GICR_FCTLR_C0	0x60020	Function Control Register
GICR_PWRR_C0	0x60024	Power Register
GICR_CLASS_C0	0x60028	Class Register
GICR_SETLPIR_C0	0x60040	
GICR_CLRLPIR_C0	0x60048	
GICR_PROPBASER_C0	0x60070	Redistributor Properties Base Address Register
GICR_PENDBASER_C0	0x60078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C0	0x600A0	
GICR_INVALLR_C0	0x600B0	
GICR_SYNCR_C0	0x600C0	

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Register Name	Offset	Description
GICR_PIDR4_C0	0x6FFD0	Peripheral ID4 Register
GICR_PIDR5_C0	0x6FFD4	Peripheral ID5 Register
GICR_PIDR6_C0	0x6FFD8	Peripheral ID6 Register
GICR_PIDR7_C0	0x6FFDC	Peripheral ID7 Register
GICR_PIDR0_C0	0x6FFE0	Peripheral ID0 Register
GICR_PIDR1_C0	0x6FFE4	Peripheral ID1 Register
GICR_PIDR2_C0	0x6FFE8	Peripheral ID2 Register
GICR_PIDR3_C0	0x6FFEC	Peripheral ID3 Register
GICR_CIDR0_C0	0x6FFF0	Component ID 0 Register
GICR_CIDR1_C0	0x6FFF4	Component ID 1 Register
GICR_CIDR2_C0	0x6FFF8	Component ID 2 Register
GICR_CIDR3_C0	0x6FFFC	Component ID 3 Register
GICR_IGROUPR0_C0	0x70080	Interrupt Group Register
GICR_ISENABLER0_C0	0x70100	Interrupt Set-Enable Register
GICR_ICENABLER0_C0	0x70180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C0	0x70200	Interrupt Set-Pending Register
GICR_ICPENDR0_C0	0x70280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C0	0x70300	Interrupt Set-Active Register
GICR_ICACTIVER0_C0	0x70380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C0	0x4*N +0x70400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C0	0x4*N +0x70C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C0	0x70D00	Interrupt Group Modifier Register
GICR_NSACR_C0	0x70E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C0	0x7C000	Miscellaneous Status Register
GICR_IERRVR_C0	0x7C008	Interrupt Error Valid Register
GICR_SGIDR_C0	0x7C010	SGI Default Register
GICR_CFGID0_C0	0x7F000	Configuration ID0 Register
GICR_CFGID1_C0	0x7F004	Configuration ID1 Register
GICR_CTLR_C1	0x80000	Redistributor Control Register
GICR_IIDR_C1	0x80004	Redistributor Implementation Identification Register
GICR_TYPER_C1	0x80008	Interrupt Controller Type Register
GICR_WAKER_C1	0x80014	Power Management Control Register
GICR_FCTLR_C1	0x80020	Function Control Register
GICR_PWRR_C1	0x80024	Power Register
GICR_CLASS_C1	0x80028	Class Register
GICR_SETLPIR_C1	0x80040	
GICR_CLRLPIR_C1	0x80048	
GICR_PROPBASER_C1	0x80070	Redistributor Properties Base Address Register
GICR_PENDBASER_C1	0x80078	Redistributor LPI Pending Table Base Address

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Register Name	Offset	Description
		Register
GICR_INVLPIR_C1	0x800A0	
GICR_INVALLR_C1	0x800B0	
GICR_SYNCR_C1	0x800C0	
GICR_PIDR4_C1	0x8FFD0	Peripheral ID4 Register
GICR_PIDR5_C1	0x8FFD4	Peripheral ID5 Register
GICR_PIDR6_C1	0x8FFD8	Peripheral ID6 Register
GICR_PIDR7_C1	0x8FFDC	Peripheral ID7 Register
GICR_PIDR0_C1	0x8FFE0	Peripheral ID0 Register
GICR_PIDR1_C1	0x8FFE4	Peripheral ID1 Register
GICR_PIDR2_C1	0x8FFE8	Peripheral ID2 Register
GICR_PIDR3_C1	0x8FFEC	Peripheral ID3 Register
GICR_CIDR0_C1	0x8FFF0	Component ID 0 Register
GICR_CIDR1_C1	0x8FFF4	Component ID 1 Register
GICR_CIDR2_C1	0x8FFF8	Component ID 2 Register
GICR_CIDR3_C1	0x8FFFC	Component ID 3 Register
GICR_IGROUPR0_C1	0x90080	Interrupt Group Register
GICR_ISENABLER0_C1	0x90100	Interrupt Set-Enable Register
GICR_ICENABLER0_C1	0x90180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C1	0x90200	Interrupt Set-Pending Register
GICR_ICPENDR0_C1	0x90280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C1	0x90300	Interrupt Set-Active Register
GICR_ICACTIVER0_C1	0x90380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C1	0x4*N +0x90400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C1	0x4*N +0x90C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C1	0x90D00	Interrupt Group Modifier Register
GICR_NSACR_C1	0x90E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C1	0x9C000	Miscellaneous Status Register
GICR_IERRVR_C1	0x9C008	Interrupt Error Valid Register
GICR_SGIDR_C1	0x9C010	SGI Default Register
GICR_CFGID0_C1	0x9F000	Configuration ID0 Register
GICR_CFGID1_C1	0x9F004	Configuration ID1 Register
GICR_CTLR_C2	0xA0000	Redistributor Control Register
GICR_IIDR_C2	0xA0004	Redistributor Implementation Identification Register
GICR_TYPER_C2	0xA0008	Interrupt Controller Type Register
GICR_WAKER_C2	0xA0014	Power Management Control Register
GICR_FCTLR_C2	0xA0020	Function Control Register
GICR_PWRR_C2	0xA0024	Power Register
GICR_CLASS_C2	0xA0028	Class Register

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Register Name	Offset	Description
GICR_SETLPIR_C2	0xA0040	
GICR_CLRLPIR_C2	0xA0048	
GICR_PROPBASER_C2	0xA0070	Redistributor Properties Base Address Register
GICR_PENDBASER_C2	0xA0078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C2	0xA00A0	
GICR_INVALLR_C2	0xA00B0	
GICR_SYNCR_C2	0xA00C0	
GICR_PIDR4_C2	0xAFFD0	Peripheral ID4 Register
GICR_PIDR5_C2	0xAFFD4	Peripheral ID5 Register
GICR_PIDR6_C2	0xAFFD8	Peripheral ID6 Register
GICR_PIDR7_C2	0xAFFDC	Peripheral ID7 Register
GICR_PIDR0_C2	0xAFFE0	Peripheral ID0 Register
GICR_PIDR1_C2	0xAFFE4	Peripheral ID1 Register
GICR_PIDR2_C2	0xAFFE8	Peripheral ID2 Register
GICR_PIDR3_C2	0xAFFEC	Peripheral ID3 Register
GICR_CIDR0_C2	0xAFFF0	Component ID 0 Register
GICR_CIDR1_C2	0xAFFF4	Component ID 1 Register
GICR_CIDR2_C2	0xAFFF8	Component ID 2 Register
GICR_CIDR3_C2	0xAFFFC	Component ID 3 Register
GICR_IGROUPR0_C2	0xB0080	Interrupt Group Register
GICR_ISENABLER0_C2	0xB0100	Interrupt Set-Enable Register
GICR_ICENABLER0_C2	0xB0180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C2	0xB0200	Interrupt Set-Pending Register
GICR_ICPENDR0_C2	0xB0280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C2	0xB0300	Interrupt Set-Active Register
GICR_ICACTIVER0_C2	0xB0380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C2	0x4*N +0xB0400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C2	0x4*N +0xB0C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C2	0xB0D00	Interrupt Group Modifier Register
GICR_NSACR_C2	0xB0E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C2	0xBC000	Miscellaneous Status Register
GICR_IERRVR_C2	0xBC008	Interrupt Error Valid Register
GICR_SGIDR_C2	0xBC010	SGI Default Register
GICR_CFGID0_C2	0xBF000	Configuration ID0 Register
GICR_CFGID1_C2	0xBF004	Configuration ID1 Register
GICR_CTLR_C3	0xC0000	Redistributor Control Register
GICR_IIDR_C3	0xC0004	Redistributor Implementation Identification Register
GICR_TYPER_C3	0xC0008	Interrupt Controller Type Register

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Register Name	Offset	Description
GICR_WAKER_C3	0xC0014	Power Management Control Register
GICR_FCTLR_C3	0xC0020	Function Control Register
GICR_PWRR_C3	0xC0024	Power Register
GICR_CLASS_C3	0xC0028	Class Register
GICR_SETLPIR_C3	0xC0040	
GICR_CLRLPIR_C3	0xC0048	
GICR_PROPBASER_C3	0xC0070	Redistributor Properties Base Address Register
GICR_PENDBASER_C3	0xC0078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C3	0xC00A0	
GICR_INVALLR_C3	0xC00B0	
GICR_SYNCR_C3	0xC00C0	
GICR_PIDR4_C3	0xCFFD0	Peripheral ID4 Register
GICR_PIDR5_C3	0xCFFD4	Peripheral ID5 Register
GICR_PIDR6_C3	0xCFFD8	Peripheral ID6 Register
GICR_PIDR7_C3	0xCFFDC	Peripheral ID7 Register
GICR_PIDR0_C3	0xCFFE0	Peripheral ID0 Register
GICR_PIDR1_C3	0xCFFE4	Peripheral ID1 Register
GICR_PIDR2_C3	0xCFFE8	Peripheral ID2 Register
GICR_PIDR3_C3	0xCFFEC	Peripheral ID3 Register
GICR_CIDR0_C3	0xCFFF0	Component ID 0 Register
GICR_CIDR1_C3	0xCFFF4	Component ID 1 Register
GICR_CIDR2_C3	0xCFFF8	Component ID 2 Register
GICR_CIDR3_C3	0xCFFFC	Component ID 3 Register
GICR_IGROUPR0	0xD0080	Interrupt Group Register
GICR_ISENABLER0_C3	0xD0100	Interrupt Set-Enable Register
GICR_ICENABLER0_C3	0xD0180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C3	0xD0200	Interrupt Set-Pending Register
GICR_ICPENDR0_C3	0xD0280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C3	0xD0300	Interrupt Set-Active Register
GICR_ICACTIVER0_C3	0xD0380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C3	0x4*N +0xD0400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C3	0x4*N +0xD0C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C3	0xD0D00	Interrupt Group Modifier Register
GICR_NSACR_C3	0xD0E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C3	0xDC000	Miscellaneous Status Register
GICR_IERRVR_C3	0xDC008	Interrupt Error Valid Register
GICR_SGIDR_C3	0xDC010	SGI Default Register
GICR_CFGID0_C3	0xDF000	Configuration ID0 Register
GICR_CFGID1_C3	0xDF004	Configuration ID1 Register

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Register Name	Offset	Description
GICR_CTLR_C4	0xE0000	Redistributor Control Register
GICR_IIDR_C4	0xE0004	Redistributor Implementation Identification Register
GICR_TYPER_C4	0xE0008	Interrupt Controller Type Register
GICR_WAKER_C4	0xE0014	Power Management Control Register
GICR_FCTLR_C4	0xE0020	Function Control Register
GICR_PWRR_C4	0xE0024	Power Register
GICR_CLASS_C4	0xE0028	Class Register
GICR_SETLPIR_C4	0xE0040	
GICR_CLRLPIR_C4	0xE0048	
GICR_PROPBASER_C4	0xE0070	Redistributor Properties Base Address Register
GICR_PENDBASER_C4	0xE0078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C4	0xE00A0	
GICR_INVALLR_C4	0xE00B0	
GICR_SYNCR_C4	0xE00C0	
GICR_PIDR4_C4	0xEFFD0	Peripheral ID4 Register
GICR_PIDR5_C4	0xEFFD4	Peripheral ID5 Register
GICR_PIDR6_C4	0xEFFD8	Peripheral ID6 Register
GICR_PIDR7_C4	0xEFFDC	Peripheral ID7 Register
GICR_PIDR0_C4	0xEFFE0	Peripheral ID0 Register
GICR_PIDR1_C4	0xEFFE4	Peripheral ID1 Register
GICR_PIDR2_C4	0xEFFE8	Peripheral ID2 Register
GICR_PIDR3_C4	0xEFFEC	Peripheral ID3 Register
GICR_CIDR0_C4	0xEFFF0	Component ID 0 Register
GICR_CIDR1_C4	0xEFFF4	Component ID 1 Register
GICR_CIDR2_C4	0xEFFF8	Component ID 2 Register
GICR_CIDR3_C4	0xEFFFC	Component ID 3 Register
GICR_IGROUPR0	0xF0080	Interrupt Group Register
GICR_ISENABLER0_C4	0xF0100	Interrupt Set-Enable Register
GICR_ICENABLER0_C4	0xF0180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C4	0xF0200	Interrupt Set-Pending Register
GICR_ICPENDR0_C4	0xF0280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C4	0xF0300	Interrupt Set-Active Register
GICR_ICACTIVER0_C4	0xF0380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C4	0x4*N +0xF0400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C4	0x4*N +0xF0C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C4	0xF0D00	Interrupt Group Modifier Register
GICR_NSACR_C4	0xF0E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C4	0xFC000	Miscellaneous Status Register

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Register Name	Offset	Description
GICR_IERRVR_C4	0xFC008	Interrupt Error Valid Register
GICR_SGIDR_C4	0xFC010	SGI Default Register
GICR_CFGID0_C4	0xFF000	Configuration ID0 Register
GICR_CFGID1_C4	0xFF004	Configuration ID1 Register
GICR_CTLR_C5	0x100000	Redistributor Control Register
GICR_IIDR_C5	0x100004	Redistributor Implementation Identification Register
GICR_TYPER_C5	0x100008	Interrupt Controller Type Register
GICR_WAKER_C5	0x100014	Power Management Control Register
GICR_FCTLR_C5	0x100020	Function Control Register
GICR_PWRR_C5	0x100024	Power Register
GICR_CLASS_C5	0x100028	Class Register
GICR_SETLPIR_C5	0x100040	
GICR_CLRLPIR_C5	0x100048	
GICR_PROPBASER_C5	0x100070	Redistributor Properties Base Address Register
GICR_PENDBASER_C5	0x100078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C5	0x1000A0	
GICR_INVALLR_C5	0x1000B0	
GICR_SYNCR_C5	0x1000C0	
GICR_PIDR4_C5	0x10FFD0	Peripheral ID4 Register
GICR_PIDR5_C5	0x10FFD4	Peripheral ID5 Register
GICR_PIDR6_C5	0x10FFD8	Peripheral ID6 Register
GICR_PIDR7_C5	0x10FFDC	Peripheral ID7 Register
GICR_PIDR0_C5	0x10FFE0	Peripheral ID0 Register
GICR_PIDR1_C5	0x10FFE4	Peripheral ID1 Register
GICR_PIDR2_C5	0x10FFE8	Peripheral ID2 Register
GICR_PIDR3_C5	0x10FFEC	Peripheral ID3 Register
GICR_CIDR0_C5	0x10FFF0	Component ID 0 Register
GICR_CIDR1_C5	0x10FFF4	Component ID 1 Register
GICR_CIDR2_C5	0x10FFF8	Component ID 2 Register
GICR_CIDR3_C5	0x10FFFC	Component ID 3 Register
GICR_IGROUPR0	0x110080	Interrupt Group Register
GICR_ISENABLER0_C5	0x110100	Interrupt Set-Enable Register
GICR_ICENABLER0_C5	0x110180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C5	0x110200	Interrupt Set-Pending Register
GICR_ICPENDR0_C5	0x110280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C5	0x110300	Interrupt Set-Active Register
GICR_ICACTIVER0_C5	0x110380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C5	0x4*N +0x110400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C5	0x4*N +0x110C00	Interrupt Configuration Registers

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Register Name	Offset	Description
	(N=0-1)	
GICR_IGRPMODR0_C5	0x110D00	Interrupt Group Modifier Register
GICR_NSACR_C5	0x110E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C5	0x11C000	Miscellaneous Status Register
GICR_IERRVR_C5	0x11C008	Interrupt Error Valid Register
GICR_SGIDR_C5	0x11C010	SGI Default Register
GICR_CFGID0_C5	0x11F000	Configuration ID0 Register
GICR_CFGID1_C5	0x11F004	Configuration ID1 Register
GICR_CTLR_C6	0x120000	Redistributor Control Register
GICR_IIDR_C6	0x120004	Redistributor Implementation Identification Register
GICR_TYPER_C6	0x120008	Interrupt Controller Type Register
GICR_WAKER_C6	0x120014	Power Management Control Register
GICR_FCTLR_C6	0x120020	Function Control Register
GICR_PWRR_C6	0x120024	Power Register
GICR_CLASS_C6	0x120028	Class Register
GICR_SETLPIR_C6	0x120040	
GICR_CLRLPIR_C6	0x120048	
GICR_PROPBASER_C6	0x120070	Redistributor Properties Base Address Register
GICR_PENDBASER_C6	0x120078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C6	0x1200A0	
GICR_INVALLR_C6	0x1200B0	
GICR_SYNCR_C6	0x1200C0	
GICR_PIDR4_C6	0x12FFD0	Peripheral ID4 Register
GICR_PIDR5_C6	0x12FFD4	Peripheral ID5 Register
GICR_PIDR6_C6	0x12FFD8	Peripheral ID6 Register
GICR_PIDR7_C6	0x12FFDC	Peripheral ID7 Register
GICR_PIDR0_C6	0x12FFE0	Peripheral ID0 Register
GICR_PIDR1_C6	0x12FFE4	Peripheral ID1 Register
GICR_PIDR2_C6	0x12FFE8	Peripheral ID2 Register
GICR_PIDR3_C6	0x12FFEC	Peripheral ID3 Register
GICR_CIDR0_C6	0x12FFF0	Component ID 0 Register
GICR_CIDR1_C6	0x12FFF4	Component ID 1 Register
GICR_CIDR2_C6	0x12FFF8	Component ID 2 Register
GICR_CIDR3_C6	0x12FFFC	Component ID 3 Register
GICR_IGROUPR0	0x130080	Interrupt Group Register
GICR_ISENABLER0_C6	0x130100	Interrupt Set-Enable Register
GICR_ICENABLER0_C6	0x130180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C6	0x130200	Interrupt Set-Pending Register
GICR_ICPENDR0_C6	0x130280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C6	0x130300	Interrupt Set-Active Register

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Register Name	Offset	Description
GICR_ICACTIVER0_C6	0x130380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C6	0x4*N +0x130400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C6	0x4*N +0x130C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C6	0x130D00	Interrupt Group Modifier Register
GICR_NSACR_C6	0x130E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C6	0x13C000	Miscellaneous Status Register
GICR_IERRVR_C6	0x13C008	Interrupt Error Valid Register
GICR_SGIDR_C6	0x13C010	SGI Default Register
GICR_CFGID0_C6	0x13F000	Configuration ID0 Register
GICR_CFGID1_C6	0x13F004	Configuration ID1 Register
GICR_CTLR_C7	0x140000	Redistributor Control Register
GICR_IIDR_C7	0x140004	Redistributor Implementation Identification Register
GICR_TYPER_C7	0x140008	Interrupt Controller Type Register
GICR_WAKER_C7	0x140014	Power Management Control Register
GICR_FCTLR_C7	0x140020	Function Control Register
GICR_PWRR_C7	0x140024	Power Register
GICR_CLASS_C7	0x140028	Class Register
GICR_SETLPIR_C7	0x140040	
GICR_CLRLPIR_C7	0x140048	
GICR_PROPBASER_C7	0x140070	Redistributor Properties Base Address Register
GICR_PENDBASER_C7	0x140078	Redistributor LPI Pending Table Base Address Register
GICR_INVLPIR_C7	0x1400A0	
GICR_INVALLR_C7	0x1400B0	
GICR_SYNCR_C7	0x1400C0	
GICR_PIDR4_C7	0x14FFD0	Peripheral ID4 Register
GICR_PIDR5_C7	0x14FFD4	Peripheral ID5 Register
GICR_PIDR6_C7	0x14FFD8	Peripheral ID6 Register
GICR_PIDR7_C7	0x14FFDC	Peripheral ID7 Register
GICR_PIDR0_C7	0x14FFE0	Peripheral ID0 Register
GICR_PIDR1_C7	0x14FFE4	Peripheral ID1 Register
GICR_PIDR2_C7	0x14FFE8	Peripheral ID2 Register
GICR_PIDR3_C7	0x14FFEC	Peripheral ID3 Register
GICR_CIDR0_C7	0x14FFF0	Component ID 0 Register
GICR_CIDR1_C7	0x14FFF4	Component ID 1 Register
GICR_CIDR2_C7	0x14FFF8	Component ID 2 Register
GICR_CIDR3_C7	0x14FFFC	Component ID 3 Register
GICR_IGROUPR0	0x150080	Interrupt Group Register
GICR_ISENABLER0_C7	0x150100	Interrupt Set-Enable Register

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Register Name	Offset	Description
GICR_ICENABLER0_C7	0x150180	Interrupt Clear-Enable Register
GICR_ISPENDR0_C7	0x150200	Interrupt Set-Pending Register
GICR_ICPENDR0_C7	0x150280	Peripheral Clear Pending Register
GICR_ISACTIVER0_C7	0x150300	Interrupt Set-Active Register
GICR_ICACTIVER0_C7	0x150380	Interrupt Clear-Active Register
GICR_IPRIORITYRn_C7	0x4*N +0x150400 (N=0-7)	Interrupt Priority Registers
GICR_ICFGRn_C7	0x4*N +0x150C00 (N=0-1)	Interrupt Configuration Registers
GICR_IGRPMODR0_C7	0x150D00	Interrupt Group Modifier Register
GICR_NSACR_C7	0x150E00	Non-secure Access Control Register
GICR_MISCSTATUSR_C7	0x15C000	Miscellaneous Status Register
GICR_IERRVR_C7	0x15C008	Interrupt Error Valid Register
GICR_SGIDR_C7	0x15C010	SGI Default Register
GICR_CFGID0_C7	0x15F000	Configuration ID0 Register
GICR_CFGID1_C7	0x15F004	Configuration ID1 Register
GICDA_CTLR	0x160000	Distributor Control Register
GICDA_TYPER	0x160004	Interrupt Controller Type Register
GICDA_IIDR	0x160008	Distributor Implementer Identification Register
GICDA_FCTLR	0x160020	Function Control Register
GICDA_SAC	0x160024	Secure Access Control
GICDA_SETSPI_NSR	0x160040	Non-secure SPI Set Register
GICDA_CLRSPI_NSR	0x160048	Non-secure SPI Clear Register
GICDA_CLRSPI_NSR	0x160050	Secure SPI Set Register
GICDA_CLRSPI_SR	0x160058	Secure SPI Clear Register
GICDA_IGROUPRn	0x4*N +0x160080 (N=0-31)	Interrupt Group Registers
GICDA_ISENABLERn	0x4*N +0x160100 (N=0-31)	Interrupt Set-Enable Registers 0-N
GICDA_ICENABLERn	0x4*N +0x160180 (N=0-31)	Interrupt Clear-Enable Registers 0-N
GICDA_ISPENDRn	0x4*N +0x160200 (N=0-31)	Interrupt Set-Pending Registers
GICDA_ICPENDRn	0x4*N +0x160280 (N=0-31)	Interrupt Clear-Pending Registers
GICDA_ISACTIVERn	0x4*N +0x160300 (N=0-31)	Interrupt Set-Active Registers
GICDA_ICACTIVERn	0x4*N +0x160380 (N=0-31)	Interrupt Clear-Active Registers
GICDA_IPRIORITYRn	0x4*N +0x160400 (N=0-255)	Interrupt Priority Registers
GICDA_ICFGRn	0x4*N +0x160C00	Interrupt Configuration Registers

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Register Name	Offset	Description
	(N=0-63)	
GICDA_IGRPMODRn	0x4*N +0x160D00 (N=0-63)	Interrupt Group Modifier Registers
GICDA_NSACRn	0x4*N +0x160E00 (N=0-63)	Non-secure Access Control Registers
GICDA_IROUTERn	0x16*N +0x166000 (N=32-1019)	Interrupt Routing Registers
GICDA_CHIPSR	0x16C000	Chip Status Register
GICDA_DCHIPR	0x16C004	Default Chip Register
GICDA_CHIPRn	0x4*N +0x16C000 (N=2-32)	Chip Registers
GICDA_ICLARn	0x4*N +0x16E000 (N=2-63)	Interrupt Class Registers
GICDA_IERRRn	0x4*N +0x16E100 (N=2-31)	Interrupt Error Registers
GICDA_CFGID	0x16F000	Configuration ID Register
GICDA_PIDR4	0x16FFD0	Peripheral ID4 Register
GICDA_PIDR5	0x16FFD4	Peripheral ID5 Register
GICDA_PIDR6	0x16FFD8	Peripheral ID6 Register
GICDA_PIDR7	0x16FFDC	Peripheral ID7 Register
GICDA_PIDR0	0x16FFE0	Peripheral ID0 Register
GICDA_PIDR1	0x16FFE4	Peripheral ID1 Register
GICDA_PIDR2	0x16FFE8	Peripheral ID2 Register
GICDA_PIDR3	0x16FFEC	Peripheral ID3 Register
GICDA_CIDR0	0x16FFF0	Component ID 0 Register
GICDA_CIDR1	0x16FFF4	Component ID 1 Register
GICDA_CIDR2	0x16FFF8	Component ID 2 Register
GICDA_CIDR3	0x16FFFC	Component ID 3 Register

2.7.4 Register Description

For detailed register description, please refer to *Arm® CoreLink™ GIC-600 Generic Interrupt Controller Technical Reference Manual* and *Arm® Generic Interrupt Controller Architecture Specification GIC architecture version 3 and version 4*.

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2.8 Core-Local Interrupt Controller (CLIC)

2.8.1 Overview

The Core-Local Interrupt Controller (CLIC) is only used for sampling, priority arbitration and distribution for external interrupt sources.

- supports RISC-V Core-Local Interrupt Controller Version 0.8 specification
- Up to 144 interrupt source sampling, supporting level interrupt and pulse interrupt
- 32 levels of interrupt priority
- 4 memory-mapped control registers for each interrupt
- Each attribute of this interrupt source can be configured by writing the control register of the corresponding interrupt source.

2.8.2 Functional Description

The following table describes the detail of interrupt sources.

Table 2-16 Interrupt Sources

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0-15	Reserved	0x0000-0x003C	Not Used
16	RISCV_WDT	0x0040	RISCV watchdog interrupt
17	RISCV_MSGBOX_RISCV	0x0044	RISCV MSGBOX read IRQ
18		0x0048	
19		0x004C	
20		0x0050	
21		0x0054	
22		0x0058	
23		0x005C	
24		0x0060	
25	MCU_TIMER0	0x0064	
26	MCU_TIMER1	0x0068	
27	MCU_TIMER2_	0x006C	
28	AHB0_HREADY_TIME_OUT	0x0070	MCU AHB decoder0 timer out interrupt
29	AHB1_HREADY_TIME_OUT	0x0074	MCU AHB decoder1 timer out interrupt
30	AUDIO CODEC	0x0078	Audio Codec IRQ
31	DMIC	0x007C	DMIC IRQ
32	I2S0	0x0080	I2S0 IRQ
33	I2S1	0x0084	I2S1 IRQ

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
34	I2S2	0x0088	I2S2 IRQ
35	I2S3	0x008C	I2S3 IRQ
36	OWA	0x0090	OWA IRQ
37	MCU_DMAC_NS	0x0094	MCU DMAC channel IRQ non-secure to MCU
38	MCU_DMAC_S	0x0098	MCU DMAC channel IRQ secure to MCU
39		0x009C	
40		0x00A0	
41	MCU_TIMER3	0x00A4	
42	MCU_TIMER4	0x00A8	
43	MCU_TIMER5	0x00AC	
44	MCU_PWMCTRL	0x00B0	MCU PWMCTRL Interrupt
45		0x00B4	
46		0x00B8	
47		0x00BC	
48		0x00C0	
49		0x00C4	
50		0x00C8	
51		0x00CC	
52	NMI	0x00D0	NMI interrupt in CPUS domain
53	S_PPU	0x00D4	PCK600 Q-channel Interrupt
54	S_PPU1	0x00D8	/
55	S_TWD	0x00DC	S_TWD interrupt
56	CPUS_WDT	0x00E0	CPUS_WDT interrupt
57	CPUS_TIMER0	0x00E4	CPUS_TIMER0 interrupt
58	CPUS_TIMER1	0x00E8	CPUS_TIMER1 interrupt
59	CPUS_TIMER2	0x00EC	CPUS_TIMER2 interrupt
60	S_TWI2	0x00F0	
61	ALARM	0x00F4	RTC ALARM0 interrupt
62	GPIOL_S	0x00F8	
63	GPIOL_NS	0x00FC	
64	GPIOM_S	0x0100	
65	GPIOM_NS	0x0104	
66	S_UART0	0x0108	S_UART0 interrupt
67	S_UART1	0x010C	
68	S_TWI0	0x0110	
69	S_TWI1	0x0114	
70		0x0118	
71	S_CIRRX	0x011C	S_CIRRX interrupt
72	S_PWMCTRL	0x0120	S_PWMCTRL interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
73		0x0124	
74	AHBS_HREADY_TOUT	0x0128	AHBS TIMEOUT interrupt in CPUS domain
75	PCK600_CPU	0x012C	CPUIDLE(PCK600_CPU) interrupt
76	S_SPI	0x0130	S_SPI interrupt
77	S_SPINLOCK	0x0134	S_SPINLOCK interrupt
78	CPUS_MSGBOX_CPUX	0x0138	CPUS MSGBOX write IRQ for CPUX
79		0x013C	
80		0x0140	
81	CPUS_MSGBOX_RISCV	0x0144	CPUS MSGBOX write IRQ for RISCV
82		0x0148	
83	INT_SCRI[0]	0x014C	CPUX_MSGBOX_IRQ_RISCV
84	INT_SCRI[1]	0x0150	CPUX_MSGBOX_IRQ_CPUS
85	INT_SCRI[2]	0x0154	SPLOCK_IRQ
86		0x0158	
87	INT_SCRI[4]	0x015C	
88	INT_SCRI[5]	0x0160	DMAC_IRQ1_NS
89	INT_SCRI[6]	0x0164	DMAC_IRQ1_S
90	INT_SCRI[7]	0x0168	GIC IRQ 32-39 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[7:0] in S_INTC. Group GIC IRQ bit [33:32] are fixed to be masked.
91	INT_SCRI[8]	0x016C	GIC IRQ 40-47 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[15:8] in S_INTC.
92	INT_SCRI[9]	0x0170	GIC IRQ 48-55 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[23:16] in S_INTC.

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
93	INT_SCRI[10]	0x0174	GIC IRQ 56-63 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG0[31:24] in S_INTC.
94	INT_SCRI[11]	0x0178	GIC IRQ 64-71 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[7:0] in S_INTC.
95	INT_SCRI[12]	0x017C	GIC IRQ 72-79 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[15:8] in S_INTC.
96	INT_SCRI[13]	0x0180	GIC IRQ 80-87 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[23:16] in S_INTC. Group GIC IRQ bit [83:82] are fixed to be masked.
97	INT_SCRI[14]	0x0184	GIC IRQ 88-95 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG1[31:24] in S_INTC.
98	INT_SCRI[15]	0x0188	GIC IRQ 96-103 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[7:0] in S_INTC.
99	INT_SCRI[16]	0x018C	GIC IRQ 104-111 Group Interrupt, the corresponding interrupt group mask register is

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
			GINTC_CONFIG_REG2[15:8] in S_INTC.
100	INT_SCRI[17]	0x0190	GIC IRQ 112-119 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[23:16] in S_INTC.
101	INT_SCRI[18]	0x0194	GIC IRQ 120-127 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG2[31:24] in S_INTC.
102	INT_SCRI[19]	0x0198	GIC IRQ 128-135 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[7:0] in S_INTC.
103	INT_SCRI[20]	0x019C	GIC IRQ 136-143 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[15:8] in S_INTC.
104	INT_SCRI[21]	0x01A0	GIC IRQ 144-151 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[23:16] in S_INTC.
105	INT_SCRI[22]	0x01A4	GIC IRQ 152-159 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG3[31:24] in S_INTC.
106	INT_SCRI[23]	0x01A8	GIC IRQ 160-167 Group Interrupt, the corresponding interrupt group mask register is

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
			GINTC_CONFIG_REG4[7:0] in S_INTC.
107	INT_SCRI[24]	0x01AC	GIC IRQ 168-175 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG4[15:8] in S_INTC.
108	INT_SCRI[25]	0x01B0	GIC IRQ 176-183 Group Interrupt, the corresponding interrupt group mask register is GINTC_CONFIG_REG4[23:16] in S_INTC. Group GIC IRQ bit [183:180] are fixed to be masked.
109		0x01B4	
110		0x01B8	
111		0x01BC	
112		0x01C0	
113		0x01C4	
114		0x01C8	
115		0x01CC	
116		0x01D0	
117		0x01D4	
118		0x01D8	
119		0x01DC	
120		0x01E0	
121		0x01E4	
122		0x01E8	
123		0x01EC	
124		0x01F0	
125		0x01F4	
126		0x01F8	
127		0x01FC	
128		0x0200	
129		0x0204	
130		0x0208	
131		0x020C	
132		0x0210	
133		0x0214	

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
134		0x0218	
135		0x021C	
136		0x0220	
137		0x0224	
138		0x0228	
139		0x022C	
140		0x0230	
141		0x0234	
142		0x0238	
143		0x023C	
144		0x0240	

2.8.3 Register List

2.8.3.1 CLIC Register List

Module Name	Base Address
RISCV CLIC	0xE080_0000

Register Name	Offset	Description
CLIC_CFG_REG	0x0000	CLIC Configuration Register
CLIC_MINTTHRESH_REG	0x0008	CLIC MINTTHRESH Register
CLIC_INT_REGn	0x1000+n*4	CLIC Interrupt Register n

2.8.3.2 S_INTC Register List

Module Name	Base Address
S_INTC	0x0702_1000

Register Name	Offset	Description
GINTC_CONFIG_REG0	0x00C0	Group Interrupt Configuration Register 0
GINTC_CONFIG_REG1	0x00C4	Group Interrupt Configuration Register 1
GINTC_CONFIG_REG2	0x00C8	Group Interrupt Configuration Register 2
GINTC_CONFIG_REG3	0x00CC	Group Interrupt Configuration Register 3
GINTC_CONFIG_REG4	0x00D0	Group Interrupt Configuration Register 4

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2.8.4 CLIC Register description

2.8.4.1 0x0000 CLIC Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CLICCFG_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:5	R/W	0x0	NM Indicates the effective number of bits in privilege mode. RISC-V only supports to process interrupt requests in machine mode whatever the value of CLICINTATTR MODE bit in CLIC_INT_REGn register is. The value of this bit is always 0.
4:1	R/W	0x0	NL Indicates the effective number of interrupt priority level bits. The number of bits is fixed at 8. You can fill the empty bits with 1.
0	R/W	0x1	NV Indicates the interrupt flag in hardware vector mode. This bit is fixed at 1 and this indicates that the CLIC controller supports hardware vector mode interrupt. RISC-V could perform a hardware two-stage jump to obtain the service program entry address of the hardware vector interrupt. RISC-V fetches the entry address from MTVT+ interrupt ID*4 after saving the processor field. Then RISC-V jumps to this address to process interrupt. The entry address of other mode interrupts is MTVEC[31:6]<<6.

2.8.4.2 0x0008 CLIC_MINTTHRESH_REG (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CLIC_MINTTHRESH_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	MTH Machine Mode Threshold
23:0	/	/	/

2.8.4.3 0x1000+n*0x4 CLIC Interrupt Register n (Default Value: 0x07C0_0000)

Offset: 0x1000+n*0x4			Register Name: CLIC_INT_REGn
Bit	Read/Write	Default/Hex	Description
31:27	R/W	0x0	CLICINTCTL PRIO

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Offset: 0x1000+n*0x4			Register Name: CLIC_INT_REGn
Bit	Read/Write	Default/Hex	Description
			Interrupt Priority Level
26:24	/	0x3	/
23:22	R/W	0x3	CLICINTATTR MODE Interrupt Privilege Mode RISC-V only supports to process interrupt requests in machine mode. The value of this bit is always 2'b11.
21:19	/	/	/
18:17	R/W	0x0	CLICINTATTR TRIG Interrupt Trigger Used to distinguish interrupt trigger mode. CLICINTATTR TRIG [0] = 0: Level Interrupt CLICINTATTR TRIG [0] = 1: Pulse Interrupt CLICINTATTR TRIG [1] =0: Triggered on Rising Edge CLICINTATTR TRIG[1]=1: Triggered on Falling Edge
16	R/W	0x0	CLICINTATTR SHV Hardware Vector Interrupt Indicates whether the interrupt is in hardware vector mode.
15:9	/	/	/
8	R/W	0x0	CLICINTIE Interrupt Enable
7:1	/	/	/
0	R/W	0x0	CLICINTIP Interrupt Pending **Level Interrupt Mode** the CLICINTIP bit is read-only. To modify the value of this bit, you could set the external interrupt source directly: If external interrupt source is high level, IP = 1. If external interrupt source is low level, IP =0. **Pulse Interrupt Mode** the CLICINTIP bit can be read or written. In hardware vector mode: The IP can be cleared automatically while RISC-V responds interrupt requests. In non-hardware vector mode: While RISC-V executes a CSR command, it is suggested to perform effective reading and writing operations on MNXTI register to obtain the waiting status of interrupt and the corresponding value of IP will be cleared automatically at the same time. If the interrupt request is transmitted to the RISC-V pipeline

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Offset: 0x1000+n*0x4			Register Name: CLIC_INT_REGn
Bit	Read/Write	Default/Hex	Description
			core directly, hardware is not able to clear the value of IP when RISC-V responds this interrupt. It needs to be cleared by software.

2.8.5 S_INTC Register Description

2.8.5.1 0x00C0 Group Interrupt Configuration Register 0 (Default Value:0x0000_0000)

Offset: 0x00C0			Register Name: GINTC_CONFIG_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG0. Group Interrupt [31:0] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

2.8.5.2 0x00C4 Group Interrupt Configuration Register 1 (Default Value:0x0000_0000)

Offset: 0x00C4			Register Name: GINTC_CONFIG_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG1 Group Interrupt [63:32] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

2.8.5.3 0x00C8 Group Interrupt Configuration Register 2 (Default Value:0x0000_0000)

Offset: 0x00C8			Register Name: GINTC_CONFIG_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG2 Group Interrupt [95:64] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

2.8.5.4 0x00CC Group Interrupt Configuration Register 3 (Default Value:0x0000_0000)

Offset: 0x00CC	Register Name: GINTC_CONFIG_REG3

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Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG3. Group Interrupt [127:96] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

2.8.5.5 0x00D0 Group Interrupt Configuration Register 4 (Default Value:0x0000_0000)

Offset: 0x00D0			Register Name: GINTC_CONFIG_REG4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GINT_CONFIG4. Group Interrupt [159:128] Configuration Bit. 0: Interrupt signal will not send to interrupt controller. 1: Interrupt signal will send to interrupt controller if it happens.

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2.9 I/O Memory Management Unit (IOMMU)

2.9.1 Overview

IOMMU (I/O Memory management unit) is designed for the specific memory requirements. It maps the virtual address (sent by the peripheral access memory) to the physical address. IOMMU allows multiple ways to manage the location of the physical address. It can use the physical address which has the potentially conflict mapping for different processes to allocate the memory space, and also allow application of non-continuous address mapping to the continuous virtual address space.

The IOMMU has the following features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI parallel address mapping
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI bypass function independently
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI pre-fetch independently
- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.9.2 Block Diagram

The internal module of IOMMU mainly includes the following parts.

Micro TLB: Level1 TLB, 64 words. Each peripheral corresponds to a TLB, which caching the level2 page table for the peripheral.

Macro TLB: Level2 TLB, 4K words. Each peripheral shares a level2 TLB for caching the level2 page table.

Pre-fetch Logic: Each Micro TLB corresponds to a Pre-fetch Logic. By monitoring each master device to predict the bus access, the secondary page table corresponding to the address to be accessed can be read from the memory and stored in the secondary TLB to improve the hit ratio.

PTW Logic: Page Table Walk, mainly contains PTW Cache and PTW. The PTW Cache is used to store the level1 page table; when the virtual address is missed in the level1 and level2 TLB, it will trigger the PTW. PTW Cache can store 512 level1 page tables, that is, 512 words.

PMU: Performance Monitoring Unit, which is used to count the hit efficiency and the latency.

APB Interface: IOMMU register instantiation module. CPU reads and writes the IOMMU register by APB bus.

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The following figure shows the internal block diagram of IOMMU.

Figure 2-16 IOMMU Block Diagram

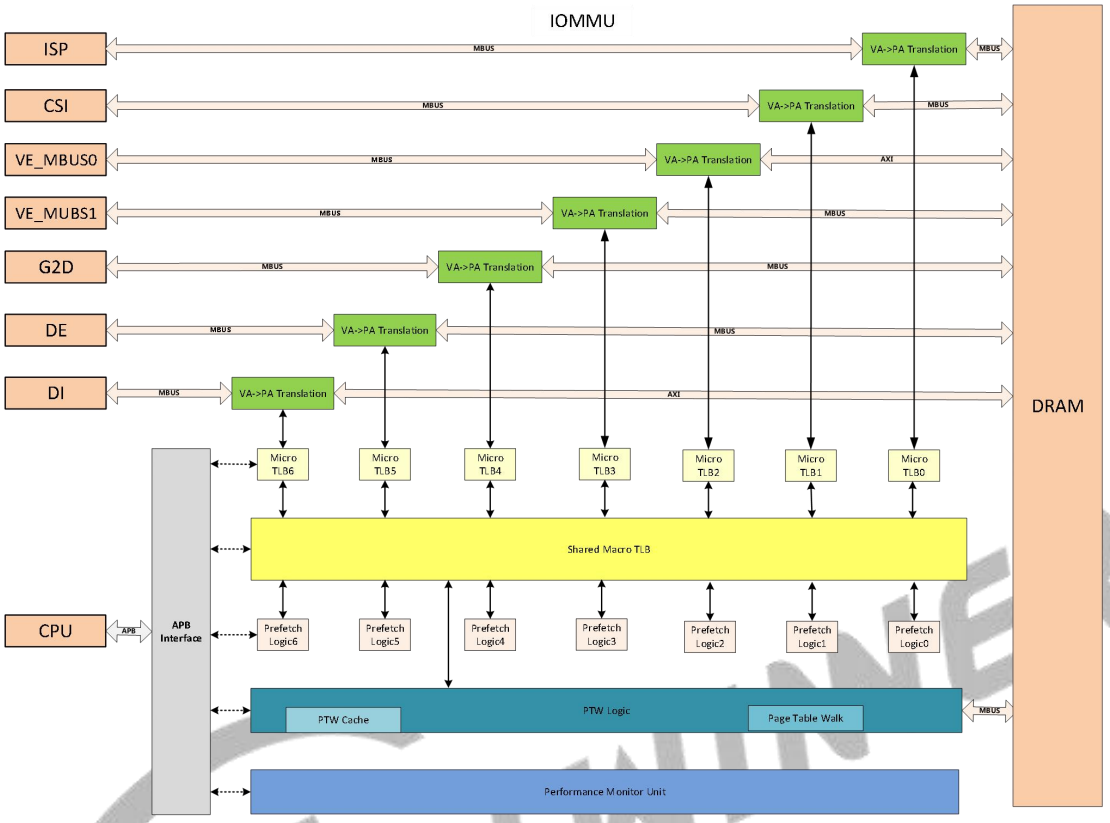

Table 2-17 Correspondence Relation between Master and Module

Master number	module
Master0	ISP
Master1	CSI
Master2	VE_MBUS0
Master3	VE_MBUS1
Master4	G2D
Master5	DE
Master6	DI

2.9.3 Functional Descriptions

2.9.3.1 Initialization

- Release the IOMMU reset signal by writing 1 to the bit[31] of the IOMMU_RESET_REG (Offset: 0x0010);
- Write the base address of the first TLB to the IOMMU_TTB_REG (Offset: 0x0050);
- Set the IOMMU_INT_ENABLE_REG (Offset: 0x0100);
- Enable the IOMMU by configuring the IOMMU_ENABLE_REG (Offset: 0x0020) in the final.

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2.9.3.2 Address Translation

In the process of address mapping, the peripheral virtual address [31:12] are retrieved in the Level1 TLB. When TLB is hit, the mapping is finished. Otherwise, they are retrieved in the Level2 TLB in the same way. If TLB is hit, the hit mapping will be written to the Level1 TLB, and hit in Level1 TLB. If Level1 and Level2 TLB are retrieved fail, the PTW will be triggered. After opening the peripheral bypass function by setting IOMMU_BYPASS_REG (Offset: 0x0030), IOMMU will not map the address typed by this peripheral, and it will output the virtual address as the physical address. The typical applications are as follows.

Micro TLB hit

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is hit, it will return a Level2 page table containing the corresponding physical addresses and the permission Index;

Step 3 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB hit

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is missed, continue to search Macro TLB;

Step 3 If Macro TLB is hit, it will return the Level2 page table to Micro TLB;

Step 4 Micro TLB receives this page table, puts it in Micro TLB (If this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;

Step 5 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache hit

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is missed, continue to search Macro TLB;

Step 3 If Macro TLB is missed, send the request to the PTW to return the corresponding page table;

Step 4 PTW first accesses PTW Cache. If the required Level1 page table exists in the PTW Cache, send the page table to PTW logic;

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Step 5 PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;

Step 6 Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;

Step 7 Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;

Step 8 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache miss

Step 1 The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;

Step 2 If Micro TLB is missed, continue to search Macro TLB;

Step 3 If Macro TLB is missed, send the request to the PTW to return the corresponding page table;

Step 4 PTW accesses PTW Cache, there is no necessary Level1 page table;

Step 5 PTW accesses the memory, gets the corresponding Level1 page table and stores it in the PTW Cache (the replace activities may happen);

Step 6 PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;

Step 7 Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;

Step 8 Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;

Step 9 The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Permission error

Step 1 The permission checking is always performed during the process of translating the address;

Step 2 Once the permission checking makes mistake, the new access of the master suspends, but the access before this checking can be continued;

Step 3 Set the error status register;

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Step 4 Trigger the interrupt.

Invalid Level1 page table

Step 1 The invalid Level1 page table is checked when PTW logic reads the new level page table from the memory;

Step 2 The PTW reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the PTW cache;

Step 3 If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.

NOTE

- Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in PTW Cache with target page table is found to be invalid after using;
- If a page table is invalid, invalidate the total cache line (that is two page tables).

Invalid Level2 page table

Step 1 The invalid Level2 page table is checked when Macro TLB reads the new level page table from the memory;

Step 2 The Macro TLB reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the Macro TLB;

Step 3 If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.

NOTE

- Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in Macro TLB with target page table is found to be invalid after using;
- If a page table is invalid, invalidate the total cache line (that is two page tables).

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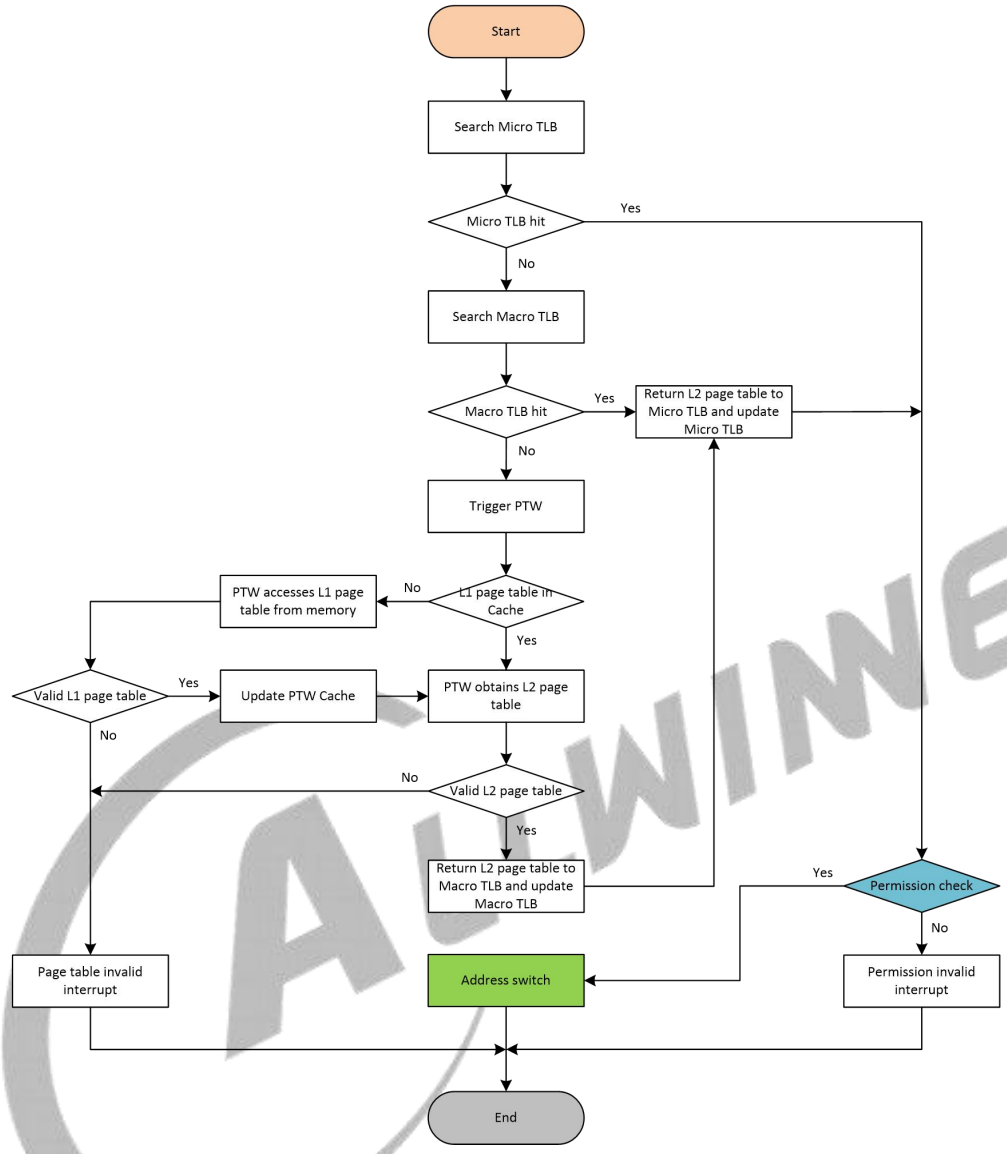
The internal address translation process is shown in the following figure.

Figure 2-17 Internal Switch Process



2.9.3.3 VA-PA Mapping

IOMMU page table is defined as the Level2 mapping. The first level is 1M address space mapping, the second level is 4K address space. This version does not support 1K, 16K and other page table sizes. IOMMU only supports a page table, the meaning is:

- All peripherals connected to IOMMU use the same virtual address space;
- The virtual address space of the peripherals can overlap;
- Different virtual addresses can map to the same physical address space;

Base address of this page table is defined by the software, and it needs 16 KB address alignment. The page table of the Level2 table item needs 1 KB address alignment. A complete VA-PA address translation process is shown in the following figure.

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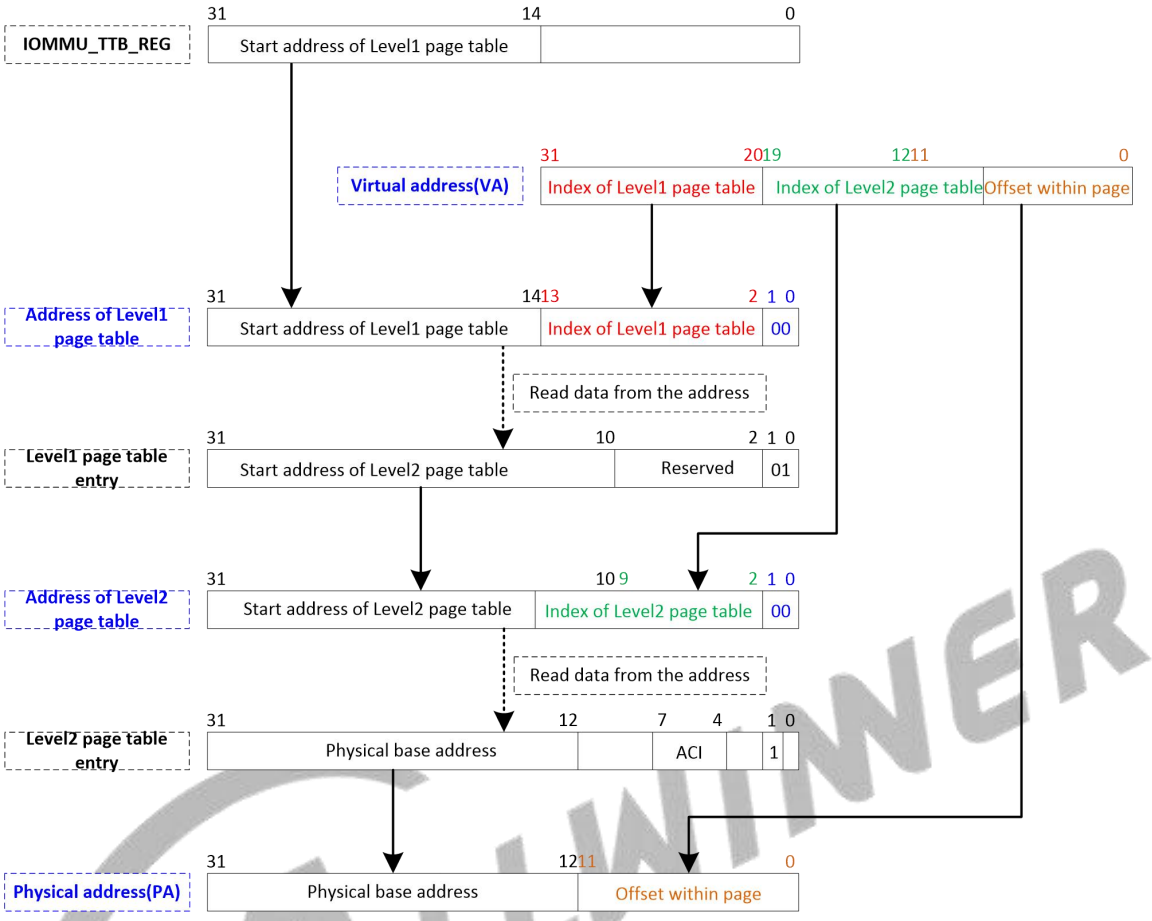
Figure 2-18 VA-PA Switch Process



2.9.3.4 Clearing and Invalidating TLB

When multi page table contents are refreshed or table address changes, all VA-PA mappings which have been cached in TLB will be invalid. You need to configure IOMMU_TLB_FLUSH_ENABLE_REG (Offset: 0x0080) to clear the TLB or PTW Cache according to the following steps:

Step 1 Suspend the access to TLB or Cache.

Step 2 Configure the corresponding Flush bit of IOMMU_TLB_FLUSH_ENABLE_REG (Offset: 0x0080).

Step 3 After the operation takes effect, the related peripherals can continue to send the new access memory operations.

When some page table is invalid or the mapping is incorrect, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. The invalid TLB supports the following two modes:

- Mode0

Step 1 Set IOMMU_TLB_IVLD_MODE_SEL_REG (Offset: 0x0084) to 0 and select mode0;

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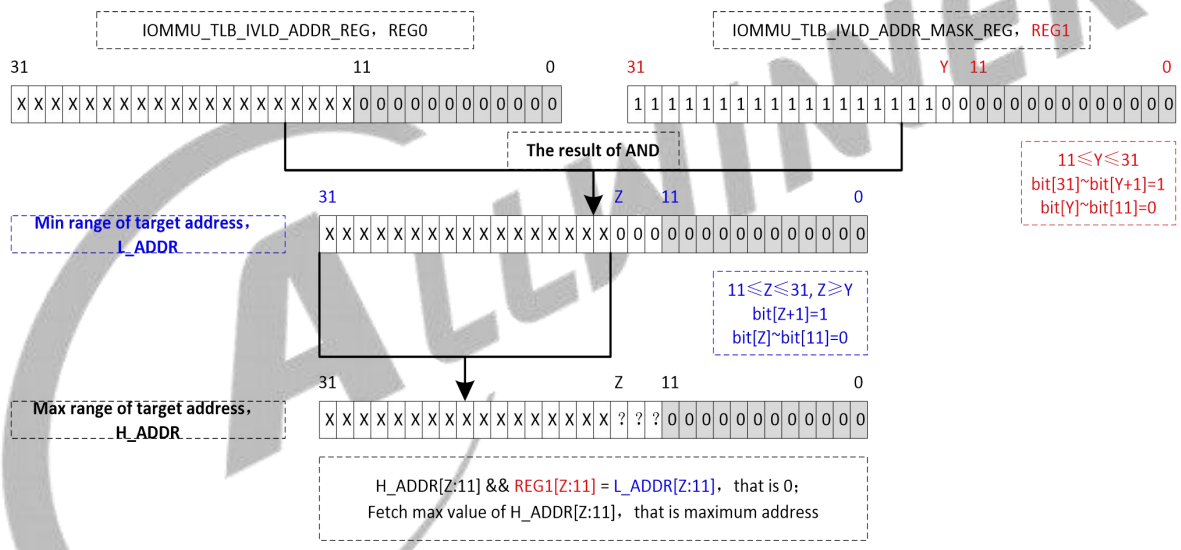
Step 2 Write the target address to IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090);

Step 3 Set the configuration values to IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094), the requirements are as follows:

- The value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) cannot be less than the IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090).
- The higher bit of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) must be continuous 1, the lower bit must be continuous 0. For example, 0xFFFFF000, 0xFFFFE000, 0xFFFFC000, 0xFFFF8000, and 0xFFFF0000 are legal values; while 0xFFFFD000, 0xFFFFB000, 0xFFFFA000, 0xFFFF9000, and 0xFFFF7000 are illegal values.

Step 4 Configure IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098) to enable the invalid operation. Among the way to determine the invalid address is to get the maximum valid bit and determine the target address range by the target address AND the mask address. The process is shown as follows.

Figure 2-19 Invalid TLB Address Range



The examples are shown below:

- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFF000 by default, the result of AND is target address. That is, only the target address is invalid.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFF0000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEEF000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFC000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEEB000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFF8000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEEC000, then target address range is from 0xEEEE8000 to 0xEEEEF000.

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- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFC000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEEE3000.

- Mode1

Step 1 Set IOMMU_TLB_IVLD_MODE_SEL_REG (Offset: 0x0084) to 1 and select mode1;

Step 2 Set the starting address and the ending address of the invalid TLB by IOMMU_TLB_IVLD_STA_ADDR_REG (Offset: 0x0088);

Step 3 Configure IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098) to enable the invalid operation, then the TLB invaliding operation can be completed.

2.9.3.5 Clearing and Invalidating PTW Cache

- Mode0

Step 1 Set IOMMU_PC_IVLD_MODE_SEL_REG (Offset: 0x009C) to 0 and select mode0.

Step 2 Invalid the IOMMU_PC_IVLD_ADDR_REG (Offset: 0x00A0), 1MB aligned.

Step 3 Configure IOMMU_PC_IVLD_ENABLE_REG (Offset: 0x00A8) to enable the invalid operation, then you can invalid one piece of CacheLine.

- Mode1

Step 1 Set IOMMU_PC_IVLD_MODE_SEL_REG (Offset: 0x009C) to 1 and select mode1.

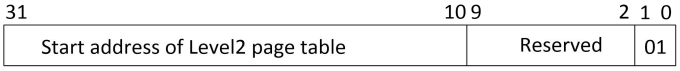
Step 2 Set the starting address and the ending address of the invalid TLB by IOMMU_PC_IVLD_STA_ADDR_REG (Offset: 0x00A4).

Step 3 Configure IOMMU_PC_IVLD_ENABLE_REG (Offset: 0x00A8) to enable the invalid operation, then you can invalid a period of sections.

2.9.3.6 Level1 Page Table

The format of Level1 page table is as follows.

Figure 2-20 Level1 Page Table Format



Bit [31:10]: Base address of Level2 page table;

Bit [9:2]: Reserved;

Bit [1:0]: 01 is a valid page table; other values are fault;

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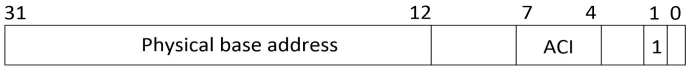
2.9.3.7 Level2 Page Table

The format of Level2 page table is as follows.

Figure 2-21 Level2 Page Table Format



Bit [31:12]: Physical address of 4K address;

Bit [11:8]: Reserved;

Bit [7:4]: ACI, permission control index; correspond to permission control bit of IOMMU Domain Authority Control Register;

Bit [3:2]: Reserved;

Bit [1]: 1 is a valid page table; 0 is fault;

Bit [0]: Reserved

2.9.4 Programming Guidelines

2.9.4.1 Resetting IOMMU

Before the IOMMU module software reset operation, make sure IOMMU is never opened, or all bus operations are completed, or DRAM and peripherals already open the corresponding switch, to shield the influence of IOMMU reset.

2.9.4.2 Enabling IOMMU

Before opening the IOMMU address mapping function, IOMMU_TTB_REG (Offset: 0x0050) should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

2.9.4.3 Configuring TTB

Operating the register must close IOMMU address mapping function, namely IOMMU_ENABLE_REG (Offset: 0x0020) is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

2.9.4.4 Clearing TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

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2.9.4.5 Reading/Writing VA Data

For the virtual address, read and write the corresponding physical address data to make sure whether IOMMU module address mapping function is normal. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after the operation is finished, check if the results are as expected.

2.9.4.6 PMU Statistics

When PMU function is used for the first time, set IOMMU_PMU_ENABLE_REG (Offset: 0x0200) to enable statistics function; when reading the relevant Register, clear the enable bit of IOMMU_PMU_ENABLE_REG (Offset: 0x0200); when PMU function is used next time, first IOMMU_PMU_CLR_REG (Offset: 0x0210) is set, after counter is cleared, set the enable bit of IOMMU_PMU_ENABLE_REG (Offset: 0x0200).

Given a Level2 page table administers continuous 4KB address, if Micro TLB misses in continuous virtual address, a Level2 page table needs to be returned from Macro TLB to hit; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So the true hit rate calculation is as follows:

```
Hit Rate = N1/M1 + (1-N1/M1)*N2/M2

N1: Micro TLB hit number
M1: Micro TLB access number
N2: Macro TLB hit number
M2: Macro TLB access number
```

2.9.5 Register List

Module Name	Base Address
IOMMU	0x0201_0000

Register Name	Offset	Description
IOMMU_RESET_REG	0x0010	IOMMU Reset Register
IOMMU_ENABLE_REG	0x0020	IOMMU Enable Register
IOMMU_BYPASS_REG	0x0030	IOMMU Bypass Register
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto Gating Register
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table Base Register
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB Enable Register

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Register Name	Offset	Description
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB Prefetch Register
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_MODE_SEL_REG	0x0084	IOMMU TLB Invalidation Mode Select Register
IOMMU_TLB_IVLD_STA_ADDR_REG	0x0088	IOMMU TLB Invalidation Start Address Register
IOMMU_TLB_IVLD_END_ADDR_REG	0x008C	IOMMU TLB Invalidation End Address Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register
IOMMU_PC_IVLD_MODE_SEL_REG	0x009C	IOMMU PC Invalidation Mode Select Register
IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register
IOMMU_PC_IVLD_STA_ADDR_REG	0x00A4	IOMMU PC Invalidation Start Address Register
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_PC_IVLD_END_ADDR_REG	0x00AC	IOMMU PC Invalidation End Address Register
IOMMU_INT_ENABLE_REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR_REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA_REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR0_REG	0x0110	IOMMU Interrupt Error Address 0 Register
IOMMU_INT_ERR_ADDR1_REG	0x0114	IOMMU Interrupt Error Address 1 Register
IOMMU_INT_ERR_ADDR2_REG	0x0118	IOMMU Interrupt Error Address 2 Register
IOMMU_INT_ERR_ADDR3_REG	0x011C	IOMMU Interrupt Error Address 3 Register
IOMMU_INT_ERR_ADDR4_REG	0x0120	IOMMU Interrupt Error Address 4 Register
IOMMU_INT_ERR_ADDR5_REG	0x0124	IOMMU Interrupt Error Address 5 Register
IOMMU_INT_ERR_ADDR6_REG	0x0128	IOMMU Interrupt Error Address 6 Register
IOMMU_INT_ERR_ADDR7_REG	0x0130	IOMMU Interrupt Error Address 7 Register
IOMMU_INT_ERR_ADDR8_REG	0x0134	IOMMU Interrupt Error Address 8 Register
IOMMU_INT_ERR_DATA0_REG	0x0150	IOMMU Interrupt Error Data 0 Register
IOMMU_INT_ERR_DATA1_REG	0x0154	IOMMU Interrupt Error Data 1 Register
IOMMU_INT_ERR_DATA2_REG	0x0158	IOMMU Interrupt Error Data 2 Register
IOMMU_INT_ERR_DATA3_REG	0x015C	IOMMU Interrupt Error Data 3 Register
IOMMU_INT_ERR_DATA4_REG	0x0160	IOMMU Interrupt Error Data 4 Register
IOMMU_INT_ERR_DATA5_REG	0x0164	IOMMU Interrupt Error Data 5 Register
IOMMU_INT_ERR_DATA6_REG	0x0168	IOMMU Interrupt Error Data 6 Register
IOMMU_INT_ERR_DATA7_REG	0x0170	IOMMU Interrupt Error Data 7 Register
IOMMU_INT_ERR_DATA8_REG	0x0174	IOMMU Interrupt Error Data 8 Register
IOMMU_L1PG_INT_REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT_REG	0x0184	IOMMU L2 Page Table Interrupt Register
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE_REG	0x0200	IOMMU PMU Enable Register

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Register Name	Offset	Description
IOMMU_PMU_CLR_REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW0_REG	0x0230	IOMMU PMU Access Low 0 Register
IOMMU_PMU_ACCESS_HIGH0_REG	0x0234	IOMMU PMU Access High 0 Register
IOMMU_PMU_HIT_LOW0_REG	0x0238	IOMMU PMU Hit Low 0 Register
IOMMU_PMU_HIT_HIGH0_REG	0x023C	IOMMU PMU Hit High 0 Register
IOMMU_PMU_ACCESS_LOW1_REG	0x0240	IOMMU PMU Access Low 1 Register
IOMMU_PMU_ACCESS_HIGH1_REG	0x0244	IOMMU PMU Access High 1 Register
IOMMU_PMU_HIT_LOW1_REG	0x0248	IOMMU PMU Hit Low 1 Register
IOMMU_PMU_HIT_HIGH1_REG	0x024C	IOMMU PMU Hit High 1 Register
IOMMU_PMU_ACCESS_LOW2_REG	0x0250	IOMMU PMU Access Low 2 Register
IOMMU_PMU_ACCESS_HIGH2_REG	0x0254	IOMMU PMU Access High 2 Register
IOMMU_PMU_HIT_LOW2_REG	0x0258	IOMMU PMU Hit Low 2 Register
IOMMU_PMU_HIT_HIGH2_REG	0x025C	IOMMU PMU Hit High 2 Register
IOMMU_PMU_ACCESS_LOW3_REG	0x0260	IOMMU PMU Access Low 3 Register
IOMMU_PMU_ACCESS_HIGH3_REG	0x0264	IOMMU PMU Access High 3 Register
IOMMU_PMU_HIT_LOW3_REG	0x0268	IOMMU PMU Hit Low 3 Register
IOMMU_PMU_HIT_HIGH3_REG	0x026C	IOMMU PMU Hit High 3 Register
IOMMU_PMU_ACCESS_LOW4_REG	0x0270	IOMMU PMU Access Low 4 Register
IOMMU_PMU_ACCESS_HIGH4_REG	0x0274	IOMMU PMU Access High 4 Register
IOMMU_PMU_HIT_LOW4_REG	0x0278	IOMMU PMU Hit Low 4 Register
IOMMU_PMU_HIT_HIGH4_REG	0x027C	IOMMU PMU Hit High 4 Register
IOMMU_PMU_ACCESS_LOW5_REG	0x0280	IOMMU PMU Access Low 5 Register
IOMMU_PMU_ACCESS_HIGH5_REG	0x0284	IOMMU PMU Access High 5 Register
IOMMU_PMU_HIT_LOW5_REG	0x0288	IOMMU PMU Hit Low 5 Register
IOMMU_PMU_HIT_HIGH5_REG	0x028C	IOMMU PMU Hit High 5 Register
IOMMU_PMU_ACCESS_LOW6_REG	0x0290	IOMMU PMU Access Low 6 Register
IOMMU_PMU_ACCESS_HIGH6_REG	0x0294	IOMMU PMU Access High 6 Register
IOMMU_PMU_HIT_LOW6_REG	0x0298	IOMMU PMU Hit Low 6 Register
IOMMU_PMU_HIT_HIGH6_REG	0x029C	IOMMU PMU Hit High 6 Register
IOMMU_PMU_ACCESS_LOW7_REG	0x02D0	IOMMU PMU Access Low 7 Register
IOMMU_PMU_ACCESS_HIGH7_REG	0x02D4	IOMMU PMU Access High 7 Register
IOMMU_PMU_HIT_LOW7_REG	0x02D8	IOMMU PMU Hit Low 7 Register
IOMMU_PMU_HIT_HIGH7_REG	0x02DC	IOMMU PMU Hit High 7 Register
IOMMU_PMU_ACCESS_LOW8_REG	0x02E0	IOMMU PMU Access Low 8 Register
IOMMU_PMU_ACCESS_HIGH8_REG	0x02E4	IOMMU PMU Access High 8 Register
IOMMU_PMU_HIT_LOW8_REG	0x02E8	IOMMU PMU Hit Low 8 Register
IOMMU_PMU_HIT_HIGH8_REG	0x02EC	IOMMU PMU Hit High 8 Register
IOMMU_PMU_TL_LOW0_REG	0x0300	IOMMU Total Latency Low 0 Register
IOMMU_PMU_TL_HIGH0_REG	0x0304	IOMMU Total Latency High 0 Register
IOMMU_PMU_ML0_REG	0x0308	IOMMU Max Latency 0 Register
IOMMU_PMU_TL_LOW1_REG	0x0310	IOMMU Total Latency Low 1 Register
IOMMU_PMU_TL_HIGH1_REG	0x0314	IOMMU Total Latency High 1 Register

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Register Name	Offset	Description
IOMMU_PMU_ML1_REG	0x0318	IOMMU Max Latency 1 Register
IOMMU_PMU_TL_LOW2_REG	0x0320	IOMMU Total Latency Low 2 Register
IOMMU_PMU_TL_HIGH2_REG	0x0324	IOMMU Total Latency High 2 Register
IOMMU_PMU_ML2_REG	0x0328	IOMMU Max Latency 2 Register
IOMMU_PMU_TL_LOW3_REG	0x0330	IOMMU Total Latency Low 3 Register
IOMMU_PMU_TL_HIGH3_REG	0x0334	IOMMU Total Latency High 3 Register
IOMMU_PMU_ML3_REG	0x0338	IOMMU Max Latency 3 Register
IOMMU_PMU_TL_LOW4_REG	0x0340	IOMMU Total Latency Low 4 Register
IOMMU_PMU_TL_HIGH4_REG	0x0344	IOMMU Total Latency High 4 Register
IOMMU_PMU_ML4_REG	0x0348	IOMMU Max Latency 4 Register
IOMMU_PMU_TL_LOW5_REG	0x0350	IOMMU Total Latency Low 5 Register
IOMMU_PMU_TL_HIGH5_REG	0x0354	IOMMU Total Latency High 5 Register
IOMMU_PMU_ML5_REG	0x0358	IOMMU Max Latency 5 Register
IOMMU_PMU_TL_LOW6_REG	0x0360	IOMMU Total Latency Low 6 Register
IOMMU_PMU_TL_HIGH6_REG	0x0364	IOMMU Total Latency High 6 Register
IOMMU_PMU_ML6_REG	0x0368	IOMMU Max Latency 6 Register

2.9.6 Register Description

2.9.6.1 0x0010 IOMMU Reset Register (Default Value: 0x8003_007F)

Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	IOMMU_RST IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; or all bus operations are completed; or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset.
30:18	/	/	/
17	R/W	0x1	PC_RST PTW Cache address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, this bit is used to reset PTW Cache individually.
16	R/W	0x1	MTLB_RST Macro TLB address convert lane software reset switch. 0: Set reset signal

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Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
			1: Release reset signal When Macro TLB occurs abnormal, this bit is used to reset Macro TLB individually.
15:7	/	/	/
6	R/W	0x1	M6_RST Master6 address convert lane software reset switch 0: Set reset signal 1: Release reset signal When Master6 occurs abnormal, this bit is used to reset Master6 individually.
5	R/W	0x1	M5_RST Master5 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, this bit is used to reset Master5 individually.
4	R/W	0x1	M4_RST Master4 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, this bit is used to reset Master4 individually.
3	R/W	0x1	M3_RST Master3 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, this bit is used to reset Master3 individually.
2	R/W	0x1	M2_RST Master2 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, this bit is used to reset Master2 individually.
1	R/W	0x1	M1_RST Master1 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master1 occurs abnormal, this bit is used to reset Master1 individually.
0	R/W	0x1	M0_RST

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Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	Read/Write	Default/Hex	Description
			Master0 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, this bit is used to reset Master0 individually.

2.9.6.2 0x0020 IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	I ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU Before IOMMU address mapping function opens, configure the Translation Table Base register; or ensure all masters are in bypass status or no the status of sending bus demand(such as reset)

2.9.6.3 0x0030 IOMMU Bypass Register (Default Value: 0x0000_007f)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	M6_BP Master6 bypass switch After bypass function is opened, IOMMU can not map the address of Master6 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
5	R/W	0x1	M5_BP Master5 bypass switch After bypass function is opened, IOMMU can not map the address of Master5 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
4	R/W	0x1	M4_BP

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Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
			Master4 bypass switch After bypass function is opened, IOMMU can not map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
3	R/W	0x1	M3_BP Master3 bypass switch After bypass function is opened, IOMMU can not map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
2	R/W	0x1	M2_BP Master2 bypass switch After bypass function is opened, IOMMU can not map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
1	R/W	0x1	M1_BP Master1 bypass switch After bypass function is opened, IOMMU can not map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
0	R/W	0x1	M0_BP Master0 bypass switch After bypass function is opened, IOMMU can not map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

NOTE

- Operating the register belongs to non-accurate timing sequence control function. That is, before the function is valid, master operation will complete address mapping function, and any subsequent operation will not perform address mapping.

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- It is suggested that master is in reset state or in no any bus operation before operating the register.

2.9.6.4 0x0040 IOMMU Auto Gating Register (Default Value: 0x0000_0001)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	IOMMU_AUTO_GATING IOMMU circuit auto gating control The purpose is to decrease power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

2.9.6.5 0x0044 IOMMU Write Buffer Control Register (Default Value: 0x0000_007f)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	Reserved
5	R/W	0x1	Reserved
4	R/W	0x1	Reserved
3	R/W	0x1	Reserved
2	R/W	0x1	Reserved
1	R/W	0x1	Reserved
0	R/W	0x1	Reserved

2.9.6.6 0x0048 IOMMU Out of Order Control Register (Default Value: 0x0000_007F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	M6_OOO_CTRL. Master6 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
5	R/W	0x1	M5_OOO_CTRL. Master5 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
4	R/W	0x1	M4_OOO_CTRL.

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Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			Master4 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
3	R/W	0x1	M3_OOO_CTRL. Master3 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
2	R/W	0x1	M2_OOO_CTRL. Master2 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
1	R/W	0x1	M1_OOO_CTRL. Master1 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order
0	R/W	0x1	M0_OOO_CTRL. Master0 Out of Order Control 0: Disable out-of-order 1: Enable out-of-order

2.9.6.7 0x004C IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_007F)

NOTE

When the virtual address sent by master is over the 4 KB boundary, 4 KB protection unit will split it into two serial access.

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x1	M6_4KB_BDY_PRT_CTRL Master6 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
5	R/W	0x1	M5_4KB_BDY_PRT_CTRL Master4 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
4	R/W	0x1	M4_4KB_BDY_PRT_CTRL Master4 4 KB boundary protect control bit

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Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
3	R/W	0x1	M3_4KB_BDY_PRT_CTRL Master3 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
2	R/W	0x1	M2_4KB_BDY_PRT_CTRL Master2 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
1	R/W	0x1	M1_4KB_BDY_PRT_CTRL Master1 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect
0	R/W	0x1	M0_4KB_BDY_PRT_CTRL Master0 4 KB boundary protect control bit 0: Disable 4 KB boundary protect 1: Enable 4 KB boundary protect

2.9.6.8 0x0050 IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: IOMMU_TTB_REG
Bit	Read/Write	Default/Hex	Description
31:14	R/W	0x0	TTB Translation Table Base Level1 page table starting address, aligned to 16 KB. When operating the register, IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0; Or Bypass function of all main equipment is set to 1, or no the state of transfer bus commands (such as setting).
13:0	/	/	/

2.9.6.9 0x0060 IOMMU TLB Enable Register (Default Value: 0x0003_007F)

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	PC_EN PTW Cache Enable 0: Disable

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Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
			1: Enbale
16	R/W	0x1	MICRO_TLB_ENABLE Micro TLB enable bit 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	MICRO_TLB6_ENABLE Micro TLB6 enable bit 0: Disable 1: Enable
5	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable
4	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable
3	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
1	R/W	0x1	MICRO1_TLB0_ENABLE Micro TLB01 enable bit 0: Disable 1: Enable
0	R/W	0x1	MACRO0_TLB_ENABLE Macro TLB0 enable bit 0: Disable 1: Enable

2.9.6.10 0x0070 IOMMU TLB PreFetch Register (Default Value: 0x0003_0000)

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

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Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x1	PF_VL_PT_TO_PC Prefetch Value Page Table to PTW Cache 0: Disable 1: Enable If the function is enabled, the prefetch function will not update the invalid Level1 page table to PTW cache.
16	R/W	0x1	PF_VL_PT_TO_MT Prefetch Value Page Table to Macro TLB 0: Disable 1: Enable If the function is enabled, the prefetch function will not update the invalid Level2 page table to Macro TLB.
15:7	/	/	/
6	R/W	0x0	MI_TLB6_PF Micro TLB6 Prefetch Enable 0: Disable 1: Enable
5	R/W	0x0	MI_TLB5_PF Micro TLB5 Prefetch Enable 0: Disable 1: Enable
4	R/W	0x0	MI_TLB4_PF Micro TLB4 Prefetch Enable 0: Disable 1: Enable
3	R/W	0x0	MI_TLB3_PF Micro TLB3 Prefetch Enable 0: Disable 1: Enable If G2D accesses DDR, it is suggested to disable the prefetch function.
2	R/W	0x0	MI_TLB2_PF Micro TLB2 Prefetch Enable 0: Disable 1: Enable
1	R/W	0x0	MI_TLB1_PF Micro TLB1 Prefetch Enable 0: Disable 1: Enable
0	R/W	0x0	MI_TLB0_PF Micro TLB0 Prefetch Enable

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Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable

2.9.6.11 0x0080 IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

When performing flush operations, all TLB/Cache access will be paused.

Before flush starts, the operation that has entered will continue until it finishes.

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PC_FS PTW Cache Flush Clear PTW Cache 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
16	R/WAC	0x0	MA_TLB_FS Macro TLB Flush Clear Macro TLB 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
15:7	/	/	/
6	R/WAC	0x0	MI_TLB6_FS Micro TLB6 Flush Clear Micro TLB6 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
5	R/WAC	0x0	MI_TLB5_FS Micro TLB5 Flush Clear Micro TLB5 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
4	R/WAC	0x0	MI_TLB4_FS

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Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
			Micro TLB4 Flush Clear Micro TLB4 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
3	R/WAC	0x0	MI_TLB3_FS Micro TLB3 Flush Clear Micro TLB3 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
2	R/WAC	0x0	MI_TLB2_FS Micro TLB2 Flush Clear Micro TLB2 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
1	R/WAC	0x0	MI_TLB1_FS Micro TLB1 Flush Clear Micro TLB1 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.
0	R/WAC	0x0	MI_TLB0_FS Micro TLB0 Flush Clear Micro TLB0 0: No clear operation or clear operation is completed 1: Enable clear operation After the Flush operation is completed, the bit can be cleared automatically.

2.9.6.12 0x0084 IOMMU TLB Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TLB_IVLD_MODE_SEL

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Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
			0: Invalidate TLB by using the Mask mode 1: Invalidate TLB by using the Start and End mode

2.9.6.13 0x0088 IOMMU TLB Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: IOMMU_TLB_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_SA TLB Invalid Start Address TLB invalid start address, 4 KB aligned.
11:0	/	/	/

2.9.6.14 0x008C IOMMU TLB Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: IOMMU_TLB_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_EA TLB Invalid End Address TLB invalid end address, 4 KB aligned.
11:0	/	/	/

2.9.6.15 0x0090 IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_ADDR TLB Invalid Address TLB invalid address, 4 KB aligned
11:0	/	/	/

Operation:

- Set the virtual address that needs to be operated in IOMMU_TLB_IVLD_ADDR_REG.
- Set the mask of virtual address that needs to be operated in IOMMU_TLB_IVLD_ADDR_MASK_REG.
- Write '1' to IOMMU_TLB_IVLD_ENABLE_REG [0].
- Read IOMMU_TLB_IVLD_ENABLE_REG [0], when it is '0', it indicates that invalidation behavior is finished.

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NOTE

- When performing invalidation operation, TLB/Cache operation has not affected.
- After or before invalidation operation starts, there is no absolute relationship between the same address switch operation and invalidation operation.

2.9.6.16 0x0094 IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB Invalid Address Mask TLB invalid address mask register, 4 KB aligned
11:0	/	/	/

2.9.6.17 0x0098 IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	TLB_IVLD_ENABLE. Enable TLB invalidation operation 0: No operation or operation is completed 1: Enable invalidation operation After invalidation operation is completed, the bit can clear automatically. When operating invalidation operation, TLB/Cache operation has not affected. After or before invalidation operation starts, there is no absolute relationship between the same address switch operation and invalidation operation.

2.9.6.18 0x009C IOMMU PC Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: IOMMU_PC_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PC_IVLD_MS. PTW Cache Invalid Mode Select. 0: Invalidate PTW by using the Mask mode

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Offset: 0x009C			Register Name: IOMMU_PC_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
			1: Invalidate PTW by using the Start and End mode

2.9.6.19 0x00A0 IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_ADDR. PTW Cache Invalid Address, 1 MB aligned.
19:0	/	/	/

2.9.6.20 0x00A4 IOMMU PC Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: IOMMU_PC_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_SA. PTW Cache Invalid Start Address, 1M aligned.
19:0	/	/	/

2.9.6.21 0x00A8 IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: IOMMU_PC_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PC_IVLD_EN. Enable PTW Cache invalidation operation 0: No operation or operation is completed 1: Enable invalidation operation After invalidation operation is completed, the bit can clear automatically. After or before invalidation operation starts, there is no absolute relationship between the same address switch operation and invalidation operation.

2.9.6.22 0x00AC IOMMU PC Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: IOMMU_PC_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_EA. PTW Cache invalid end address, 1 MB aligned.

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Offset: 0x00AC			Register Name: IOMMU_PC_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
19:0	/	/	/

2.9.6.23 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Invalid page table and permission error can not make one device or multi-devices in system work normally.

Permission error usually happens in MicroTLB. The error generates interrupt and waits for processing through software.

Invalid page table usually happens in Macro TLB. The error can not influence the access of other devices. So the error page table needs go back the way it comes, but the error should not be written in each level TLB.

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	DBG_PF_L2_IV_PT_EN. Debug or Prefetch Invalid Page Table Enable 0: Mask interrupt 1: Enable interrupt
19	R/W	0x0	DBG_PF_PC_IV_L1_PT_EN. Debug or Prefetch PTW Cache Invalid Level1 Page Table Enable 0: Mask interrupt 1: Enable interrupt
18	R/W	0x0	DBG_PF_DRAM_IV_L1_PT_EN. Debug or Prefetch DRAM Invalid Level1 Page Table Enable 0: Mask interrupt 1: Enable interrupt
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN Micro TLB6 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

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Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

2.9.6.24 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 permission invalid interrupt clear bit

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Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
			0: Invalid operation 1: Clear interrupt **Note: The bit is not used.**
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt

2.9.6.25 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

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Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens **Note: The bit is not used.**
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

2.9.6.26 0x0110 IOMMU Interrupt Error Address 0 Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR0. Interrupt Error Address0. Virtual address that caused Micro TLB0 to interrupt

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2.9.6.27 0x0114 IOMMU Interrupt Error Address 1 Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR1. Interrupt Error Address1. Virtual address that caused Micro TLB1 to interrupt

2.9.6.28 0x0118 IOMMU Interrupt Error Address 2 Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR2. Interrupt Error Address2. Virtual address that caused Micro TLB2 to interrupt

2.9.6.29 0x011C IOMMU Interrupt Error Address 3 Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR3. Interrupt Error Address3. Virtual address that caused Micro TLB3 to interrupt

2.9.6.30 0x0120 IOMMU Interrupt Error Address 4 Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR4. Interrupt Error Address4. Virtual address that caused Micro TLB4 to interrupt

2.9.6.31 0x0124 IOMMU Interrupt Error Address 5 Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR5. Interrupt Error Address5. Virtual address that caused Micro TLB5 to interrupt

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2.9.6.32 0x0128 IOMMU Interrupt Error Address 6 Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR6. Interrupt Error Address6. Virtual address that caused Micro TLB6 to interrupt

2.9.6.33 0x0130 IOMMU Interrupt Error Address 7 Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR7. Interrupt Error Address7. Virtual address that caused L1 page table to interrupt

2.9.6.34 0x0134 IOMMU Interrupt Error Address 8 Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR8. Interrupt Error Address8. Virtual address that caused L2 page table to interrupt

2.9.6.35 0x0150 IOMMU Interrupt Error Data 0 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA0. Interrupt Error Data0. Corresponding page table of virtual address that caused Micro TLB0 to interrupt

2.9.6.36 0x0154 IOMMU Interrupt Error Data 1 Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA1. Interrupt Error Data1. Corresponding page table of virtual address that caused Micro TLB1 to interrupt

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2.9.6.37 0x0158 IOMMU Interrupt Error Data 2 Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA2. Interrupt Error Data2. Corresponding page table of virtual address that caused Micro TLB2 to interrupt

2.9.6.38 0x015C IOMMU Interrupt Error Data 3 Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA3. Interrupt Error Data3. Corresponding page table of virtual address that caused Micro TLB3 to interrupt

2.9.6.39 0x0160 IOMMU Interrupt Error Data 4 Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA4. Interrupt Error Data4. Corresponding page table of virtual address that caused Micro TLB4 to interrupt

2.9.6.40 0x0164 IOMMU Interrupt Error Data 5 Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA5. Interrupt Error Data5. Corresponding page table of virtual address that caused Micro TLB5 to interrupt

2.9.6.41 0x0168 IOMMU Interrupt Error Data 6 Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA6.

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Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA6_REG
Bit	Read/Write	Default/Hex	Description
			Interrupt Error Data6. Corresponding page table of virtual address that caused Micro TLB6 to interrupt

2.9.6.42 0x0170 IOMMU Interrupt Error Data 7 Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA7. Interrupt Error Data7. Corresponding page table of virtual address that caused L1 page table to interrupt

2.9.6.43 0x0174 IOMMU Interrupt Error Data 8 Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA8. Interrupt Error Data8. Corresponding page table of virtual address that caused L2 page table to interrupt

2.9.6.44 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L1PG_INT Debug mode address switch causes L1 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT Master6 address switch causes L1 page table to occur interrupt.
5	R	0x0	MASTER5_L1PG_INT Master5 address switch causes L1 page table to occur interrupt.
4	R	0x0	MASTER4_L1PG_INT Master4 address switch causes L1 page table to occur interrupt.

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Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
3	R	0x0	MASTER3_L1PG_INT Master3 address switch causes L1 page table to occur interrupt.
2	R	0x0	MASTER2_L1PG_INT Master2 address switch causes L1 page table to occur interrupt.
1	R	0x0	MASTER1_L1PG_INT Master1 address switch causes L1 page table to occur interrupt.
0	R	0x0	MASTER0_L1PG_INT Master0 address switch causes L1 page table to occur interrupt.

2.9.6.45 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L2PG_INT Debug mode address switch causes L2 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L2PG_INT Master6 address switch causes L2 page table to occur interrupt. **Note: The bit is not used.**
5	R	0x0	MASTER5_L2PG_INT Master5 address switch causes L2 page table to occur interrupt.
4	R	0x0	MASTER4_L2PG_INT Master4 address switch causes L2 page table to occur interrupt.
3	R	0x0	MASTER3_L2PG_INT Master3 address switch causes L2 page table to occur interrupt.
2	R	0x0	MASTER2_L2PG_INT Master2 address switch causes L2 page table to occur interrupt.
1	R	0x0	MASTER1_L2PG_INT Master1 address switch causes L2 page table to occur interrupt.

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Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	MASTER0_L2PG_INT Master0 address switch causes L2 page table to occur interrupt.

2.9.6.46 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA Virtual address of read/write

2.9.6.47 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA_DATA Data corresponding to read/write virtual address

2.9.6.48 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MODE_SEL 0: Prefetch 1: Debug Mode It is used to choose prefetch mode or Debug mode.
30:9	/	/	/
8	R/W	0x0	VA_CONFIG Virtual Address Configuration 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation is completed 1: Start After the operation is completed, the bit can clear automatically.

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Read operation process:

- Write IOMMU_VA_REG [31:0];
- Write IOMMU_VA_CONFIG_REG [8] to 0;
- Write IOMMU_VA_CONFIG_REG [0] to 1 to start read-process;
- Query IOMMU_VA_CONFIG_REG [0] until it is 0;
- Read IOMMU_VA_DATA_REG [31:0].

Write operation process:

- Write IOMMU_VA_REG [31:0];
- Write IOMMU_VA_DATA_REG [31:0];
- Write IOMMU_VA_CONFIG_REG [8] to 1;
- Write IOMMU_VA_CONFIG_REG [0] to 1 to start write-process;
- Query IOMMU_VA_CONFIG_REG [0] until it is 0.

2.9.6.49 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disable statistical function 1: Enable statistical function

2.9.6.50 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation is completed 1: Clear counter data After the operation is completed, the bit can clear automatically.

2.9.6.51 0x0230 IOMMU PMU Access Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW0_REG
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW0 Record total number of Micro TLB0 access, lower 32-bit register.

2.9.6.52 0x0234 IOMMU PMU Access High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record total number of Micro TLB0 access, higher 32-bit register

2.9.6.53 0x0238 IOMMU PMU Hit Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW0 Record total number of Micro TLB0 hit, lower 32-bit register.

2.9.6.54 0x023C IOMMU PMU Hit High 0 Register (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record total number of Micro TLB0 hit, higher 32-bit register.

2.9.6.55 0x0240 IOMMU PMU Access Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW1 Record total number of Micro TLB1 access, lower 32-bit register.

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2.9.6.56 0x0244 IOMMU PMU Access High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH1 Record total number of Micro TLB1 access, higher 32-bit register.

2.9.6.57 0x0248 IOMMU PMU Hit Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW1 Record total number of Micro TLB1 hit, lower 32-bit register.

2.9.6.58 0x024C IOMMU PMU Hit High 1 Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record total number of Micro TLB1 hit, higher 11-bit register.

2.9.6.59 0x0250 IOMMU PMU Access Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW2 Record total number of Micro TLB2 access, lower 32-bit register.

2.9.6.60 0x0254 IOMMU PMU Access High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record total number of Micro TLB2 access, higher 11-bit register.

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2.9.6.61 0x0258 IOMMU PMU Hit Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW2 Record total number of Micro TLB2 hit，lower 32-bit register.

2.9.6.62 0x025C IOMMU PMU Hit High 2 Register (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record total number of Micro TLB2 hit，higher 11-bit register.

2.9.6.63 0x0260 IOMMU PMU Access Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW3 Record total number of Micro TLB3 access, lower 32-bit register.

2.9.6.64 0x0264 IOMMU PMU Access High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record total number of Micro TLB3 access, higher 11-bit register.

2.9.6.65 0x0268 IOMMU PMU Hit Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW3 Record total number of Micro TLB3 hit，lower 32-bit register.

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2.9.6.66 0x026C IOMMU PMU Hit High 3 Register (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record total number of Micro TLB3 hit，higher 11-bit register.

2.9.6.67 0x0270 IOMMU PMU Access Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW4 Record total number of Micro TLB4 access, lower 32-bit register.

2.9.6.68 0x0274 IOMMU PMU Access High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record total number of Micro TLB4 access, higher 11-bit register.

2.9.6.69 0x0278 IOMMU PMU Hit Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW4 Record total number of Micro TLB4 hit，lower 32-bit register.

2.9.6.70 0x027C IOMMU PMU Hit High 4 Register (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record total number of Micro TLB4 hit，higher 11-bit register.

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2.9.6.71 0x0280 IOMMU PMU Access Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW5 Record total number of Micro TLB5 access, lower 32-bit register.

2.9.6.72 0x0284 IOMMU PMU Access High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record total number of Micro TLB5 access, higher 11-bit register.

2.9.6.73 0x0288 IOMMU PMU Hit Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW5 Record total number of Micro TLB5 hit，lower 32-bit register.

2.9.6.74 0x028C IOMMU PMU Hit High 5 Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record total number of Micro TLB5 hit，higher 11-bit register.

2.9.6.75 0x0290 IOMMU PMU Access Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW6 Record total number of Micro TLB6 access, lower 32-bit register.

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2.9.6.76 0x0294 IOMMU PMU Access High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record total number of Micro TLB6 access, higher 11-bit register.

2.9.6.77 0x0298 IOMMU PMU Hit Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW6 Record total number of Micro TLB6 hit，lower 32-bit register.

2.9.6.78 0x029C IOMMU PMU Hit High 6 Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record total number of Micro TLB6 hit，higher 11-bit register.

2.9.6.79 0x02D0 IOMMU PMU Access Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW7 Record total number of Macro TLB access, lower 32-bit register.

2.9.6.80 0x02D4 IOMMU PMU Access High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record total number of Macro TLB access, higher 11-bit register.

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2.9.6.81 0x02D8 IOMMU PMU Hit Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW7 Record total number of Macro TLB hit，lower 32-bit register.

2.9.6.82 0x02DC IOMMU PMU Hit High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record total number of Macro TLB hit，higher 11-bit register.

2.9.6.83 0x02E0 IOMMU PMU Access Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW8 Record total number of PTW Cache access, lower 32-bit register.

2.9.6.84 0x02E4 IOMMU PMU Access High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH8 Record total number of PTW Cache access, higher 11-bit register.

2.9.6.85 0x02E8 IOMMU PMU Hit Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW8 Record total number of PTW Cache hit，lower 32-bit register.

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2.9.6.86 0x02EC IOMMU PMU Hit High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record total number of PTW Cache hit，higher 11-bit register.

2.9.6.87 0x0300 IOMMU Total Latency Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW0 Record total latency of Master0, lower 32-bit register.

2.9.6.88 0x0304 IOMMU Total Latency High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record total latency of Master0, higher 18-bit register.

2.9.6.89 0x0308 IOMMU Max Latency 0 Register (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML0 Record the max latency of Master0.

2.9.6.90 0x0310 IOMMU Total Latency Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW1 Record total latency of Master1, lower 32-bit register.

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2.9.6.91 0x0314 IOMMU Total Latency High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record total latency of Master1, higher 18-bit register.

2.9.6.92 0x0318 IOMMU Max Latency 1 Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML1 Record the max latency of Master1.

2.9.6.93 0x0320 IOMMU Total Latency Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW2 Record total latency of Master2, lower 32-bit register.

2.9.6.94 0x0324 IOMMU Total Latency High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record total latency of Master2, higher 18-bit register.

2.9.6.95 0x0328 IOMMU Max Latency 2 Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML2 Record the max latency of Master2.

2.9.6.96 0x0330 IOMMU Total Latency Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0330	Register Name: IOMMU_PMU_TL_LOW3_REG

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Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW3 Record total latency of Master3, lower 32-bit register.

2.9.6.97 0x0334 IOMMU Total Latency High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record total latency of Master3, higher 18-bit register.

2.9.6.98 0x0338 IOMMU Max Latency 3 Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML3 Record the max latency of Master3.

2.9.6.99 0x0340 IOMMU Total Latency Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW4 Record total latency of Master4, lower 32-bit register.

2.9.6.100 0x0344 IOMMU Total Latency High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record total latency of Master4, higher 18-bit register.

2.9.6.101 0x0348 IOMMU Max Latency 4 Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML4 Record the max latency of Master4.

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2.9.6.102 0x0350 IOMMU Total Latency Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW5 Record total latency of Master5, lower 32-bit register.

2.9.6.103 0x0354 IOMMU Total Latency High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH5 Record total latency of Master5, higher 18-bit register.

2.9.6.104 0x0358 IOMMU Max Latency 5 Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML5 Record the max latency of Master5.

2.9.6.105 0x0360 IOMMU Total Latency Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW6 Record total latency of Master6, lower 32-bit register.

2.9.6.106 0x0364 IOMMU Total Latency High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record total latency of Master6, higher 18-bit register.

2.9.6.107 0x0368 IOMMU Max Latency 6 Register (Default Value: 0x0000_0000)

Offset: 0x0368	Register Name: IOMMU_PMU_ML6_REG

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Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML6 Record the max latency of Master6.

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2.10 Message Box (MSGBOX)

2.10.1 Overview

The Message Box (MSGBOX) provides interrupt communication mechanism for on-chip processor.

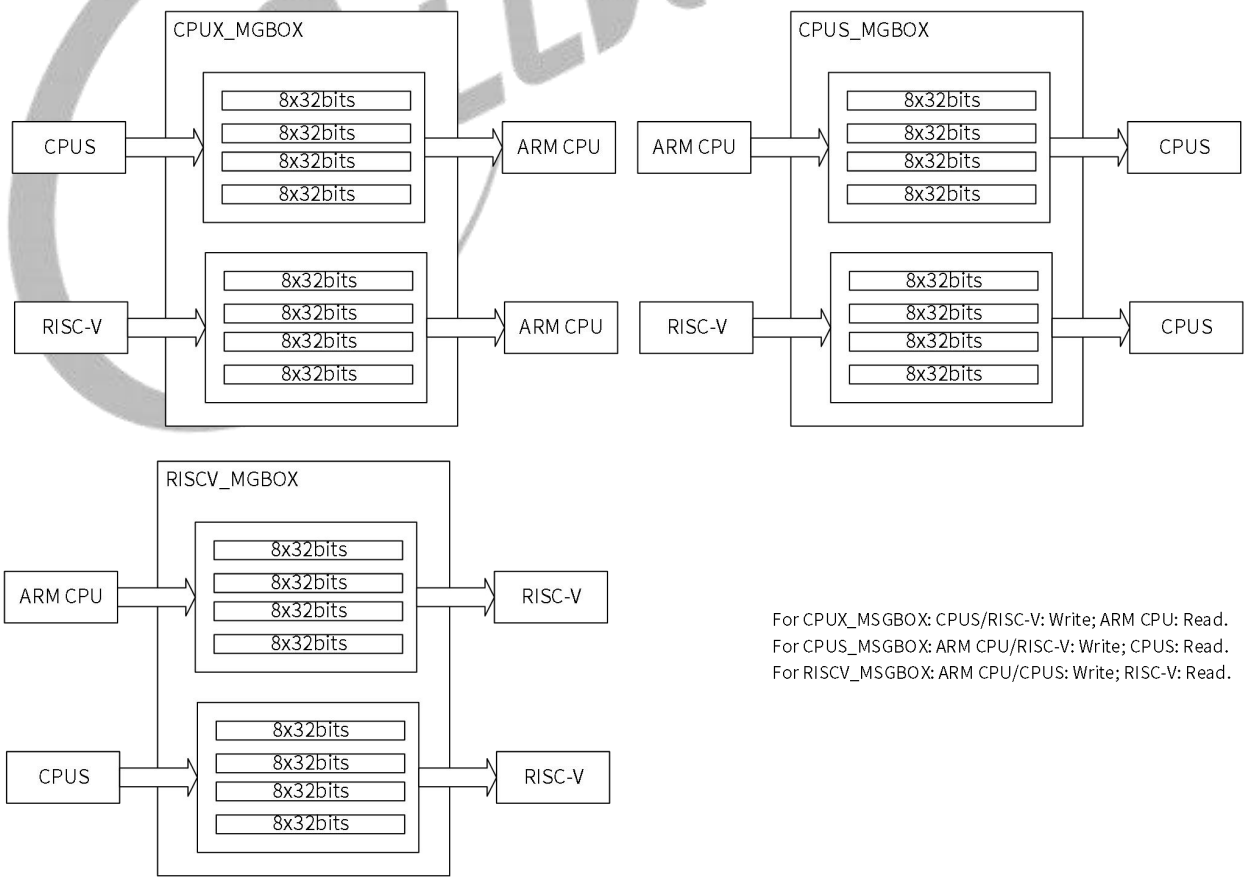
The MSGBOX has the following features:

- Supports communication between two CPUs through one way channels. Each CPU has one MSGBOX and can only read or write in one communication
  - CPUX_MSGBOX: CPUS/RISC-V write; ARM CPU read
  - CPUS_MSGBOX: ARM CPU/RISC-V write; CPUS read
  - RISCV_MSGBOX: ARM CPU/CPUS write; RISC-V read
- The channel between two CPU has 4 channels, and the FIFO depth of a channel is 8 x 32 bits
- Supports interrupts

2.10.2 Block Diagram

The following figure shows the block diagram of the message box.

Figure 2-22 Message Box Block Diagram



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Each CPU has 4 channels. The two channels can be configured to be secure by software, the other two channels can be configured to be non-secure by software. The two secure channels or two non-secure channels can be configured as one synchronous box (Sending a message requires a response) or one asynchronous box (Sending a message does not require a response).

2.10.3 Functional Description

2.10.3.1 Clock and Reset

The MSGBOX is mounted on AHB. Before accessing the MSGBOX registers, you need to de-assert the MSGBOX reset signal on AHB bus and then open the MSGBOX gating signal on AHB bus.

2.10.3.2 Transmitter/Receiver Mode

At the same channel, user1 is fixed as transmitter, user0 is fixed as receiver.

2.10.3.3 Typical Application

Several masters can build communication by configuring the MSGBOX. The communication parties have 4 channels. In a channel, the user1 is fixed as the transmitter and the user0 is fixed as the receiver. During the communication process, the current status can be judged through the interrupt or FIFO status.

2.10.3.4 Interrupt

Each channel can configure indepedently the interrupt enable bit, a read interrupt will be generated when the channel is empty, a write interrupt will be generated when the channel is non-full. For each CPU, all channels generate a read interrupt together, that is, if only a channel is non-full, the read interrupt will be generated, this channel can be obtained by quering the interrupt status register.

2.10.3.5 FIFO Status

When channel FIFO is non-full, the FIFO_NOT_AVA_FLAG is 0, at the moment the FIFO can be written.

When channel FIFO is full, the FIFO_NOT_AVA_FLAG is 1, at the moment if FIFO is written again, the first data of FIFO can be covered.

See MSGBOX_FIFO_STATUS_REG for FIFO status.

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2.10.4 Programming Guidelines

2.10.4.1 Checking the Transfer Status via the Interrupt

Follow the steps below to check the transfer status:

Step 1 Enable the interrupt for the channel: Configure the interrupt enable bits of transmitter/receiver through MSGBOX_WR_IRQ_EN_REG/MSGBOX_RD_IRQ_EN_REG. (user0: RX interrupt enable; user1: TX interrupt enable)

Step 2 Check the IRQ status of the corresponding queue through MSGBOX_WR_IRQ_STATUS_REG/MSGBOX_RD_IRQ_STATUS_REG.

- If the FIFO is not full, the channel generates a transmission interrupt to remind the transmitter to transmit data. Write data to the FIFO in the interrupt handler, then clear the pending bit of the transmitter in MSGBOX_WR_IRQ_STATUS_REG and the enable bit of the transmitter in MSGBOX_WR_IRQ_EN_REG.
- If the FIFO has new data, the channel generates a reception interrupt to remind the receiver to receive data. Read data from the FIFO in interrupt handler, then clear the pending bit of the receiver in MSGBOX_RD_IRQ_STATUS_REG and the enable bit of the receiver in MSGBOX_RD_IRQ_EN_REG.

2.10.4.2 Checking the Transfer Status via the FIFO

Follow the steps below to check the FIFO status of the corresponding queue:

- If the FIFO is not full, the transmitter fills the FIFO to 8*32 bits.
- If the FIFO is full, the receiver reads the FIFO data, and reads MSGBOX_FIFO_STATUS_REG to acquire the current FIFO data amount and the FIFO data amount before reading, which means no data is dropped.

2.10.4.3 Transmitting/Receiving Message

The following figure shows the communication process between CPUX_MSGBOX and CPUS_MSGBOX.

CPUX_MSGBOX: Receiving message

CPUS_MSGBOX: Transmitting message

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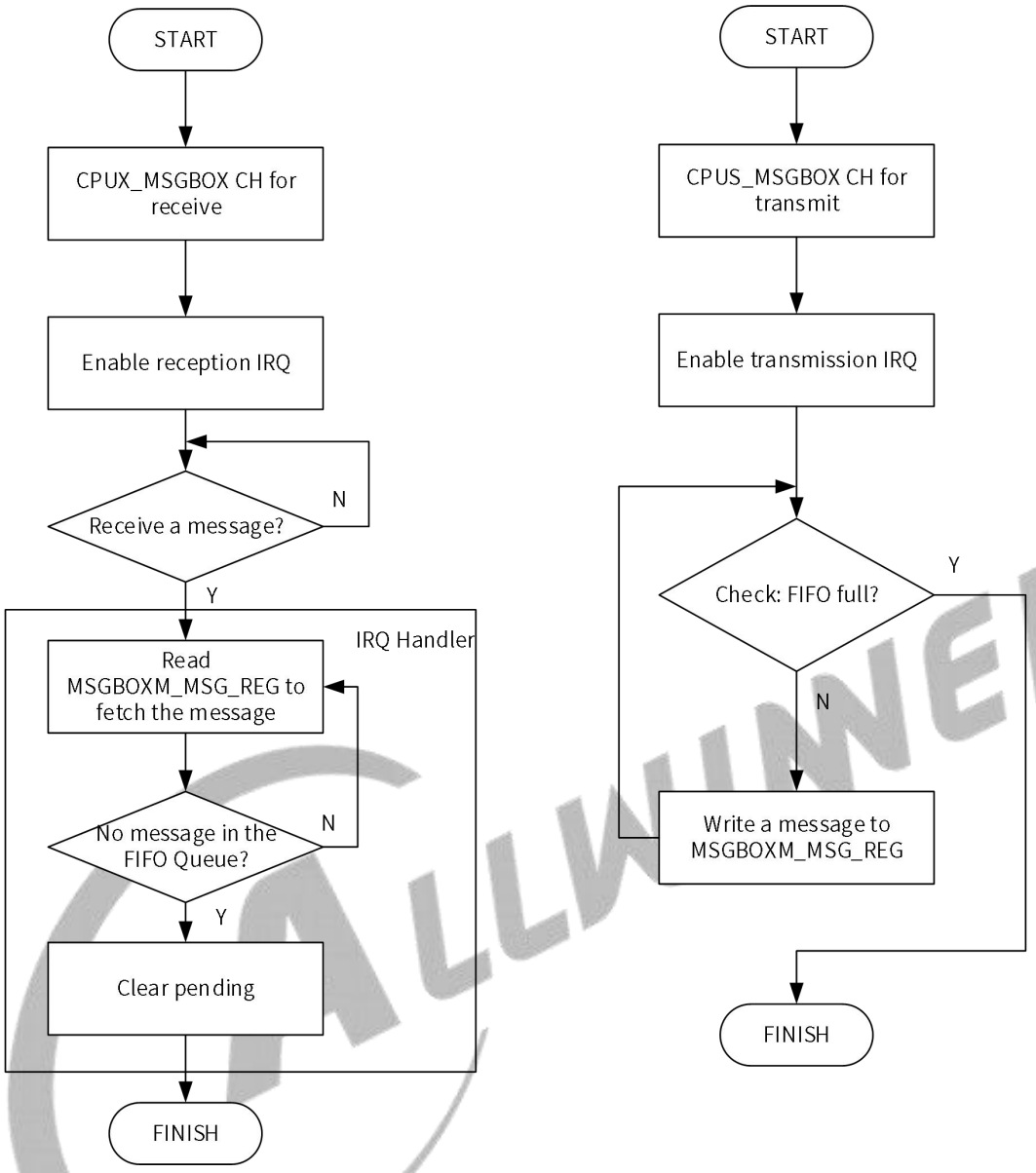
Figure 2-23 The Communication Process between CPUX_MSGBOX and CPUS_MSGBOX



2.10.5 Register List

Module Name	Base Address
CPUX_MSGBOX	0x0300 3000
CPUS_MSGBOX	0x0709 4000
RISCV_MSGBOX	0x0713 6000

Parameter	Description	Value
N	The CPU numbers that communicates with the current CPU	0 or 2
P	The channel numbers between two communication CPU	0-3

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MSGBOX	CPU	The Value of N
CPUX_MSGBOX	CPUS->CPUX	N=0
CPUX_MSGBOX	RISCV->CPUX	N=2
CPUS_MSGBOX	CPUX->CPUS	N=0
CPUS_MSGBOX	RISCV->CPUS	N=2
RISCV_MSGBOX	CPUS->RISCV	N=0
RISCV_MSGBOX	CPUX->RISCV	N=2

Register Name	Offset	Description
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100(N=0, 2)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100(N=0, 2)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100(N=0, 2)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100(N=0, 2)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100(N=0, 2)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004(N=0, 2)(P=0-3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004(N=0, 2)(P=0-3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004(N=0, 2)(P=0-3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESHOLD_REG	0x0080+N*0x0100+P*0x0004(N=0, 2)(P=0-3)	MSGBOX Write IRQ Threshold Register

2.10.6 Register Description

2.10.6.1 0x0020+N*0x0100(N=0, 2) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020+N*0x0100(N=0, 2)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN Reception Channel3 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 3 has received a new message.)
5	/	/	/

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Offset: 0x0020+N*0x0100(N=0, 2)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN Reception Channel2 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 2 has received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN Reception Channel1 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 1 has received a new message.)
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN Reception Channel0 Interrupt Enable 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

2.10.6.2 0x0024+N*0x0100(N=0, 2) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0024+N*0x0100(N=0, 2)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:3	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND Reception Channel3 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Set one to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. Reception Channel2 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Set one to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND Reception Channel1 Interrupt Pending

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Offset: 0x0024+N*0x0100(N=0, 2)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
			0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Set one to this bit will clear it.
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND Reception Channel0 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Set one to this bit will clear it.

2.10.6.3 0x0030+N*0x0100(N=0, 2) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x0100(N=0, 2)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN Transmit Channel3 Interrupt Enable. 0: Disable 1: Enable (It will notify user 1 by interrupt when Message Queue 3 empty level reach the configured threshold.)
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN Transmit Channel2 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 2 empty level reach the configured threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN Transmit Channel1 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 1 empty level reach the configured threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN Transmit Channel0 Interrupt Enable 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue

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Offset: 0x0030+N*0x0100(N=0, 2)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	R/W	Default/Hex	Description
			0 empty level reach the configured threshold.)
0	/	/	/

2.10.6.4 0x0034+N*0x0100(N=0, 2) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0034+N*0x0100(N=0, 2)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	R/W	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND Transmit Channel3 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configured threshold. Set one to this bit will clear it.
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND Transmit Channel2 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configured threshold. Set one to this bit will clear it.
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND Transmit Channel1 Interrupt Pending 0: No effect 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configured threshold. Set one to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND Transmit Channel0 Interrupt Pending 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configured threshold. Set one to this bit will clear it.
0	/	/	/

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2.10.6.5 0x0040+N*0x0100(N=0, 2) MSGBOX Debug Register (Default Value: 0x0000_0000)

Offset: 0x0040+N*0x0100(N=0, 2)			Register Name: MSGBOX_DEBUG_REG
Bit	R/W	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0x0	FIFO_CTRL FIFO Control MQ [7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE Debug Mode In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

2.10.6.6 0x0050+N*0x0100+P*0x0004(N=0, 2) (P=0-3) MSGBOX FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050+N*0x0100+P*0x0004(N=0, 2)(P=0-3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	R/W	Default/Hex	Description
31: 1	/	/	/
0	R	0x0	FIFO_NOT_AVA_FLAG FIFO is not available flag 0: The Message FIFO queue empty level is not reached the configured threshold. 1: The Message FIFO queue empty level reached the configured threshold. This FIFO status register has the status related to the message queue.

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2.10.6.7 0x0060+N*0x0100+P*0x0004(N=0, 2) (P=0-3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset: 0x0060+N*0x0100+P*0x0004(N=0, 2)(P=0-3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	MSG_NUM Message Number Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001-1111:/

2.10.6.8 0x0070+N*0x0100+P*0x0004(N=0, 2) (P=0-3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset: 0x0070+N*0x0100+P*0x0004(N=0, 2)(P=0-3)			Register Name: MSGBOX_MSG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	MSG_QUE The message register stores the next to be read message of the message FIFO queue. Reads remove

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Offset: 0x0070+N*0x0100+P*0x0004(N=0, 2)(P=0-3)			Register Name: MSGBOX_MSG_REG
Bit	R/W	Default/Hex	Description
			the message from the FIFO queue.

2.10.6.9 0x0080+N*0x0100+P*0x0004(N=0, 2) (P=0-3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0080+N*0x0100+P*0x0004(N=0, 2)(P=0-3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Configure the FIFO empty level to trigger the write interrupt for user1. 00: 1 01: 2 10: 4 11: 8

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2.11 Power Reset Clock Management (PRCM)

2.11.1 Overview

The Power Reset Clock Management (PRCM) module is one of the most import design aspects in this system. It provides a versatile supporting multiple power-management techniques. And it also manages the gating and enabling of the clocks to the device modules.

The system-level reset management provides correct reset routing and sequencing when one or more devices are stacked together in the same package. The device-level reset management provides reset routing to relevant devices, such as CPUS_TIMER, S_UART and so on.

The PRCM has the following features:

- Two PRCMs in CPUS domain: PRCM and MCU_PRCM
- 1 PLL
- CPUS Clock Configuration
- APBS Clock Configuration
- CPUS Module Clock Configuration
- CPUS Module BUS Gating and Reset
- RAM configure Control for PRCM

NOTE

- There are 15 PLLs in A523. 10 PLLs in CCU, 4 PLLs in CPUX system, and 1 PLL in MCU_PRCM.
- PRCM describes module clocks in CPUS domain.
- For clock description of CPUX system, please refer to section 2.2.3.2 CPU PLL Distribution and Clock Sources.
- For module clocks in CPUX domain (excluding the clocks of CPUX system.), please refer to section 2.5 Clock Controller Unit (CCU).

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2.11.2 Functional Description

2.11.2.1 System Bus Tree

The following figures show the diagram of the System Bus Tree.

Figure 2-24 System Bus Tree of PRCM

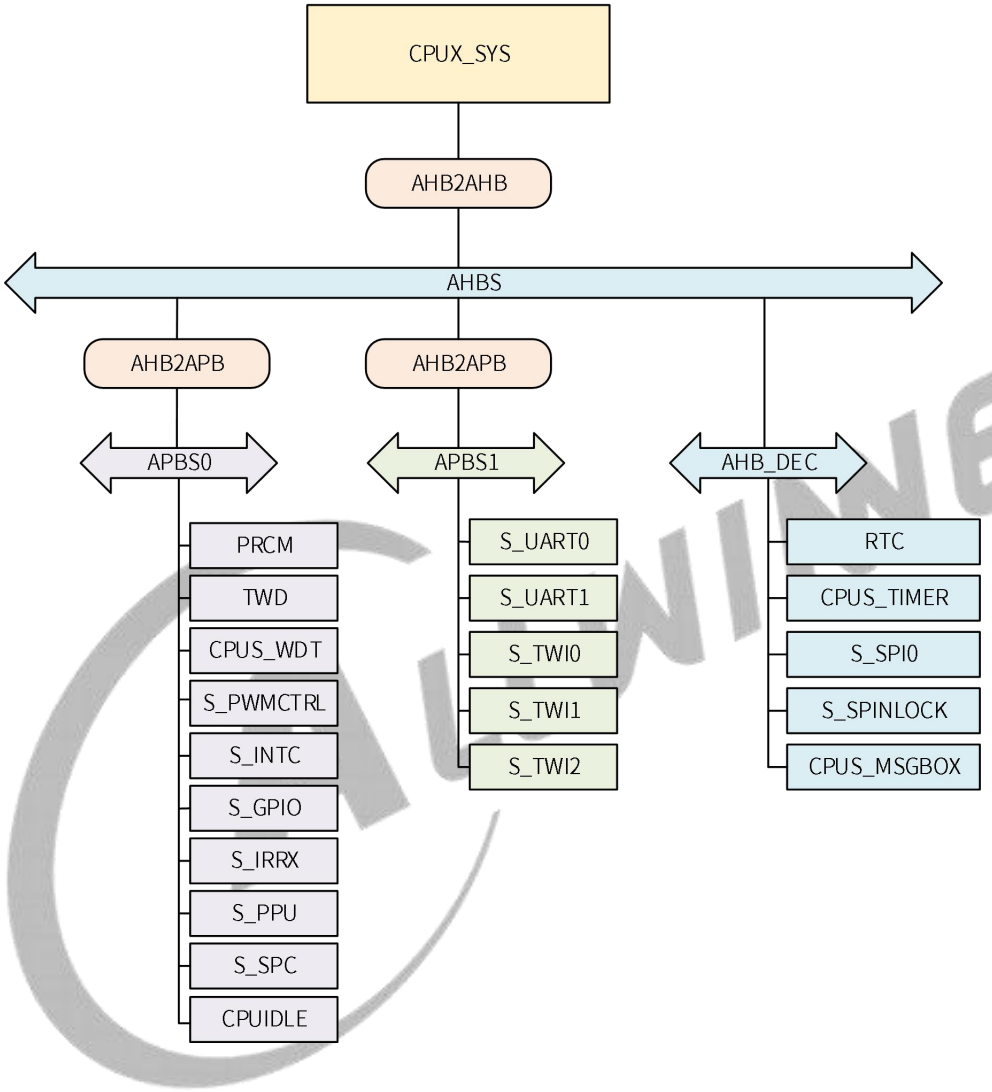

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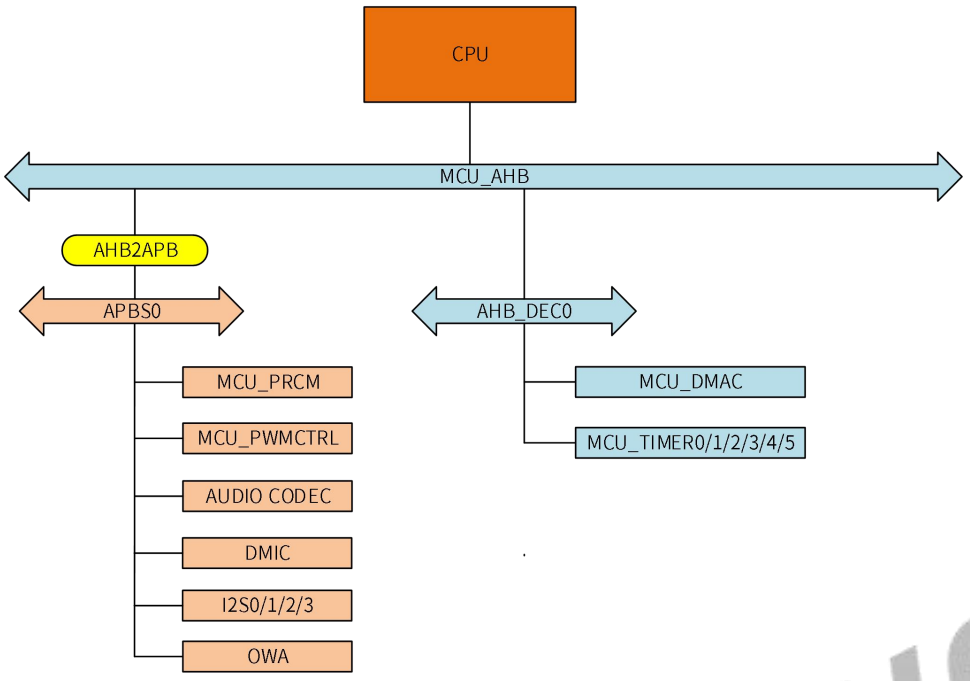
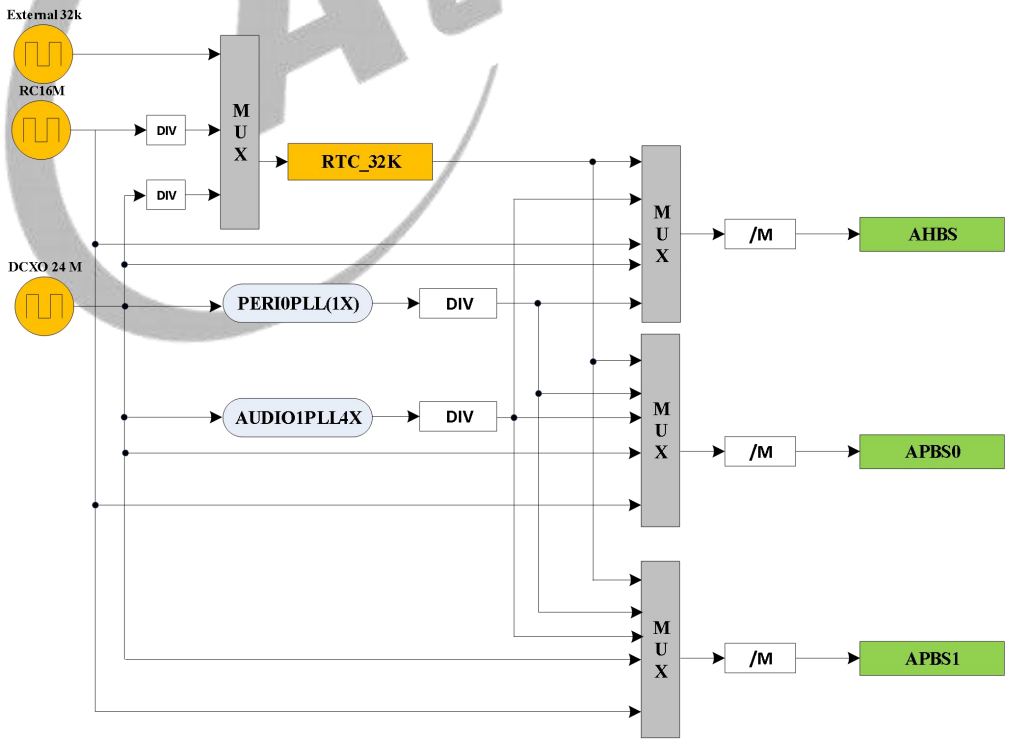
Figure 2-25 System Bus Tree of MCU_PRCM



2.11.2.2 Bus Clock Tree

The following figures show a block diagram of the clock tree Diagram in CPUS domain.

Figure 2-26 Bus Clock Tree



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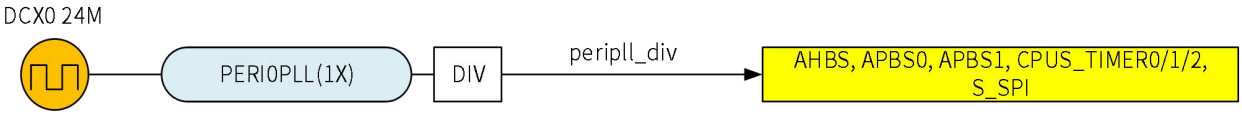
2.11.2.3 PLL Distribution

The following figures show the block diagram of the PLL distribution.

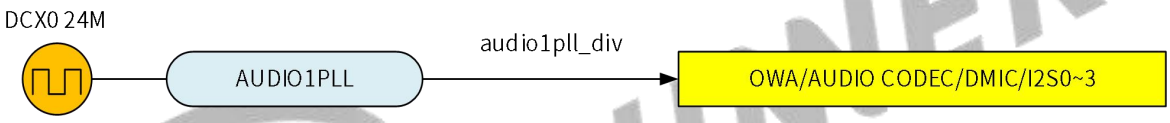
Figure 2-27 PLL Distribution of PRCM



NOTE

PERI0PLL(1X) is PERI0_600M = PERI0PLL2X/2. For detailed information of PLL_PERI0, see section 2.5.3.3 PLL Features.

Figure 2-28 PLL Distribution of MCU_PRCM



2.11.2.4 PLL Features

The following table shows the PLL features.

Table 2-18 PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Pk-Pk	Lock Time
PLL_AUDIO1	1.52 GHz-3.1GHz	Integer mode: 1/2x: 1.536 GHz 1/5x: 614.4 MHz Decimal mode: 1/2x: 1.1179648 GHz 1/5x: 471.8592 MHz	**Yes**	No	< 200ps	500us

2.11.3 Programming Guidelines

2.11.3.1 Enabling the PLL

Follow the steps below to enable the PLL:

Step 1 Configure the N, M, and P factors of the PLL control register.

Step 2 Write 1 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register, write 0 to the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register.

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Step 3 Write 1 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

Step 4 Wait for the status of the Lock to change to 1.

Step 5 Delay 20 us.

Step 6 Write the PLL_OUTPUT_GATE bit (bit [27]) of the PLL control register to 1 and then the PLL will be available.

2.11.3.2 Configuring the Frequency of PLL_AUDIO1

The frequency configuration formula of PLL_AUDIO1:

PLL_AUDIO1 = 24 MHz*N/M0/M1/P

PLL_AUDIO1 does not support dynamic adjustment because changing any parameter of N, M0, M1, and P will affect the normal work of PLL, and the PLL will need to be relocked.

Generally, PLL_AUDIO1 only needs two frequency points: 24.576*4 MHz or 22.5792*4 MHz. For these two frequencies, there are usually special recommended matching factors. To implement the desired frequency point of PLL_AUDIO1, you need to use the decimal frequency-division function, so follow the steps below:

Step 1 Configure the N, M0, M1 and P factors.

Step 2 Write 1 to the PLL_SDM_EN bit (bit [24]) of PLL_AUDIO1_CTRL register.

Step 3 Configure PLL_AUDIO1_PAT0_CTRL register to enable the digital spread spectrum.

Step 4 Write 0 and then write 1 to the LOCK ENABLE bit (bit [29]) of PLL_AUDIO1_CTRL register.

Step 5 Write 1 to the LOCK bit (bit [28]) of PLL_ AUDIO1_CTRL register.

End

NOTE

When the P factor of PLL_AUDIO1 is an odd number, the clock output is an unequal-duty-cycle signal.

2.11.3.3 Disabling the PLL

Follow the steps below to disable the PLL:

Step 1 Write 0 to the PLL_EN bit (bit [31]) and the PLL_LDO_EN bit (bit [30]) of the PLL control register.

Step 2 Write 0 to the LOCK_ENABLE bit (bit [29]) of the PLL control register.

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2.11.3.4 Implementing Spread Spectrum

The spread spectrum technology is to convert a narrowband signal into a wideband signal. It helps to reduce the effect of electromagnetic interference (EMI) associated with the fundamental frequency of the signal.

For the general PLL frequency, the calculation formula is as follows:

$$f = \frac{N+1+X}{P\cdot(M0+1)\cdot(M1+1)}\cdot 24MHz,\ 0<X<1$$

Where,

P is the frequency division factor of module or PLL;

M0 is the post-frequzency division factor of PLL;

M1 is the pre-frequency division factor of PLL;

N is the frequency doubling factor of PLL;

X is the amplitude coefficient of the spread spectrum.

The parameters N, P, M1, and M0 are for the frequency division.

When M1 = 0, M0 = 0, and P = 1 (no frequency division), the calculation formula of PLL frequency can be simplified as follows:

$$f = (N+1+X)\cdot 24MHz,\ 0<X<1$$

$$[f_1, f_2] = (N+1+[X_1, X_2])\cdot 24MHz$$

$$SDM\_BOT = 2^{17}\cdot X_1$$

$$\text{WAVE\_STEP} = 2^{17}\cdot(X_2 - X_1)/(24\ \text{MHz}\ /PREQ)\cdot 2$$

Where, SDM_BOT and WAVE_STEP are bits of the PLL pattern control register, and PREQ is the frequency of the spread spectrum.

Follow the steps below to implement the spread spectrum:

Step 1 Configure the control register of the corresponding PLL

a) Calculate the factor N and decimal value X according to the PLL frequency and PLL frequency formula. Refer to the control register of the corresponding PLL (named PLL_xxx_CTRL_REG, where xxx is the module name) in 3.3.6 Register Description for the corresponding PLL frequency formula.

b) Write M0, M1, N, and PLL frequency to the PLL control register.

c) Configure the PLL_SDM_EN bit (bit [24]) of the PLL control register to 1 to enable the spread spectrum function.

Step 2 Configure the pattern control register of the corresponding PLL

a) Calculate the SDM_BOT and WAVE_STEP of the pattern control register according to decimal value X and spread spectrum frequency (the bit [18:17] of the PLL pattern register)

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b) Configure the spread spectrum mode (SPR_FREQ_MODE) to 2 or 3.

c) If the PLL_INPUT_DIV2 of the PLL control register is 1, configure the spread spectrum clock source select bit (SDM_CLK_SEL) of the PLL pattern control register to 1. Otherwise, configure SDM_CLK_SEL to the default value 0.

d) Write SDM_BOT, WAVE_STEP, PREQ, SPR_FREQ_MODE, and SDM_CLK_SEL to the PLL pattern control register, and configure the SIG_DELT_PAT_EN bit (bit[31]) of this register to 1.

Step 3 Delay 20 us

2.11.3.5 Configuring Bus Clock

The bus clock supports dynamic switching, but the process of switching needs to follow the following two rules.

- From a higher frequency to a lower frequency: switch the clock source first, and then set the frequency division factor;
- From a lower frequency to a higher frequency: configure the frequency division factor first, and then switch the clock source.

The typical bus frequency for each bus in PRCM and MCU_PRCM is as follows:

- AHBS: 200 MHz
- APBS0: 100 MHz
- APBS1: 24 MHz

2.11.3.6 Configuring Module Clock

For the Bus Gating Reset register of a module, the reset bit is de-asserted first, and then the clock gating bit is enabled to avoid potential problems caused by the asynchronous release of the reset signal.

For all module clocks except the DDR clock, configure the clock source and frequency division factor first, and then release the clock gating (that is, set to 1). For the configuration order of the clock source and frequency division factor, follow the rules below:

- With the increasing of the clock source frequency, configure the frequency division factor before the clock source.
- With the decreasing of the clock source frequency, configure the clock source before the frequency division factor.

2.11.4 Register List

PRCM module includes two groups of registers:

Module Name	Base Address

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Module Name	Base Address
PRCM	0x0701 0000
MCU_PRCM	0x0710 2000

2.11.4.1 PRCM Register List

Module Name	Base Address
PRCM	0x0701 0000

Register Name	Offset	Description
AHBS_CFG_REG	0x0000	AHBS Configuration Register
APBS0_CFG_REG	0x000C	APBS0 Configuration Register
APBS1_CFG_REG	0x0010	APBS1 Configuration Register
CPUS_TIMER0_CLK_REG	0x0100	CPUS_TIMER0 Clock Register
CPUS_TIMER1_CLK_REG	0x0104	CPUS_TIMER1 Clock Register
CPUS_TIMER2_CLK_REG	0x0108	CPUS_TIMER2 Clock Register
CPUS_TIMER_BGR_REG	0x011C	CPUS_TIMER Bus Gating Reset Register
S_TWD_BGR_REG	0x012C	S_TWD Bus Gating Reset Register
S_PWMCTRL_CLK_REG	0x0130	S_PWMCTRL Clock Register
S_PWMCTRL_BGR_REG	0x013C	S_PWMCTRL Bus Gating Reset Register
S_SPI_CLK_REG	0x0150	S_SPI Clock Register
S_SPI_BGR_REG	0x015C	S_SPI Bus Gating Reset Register
S_SPINLOCK_BGR_REG	0x016C	S_SPINLOCK Bus Gating Reset Register
CPUS_MSGBOX_BGR_REG	0x017C	CPUS_MSGBOX Bus Gating Reset Register
S_UART_BGR_REG	0x018C	S_UART Bus Gating Reset Register
S_TWI_BGR_REG	0x019C	S_TWI Bus Gating Reset Register
S_PPU_BGR_REG	0x01AC	S_PPU Bus Gating Reset Register
S_CPUS_BIST_BGR_REG	0x01BC	S_CPUS_BIST Bus Gating Reset Register
S_IRRX_CLK_REG	0x01C0	S_IRRX Clock Register
S_IRRX_BGR_REG	0x01CC	S_IRRX Bus Gating Reset Register
DMA_ADB400_CLKEN_REG	0x01DC	DMA ADB400 Gating Register
RTC_BGR_REG	0x020C	RTC Bus Gating Reset Register
S_CPUCFG_BGR_REG	0x022C	S_CPUCFG Bus Gating Reset Register
PLL_CTRL_REG0	0x0240	PLL Control Register 0
PLL_CTRL_REG1	0x0244	PLL Control Register 1
VDD_SYS_PWROFF_GATING_REG	0x0250	VDD_SYS Power Off Gating Register
ANA_PWR_RST_REG	0x0254	Analog Power Off Gating Register
VDD_SYS_PWR_RST_REG	0x0260	VDD_SYS Power Domain Reset Register
MCU_SYS_PWR_RST_REG	0x0264	MCU_SYS Power Domain Reset Register
RAM1P_CFG_REG	0x0270	RAM1P Configuration Register
RAM2P_CFG_REG	0x0274	RAM2P Configuration Register

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Register Name	Offset	Description
RAMSP_CFG_REG	0x0278	RAMSP Configuration Register
ROM_CFG_REG	0x027C	ROM Configuration Register
NMI_INT_CTRL_REG	0x0320	NMI Interrupt Control Register
NMI_INT_EN_REG	0x0324	NMI Interrupt Enable Register
NMI_INT_PEND_REG	0x0328	NMI Interrupt Pending Register
DEV_BUS_AUTOG_CTRL_REG	0x0338	DEV_BUS_AUTOG_CTRL_REG Register
BUS_ACG_REG	0x033C	Bus Auto Clock Gating Register
MSRAMOC_CTRL_REG	0x0360	MSRAMOC Control Register
REMAP_CTRL_REG	0x0364	REMAP Control Register
AHBS_RDY_TOUT_CTRL_REG	0x0368	AHBS Ready Timeout Control Register
CPUS_DEV_DMA_SEL_REG	0x0370	CPUS Device DMA Configuration Register
CRY_CONFIG_REG	0x03E0	Crypt Configuration Register
CRY_KEY_REG	0x03E4	Crypt Key Register
CRY_EN_REG	0x03E8	Crypt Enable Register

2.11.4.2 MCU_PRCM Register List

Module Name	Base Address
MCU_PRCM	0x0710 2000

Register Name	Offset	Description
PLL_CTRL_REG0	0x0000	PLL Control Register0
PLL_CTRL_REG1	0x0004	PLL Control Register 1
PLL_AUDIO1_CTRL_REG	0x000C	PLL_AUDIO1 Control Register
PLL_AUDIO1_PAT0_CTRL_REG	0x0010	PLL_AUDIO1 Pattern0 Control Register
PLL_AUDIO1_PAT1_CTRL_REG	0x0014	PLL_AUDIO1 Pattern1 Control Register
PLL_AUDIO1_BIAS_REG	0x0018	PLL_AUDIO1 Bias Register
AUD_CLK_REG	0x001C	Audio Out Clock Register
I2S0_CLK_REG	0x002C	I2S0 Clock Register
I2S1_CLK_REG	0x0030	I2S1 Clock Register
I2S2_CLK_REG	0x0034	I2S2 Clock Register
I2S3_CLK_REG	0x0038	I2S3 Clock Register
I2S3_ASRC_CLK_REG	0x003C	I2S3_ASRC Clock Register
I2S_BGR_REG	0x0040	I2S Bus Gating Reset Register
OWA_TX_CLK_REG	0x0044	OWA_TX Clock Register
OWA_RX_CLK_REG	0x0048	OWA_RX Clock Register
OWA_BGR_REG	0x004C	OWA Bus Gating Reset Register
DMIC_CLK_REG	0x0050	DMIC Clock Register
DMIC_BGR_REG	0x0054	DMIC Bus Gating Reset Register
AUDIO_CODEC_DAC_CLK_REG	0x0058	AUDIO_CODEC_DAC Clock Register

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Register Name	Offset	Description
AUDIO_CODEC_ADC_CLK_REG	0x005C	AUDIO_CODEC_ADC Clock Register
AUDIO_CODEC_BGR_REG	0x0060	AUDIO_CODEC Bus Gating Reset Register
AHBS_RDY_TOUT_CTRL_REG	0x0064	AHBS Ready Timeout Control Register
MCU_TIMER0_CLK_REG	0x0074	MCU_TIMER0 Clock Register
MCU_TIMER1_CLK_REG	0x0078	MCU_TIMER1 Clock Register
MCU_TIMER2_CLK_REG	0x007C	MCU_TIMER2 Clock Register
MCU_TIMER3_CLK_REG	0x0080	MCU_TIMER3 Clock Register
MCU_TIMER4_CLK_REG	0x0084	MCU_TIMER4 Clock Register
MCU_TIMER5_CLK_REG	0x0088	MCU_TIMER5 Clock Register
MCU_TIMER_BUS_BGR_REG	0x008C	MCU_TIMER Bus Gating Reset Register
MCU_DMAC_BGR_REG	0x0104	MCU_DMAC Bus Gating Reset Register
PUBSRAM_BGR_REG	0x0114	PUBSRAM Bus Gating Reset Register
AHBS1_RDY_TOUT_CTRL_REG	0x0118	AHBS1 Ready Timeout Control Register
MCLK_GATING_CFG_REG	0x011C	MCLK Gating Configuration Register
RISCV_CLK_REG	0x0120	RISCV Clock Register
RISCV_CFG_BGR_REG	0x0124	RISCV Configuration Bus Gating Reset Register
RISCV_MSGBOX_BGR_REG	0x0128	RISCV MSGBOX Bus Gating Reset Register
MCU_PWMCTRL_CLK_REG	0x0130	MCU_PWMCTRL Clock Register
MCU_PWMCTRL_BGR_REG	0x0134	MCU_PWMCTRL Bus Gating Reset Register
PLL_BACKDOOR_OUTPUT_EN_REG	0x0160	PLL Backdoor Output Enable Register
TEST_DBG_REG	0x0164	Test Debug Register

2.11.5 PRCM Register Description

2.11.5.1 0x0000 AHBS Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AHBS_CFG_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	AHBS_CLK_SRC_SEL AHBS Clock Source Selection 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV = PERI0PLL1X/3 100: AUDIO1PLL4X Others: / CLK = Clock Source/M
23:5	/	/	/

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Offset: 0x0000			Register Name: AHBS_CFG_REG
Bit	R/W	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.5.2 0x000C APBS0 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: APBS0_CFG_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	APBS0_CLK_SRC_SEL APBS0 Clock Source Selection 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X Others: / CLK = Clock Source/M
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.11.5.3 0x0010 APBS1 Configuration Register (Default: 0x0000_0000)

Offset: 0x0010			Register Name: APBS1_CFG_REG
Bit	R/W	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	APBS1_CLK_SRC_SEL APBS1 Clock Source Selection 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV = PERI0PLL1X/3 100: AUDIO1PLL4X Others:/ CLK = Clock Source/ M
23:5	/	/	/

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Offset: 0x0010			Register Name: APBS1_CFG_REG
Bit	R/W	Default/Hex	Description
4:0	R/W	0x0	FACTOR_M Factor M (M= FACTOR_M +1) FACTOR_M is from 0 to 31.

2.11.5.4 0x0100 CPUS_TIMER0 Clock Register (Default: 0x0000_0000)

Offset: 0x0100			Register Name: CPUS_TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL. CPUS_TIMER0 Clock Source Selection. 000: CLK24M 001: CLK32K 010: CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X CPUS_TIMER0_CLK = Clock Source / N.
3:1	R/W	0x0	CPUS_TIMER0_CLK_DIVN. Select the pre-scale of CPUS_TIMER0 clock source. Factor N 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	CPUS_TIMER0_CLK_GATING 0: Disable 1: Enable

2.11.5.5 0x0104 CPUS_TIMER1 Clock Register (Default: 0x0000_0000)

Offset: 0x0104			Register Name: CPUS_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL CPUS_TIMER1 Clock Source Selection 000: CLK24M

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Offset: 0x0104			Register Name: CPUS_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
			001: CLK32K 010:CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X CPUS_TIMER1_CLK = Clock Source/N
3:1	R/W	0x0	CPUS_TIMER1_CLK_DIVN Select the pre-scale of CPUS_TIMER1 clock source. Factor N 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	CPUS_TIMER1_CLK_GATING 0: Disable 1: Enable

2.11.5.6 0x0108 CPUS_TIMER2 Clock Register (Default: 0x0000_0000)

Offset: 0x0108			Register Name: CPUS_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	CLK_SRC_SEL CPUS_TIMER2 Clock Source Selection 000: CLK24M 001: CLK32K 010:CLK_RC 011: PERIPLL_DIV=PERI0PLL1X/3 100: AUDIO1PLL4X CPUS_TIMER2_CLK = Clock Source/N
3:1	R/W	0x0	CPUS_TIMER2_CLK_DIVN Select the pre-scale of CPUS_TIMER2 clock source. Factor N 000: /1 001: /2 010: /4 011: /8 100: /16

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Offset: 0x0108			Register Name: CPUS_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
			101: /32 110: /64 111: /128
0	R/W	0x0	CPUS_TIMER2_CLK_GATING 0: Disable 1: Enable

2.11.5.7 0x011C CPUS_TIMER BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: CPUS_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUS_TIMER_RST CPUS_TIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUS_TIMER_GATING Gating Clock for CPUS_TIMER 0: Mask 1: Pass

2.11.5.8 0x012C S_TWD BUS GATING RESET Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: S_TWD_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	S_TWD_GATING Gating Clock for S_TWD 0: Mask 1: Pass

2.11.5.9 0x0130 S_PWMCTRL Clock Register (Default: 0x0000_0000)

Offset: 0x0130			Register Name: S_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	S_PWMCTRL_CLK_GATING Gating Special Clock 0: Clock is OFF

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Offset: 0x0130			Register Name: S_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description
			1: Clock is ON S_PWMCTRL_CLK = Clock Source
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 00: CLK24M 01: CLK32K 10: CLK_RC 11:/ CLK32K is generated by calibrated CLK_RC or external low speed crystal. For more information, please refer to section 2.12 RTC.
23:0	/	/	/

2.11.5.10 0x013C S_PWMCTRL BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x013C			Register Name: S_PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_ PWMCTRL _RST S_ PWMCTRL Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_ PWMCTRL _GATING Gating bus Clock for S_ PWMCTRL 0: Mask 1: Pass

2.11.5.11 0x0150 S_SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: S_SPI0_CLK_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON R_SPI_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	SPI_CLK_SRC_SEL

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Offset: 0x0150			Register Name: S_SPI0_CLK_REG
Bit	R/W	Default/Hex	Description
			SPI Clock Source Selection 000: CLK24M 001: PERIPLL_DIV=PERI0PLL1X/3 010: PERI0_300M 011: PERI1_300M 100: AUDIO1PLL4X
23:13	/	/	/
12:8	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.11.5.12 0x015C S_SPI0 BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x015C			Register Name: S_SPI0_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_SPI0_RST S_SPI0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_SPI0_GATING Gating Clock for S_SPI0 0: Mask 1: Pass

2.11.5.13 0x016C S_SPINLOCK BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x016C			Register Name: S_SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_SPINLOCK_RST S_SPINLOCK Reset 0: Assert

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Offset: 0x016C			Register Name: S_SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
			1: De-assert
15:1	/	/	/
0	R/W	0x0	S_SPINLOCK_GATING Gating Clock for S_SPINLOCK 0: Mask 1: Pass

2.11.5.14 0x017C CPUS_MSGBOX BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x017C			Register Name: CPUS_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	CPUS_MSGBOX_RST CPUS_MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CPUS_MSGBOX_GATING Gating Clock for CPUS_MSGBOX 0: Mask 1: Pass

2.11.5.15 0x018C S_UART BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x018C			Register Name: S_UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_UART1_RST S_UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	S_UART0_RST S_UART0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	S_UART1_GATING Gating Clock for S_UART1 0: Mask 1: Pass

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Offset: 0x018C			Register Name: S_UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	S_UART0_GATING Gating Clock for S_UART0 0: Mask 1: Pass

2.11.5.16 0x019C S_TWI BUS GATING RESET Register (Default: 0x0000_0000)

Offset: 0x019C			Register Name: S_TWI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	S_TWI2_RST S_TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	S_TWI1_RST R_TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	S_TWI0_RST R_TWI0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	S_TWI2_GATING Gating Clock for S_TWI2 0: Mask 1: Pass
1	R/W	0x0	S_TWI1_GATING Gating Clock for S_TWI1 0: Mask 1: Pass
0	R/W	0x0	S_TWI0_GATING Gating Clock for S_TWI0 0: Mask 1: Pass

2.11.5.17 0x01AC S_PPU BUS GATING RESET Register (Default Value: 0x0001_0001)

Offset: 0x01AC			Register Name: S_PPU_BGR_REG
Bit	Read/Write	Default/Hex	Description

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Offset: 0x01AC			Register Name: S_PPU_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_PPU1_RST S_PPU1 Reset 0: Assert 1: De-assert
16	R/W	0x1	Reserved
15:2	/	/	/
1	R/W	0x0	S_PPU1_GATING Gating Clock for S_PPU1 0: Mask 1: Pass
0	R/W	0x1	S_PPU_GATING Gating Clock for S_PPU(PCK600) 0: Mask 1: Pass

2.11.5.18 0x01BC S_CPUS_BIST BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: S_CPUS_BIST_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	S_CPUS_BIST_GATING Gating Clock for S_CPUS_BIST 0: Mask 1: Pass

2.11.5.19 0x01C0 S_IRRX Clock Register (Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: S_IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON S_IRRX_CLK = Clock Source/M
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 00: CLK32K 01: CLK24M

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Offset: 0x01C0			Register Name: S_IRRX_CLK_REG
Bit	Read/Write	Default/Hex	Description
			10:/ 11:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.11.5.20 0x01CC S_IRRX BUS GATING RESET Register (Default Value: 0x0000_0000)

Offset: 0x01CC			Register Name: S_IRRX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	S_IRRX_RST S_IRRX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	S_IRRX_GATING Gating Clock for S_IRRX 0: Mask 1: Pass

2.11.5.21 0x01DC DMA ADB400 GATING Register (Default Value: 0x0000_0001)

Offset: 0x01DC			Register Name: DMA_ADB400_CLKEN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	DMA_CLKEN_SW Gating Clock for DMA ADB400 MST 0: Mask 1: Pass

2.11.5.22 0x020C RTC Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: RTC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	RTC_RST

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Offset: 0x020C			Register Name: RTC_BGR_REG
Bit	Read/Write	Default/Hex	Description
			RTC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	RTC_GATING Gating Clock for RTC 0: Mask 1: Pass

2.11.5.23 0x022C S_CPUCFG Bus Gating Reset Register (Default Value: 0x0001_0001)

Offset: 0x022C			Register Name: S_CPUCFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x1	S_CPUCFG_RST S_CPUCFG Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	S_CPUCFG_GATING Gating Clock for S_CPUCFG 0: Mask 1: Pass

2.11.5.24 0x0240 PLL Control Register 0 (Default Value: 0x0000_0007)

Offset: 0x0240			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL PLL Reference Clock Selection 0: DCXO 1: External Test Clock
23:3	/	/	/
2	R/W	0x1	GM1 XTAL Gain Control Bit1
1	R/W	0x1	GM0 XTAL Gain Control Bit0
0	R/W	0x1	Reserved

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2.11.5.25 0x0244 PLL Control Register 1 (Default Value: 0x0004_0005)

Offset: 0x0244			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD Key Field for LDO Enable bit If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/
18:16	R/W	0x4	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control 000: 0.82 V 001: 0.86 V 010: 0.9 V 011: 0.94v 100: 0.98v 101: 1.02v 110: 1.06v 111: 1.10v
15:5	/	/	/
4	R/W	0x0	MBIAS_EN Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias
3	R/W	0x0	PLLTEST_EN For Verify (Back door clock PLLTEST enable) 0：Output clock is gated off. 1：Clock Output. The clock is the clock output to the PLL and the clock after frequency division through pins.
2:1	R/W	0x2	Reserved
0	R/W	0x1	LDO_EN LDO Enable 0: Disable 1: Enable Note: PLL Power enable (power source from VCC_PLL).

2.11.5.26 0X0250 VDD_SYS Power Off Gating Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	R/W	Default/Hex	Description

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Offset: 0x0250			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	R/W	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	VDD_USB2CPUS_GATING 0: Invalid 1: Valid To gate off the signal output to VDD-CPUS from USB module, set this bit to 1.
7:6	/	/	/
5	R/W	0x0	VDD_SYS2MCU_GATING Gating the corresponding modules to the MCU module when VDD-SYS powers off. 0: Invalid 1: Valid This bit should be set to 1 before VDD-SYS power off while it should be set to 0 after the VDD-SYS power on. MCU CLK Source should switch to Internal OSC or AUDIO1PLL before VDD-SYS Power Off Gating.
4	R/W	0x0	VDD_MCU2CPUS_GATING Gating the corresponding modules to the CPUS module when MCU_SYS powers off. 0: Invalid 1: Valid This bit should be set to 1 before MCU_SYS powers off while it should be set to 0 after the MCU_SYS power on.
3	R/W	0x0	VDD_SYS2USB_GATING Gating the corresponding modules to the USB module when VDD_SYS power off. 0: Invalid 1: Valid This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on. USB CLK Source should switch to Internal OSC before VDD_SYS Power Off Gating.
2	R/W	0x0	VDD_SYS2CPUS_GATING Gating the corresponding modules to the CPUS Power Domain when VDD_SYS power off. 0: Invalid 1: Valid This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on. CPUS CLK Source should switch to Internal OSC

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Offset: 0x0250			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	R/W	Default/Hex	Description
			before VDD_SYS Power Off Gating.
1	/	/	/
0	R/W	0x0	VDD_DDR_GATING 0: valid (gate valid) 1: Inalid (gate invalid) When DDR entrys into power-down (low voltage) self-refresh mode, this signal will fix CLKE to 0.

2.11.5.27 0x0254 ANALOG Power Off Gating Register (Default Value: 0x0000_0005)

Offset: 0x0254			Register Name: ANA_PWR_RST_REG
Bit	R/W	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	PWROFF_ANA_EN_CPU Gating The CPU PLL ANA Module Input When CPU_SYS Is Power Off. 0: Invalid, not gating 1: Valid, gating When system is cold start, this bit is default not gating, before using the relate ANA module, must set this bit to 0. Relate ANA module: PLL
2	R/W	0x1	PWROFF_ANA_EN_MCU Gating The MCU SYS PLL ANA Module Input When MCU_SYS Is Power Off. 0: Invalid, not gating 1: Valid, gating Note: When system is cold start, this bit is default gating, before using the related ANA module, must set this bit to 0. Related ANA module: PLL/AUDIO CODEC
1	R/W	0x0	PWROFF_ANA_EN Gating The PLL ANA Module Input When VDD Is Power Off. 0: Invalid, not gating 1: Valid, gating Note: When system is cold start, this bit is default not gating, before using the relate ANA module, must set this bit to 0. Relate ANA module: PLL
0	R/W	0x1	SYS_ANA_VDDON_CTRL

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Offset: 0x0254			Register Name: ANA_PWR_RST_REG
Bit	R/W	Default/Hex	Description
			Gating The System Domain ANA Module Input When VDD Is Power Off. 0: Invalid, not gating 1: Valid, gating Note: When system is cold start, this bit is default gating, before using the relate ANA module, must set this bit to 0. Relate ANA module: RES/RES_CAL_DCAP/GPADC/DSI/LVDS/LRADC/USB/CSI

2.11.5.28 0x0260 VDD_SYS Power Domain Reset Register (Default: 0x0000_0001)

Offset: 0x0260			Register Name: VDD_SYS_PWR_RST_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	MODULE_RST VDD_SYS Power Domain Modules should be reset before VDD_SYS power on 0: Assert 1: De-assert

2.11.5.29 0x0264 MCU_SYS Power Domain Reset Register (Default: 0x0000_0001)

Offset: 0x0264			Register Name: MCU_SYS_PWR_RST_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	MCU_SYS_RSTN MCU_SYS Power Domain Modules should be reset before MCU_SYS power on. 0: Assert 1: De-assert

2.11.5.30 0x0270 RAM1P Configuration Register (Default Value: 0x0000_0413)

Offset: 0x0270			Register Name: RAM1P_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x413	RF1P_MEM RF1P Configuration Information

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2.11.5.31 0x0274 RAM2P Configuration Register (Default Value: 0x0000_8421)

Offset: 0x0274			Register Name: RAM2P_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x8421	RF2P_MEM RF2P Configuration Information

2.11.5.32 0x0278 RAMSP Configuration Register (Default Value: 0x0000_0403)

Offset: 0x0278			Register Name: RAMSP_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x403	SRAM_MEM SRAM Configuration Information

2.11.5.33 0x027C ROM Configuration Register (Default Value: 0x0000_0015)

Offset: 0x027C			Register Name: ROM_CFG_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x15	ROM_MEM ROM Configuration Information

2.11.5.34 0x0320 NMI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: NMI_INT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	NMI_SRC_TYPE External NMI Interrupt Source Type 00: Low level sensitive 01: Negative edge trigged 10: High level sensitive 11: Positive edge sensitive

2.11.5.35 0x0324 NMI Interrupt Enable Register (Default Value: 0x8000_0000)

Offset: 0x0324			Register Name: NMI_INT_EN_REG
Bit	R/W	Default/Hex	Description
31	R/W	0x1	NMI_INPUT_DET_EN NMI Input Detect Enable 0: Disable 1:Enable

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Offset: 0x0324			Register Name: NMI_INT_EN_REG
Bit	R/W	Default/Hex	Description
30:1	/	/	/
0	R/W	0x0	NMIIRQ_SYS_EN Interrupt NMI for CPUX Enable Bits 0: Interrupt is disabled. 1: Interrupt is enabled.

2.11.5.36 0x0328 NMI Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: NMI_INT_PEND_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	NMI_IRQ_PEND NMI IRQ Pending Interrupt NMI Pending/Clear Bit. Set 1 to the bit will clear it. (after first enabling NMI IRQ function, must set this bit to 1 to clear the unexpected pending once) 0: Corresponding interrupt is not pending 1: Corresponding interrupt is pending

2.11.5.37 0x0338 DEV_BUS_AUTOG_CTRL Register（Default Value：0x0000_0000

Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	CPUCLK_REC_DLY_TIME This bit indicates the delay time needed to respond to CPUS clock after respinding to peripherals and bus clocks, when exiting LP mode. The unit is PRCM clock. 0=256 cycle 1=1 cycle ..... 255=255 cycle
23:21	/	/	/
20	R/W	0x0	LPI_OUT_SYNC_EN LPI Interface from CPUS to PRCM Enable 0: CPUS clock is synchronous with PRCM clock. 1: CPUS clock is asynchronous with PRCM clock.
18:12	/	/	/
11	R/W	0x0	LPI_IF_EN

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Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL
Bit	R/W	Default/Hex	Description
			LPI Interfece Between CPUS and PRCM Enable 0: Disable 1: Enable When LPI is disabled, CPUS status will not be routed to PRCM.
10	R/W	0x0	LPI_IN_SYNC_EN LPI Interface from PRCM to CPUS Enable 0: CPUS clock is synchronous with PRCM clock. 1: CPUS clock is asynchronous with PRCM clock.
9	R/W	0x0	TT_AUTOGATE_EN CPUS Ticktimer Auto Gating Enbale When this bit is enabled and PM_TT_O is high, the ticktimer clock will be gated on automatically.
8	R/W	0x0	CPU_ICACHE_AUTOGATE_EN Clock (excludes ticktimer clock) Auto Gating Enable 0: Auto gating is disabled. 1: Auto gating is enabled. When this bit is enabled and both of PM_CPU_O and PM_ICACHE_O are high simultaneously, the clocks of CPUS, ICACHE, QMEM, and PM will be gated on automatically.
7	R	0x0	PM_TT_STAT CPUS LP Interface Status 0: CPUS is in normal mode and the ticktimer clock is disable to be gated off 1: The ticktimer clock is able to be gated off.
6	R	0x0	PM_ICACHE_STAT CPUS LP Interface Status 0: CPUS is in normal mode and the ICACHE clock is disable to be gated off 1: The ICACHE clock is able to be gated off.
5	R	0x0	PM_CPU_STAT CPUS LP Interface Status 0: CPUS is in normal mode and the CPU clock is disable to be gated off. 1: The CPU clock is able to be gated off.
4	R	0x1	CACTIVE_STAT LPI CACTIVE Status 0: CPUS is in low power mode. 1: CPUS is in normal mode.
3:1	/	/	/

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Offset: 0x0338			Register Name: DEV_BUS_AUTOG_CTRL
Bit	R/W	Default/Hex	Description
0	R/W	0x0	CPUS_CLKAUTG_EN 0: Auto gating is disabled. 1: Auto gating is enabled. When MCU gets into sleep mode, auto gating signal will be generated and then every modul bus and work clock will be gated on automatically.

2.11.5.38 0x033C Bus Auto Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: BUS_ACG_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	AHBS_AUTO_CLK_GATE_EN AHBS Bus Auto Clock Gating Function Enable 1: Enable auto clock gate 0: Disable auto clock gate
23:7	/	/	/
6	R/W	0x0	CPUS_MSGBOX_ACG_MODE_EN CPUS_MSGBOX Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, CPUS_MSGBOX HCLK will also be closed when AHBS bus clock is closed.
5	R/W	0x0	S_SPINLOCK_ACG_MODE_EN S_SPINLOCK Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, S_SPINLOCK HCLK will also be closed when AHBS bus clock is closed.
4	R/W	0x0	Reserved
3	R/W	0x0	CPUS_TIMER_ACG_MODE_EN CPUS_TIMER Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, CPUS_ TIMER HCLK will also be closed when AHBS bus clock is closed.
2	R/W	0x0	MSRAM_ACG_MODE_EN MSRAMOC Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto AW1890clock gating function is enable, MSRAMOC HCLK will close when AHBS bus clock close.
1	R/W	0x0	RTC_ACG_MODE_EN RTC Auto Clock Gating Mode Enable SYSRTC module auto clock gating mode enable, if

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Offset: 0x033C			Register Name: BUS_ACG_REG
Bit	R/W	Default/Hex	Description
			this bit is 1 and AHBS auto clock gating function is enable, SYSRTC module hclk will close when AHBS bus clock close.
0	R/W	0x0	BM_ACG_MODE_EN AHBS Bus Matrix Auto Clock Gating Mode Enable If this bit is 1 and AHBS auto clock gating function is enable, AHBS bus matrix HCLK will also be closed when AHBS bus clock is closed.

2.11.5.39 0x360 MSRAMOC Control Register (Default: 0x0000_0000)

Offset: 0x360			Register Name: MSRAMOC_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	MSRAMOC_PORT_HOLD_EN MSRAMOC Port Hold Enable 0: Disable 1: Enable
0	R/W	0x0	MSRAMOC_ACG_EN MSRAMOC Auto Clock Gating Enable 0: Disable 1: Enable

2.11.5.40 0x364 REMAP Control Register (Default: 0x0000_0001)

Offset: 0x364			Register Name: REMAP_CTRL_REG
Bit	R/W	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	SRAMA3_2_RAM_REMAP 0: SRAMA3_2 does not share for MCU_SYS 1: SRAMA3_2 shares for MCU_SYS
0	R/W	0x1	Reserved

2.11.5.41 0x0368 AHBS Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS_RDY_TIMEOUT_IRQ_PEND

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Offset: 0x0368			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
			AHBS Hready Time Out IRQ Pending Write 1 Clear
23:9	/	/	/
8	R/W	0x0	AHBS_RDY_TIMEOUT_IRQ_EN AHBS Hready Time Out IRQ Enable 1: IRQ Enable 0: IRQ Disable
7	R/W	0x0	AHBS_TIMEOUT_INT_VAL_SEL AHBS Time Out Interval Value Selection 0: interal_value* 2^10 + 2^10 -1 1: interal_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS_TIMEOUT_CNT_INT_VAL AHBS Time Out Counter Interval Value
0	R/W	0x0	AHBS_RDY_TIMEOUT_EN AHBS Hready Time Out Enable

2.11.5.42 0x0370 CPUS Device DMA Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0370			Register Name: CPUS_DEV_DMA_SEL_REG
Bit	R/W	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	DMA_SPI_SEL SPI DMA Selection 0: MCU DMA 1: SYS DMA
3	R/W	0x0	DMA_UART1_SEL UART1 DMA Selection 0: MCU DMA 1: SYS DMA
2	R/W	0x0	DMA_UART0_SEL UART0 DMA Selection 0: MCU DMA 1: SYS DMA
1	R/W	0x0	DMA_TWI1_SEL TWI1 DMA Selection 0: MCU DMA 1: SYS DMA
0	R/W	0x0	DMA_TWI0_SEL TWI0 DMA Selection 0: MCU DMA

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Offset: 0x0370			Register Name: CPUS_DEV_DMA_SEL_REG
Bit	R/W	Default/Hex	Description
			1: SYS DMA

2.11.5.43 0x0374 I2S0 PAD Selection Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0374			Register Name: I2S0_PAD_SEL_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	I2S0_PAD_SEL I2S0 PAD Selection 0: Use CPUS PAD 1: Use SYS PAD

2.11.5.44 0x0378 DMIC PAD Selection Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0378			Register Name: DMIC_PAD_SEL_REG
Bit	R/W	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMIC_PAD_SEL DMIC PAD Selection 0: Use CPUS PAD 1: Use SYS PAD

2.11.5.45 0x03E0 Crypt Configuration Register (Default Value: 0x0000_0000)

Offset: 0x03E0			Register Name: CRY_CONFIG_REG
Bit	R/W	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field If you want to read or write Crypt Key Register/Crypt Enable Register, you should write 0x1689 in these bits.

2.11.5.46 0x03E4 Crypt Key Register (Default Value: 0x0000_0000)

Offset: 0x03E4			Register Name: CRY_KEY_REG
Bit	R/W	Default/Hex	Description
31:0	R/W	0x0	CRY_KEY Crypt Key

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2.11.5.47 0x03E8 Crypt Enable Register (Default Value: 0x0000_0000)

Offset: 0x03E8			Register Name: CRY_EN_REG
Bit	R/	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypt Enable

2.11.6 MCU_PRCM Register Description

2.11.6.1 0x0000 PLL Control Register0 (Default Value: 0x0000_0007)

Offset: 0x0000			Register Name: PLL_CTRL_REG0
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	TEST_CLK_SEL PLL Reference Clock Selection 0: DCXO. 1: External Test Clock.
23:3	/	/	/
2	R/W	0x1	GM1 XTAL Gain Control Bit1
1	R/W	0x1	GM0. XTAL Gain Control Bit0
0	R/W	0x1	Reserved

2.11.6.2 0x0004 PLL Control Register 1 (Default Value: 0x0004_0005)

Offset: 0x0004			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
31:24	R/W	0x0	KEY_FIELD Key Field for LDO Enable If the key field value is 0xA7, the bit[23:0] can be modified.
23:19	/	/	/
18:16	R/W	0x4	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control 000: 0.90 V 001: 0.94 V 010: 0.98 V 011: 1.02 V 100: 1.06 V

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Offset: 0x0004			Register Name: PLL_CTRL_REG1
Bit	R/W	Default/Hex	Description
			101: 1.10 V 110: 1.14 V 111: 1.18 V
15:5	/	/	/
4	R/W	0x0	MBIAS_EN Chip Master Bias Enable 0: From Internal Bias 1: From ADDA Bias
3	R/W	0x0	PLLTEST_EN For Verify (Back door clock PLLTEST enable) 0：Output clock is gated off. 1：Clock Output. The clock is the clock output to the PLL and the clock after frequency division through pins.
2:1	R/W	0x2	Reserved
0	R/W	0x1	LDO_EN LDO Enable 0: Disable 1: Enable Note: PLL Power enable (power source from VCC_PLL).

2.11.6.3 0x000C PLL_AUDIO1 Control Register (Default Value: 0x4841_7F00)

Offset: 0x000C			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL_AUDIO1 = 24 MHz*N/M The PLL_AUDIO1 (DIV2) = 24 MHz*N/M /P0 The PLL_AUDIO1 (DIV5) = 24 MHz*N/M /P1 The working frequency range of 24 MHz/M*N is from 180 MHz to 3.5 GHz. The default frequency of PLL_AUDIO1 is 3072 MHz. The default frequency of PLL_AUDIO1 (DIV2) is 1536 MHz. The default frequency of PLL_AUDIO1 (DIV5) is 614.4MHz(24.576 MHz*25).
30	R/W	0x1	PLL_LDO_EN

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Offset: 0x000C			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			LDO enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.) This bit is only valid when the bit[29] is set to 1.
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable This bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1: Enable Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x4	PLL_P1 PLL Output Div P1 P1=PLL_OUTPUT_DIV_P1 + 1 PLL_OUTPUT_DIV_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0 PLL Output Div P0 P0=PLL_OUTPUT_DIV_P0 + 1 PLL_OUTPUT_DIV_P0 is from 0 to 7.
15:8	R/W	0x7F	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254 In application, PLL_FACTOR_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL

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Offset: 0x000C			Register Name: PLL_AUDIO1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M M=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	/	/	/

2.11.6.4 0x0010 PLL_AUDIO1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PLL_AUDIO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Selection 0: 24MHz 1: 12MHz When PLL_INPUT_DIV_M1=1, this bit needs to be set to 1.
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz

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Offset: 0x0010			Register Name: PLL_AUDIO1_PAT0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
16:0	R/W	0x0	WAVE_BOT Wave Bottom

2.11.6.5 0x0014 PLL_AUDIO1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: PLL_AUDIO1_PAT1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DITHER_EN Dither Enable
23:21	/	/	/
20	R/W	0x0	FRAC_EN Fraction Enable
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN Fraction In

2.11.6.6 0x0018 PLL_AUDIO1 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0018			Register Name: PLL_AUDIO1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP PLL Bias Control
15:0	/	/	/

2.11.6.7 0x001C Audio Out Clock Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: AUD_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUD_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON AUD_CLK = PLL_AUDIO1 (DIV2)/M
30:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1

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Offset: 0x001C			Register Name: AUD_CLK_REG
Bit	Read/Write	Default/Hex	Description
			FACTOR_M is from 0 to 31

2.11.6.8 0x002C I2S0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S0_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S0_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.9 0x0030 I2S1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S1_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S1_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL

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Offset: 0x0030			Register Name: I2S1_CLK_REG
Bit	Read/Write	Default/Hex	Description
			Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31.
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31.

2.11.6.10 0x0034 I2S2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S2_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S2_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1

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Offset: 0x0034			Register Name: I2S2_CLK_REG
Bit	Read/Write	Default/Hex	Description
			FACTOR_M is from 0 to 31

2.11.6.11 0x0038 I2S3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: I2S3_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S3_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S3_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.12 0x003C I2S3_ASRC Clock Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: I2S3_ASRC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S3_ASRC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON I2S3_ASRC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL

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Offset: 0x003C			Register Name: I2S3_ASRC_CLK_REG
Bit	Read/Write	Default/Hex	Description
			Clock Source Selection 000: PERI0_300M 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.13 0x0040 I2S Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: I2S_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
19	R/W	0x0	I2S3_RST I2S3 Reset 0: Assert 1: De-assert
18	R/W	0x0	I2S2_RST I2S2 Reset 0: Assert 1: De-assert
17	R/W	0x0	I2S1_RST I2S1 Reset 0: Assert 1: De-assert
16	R/W	0x0	I2S0_RST I2S0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	I2S3_GATING Gating Clock for I2S3 0: Mask

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Offset: 0x0040			Register Name: I2S_BGR_REG
Bit	Read/Write	Default/Hex	Description
			1: Pass
2	R/W	0x0	I2S2_GATING Gating Clock for I2S2 0: Mask 1: Pass
1	R/W	0x0	I2S1_GATING Gating Clock for I2S1 0: Mask 1: Pass
0	R/W	0x0	I2S0_GATING Gating Clock for I2S0 0: Mask 1: Pass

2.11.6.14 0x0044 OWA_TX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: OWA_TX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	OWA_TX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON OWA_TX_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N N= FACTOR_N +1
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

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2.11.6.15 0x0048 OWA_RX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: OWA_RX_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	OWA_RX_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON OWA_RX_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: PERI0_300M 001: AUDIO1PLL_DIV2(low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.16 0x004C OWA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: OWA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	OWA_RST OWA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	OWA_GATING Gating Clock for OWA 0: Mask 1: Pass

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2.11.6.17 0x0050 DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: DMIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMIC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON DMIC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_M +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.18 0x0054 DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: DMIC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DMIC_RST DMIC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING Gating Clock for DMIC 0: Mask 1: Pass

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2.11.6.19 0x0058 AUDIO_CODEC_DAC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: AUDIO_CODEC_DAC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUDIO_CODEC_DAC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_DAC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS) 010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.20 0x005C AUDIO_CODEC_ADC Clock Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: AUDIO_CODEC_ADC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	AUDIO_CODEC_ADC_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_ADC_CLK = Clock Source/M/N
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Selection 000: AUDIO0PLL4X 001: AUDIO1PLL_DIV2 (low power CLK from MCU_PRCM AUDIO_SYS)

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Offset: 0x005C			Register Name: AUDIO_CODEC_ADC_CLK_REG
Bit	Read/Write	Default/Hex	Description
			010: AUDIO1PLL_DIV5 (from MCU_PRCM AUDIO_SYS)
23:10	/	/	/
9:5	R/W	0x0	FACTOR_N Factor N N= FACTOR_N +1 FACTOR_N is from 0 to 31
4:0	R/W	0x0	FACTOR_M Factor M M= FACTOR_M +1 FACTOR_M is from 0 to 31

2.11.6.21 0x0060 AUDIO_CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: AUDIO_CODEC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST AUDIO_CODEC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING Gating Clock for AUDIO_CODEC 0: Mask 1: Pass

2.11.6.22 0x0064 AHBS Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS_RDY_TIMEOUT_IRQ_PEND AHBS Hready Time Out IRQ Pending Write 1 Clear
23:9	/	/	/
8	R/W	0x0	AHBS_RDY_TIMEOUT_IRQ_EN AHBS Hready Time Out IRQ Enable 1: IRQ Enable 0: IRQ Disable

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Offset: 0x0064			Register Name: AHBS_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
7	R/W	0x0	AHBS_TIMEOUT_INT_VAL_SEL AHBS Time Out Interval Value Selection 0: interal_value* 2^10 + 2^10 -1 1: interal_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS_TIMEOUT_CNT_INT_VAL AHBS Time Out Counter Interval Value
0	R/W	0x0	AHBS_RDY_TIMEOUT_EN AHBS Hready Time Out Enable

2.11.6.23 0x0074 MCU_TIMER0 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, MCU_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in MCU_PRCM.

Offset: 0x0074			Register Name: TIMER0_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL MCU_TIMER0 Clock Source Selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz) MCU_TIMER0 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	MCU_TIMER0_CLK_DIVN Select the pre-scale of MCU_TIMER0 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	MCU_TIMER0_CLK_GATING 0: Disable 1: Enable

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2.11.6.24 0x0078 MCU_TIMER1 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, MCU_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in MCU_PRCM.

Offset: 0x0078			Register Name: MCU_TIMER1_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL MCU_TIMER1 clock source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) MCU_TIMER1 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	MCU_TIMER1_CLK_DIVN Select the pre-scale of MCU_TIMER1 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	MCU_TIMER1_CLK_GATING 0: Disable 1: Enable

2.11.6.25 0x007C MCU_TIMER2 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, MCU_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in MCU_PRCM.

Offset: 0x007C			Register Name: MCU_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description

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Offset: 0x007C			Register Name: MCU_TIMER2_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL MCU_TIMER2 clock source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) MCU_TIMER2 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	MCU_TIMER2_CLK_DIVN Select the pre-scale of MCU_TIMER2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	MCU_TIMER2_CLK_GATING 0: Disable 1: Enable

2.11.6.26 0x0080 MCU_TIMER3 Clock Register (Default: 0x0000_0000)

NOTE

In low power mode, MCU_TIMER uses AHB_HCLK_MUX clock which is generated by the PLL in MCU_PRCM.

Offset: 0x0080			Register Name: MCU_TIMER3_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL MCU_TIMER3 Clock Source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) MCU_TIMER3 clock input, the clock sources are 24

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Offset: 0x0080			Register Name: MCU_TIMER3_CLK_REG
Bit	R/W	Default/Hex	Description
			MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	MCU_TIMER3_CLK_DIVN Select the pre-scale of MCU_TIMER2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	MCU_TIMER3_CLK_GATING 0: Disable 1: Enable

2.11.6.27 0x0084 MCU_TIMER4 Clock Register (Default: 0x0000_0000)

Offset: 0x0084			Register Name: MCU_TIMER4_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL MCU_TIMER4 clock source selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) MCU_TIMER4 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	MCU_TIMER4_CLK_DIVN Select the pre-scale of MCU_TIMER4 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	MCU_TIMER4_CLK_GATING 0: Disable 1: Enable

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2.11.6.28 0x0088 MCU_TIMER5 Clock Register (Default: 0x0000_0000)

Offset: 0x0088			Register Name: MCU_TIMER5_CLK_REG
Bit	R/W	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	CLK_SRC_SEL MCU_TIMER5 Clock Source Selection 00: CLK24M 01: CLK32K 10:CLK_RC 11: AHB_HCLK_MUX(200MHz/24.576x4M) MCU_TIMER5 clock input, the clock sources are 24 MHz/RC 16M/CLK32K/ 200 MHz.
3:1	R/W	0x0	MCU_TIMER5_CLK_DIVN Select the pre-scale of MCU_TIMER5 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
0	R/W	0x0	MCU_TIMER5_CLK_GATING 0: Disable 1: Enable

2.11.6.29 0x008C MCU_TIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: MCU_TIMER_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	MCU_TIMER_RST MCU_TIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MCU_TIMER_GATING Gating Clock for MCU_TIMER AHB_CLK 0: Mask 1: Pass

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2.11.6.30 0x0104 MCU_DMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: MCU_DMA_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	MCU_DMAC_RST MCU DMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MCU_DMAC_GATING Gating Clock for MCU_DMAC 0: Mask 1: Pass

2.11.6.31 0x0114 PUBSRAM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PUBSRAM_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PUBSRAM_RST PUBSRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PUBSRAM_GATING Gating Clock for PUBSRAM 0: Mask 1: Pass

2.11.6.32 0x0118 AHBS1 Ready Timeout Control Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: AHBS1_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
31:25	/	/	/
24	R/W1C	0x0	AHBS1_RDY_TIMEOUT_IRQ_PEND AHBS Hready Time Out IRQ Pending Write 1 Clear
23:9	/	/	/
8	R/W	0x0	AHBS1_RDY_TIMEOUT_IRQ_EN AHBS Hready Time Out IRQ Enable 1: IRQ Enable

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Offset: 0x0118			Register Name: AHBS1_RDY_TOUT_CTRL_REG
Bit	R/W	Default/Hex	Description
			0: IRQ Disable
7	R/W	0x0	AHBS1_TIMEOUT_INT_VAL_SEL AHBS Time Out Interval Value Selection 0: interal_value* 2^10 + 2^10 -1 1: interal_value* 2^16 + 2^16 -1
6:1	R/W	0x0	AHBS1_TIMEOUT_CNT_INT_VAL AHBS Time Out Counter Interval Value
0	R/W	0x0	AHBS1_RDY_TIMEOUT_EN AHBS Hready Time Out Enable

2.11.6.33 0x011C MCLK Gating Configuration Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: MCLK_GATING_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	MCUSYS_MCLK_EN Gating Clock for MCUSYS_MCLK 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_EN Gating Clock for DMA_MCLK 0: Mask 1: Pass

2.11.6.34 0x0120 RISCV Clock Register (Default Value: 0x0000_0020)

Offset: 0x0120			Register Name: RISCV_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RISCV_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON RISCV_CLK = Clock Source/M/N
30	/	/	/
29:27	R/W	0x0	RSICVCLK_24M_SRC_SEL Clock Source Selection 000: CLK24M（from CCU) 001: CLK32K（from CCU) 010: CLK_RC（from CCU 16M)
26:0	/	/	/

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2.11.6.35 0x0124 RISCV CFG Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: RISCV_CFG_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	RISCV_CORE_RST RISCV CORE Reset 0: Assert 1: De-assert
17	R/W	0x0	RISCV_APB_DB_RST RISCV APB Debug Reset 0: Assert 1: De-assert
16	R/W	0x0	RISCV_CFG_RST RISCV CFG Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	RISCV_CFG_GATING Gating Clock for RISCV_CFG 0: Mask 1: Pass

2.11.6.36 0x0128 RISCV_MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: RISCV_MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	RISCV_MSGBOX_RST RISCV_MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	RISCV_MSGBOX_GATING Gating Clock for RISCV_MSGBOX 0: Mask 1: Pass

2.11.6.37 0x0130 MCU_PWMCTRL Clock Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: MCU_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0130			Register Name: MCU_PWMCTRL_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PWMCTRL_CLK_GATING Gating Clock 0: Clock is OFF 1: Clock is ON
30	/	/	/
26:24	R/W	0x0	PWMCTRL_CLK_SRC_SEL Clock Source Selection 000: CLK24M 001: CLK32K 010:CLK_RC
23:0	/	/	/

2.11.6.38 0x0134 MCU_PWMCTRL Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: MCU_PWMCTRL_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	MCU_PWMCTRL_RST MCU_PWMCTRL Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MCU_PWMCTRL_GATING Gating Clock for MCU_PWMCTRL PCLK 0: Mask 1: Pass

2.11.6.39 0x0160 PLL Backdoor Output Enable Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PLL_BACKDOOR_OUTPUT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PLL_AUDIO1_ENABLE PLL AUDIO1 Enable 0: Disable 1: Enable

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2.11.6.40 0x0164 Test Debug Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: TEST_DBG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL_OUT_TEST_EN PLL Clock Output to PLLTEST pin Enable PLLTEST = PLL CLK Source/PLL_TEST_P_DIV 0: disable, 1: PLL Clock Output to PLLTEST
30:25	/	/	/
24	R/W	0x0	PLL_CLK_SOURCE AUDIOPLL Clock output selection on 0: AudioPLL output clock 1:AudioPLL reference clock
23:22	/	/	/
21:20	R/W	0x0	PLL_TEST_P_DIV PLL TEST Post Divider 00: /1 01: /2 10: /4 11: /8
19:0	/	/	/

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2.12 RTC

2.12.1 Overview

The Real Time Clock (RTC) is used to implement the time counter and the timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing the power-off information
- Multiple special registers for recording the BROM information

NOTE

The register configuration of RTC is AHB bus, it only can support word operation, not byte operation and half-word operation.

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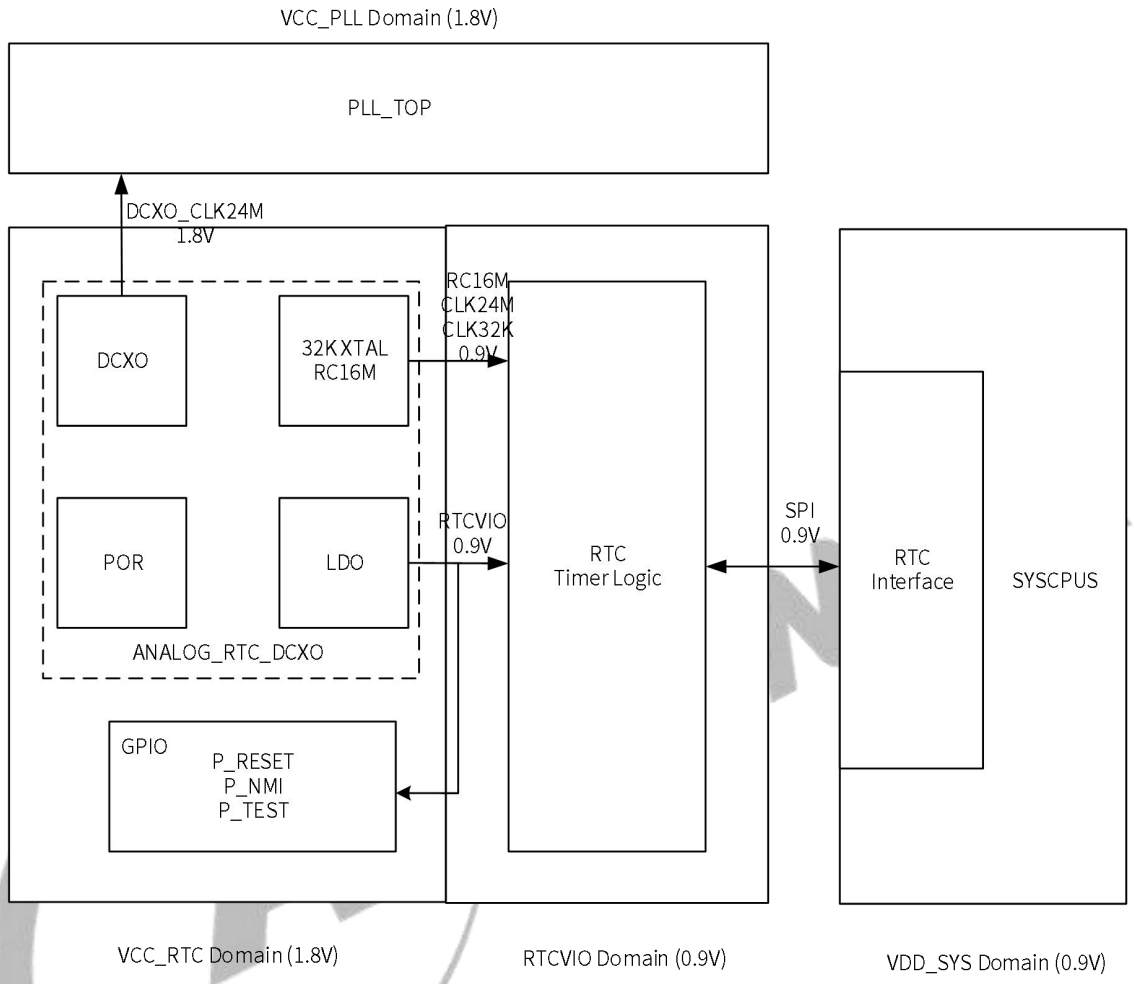
2.12.2 Block Diagram

The following figure shows the block diagram of the RTC.

Figure 2-29 RTC Block Diagram



2.12.3 Functional Descriptions

2.12.3.1 External Signals

Table 2-19 RTC External Signals

Signal Name	Description	Type
X32KFOUT	32.768 kHz clock Fanout Provides low frequency clock for external devices	AO,OD
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO

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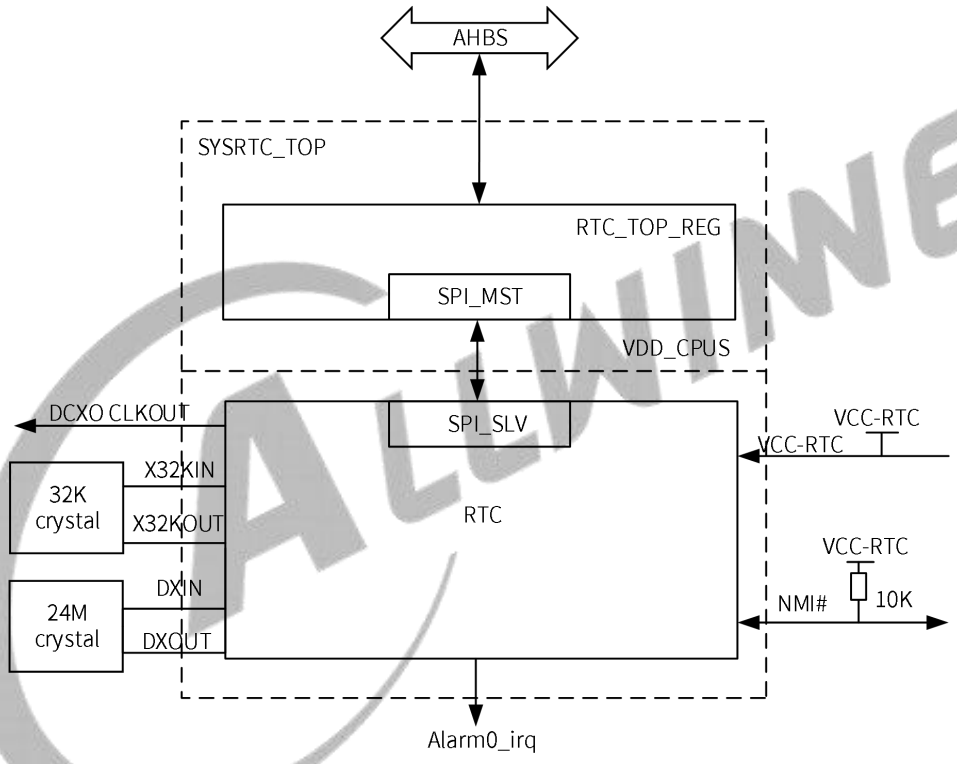
Signal Name	Description	Type
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
WREQIN	Request signal of REFCLK_OUT	AI
NMI	Non-Maskable Interrupt	I/O, OD
RESET	Reset Signal (Low Active)	I/O, OD
VCC-DCXO	Digital Compensated Crystal Oscillator Power Supply	P
VCC-RTC	RTC Power	P

2.12.3.2 Typical Application

Figure 2-30 RTC Application Diagram



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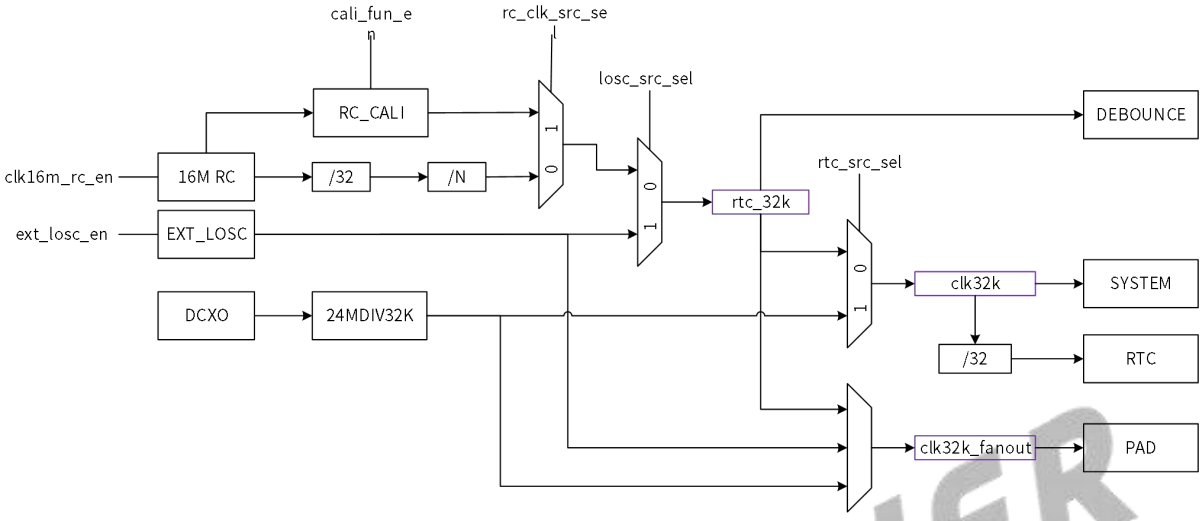
2.12.3.3 Clock Tree

The following figure shows the clock tree of the RTC.

Figure 2-31 RTC Clock Tree



RTC

The RTC has three clock sources:

- 32K divided by internal 16 MHz RC
- 32K divided by external DCXO
- external 32.768 kHz crystal

The RTC selects the internal RC by default, when the system starts, the RTC can select the external low frequency crystal to provide much accurate clock by software. The clock accuracy of the RTC is related to the accuracy of the external low frequency crystal. Usually 32.768 kHz crystal with ±50 ppm frequency tolerance is selected as the clock source. When using internal RC, the clock can be changed by changing division ratio. When using external clock, the clock cannot be changed.

System 32K

The system32K has three clock sources:

- 32K divided by the internal 16 MHz RC
- 32K divided by external DCXO
- external 32.768 kHz crystal

RTC_32K_FANOUT

The RTC_32K_FANOUT has three clock sources:

- 32K divided by the internal 16 MHz RC
- 32K divided by external DCXO
- external 32.768 kHz crystal

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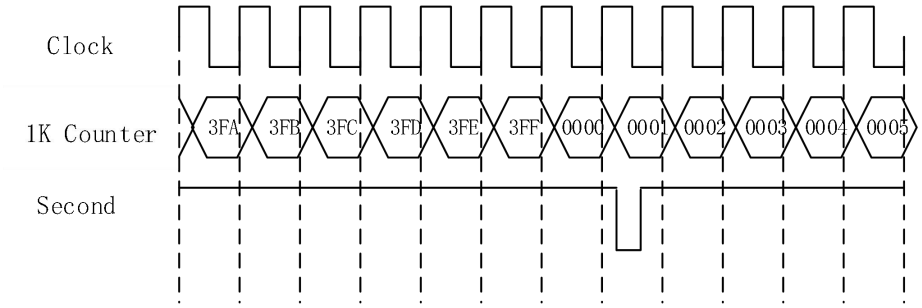
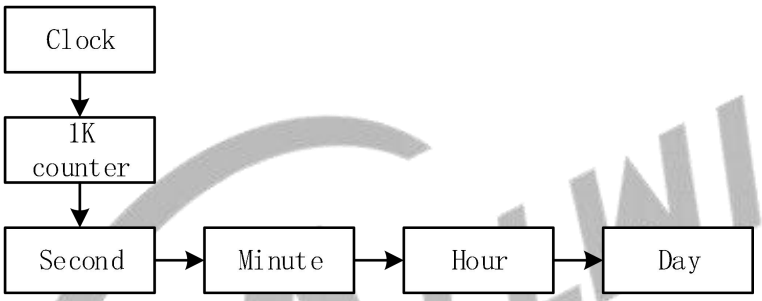
2.12.3.4 Real Time Clock

Figure 2-32 RTC Counter



The 1 kHz counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1 kHz counter starts to count again from 0, and the second counter adds 1. The step structure of 1 kHz counter is as follows.

Figure 2-33 RTC 1 kHz Counter Step Structure



According to above implementation, the changing range of each counter is as follows.

Table 2-20 RTC Counter Changing Range

Counter	Range
Second	0 to 59
Minute	0 to 59
Hour	0 to 23
Day	0 to 65535 (The year, month, day need be transformed by software according to day counter)

CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

2.12.3.5 Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

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The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC need set a new scheduled time, the next interrupt can be generated.

2.12.3.6 RTC-VIO

The RTC module has a LDO, the input source of the LDO is VCC-RTC, the output of the LDO is RTC-VIO, the value of RTC-VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

2.12.3.7 RC Calibration

Figure 2-34 Calibration Circuit

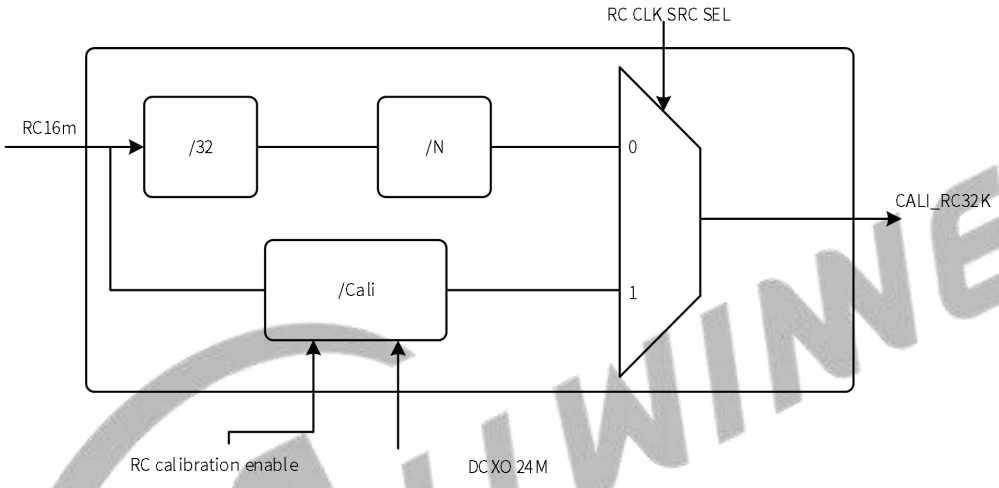
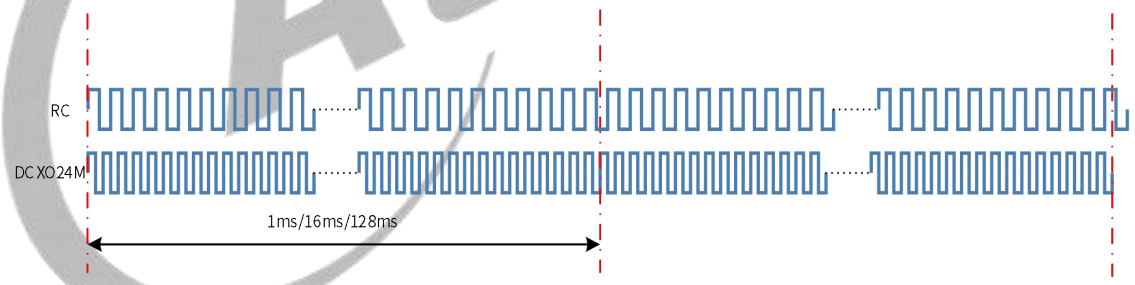


Figure 2-35 RC Waveform



The basic circuit of RC calibration is shown in Figure 2-34. Whether to output the calibrated RC clock can be selected by the RC_Cali_SEL control bit, the calibration principle is as follows:

Step 1 As shown in Figure 2-35, with DCXO 24M as the reference clock, calculate the counter number M of RC clock within 1 ms/16 ms/128 ms to obtain the accurate frequency of internal RC.

Step 2 Divide the accurate frequency by 32.768 kHz and the frequency divider(K) from RC clock to 32.768 kHz is obtained.

Step 3 Divide RC16M by the frequency divider(K) to obtain 32.768 kHz frequency.

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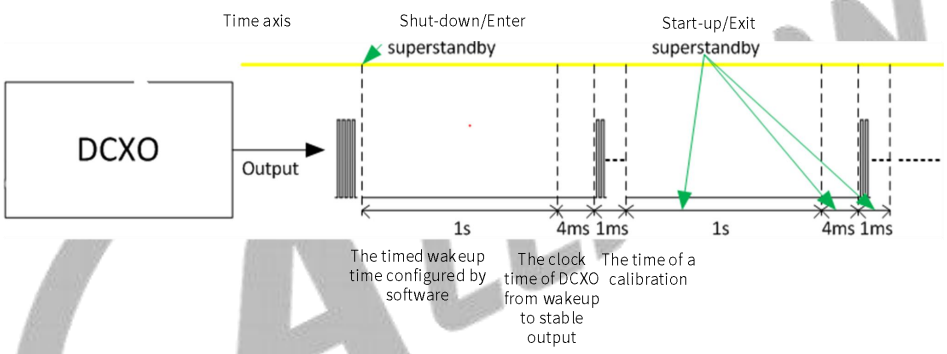
NOTE

The calibration principle is to output 32.768 kHz, not to input 16 MHz.

2.12.3.8 DCXO Timed Wakeup

The logic of DCXO timed wakeup circuit includes two controls: timed wakeup hardware automatic enable and timed wakeup time length (software configuration). The timed wakeup means that DCXO circuit is required to wakeup the output clock once every second (1s-60s, usually the ambient temperature changes little in a few seconds) for 32K calibration in the super standby or shutdown scenario, after calibration, DCXO circuit is closed, the closed time is timed wakeup time length (software configuration). The time of DCXO circuit from wakeup starting to stable output is 3 ms-4 ms. Although the timed wakeup function is closed, DCXO circuit always had worked. The process of timed wakeup is shown in the following figure.

Figure 2-36 DCXO Timed Wakeup Waveform



The time of a calibration in shutdown or super standby:

the timed wakeup time configured by software + the clock time of DCXO from wakeup to stable output + the time of a calibration.

The timed wakeup time configured by the software in the figure is 1 s, and can be configured by software in application. It is the theoretical maximum value for DCXO from wakeup to stable output clock in 4 ms, the specific value is subject to IC measured results. In the any time of these three periods, the startup or exit of the super standby action will not cause DCXO abnormal.

The enable signal of DCXO and the enable signal of timed wakeup DCXO is “OR” logic, and they do not contradict each other.

The interval between continuous DCXO enable operation and disable operation is at least greater than 4 ms.

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2.12.3.9 RC Calibration Usage Scenario

Power-on: Select non-accurate 32K divided by internal RC.

Normal scenario: Select external accurate 32K, or external calibrated 32K.

Standby or power-off scenario: Select external accurate 32K, or external calibrated 32K.

2.12.4 Programming Guidelines

2.12.4.1 RTC Clock Control

Step 1 Select clock source: Select clock source by the bit0 of LOSC_CTRL_REG, the clock source is the internal RC oscillator by default. When the system starts, the clock source can be switched to the external 32K oscillator by software.

Step 2 Auto switch: After enabled the bit [15:14] of LOSC_CTRL_REG, the RTC automatically switches clock source to the internal oscillator when the external crystal could not output waveform, the switch status can query by the bit [1] of LOSC_AUTO_SWT_STA_REG.

NOTE

If only configuring the bit [15] of LOSC_CTRL_REG, the clock source status bit cannot be changed after the auto switch is valid, because the two functions are independent.

Here are the basic code samples.

```
Write (0x16aa4000, LOSC_Ctrl); //Write key field
Write (0x16aa4001, LOSC_Ctrl); //Select the external 32K clock
```

2.12.4.2 RTC Calendar

Step 1 Write time initial value: Write the current time to RTC_DAY_REG and RTC_HH_MM_SS_SET_REG.

Step 2 After updated time, the RTC restarts to count again. The software can read the current time anytime.

NOTE

- The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.
- Ensure the bit [8:7] of LOSC_CTRL_REG is 0 before the next time configuration is performed.

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Here are the basic code samples.

For example: set time to 21st, 07:08:09 and read it.

RTC_DAY_REG = 0x00000015;

RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)

Read (RTC_DAY_REG);

Read (RTC_HH_MM_SS_REG);

2.12.4.3 Alarm0

Step 1 Enable alram0 interrupt by writing ALARM0_IRQ_EN.

Step 2 Set the counter comparator, write the count-down day, hour, minute, second number to ALARM0_DAY_SET_REG and ALARM0_CUR_VLU_REG.

Step 3 Enable alarm0 function by writing ALARM0_ENABLE_REG, then the software can query alarm count value in real time by ALARM0_DAY_SET_REG and ALARM0_CUR_VLU_REG. When the setting time reaches, ALARM0_IRQ_STA_REG is set to 1 to generate interrupt.

Step 4 After enter the interrupt process, write ALARM0_IRQ_STA_REG to clear the interrupt pending, and execute the interrupt process.

Step 5 Resume the interrupt and continue to execute the interrupted process.

Step 6 The power-off wakeup is generated via SoC hardware and PMIC, the software only needs to set the pending condition of alarm0, and set ALARM0_CONFIG_REG to 1.

2.12.4.4 Fanout

CLK32K Fanout

Set the LOSC_OUT_GATING bit (bit [0]) of CLK32K_FOUT_CTRL_GATING_REG register to 1, and ensure external pull-up resistor, voltage, and clock source are normal, then 32.768kHz square wave can be output.

CLK24M Fanout

To fanout CLK24M clock though REFCLK-OUT pin, configure the CLK_REQ_ENB bit (bit [31]) of DCXO_CTRL_REG register.

2.12.5 Register List

Module Name	Base Address
RTC	0x0709 0000

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Register Name	Offset	Description
VDD_RTC Power Domain		
LOSC_CTRL_REG	0x0000	LOSC Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
INTOSC_CLK_AUTO_CALI_REG	0x000C	Internal OSC Clock Auto Calibration Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_SET_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_DAY_SET_REG	0x0020	Alarm 0 Day Set Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM0_CONFIG_REG	0x0050	Alarm 0 Configuration Register
CLK32K_FOUT_CTRL_GATING_REG	0x0060	CLK32K Fanout Control register
GP_DATA_REGn	0x0100+N*0x0004 (N=0-7)	General Purpose Register
FBOOT_INFO_REG0	0x0120	Fast Boot Info Register0
FBOOT_INFO_REG1	0x0124	Fast Boot Info Register1
DCXO_CTRL_WP_REG	0x015C	DCXO Control Write Protect Register
DCXO_CTRL_REG	0x0160	DCXO Control Register
CALI_CTRL_REG	0x0164	Calibration Control Register
VDD_RTC_REG	0x0190	VDD_RTC Regulation Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_OFF_GATING_CTRL_REG	0x01F4	VDD Off Gating Control Register
EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
VDD_SYS Power Domain		
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

2.12.6 Register Description

2.12.6.1 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD KEY Field. This field should be filled with 0x16AA, and then the bit 0 and bit 1 can be written with the new value.

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Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable. 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K CLK source selection enable. 0: Disable. When the LOSC losts, 32k CLK source will not change to RC 1: Enable. When LOSC losts, 32k CLK source will change to RC (LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/
8	R	0x0	RTC_HHMMSS_ACCE RTC Hour Minute Second access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS register, the HH-MM-SS register will be refreshed for at most one second. Note: Make sure that the bit is 0 for time configuration.
7	R	0x0	RTC_DAY_ACCE RTC DAY access. After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second. Note: Make sure that the bit is 0 for time configuration.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32768Hz Crystal Enable. 0: disable 1: enable
3:2	R/W	0x0	EXT_LOSC_GSM External 32768Hz Crystal GSM. 00: Low 01: Reserved 10: Reserved

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Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			11: High When GSM is changed, the 32K oscillation circuit will arise transient instability. If the auto switch function (bit 15) is enabled, 32K changes to RC16M with certain probability. The GSM can influence the time of 32K starting oscillation, the more the GSM, the shorter the time of starting oscillation. So modifying GSM is not recommended. If you need to modify the GSM, firstly disable the auto switch function (bit 15), with a delay of 50 us, then change the GSM, the 32K clock source is changed to external clock.
1	R/W	0x0	RTC_SRC_SEL RTC_TIMER Clock Source Select. 0: LOSC_SRC 1: 24MDIV32K Before switching the bit, make sure that the 24MDIV32K function is enabled, that is, the bit16 of the 32K Fanout Control Register is 1.
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock Source Select. 'N' is the value of Internal OSC Clock Prescalar register. 0: Low Frequency Clock from 16M RC 1: External 32.768 kHz OSC.

2.12.6.2 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when auto switch function is enable. 0: External 32.768 kHz OSC work normally. 1: External 32.768 kHz OSC work abnormally.
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending. 0: No effect 1: Auto switches pending, means LOSC_SRC_SEL is changed from 1 to 0.
0	R	0x0	LOSC_SRC_SEL_STA

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Offset: 0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Write	Default/Hex	Description
			Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar register. 0: Low Frequency Clock from 16M RC 1: External 32.768 kHz OSC

2.12.6.3 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset: 0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescalar value N The clock output = Internal RC/32 / N 00000: 1 00001: 2 00002: 3 ..... 11111: 32

2.12.6.4 0x000C Internal OSC Clock Auto Calibration Register (Default Value: 0x01E8_0000)

Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	Read/Write	Default/Hex	Description
31:22	R	0x1E8	32k calibration integer divide factor.
21:5	R	0x0	32k calibration decimal divide factor.
4	R/W	0x0	Calibration function Clk16M_RC_enable 0: Auto gating 1: Soft bypass
3:2	R/W	0x0	RC Calibration Precise Selection 00: 1ms calibration precise 01: 16ms calibration precise 10: 128ms calibration precise
1	R/W	0x0	RC calibration enable 0: Close Calibration circuit 1: Open Calibration circuit
0	R/W	0x0	RC CLK SRC SEL Select the RTC 32k clock source from normal RC or Calibrated RC: 0: Normal RC

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Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	Read/Write	Default/Hex	Description
			1: Calibrated RC

2.12.6.5 0x0010 RTC Year-Month-DAY Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: RTC_DAY_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	UDF	DAY Set DAY. Range from 0-65535.

2.12.6.6 0x0014 RTC Hour-Minute-Second Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: RTC_HH_MM_SS_SET_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Set Hour. Range from 0-23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Set Minute. Range from 0-59
7:6	/	/	/
5:0	R/W	UDF	SECOND Set second. Range from 0-59

2.12.6.7 0x0020 Alarm 0 Day Set Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is Based on Day.

2.12.6.8 0x0024 Alarm 0 Counter Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0024	Register Name: ALARM0_CUR_VLU_REG

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Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	UDF	HOUR Current hour. Range from 0-23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Current minute. Range from 0-59
7:6	/	/	/
5:0	R/W	UDF	SECOND Current second. Range from 0-59

2.12.6.9 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: ALARM0_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. 0: Disable 1: Enable

2.12.6.10 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: ALARM0_IRQ_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable. 0: Disable 1: Enable

2.12.6.11 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit.

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Offset: 0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
			0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 IRQ enable is set to 1, the pending bit will be sent to the interrupt controller.

2.12.6.12 0x0050 Alarm 0 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ALARM0_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

2.12.6.13 0x0060 CLK32K Fanout Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: CLK32K_FOUT_CTRL_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DCXO_TO_32K_DIVIDER_ENABLE DCXO to 32k divider enable. 1: Enable the DCXO 24M to 32K divider circuit 0: Disable the DCXO 24M to 32K divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL LOSC Output Source Select. 00: RTC_32K (select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: LOSC 10: DCXO divided 32K
0	R/W	0x0	LOSC_OUT_GATING LOSC Output Gating Enable. Configuration of LOSC output, and no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

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2.12.6.14 0x0100+N*0x0004 (N=0-7) General Purpose Register (Default Value: 0x0000_0000)

Offset: 0x0100+N*0x0004 (N=0-7)			Register Name: GP_DATA_REGn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA Data.

NOTE

General purpose register 0 to 7 value can be stored if the RTC-VI O is larger than 0.7 V.

2.12.6.15 0x0120 Fast Boot Info Register0 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: FBOOT_INFO_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO0. Fast Boot info. Fast Boot Information, refer to BROM spec.

2.12.6.16 0x0124 Fast Boot Info Register1 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: FBOOT_INFO_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FBOOT_INFO1. Fast boot info. Fast Boot Information, refer to BROM spec.

2.12.6.17 0x015C DCXO Control Write Protect Register (Default Value:0x0000_0000)

Offset: 0x015C			Register Name: DCXO_CTRL_WP_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	Key Filed. Write protection for XO_CTRL_REG(0x0160). Write this field as 0x16AA before configuring XO_CTRL_REG(0x0160) and this field will be automatically cleared to 0 after XO_CTRL_REG is configured.

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2.12.6.18 0x0160 DCXO Control Register (Default Value: 0x983F_10F7)

Offset: 0x0160			Register Name: DCXO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CLK_REQ_ENB CLK REQ Enable 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:29	/	/	/
28	R	0x1	DCXO_STABLE_STS DCXO Stable Status 0: no stable 1: stable
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value.
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value. cap cell is 55fF
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage.
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal active high.
6	R/W	0x1	XTAL_MODE XTAL mode enable signal active high. 0x0 for external CLK input mode. 0x1 for normal mode.
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO RFCLK Enhance. Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for 10pF, 0x2 for 15pF, 0x3 for 20pF
3	/	/	/
2	R/W	0x1	RSTO_DLY_SEL RSTO delay select. For Debug Use Only It cannot configure to 0 in normal state.
1	R/W	0x1	DCXO_EN DCXO Enable. 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN Clock RC16M Enable.

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Offset: 0x0160			Register Name: DCXO_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			1: Enable 0: Disable The related register configuration is necessary to ensure the reset debounce circuit has a stable clock source. The first time SoC starts up, by default, the reset debounce circuit of SoC uses 32K divided by RC16M. In power-off, software reads the related bit to ensure whether EXT32K is working normally, if it is normal, first switch the clock source of debounce circuit to EXT32K, then close RC16M. Without EXT32K scenario or external RTC scenario, software confirms firstly whether EXT32K is working normally before switching, or software does not close RC16M.

2.12.6.19 0x0164 Calibration Control Register (Default Value: 0x0000_0043)

Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WAKEUP_DCXO_EN Wake up DCXO circuit enable.
30:17	/	/	/
16	R/W	0x0	WAKEUP_READY_SLEEP_MODE Calibration wake up ready sleep mode, it must be set before 0x164 bit31 WAKEUP_DCXO_EN is set to 1. 0: Disable 1: Enable
15:12	R/W	0x0	TIMER FOR READY SLEEP Total timer for ready sleep 0x00: 15s 0x01: 30s 0x02: 45s 0x03: 60s 0x04: 90s 0x05: 120s 0x06: 150s Others: /
11:8	R/W	0x0	WAKEUP_CNT FOR READY SLEEP Wake up counter for ready sleep 0x00: 250ms

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Offset: 0x0164			Register Name: CALI_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0x01: 500ms 0x02: 750ms 0x03: 1s 0x04: 1.25s 0x05: 1.5s 0x06: 1.75s 0x07: 2s 0x08: 2.25s 0x09: 2.5s 0x0A: 2.75s 0x0B: 3s 0x0C: 3.25s 0x0D: 3.5s 0x0E: 3.75s 0x0F: 4s
7:4	R/W	0x4	WAKEUP_CNT FOR SLEEP Wake up counter for sleep 0x00: 250ms 0x01: 500ms 0x02: 1s 0x03: 10s 0x04: 60s 0x05: 120s 0x06: 180s 0x07: 240s 0x08: 300s 0x09: 360s 0x0A: 420s 0x0B: 480s 0x0C: 540s 0x0D: 600s 0x0E: 1200s 0x0F: 1800s
3:0	R/W	0x3	WAIT DCXO SEL Select for DCXO active after DCXO enable 0x0: 1ms 0x1:2ms 0x2:3ms 0x3:4ms ... 0xF: 16ms

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2.12.6.20 0x0190 VDD RTC Regulation Register (Default Value: 0x0000_0004)

Offset: 0x0190			Register Name: VDD_RTC_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	V_SEL VDD Select 0: Resistance divider 1: Band gap
3	/	/	/
2:0	R/W	0x4	VDD_RTC_REGU RTC VIO voltage select The RTC-VIO is provided power for RTC digital part. These bits are useful for regulating the RTC_VIO from 0.65 V to 1.3 V: 0x0: 1.0 V 0x1: 0.65 V 0x2: 0.7 V 0x3: 0.8 V 0x4: 0.9 V 0x5: 1.1 V 0x6: 1.2 V 0x7: 1.3 V

2.12.6.21 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: IC_CHARA_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	KEY_FIELD Write protect. Should be written at value 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA IC_CHARA. Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

2.12.6.22 0x01F4 VDD Off Gating Control Register (Default Value: 0x0000_0021)

Offset: 0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD

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Offset: 0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			Write protect. This field should be filled with 0x16AA, and then the bit 15 can be configured.
15	WAC	0x0	PWROFF_GAT_RTC_CFG. Power off gating control signal. When use VDD-SYS to RTC isolation software control, write this bit 1, it will only be clear by RESETB release. (For Debug Use Only)
14:12	/	/	/
11:4	R/W	0x2	VCCIO_DET_SPARE VCCIO detect spare. Bit [7:5]: Reserved Bit [4]: Bypass debounce circuit 0: bypass 1: no bypass Bit [3]: Enable control 0: Disable VCC-IO detecter 1: Force the detection output Bit [2:0]: Gear adjustment 000: Detection threshold is 2.5 V 001: Detection threshold is 2.6 V 010: Detection threshold is 2.7 V 011: Detection threshold is 2.8 V 100: Detection threshold is 2.9 V 101: Detection threshold is 3 V 110-111: N/A
3:1	/	/	/
0	R/W	0x1	VCCIO_DET_BYPASS_EN VCCIO detect bypass enable. 0: not bypass 1: bypass

2.12.6.23 0x0204 eFuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EFUSE_1P8V_POWER_SWITCH_CONTROL EFUSE power switch control 1: open power switch

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Offset: 0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0: close power switch

2.12.6.24 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0009)

Offset: 0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RTC_SPI_GATE_EN RTC Reg CFG SPI Clock Gating. 0: Gating 1: Not Gating Before configurating RTC register, the clock divider of SPI needs be configured firstly, then clock gating needs be enabled. Note: Frequency division and clock gating can not be set at the same time.
30:5	/	/	/
4:0	R/W	0x9	RTC_SPI_DIV RTC Reg CFG SPI Clock Divider M. Actual SPI Clock = AHBS1/(M+1), (0 to 15) The default frequency of AHBS1 is 200 MHz, and the default frequency of SPI Clock is 20 MHz. **Note: The SPI clock can not exceed 50 MHz, or else the RTC register may be abnormal.**

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2.13 Spinlock

2.13.1 Overview

The spinlock provides hardware synchronization mechanism in multi-core systems. With the lock operation, the spinlock prevents multiple processors from handling the sharing data simultaneously and thus ensure the coherence of data.

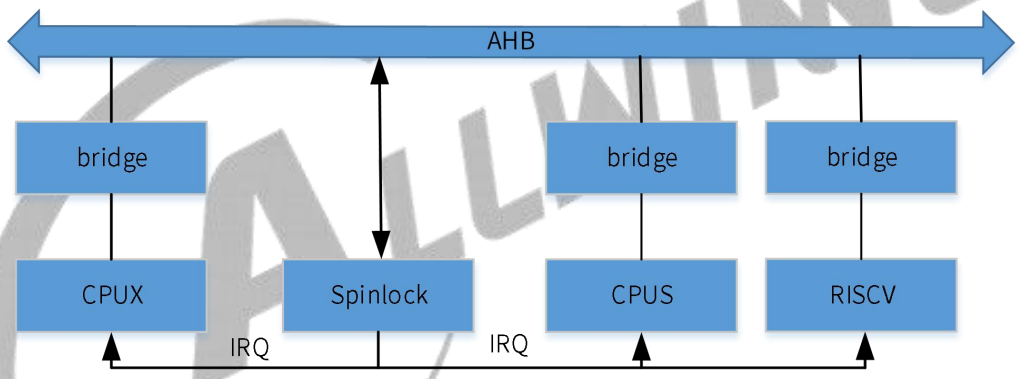
The spinlock has the following features:

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

2.13.2 Block Diagram

The following figure shows the block diagram of the spinlock.

Figure 2-37 Spinlock Block Diagram



2.13.3 Functional Description

2.13.3.1 Clock and Reset

The spinlock is mounted on AHB. Before accessing the spinlock registers, you need to de-assert the reset signal on AHB bus and then open the corresponding gating signal on AHB bus.

2.13.3.2 Typical Application

The following figure shows a typical application of the spinlock. A processor locks spinlock0 before executing specific codes, and then unlocks the codes. After the lock is freed, other processors can read or write the data.

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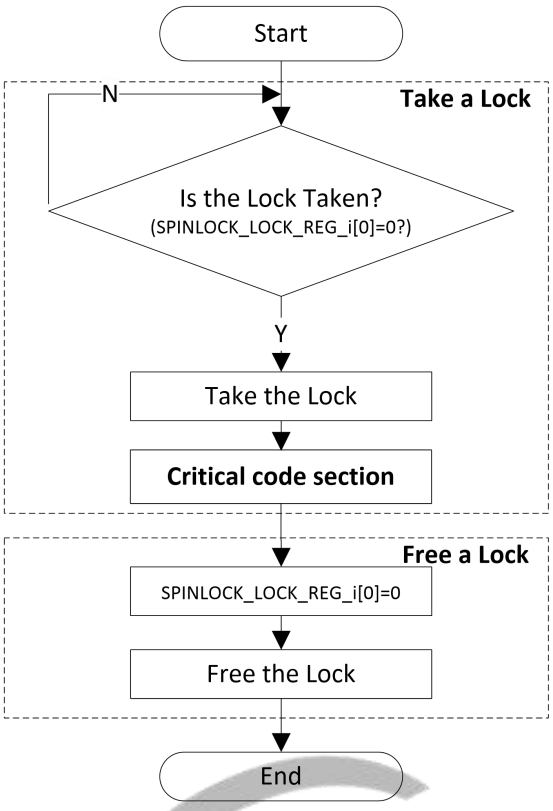
Figure 2-38 Spinlock Typical Application Diagram



2.13.3.3 Spinlock State Machine

When a processor uses spinlock, it needs to acquire the spinlock status through SPINLOCK_STATUS_REG.

Reading operation

when the return value is 0, it indicates that the spinlock enters the locked status; reading this status bit again can return 1, it indicates that the spinlock is the locked status.

Writing operation

when the spinlock is in the locked status, writing 0 can convert the spinlock to the unlocked status, the writing operation for other status is invalid.

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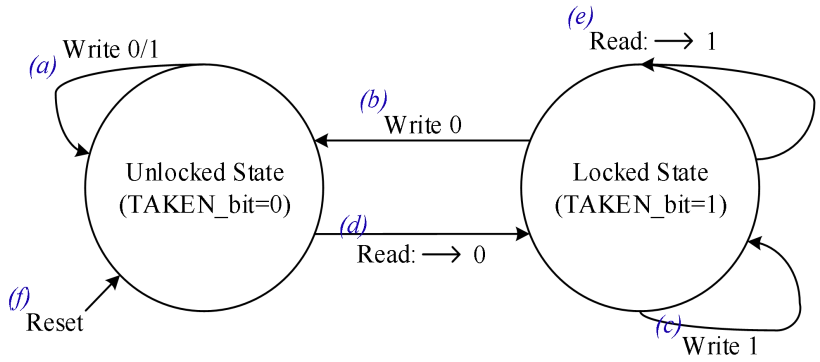
The following figure shows the spinlock state machine.

Figure 2-39 Spinlock State Machine



- When the spinlock is in the unlocked state, writing 0/1 has no effect;
- When the spinlock is in the locked state, writing 0 can convert the corresponding spinlock to the unlocked state;
- When the spinlock is in the locked state, writing 1 has no effect;
- When the spinlock is in the unlocked state, reading the bit can return 0 (it indicates spinlock enters into the locked state);
- When the spinlock is in the locked state, reading the bit can return 1 (it indicates spinlock is in the locked state);
- After reset, the spinlock is in the unlock state by default.

2.13.4 Programming Guidelines

2.13.4.1 Switching the Status

Follow the steps below to switch the lock status of a spinlock.

Step 1 When the read value from SPINLOCKN_LOCK_REG (N=0–31) is 0, the spinlock comes into the locked status.

Step 2 Execute the application codes, and the status of SPINLOCK_STATUS_REG is 1.

Step 3 Write 0 to SPINLOCKN_LOCK_REG (N=0–31), the spinlock converts into the unlocked status, and the corresponding spinlock is released.

2.13.4.2 Processing the Interrupt

The spinlock generates an interrupt when a lock is freed (the lock status converts from the locked status to the unlocked status).

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Follow the steps below to process the interrupt:

Step 1 Configure the interrupt enable bit of the corresponding spinlock in SPINLOCK_IRQ_EN_REG to enable the interrupt.

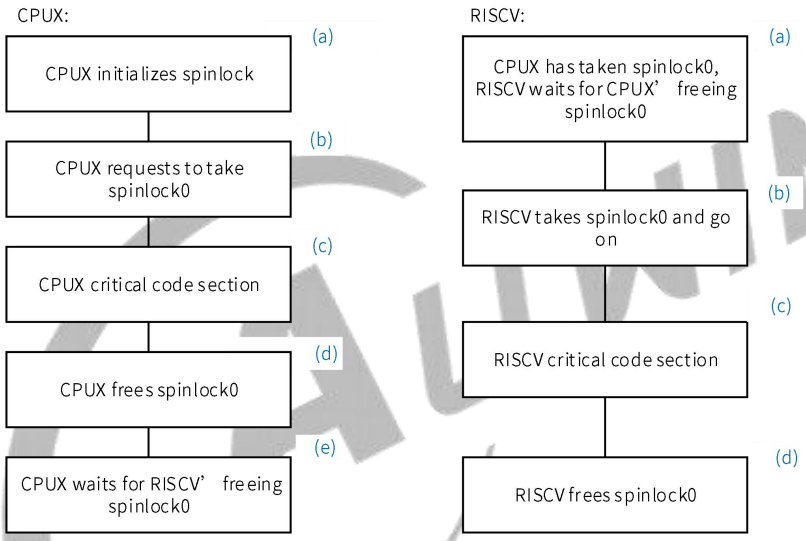
Step 2 The spinlock generates an interrupt when its status converts from the locked status to the unlocked status, and the corresponding bit of the SPINLOCK_IRQ_STA_REG turns to 1.

Step 3 Execute the interrupt handle function and clear the pending bit.

2.13.4.3 Taking/Freeing Spinlock

Take the synchronization between CPUX and RISCV with Spinlock0 as an example, the CPUX and RISCV perform the following steps.

Figure 2-40 CPUX and RISCV Taking/Freeing Spinlock0 Process



CPUX:

a) The CPUX initializes Spinlock.

b) Check lock register0 (SPINLOCK_STATUS_REG0) status. If it is taken, check until CPUX frees spinlock0 and then request to take spinlock0. Otherwise, retry until the lock register0 is taken.

c) Execute CPUX critical code.

d) After executing CPUX critical code, the CPUX frees spinlock0.

The CPUX waits for RISCV to free spinlock0.

RISCV:

a) If the CPUX has taken spinlock0, the RISCV waits for CPUX to free spinlock0.

b) The RISCV requests to take spinlock0. If it fails, retry until the lock register0 is taken.

c) Execute RISCV critical code.

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d) After executing RISCV critical code, the RISCV frees spinlock0.

The following codes are for reference.

----------CPUX----------

Step 1 CPUX initializes Spinlock

```
put_wvalue(SPINLOCK_BGR_REG,0x00010000);
put_wvalue(SPINLOCK_BGR_REG,0x00010001);
```

Step 2 CPUX requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG0);                  //Check lock register0 status
if (rdata != 0) writel (0, SPINLOCK_LOCK_REG0); //If it is taken, check till CPUX frees spinlock0
rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
if (rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0);    //If it fails, retry till lock register0 is taken
```

---------- **CPUX critical code section** ----------

Step 3 CPUX frees spinlock0

```
writel (0, SPINLOCK_LOCK_REG0);                     //CPUX frees spinlock0
```

Step 4 CPUX waits for RISCV' freeing spinlock0

```
writel(readl(SPINLOCK_STATUS_REG0) == 1);       //CPUX waits for RISCV' freeing spinlock0
```

----------RISCV----------

Step 1 CPUX has taken spinlock0, RISCV waits for CPUX' freeing spinlock0

```
while(readl(SPINLOCK_STATUS_REG0) == 1);        //RISCV waits for CPUX' freeing spinlock0
```

Step 2 RISCV takes spinlock0 and go on

```
rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
if (rdata != 0) rdata=readl(SPINLOCK_LOCK_REG0);    //If it fails, retry till lock register0 is taken
```

---------- **RISCV critical code section** ----------

Step 3 RISCV frees spinlock0

```
writel (0, SPINLOCK_LOCK_REG0);                     //RISCV frees spinlock0
```

2.13.5 Register List

Module Name	Base Address
SPINLOCK	0x03005000
S_SPINLOCK	0x07093000

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Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	Spinlock Interrupt Enable Register
SPINLOCK_IRQ_STA_REG	0x0040	Spinlock Interrupt Status Register
SPINLOCK_LOCKID0_REG	0x0080	Spinlock Lockid0 Register
SPINLOCK_LOCKID1_REG	0x0084	Spinlock Lockid1 Register
SPINLOCK_LOCKID2_REG	0x0088	Spinlock Lockid2 Register
SPINLOCK_LOCKID3_REG	0x008C	Spinlock Lockid3 Register
SPINLOCK_LOCKID4_REG	0x0090	Spinlock Lockid4 Register
SPINLOCK_LOCK_REGN	0x0100 + N*0x0004	Spinlock Register N (N = 0 to 31)

2.13.6 Register Description

2.13.6.1 0x0000 Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 256 lock registers 01: This instance has 32 lock registers 10: This instance has 64 lock registers 11: This instance has 128 lock registers
27:9	/	/	/
8	R	0x0	IU0 In-Use flag0, covering lock register0-31 0: All lock registers 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

2.13.6.2 0x0010 Spinlock Register Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LOCK_REG_STATUS SpinLock[i] status 0: The Spinlock is free

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Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	Read/Write	Default/Hex	Description
			1: The Spinlock is taken

2.13.6.3 0x0020 Spinlock Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LOCK_IRQ_EN SpinLock[i] interrupt enable 0: Disable 1: Enable

2.13.6.4 0x0040 Spinlock Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	LOCK_IRQ_STATUS SpinLock[i] interrupt status 0: No effect 1: Pending Writing 1 clears this bit.

2.13.6.5 0x0080 Spinlock Lockid0 Register (Default Value: 0x7777_7777)

Offset: 0x0080			Register Name: SPINLOCK_LOCKIN0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID0

2.13.6.6 0x0084 Spinlock Lockid1 Register (Default Value: 0x7777_7777)

Offset: 0x0084			Register Name: SPINLOCK_LOCKIN1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID1

2.13.6.7 0x0088 Spinlock Lockid2 Register (Default Value: 0x7777_7777)

Offset: 0x0088			Register Name: SPINLOCK_LOCKIN2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID2

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2.13.6.8 0x008C Spinlock Lockid3 Register (Default Value: 0x7777_7777)

Offset: 0x008C			Register Name: SPINLOCK_LOCKIN3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID3

2.13.6.9 0x0090 Spinlock Lockid4 Register (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: SPINLOCK_LOCKIN4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x77777777	LOCKID4

2.13.6.10 0x0100 + N*0x04 Spinlock Register N (N = 0 to 31) (Default Value: 0x0000_0000)

Offset: 0x0100 + N*0x0004 (N = 0 to 31)			Register Name: SPINLOCKN_LOCK_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TAKEN Lock State Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

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2.14 Thermal Sensor Controller (THS)

2.14.1 Overview

The thermal sensors are common elements in wide range of modern system on chips (SoCs) platform. The thermal sensors are used to constantly monitor the temperature on the chip.

The thermal sensor controller (THS) embeds four thermal sensors. TSENSOR0 is located in the 'big' cores of CPUX; TSENSOR1 is located in the 'LITTLE' cores of CPUX; TSENSOR2 is located in the GPU; TSENSOR4 is located in the DDR. When the temperature reaches a certain thermal threshold, the thermal sensor can generate interrupts to the software to lower the temperature via the dynamic voltage and frequency scaling (DVFS) technology.

The THS has the following features:

- Two THS controllers
  - THS0, including TSENSOR4
  - THS1, including TSENSOR0, TSENSOR1, and TSENSOR2
- Temperature accuracy: ±5°C from -40°C to 60°C, ±3°C from -60°C to +125°C
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

2.14.2 Block Diagram

The following figures show the block diagrams of the THS0 and THS1.

Figure 2-41 THS0 Block Diagram

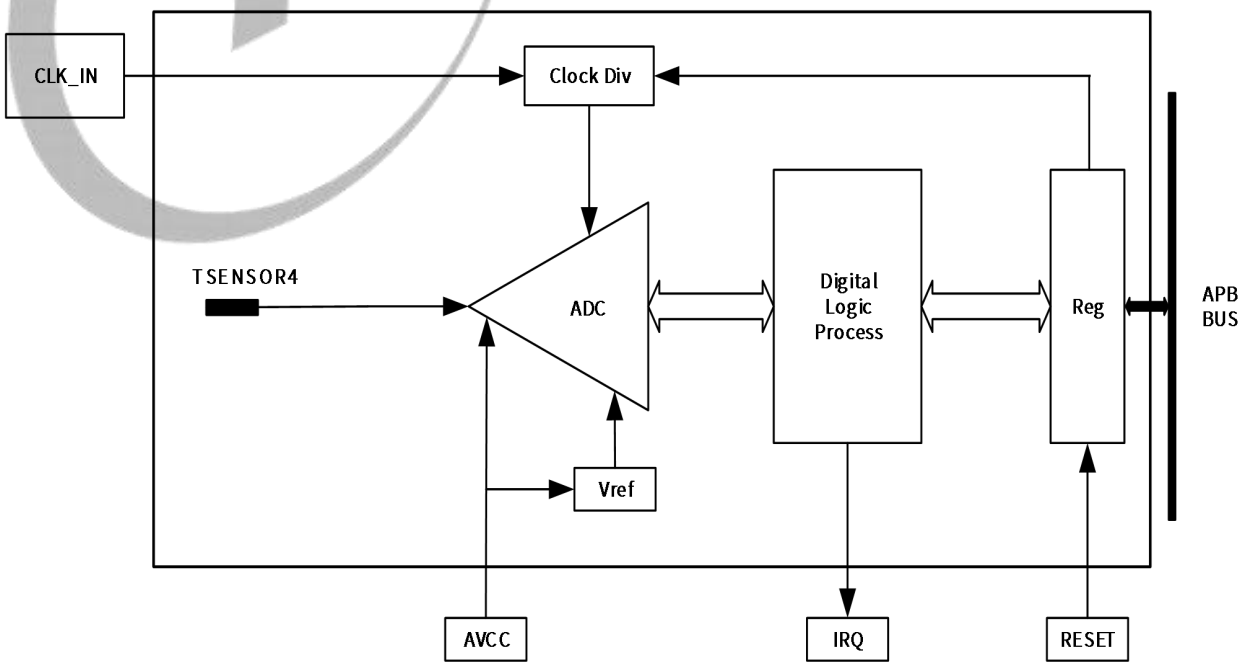

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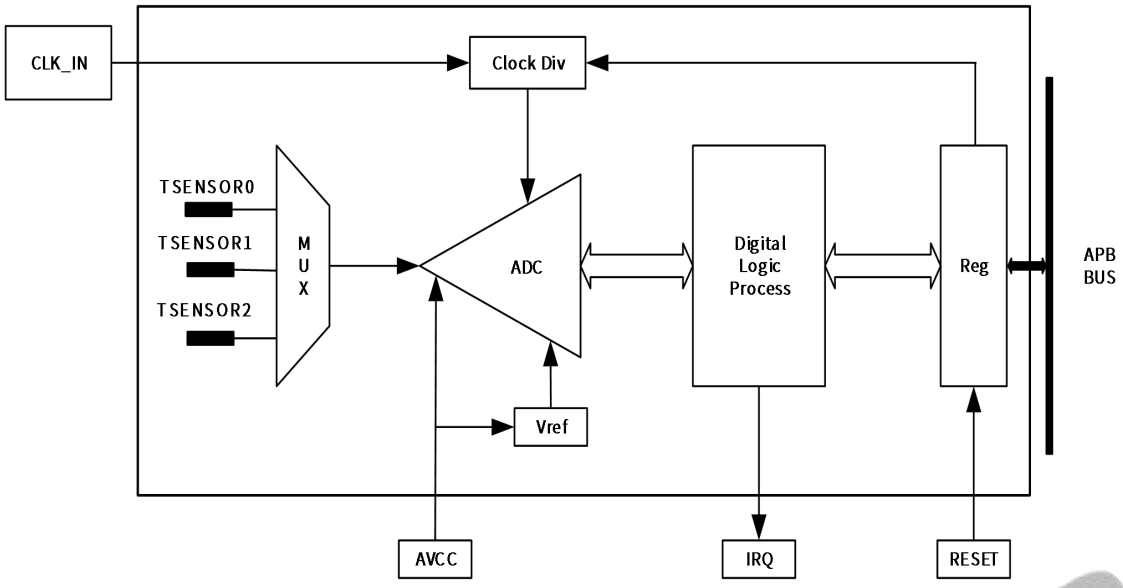
Figure 2-42 THS1 Block Diagram



2.14.3 Functional Description

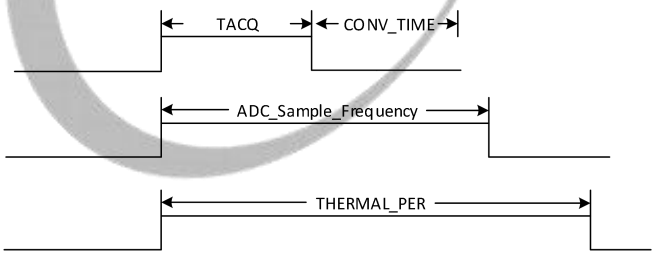
2.14.3.1 Clock Source

Both of THS0 and THS1 get two clock sources: DCXO24M and PCLK. For details about clock configurations, refer to section 2.5 Clock Controller Unit (CCU).

2.14.3.2 Timing Requirements

The following figure shows the timing requirements for the THS module.

Figure 2-43 Thermal Sensor Timing Requirement



CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/24 MHz x 14 Cycles = 0.583 us

TACQ > 1/24 MHz x 24 Cycles

THERMAL_PER > ADC_Sample_Frequency > TACQ + CONV_TIME

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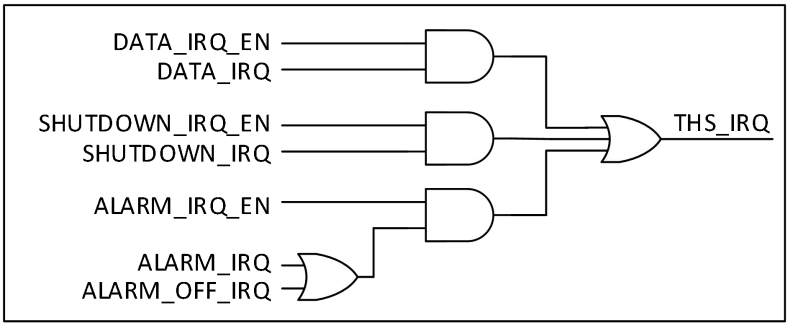
2.14.3.3 Interrupts

The THS module has four interrupt sources: DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ, and ALARM_OFF_IRQ. The following figure shows thermal sensor interrupt sources.

Figure 2-44 Thermal Sensor Controller Interrupt Source



DATA_IRQ

The interrupt is generated when the measured sensor_data is updated.

SHUTDOWN_IRQ

The interrupt is generated when the temperature is higher than the shutdown threshold.

ALARM_IRQ

The interrupt is generated when the temperature is higher than the Alarm_Threshold.

ALARM_OFF_IRQ

The interrupt is generated when the temperature drops to lower than the Alarm_Off_Thershold. It is triggered at the fall edge.

2.14.3.4 THS Temperature Conversion Formula

-40°C to +55°C: T=(sensor_data-2736)/(-13.54)

+55°C to 125°C: T= (sensor_data-2825)/(-15.33)

Unit of T: Celsius degree (°C).

The sensor_data is read from the sensor data register.

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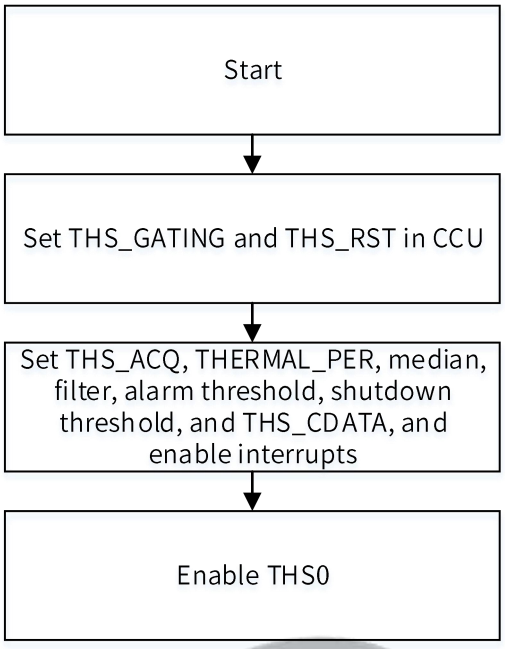
2.14.4 Programming Guidelines

The initial process of the THS is as follows.

Figure 2-45 THS Initial Process



In the final test (FT) stage, the THS is calibrated through the ambient temperature, and the calibration value is written in the SID module. The following table shows the THS0 and THS1 information in the SID.

Table 2-21 THS Information in the SID

eFuse Name	Base Address	Bit	Description
T-sensor Calibration	0x3B-0x3F (72 bits)	35-24	The calibration value of TSENSOR0
		23-12	The calibration value of TSENSOR1
		11-0	ROOM
	0x44-0x48 (72 bits)	35-24	The calibration value of TSENSOR4
		11-0	The calibration value of TSENSOR2

Before enabling THS, read eFuse value and write the value to TSENSORn_CDATA (n=0, 1, 2, or 4).

Query Mode

The following takes THS0 as an example, THS0 and THS1 are the same.

Step 1 Write 0x1 to the bit [16] of THS_BGR_REG to dessert the reset.

Step 2 Write 0x1 to the bit [0] of THS_BGR_REG to open the THS clock.

Step 3 Write 0x2F to the bit [15:0] of THS0_CTRL to set the ADC acquire time.

Step 4 Write 0x1DF to the bit [31:16] of THS0_CTRL to set the ADC sample frequency divider.

Step 5 Write 0x3A to the bit [31:12] of THS0_PER to set the THS work period.

Step 6 Write 0x1 to the bit [2] of THS0_FILTER to enable the temperature convert filter.

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Step 7 Write 0x1 to the bit [1:0] of THS0_FILTER to select the filter type.

Step 8 Read THS eFuse value from SID, then write the eFuse value to TSENSOR4_CDATA to calibrate THS.

Step 9 Write 0x1 to the bit [0] 0f THS0_EN to enable THS.

Step 10 Read the bit [0] of THS0_DATA_INTS. If it is 1, the temperature conversion is complete.

Step 11 Read the bit [11:0] of TSENSOR4_DATA, and calculate the THS temperature based on section 2.14.3.4 THS Temperature Conversion Formula.

Interrupt Mode

The following takes THS0 as an example, THS0 and THS1 are the same.

Step 1 Write 0x1 to the bit16 of THS_BGR_REG to dessert the reset.

Step 2 Write 0x1 to the bit0 of THS_BGR_REG to open the THS clock.

Step 3 Write 0x2F to the bit [15:0] of THS0_CTRL to set the ADC acquire time.

Step 4 Write 0x1DF to the bit [31:16] of THS0_CTRL to set the ADC sample frequency divider.

Step 5 Write 0x3A to the bit [31:12] of THS0_PER to set the THS work period.

Step 6 Write 0x1 to the bit2 of THS0_FILTER to enable the temperature convert filter.

Step 7 Write 0x1 to the bit [1:0] of THS0_FILTER to select the filter type.

Step 8 Read THS eFuse value from SID, and then write the eFuse value to TSENSOR4_CDATA to calibrate THS.

Step 9 Write 0x1 to the bit [0] of THS0_DATA_INTC to enable the interrupt of THS.

Step 10 Set GIC interface based on IRQ 71.

Step 11 Put the interrupt handler address into the interrupt vector table.

Step 12 Write 0x1 to the bit [0] 0f THS0_EN to enable THS.

Step 13 Read the bit [0] of THS0_DATA_INTS. If it is 1, the temperature conversion is complete.

Step 14 Read the bit [11:0] of TSENSOR4_DATA, and calculate the THS temperature based on section 2.14.3.4 THS Temperature Conversion Formula

2.14.5 Register List

THS module includes two groups of registers:

Module Name	Base Address
THS0	0x0200_A000
THS1	0x0200_9400

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2.14.5.1 THS0 Register list

Module Name	Base Address
THS0	0x0200_A000

Register Name	Offset	Description
THS0_CTRL	0x0000	THS0 Control Register
THS0_EN	0x0004	THS0 Enable Register
THS0_PER	0x0008	THS0 Period Control Register
THS0_DATA_INTC	0x0010	THS0 Data Interrupt Control Register
THS0_SHUT_INTC	0x0014	THS0 Shut Interrupt Control Register
THS0_ALARM_INTC	0x0018	THS0 Alarm Interrupt Control Register
THS0_DATA_INTS	0x0020	THS0 Data Interrupt Status Register
THS0_SHUT_INTS	0x0024	THS0 Shut Interrupt Status Register
THS0_ALARMO_INTS	0x0028	THS0 Alarm off Interrupt Status Register
THS0_ALARM_INTS	0x002C	THS0 Alarm Interrupt Status Register
THS0_FILTER	0x0030	THS0 Median Filter Control Register
TSENSOR4_ALARM_CTRL	0x0040	TSENSOR4 Alarm threshold Control Register
TSENSRO4_SHUTDOWN_CTRL	0x0080	TSENSRO4 Shutdown threshold Control Register
TSENSOR4_CDATA	0x00A0	TSENSOR4 Calibration Data
TSENSOR4_DATA	0x00C0	TSENSOR4 Data Register

2.14.5.2 THS1 Regsiter List

Module Name	Base Address
THS1	0x0200_9400

Register Name	Offset	Description
THS1_CTRL	0x0000	THS1 Control Register
THS1_EN	0x0004	THS1 Enable Register
THS1_PER	0x0008	THS1 Period Control Register
THS1_DATA_INTC	0x0010	THS1 Data Interrupt Control Register
THS1_SHUT_INTC	0x0014	THS1 Shut Interrupt Control Register
THS1_ALARM_INTC	0x0018	THS1 Alarm Interrupt Control Register
THS1_DATA_INTS	0x0020	THS1 Data Interrupt Status Register
THS1_SHUT_INTS	0x0024	THS1 Shut Interrupt Status Register
THS1_ALARMO_INTS	0x0028	THS1 Alarm off Interrupt Status Register
THS1_ALARM_INTS	0x002C	THS1 Alarm Interrupt Status Register
THS1_FILTER	0x0030	THS1 Median Filter Control Register

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Register Name	Offset	Description
TSENSOR0_ALARM_CTRL	0x0040	TSENSOR0 Alarm threshold Control Register
TSENSOR1_ALARM_CTRL	0x0044	TSENSOR1 Alarm threshold Control Register
TSENSOR2_ALARM_CTRL	0x0048	TSENSOR2 Alarm threshold Control Register
TSENSOR0&TSENSOR1_SHUTDOWN_CTRL	0x0080	TSENSOR0 & TSENSOR1 Shutdown threshold Control Register
TSENSOR2_SHUTDOWN_CTRL	0x0084	TSENSOR2 Shutdown threshold Control Register
TSENSOR0&TSENSOR1_CDATA	0x00A0	TSENSOR0 & TSENSOR1 Calibration Data
TSENSOR2_CDATA	0x00A4	TSENSOR2 Calibration Data
TSENSOR0_DATA	0x00C0	TSENSOR0 Data Register
TSENSOR1_DATA	0x00C4	TSENSOR1 Data Register
TSENSOR2_DATA	0x00C8	TSENSOR2 Data Register

2.14.6 THS0 Register Description

2.14.6.1 0x0000 THS0 Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS0_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC Acquire Time CLK_IN/ (n + 1) The default value is 2 us.
15:0	R	0x2F	Reserved

2.14.6.2 0x0004 THS0 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS0_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TSENSOR40_EN Enable temperature measurement sensor 0: Disable 1:Enable

2.14.6.3 0x0008 THS0 Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS0_PER
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0008			Register Name: THS0_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature measurement period 4096*(n + 1)/CLK_IN The default value is 10 ms.
11:0	/	/	/

2.14.6.4 0x0010 THS0 Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS0_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TSENSOR4_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR4 0: Disable 1:Enable

2.14.6.5 0x0014 THS0 Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS0_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SHUT_INT_EN Selects shutdown interrupt for TSENSOR4 0: Disable 1:Enable

2.14.6.6 0x0018 THS0 Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS0_ALARM_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM_INT_EN Selects alarm interrupt for TSENSOR4 0: Disable 1:Enable

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2.14.6.7 0x0020 THS0 Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS0_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	TSENSOR4_DATA_IRQ_STS Data interrupt status for TSENSOR4 Write '1' to clear this interrupt.

2.14.6.8 0x0024 THS0 Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS0_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	SHUT_INT_STS Shutdown Interrupt Status for TSENSOR4 Write '1' to clear this interrupt.

2.14.6.9 0x0028 THS0 Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS0_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM_OFF_STS Alarm Interrupt Off Pending for TSENSOR4 Write '1' to clear this interrupt.

2.14.6.10 0x002C THS0 Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS0_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM_INT_STS Alarm Interrupt Pending for TSENSOR4 Write '1' to clear this interrupt.

2.14.6.11 0x0030 THS0 Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS0_FILTER
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0030			Register Name: THS0_FILTER
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

2.14.6.12 0x0040 THS0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM_T_HOT TSENSOR4 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM_T_HYST TSENSOR4 Alarm Threshold for Hysteresis temperature

2.14.6.13 0x0080 TSENSOR4 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: TSENSOR4 _SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x4E9	SHUT_T_HOT TSENSOR4 Shutdown Threshold for Hot Temperature

2.14.6.14 0x00A0 TSENSOR4 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: TSENSOR4 _CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x800	TSENSOR4_CDATA

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Offset: 0x00A0			Register Name: TSENSOR4 _CDATA
Bit	Read/Write	Default/Hex	Description
			TSENSOR4 Calibration Data

2.14.6.15 0x00C0 TSENSOR4 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: TSENSOR4_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR4_DATA Temperature measurement data of TSENSOR4

2.14.7 THS1 Register Description

2.14.7.1 0x0000 THS1 Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS1_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC Acquire Time CLK_IN/ (n + 1) The default value is 2 us.
15:0	R	0x2F	Reserved

2.14.7.2 0x0004 THS1 Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS1_EN
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	TSENSOR2_EN Enable Temperature Measurement Sensor2 0: Disable 1:Enable
1	R/W	0x0	TSENSOR1_EN Enable Temperature Measurement Sensor1 0: Disable 1:Enable
0	R/W	0x0	TSENSOR0_EN Enable Temperature Measurement Sensor0 0: Disable 1:Enable

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2.14.7.3 0x0008 THS1 Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS1_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature Measurement Period 4096*(n + 1)/CLK_IN The default value is 10 ms.
11:0	/	/	/

2.14.7.4 0x0010 THS1 Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS1_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	TSENSOR2_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR2 0: Disable 1:Enable
1	R/W	0x0	TSENSOR1_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR1 0: Disable 1:Enable
0	R/W	0x0	TSENSOR0_DATA_IRQ_EN Selects Temperature measurement data of TSENSOR0 0: Disable 1:Enable

2.14.7.5 0x0014 THS1 Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS1_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	SHUT_INT2_EN Selects Shutdown Interrupt for TSENSOR2 0: Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects Shutdown Interrupt for TSENSOR1

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Offset: 0x0014			Register Name: THS1_SHUT_INTC
Bit	Read/Write	Default/Hex	Description
			0: Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects Shutdown Interrupt for TSENSOR0 0: Disable 1:Enable

2.14.7.6 0x0018 THS1 Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS1_ALARM_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	ALARM_INT2_EN Selects Alarm Interrupt for TSENSOR2 0: Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects Alarm Interrupt for TSENSOR1 0: Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects Alarm Interrupt for TSENSOR0 0: Disable 1:Enable

2.14.7.7 0x0020 THS1 Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS1_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	TSENSOR2_DATA_IRQ_STS Data Interrupt Status for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	TSENSOR1_DATA_IRQ_STS Data Interrupt Status for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	TSENSOR0_DATA_IRQ_STS Data Interrupt Status for TSENSOR0 Write '1' to clear this interrupt.

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2.14.7.8 0x0024 THS1 Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS1_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	SHUT_INT2_STS Shutdown Interrupt Status for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown Interrupt Status for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown Interrupt Status for TSENSOR0 Write '1' to clear this interrupt.

2.14.7.9 0x0028 THS1 Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS1_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	ALARM_OFF2_STS Alarm Interrupt Off Pending for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm Interrupt Off Pending for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm Interrupt Off Pending for TSENSOR0 Write '1' to clear this interrupt.

2.14.7.10 0x002C THS1 Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS1_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	ALARM_INT2_STS Alarm Interrupt Pending for TSENSOR2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm Interrupt Pending for TSENSOR1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS

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Offset: 0x002C			Register Name: THS1_ALARM_INTS
Bit	Read/Write	Default/Hex	Description
			Alarm Interrupt Pending for TSENSOR0 Write '1' to clear this interrupt.

2.14.7.11 0x0030 THS1 Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS1_FILTER
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

2.14.7.12 0x0040 TSENSOR0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: TSENSOR0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT TSENSOR0 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST TSENSOR0 Alarm Threshold for Hysteresis Temperature

2.14.7.13 0x0044 TSENSOR1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: TSENSOR1_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT TSENSOR1 Alarm Threshold for Hot Temperature
15:12	/	/	/

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Offset: 0x0044			Register Name: TSENSOR1_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
11:0	R/W	0x684	ALARM1_T_HYST TSENSOR1 Alarm Threshold for Hysteresis Temperature

2.14.7.14 0x0048 TSENSOR2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: TSENSOR2_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT TSENSOR2 Alarm Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST TSENSOR2 Alarm Threshold for Hysteresis Temperature

2.14.7.15 0x0080 TSENSOR0 & TSENSOR1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: TSENSOR0&TSENSOR1_SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT TSENSOR1 Shutdown Threshold for Hot Temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT TSENSOR0 Shutdown Threshold for Hot Temperature

2.14.7.16 0x0084 TSENSOR2 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0084			Register Name: TSENSOR2 _SHUTDOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT TSENSOR2 Shutdown Threshold for Hot Temperature

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2.14.7.17 0x00A0 TSENSOR0 & TSENSOR1 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: TSENSOR0&TSENSOR1_CDATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x800	TSENSOR1_CDATA TSENSOR1 Calibration Data
15:12	/	/	/
11:0	R/W	0x800	TSENSOR0_CDATA TSENSOR0 Calibration Data

2.14.7.18 0x00A4 TSENSOR2 Calibration Data (Default Value: 0x0000_0800)

Offset: 0x00A4			Register Name: TSENSOR2 _CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x800	TSENSOR2_CDATA TSENSOR2 Calibration Data

2.14.7.19 0x00C0 TSENSOR0 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: TSENSOR0_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR0_DATA Temperature Measurement Data of TSENSOR0

2.14.7.20 0x00C4 TSENSOR1 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: TSENSOR1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TSENSOR1_DATA Temperature Measurement Data of TSENSOR1

2.14.7.21 0x00C8 TSENSOR2 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: TSENSOR2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

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Offset: 0x00C8			Register Name: TSENSOR2_DATA
Bit	Read/Write	Default/Hex	Description
11:0	R	0x0	TSENSOR2_DATA Temperature Measurement Data of TSENSOR2

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2.15 Timer

2.15.1 Overview

The Timer module implements the timing and counting functions, which includes CPUX_TIMER, CPUS_TIMER, and MCU_TIMER. There are 6 timers in TIMER, 3 timers in CPUS_TIMER, and 6 timers in MCU_TIMER.

The Timer module has the following features:

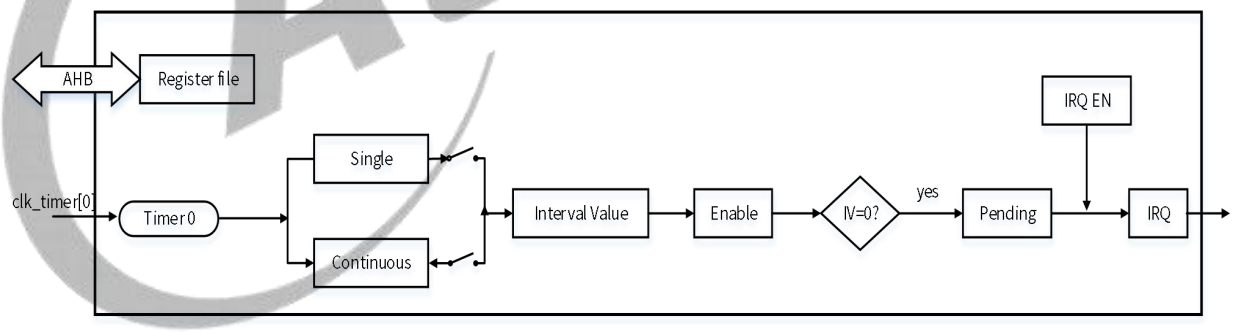
- The AHB port is used to configure the timer register
- Configurable count clock: PRCM/CCU can be switched to 32 kHz, 24 MHz, 16 MHz, and 200 MHz
- Programmable 56-bit down timer
- Supports two timing modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.15.2 Block Diagram

The timer is a 56-bit down counter. The counter value is decremented by 1 on each rising edge of the timer clock.

The following figure shows t NIhe block diagram for the timer.

Figure 2-46 Block Diagram for the Timer



NOTE

timer0 is used for illustration here. Block diagrams for other timers are the same.

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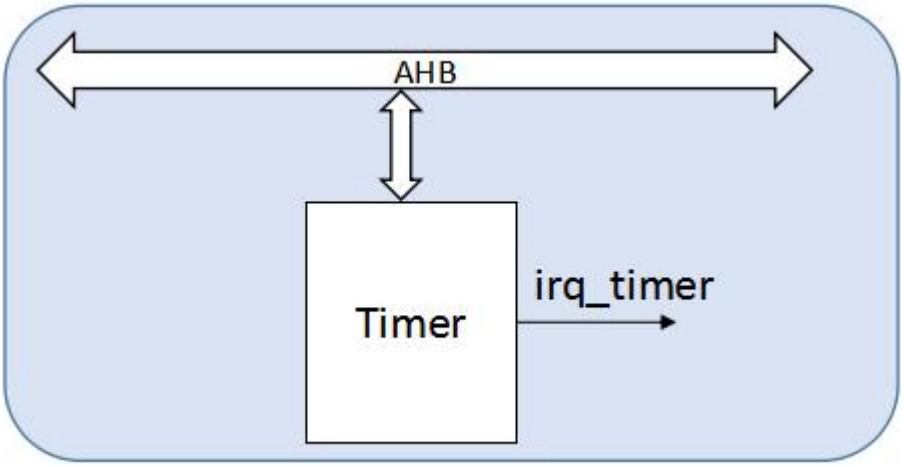
2.15.3 Functional Descriptions

2.15.3.1 Typical Application

The following figure shows the typical application of the Timer module.

Figure 2-47 Timer Typical Application



The Timer is mounted at the AHB bus. The system configures and controls the Timer via the AHB bus.

2.15.3.2 Formula for Calculating the Timer Time

The following formula describes the relationship among timer parameters.

$$T = \frac{\{\text{TIMER\_IVH}, \text{TIMER\_IVL}\} - \{\text{TIMER\_CVH}, \text{TIMER\_CVL}\}}{f_{clk\_timer}}$$

Where,

TIMER_IVH=the higher 24 bits of the interval value, which could be configured by the lower 24 bits of the TIMER_IVH_REG register;

TIMER_IVL=the lower 32 bits of the interval value, which could be configured by the TIMER_IVL_REG register;

TIMER_CVH=the higher 24 bits of the current value, which could be configured by the lower 24 bits of the TIMER_CVH_REG register;

TIMER_CVL=the lower 32 bits of the current value, which could be configured by the TIMER_CVL_REG register;

fclk_timer=the frequency of the timer clock source;

{TIMER_IVH, TIMER_IVL} = 56-bit interval value of the timer;

{TIMER_CVH, TIMER_CVL} = 56-bit current value of the timer.

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2.15.3.3 Timing Modes

The timer has two timing modes: the single counting mode and the periodic mode. You can configure the timing mode via the bit[7] of TIMER_CTRL_REG. The value 0 is for the period mode and value 1 is for the single counting mode.

- Single Counting Mode

In the single counting mode, the timer starts counting from the interval value and generates an interrupt after the counter decreases to 0, and then stops counting. It starts to count again only when the interval value is reloaded.

- Periodic Mode

In the periodic mode, the timer restarts another round of counting after generating the interrupt. It reloads data from the Timer Interval Value and then continues to count.

2.15.4 Programming Guidelines

2.15.4.1 Initializing the Timer

Refer to the following steps to initialize the timer:

Step 1 Configure the timer parameters including the clock source and timing mode by writing TIMER_CTRL_REG. There is no sequence requirement of configuring these parameters.

Step 2 Write the interval value.

a) Write TIMER_IVL bit of TIMER_IVL_REG register and TIMER_IVH bit of TIMER_IVH_REG register to configure the interval value for the timer.

b) Write bit [1] of TIMER_CTRL_REG to load the interval value to the timer. The value of the bit will be cleared automatically after the interval value is loaded.

Step 3 Write bit [0] of TIMER_CTRL_REG to start the timer. Read TIMER_CVL bit of TIMER_CVL_REG register and TIMER_CVH bit of TIMER_CVH_REG register to get the current value of the timer.

NOTE

When performing read or write operations on the current register, operate TIMER_CVL_REG register before TIMER_CVH_REG register.

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2.15.4.2 Processing the Interrupt

Refer to the following steps to process the interrupt:

Step 1 Enable interrupts for the timer: write the enable bit of the corresponding interrupt in TIMER_IRQ_REG for the timer. The timer will generate an interrupt once the count value reaches 0.

Step 2 After the software program enters the interrupt process, write the pending bit of the corresponding interrupt in TIMER_STA_REG to clear the interrupt pending.

Step 3 Resume the interrupt and continue to execute the interrupted process.

2.15.5 Register List

Module Name	Base Address	The value of N
CPUX_TIMER	0x0300 8000	0-5
CPUS_TIMER	0x0709 0400	0-2
MCU_TIMER	0x0712 3000	0-5

Register Name	Offset	Description
TIMER_IRQ_REG	0x0000	Timer IRQ Enable Register
TIMER_STA_REG	0x0004	Timer Status Register
TIMER_SEC_REG	0x0008	Timer Secure Register
TIMER_CTRL_REG	0x0020+0x0020*N	Timer Control Register
TIMER_IVL_REG	0x0024+0x0020*N	Timer Interval Value bit[31:0] Register
TIMER_CVL_REG	0x0028+0x0020*N	Timer Current Value [31:0]bit Register
TIMER_IVH_REG	0x002C+0x0020*N	Timer Interval Value bit[55:32] Register
TIMER_CVH_REG	0x0030+0x0020*N	Timer Current Value [55:32]bit Register

2.15.6 Register Description

2.15.6.1 0x0000 Timer IRQ Enable Register (Default: 0x0000_0000)

Offset: 0x0000			Register Name: TIMER_IRQ_REG
Bit	Read/Write	Default/Hex	Description
31:NUM	/	/	/
NUM-1:0	R/W	0x0	Timer (0-NUM-1) Interrupt Enable 1: Enable 0: Disable

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2.15.6.2 0x0004 Timer Status Register (Default: 0x0000_0000)

Offset: 0x0004			Register Name: TIMER_STA_REG
Bit	Read/Write	Default/Hex	Description
31:NUM	/	/	/
NUM-1:0	R/WC	0x0	Timer (0-NUM-1) Status 1: Pending 0:No effect

2.15.6.3 0x0008 Timer Secure Register (Default: 0x0000_003F)

Offset: 0x0008			Register Name: TIMER_SEC_REG
Bit	Read/Write	Default/Hex	Description
31:NUM	/	/	/
NUM-1:0	R/W	0x3F	Timer (0-NUM-1) Secure Control 1: Secure 0: Non-secure

2.15.6.4 0x0020+0x0020*N(N=0-5) Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x0020+0x0020*N(N=0-5)			Register Name: TIMER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TIMER_MODE Timer Mode 0: Continuous mode. When interval value reached, the timer will restart another round of counting automatically. 1: Single mode. When interval value is reached, the timer will stop counting.
6:2	/	/	/
1	R/W	0x0	TIMER_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TIMER_EN. Timer 0 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It

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Offset: 0x0020+0x0020*N(N=0-5)			Register Name: TIMER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

2.15.6.5 0x0024+0x0020*N(N=0-5) Timer Low Interval Value Register (Default: 0x0000_0000)

Offset: 0x0024+0x0020*N(N=0-5)			Register Name:TIMER_IVL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TIMER_IVL Timer Interval Value bit[31:0] Register

2.15.6.6 0x0028+0x0020*N(N=0-5) Timer Low Current Value Register (Default: 0x0000_0000)

NOTE

- The current value register is a 56-bit register. When read or write the current value, the TIMER_CVL should be read or write first.
- Enable the TIMER_EN.bit (bit [0]) of the TIMER_CTRL_REG register and set the bus clock frequency of the Timer to be twice the function clock frequency before reading the current value register.

Offset: 0x0028+0x0020*N(N=0-5)			Register Name: TIMER_CVL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TIMER_CVL Timer Current Value bit[31:0] Register

2.15.6.7 0x002C+0x0020*N(N=0-5) Timer High Interval Value Register (Default: 0x0000_0000)

Offset: 0x002C+0x0020*N(N=0-5)	Register Name: TIMER_IVH_REG

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Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	TIMER_IVH Timer Interval Value bit[55:32] Register

2.15.6.8 0x0030+0x0020*N(N=0-5) Timer High Current Value Register (Default: 0x0000_0000)

NOTE

Enable the TIMER_EN.bit (bit [0]) of the TIMER_CTRL_REG register and set the bus clock frequency of the Timer to be twice the function clock frequency before reading the current value register.

Offset: 0x0030+0x0020*N(N=0-5)			Register Name: TIMER_CVH_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	TIMER_CVH Timer Current Value bit[55:32] Register

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2.16 Watchdog Timer (WDT)

2.16.1 Overview

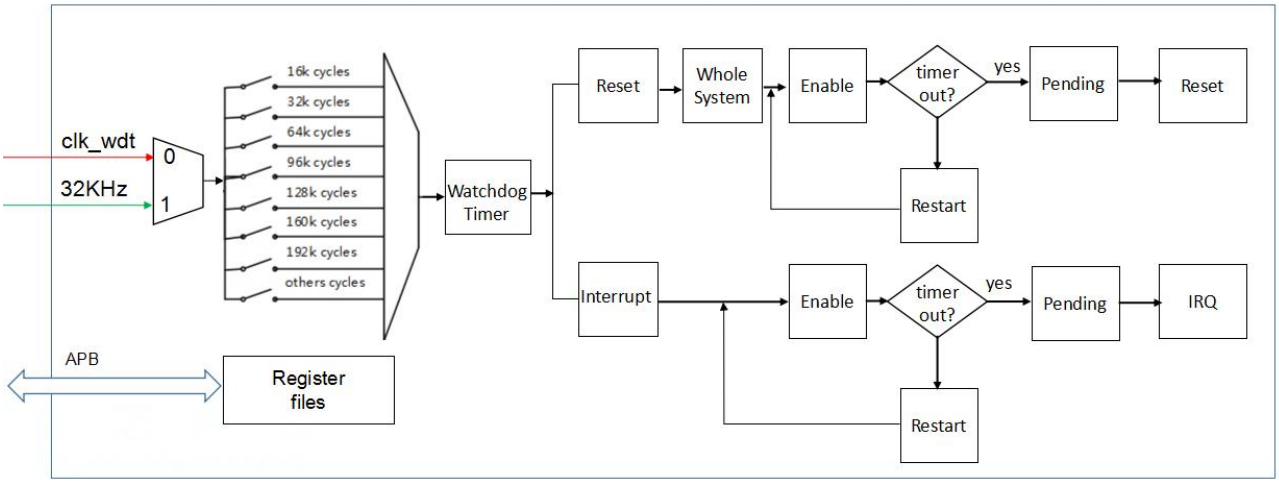
Watchdog is used to transmit a reset signal to reset the entire system after an exception occurs in the system. It has the following features:

- Three watchdog timers: CPUX_WDT in CPUX domain, CPUS_WDT and RISCV_WDT in CPUS domain
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

2.16.2 Block Diagram

The following figure shows the functional block diagram of the watchdog module.

Figure 2-48 Watchdog Block Diagram



2.16.3 Functional Descriptions

2.16.3.1 Clock Sources

The clock source of the watchdog is either LOSC (32 kHz) or HOSC/750 (24 MHz/750). Configure the bit [8] of the WDT_CFG_REG to select a clock source.

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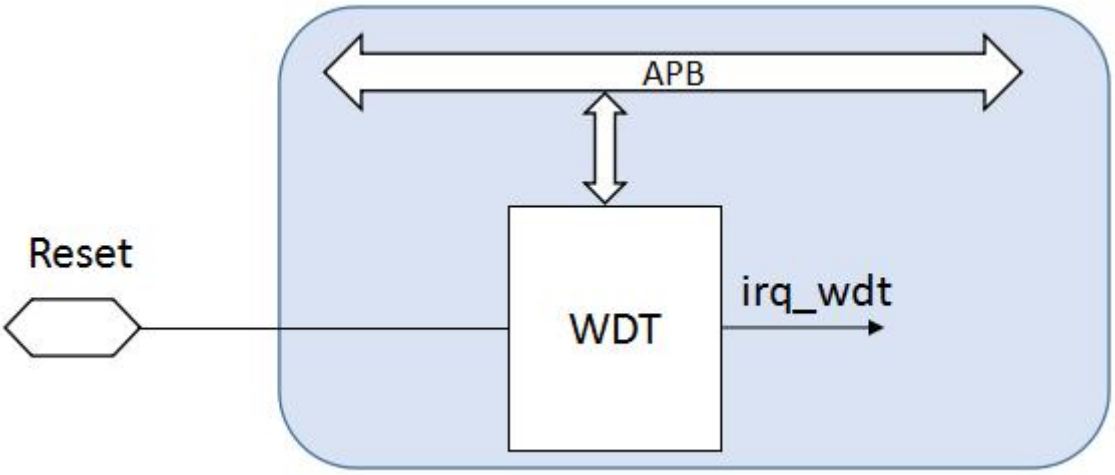
2.16.3.2 Typical Application

Figure 2-49 Watchdog Application Diagram



Watchdog configures register by APB bus.

The system configures the time of watchdog, if the system has no timing for restart watchdog (such as bus hang dead), then watchdog sends out watchdog reset external signal to reset system; meanwhile watchdog outputs signal to RESET pad to reset PMIC.

2.16.3.3 Operating Modes

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. The watchdog has two operating modes.

- Interrupt mode

The bit [1:0] of the WDT_CFG_REG is set to 0x2, when the counter value reaches 0 and the bit [0] of the WDT_IRQ_EN_REG is written to 1, the watchdog generates an interrupt, the watchdog enters into interrupt mode.

- Reset mode

The bit [1:0] of the WDT_CFG_REG is set to 0x1, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

2.16.4 Programming Guidelines

2.16.4.1 Initializing the Watchdog

Follow the steps below to initialize the watchdog:

Step 1 Configure the bit [1:0] of the WDT_CFG_REG to configure the generation of the interrupts or the output of reset signal.

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Step 2 Configure the bit [7:4] of the WDT_MODE_REG to configure the initial count value.

Step 3 Write the bit [0] of the WDT_MODE_REG to 1 to enable the watchdog.

2.16.4.2 Processing the Interrupt

Follow the steps below to process the interrupt:

Step 1 Write the bit [0] of the WDT_IRQ_EN_REG to 1 to enable the interrupt.

Step 2 After enter the interrupt process, write the bit [0] of the WDT_IRQ_STAT to 1 to clear the interrupt pending, and execute the process of waiting for the interrupt.

Step 3 Resume the interrupt and continue to execute the interrupted process.

2.16.4.3 Resetting the Watchdog

In the following instance making configurations for WDT: configure clock source as HOSC/750, configure Interval Value as 1s and configure Watchdog Configuration as to whole system. This instance indicates that reset system after 1s.

```
writel (0x16AA_0001, WDT_CFG_REG);                          //To whole system
writel (0x16AA_0010, WDT_MODE_REG);                         //Interval Value set 1s
writel(readl(WDT_MODE_REG) |(1<<0)|(0x16AA<<16), WDT_MODE_REG);      //Enable WDT
```

2.16.4.4 Restarting the Watchdog

In the following instance making configurations for WDT: configure clock source as HOSC/750, configure Interval Value as 1s and configure Watchdog Configuration as to whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
write (0x16AA_0001, WDT_CFG_REG);                           //To whole system
write (0x16AA_0010, WDT_MODE_REG);                          //Interval Value set 1s
writel(readl(WDT_MODE_REG) |(1<<0)|(0x16AA<<16), WDT_MODE_REG);   //Enable WDT
----other codes---
writel(readl(WDT_CTRL_REG) |(0xA57<<1) | (1<<0), WDT_CTRL_REG); //Write 0xA57 at Key Field and Restart WDT
```

2.16.5 Register List

Module Name	Base Address
CPUX_WDT	0x0205 0000
CPUS_WDT	0x0702 0400
RISCV_WDT	0x0713 2000

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Register Name	Offset	Description
WDT_IRQ_EN_REG	0x0000	WDT IRQ Enable Register
WDT_IRQ_STAT	0x0004	WDT Status Register
WDT_SRST_REG	0x0008	WDT Software Reset Register
WDT_CTRL_REG	0x000C	WDT Control Register
WDT_CFG_REG	0x0010	WDT Configuration Register
WDT_MODE_REG	0x0014	WDT Mode Register
WDT_OCFG_REG	0x0018	WDT Output Configuration Register

2.16.6 Register Description

2.16.6.1 0x0000 WDT IRQ Enable Register (Default: 0x0000_0000)

Offset: 0x0000			Register Name: WDT_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	WDT Interrupt Enable

2.16.6.2 0x0004 WDT Status Register (Default: 0x0000_0000)

Offset: 0x0004			Register Name: WDT_IRQ_STAT
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	WDT Status WDT IRQ Pending.set 1 to the bit will clear it. 1:pending,WDT interval value is reched 0:No effect

2.16.6.3 0x0008 WDT Software Reset Register Register (Default: 0x0000_0000)

Offset: 0x0008			Register Name: WDT_SRST_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	KEY Field This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15:1	/	/	/
0	R/W	0x0	Soft Reset Enable 0: De-assert 1: Reset System

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Offset: 0x0008			Register Name: WDT_SRST_REG
Bit	Read/Write	Default/Hex	Description
			If this bit is used for system reset, the watchdog should be disabled.

2.16.6.4 0x000C WDT Control Register Register (Default: 0x0000_0000)

Offset: 0x000C			Register Name: WDT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:1	W	0x0	Watchdog Key Field Should be written at value 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	Watchdog Restart 0: No effect 1: Restart the Watchdog 0

2.16.6.5 0x0010 WDT Configuration Register Register (Default: 0x0000_0001)

Offset: 0x0010			Register Name: WDT_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 15:0 can be written with the new value.
15:9	/	/	/
8	R/W	0x0	WDT Clock select 1: LOSC (32 kHz) 0: HOSC / 750 (24MHz/750)
7:2	/	/	/
1:0	R/W	0x1	WDT Configuration 00: / 01: to whole system 10: only interrupt 11: /

2.16.6.6 0x0014 WDT Mode Register Register (Default: 0x0000_0000)

Offset: 0x0014			Register Name: WDT_MODE_REG
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0014			Register Name: WDT_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD Key Field. This field should be filled with 0x16AA, and then the bit 15:0 can be written with the new value.
15:8	/	//	/
7:4	R/W	0x0	WDT Interval Value. Watchdog clock source is HOSC / 750. If the clock source is turned off, WDT will not work. 0000: 16k cycles (0.5s) 0001: 32k cycles (1s) 0010: 64k cycles (2s) 0011: 96k cycles (3s) 0100: 128k cycles (4s) 0101: 160K cycles (5s) 0110: 192k cycles (6s) 0111: 256k cycles (8s) 1000: 320k cycles (10s) 1001: 384k cycles (12s) 1010: 448k cycles (14s) 1011: 512k cycles (16s) 1100: / 1101: / 1110: / 1111: /
3:1	/	/	
0	R/W	0x0	Watchdog Enable. 0: disable ; 1: enable

2.16.6.7 0x0018 WDT Output Configuration Register Register (Default: 0x0000_001F)

Offset: 0x0018			Register Name: WDT_OCFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 11:0 can be written with the new value.
15:12	/	/	/
11:0	R/W	0x1F	WDT OUTPUT CONFIG WDT Reset Valid Time Configuraion T=1/32ms*(N+1)

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Offset: 0x0018			Register Name: WDT_OCFG_REG
Bit	Read/Write	Default/Hex	Description
			Default 1ms

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3 Memory

3.1 RAW NAND Flash Controller (NDFC)

The NDFC is the NAND flash controller which supports all NAND flash memory available in the market. New types of flash can be supported by software re-configuration.

The NDFC has a built-in on-the-fly error correction code (ECC) feature with BCH algorithm to enhance the reliability. It can detect and correct up to 80 bits' error per 1024 bytes' data. With the on-chip BCH code ECC circuit, the CPU is freed for other tasks. You can disable the ECC feature by software.

The NDFC supports transferring data via the DMA or CPU memory-mapped IO. It provides automatic timing control for reading or writing external Flash and maintains the proper relativity for CLE, CE#, and ALE control signal lines. There are three modes for serial read access: the mode0 is for conventional serial access, the mode1 is for EDO type, and the mode2 is for extension EDO type. The NDFC can monitor the status of the R/B# signal line.

Block management and wear leveling management are implemented in software.

The NDFC has the following features:

- Supports all SLC/MLC flash and EF-NAND memory available in the market
- Supports configuring randomize seed by software
- Software configuration method for various systems and memory types
- Up to 8-bit data bus width
- Supports 2CE/2RB
- Supports 1024, 2048, 4096, 8192, 16384, and 32768 bytes' size per page
- Conventional and EDO serial access method for serial reading Flash
- 80 bits/1 KB on-the-fly BCH code ECC check and error correction
- Output bits' number information about the corrected errors
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers, and interrupt is supported
- One command FIFO
- Two 256x32-bit RAM for Pipeline Procession
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0, and Toggle DDR2.0 RAW NAND FLASH
- Maximum IO rate of 50 MHz in SDR mode, 100 MHz in DDR1.0 and 150MHz in DDR2.0 mode
- Self-debug for NDFC debug

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3.2 SDRAM controller (DRAMC)

The DRAMC has the following features:

- 32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X interface
- Memory capacity up to 4GB
- Clock frequency up to 1066 MHz for DDR3, DDR3L, and LPDDR3
- Clock frequency up to 1200 MHz for DDR4, LPDDR4, and LPDDR4x
- 17 address lines and three bank address lines per channel
- Generate initialization and refresh sequences automatically
- Runtime-configurable parameters setting for application flexibility
- Programmable priority of transferring through multiple ports
- Supports random reading or writing
- Supports Dynamic Frequency Setting(DFS) via hardware
- Supports SSC

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3.3 SD/MMC Host Controller (SMHC)

3.3.1 Overview

The SMHC controls the read/write operations on the secure digital (SD) cards, multimedia cards (MMC), and various extended devices that is based on the secure digital input/output (SDIO) protocol. The processor provides three SMHC interfaces for controlling the SD cards, MMCs, and SDIO devices.

The SMHC has the following features:

- Three SD/MMC host controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (SD3.0)
  - SMHC1, compliant with the protocol Secure Digital I/O (SDIO3.0)
  - SMHC2, compliant with the protocol Multimedia Card (eMMC5.1)
  - Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 5.1)
- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 supports the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Supports HS400 mode and HS200 mode
  - Maximum performance
    - SDR mode 200MHz@1.8V IO pad
    - DDR mode 200MHz@1.8V IO pad
    - SDR mode 50MHz@3.3V IO pad
    - DDR mode 50MHz@3.3V IO pad
- Support block size of 1 to 65535 bytes
- Support hardware CRC generation and error detection
- Supports eMMC boot operation and alternative boot operation
- Supports command queue for eMMC V5.1 device
- Supports serial CMDQ mode for SMHC0/2
- Supports host pull-up control

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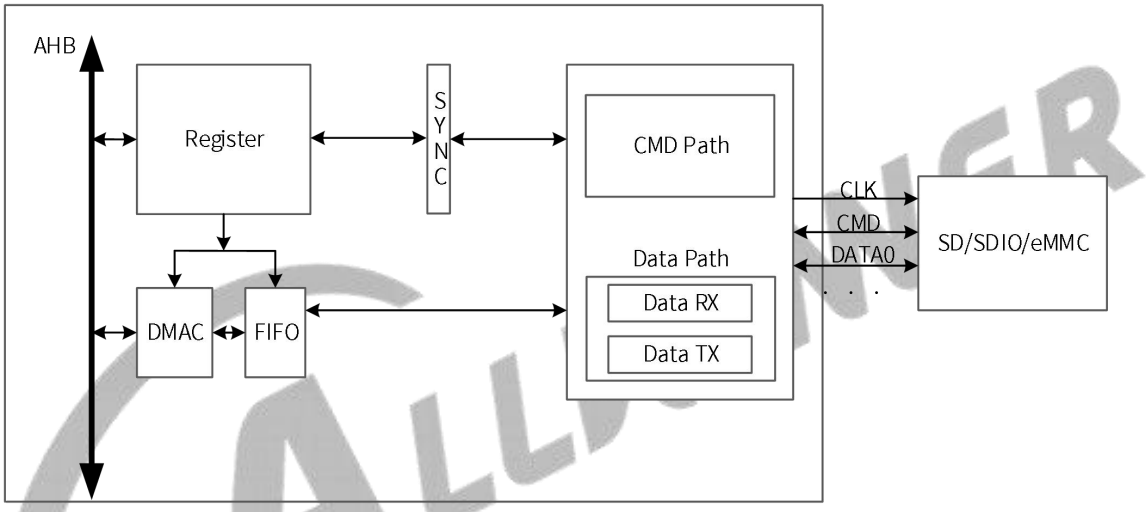
- Supports Command Completion signals and interrupts to host processor, and Command Completion signal disable feature
- Programmable baud rate
- Descriptor-based internal DMA controller
- Internal time-multiplexing 1 KB FIFO for SMHC0/2 transmitting and receiving
- Internal time-multiplexing 4 KB FIFO for SMHC1 transmitting and receiving

3.3.2 Block Diagram

The following figure shows a block diagram of the SMHC.

Figure 3-1 SMHC Block Diagram



SMHC contains the following sub-blocks:

Table 3-1 SMHC Sub-blocks

Sub-block	Description
Register	Used to configure the control signal for reading or writing the SD/SDIO/eMMC.
DMAC	The DMA controller that controls the data transfer between the memory and SMHC.
FIFO	A buffer for the data stream between the memory and the SMHC asynchronous clock domain.
SYNC	Synchronizes the signals from the AHB clock domain to the SMHC clock domain.
CMD Path	Sends commands to or receives commands from the SD/SDIO/eMMC.
Data Path	Consists of Data TX and Data RX sub-modules. The Data TX sends data blocks and the CRC codes to the SD/SDIO/eMMC. The Data RX receives data blocks and the CRC codes from the SD/SDIO/eMMC.

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3.3.3 Functional Description

3.3.3.1 External Signals

The following table describes the external signals of SMHC.

Table 3-2 SMHC External Signals

Signal Name	Description	Type
SMHC0		
SDC0-CMD	Command Signal for SD Card	I/O, OD
SDC0-CLK	Clock for SD Card	O
SDC0-D[3:0]	DATA INPUT AND OUTPUT FOR SD CARD	I/O
SMHC1		
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	I/O
SMHC2		
SDC2-CMD	Command Signal for eMMC	I/O, OD
SDC2-CLK	Clock for eMMC	O
SDC2-D[8:0]	Data Input and Output for eMMC	I/O
SDC2-RST	Reset for eMMC	O
SDC2-DS	Clock input for eMMC	I

3.3.3.2 Clock Sources

The SMHC0/1/2 has 5 different clock sources. You can select one of them as the SMHC clock source. The following table describes the clock sources of the SMHC.

For clock setting, configurations, and gating information, refer to section 2.5 Clock Controller Unit (CCU).

Table 3-3 SMHC0/1 Clock Sources

Clock Sources	Description	Module
HOSC	24 MHz Crystal	CCU
PLL_PERI0(400M)	Peripheral Clock, the default value is 400 MHz	
PLL_PERI0(300M)	Peripheral Clock, the default value is 300 MHz	
PLL_PERI1(400M)	Peripheral Clock, the default value is 400 MHz	
PLL_PERI1(300M)	Peripheral Clock, the default value is 300 MHz	

Table 3-4 SMHC2 Clock Sources

Clock Sources	Description	Module
HOSC	24 MHz Crystal	CCU
PLL_PERI0(800M)	Peripheral Clock, the default value is 800 MHz	
PLL_PERI0(600M)	Peripheral Clock, the default value is 600 MHz	

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Clock Sources	Description	Module
PLL_PERI1(800M)	Peripheral Clock, the default value is 800 MHz	
PLL_PERI1(600M)	Peripheral Clock, the default value is 600 MHz	

3.3.3.3 Timing Diagram

Refer to the following relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard (4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard (5.0)

3.3.3.4 Data Path

The SMHC and SD/SDIO/eMMC contains the following interface buses: CLK, CMD, and DATA 1/4. During one clock cycle, the SMHC can transmit one-bit command with one or two bits' data in 1-ch DATA mode, or four or eight bits' data in 4-ch DATA mode. The CMD is a bidirection channel for initializing the SD/SDIO/eMMC and transmitting commands. It can work in both the open-drain mode and push-pull mode. The DATA is also a bidirection channel. It works in the push-pull mode.

- Reading Data from the SD/SDIO/eMMC

The register configures the signals for the read operation, and synchronize the signals to the SMHC clock domain. Then the Data RX reads data from the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses and writes the data in the FIFO. After that, the DMAC transfers the data from the FIFO to the memory.

- Writing Data to the SD/SDIO/eMMC

The register configures the signals for the write operation, and synchronize the signals to the SMHC clock domain. Then the DMAC reads data from the memory and writes the data to the FIFO. After that, the Data TX reads the data from the FIFO and writes the data to the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses.

3.3.3.5 Package Format

Data transfer over the SD/eMMC bus is based on command and data bitstreams that are initiated by a start bit and terminated by a stop bit. There are three types of SD/eMMC packets: command token, response token, and data packet.

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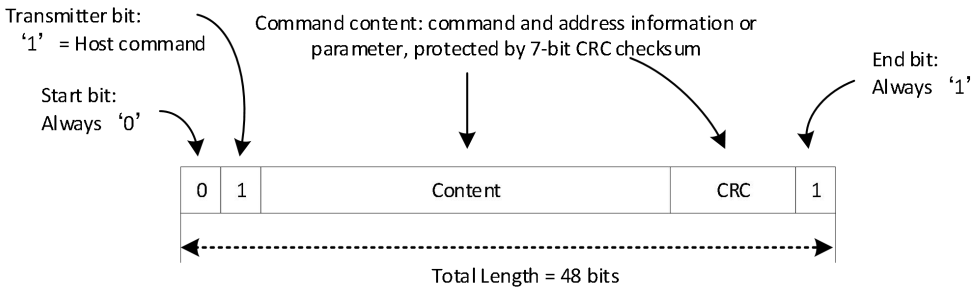
Command Tokens

The command token starts an operation. A command is sent from the host to a device. It is transferred serially on the CMD line. Command tokens have the following coding scheme:

Figure 3-2 Command Token Format



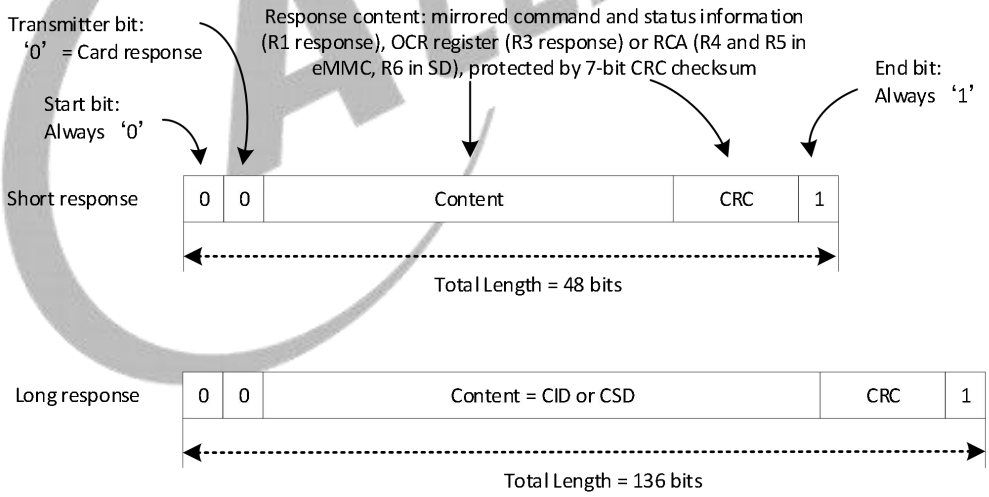
Each command token has 48 bits, preceded by a start bit ('0') and succeeded by an end bit ('1'). To detect transmission errors, each token is protected by CRC bits.

Response Tokens

After receiving a command, the card returns a 48-bit or 136-bit response based on the command type.

A response token is sent from the device to the host as an answer to a previously received command. It is transferred serially on the CMD line.

Figure 3-3 Response Token Format



Data Packet

Data can be transferred from the device to the host or vice versa. Data are transferred via the data lines.

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Figure 3-4 Data Packet Format for SDR

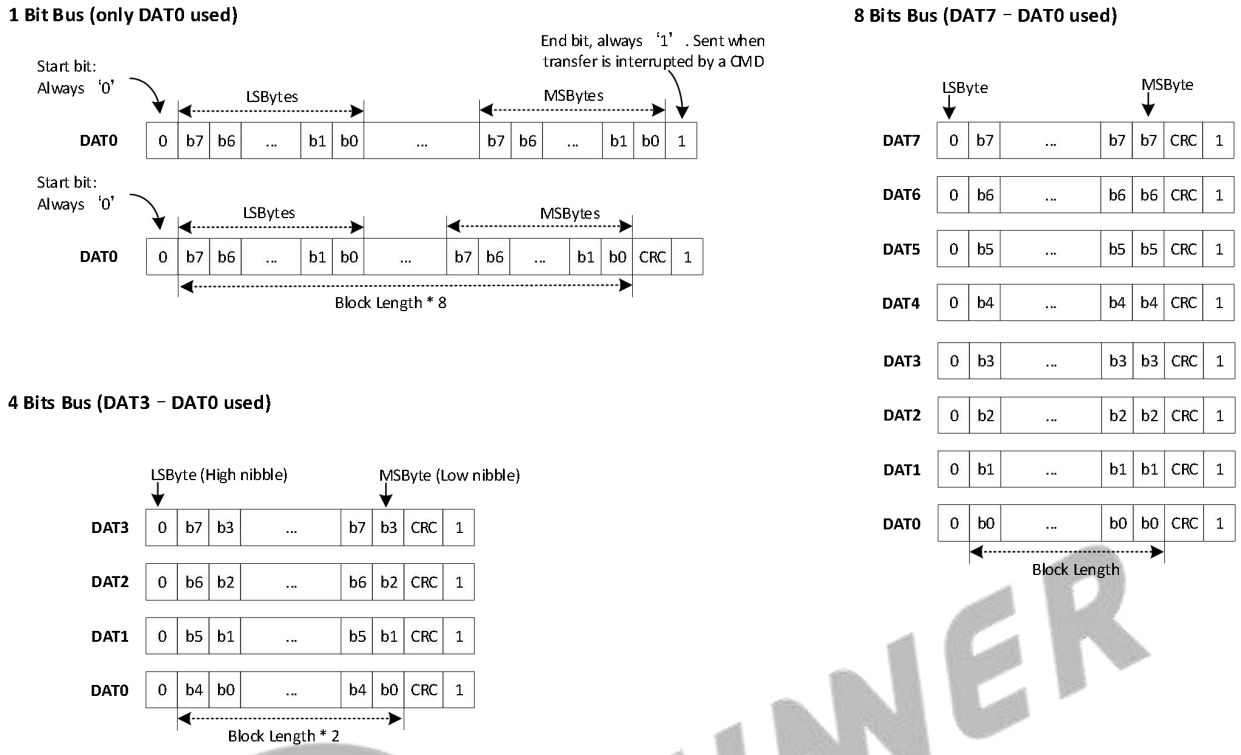

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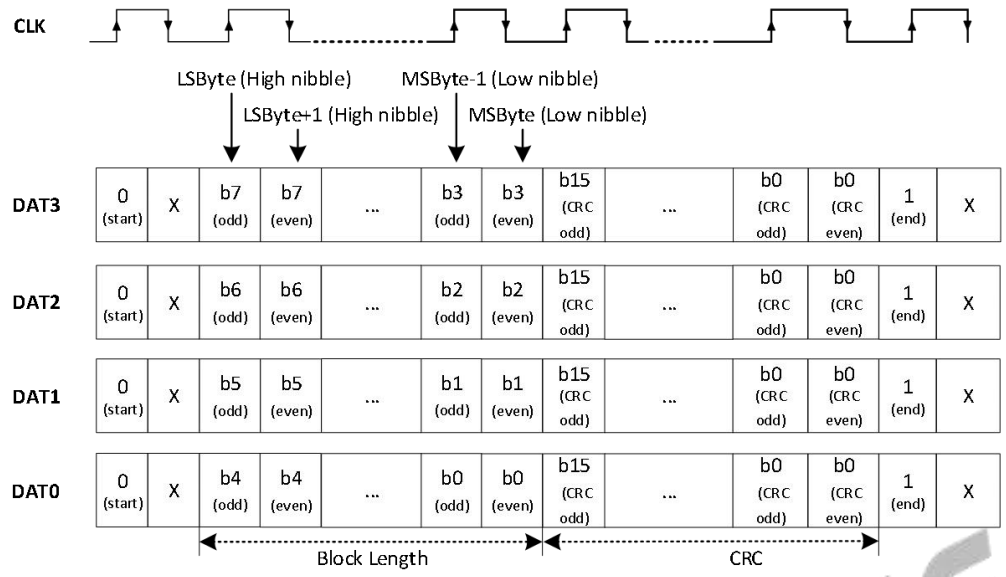
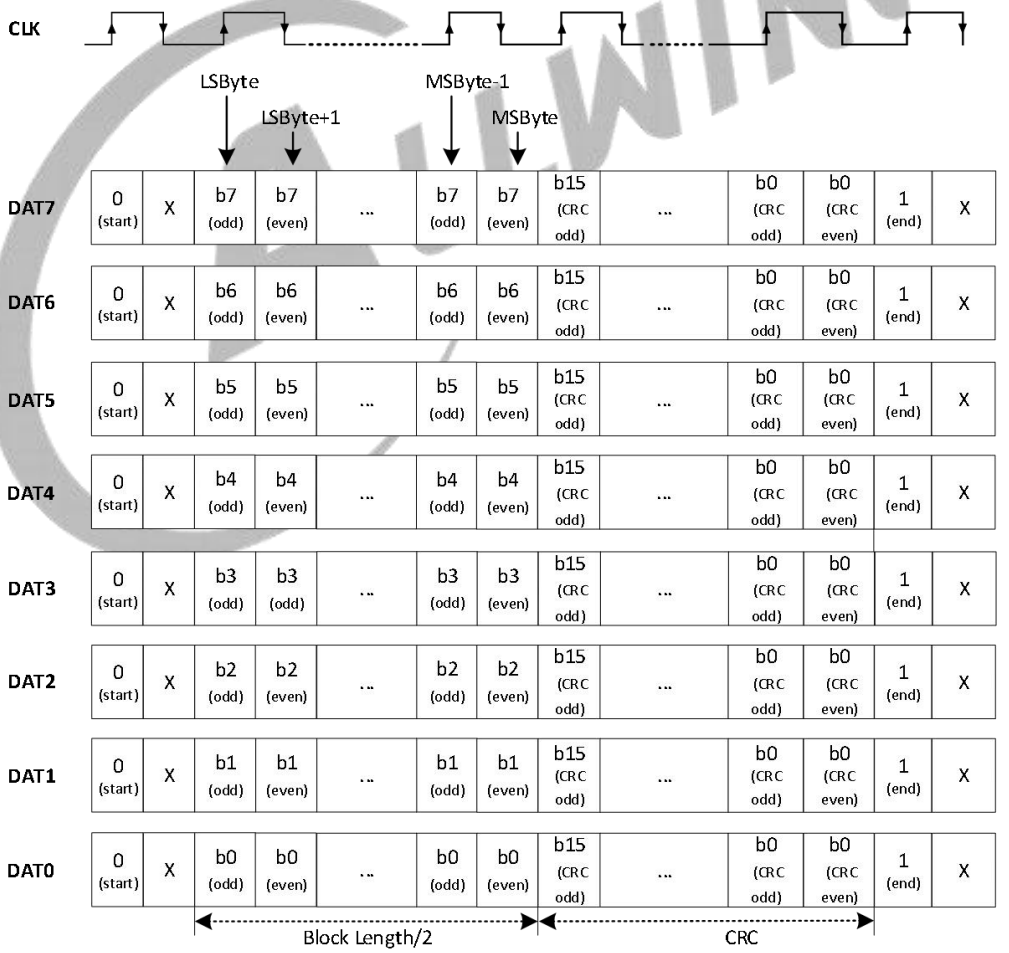
Figure 3-5 Data Packet Format for DDR

4 Bits Bus DDR (DAT3 – DAT0 used)



8 Bits Bus DDR (DAT7 – DAT0 used)



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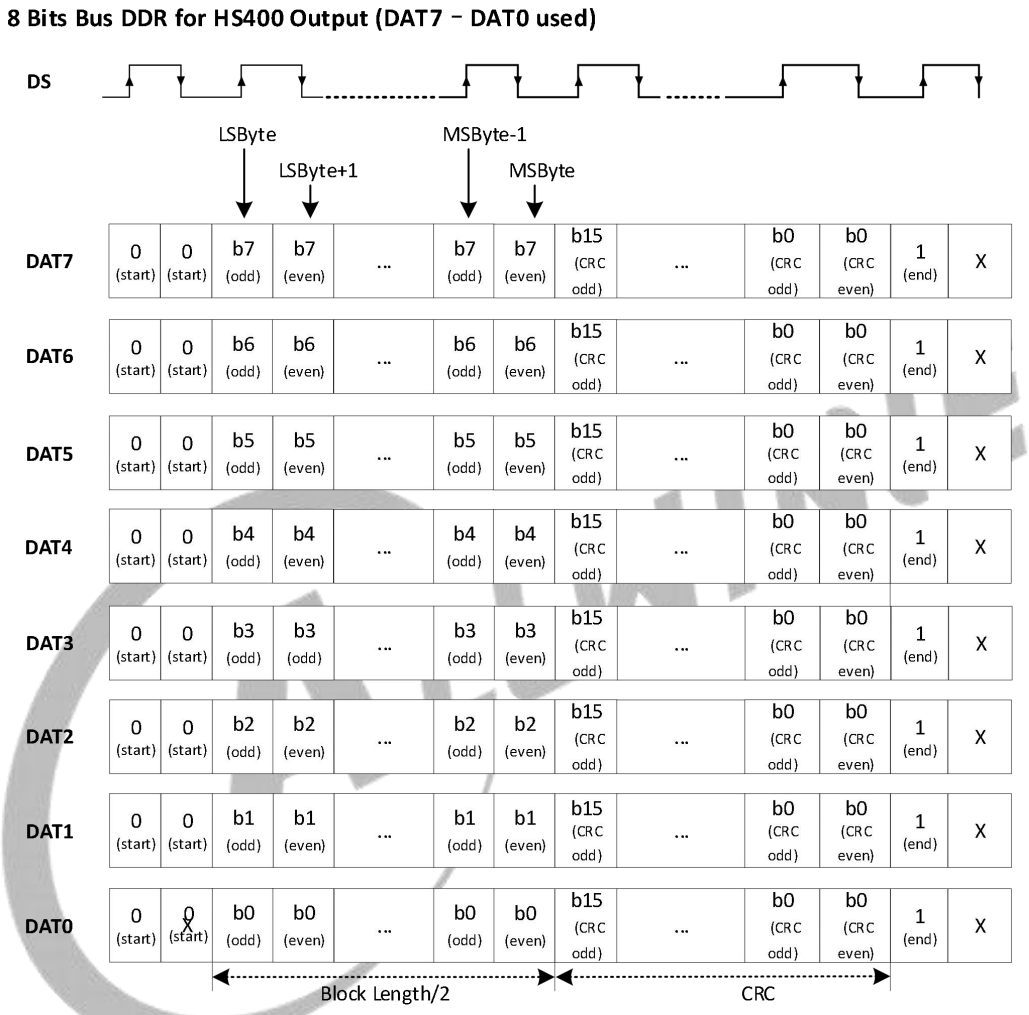
NOTE

- Bytes data are not interleaved but CRCs are interleaved.
- Start and end bits are only valid on the rising edge (“X” indicates “undefined”).

Figure 3-6 Data Packet Format for DDR in HS400 Mode



NOTE

- Bytes data are not interleaved but CRCs are interleaved.
- Start bits are valid when Data Strobe is High and Low.
- End bits are only valid when Data Strobe is High (“X” indicates “undefined”).

Data Transfer

Data transfers to or from the SD/eMMC card are done in blocks. Single and multiple block operations are widely used during data transfer.

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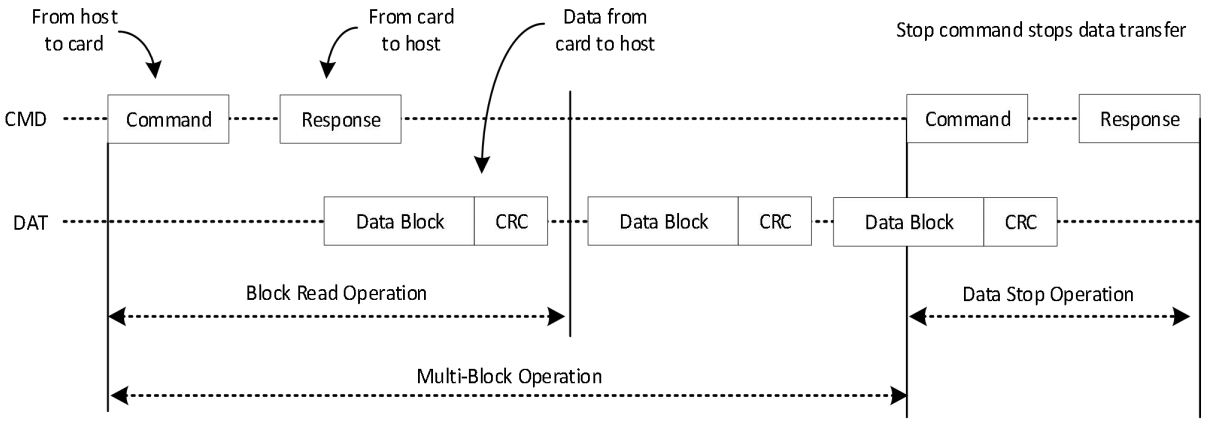
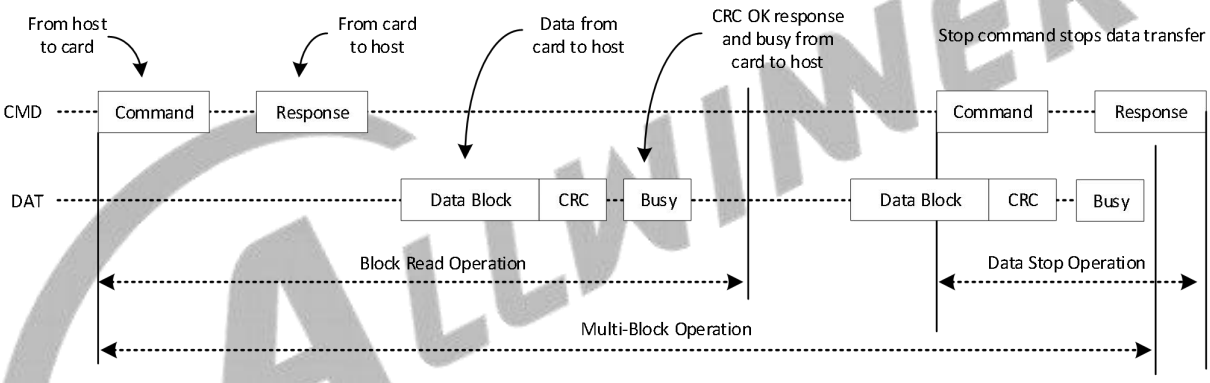
The following figure shows the single-block and multi-block read operation.

Figure 3-7 Single-Block and Multi-Block Read Operation



The following figure shows the single-block and multi-block write operation.

Figure 3-8 Single-Block and Multi-Block Read Operation



3.3.3.6 Phase Offset of the Command and Data

To obtain the command phase or data phase in output timing, follow the steps blow:

Step 1 Configure the MODE_SEL (bit [31]) andor HS400_NEW_SAM_EN (bit [0]) of SMHC_NTSR (offset: 0x005C) to choose the timing mode.

Step 2 Configure the DAT_DRV_PH_SEL (bit [17]) to select data drive phase offset and configureor CMD_DRV_PH_SEL (bit [16]) to select command drive phase offset inof SMHC_DRV_DL (offset: 0x0140) to select data or command drive phase offset.

The following table shows the specific configuration of command and data location.

Table 3-5 Command and Data Location

Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset

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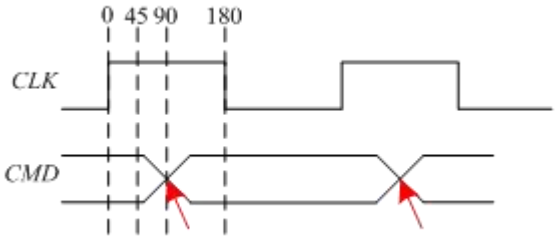
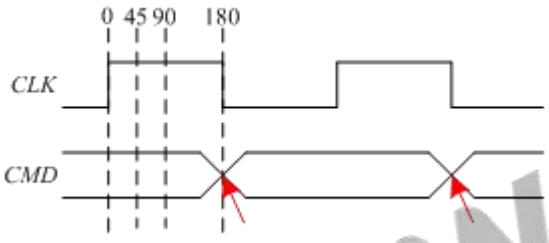
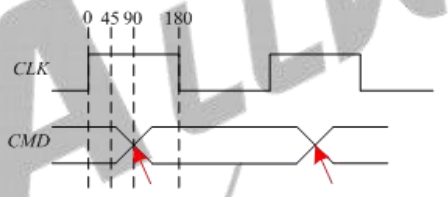
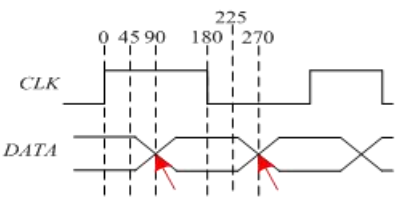
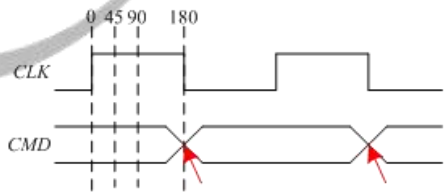
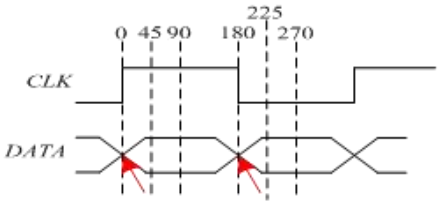
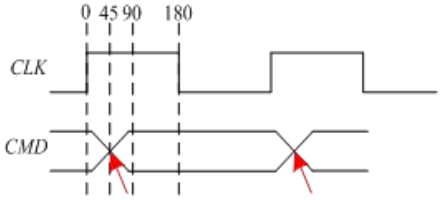
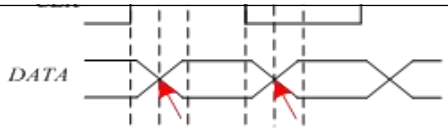
Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
SDR	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data updates at 180 degrees.
DDR4 (1x mode: 0x5c[31]=0)	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 0 or 180 degrees.
DDR4 (2x mode: 0x5c[31]=1)	0		

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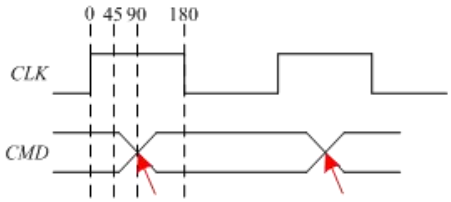
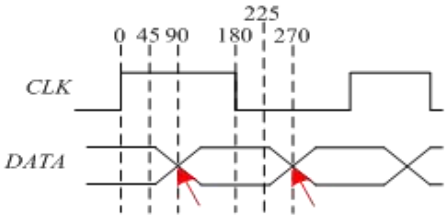
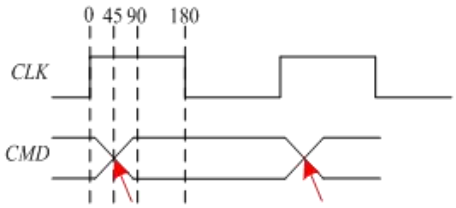
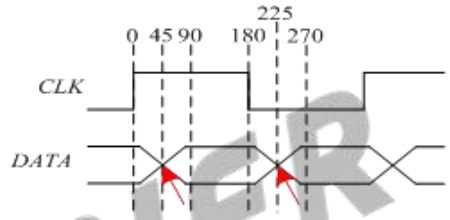
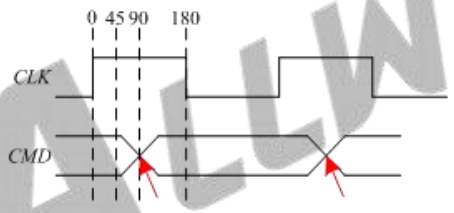
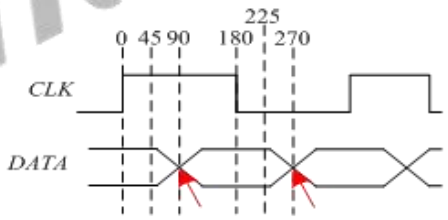
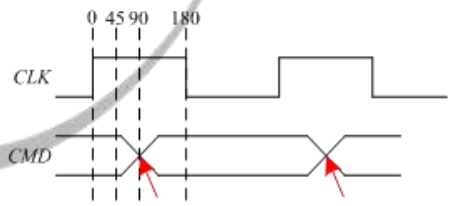
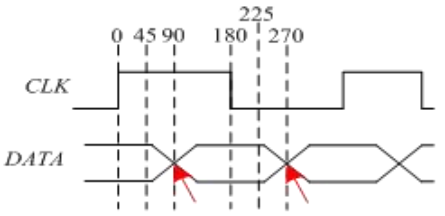
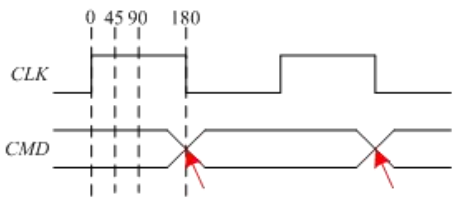
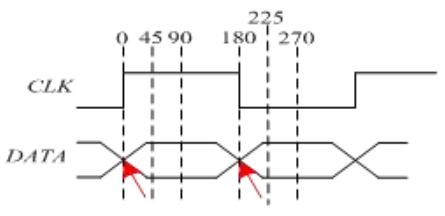
Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
		The Command updates at 45 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 45 degrees.	The data update at 90 degrees.
DDR8	0		
		The Command updates at 45 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 90 degrees.	The data update at 90 degrees.
HS400 (1x mode: 0x5c[0] =0)	0		
		The Command updates at 90 degrees.	The data update at 90 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 0 or 180 degrees.

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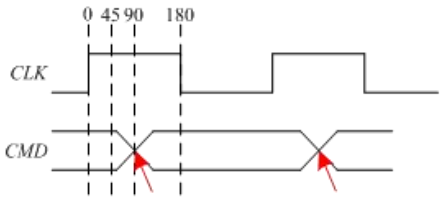
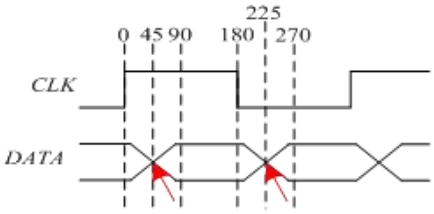
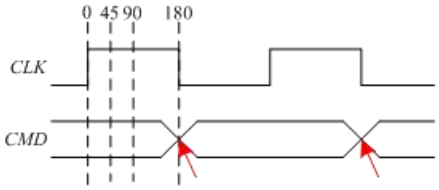
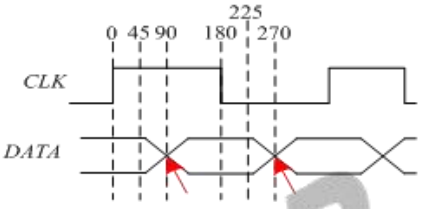
Timing Mode	DRV	Command Drive Phase offset	Data Drive Phase offset
HS400 (2x mode: 0x5c[0] =1)	0		
		The Command updates at 90 degrees.	The data update at 45 degrees.
	1		
		The Command updates at 180 degrees.	The data update at 90 degrees.

3.3.3.7 Internal DMA Controller Description

The SMHC has an internal DMA controller (IDMAC) to transfer data between the host memory and SMHC port. With a descriptor, the IDMAC can efficiently move data from the source to destination by automatically loading the next DMA transfer arguments, which needs less CPU intervention. Before transferring data in the IDMAC, the Host CPU should construct a descriptor list, configure arguments of every DMA transfer, and then launch the descriptor and start the DMA.

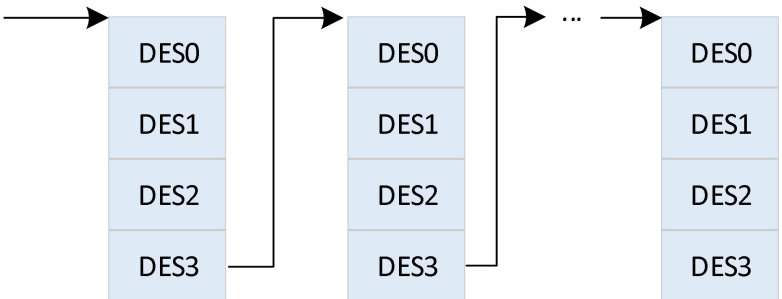
The IDMAC has an interrupt controller. When enabled, it generates an interrupt to the Host CPU in situations such as data transmission is completed or some error is happened.

IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

The following figure shows the internal formats of a descriptor.

Figure 3-9 IDMAC Descriptor Structure Diagram



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This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 corresponds to the [31:0] bits, DES1 corresponds to the [63:32] bits, DES2 corresponds to the [95:64] bits, and DES3 corresponds the [127:96] bits in a descriptor.

The following table shows the bit definition of DES0.

Table 3-6 DES0 Definition

Bits	Name	Description
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when the transfer is over. **Note: After this bit is cleared to 0, the Host CPU is able to read the transferred data or initiate next transfer by launching a new descriptor.**
30	ERROR	ERR_FLAG When some errors happen in transfer, this bit will be set to 1.
29:5	/	/
4	Chain Flag	CHAIN_MOD When set to 1, this bit indicates that the second address in the descriptor is the next descriptor address. It must be set to 1.
3	First DES Flag	FIRST_FLAG When set to 1, this bit indicates that this descriptor contains the first buffer of data. It must be set to 1 in the first DES.
2	Last DES Flag	LAST_FLAG When set to 1, this bit indicates that the buffers this descriptor points to are the last data buffer.
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set to 1, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer the descriptor points to.
0	/	/

The following table shows the bit definition of DES1.

Table 3-7 DES1 Definition

Bits	Name	Description
31:13	/	/
12:0	Buffer size	BUFF_SIZE The bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this field is 0, the DMA ignores this buffer and proceeds to the next descriptor.

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The following table shows the bit definition of DES2.

Table 3-8 DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR The bits indicate the physical address of the data buffer. It is a word address.

The following table shows the bit definition of DES3.

Table 3-9 DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR The bits indicate the pointer to the physical memory where the next descriptor is present. It is a word address.

3.3.3.8 Calibrating the Delay Chain

There are two delay chains in SMHC: data strobe delay chain and sample delay chain.

- Data strobe delay chain: used to generate delay to make proper timing between Data Strobe and data signals.
- Sample delay chain: used to generate delay to make proper timing between the internal card clock signal and data signals.

Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

Follow the steps below to calibrate the delay chain:

Step 1 Enable SMHC. In order to calibrate the delay chain by the operation registers in SMHC, the SMHC must be enabled through SMHC Bus Gating Reset Register and SMHCx Clock Register(x=0, 1, or 2).

Step 2 Configure a proper clock for SMHC. The delay chain calibration is based on the clock for SMHC from Clock Control Unit (CCU). The delay chain calibration is an internal function in SMHC and needs no devices. So it is unnecessary to open the clock signal for devices. The recommended clock frequency is 200 MHz.

Step 3 Set proper initial delay value. Writing 0xA0 to delay control register enables Delay Software Enable (bit [7]) and sets initial delay value 0x20 to Delay chain (bit [5:0]). Then write 0x0 to delay control register to clear the value.

Step 4 Write 0x8000 to delay control register to start calibrating the delay chain.

Step 5 Wait until the flag (bit14 in delay control register) of calibration done is set. The number of delay cells is shown at bit [13:8] in delay control register. The delay time generated by

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these delay cells is equal to the cycle of the SMHC clock nearly. This value is the result of calibration.

Step 6 Calculate the delay time of one delay cell according to the cycle of the SMHC clock and the result of calibration.

3.3.4 Programming Guidelines

3.3.4.1 Initializing SMHC

Before data and commands are exchanged between a card and the SMHC, the SMHC needs to be initialized. Follow the steps below to initialize the SMHC:

Step 1 Configure the corresponding GPIO register as an SMHC in section 8.5 GPIO; reset clock by writing 1 to SMHC_BGR_REG[SMHCx_RST](x=0, 1, or 2), and open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING] (x=0, 1, or 2); select clock sources and set the division factor by configuring the SMHCx_CLK_REG (x = 0, 1, or 2) register.

Step 2 Configure SMHC_CTRL to reset the FIFO and controller, and enable the global interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupts and error abnormal interrupts, and then register the interrupt function.

Step 3 Configure SMHC_CLKDIV to open clock for devices; configure SMHC_CMD as the change clock command (for example 0x80202000); send the update clock command to deliver clocks to devices.

Step 4 Configure SMHC_CMD as a normal command. Configure SMHC_CMDARG to set command parameters. Configure SMHC_CMD to set parameters like whether to send the response, the response type, and the response length and then send the commands. According to the initialization process in the protocol, you can finish SMHC initialization by sending the corresponding command one by one.

3.3.4.2 Writing a Single Data Block

To write a single data block, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

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Step 3 To write one block data to sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD24 (Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, and send CMD24 command to write data to the device.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD24 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

3.3.4.3 Reading a Single Data Block

To read a single data block, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read one block data from sector1, configure SMHC_BYTCNT[BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD17 command (Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD, and send CMD17 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

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Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer and CMD17 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

3.3.4.4 Writing Open-Ended Multiple Data Blocks (CMD25 + Auto CMD12)

To write open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data to sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, and send CMD25 command to read data from the device to DRAM/SRAM.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, the data transfer, CMD12 transfer, and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 7 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise,

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the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

3.3.4.5 Reading Open-Ended Multiple Data Blocks (CMD18 + Auto CMD12)

To read open-ended multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data from sectors begin with sector0, configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 command (Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD, and send CMD18 command to read data to the device. When the data transfer is completed, CMD12 will be sent automatically.

Step 4 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

Step 5 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are both 1. If yes, data transfer, CMD12 transfer, and CMD18 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

3.3.4.6 Writing Pre-Defined Multiple Data Blocks (CMD23 + CMD25)

To write pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

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Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To write three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, and send CMD25 command to write data to the device.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

Step 8 Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step5 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout

3.3.4.7 Reading Pre-Defined Multiple Data Blocks (CMD23 + CMD18)

To read pre-defined multiple data blocks, follow the steps below:

Step 1 Write 0x1 to SMHC_CTRL[DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_IDMAC to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

Step 2 Configure SMHC_FIFOTH to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, it indicates the burst size is 16,

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TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA to determine the start address of the DMA descriptor.

Step 3 To read three blocks of data, configure SMHC_CMDARG to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD to send the CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 4 Configure SMHC_BYTCNT[BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 (Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, and send CMD18 command to read data from device to DRAM/SRAM.

Step 5 Check whether SMHC_RINTSTS[CC] is 1. If yes, the command is sent successful; otherwise, continue to wait until timeout, and then exit the process.

Step 6 Check whether SMHC_IDST[RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

Step 7 Check whether SMHC_RINTSTS[DTC] is 1. If yes, the data transfer and CMD18 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS and SMHC_STATUS to query the existing abnormity.

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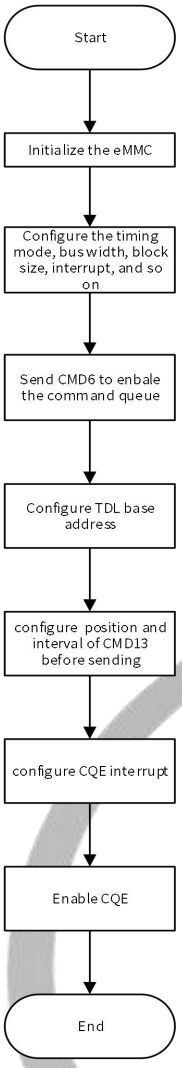
3.3.4.8 Initializing Command Queue for eMMC V5.1 Device

The following figure describes the initialization process of command queue.

Figure 3-10 Initialization Process of Command Queue



Follow the steps below to initialize the command queue:

Step 1 Initialize the eMMC. For detailed initialization steps, refer to section 3.3.4.1 Initializing SMHC.

Step 2 Send CMD6 to configure the timing mode and bus width. Send CMD16 to configure the block size as 512 B.

NOTE

The block size must be set to 512 B. After the command queue is enabled, the block size will not be able to be modified.

Step 3 Send CMD6 to enable the command queue of the eMMC device.

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Step 4 Configure CQTDLBA register to set the base address of the task descriptor list.

NOTE

When the base address of the task descriptor list crosses 4 GB, you need to write the bit [32] of the higher 32-bit address to the bit [0] of the CQTDLBA register and write the lower 32-bit address to the CQTDLBA register.

For example, assume that the base address is 0x106000000. In this case, you need to write the bit [32] of the higher 32-bit address to the bit [0] of the CQTDLBA register and write 0x06000001 to the CQTDLBA register.

Step 5 Configure CQSSC1 register to set how to query the status of the device's task queue.

Step 6 Configure CQIC register to enable/disable interrupt, set interrupt count and timer protection.

Step 7 Configure CQRMEM register to set which errors may trigger a RED interrupt.

Step 8 Configure CQCFG register to enable CQE activity.

eMMC CMDQ supports multiple operation modes, which could be selected by configuring the CMDQ_MODE bit (bit [5:4]) of CQCFG register.

3.3.5 Register List

Module Name	Base Address	Description
SMHC0	0x04020000	
SMHC1	0x04021000	SMHC1 register is the same with SMHC0
SMHC2	0x04022000	SMHC2 register is the same with SMHC0

Register Name	Offset	Description
SMHC_CTRL	0x0000	SMHC Global Control Register
SMHC_CLKDIV	0x0004	SMHC Clock Control Register
SMHC_TMOUT	0x0008	SMHC Timeout Register
SMHC_CTYPE	0x000C	SMHC Bus Width Register
SMHC_BLKSIZ	0x0010	SMHC Block Size Register
SMHC_BYTCNT	0x0014	SMHC Byte Count Register
SMHC_CMD	0x0018	SMHC Command Register
SMHC_CMDARG	0x001C	SMHC Command Argument Register
SMHC_RESP0	0x0020	SMHC Response 0 Register
SMHC_RESP1	0x0024	SMHC Response 1 Register
SMHC_RESP2	0x0028	SMHC Response 2 Register
SMHC_RESP3	0x002C	SMHC Response 3 Register
SMHC_INTMASK	0x0030	SMHC Interrupt Mask Register

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Register Name	Offset	Description
SMHC_MINTSTS	0x0034	SMHC Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	SMHC Raw Interrupt Status Register
SMHC_STATUS	0x003C	SMHC Status Register
SMHC_FIFOTH	0x0040	SMHC FIFO Water Level Register
SMHC_FUNS	0x0044	SMHC FIFO Function Select Register
SMHC_TBC0	0x0048	SMHC Transferred Byte Count Register 0
SMHC_TBC1	0x004C	SMHC Transferred Byte Count Register 1
SMHC_CSDC	0x0054	SMHC CRC Status Detect Control Register
SMHC_A12A	0x0058	SMHC Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SMHC New Timing Set Register
SMHC_HWRST	0x0078	SMHC Hardware Reset Register
SMHC_IDMAC	0x0080	SMHC IDMAC Control Register
SMHC_DLBA	0x0084	SMHC Descriptor List Base Address Register
SMHC_IDST	0x0088	SMHC IDMAC Status Register
SMHC_IDIE	0x008C	SMHC IDMAC Interrupt Enable Register
SMHC_THLD	0x0100	SMHC Card Threshold Control Register
SMHC_SFC	0x0104	SMHC Sample FIFO Control Register
SMHC_A23A	0x0108	SMHC Auto Command 23 Argument Register
EMMC_DDR_SBIT_DET	0x010C	SMHC eMMC4.5 DDR Start Bit Detection Control Register
SMHC_EXT_CMD	0x0138	SMHC Extended Command Register
SMHC_EXT_RESP	0x013C	SMHC Extended Response Register
SMHC_DRV_DL	0x0140	SMHC Drive Delay Control Register
SMHC_SAMP_DL	0x0144	SMHC Sample Delay Control Register
SMHC_DS_DL	0x0148	SMHC Data Strobe Delay Control Register
SMHC_HS400_DL	0x014C	SMHC HS400 New Timing Delay Control Register
SMHC_CIU_CNT	0x0154	SMHC Card interface counter
SMHC_FIFO	0x0200	SMHC FIFO Register
CQCFG	0x0408	Command Queuing Configuration
CQCTL	0x040C	Command Queuing Control
CQIS	0x0410	Command Queuing Interrupt Status
CQISTE	0x0414	Command Queuing Interrupt Status Enable
CQISGE	0x0418	Command Queuing Interrupt Signal Enable
CQIC	0x041C	Command Queuing Interrupt Coalescing
CQTDLBA	0x0420	Command Queuing Task Descriptor List Base Address
CQTDBR	0x0428	Command Queuing Task Doorbell
CQTCN	0x042C	Command Queuing Task Completion Notification
CQDQS	0x0430	Command Queuing Device Queue Status
CQDPT	0x0434	Command Queuing Device Pending Tasks
CQTCLR	0x0438	Command Queuing Task Clear
CQSSC1	0x0440	Command Queuing Send Status Configuration 1

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Register Name	Offset	Description
CQSSC2	0x0444	Command Queuing Send Status Configuration 2
CQCRDCT	0x0448	Command Queuing Command Response for Direct-Command Task
CQRMEM	0x0450	Command Queuing Response Mode Error Mask
CQTERRI	0x0454	Command Queuing Task Error Information
CQCRI	0x0458	Command Queuing Command Response Index
CQCRA	0x045C	Command Queuing Command Response Argument

3.3.6 Register Description

3.3.6.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:18	/	/	/
17:16	R/W	0x0	SRAM_BIST_SEL SRAM BIST Select 2'b00: for SMHC 4K SRAM(1024x32) BIST 2'b01: for CQE SRAM(32x56) BIST 2'b10: for EMCE SRAM BIST 2'b11: Reserved
15:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although the HS400 speed mode of eMMC is 8-bit DDR, this field should be cleared when

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Offset: 0x0000			Register Name: SMHC_CTRL
Bit	Read/Write	Default/Hex	Description
			HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data [3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

3.3.6.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MASK_DAT0 Mask Data0 0: Do not mask data0 when update clock 1: Mask data0 when update clock

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Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	Read/Write	Default/Hex	Description
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1 : Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0-255) when HS400_MD_EN is set, this field must be cleared.

3.3.6.3 0x0008 SMHC Timeout Register (Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device, this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect. Note: Under the following 3 conditions, the timeout limit is half of the set time. 1> DDR8 mode 2> DDR4 and SMHC_NTSR[MODE_SELEC] (0x5C [31])

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Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	Read/Write	Default/Hex	Description
			high 3> HS400 and SMHC_NTSR[HS400_NEW_SAMPLE_EN](0x5C[0]) high
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

3.3.6.4 0x000C SMHC Bus Width Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

3.3.6.5 0x0010 SMHC Block Size Register (Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

3.3.6.6 0x0014 SMHC Byte Count Register (Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

3.3.6.7 0x0018 SMHC Command Register (Default Value:0x0000_0000)

Offset: 0x0018	Register Name: SMHC_CMD

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit will be set in SMHC_RINTSTS register. You should not write any other command before this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:18	/	/	/
17	R/W	0x0	R1B_BUSY_HW_DETECT R1b busy hardware detect enable 0: Disable hardware detect r1b busy 1: Enable hardware detect r1b busy
16	R/W	0x0	R1B_RESP R1b response 0: The response type isn't r1b for current command 1: The response type is r1b for current command

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Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
			Note: if STOP_CMD_FLAG set, R1B_RESP will be set by controller when send CMD12, and will be clear by controller when send next command.
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: normal command sending 1: send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC

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Offset: 0x0018			Register Name: SMHC_CMD
Bit	Read/Write	Default/Hex	Description
			Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

3.3.6.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CMD_ARG Command argument

3.3.6.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

3.3.6.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:32] of response

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3.3.6.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

3.3.6.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

3.3.6.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:18	/	/	/
17	R/W	0x0	R1B_BUSY_CLR_INT_EN
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN

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Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	Read/Write	Default/Hex	Description
			Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

3.3.6.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	M_CARD_REMOVAL_INT Card Removed
30	R	0x0	M_CARD_INSERT Card Inserted
29:18	/	/	/
17	R	0x0	R1B_BUSY_CLR_INT
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token.
14	R	0x0	M_ACD_INT Auto Command Done

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Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
			When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative.
6	R	0x0	M_RCE_INT Response CRC Error
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD

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Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	Read/Write	Default/Hex	Description
			Index error may occurs.
0	/	/	/

3.3.6.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:18	/	/	/
17	R/W1C	0x0	R1B_BUSY_CLR R1b busy clear When set, it means that the r1b busy has finished or not set.
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. It is valid at 4-bit or 8-bit bus mode, when it set, host found start bit at data0, but not find start bit at some or all of the other data lines. When set during transmitting data, it means that

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Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
			busy signal is cleared after the last block. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0(1-bit bus) or data0-data3(4-bit bus) or data0-data7(8-bit bus). This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC

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Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	Read/Write	Default/Hex	Description
			Data Transfer Complete This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

3.3.6.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:28	/	/	/
27:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA [0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data [3] status level of DATA [3]; checks whether card is present 0: card not present

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Offset: 0x003C			Register Name: SMHC_STATUS
Bit	Read/Write	Default/Hex	Description
			1: card present
7:4	R	0x0	FSM_STA Command FSM states: 0000: Idle 0001: Send INIT sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn’t reach receive trigger level 1: FIFO reached receive trigger level

3.3.6.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
31	/	/	/

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Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD(4Byte). A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: BSIZE_OF_TRANS = 3, MSize = 16, TX_TL = 240, RX_TL = 15 FIFO_DEPTH = 256 FIFO_SIZE = 256 * 32 = 1K
27	/	/	/
26:16	R/W	0xF	RX_TL RX Trigger Level When BLOCK2K_EXIST is 1'b1: 0x0-0x3FE: RX Trigger Level is 0-1022(Unit is equal to the FIFO_WIDTH) 0x3FF reserved When BLOCK2K_EXIST is 1'b0: 0x0-0xFE: RX Trigger Level is 0-254 (Unit is equal to the FIFO_WIDTH) 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. When CARD_WR_THLD_ENB is set, RX_TL*4 should be less than CARD_WR_THLD. 15 (means greater than 15)
15:11	/	/	/
10:0	R/W	0x0	TX_TL TX Trigger Level

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Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	Read/Write	Default/Hex	Description
			When BLOCK2K_EXIST is 1'b1: 0x1-0x3FF: TX Trigger Level is 1-1023 (Unit is equal to the FIFO_WIDTH) 0x0: no trigger When BLOCK2K_EXIST is 1'b0: 0x1-0xFF: TX Trigger Level is 1-255 (Unit is equal to the FIFO_WIDTH) 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)

3.3.6.18 0x0044 SMHC FIFO Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response

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Offset: 0x0044			Register Name: SMHC_FUNS
Bit	Read/Write	Default/Hex	Description
			When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

3.3.6.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

3.3.6.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

3.3.6.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA CRC Detect Para 110: HS400 speed mode 011: Other speed mode

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Offset: 0x0054			Register Name: SMHC_CSDC
Bit	Read/Write	Default/Hex	Description
			Others: Reserved

3.3.6.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFF	A12A Auto CMD12 Argument The argument of command 12 automatically send by controller with this field.

3.3.6.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	MODE_SEL Mode Select 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:26	/	/	/
25	R/W	0x0	BOOT_DAT_RX_PHASE_CLR After boot ACK, before receive boot data, clear data lines' input phase. 0: Disable 1: Enable
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear the input phase of command lines and data lines during the update clock operation. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines' input phase. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines' input phase. 0: Disable

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Offset: 0x005C			Register Name: SMHC_NTSR
Bit	Read/Write	Default/Hex	Description
			1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines' input phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command RX phase before sending the command. 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAM_TIM_PHS Data Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0（only for SD2 hs400 mode） Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAM_TIM_PHS Command Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAM_EN HS400 New Sample Enable 1：enable hs400 new sample method 0：disable hs400 new sample method

3.3.6.24 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

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Offset: 0x0078			Register Name: SMHC_HWRST
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	HW_RST Hardware Reset 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

3.3.6.25 0x0080 SMHC IDMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	Read/Write	Default/Hex	Description
31	W	0x0	DES_LOAD_CTRL When IDMAC fetches a descriptor, if the valid bit of a descriptor is not set, IDMAC FSM will go to the suspend state. Setting this bit will make IDMAC re-fetch descriptor again and do the transfer normally.
30:8	/	/	/
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	/	/	/
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

3.3.6.26 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DES_BASE_ADDR

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Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
			Start of Descriptor List. Contains the base address of the First Descriptor, is a word(4byte) address

3.3.6.27 0x0088 SMHC IDMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:10	R	0x0	IDMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (SMHC_ IDST [2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved This bit is read-only.
9	R/W1C	0x0	AIS Abnormal Interrupt Summary. Logical OR of the following: SMHC_IDST [2]: Fatal Bus Interrupt SMHC_IDST [4]: Descriptor unavailable bit Interrupt SMHC_IDST [5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NIS Normal Interrupt Summary. Logical OR of the following: SMHC_IDST [0]: Transmit Interrupt SMHC_IDST [1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the

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Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
			card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (SMHC_IDST [12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.

3.3.6.28 0x008C SMHC IDMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB

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Offset: 0x008C			Register Name: SMHC_IDIE
Bit	Read/Write	Default/Hex	Description
			Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set, Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set, Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

3.3.6.29 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	CARD_WR_THLD Card Read/write Threshold Size (Unit: byte)
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disable 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO. **Note: Not support DDR 8-wire mode.**
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled

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Offset: 0x0100			Register Name: SMHC_THLD
Bit	Read/Write	Default/Hex	Description
			The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

3.3.6.30 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be change between 0x0 and 0xF, but actually the available value and the position of stopping clock must be decided by the actual situation. The value increase one in this field is linked to one cycle(two cycle in DDR mode) that the position of stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

3.3.6.31 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	A23A Auto CMD23 Argument

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Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
			The argument of command 23 is automatically sent by controller with this field.

3.3.6.32 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside host controller based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

3.3.6.33 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When set this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST set, this field will be cleared.

3.3.6.34 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	Read/Write	Default/Hex	Description

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Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

3.3.6.35 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C [31] is low, 45^0 at DDR4 mode when 0x5C [31] is high, 90^0 at HS400 mode when 0x5C [0] is low, 45^0 at HS400 mode when 0x5C [0] is high. 1: Data drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C [31] is low, 90^0 at DDR4 mode when 0x5C [31] is high, 180^0 at HS400 mode when 0x5C [0] is low, 90^0 at HS400 mode when 0x5C[0] is high.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C [31] is low, 45^0 at DDR4 mode when 0x5C [31] is high, 90^0 at HS400 mode 1: Command drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C [31] is low, 90^0 at DDR4 mode when 0x5C [31] is high, 180^0 at HS400 mode.
15:0	/	/	/

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3.3.6.36 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

3.3.6.37 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

3.3.6.38 0x014C SMHC HS400 New Timing Delay Control Register (Default Value: 0x0000_0800)

Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	HS400_DL_CAL_START HS400 Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	HS400_DL_CAL_DONE HS400 Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in HS400_DL.
13:12	/	/	/
11:8	R	0x8	HS400_DL HS400 Delay It indicates the number of delay cells corresponding to current card clock. The delay

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Offset: 0x014C			Register Name: SMHC_HS400_DL
Bit	Read/Write	Default/Hex	Description
			time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when HS400_DL_CAL_DONE is set.
7	R/W	0x0	HS400_DL_SW_EN Sample Delay Software Enable
6:4	/	/	/
3:0	R/W	0x0	HS400_DL_SW HS400 Delay Software

3.3.6.39 0x0154 SMHC Card interface counter Register (Default Value:0x0)

Offset: 0x0154			Register Name: SMHC_CIU_CNT
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	DATA_PATH_CNT Data Path Counter This field indicates the count value of counters for each stage when host read or write data. When Host read data, this field is one of the following values: 1. The time of wait data start bit 2. The byte count of receive data 3. The count of receive crc16 When Host write data, this field is one of the following values: 1. The byte count of transmit data 2. The count of transmit crc16 3. The time of wait receive CRC status
7:0	/	/	/

3.3.6.40 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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3.3.6.41 0x0408 CQCFG Command Queuing Configuration Register (Default Value: 0x0200_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x200	CQE_BLOCK_SIZE CQE Block Size Configuration It must be 0x200 when CMDQ_MODE is CMDQ or CMDQ_HALF or CMDQ_ALMOST.
15:13	/	/	/
12	R/W	0x0	CQE_DCMD_EN Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 1 = Task descriptor in slot #31 is a DCMD Task Descriptor 0 = Task descriptor in slot #31 is a Data Transfer Task Descriptor
11:9	/	/	/
8	R/W	0x0	CQE_TASK_DESC_SIZE Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits as detailed in Data Structures section. This bit can only be configured when Command Queuing Enable bit is '0' (command queuing is disabled) Bit Value Description 1 = Task descriptor size is 128 bits 0 = Task descriptor size is 64 bits
7:6	/	/	/
5:4	R/W	0x0	CMDQ_MODE Command Queue Mode select This field is used to select CMDQ mode, there are four kinds of CMDQ mode: • CMDQ_HALF mode CMD and data can't be transmitted at the same time, but the current task can be sent to the device before the previous task is completed.

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Offset: 0x0408			Register Name: CQCFG
Bit	Read/Write	Default/Hex	Description
			• CMDQ_ALMOST mode CMD can be sent at the start of block, and the current task can be sent to the device before the previous task is completed. The Field Value Description 2'b00: Reserved 2'b01: CMDQ_HALF mode 2'b10: CMDQ_ALMOST mode (Not support DDR 8-wire mode) 2'b11: Reserved **Note: The CARD_WR_THLD_ENB must be set and the value of CARD_WR_THLD must be greater than or equal CQE_BLOCK_SIZE when CQE_MODE is CMDQ_ALMOST.**
3:1	/	/	/
0	R/W	0x0	CQE_EN Command Queuing Enable Software shall write '1' this bit when in order to enable command queuing mode (i.e., enable CQE). When this bit is 0, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller. Before software writes '1' to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing. When software wants to exit command queuing mode, it shall clear all previous tasks if such exist before setting this bit to 0.

3.3.6.42 0x040C CQCTL Command Queuing Control Register (Default Value: 0x0000_0000)

This register controls CQE behavior affecting the general operation of command queuing module or operation of multiple tasks in the same time.

Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/WAC	0x0	CQE_TCL_ALL CQE Task Cleared All Software shall write '1' this bit when it wants to clear all the tasks sent to the device. This bit can only be

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Offset: 0x040C			Register Name: CQCTL
Bit	Read/Write	Default/Hex	Description
			written when CQE is in halt state (i.e., Halt bit is 1). When software writes 1, the value of the register is updated to '1', and CQE shall reset CQTDBR register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is software's responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing '0' to this register shall have no effect.
7:1	/	/	/
0	R/W	0x0	CQE_HALT Host software shall write '1' to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT) When software writes '1', CQE shall complete the ongoing task if such a task is in progress. Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1. Software may poll on this bit until it is set to 1, and may only then send commands on the eMMC bus. In order to exit halt state (i.e., resume CQE activity), software shall clear this bit (write '0'). Writing '0' when the value is already '0' shall have no effect.

3.3.6.43 0x0410 CQIS Command Queuing Interrupt Status Register (Default Value: 0x0000_0000)

This register indicates pending interrupts that require service. Each bit in this registers is asserted in response a specific event, only if the respective bit is set in CQISTE register.

Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	CQIS_TCL Task Cleared

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Offset: 0x0410			Register Name: CQIS
Bit	Read/Write	Default/Hex	Description
			This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL).
2	R/W1C	0x0	CQIS_RED Response Error Detected Interrupt This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked.
1	R/W1C	0x0	CQIS_TCC Task Complete Interrupt This status bit is asserted (if CQISTE.TCC=1) when at least one of the following two conditions are met: A task is completed and the INT bit is set in its Task Descriptor Interrupt caused by Interrupt Coalescing logic (see 0)
0	R/W1C	0x0	CQIS_HAC Halt Complete Interrupt This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that host controller has completed its current ongoing task and has entered halt state.

3.3.6.44 0x0414 CQISTE Command Queuing Interrupt Status Enable Register (Default Value: 0x0000_0000)

This register enables and disables the reporting of the corresponding interrupt to host software in CQIS register. When a bit is set (‘1’) and the corresponding interrupt condition is active, then the bit is CQIS is asserted. Interrupt sources that are disabled (‘0’) are not indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CQISTE_TCL Task Cleared Status Enable 1: CQIS.TCL will be set when its interrupt condition is active

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Offset: 0x0414			Register Name: CQISTE
Bit	Read/Write	Default/Hex	Description
			0: CQIS.TCL is disabled
2	R/W	0x0	CQISTE_RED Response Error Detected Status Enable 1: CQIS.RED will be set when its interrupt condition is active 0: CQIS.RED is disabled
1	R/W	0x0	CQISTE_TCC Task Complete Status Enable 1: CQIS.TCC will be set when its interrupt condition is active 0: CQIS.TCC is disabled
0	R/W	0x0	CQISTE_HAC Halt Complete Status Enable 1: CQIS.HAC will be set when its interrupt condition is active 0: CQIS.HAC is disabled

3.3.6.45 0x0418 CQISGE Command Queuing Interrupt Signal Enable Register (Default Value: 0x0000_0000)

This register enables and disables the generation of interrupts to host software. When a bit is set ('1') and the corresponding bit in CQIS is set, then an interrupt is generated. Interrupt sources that are disabled ('0') are still indicated in the CQIS register. This register is bit-index matched to CQIS register.

Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CQISGE_TCL Task Cleared Signal Enable When set and CQIS.TCL is asserted, the CQE shall generate an interrupt
2	R/W	0x0	CQISGE_RED Response Error Detected Signal Enable When set and CQIS.RED is asserted, the CQE shall generate an interrupt
1	R/W	0x0	CQISGE_TCC Task Complete Signal Enable When set and CQIS.TCC is asserted, the CQE shall generate an interrupt
0	R/W	0x0	CQISGE_HAC

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Offset: 0x0418			Register Name: CQISGE
Bit	Read/Write	Default/Hex	Description
			Halt Complete Signal Enable When set and CQIS.HAC is asserted, the CQE shall generate an interrupt

3.3.6.46 0x041C CQIC Interrupt Coalescing Register (Default Value: 0x0000_0000)

This register controls the interrupt coalescing feature.

Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CQIC_EN Interrupt Coalescing Enable/Disable When set to '0' by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT=1 in the Task Descriptor. When set to '1', the interrupt coalescing mechanism is enabled and coalesced interrupts are generated
30:21	/	/	/
20	R	0x0	CQIC_SB Interrupt Coalescing Status Bit This bit indicates to software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (i.e., ICSB is set if and only if IC counter > 0). Bit Value Description 1: At least one task completion has been counted (IC counter >0) 0: No task completions have occurred since last counter reset (IC counter =0)
19:17	/	/	/
16	W	0x0	CQIC_CTR Counter and Timer Reset When host driver writes '1', the interrupt coalescing timer and counter are reset
15	W	0x0	CQIC_CTH_WEN Interrupt Coalescing Counter Threshold Write Enable When software writes '1', the value ICCTH is updated with the contents written at the same cycle. When software writes '0', the value in ICCTH is not updated. Note: Write operations to ICCTH are only allowed when

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Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
			the task queue is empty.
14:13	/	/	/
12:8	R/W	0x0	CQIC_CTH Interrupt Coalescing Counter Threshold Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31 Note: • When ICCTH is 0, task completions are not counted, and counting-based interrupts are not generated. • In order to write to this field, the ICCTHWEN bit must be set at the same write operation.
7	W	0x0	CQIC_TOVAL_WEN Interrupt Coalescing Timeout Value Write Enable When software writes '1', the value ICTOVAL is updated with the contents written at the same cycle. When software writes '0', the value in ICTOVAL is not updated. Note: Write operations to ICTOVAL are only allowed when the task queue is empty.
6:0	R/W	0x0	CQIC_TOVAL Interrupt Coalescing Timeout Value Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register.

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Offset: 0x041C			Register Name: CQIC
Bit	Read/Write	Default/Hex	Description
			The minimum value is 01h (1024 clock periods) and the maximum value is 7Fh (127*1024 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16*1024*52.08 ns= 853.33 us Note: When ICTOVAL is 0, the timer is not running, and timer-based interrupts are not generated. In order to write to this field, the ICTOVALWEN bit must be set at the same write operation.

3.3.6.47 0x0420 CQTDLBA Command Queuing Task Descriptor List Base Address Register (Default Value: 0x0000_0000)

This register is used for configuring the lower 32 bits of the byte address of the head of the Task Descriptor List in the host memory.

Offset: 0x0420			Register Name: CQTDLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CQE_TDLBA Task Descriptor List Base Address This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KByte boundary.

3.3.6.48 0x0428 CQTDBR Command Queuing Task Doorbell Register (Default Value: 0x0000_0000)

Using this register, software triggers CQE to process a new task.

Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W1S	0x0	CQE_TDBR Command Queuing Task Doorbell Software shall configure TDLBA and TDLBAU, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot

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Offset: 0x0428			Register Name: CQTDBR
Bit	Read/Write	Default/Hex	Description
			n of the TDL. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to '0' by CQE in one of the following events: When a task execution is completed (with success or error) The task is cleared using CQTCLR register All tasks are cleared using CQCTL register CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission: CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order. Writing 0 by software shall have no impact on the hardware, and will not change the value of the register bit.

3.3.6.49 0x042C CQTCN Task Completion Notification Register (Default Value: 0x0000_0000)

This register is used by CQE to notify software about completed tasks.

Offset: 0x042C			Register Name: CQTCN
Bit	Read/Write	Default/Hex	Description
31:0	R/W1C	0x0	CQE_TCN Task Complete Notification CQE shall set bit *n* of this register (at the same time it clears bit *n* of CQTDBR) when a task execution is completed (with success or error).

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Offset: 0x042C			Register Name: CQTCN
Bit	Read/Write	Default/Hex	Description
			When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

3.3.6.50 0x0430 CQDQS Device Queue Status Register (Default Value: 0x0000_0000)

This register stores the most recent value of the device's queue status.

Offset: 0x0430			Register Name: CQDQS
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CQE_DQS Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command, i.e., the device's queue status.

3.3.6.51 0x0434 CQDPT Device Pending Tasks Register (Default Value: 0x0000_0000)

This register indicates to software which tasks are queued in the device, awaiting execution.

Offset: 0x0434			Register Name: CQDPT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DPT Device Pending Tasks Bit *n* of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasn't been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using CQCTL register.

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3.3.6.52 0x0438 CQTCLR Task Clear Register (Default Value: 0x0000_0000)

This register is used for removing an outstanding task in the CQE. The register should be used only when CQE is in Halt state.

Offset: 0x0438			Register Name: CQTCLR
Bit	Read/Write	Default/He	Description
31:0	R/W	0x0	CQE_TASK_CLR Command Queuing Task Clear Writing 1 to bit *n* of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCTL register Halt bit. When software writes '1' to a bit in this register, CQE updates the value to '1', and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once clear operation is complete. Software should poll on the CQTCLR until it is cleared to verify clear operation was complete. Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK _MGMT while CQE is still in Halt state. Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using CQCTL register. Writing 0 to a register bit shall have no impact.

3.3.6.53 0x0440 CQSSC1 Send Status Configuration 1 Register (Default Value: 0x0001_1000)

The register controls the when SEND_QUEUE_STATUS commands are sent.

Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Write	Default/He	Description
31:20	/	/	/
19:16	R/W	0x1	CQE_SSC_CBC Send Status Command Block Counter This field indicates to CQE when to send SEND_QUEUE_STATUS (CMD13) command to inquire the status of the device's task queue. A value of *n* means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-*n*, on the data lines, where BLOCK_CNT is

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Offset: 0x0440			Register Name: CQSSC1
Bit	Read/Write	Default/He	Description
			the number of blocks in the current transaction. A value of 0 means that SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. A value of 1 means that STATUS command is to be sent during the last block of the transaction.
15:0	R/W	0x1000	CQE_SSC_CIT Send Status Command Idle Timer This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0001h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 1000h, the calculated polling period is 4096*52.08 ns= 213.33 us

3.3.6.54 0x0444 CQSSC2 Send Status Configuration 2 Register (Default Value: 0x0000_0000)

This register is used for configuring RCA field in SEND_QUEUE_STATUS command argument.

Offset: 0x0444			Register Name: CQSSC2
Bit	Read/Write	Default/He	Description
31:16	/	/	/
15:0	R/W	0x0	CQE_SSC_RCA Send Queue Status RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_ STATUS (CMD13) command argument. CQE shall copy this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

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3.3.6.55 0x0448 CQCRDCT Command Response for Direct-Command Task Register (Default Value: 0x0000_0000)

This register is used for passing the response of a DCMD task to software.

Offset: 0x0448			Register Name: CQCRDCT
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_DCMD_LAST_RESP Direct Command Last Response This register contains the response of the command generated by the last direct- command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of CQTDBR register is cleared by CQE.

3.3.6.56 0x0450 CQRMEM Response Mode Error Mask Register (Default Value: 0xFDF9_A080)

This register controls the generation of Response Error Detection (RED) interrupt.

Offset: 0x0450			Register Name: CQRMEM
Bit	Read/Write	Default/He	Description
31:0	R/W	0xFDF9A080	CQE_RMEM Response Mode Error Mask This bit is used as in interrupt mask on the device status filed which is received in R1/R1b responses. Bit Value Description (for any bit 'i'): 1: When a R1/R1b response is received, with bit 'I' in the device status set, a RED interrupt is generated 0: When a R1/R1b response is received, bit *i* in the device status is ignored The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. Note: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.

3.3.6.57 0x0454 CQTERRI Task Error Information Register (Default Value: 0x0000_0000)

This register is updated by CQE when an error occurs on data or command related to a task activity.

When such error is detected by CQE or indicated by the eMMC controller CQE stores in CQTERRI the task IDs and the command indices of the commands which were executed on the command line and data lines when the error occurred.

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Software is expected to use this information in the error recovery procedure.

Offset: 0x0454			Register Name: CQERRI
Bit	Read/Write	Default/He	Description
31	R	0x0	CQE_DTE_VLD Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0.
30:29	/	/	/
28:24	R	0x0	CQE_DTE_TASK_ID Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23:22	/	/	/
21:16	R	0x0	CQE_DTE_CMD_IDX Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	R	0x0	CQE_RME_VLD Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0.
14:13	/	/	/
12:8	R	0x0	CQE_RME_TASK_ID Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred.

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Offset: 0x0454			Register Name: CQERRI
Bit	Read/Write	Default/He	Description
			The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7:6	/	/	/
5:0	R	0x0	CQE_RME_CMD_IDX Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

3.3.6.58 0x0458 CQCRI Command Response Index Register (Default Value: 0x0000_0000)

This register stores the index of the last received command response.

Offset: 0x0458			Register Name: CQCRI
Bit	Read/Write	Default/He	Description
31:6	/	/	/
5:0	R	0x0	CQE_LAST_RESP_IDX Last Command Response index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

3.3.6.59 0x045C CQCRA Command Response Argument Register (Default Value: 0x0000_0000)

This register stores the argument of the last received command response.

Offset: 0x045C			Register Name: CQCRA
Bit	Read/Write	Default/He	Description
31:0	R	0x0	CQE_LAST_RESP_ARG Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

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4 Audio

4.1 Audio Codec

4.1.1 Overview

The Audio Codec is high-performance audio encoder and decoder module which supports DAC/ADC, dynamic range controller (DRC) and dynamic voltage controller (DVC) functions.

The Audio Codec has the following features:

- Two audio digital-to-analog converter (DAC) channels
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 100 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- Three audio outputs
  - One stereo headphone output: HPOUTL/R
  - Two differential lineout outputs: LINEOUTLP/N and LINEOUTRP/N
- Three audio analog-to-digital converter (ADC) channels
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95 ± 3dB SNR@A-weight, -80 ± 3dB THD+N
- Three differential microphone inputs: MICIN1P/1N, MICIN2P/2N, and MICIN3P/3N (for echo reduction)
- Two low-noise analog microphone bias outputs: MBIAS and HBIAS
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA
- Internal ALDO output for AVCC

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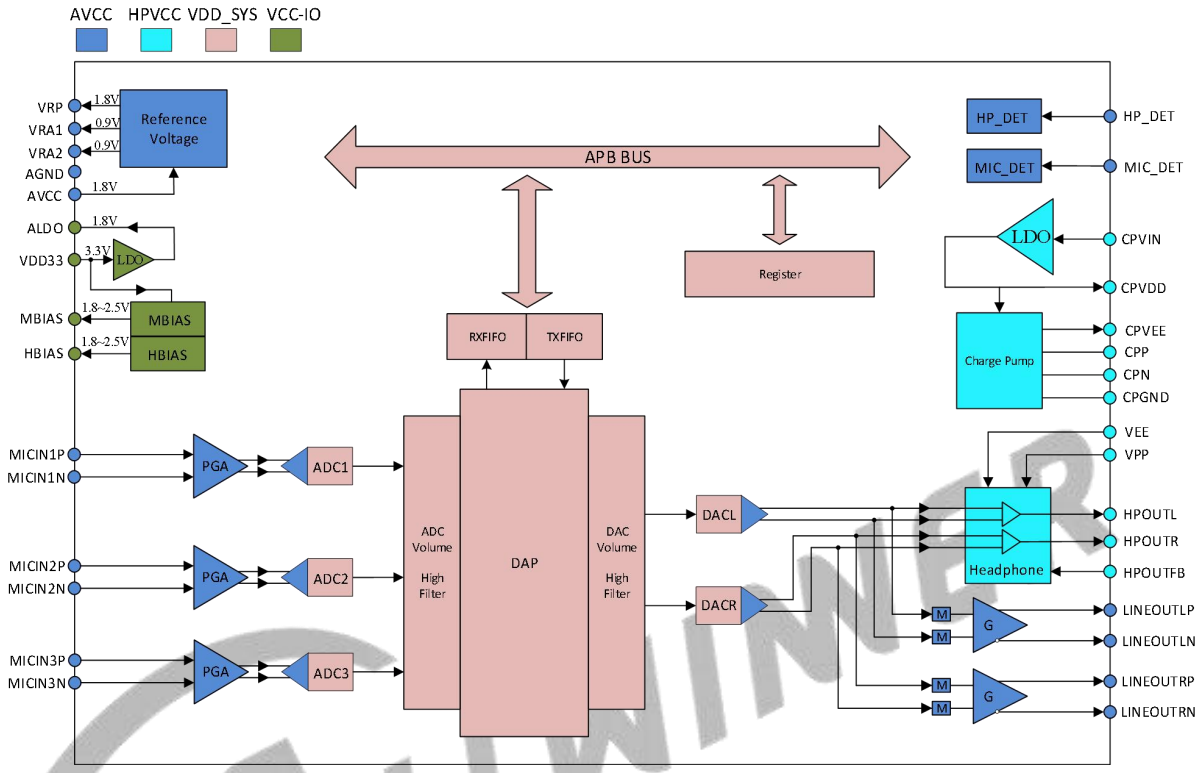
4.1.2 Block Diagram

The following figure shows the block diagram of Audio Codec.

Figure 4-1 Audio Codec Block Diagram



4.1.3 Functional Description

4.1.3.1 External Signals

Table 4-1 Audio Codec External Signals

Signal Name	Description	Type
MICIN1N	Microphone Differential Negative Input 1	AI
MICIN1P	Microphone Differential Positive Input 1	AI
MICIN2N	Microphone Differential Negative Input 2	AI
MICIN2P	Microphone Differential Positive Input 2	AI
MICIN3N	Microphone Differential Negative Input 3	AI
MICIN3P	Microphone Differential Positive Input 3	AI
LINEOUTLN	Lineout Left Channel Negative Differential Output	AO
LINEOUTLP	Lineout Left Channel Positive Differential Output	AO
LINEOUTRN	Lineout Right Channel Negative Differential Output	AO
LINEOUTRP	Lineout Right Channel Positive Differential Output	AO
HPOUTL	Headphone Light Output	AO
HPOUTR	Headphone Right Output	AO
HPOUTFB	Pseudo Differential Headphone Ground Reference	AI

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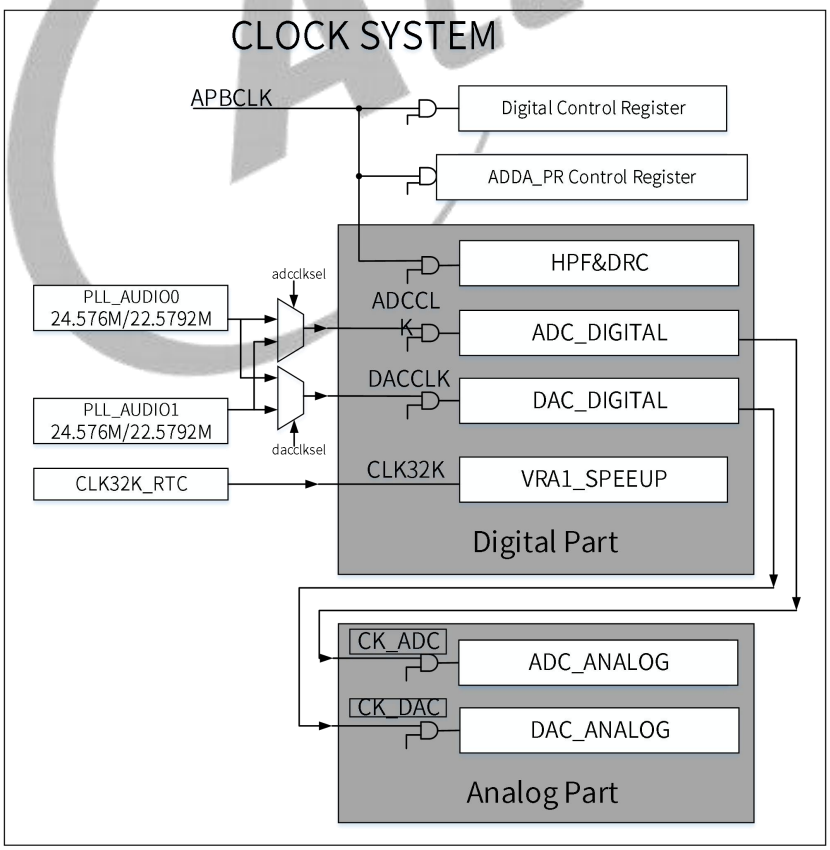
Signal Name	Description	Type
MIC-DET	Headphone MIC detect	AI
HP-DET	Headphone Jack detect	AI
MBIAS	First bias voltage output for main microphone	AO
HBIAS	Second bias voltage output for headset microphone	AO
CPVDD	Analog power for headphone charge pump	P
CPVEE	Charge pump negative voltage output	P
CPVIN	Analog power for LDO	P
AVCC	Power Supply for Analog Part	P
ALDO-OUT	Power Supply for AVCC	P
VDD33	Power Supply for 3.3V Analog Part	P
VEE	Negative Voltage to Headphone	P
VRA1	Internal Reference Voltage	AO
VRA2	Internal Reference Voltage	AO
VRP	Internal Reference Voltage	AO
AGND	Analog Ground	G

4.1.3.2 Clock Sources

The following figure describes the clock source of Audio Codec. For clock setting, configuration, and gating information, refer to section 2.11 Power Reset Clock Management (PRCM).

Figure 4-2 Audio Codec Clock Diagram



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- Digital Part

The clock sources for the digital ADC and DAC are the PLL_AUDIO0 and PLL_AUDIO1. Configure the CLK_SRC_SEL bit (bit [26:24]) of AUDIO_CODEC_ADC_CLK_REG register to select clock sources for ADC. Configure CLK_SRC_SEL bit (bit [26:24]) of AUDIO_CODEC_DAC_CLK_REG register to select clock sources for DAC. The PK-PK jitter of PLL_AUDIO0 and PLL_AUDIO1 should be less than 200 ps.

The clock source for VRA1_SPEEDUP is CLK32K from RTC.

- Analog Part

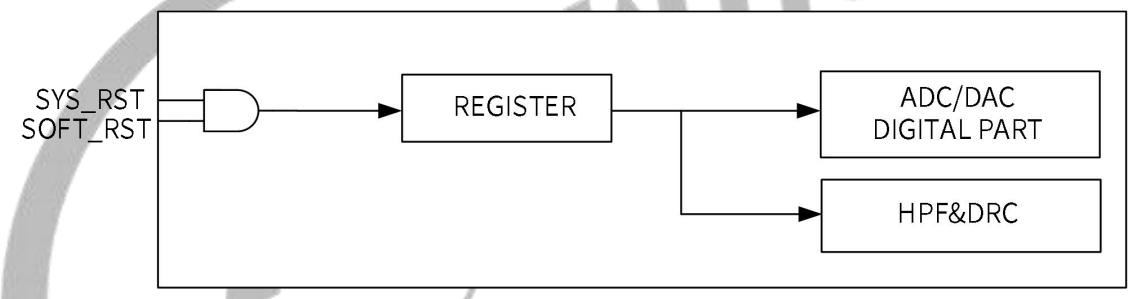
The clock source for the analog part is the CK_ADC and CK_DAC, both of which are divided from the digital part.

4.1.3.3 Reset System

Digital Part Reset System

The following figure shows the reset system of the audio codec digital part.

Figure 4-3 Audio Codec Digital Part Reset System



The MCU_SYS_RST comes from the VDD-SYS domain and is produced by the RTC domain which is controlled by MCU_PRCM. Each domain has the de-bounce to confirm the reset system is strong. For the codec register part, MIX can be reset by the MCU_SYS_RST when being powered on or the system soft is writing the reset control logic. The other parts can be reset by the soft configuration through writing the register.

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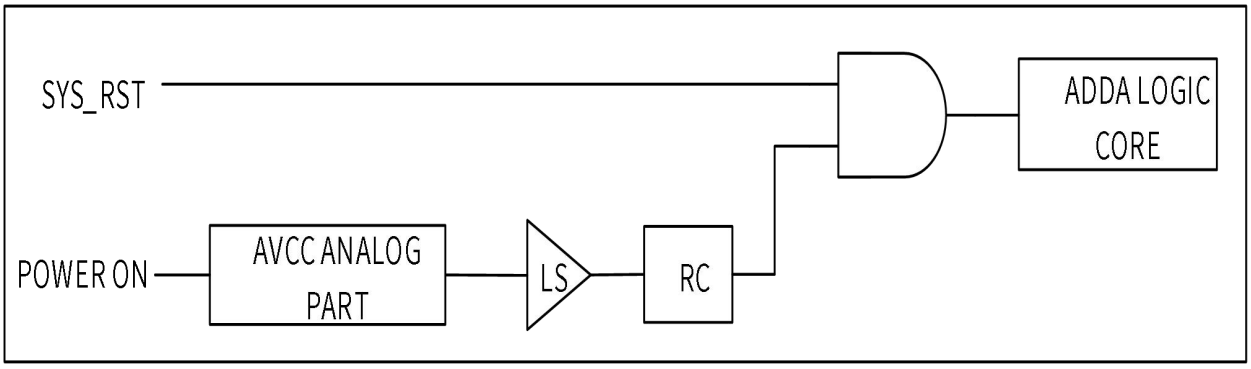
Analog Part Reset System

The following figure shows the reset system of the audio codec analog part.

Figure 4-4 Audio Codec Analog Part Reset System



When AVCC is powered on, it sends the AVCC_POR signal. The AVCC_POR signal passes the level shift and RC filter part to the Audio Codec logic core.

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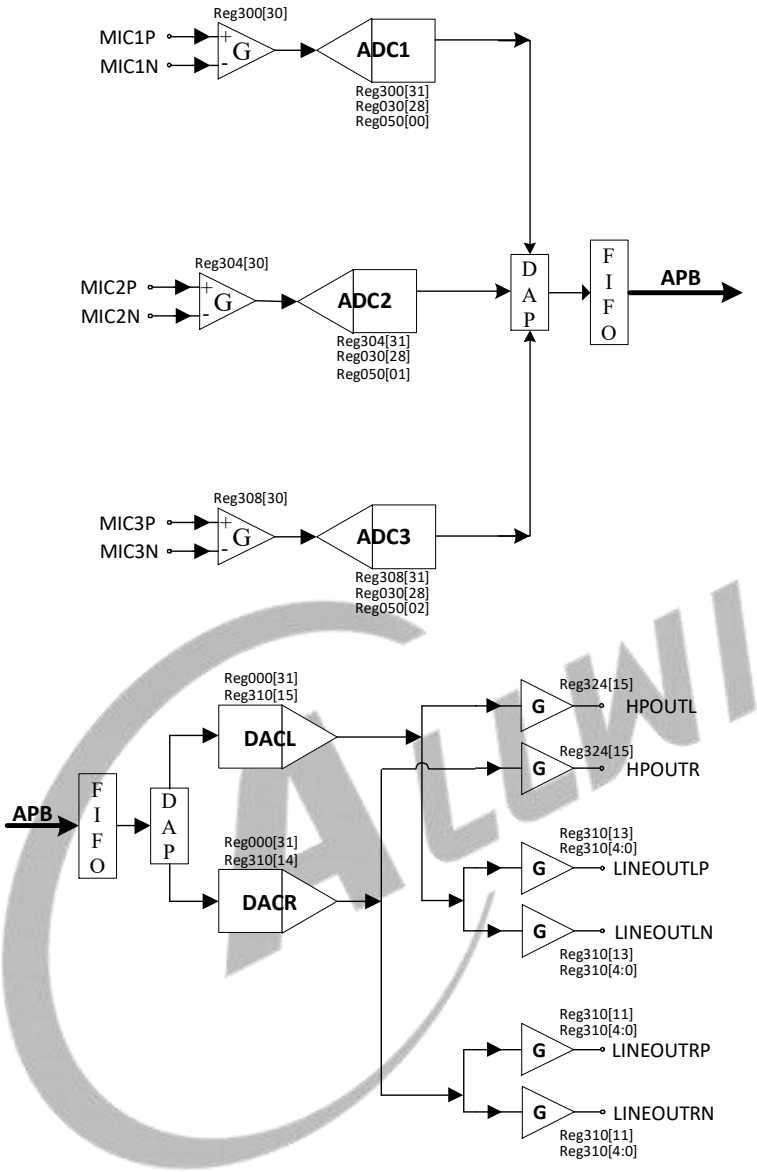
4.1.3.4 Data Path Diagram

The following figure shows a data path of the Audio Codec.

Figure 4-5 Audio Codec Data Path Diagram



4.1.3.5 Three ADCs

The three ADCs are used for recording stereo sound and a reference signal. The sample rates of the three ADCs are independent of the DAC sample rate. The digital ADC part can be enabled or disabled by the bit[28] of the AC_ADC_FIFOC register.

4.1.3.6 Stereo DACs

The stereo DAC sample rate can be configured by setting the register. To save power, the analog DACL can be enabled or disabled by setting the bit [15] of the DAC_REG register, and the analog

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DACR can be enabled or disabled by setting the bit [14] of the DAC_REGregister. The digital DAC part can be enabled or disabled by the bit [31] of the AC_DAC_DPC register.

4.1.3.7 Analog Audio Input Path

The Audio Codec supports 3 analog audio input paths:

- MICIN1P/N
- MICIN2P/N
- MICIN3P/N

The MICIN is a high impedance, low capacitance input suitable for connecting to various differential microphones of different dynamics and sensitivity. The gain for each pre-amplifier can be set independently. MBIAS provide reference voltage for electret condenser type(ECM) microphones.

4.1.3.8 Analog Audio Output Path

The Audio Codec has two types of analog output ports:

- LINEOUTLP
- LINEOUTLN
- LINEOUTRP
- LINEOUTRN
- HPOUTL
- HPOUTR

LINEOUTL/R

LINEOUTL/R provides one differential output to drive line signals to external audio equipment. The LINEOUTLP/N output source from DACL. The LINEOUTRP/N output source from DACR. The volume control is logarithmic with a 43.5 dB rang in 1.5 dB step from -43.5 dB to 0 dB. The LINEOUTL/R output buffer power up or down by bit [13] or bit [11] of DAC_REG (Offset: 0x0310).

Headphone Output

The headphone PA power up or down by bit [15] of HP_REG (Offset: 0x0324). HPOUTL/R can drive a 16R or 32R headphone load without DC capacitors by using Charge Pump to generate the negative rails. HP-FB is the ground loop noise rejection feedback. HBIAS provides reference voltage for electret condenser type (ECM) microphones.

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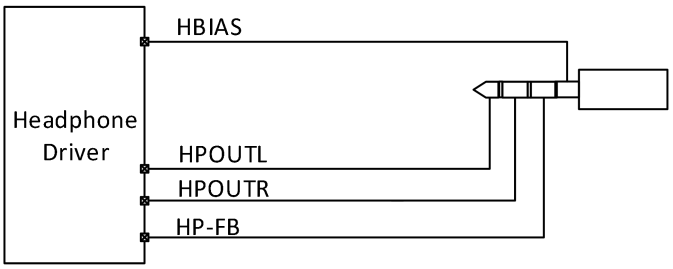
Figure 4-6 Headphone Output Application



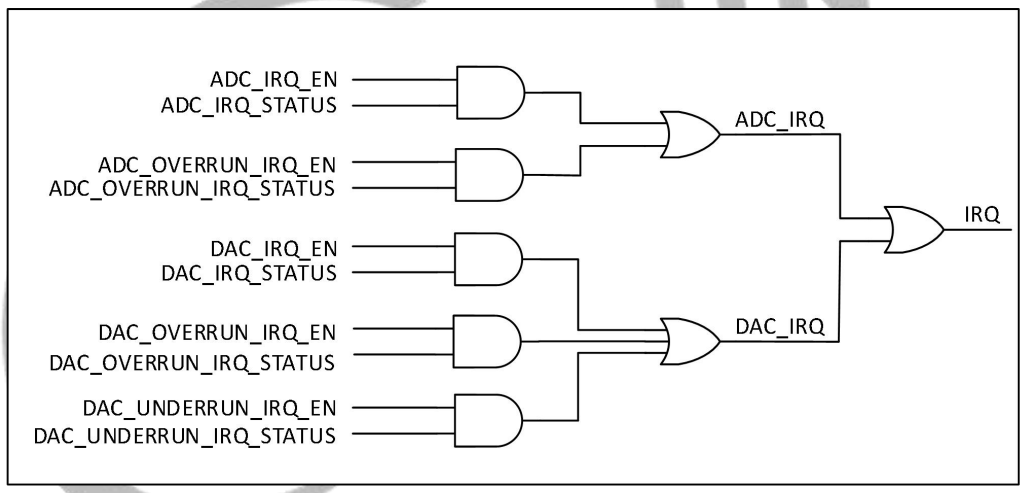
4.1.3.9 Microphone BIAS

The MBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network.

4.1.3.10 Interrupt

The Audio Codec has two groups of interrupt. The following figure describes the Audio Codec interrupt system.

Figure 4-7 Audio Codec Interrupt System



4.1.3.11 Digital Audio Processor (DAP)

The DAP module is used to remove the DC offset and automatically adjusts the volume to a flatten volume level. It mainly consists of two HPF and one DRC.

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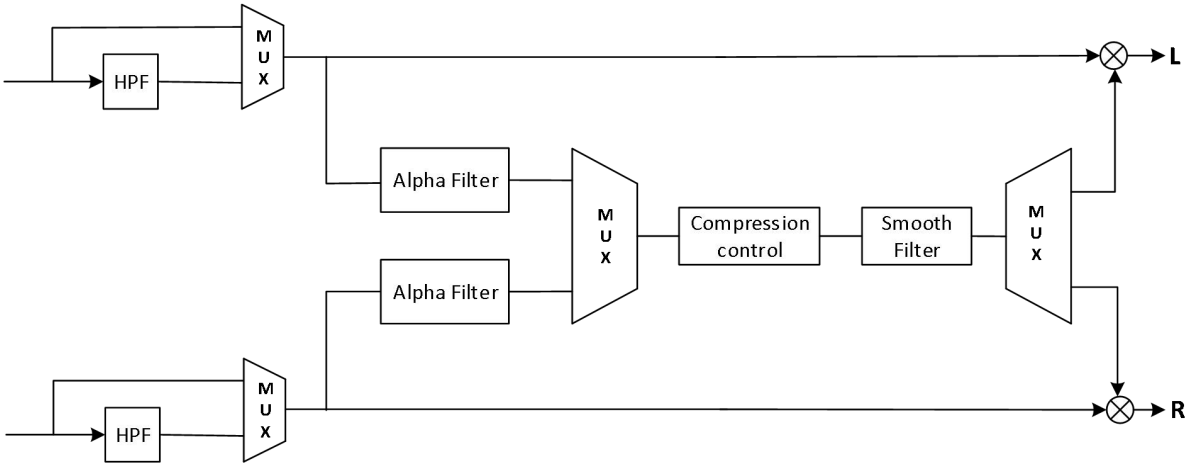
The following figure shows the DAP data flow.

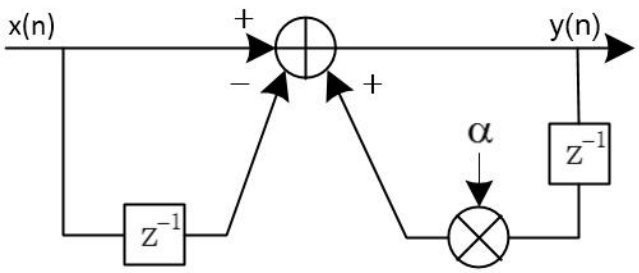
Figure 4-8 DAP Data Flow



HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enabled and disabled. The filter cutoff frhequency is less than 1 Hz that can be removed DC offset from ADC recording. The HPF can also be bypassed.

Figure 4-9 HPF Logic Structure



HPF transfer function is $H(z) = \frac{1 - z^{-1}}{1 - \alpha z^{-1}}$,that is y(n)=αy(n-1)+x(n)-x(n-1).

For cut-off frequency Fpass: w = Fpass/Fs * 2 * pi. Generally, w is small. So, $\alpha < 0, |\alpha| < 1$.

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DRC Function

The DRC scheme has three thresholds, three offsets, and four slopes (all programmable). There is one ganged DRC for the left and right channels. The following figure shows the diagram of DRC input/output.

Figure 4-10 DRC static Curve Parameters

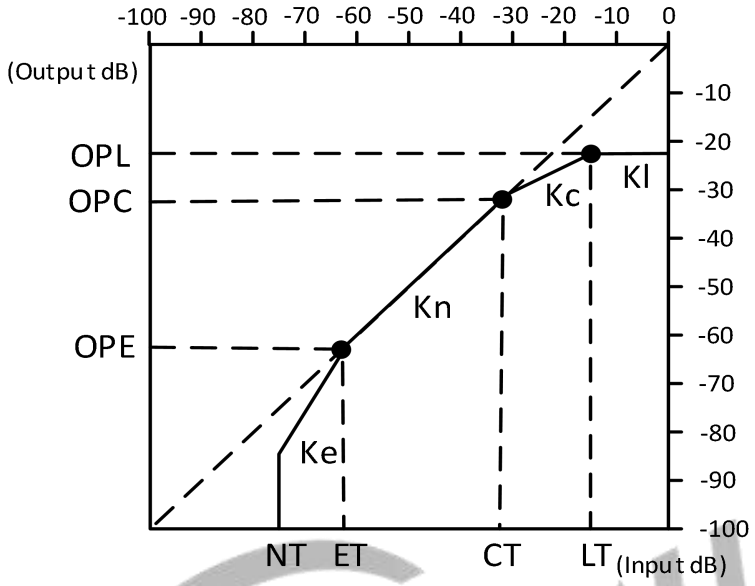

Figure 4-11 DRC Block Diagram

Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

One DRC for left/right and one DRC for subwoofer.

Each DRC has the adjustable threshold, offset, compression levels, programmable energy, attack, and decay time constants.

Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Configure the DRC parameters according to the following guidelines:

- Number format

The Number format is N.M which means there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 9.23 means that there are 9 bits at the left of the decimal point and 23 bits at the right decimal point.

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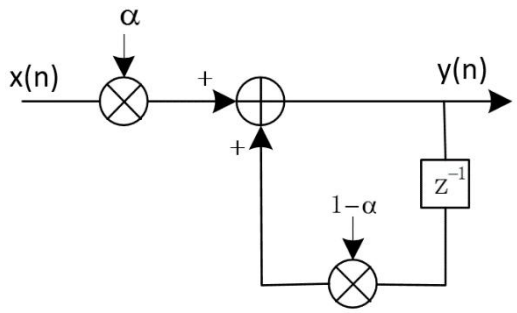
- Energy Filter

The following figure shows the structure of the energy filter.

Figure 4-12 Energy Filter Structure



The Energy Filter is to estimate of the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by $\alpha = 1 - e^{-2.2Ts/ta}$.

- Compression Control

This element has six parameters (ET, CT, LT, Ke, Kn, Kc, Kl, OPL, OPC, OPE), which are all programmable, and the computation will be explained as follows.

Threshold Parameter Computation (T parameter)

The threshold is the value that determines the signal to be compressed or not. When the signal's RMS is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by

$$Tin = -\frac{T_{dB}}{6.0206}$$

Where, T_{dB} must less than zero, the positive value is illegal.

For example, it is desired to set CT=-40dB, then the Tin require to set CT to -40dB is CTin = -(-40dB)/6.0206 = 6.644, CTin is entered as a 32-bit number in 8.24 format.

Therefore, CTin = 6.644 = 0000 0110.1010 0100 1101 0011 1100 0000 = 0x06A4 D3C0 in 8.24 format.

Slope Parameter Computation (K parameter)

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB is for n dB RMS input. The k input to the coefficient ram is computed by

$$K = \frac{1}{n}.$$

Where, n is from 1 to 50, and must be integer.

For example, it is desired to set 2:1, then the Kc require to set to 2:1 is Kc = 1/2 = 0.5, Kc is entered as a 32-bit number in 8.24 format.

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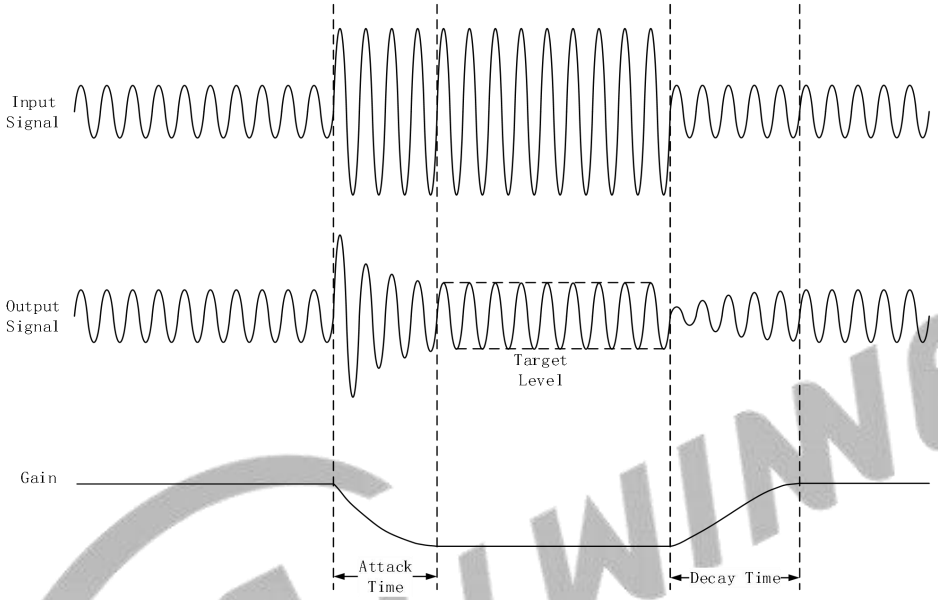
Therefore, Kc = 0.5 = 0000 0000.1000 0000 0000 0000 0000 0000 = 0x0080 0000 in 8.24 format.

- Gain Smooth Filter

The Gain Smooth Filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 1-17. The structure of the Gain Smooth filter is also the Alpha filter, so the rise time computation is the same as the Energy filter which is $\alpha = 1 - e^{-2.2Ts/ta}$.

Figure 4-13 Gain Smooth Filter



4.1.4 Programming Guidelines

4.1.4.1 Playing

Step 1 Codec initialization: configure AUDIO_CODEC_BGR_REG and AUDIO_CODEC_DAC_CLK_REG to open the audio codec bus clock gating, release the bus reset, and open the PLL_AUDIO DAC clock gating; set up PLL_AUDIO0_CTRL_REG to configure PLL_AUDIO0 frequency and enable PLL_AUDIO0. For details of PLL_AUDIO0, refer to section 2.5 Clock Controller Unit (CCU).

Step 2 Set up the sample rate and data transfer format, then open the DAC.

Step 3 Configure the DMA and DMA request.

Step 4 Enable the DAC DRQ and DMA.

4.1.4.2 Recording

Step 1 Codec initialization: configure AUDIO_CODEC_BGR_REG and AUDIO_CODEC_ADC_CLK_REG to open the audio codec bus clock gating, release the

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bus reset, and open the PLL_AUDIO1 ADC clock gating; set up PLL_AUDIO1_CTRL_REG to configure PLL_AUDIO1 frequency and enable PLL_AUDIO1. For details, refer to section 2.11 Power Reset Clock Management (PRCM).

Step 2 Configure the sample rate and data transfer format, then open the ADC.

Step 3 Configure the DMA and DMA request.

Step 4 Enable the ADC DRQ and DMA.

4.1.5 Register List

Module Name	Base Address
AUDIO CODEC	0x07110000

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
DAC_VOL_CTRL	0x0004	DAC Volume Control Register
AC_DAC_FIFOC	0x0010	DAC FIFO Control Register
AC_DAC_FIFOS	0x0014	DAC FIFO Status Register
AC_DAC_TXDATA	0x0020	DAC TX DATA Register
AC_DAC_CNT	0x0024	DAC TX FIFO Counter Register
AC_DAC_DG	0x0028	DAC Debug Register
AC_ADC_FIFOC	0x0030	ADC FIFO Control Register
ADC_VOL_CTRL1	0x0034	ADC Volume Control1 Register
AC_ADC_FIFOS	0x0038	ADC FIFO Status Register
AC_ADC_RXDATA	0x0040	ADC RX Data Register
AC_ADC_CNT	0x0044	ADC RX Counter Register
AC_ADC_DG	0x004C	ADC Debug Register
ADC_DIG_CTRL	0x0050	ADC Digtial Control Register
VRA1SPEEDUP_DOWN_CTRL	0x0054	VRA1Speedup Down Control Register
AC_DAC_DAP_CTRL	0x00F0	DAC DAP Control Register
AC_ADC_DAP_CTR	0x00F8	ADC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Left Peak Filter Low Attack Time Coef

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Register Name	Offset	Description
		Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_RPFHRT	0x0124	DAC DRC Right Peak filter High Release Time Coef Register
AC_DAC_DRC_RPFLRT	0x0128	DAC DRC Right Peak filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_RRMSHAT	0x0134	DAC DRC Right RMS Filter High Coef Register
AC_DAC_DRC_RRMSLAT	0x0138	DAC DRC Right RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Threshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Threshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Threshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold
AC_DAC_DRC_HET	0x016C	DAC DRC Expander Threshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Threshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth filter Gain Low Attack Time Coef

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Register Name	Offset	Description
		Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_RPFHAT	0x0214	ADC DRC Right Peak Filter High Attack Time Coef Register
AC_ADC_DRC_RPFLAT	0x0218	ADC DRC Right Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_RPFHRT	0x0224	ADC DRC Right Peak filter High Release Time Coef Register
AC_ADC_DRC_RPFLRT	0x0228	ADC DRC Right Peak filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_RRMSHAT	0x0234	ADC DRC Right RMS Filter High Coef Register
AC_ADC_DRC_RRMSLAT	0x0238	ADC DRC Right RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Threshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register

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Register Name	Offset	Description
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Threshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Threshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Threshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Threshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGHS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MNGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
ADC1_REG	0x0300	ADC1 Analog Control Register
ADC2_REG	0x0304	ADC2 Analog Control Register

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Register Name	Offset	Description
ADC3_REG	0x0308	ADC3 Analog Control Register
DAC_REG	0x0310	DAC Analog Control Register
DAC2_REG	0x0314	DAC2 Analog Control Register
MICBIAS_REG	0x0318	MICBIAS Analog Control Register
BIAS_REG	0x0320	BIAS Analog Control Register
HP_REG	0x0324	HEADPHONE Analog Control Register
HMIC_CTRL	0x0328	HMIC Control Register
HMIC_STS	0x032C	HMIC Status Register
POWER_REG	0x0348	POWER Analog Control Register

4.1.6 Register Description

4.1.6.1 0x0000 DAC Digital Part Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EN_DA DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels= [7*(21+MODQU [3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT=DVC [5:0] *(-1.16dB) 64 steps, -1.16dB/step
11	/	/	/
10:8	R/W	0x1	DITHER_SGM Dither Sigma

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Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	Read/Write	Default/Hex	Description
			000: Reserved 001: 1/2 010: $1/2^2$ 011: $1/2^3$ 100: $1/2^4$ 101: $1/2^5$ 110: $1/2^6$ 111: Reserved
7:4	R/W	0x0	DITHER_SFT Dither Shift Can increase the output amplitude of dither. 0000: $x2^0$ 0001: $x2^1$ 0010: $x2^2$ 0011: $x2^3$ ... 1011: $x2^{11}$ 1100: $x2^{12}$ 1101—1111:Reserved
3:2	/	/	/
1	R/W	0x0	DITHER_EN DSM Dither Enable 0: Disable 1: Enable
0	R/W	0x0	HUB_EN Audio Hub Enable The bit takes effect only when the EN_DA is set to 1. CPUS Domain: Audio Codec/ I2S0/ I2S1/ I2S2/I2S3/ OWA TXFIFO Hub Enable. 0: Disable 1: Enable

4.1.6.2 0x0004 DAC Volume Control Register (Default Value: 0x0000_A0A0)

Offset: 0x0004			Register Name: DAC_VOL_CTRL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DAC_VOL_SEL DAC Volume Control Selection Enable 0: Disable

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Offset: 0x0004			Register Name: DAC_VOL_CTRL
Bit	Read/Write	Default/Hex	Description
			1: Enable
15:8	R/W	0xA0	DAC_VOL_L DAC left channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB
7:0	R/W	0xA0	DAC_VOL_R DAC right channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB

4.1.6.3 0x0010 DAC FIFO Control Register (Default Value: 0x0000_4000)

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	DAC_FS Sample Rate of DAC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: 192 kHz 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: 96 kHz 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0	FIR_VER

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Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default/Hex	Description
			FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 20-bits transmitted audio sample: 00/10: FIFO_I [19:0] = {TXDATA [31:12]} 01/11: FIFO_I [19:0] = {TXDATA [19:0]} For 16-bits transmitted audio sample: 00/10: FIFO_I [19:0] = {TXDATA [31:16], 4'b0} 01/11: FIFO_I[19:0] = {TXDATA[15:0], 4'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, the DRQ request will be de-asserted. N is defined here: 00: IRQ/DRQ De-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL [12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ≤ TXTL Notes: WLEVEL represents the number of valid samples in the TX FIFO Only TXTL[6:0] valid when TXMODE = 0
7	/	/	/
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data
5	R/W	0x0	TX_SAMPLE_BITS

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Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default/Hex	Description
			Transmitting Audio Sample Resolution 0: 16 bits 1: 20 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Under Run IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	FIFO_FLUSH DAC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

4.1.6.4 0x0014 DAC FIFO Status Register (Default Value: 0x0080_8008)

Offset: 0x0014			Register Name: AC_DAC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/WC	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if

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Offset: 0x0014			Register Name: AC_DAC_FIFOS
Bit	Read/Write	Default/Hex	Description
			interrupt condition fails.
2	R/WC	0x0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/WC	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

4.1.6.5 0x0020 DAC TX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

4.1.6.6 0x0024 DAC TX FIFO Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: AC_DAC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

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4.1.6.7 0x0028 DAC Debug Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select: cksel 0: CODEC Clock from PLL 1: CODEC Clock from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC output channel swap enable, DA_SWP 0: Disable 1:Enable
5:3	/	/	/
2:0	R/W	0x0	ADDA_LOOP_MODE Audio Codec Loop MODE SELECT 000: Disable 001: ADDA LOOP MODE DACL/DACR connect to ADC1/ADC2 010: ADDA LOOP MODE DACL connect to ADC3 1xx: Reserved

4.1.6.8 0x0030 ADC FIFO Control Register (Default Value: 0x0000_0400)

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48 kHz 010: 24 kHz 100: 12 kHz

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Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
			110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable
27:26	R/W	0x0	ADCFDT ADC FIFO Delay Time for writing Data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms
25	R/W	0x0	ADCDFEN ADC FIFO Delay Function for writing Data after EN_AD 0: Disable 1: Enable
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 20-bits received audio sample: Mode 0: RXDATA [31:0] = {FIFO_O [19:0], 12'h0} Mode 1: RXDATA [31:0] = {12{FIFO_O [19]}, FIFO_O [19:0]} For 16-bits received audio sample: Mode 0: RXDATA [31:0] = {FIFO_O [19:4], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[19]}, FIFO_O[19:4]}
23:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START Only if RX_SYNC_EN set 1, RX_SYNC_EN_START can take effect. CPUS Domain：Audio Codec/ I2S0/ I2S1/ I2S2/ DMIC/ OWA RX

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Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
			Synchronize Enable Start. 0: Disable 1: Enable
20	R/W	0x0	RX_SYNC_EN Audiocodec RX Synchronize Enable 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 20 bits
15:12	/	/	/
11:4	R/W	0x40	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL [5:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ Generated when WLEVEL ＞ RXTL[5:0] Notes: WLEVEL represents the number of valid samples in the RX FIFO
3	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self-clear to '0'.

4.1.6.9 0x0034 ADC Volume Control1 Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: ADC_VOL_CTRL1
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0034			Register Name: ADC_VOL_CTRL1
Bit	Read/Write	Default/Hex	Description
31:24	R	0xA0	PLACE_HOLDER No meaning
23:16	R/W	0xA0	ADC3_VOL ADC3 channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB
15:8	R/W	0xA0	ADC2_VOL ADC2 channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB
7:0	R/W	0xA0	ADC1_VOL ADC1 channel volume (-119.25dB to 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ..... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ..... 0xFF = 71.25dB

4.1.6.10 0x0038 ADC FIFO Status Register (Default Value: 0x0000_0001)

Offset: 0x0038			Register Name: AC_ADC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

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Offset: 0x0038			Register Name: AC_ADC_FIFOS
Bit	Read/Write	Default/Hex	Description
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:17	/	/	/
16:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/WC	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/WC	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	R	0x1	PLACE_HOLDER No meaning

4.1.6.11 0x0040 ADC RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_ADC_RXDATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

4.1.6.12 0x0044 ADC RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO.

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Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	Read/Write	Default/Hex	Description
			When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

4.1.6.13 0x004C ADC Debug Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	AD_SWP2 ADC output channel swap enable (for digital filter) 0: Disable 1: Enable Note:ADC3 and ADC4(2`b0) swap data.
24	R/W	0x0	AD_SWP1 ADC output channel swap enable (for digital filter) 0: Disable 1: Enable Note:ADC1 and ADC2 swap data.
23:0	/	/	/

4.1.6.14 0x0050 ADC Digtial Control Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ADC_DIG_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	ADC3_VOL_EN ADC3 Volume Control Enable 0: Disable 1: Enable
16	R/W	0x0	ADC1_2_VOL_EN ADC1/2 Volume Control Enable 0: Disable 1: Enable
15:3	/	/	/

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Offset: 0x0050			Register Name: ADC_DIG_CTRL
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	ADC_CHANNEL_EN Bit 2: ADC3 enable Bit 1: ADC2 enable Bit 0: ADC1 enable

4.1.6.15 0x0054 VRA1Speedup Down Control Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: VRA1SPEEDUP_DOWN_CTRL
Bit	Read/Write	Default/Hex	Description
31:05	/	/	/
4	R	0x0	VRA1SPEEDUP_DOWN_STATE Only if VAR1SPEEDUP_DOWN_Further_CTRL (0x310[22]) set 0, VAR1Speedup Down State is valid. 0: VAR1Speedup_Down not work 1: VAR1Speedup_Down work
3:2	/	/	/
1	R/W	0x0	VRA1SPEEDUP_DOWN_CTRL VAR1Speedup Down Manual Control Enable 0: Disable, VAR1Speedup Down convert 1 after bus RST release 32ms. 1: Enable,VAR1Speedup Down convert 1 immediately.
0	R/W	0x0	VRA1SPEEDUP_DOWN_RST_CTRL VAR1Speedup Down RST Manual Control Enable 0: Disable, VAR1Speedup Down convert 1 after bus RST release 32ms. 1: Enable,VAR1Speedup Down reset 0 immediately.

4.1.6.16 0x00F0 DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0X0	DDAP_EN DAP for DRC Enable 0: Bypass 1: Enable
30	/	/	/
29	R/W	0X0	DDAP_DRC_EN

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Offset: 0x00F0			Register Name: AC_DAC_DAP_CTRL
Bit	Read/Write	Default/Hex	Description
			DRC Enable Control 0: Disable 1: Enable
28	R/W	0X0	DDAP_HPF_EN HPF Enable Control 0: Disable 1: Enable
27:0	/	/	/

4.1.6.17 0x00F8 ADC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ADC_DAP0_EN DAP for ADC1/2 Enable (Adjust the position, and two DRCs use the same parameter) 0: bypass 1:enable
30	/	/	/
29	R/W	0x0	ADC_DRC0_EN ADC DRC0 Enable Control 0: disable 1:enable
28	R/W	0x0	ADC_HPF0_EN ADC HPF0 Enable Control 0: disable 1:enable
27	R/W	0x0	ADC_DAP1_EN ADC DAP1 Enable Control This bit is to control the DAP for ADC3.
26	/	/	/
25	R/W	0x0	ADC_DRC1_EN ADC DRC1 enable control 0: disable 1:enable
24	R/W	0x0	ADC_HPF1_EN ADC HPF1 enable control 0: disable 1:enable

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Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	Read/Write	Default/Hex	Description
23:0	/	/	/

4.1.6.18 0x0100 DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0xFF	DAC_DRC_HHPF_COE HPF coefficient setting and the data is 3.24 format.

4.1.6.19 0x0104 DAC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	DAC_DRC_LHPF_COE HPF coefficient setting and the data is 3.24 format.

4.1.6.20 0x0108 DAC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0	DAC_DRC_DELAY_BUF_STATE DRC delay buffer data output state when DRC delay function is enable and the DRC function disable. After disable DRC function and this bit go to 0, the user should write the DRC delay function bit to 0; 0: not complete 1 : is complete
14:10	/	/	/
13:8	R/W	0	DAC_DRC_SIGNAL_DELAY_TIME_SET Signal delay time setting 6'h00: (8x1) fs 6'h01: (8x2) fs 6'h02: (8x3) fs ---------- 6'h2e: (8*47) fs

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Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
			6'h2f: (8*48) fs 6'h30 -- 6'h3f: (8*48) fs Delay time = 8*(n+1) fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	DAC_DRC_DELAY_BUF_EN The delay buffer use or not when the DRC disable and the DRC buffer data output completely 0: don't use the buffer 1 : use the buffer
6	R/W	0x0	DAC_DRC_GAIN_MAX_LIMIT_EN DRC gain max limit enable 0: disable 1 : enable
5	R/W	0x0	DAC_DRC_GAIN_MIN_LIMIT_EN DRC gain min limit enable. when this function enables, it will overwrite the noise detect function. 0: disable 1 : enable
4	R/W	0x0	DAC_DRC_DETECT_NOISE_EN Control the DRC to detect noise when ET enable 0: disable 1 : enable
3	R/W	0x0	DAC_DRC_SIGNAL_FUNC_SEL Signal function Select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	DAC_DRC_DELAY_FUNC_EN Delay function enable 0: disable 1: enable

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Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
			When the Delay function enable is disable, the Signal delay time is unused.
1	R/W	0x0	DAC_DRC_LT_EN DRC LT enable 0: disable 1: enable When the DRC LT is disable the LT, Kl and OPL parameter is unused.
0	R/W	0x0	DAC_DRC_ET_EN DRC ET enable 0: disable 1: enable When the DRC ET is disable the ET, Ke and OPE parameter is unused.

4.1.6.21 0x010C DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x000B	DAC_DRC_LPFHAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.22 0x0110 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	DAC_DRC_LPFLAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

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4.1.6.23 0x0114 DAC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0114 0x0000_000B)

Offset: 0x0114			Register Name: AC_DAC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x000B	DAC_DRC_RPFHAT The right peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.24 0x0118 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	DAC_DRC_RPFLAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.25 0x011CDAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	DAC_DRC_LPFHRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.26 0x0120 DAC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	DAC_DRC_LPFLRT The left peak filter release time parameter setting,

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Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
			which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.27 0x0124 DAC DRC Right Peak filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0124			Register Name: AC_DAC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	DAC_DRC_RPFHRT The right peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.28 0x0128 DAC DRC Right Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0128			Register Name: AC_DAC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	DAC_DRC_RPFLRT The right peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.29 0x012CDAC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	DAC_DRC_LRMSHAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24.(The default value is 10ms)

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4.1.6.30 0x0130 DAC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_LRMSLAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.31 0x0134 DAC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0134			Register Name: AC_DAC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0001	DAC_DRC_RRMSHAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24.(The default value is 10ms)

4.1.6.32 0x0138 DAC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0138			Register Name: AC_DAC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_RRMSLAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24.(10ms)

4.1.6.33 0x013CDAC DRC Compressor Threshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	DAC_DRC_HCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

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4.1.6.34 0x0140 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	DAC_DRC_LCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.35 0x0144 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	DAC_DRC_HKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (The default value is <2 : 1>)

4.1.6.36 0x0148 DAC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is <2 : 1>)

4.1.6.37 0x014C DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	DAC_DRC_HOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is

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Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
			8.24. (The default value is -40dB)

4.1.6.38 0x0150 DAC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	DAC_DRC_LOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.39 0x0154 DAC DRC Limiter Threshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	DAC_DRC_HLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

4.1.6.40 0x0158 DAC DRC Limiter Threshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	DAC_DRC_LLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

4.1.6.41 0x015C DAC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0005	DAC_DRC_HKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50:1>)

4.1.6.42 0x0160 DAC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	DAC_DRC_LKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50 :1>)

4.1.6.43 0x0164 DAC DRC Limiter High Output at Limiter Threshold (Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	DAC_DRC_HOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

4.1.6.44 0x0168 DAC DRC Limiter Low Output at Limiter Threshold (Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	DAC_DRC_LOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

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4.1.6.45 0x016C DAC DRC Expander Threshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	DAC_DRC_HET The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

4.1.6.46 0x0170 DAC DRC Expander Threshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	DAC_DRC_LET The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

4.1.6.47 0x0174 DAC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0500	DAC_DRC_HKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.48 0x0178 DAC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must

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Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
			larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.49 0x017C DAC DRC Expander High Output at Expander Threshold (Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	DAC_DRC_HOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.50 0x0180 DAC DRC Expander Low Output at Expander Threshold (Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	DAC_DRC_LOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.51 0x0184 DAC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	DAC_DRC_HKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.52 0x0188 DAC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0000	DAC_DRC_LKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.53 0x018C DAC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	DAC_DRC_SFHAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.54 0x0190 DAC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	DAC_DRC_SFLAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.55 0x0194 DAC DRC Smooth Filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	DAC_DRC_SFHRT The gain smooth filter release time parameter setting, which determine by the equation that RT

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Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
			= 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.56 0x0198 DAC DRC Smooth Filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	DAC_DRC_SFLRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.57 0x019C DAC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFE56	DAC_DRC_MXGHS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB. (The default value is -10dB)

4.1.6.58 0x01A0 DAC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	DAC_DRC_MXGLS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB. (The default value is -10dB)

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4.1.6.59 0x01A4 DAC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	DAC_DRC_MNGHS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.60 0x01A8 DAC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	DAC_DRC_MNGLS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.61 0x01AC DAC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	DAC_DRC_EPSHC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.62 0x01B0 DAC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	DAC_DRC_EPSLC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT =

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Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
			1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.63 0x01B8 DAC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	DAC_DRC_HPFHGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.64 0x01BC DAC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_HPFLGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.65 0x0200 ADC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0xFF	ADC_DRC_HHPFC HPF coefficient setting and the data is 3.24 format.

4.1.6.66 0x0204 ADC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	ADC_DRC_LHPFC HPF coefficient setting and the data is 3.24 format.

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4.1.6.67 0x0208 ADC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ADC_DRC_DELAY_BUF_OUTPUT_STATE DRC delay buffer data output state when DRC delay function is enable and the DRC function disable. After disable DRC function and this bit go to 0, the user should write the DRC delay function bit to 0; 0: not complete 1 : is complete
14:10	/	/	/
13:8	R/W	0x0	ADC_DRC_SIGNAL_DELAY_TIME_SET Signal delay time setting 6'h00: (8x1) fs 6'h01: (8x2) fs 6'h02: (8x3) fs ---------- 6'h2e: (8*47) fs 6'h2f: (8*48) fs 6'h30 -- 6'h3f: (8*48) fs Delay time = 8*(n+1) fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	ADC_DRC_DELAY_BUF_EN The delay buffer use or not when the dry disable and the DRC buffer data output completely 0: don't use the buffer 1 : use the buffer
6	R/W	0x0	ADC_DRC_GAIN_MAX_LIMIT_EN DRC gain max limit enable 0: disable 1 : enable
5	R/W	0x0	ADC_DRC_GAIN_MIN_LIMIT_EN DRC gain min limit enable. when this function enables, it will overwrite the noise detect function. 0: disable 1 : enable
4	R/W	0x0	ADC_DRC_DETECT_NOISE_EN Control the DRC to detect noise when ET enable

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Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
			0: disable 1 : enable
3	R/W	0x0	ADC_DRC_SIGNAL_FUNC_SEL Signal function Select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	ADC_DRC_DELAY_FUNC_EN Delay function enable 0: disable 1: enable When the Delay function enable is disable, the Signal delay time is unused.
1	R/W	0x0	ADC_DRC_LT_EN DRC LT enable 0: disable 1: enable DRC LT enable 0: disable 1: enable When the DRC LT is disable the LT, Kl and OPL parameter is unused.
0	R/W	0x0	ADC_DRC_ET_EN DRC ET enable 0: disable 1: enable When the DRC ET is disable the ET, Ke and OPE parameter is unused.

4.1.6.68 0x020C ADC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x020C	Register Name: AC_ADC_DRC_LPFHAT

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Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x000B	ADC_DRC_LPFHAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.69 0x0210 ADC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	ADC_DRC_LPFLAT The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.70 0x0214 ADC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0214			Register Name: AC_ADC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x000B	ADC_DRC_RPFHAT The right peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

4.1.6.71 0x0218 ADC DRC Right Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0218			Register Name: AC_ADC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	ADC_DRC_RPFLAT The right peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(The default value is 1ms)

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4.1.6.72 0x021C ADC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	ADC_DRC_LPFHRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.73 0x0220 ADC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	ADC_DRC_LPFLRT The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.74 0x0224 ADC DRC Right Peak filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0224			Register Name: AC_ADC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	ADC_DRC_RPFHRT The right peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.75 0x0228 ADC DRC Right Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	ADC_DRC_RPFLRT The right peak filter release time parameter setting, which determine by the equation that AT

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Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
			= exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

4.1.6.76 0x022C ADC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	ADC_DRC_LRMSHAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.77 0x0230 ADC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	ADC_DRC_LRMSLAT The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.78 0x0234 ADC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0234			Register Name: AC_ADC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0001	ADC_DRC_RRMSHAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.79 0x0238 ADC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0238	Register Name: AC_ADC_DRC_RRMSLAT

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Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	ADC_DRC_RRMSLAT The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

4.1.6.80 0x023C ADC DRC Compressor Threshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	ADC_DRC_HCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.81 0x0240 ADC DRC Compressor Slope High Setting RegisterB (Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	ADC_DRC_LCT The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.82 0x0244 ADC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	ADC_DRC_HKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (The default value is <2 : 1>)

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4.1.6.83 0x0248 ADC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKC The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is integer. The format is 8.24. (The default value is <2 : 1>)

4.1.6.84 0x024C ADC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	ADC_DRC_HOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.85 ADC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0250 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	ADC_DRC_LOPC The output of the compressor which determine by the equation OPCin=OPC/6.0206. The format is 8.24. (The default value is -40dB)

4.1.6.86 0x0254 ADC DRC Limiter Threshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	ADC_DRC_HLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is

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Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
			8.24. (The default value is -10dB)

4.1.6.87 0x0258 ADC DRC Limiter Threshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	ADC_DRC_LLT The limiter threshold setting, which set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

4.1.6.88 0x025C ADC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0005	ADC_DRC_HKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50:1>)

4.1.6.89 0x0260 ADC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	ADC_DRC_LKl The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is integer. The format is 8.24. (The default value is <50:1>)

4.1.6.90 0x0264 ADC DRC Limiter High Output at Limiter Threshold (Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xFBD8	ADC_DRC_HOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

4.1.6.91 0x0268 ADC DRC Limiter Low Output at Limiter Threshold (Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	ADC_DRC_LOPL The output of the limiter which determine by equation OPTin=OPT/6.0206. The format is 8.24. (The default value is -25dB)

4.1.6.92 0x026C ADC DRC Expander Threshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	ADC_DRC_HET The expander threshold setting, which set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.93 0x0270 ADC DRC Expander Threshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	ADC_DRC_LET The expander threshold setting, which set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.94 0x0274 ADC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description

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Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0500	ADC_DRC_HKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.95 0x0278 ADC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKE The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

4.1.6.96 0x027C ADC DRC Expander High Output at Expander Threshold (Default Value: 0x0000F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	ADC_DRC_HOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

4.1.6.97 0x0280 ADC DRC Expander Low Output at Expander Threshold (Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	ADC_DRC_LOPE The output of the expander which determine by equation OPEin=OPE/6.0206. The format is 8.24. (The default value is -70dB)

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4.1.6.98 0x0284 ADC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	ADC_DRC_HKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.99 0x0288 ADC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKN The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is integer. The format is 8.24. (The default value is <1:1>)

4.1.6.100 0x028C ADC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	ADC_DRC_SFHAT The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.101 0x0290 ADC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	ADC_DRC_SFLAT

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Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
			The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

4.1.6.102 0x0294 ADC DRC Smooth Filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	ADC_DRC_SFHRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.103 0x0298 ADC DRC Smooth Filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	ADC_DRC_SFLRT The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

4.1.6.104 0x029C ADC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFE56	ADC_DRC_MXGHS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (The default value is -10dB)

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4.1.6.105 0x02A0 ADC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	ADC_DRC_MXGLS The max gain setting which determine by equation MXGin=MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (The default value is -10dB)

4.1.6.106 0x02A4 ADC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	ADC_DRC_MNGHS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.107 0x02A8 ADC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	ADC_DRC_MNGLS The min gain setting which determine by equation MNGin=MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB. (The default value is -40dB)

4.1.6.108 0x02AC ADC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	ADC_DRC_EPSHC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default

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Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
			value is 30ms)

4.1.6.109 0x02B0 ADC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	ADC_DRC_EPSLC The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

4.1.6.110 0x02B8 ADC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	ADC_DRC_HPFHGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.111 0x02BC ADC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_HPFLGAIN The gain of the HPF coefficient setting which format is 3.24.(gain = 1)

4.1.6.112 0x0300 ADC1 Analog Control Register (Default Value:0x001C_C055)

Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
31	R/W	0x0	ADC1_EN ADC1 Channel Enable 0: Disable

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Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
			1: Enable
30	R/W	0x0	MIC1_PGA_EN MIC1 PGA Enable 0: Disable 1: Enable
29	R/W	0x0	ADC1 Dither Control 0: New Dither Off 1: New Dither On
28:26	R/W	0x0	/
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 0: No Level 1: Min Level 2: Middle Level 3:Max Level
23:22	R/W	0x0	/
21:20	R/W	0x1	ADC1_OUTPUT_CURRENT ADC1 high gain OP Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7uA
19:18	R/W	0x3	ADC1_PGA_CTRL_RCM ADC1 PGA Common Mode Input Impedance Control for MIC 0: 100 kΩ 1: 75 kΩ 2: 50 kΩ 3: 25 kΩ
17:16	R/W	0x0	ADC1_PGA_IN_VCM_CTRL ADC1 PGA Common-Mode Voltage Control 0: 900mV 1: 800mV 2: 750mV 3: 700mV
15:14	R/W	0x3	IOPADC ADC1-ADC3 Bias Current Select 00: 1uA 01: 2uA

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Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
			10: 3uA 11: 4uA
13	R/W	0x0	/
12:8	R/W	0x0	ADC1_PGA_GAIN_CTRL ADC1 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
7:6	R/W	0x1	ADC1_IOPAAF ADC1 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA For example: ADC1_REG<15:14> =11，IOPADC=4uA 00: 1.50*4uA=6uA 01: 1.75*4uA=7uA 10: 2.00*4uA=8uA 11: 2.25*4uA=9uA
5:4	R/W	0x1	ADC1_IOPSDM1 ADC1 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

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Offset: 0x0300			Register Name: ADC1_REG
Bit	R/W	Default	Description
3:2	R/W	0x1	ADC1_IOPSDM2 ADC1 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
1:0	R/W	0x1	ADC1_IOPMIC ADC1 OP MIC Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

4.1.6.113 0x0304 ADC2 Analog Control Register (Default Value:0x001C_0055)

Offset: 0x0304			Register Name: ADC2_REG
Bit	R/W	Default	Description
31	R/W	0x0	ADC2_EN ADC2 Channel Enable 0: Disable 1: Enable
30	R/W	0x0	MIC2_PGA_EN MIC2 PGA Enable 0: Disable 1: Enable
29	R/W	0x0	ADC2 Dither Control 0: New Dither Off 1: New Dither On
28:26	R/W	0x0	/
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 0: No Level 1: Min Level 2: Middle Level 3:Max Level
23:22	R/W	0x0	/
21:20	R/W	0x1	ADC2_OUTPUT_CURRENT ADC2 high gain OP Output Current Select

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Offset: 0x0304			Register Name: ADC2_REG
Bit	R/W	Default	Description
			00: 15I 01: 20I 10: 35I 11: 40I I=7uA
19:18	R/W	0x3	ADC2_PGA_CTRL_RCM ADC2 PGA Common Mode Input Impedance Control for MICIN 0: 100 kΩ 1: 75 kΩ 2: 50 kΩ 3: 25 kΩ
17:16	R/W	0x0	ADC2_PGA_IN_VCM_CTRL ADC2 PGA Common-Mode Voltage Control 0: 900mV 1: 800mV 2: 750mV 3: 700mV
15:13	/	/	/
12:8	R/W	0x0	ADC2_PGA_GAIN_CTRL ADC2 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
7:6	R/W	0x1	ADC2_IOPAAF ADC2 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC

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Offset: 0x0304			Register Name: ADC2_REG
Bit	R/W	Default	Description
			10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
5:4	R/W	0x1	ADC2_IOPSDM1 ADC2 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
3:2	R/W	0x1	ADC2_IOPSDM2 ADC2 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
1:0	R/W	0x1	ADC2_IOPMIC1 ADC2 OP MIC1 Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

4.1.6.114 0x0308 ADC3 Analog Control Register (Default Value:0x001C_0055)

Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
31	R/W	0x0	ADC3_EN ADC3 Channel Enable 0: Disable 1: Enable
30	R/W	0x0	MIC3_PGA_EN MIC3 PGA Enable 0: Disable 1: Enable
29	R/W	0x0	ADC3 Dither Control 0: New Dither Off 1: New Dither On
28:26	R/W	0x0	/

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Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive related to the ctrl bits) 0: No Level 1: Min Level 2: Middle Level 3:Max Level
23:22	R/W	0x0	/
21:20	R/W	0x1	ADC3_OUTPUT_CURRENT ADC3 high gain OP Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7uA
19:18	R/W	0x3	ADC3_PGA_CTRL_RCM ADC3 PGA Common Mode Input Impedance Control for MICIN 0: 100 kΩ 1: 75 kΩ 2: 50 kΩ 3: 25 kΩ
17:16	R/W	0x0	ADC3_PGA_IN_VCM_CTRL ADC3 PGA Common-Mode Voltage Control 0: 900mV 1: 800mV 2: 750mV 3: 700mV
15:13	/	/	/
12:8	R/W	0x0	ADC3_PGA_GAIN_CTRL ADC3 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB

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Offset: 0x0308			Register Name: ADC3_REG
Bit	R/W	Default	Description
			0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
7:6	R/W	0x1	ADC3_IOPAAF ADC3 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
5:4	R/W	0x1	ADC3_IOPSDM1 ADC3 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
3:2	R/W	0x1	ADC3_IOPSDM2 ADC3 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA
1:0	R/W	0x1	ADC3_IOPMIC ADC3 OP MIC Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1uA to 4uA

4.1.6.115 0x0310 DAC Analog Control Register (Default Value:0x0455_0100)

Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
31	R/W	0x0	CURRENT_TEST_SELECT Internal Current Sink Test Enable (from MICIN3P pin)

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Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
			0: Normal 1: For Debug
30:28	R/W	0x0	HEADPHONE_GAIN 000: -0dB 001: -6dB 010: -12dB 011: -18dB 100: -24dB 101: -30dB 110: -36dB 111:-42dB
27:26	R/W	0x1	IOPHPDRV HPDRVL/R OP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
25:24	R/W	0x0	CPLDO_VOLTAGE 00:0.9V 01:1.0V 10:1.1V 11:1.2V
23:22	R/W	0x1	OPDRV_CUR. OPDRV output stage current setting 00:6uA 01:7uA 10:8uA 11:9uA
21:20	R/W	0x1	IOPVRS VRA2 Buffer OP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
19:18	R/W	0x1	ILINEOUTAMPS LINEOUTL/R AMP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
17:16	R/W	0x1	IOPDACS

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Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
			OPDAC Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
15	R/W	0x0	DACL_EN DACL Enable 0: Disable 1: Enable
14	R/W	0x0	DACR_EN DACR Enable 0: Disable 1: Enable
13	R/W	0x0	LINEOUTLEN Left Channel LINEOUT Enable 0: Disable 1: Enable
12	R/W	0x0	LMUTE DACL to Left Channel LINEOUT Mute Control 0: Mute 1: Not mute
11	R/W	0x0	LINEOUTREN Right Channel LINEOUT Enable 0: Disable 1: Enable
10	R/W	0x0	RMUTE DACR to Right Channel LINEOUT Mute Control 0: Mute 1: Not mute
9:8	R/W	0x1	ICPLDO CPLDO Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
7	R/W	0x0	CPLDO_ENABLE 0: Disable 1:Enable
6:5	R/W	0x0	/
4:0	R/W	0x0	LINEOUT Volume Control, Total 30 level from 0x1F to 0x02 with the volume 0dB to -43.5dB, -1.5dB/step, mute when

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Offset: 0x0310			Register Name: DAC_REG
Bit	R/W	Default	Description
			00000 & 00001.

4.1.6.116 0x0314 DAC2 Analog Control Register (Default Value:0x0000_0000)

Offset: 0x0314			Register Name: DAC2_REG
Bit	R/W	Default	Description
31:18	R/W	0x0	/
17:16	R/W	0x0	CKDAC_DELAY_SET clock delay time after CKDAC 0: min 3: max
15	R/W	0x0	DACL/R_CHOPPER_ENABLE DACL/R chopper enable 0: chopper disable 1: chopper enable
14	R/W	0x0	DACL/R_CHOPPER_NOL_ENABLE DACL/R chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled 1: chopper non-overlapping clock enabled
13:12	R/W	0x0	DACL/R_CHOPPER_CKSET DACL/R chopper clock frequency Fs:6.144MHz 0: 96 kHz 1: 192 kHz 2: 384 kHz 3: 768 kHz
11:10	R/W	0x0	DACL/R_CHOPPER_DELAY_SET Control DACL/R chopper clock delay time after CKDAC 0: Min 3: Max
9:8	R/W	0x0	DACL/R_CHOPPER_NOL_DELAY_SET Control DACL/R chopper clock non-overlapping time 0: Min when DAC_CHOPPER_NOL_ENABLE=1 3: Max when DAC_CHOPPER_NOL_ENABLE=1
7	R/W	0x0	LINEOUTL/R_CHOPPER_ENABLE LINEOUTL/R chopper enable 0: chopper disable 1: chopper enable
6	R/W	0x0	LINEOUTL/R_CHOPPER_NOL_ENABLE LINEOUTL/R chopper non-overlapping clock enable 0: chopper non-overlapping clock disabled

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Offset: 0x0314			Register Name: DAC2_REG
Bit	R/W	Default	Description
			1: chopper non-overlapping clock enabled
5:4	R/W	0x0	LINEOUTL/R_CHOPPER_CKSET LINEOUTL/R chopper clock frequency Fs:6.144MHz 0: 96kHz 1: 192kHz 2: 384kHz 3: 768kHz
3:2	R/W	0x0	LINEOUTL/R_CHOPPER_DELAY_SET Control LINEOUTL/R chopper clock delay time after CKDAC 0: Min 3: Max
1:0	R/W	0x0	LINEOUTL/R_CHOPPER_NOL_DELAY_SET Control LINEOUTL/R chopper clock non-overlapping time 0: Min when LINEOUT_CHOPPER_NOL_ENABLE=1 3: Max when LINEOUT_CHOPPER_NOL_ENABLE=1

4.1.6.117 0x0318 MICBIAS Analog Control Register (Default Value:0x4000_3030)

Offset: 0x0318			Register Name: MICBIAS_REG
Bit	R/W	Default	Description
31	R/W	0x0	/
30:28	R/W	0x4	SELDETADCFS Select sample interval of the ADC sample 000: 2ms … 100: 32ms … 111: 256ms
27:26	R/W	0x0	SELDETADCDB Select debounce time when jack removal 00: 128ms 01: 256ms 10: 512ms 11: 1024ms
25:24	R/W	0x0	SELDETADCBF Select the time to enable HBIAS before MICADC work 00: 2ms 01: 4ms 10: 8ms

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Offset: 0x0318			Register Name: MICBIAS_REG
Bit	R/W	Default	Description
			11: 16ms
23	R/W	0x0	JACKDETEN Jack detect enable 0: Disable 1: Enable
22:21	R/W	0x0	SELDETADCDY Select the delay time to pull low the MICDET when jack removal 00: 0.5ms 01: 1ms 10: 1.5ms 11: 2ms
20	R/W	0x0	MICADCEN Microphone detect ADC enable 0: Disable 1: Enable
19	R/W	0x0	POPFREE When this bit is 0, HBIAS MICADC is controlled by register
18	R/W	0x0	Det Mode 0: Jack in pull low 1: Jack in pull high
17	R/W	0x0	AUTOPLEN Enable the function to auto pull low MICDET when jack removal 0: Disable 1: Enable
16	R/W	0x0	MICDETPL When this bit is 1and AUTOPLEN is 0, the MICDET is pull to GND
15	R/W	0x0	HMICBIASEN Headphone Microphone Bias Enable 0: Disable 1: Enable
14:13	R/W	0x1	HBIASSEL HMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.55V
12	R/W	0x1	HMIC BIAS chopper enable 0: Disable

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Offset: 0x0318			Register Name: MICBIAS_REG
Bit	R/W	Default	Description
			1: Enable
11:10	R/W	0x0	HMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1MHz 11: 2MHz
9:8	R/W	0x0	/
7	R/W	0x0	MMICBIASEN Master Microphone Bias Enable 0: Disable 1: Enable
6:5	R/W	0x1	MBIASSEL MMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V
4	R/W	0x1	MMIC BIAS chopper enable 0: Disable 1: Enable
3:2	R/W	0x0	MMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1MHz 11: 2MHz
1:0	R/W	0x0	/

4.1.6.118 0x031C Ramp Control Register (Default Value:0x0018_0000)

Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
31	R/W	0x0	RAMP RISE INT En 0: Enable 1:Disable
30	R/W1C	0x0	RAMP RISE INT RK Increase Upward Finish and Rampen Pull Down Instruction 0: No Pending IRQ 1: Ramp Rise Finish Pending Interrupt Write '1' to clear this interrupt
29	R/W	0x0	RAMP FALL INT EN

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Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
			0: Enable 1:Disable
28	R/W1C	0x0	RAMP FALL INT RK Downward Decrease Finish and Rampen Pull Down Instruction 0: No Pending IRQ 1: Ramp Fall Finish Pending Interrupt Write '1' to clear this interrupt
27:25	/	/	/
24	R/W	0x0	RAMP SOFT RESET 0: Disable 1:Enable
23:21	/	/	/
20:16	R/W	0x18	RAMP_CLK_DIV_M Analog Ramp Clk Div Freq Value: M (from 0 to 31, Default:24). Ana_Ramp_Clk= 24MHz/(M+1) Default Ramp Clk Freq: 24MHz/(24+1)=960 kHz
15	R/W	0x0	HP PULL OUT EN 0: Disable 1:Enable
14:12	R/W	0x0	RAMP HOLD STEP 000: 9600 001: 19200 010: 38400 011: 76800 100: 96000 101: 115200 110: 153600 111: 192000 Ramp Hold Time = Ramp Hold Step/Ramp Clk Freq When Ramp Clk Freq equal to 960 kHz, Corresponding Ramp Hold time of each gear: 000: 9600/960 kHz=10ms 001: 19200/960 kHz=20ms 010: 38400/960 kHz=40ms 011: 76800/960 kHz=80ms 100: 96000/960 kHz=100ms 101: 115200/960 kHz=120ms 110: 153600/960 kHz=160ms

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Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
			111: 192000/960 kHz=200ms
11:10	/	/	/
9:8	R/W	0x0	GAP STEP 00: ramp step 01: ramp step*2 10: ramp step*3 11: ramp step*4
7	/	/	/
6:4	R/W	0x0	RAMP STEP RK Frequency Gear, Control Ramp Rise/Fall Total Time 000: 20 001: 30 010: 40 011: 60 100: 80 101: 120 110: 160 111: 240 Ramp Rise/Fall Total Time = (Ramp Step/Ramp Clk Freq) *4096 When Default Ramp Clk Freq equal to 960 kHz, Corresponding time of each gear: 000: (20/960 kHz) *4096=85.3ms 001: (30/960 kHz) *4096=128ms 010: (40/960 kHz) *4096=170.6ms 011: (60/960 kHz) *4096=256ms 100: (80/960 kHz) *4096=341.3ms 101: (120/960 kHz) *4096=512ms 110: (160/960 kHz) *4096=682.6ms 111: (240/960 kHz)*4096=1024ms
3	R/W	0x0	RMD_EN Ramp Manual Down Enable 0: Disable 1: Enable
2	R/W	0x0	RMU_EN Ramp Manual Up Enable 0: Disable 1: Enable
1	R/W	0x0	RMC_EN Ramp Manual Control Enable

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Offset: 0x031C			Register Name: RAMP_REG
Bit	R/W	Default	Description
			0: Disable, and there is no signal output for DAC. 1: Enable
0	R/W	0x0	RD_EN Ramp Digital Enable 0: Disable 1: Enable

4.1.6.119 0x0320 BIAS Analog Control Register (Default Value:0x0000_0080)

Offset: 0x0320			Register Name: BIAS_REG
Bit	R/W	Default	Description
31:8	R/W	0x0	/
7:0	R/W	0x80	BIASDATA Bias Current Register Setting Data This 8-bit register is not controlled by the AUDIO CODEC reset, only controlled by the system bus reset.

4.1.6.120 0x0324 HEADPHONE Analog Control Register (Default Value:0x8080_0C44)

Offset: 0x0324			Register Name: HP_REG
Bit	R/W	Default	Description
31:24	R/W	0x80	HPRCALIVERIFY Right Headphone calibration Setting Data
23:16	R/W	0x80	HPLCALIVERIFY Left Headphone calibration Setting Data
15	R/W	0x0	HPPA_EN Right & Left Headphone PA Enable 0: Disable; 1: Enable
14:12	R/W	0x0	/
11	R/W	0x1	HPINPUTENABLE When this bit is write to 0, the input stage of headphone disabled
10	R/W	0x1	HPOUTPUTENABLE When this bit is write to 0, the output stage of headphone disabled
9:8	R/W	0x0	HPPA_DEL Headphone delay time when start up 00: 4ms 01: 8ms 10: 16ms

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Offset: 0x0324			Register Name: HP_REG
Bit	R/W	Default	Description
			11: 32ms
7:6	R/W	0x1	CP_CLKS Charge Pump Clock select 00: 250k 01: 330k 10: 660k 11: 1000k
5	R/W	0x0	HPCALIMODE HEADPHONE calibration equilibration MODE select 0: equilibration mode 1: no equilibration
4	R/W	0x0	HPCALIVERIFY HEADPHONE calibration in verify mode enable 0: Disable; 1: Enable
3	R/W	0x0	HPCALIFIRST When this bit is write to 1 , HEADPHONE Calibration once before enable
2:0	R/W	0x4	HPCALICKS HEADPHONE Calibration clock frequency select 000: 4 … 100: 64 … 111: 512

4.1.6.121 0x0328 HMIC Control Register (Default Value: 0x0000_0008)

Offset: 0x0328			Register Name: HMIC_CTRL
Bit	R/W	Default	Description
31:23	/	/	/
22:21	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11 : Down by 8, 16Hz
20:16	R/W	0x0	MDATA_Threshold The threshold of MIC_DET pending When HMIC_M is not set, and the deviation between the current obtained value and the threshold exceeds MDATA_Threshold_Debounce at twice time, the interrupt

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Offset: 0x0328			Register Name: HMIC_CTRL
Bit	R/W	Default	Description
			is pending.
15:14	R/W	0x0	HMIC_SF HMIC Smooth Filter setting The compare value of MIC interrupt is the value after Smooth Filter. 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8
13:10	R/W	0x0	HMIC_M Debounce when the MIC Key down or up. 0000:1 samlpe data 0001:2 samlpe data ... 1111:16 samlpe data
9:6	R/W	0X0	HMIC_N Debounce when earphone plug in or pull out 125ms-2s 0000:125ms 0001:250ms ... 1111:2s
5:3	R/W	0x1	MDATA_Threshold_Debounce 000:0 001:1 010:2 011:3 100:4 101:5 110:6 111:7 11: Reserve (default 1) When a MDATA value is added, if the variation is beyond this threshold, the MIC interrupt will be pending
2	R/W	0x0	JACK_OUT_IRQ_EN MIC Detect Interrupt Set 0: disable 1 : enable
1	R/W	0x0	JACK_IN_IRQ_EN MIC Detect Interrupt Set 0: disable

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Offset: 0x0328			Register Name: HMIC_CTRL
Bit	R/W	Default	Description
			1 : enable
0	R/W	0x0	MIC_DET_IRQ_EN MIC Detect Interrupt Set 0: Disable 1:Enable

4.1.6.122 0x032C HMIC Status Register (Default Value: 0x0000_6000)

Offset: 0x032C			Register Name: HMIC_STS
Bit	R/W	Default	Description
31:15	/	/	/
14:13	R/W	0x3	MDATA_DISCARD After MIC DATA data receiving, the first N-data will be discarded. N defined as follows: 00: 0; None discarded 01: 1; 1-data discarded 10: 2; 2-data discarded 11: 4; 4-data discarded
12:8	R	0x0	HMIC_DATA HMIC Average Data
7:5	/	/	/
4	R/W1C	0x0	JACK_DET_OIRQ Jack output detect Pending interrupt 0: No Pending IRQ 1: Pending IRQ Writing 1 clear pending
3	R/W1C	0x0	JACK_DET_IIRQ Jack input detect pending interrupt 0: No Pending IRQ 1: Pending IRQ Writing 1 clear pending
2:1	/	/	/
0	R/W1C	0x0	MIC_DET_ST. MIC Detect Pending interrupt 0: No pending IRQ 1: Pending IRQ Writing 1 clear pending

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4.1.6.123 0x0348 POWER Analog Control Register (Default Value:0x8800_3711)

Offset: 0x0348			Register Name: POWER_REG
Bit	R/W	Default	Description
31	R/W	0x1	ALDO_EN 0: Disable 1: Enable
30	R/W	0x0	/
29	R/W	0x0	VAR1SPEEDUP_DOWN_Further_CTRL VRA1Speedup Down Further Control in AUDIO CODEC Analog 0: Digital Signal Interface Pin l_vra1speedup (vra1_speedup_down) Normally Control VRA1 Speedup down 1:Manual Control Finish VRA1 Speedup down，Ignore Digital Signal Interface Pin l_vra1speedup (vra1_speedup_down) Control
28	R/W	0x0	/
27	R/W	0x1	LDO for VRP Chopper Enable 0: Disable 1: Enable
26:25	R/W	0x0	LDO for VRP chopper clock select 00: 250 kHz 01: 500 kHz 10: 1MHz 11: 2MHz
24	R/W	0x0	VRP_LDO_EN LDO for VRP Enable Control 0: Disable 1:Enable
23:17	R/W	0x0	/
16	R	0x0	AVCCPOR AVCCPOR Monitor
15	R/W	0x0	BG_BUFFER_DISABLE 0: Enable 1: Disable
14:12	R/W	0x3	ALDO_OUTPUT_VOLTAGE ALDO Output Voltage Control 0: 2.03 V 4: 1.73 V 1: 1.95 V 5: 1.67 V 2: 1.87 V 6: 1.61 V 3: 1.80 V 7: 1.56V When the BG output voltage is 0.9V, the voltages above

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Offset: 0x0348			Register Name: POWER_REG
Bit	R/W	Default	Description
			are the values of this bit. When the BG output voltage is not 0.9V, it is needed to convert the above voltages according to the corresponding ratio to get the actual ALDO ouput voltages.
11:8	R/W	0x7	BG_ROUGH_TRIM BG Output ROUGH Voltage Rough Trimming Every step is 25 mV. The BG output voltage range is from 710 mV to 1085 mV. The default output voltage is 885 mV.
7:0	R/W	0x11	BG_FINE_TRIM BG Output Voltage Fine Trimming Only lower 6-bit is used and every step is 0.5 mV. The BG output voltage range is from 0 to 32.5 mV. The default output voltage is 15 mV. **Note: This register is only controlled by system bus clock and reset.**

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4.2 I2S/PCM

4.2.1 Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format, and TDM mode format.

The I2S/PCM controller includes the following features:

- Four I2S/PCM external interfaces (I2S0, I2S1, I2S2, and I2S3) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- FIFOs for transmitting and receiving data
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width ⩽ 24.576 MHz)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

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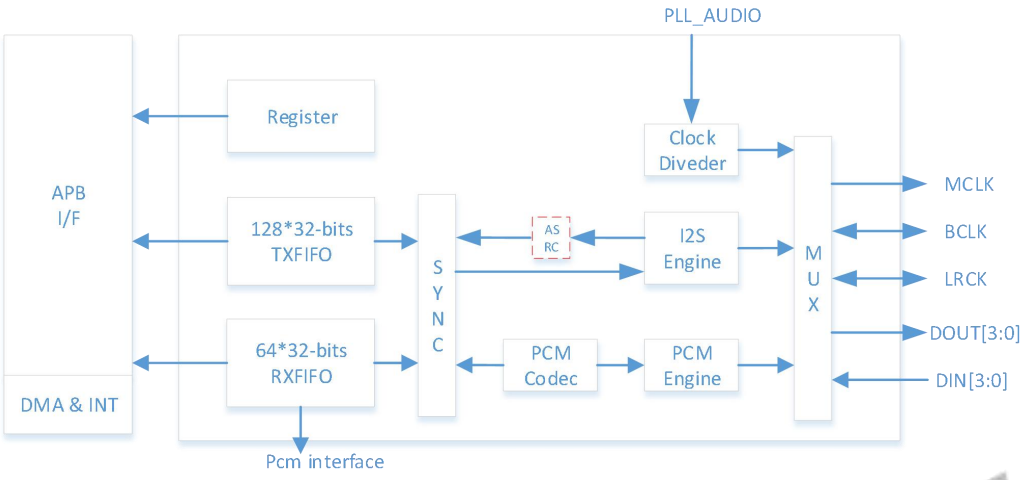
4.2.2 Block Diagram

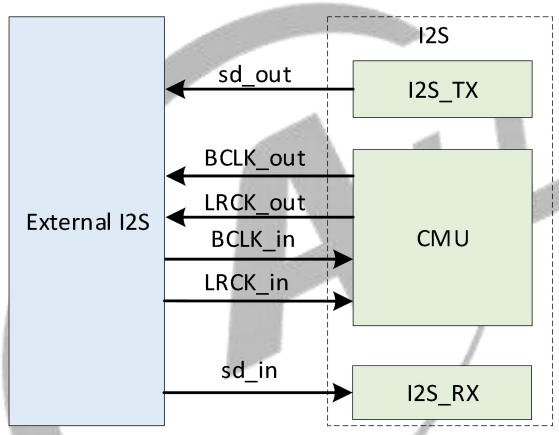
The following figure shows the functional block diagram of the I2S/PCM interface.

Figure 4-14 I2S/PCM Interface System Block Diagram



The following figure shows the typical application of the I2S/PCM interface.

Figure 4-15 Typical Application of I2S/PCM Interface



The I2S/PCM interface system integrates one I2S_TX and one I2S_RX.

- The I2S_TX is for playing music in I2S or PCM format.
- The I2S_RX is for receiving data in I2S or PCM format.
- When the I2S works in the master mode, the external I2S module provides BCLK_in and LRCK_in for the clock management unit (CMU), and the I2S_TX and I2S_RX work with the two external clocks.
- When the I2S works in the slave mode, the CMU provides clocks BCLK_out and LRCK_out for the external I2S module, and the I2S_TX and I2S_RX work with the internal clocks.

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4.2.3 Functional Description

4.2.3.1 External Signals

The following table describes the external signals of the I2S/PCM interface.

LRCK and BCLK are bidirectional I/O. When the I2S/PCM interface works in the Master mode, LRCK and BCLK are output pins. When the I2S/PCM interface works in the Slave mode, LRCK and BCLK are input pins.

MCLK is an output pin for external devices. DOUT are the serial data output pins and DIN are the serial data input pins. For details about General Purpose I/O port, refer to section 8.5 GPIO.

Table 4-2 I2S/PCM External Signals

Signal Name	Description	Type
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[3:0]	I2S0/PCM0 Serial Data Input Channel [3:0]	I
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM01Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S2-DOUT[3:0]	I2S2/PCM2 Serial Data Output Channel [3:0]	O
I2S2-DIN[3:0]	I2S2/PCM2 Serial Data Input Channel [3:0]	I
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S3-DOUT[3:0]	I2S3/PCM3 Serial Data Output Channel [3:0]	O
I2S3-DIN[3:0]	I2S3/PCM3 Serial Data Input Channel [3:0]	I
I2S3-MCLK	I2S3 Master Clock	O
I2S3-LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3-BCLK	I2S3/PCM3 Bit Rate Clock	I/O

4.2.3.2 Clock Sources

The following table describes the clock sources for I2S/PCM. For clock setting, configurations, and gating information, refer to section 2.11 Power Reset Clock Management (PRCM).

Table 4-3 I2S/PCM Clock Sources

Clock Source	Description	Module
PLL_AUODIO(4x)	By default, PLL_AUDIO(4X) is 98.2856 MHz.	CCU

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Clock Source	Description	Module
PLL_AUDIO1 (DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1 (DIV2) is 1536 MHz, and PLL_AUDIO1 (DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1 (DIV5)		

4.2.3.3 Timing Diagram

The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode, and TDM mode. The software can select the modes by setting I2S/PCM_CTL. The following figures describe the waveforms for SYNC, BCLK, DOUT, and DIN in different modes.

Each sampling period contains an LRCK. The low level of LRCK is the left channel corresponding to the even slots, and the high level is the right channel corresponding to the odd slots. Each slot is the sampling point of a mono channel. The sampling period can support the transmission of 2/4/8/16 slots. The BCLK corresponds to the serial data bit.

Figure 4-16 I2S Standard Mode Timing

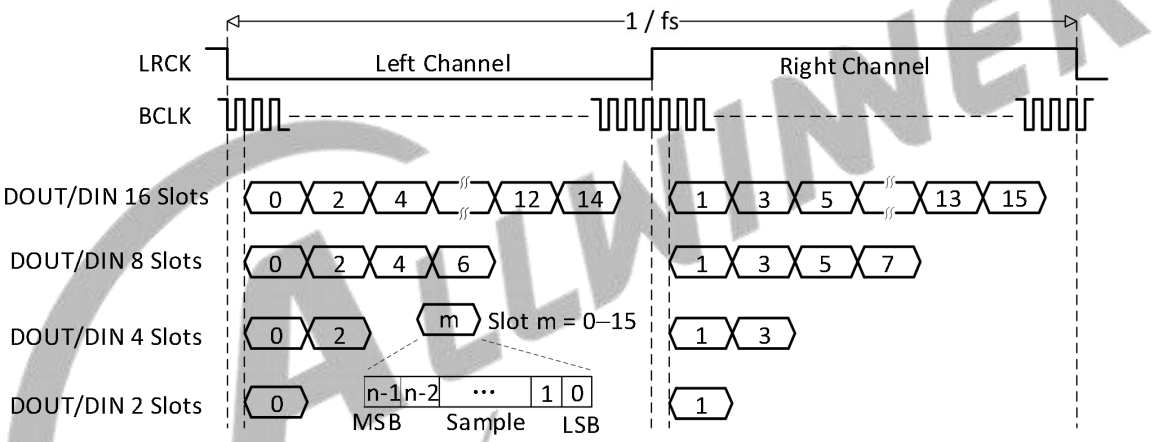

Figure 4-17 Left-Justified Mode Timing

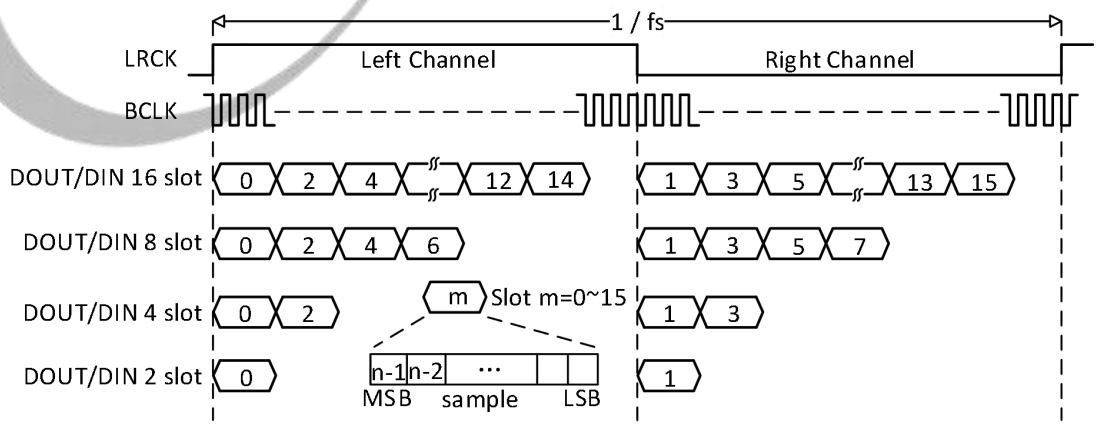

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Figure 4-18 Right-Justified Mode Timing

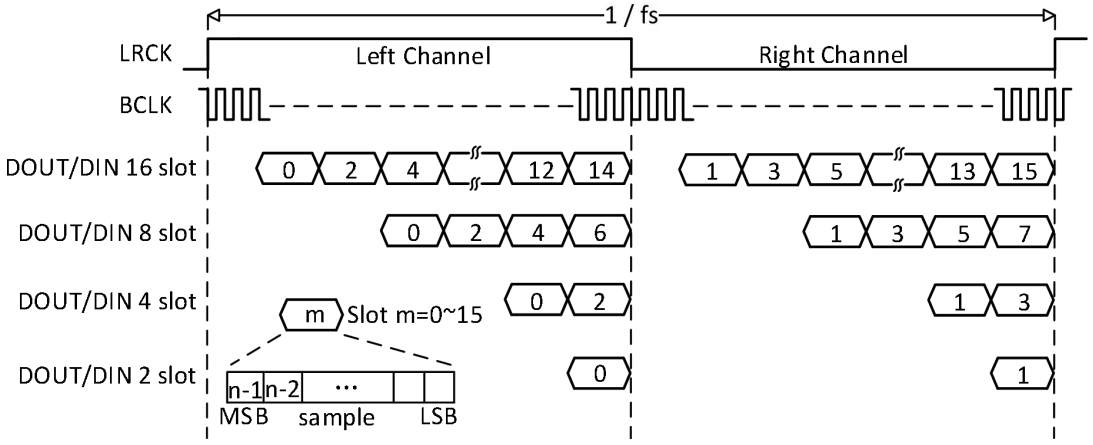


Figure 4-19 PCM Long Frame Mode Timing

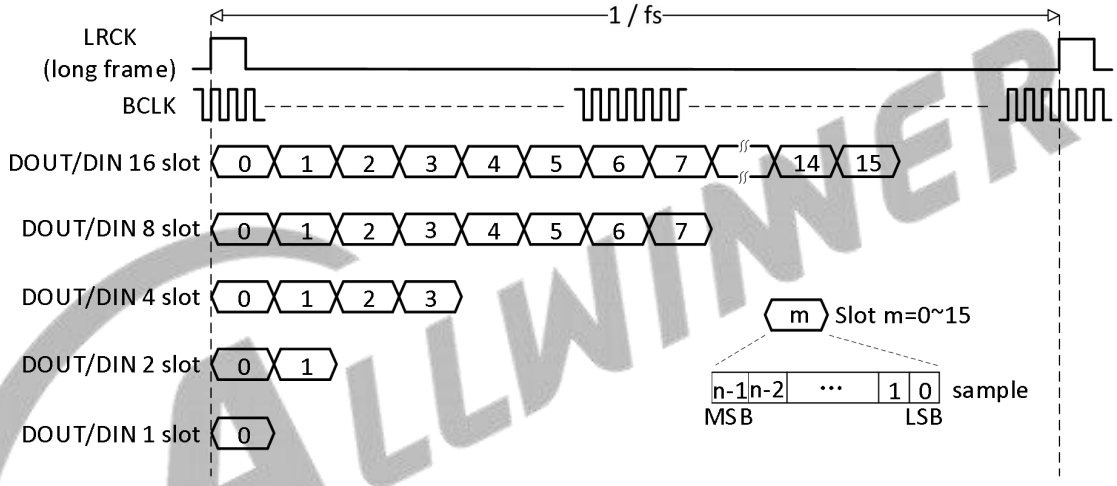
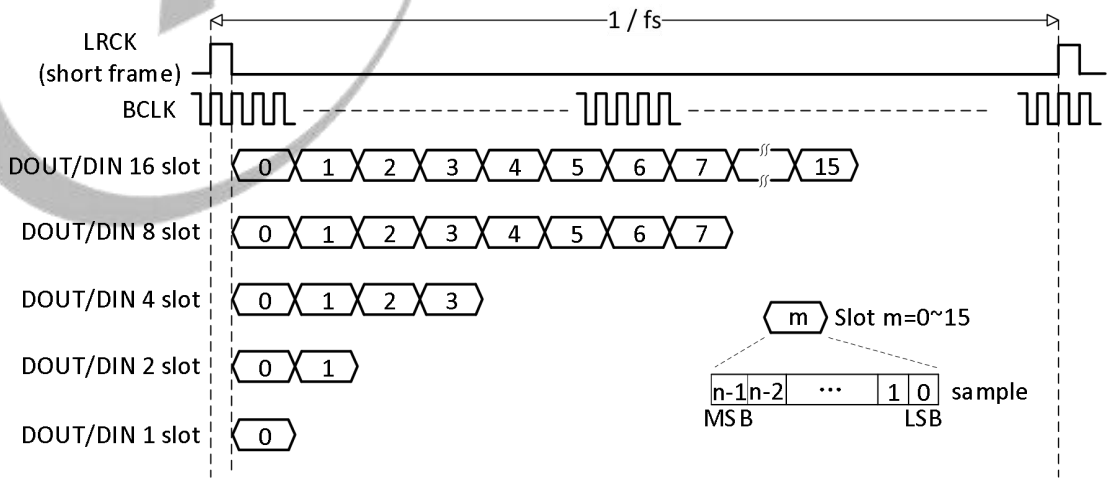


Figure 4-20 PCM Short Frame Mode Timing (one BCLK cycle)



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4.2.3.4 ASRC

The ASRC module supports sampling rate conversion between the up-sampling and down-sampling. The ASRC also supports sampling rate conversion between dual-channel audio data, and the size of the sampling data is up to 24 bits.

The ASRC module has the following features:

- Typical THD + N: -130 dB (Range: -125 dB to -139 dB)
- Supports sampling rate conversion between the up-sampling and down-sampling to implement the sampling rate conversion for stereo data
  - The up-sampling ratio ranges from 1 to 7.5x
  - The down-sampling ratio ranges from 8 to 1x
- Supports sampling rate conversion between two identical frequencies
- Sampling rate for both the input and output range is from 8 kHz to 192 kHz and can be decimal
- Sampling rate can be configured manually or via adaptive generation
- The ASRC input is connected to I2S RX_FIFO_WDATA [31:8], and the input data is 24-bit MSB big-endian. For the input data that is less than 24 bits, use zeros to pad out the values at the low bits instead of high bits
- The ASRC needs some time to calculate the result. The output outsamplea/b will keep 0 during the calculation, and then change to the valid value when the result comes out

Calculating the ASRC Latency

Calculate the ASRC up-sampling and down-sampling latency according to the following formulas.

$$\text{Upsampling Latency} = \text{Phase Delay} + \text{FIFO Delay} = 32 + 16 = 48 \text{ Input Sample Periods}$$

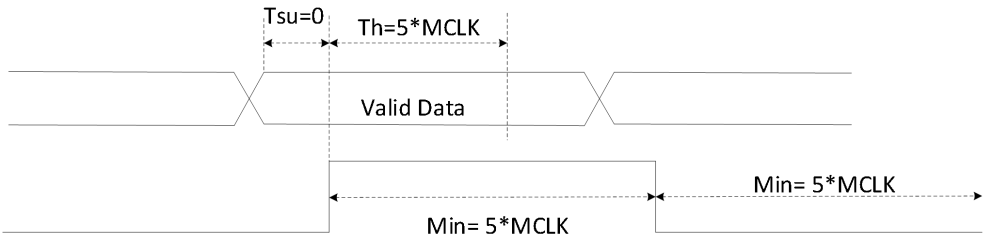
$$\text{Downsampli ng Latency} = \text{Phase Delay} + \text{FIFO Delay} = (32 * f_{sout}/f_{sin}) + 16 \text{ Input Sample Periods}$$

ASRC Timing

The MCLK samples the input clock CLKIN to generate pulse signals.

The following figure shows the timing requirements for the inputs.

Figure 4-21 Timing Requirements for Inputs



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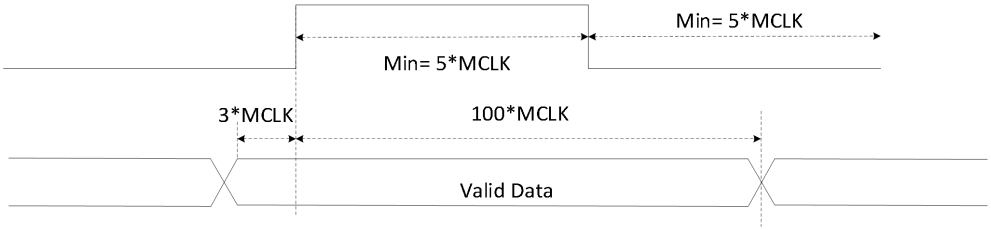
The following figure shows the timing requirements for the outputs.

Figure 4-22 Timing Requirements for Outputs



For the up-sampling, $F_{MCLK} = F_{sout} * 1350$

For the down-sampling, $F_{MCLK} = F_{sin} * 0.30 + F_{sout} * 295$

The following table provides the proper values of MCLK in MHz with different Fsin and Fsout in kHz.

Table 4-4 Proper MCLK Values with Different Fsin and Fsout

Fsin \ Fsout	32	44.1	48	88.2	96	144	192
32	45	60	65	120	130	195	260
44.1	55	60	65	120	130	195	260
48	60	65	65	120	130	195	260
88.2	105	105	110	120	130	195	260
96	110	115	115	125	130	195	260
144	160	165	165	175	180	195	260
192	210	215	215	225	230	245	260

NOTE

The units for Fsin and Fsout are kHz and MCLK is MHz.

4.2.3.5 Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup, and Enable/Disable module.

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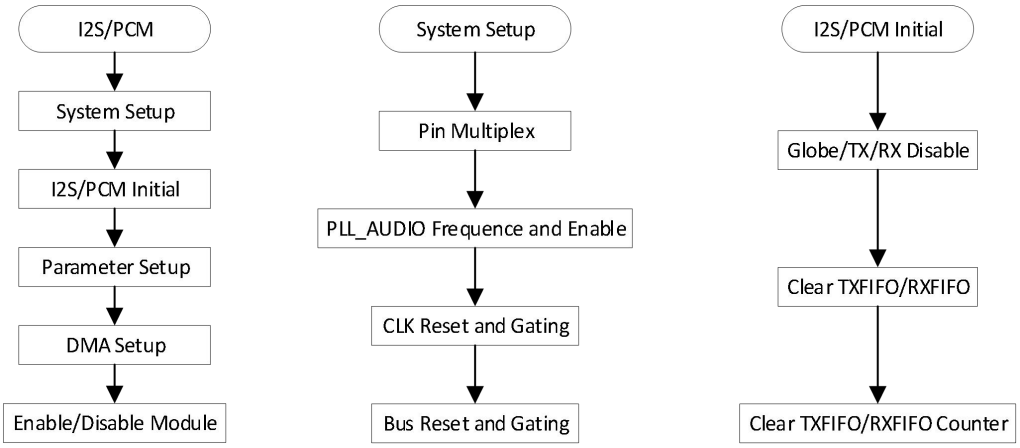
The following figure shows the whole operation flow of I2S/PCM.

Figure 4-23 I2S/PCM Operation Flow



Step 1 System Setup and I2S/PCM Initialization

The clock source for the I2S/PCM should be followed. Firstly, disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE] in the CCU or PRCM. Secondly, set up the frequency of the PLL_AUDIO in the PLL_AUDIOx Control Register. After that, enable the I2S/PCM gating through the I2S/PCMx_CLK_REG when you checkout that the PLL_AUDIOx Control Register[LOCK] becomes to 1. At last, reset and enable the I2S/PCM bus gating by setting I2S_BGR_REG.

After the system setup, the register of I2S/PCM can be setup. Firstly, initialize the I2S/PCM. You should close the Globe Enable bit (I2S/PCM_CTL[0]), Transmitter Block Enable bit (I2S/PCM_CTL[2]), and Receiver Block Enable bit (I2S/PCM_CTL[1]) by writing 0. After that, clear the TX/RX FIFO by writing 0 to the bit[25:24] of I2S/PCM_FCTL. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to I2S/PCM_TXCNT and I2S/PCM_RXCNT.

Step 2 Parameter Setup and DMA Setup

First, you can set up the I2S/PCM of master and slave. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of the slot, the channel slot number, and the trigger level, and so on. The setup of the register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the section 2.6 DMA Controller (DMAC). In this module, you just enable the DRQ.

Step 3 Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing I2S/PCM_CTL[TXEN]/I2S/PCM_CTL[RXEN]. After that, enable I2S/PCM by writing 1 to I2S/PCM_CTL[Globe Enable]. Write 0 to the Globe Enable bit to disable I2S/PCM.

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4.2.4 Programming Guidelines

4.2.4.1 Application Example of Processing ASRC Input and Output Data

The following example shows a typical application of ASRC: the input data is 24-bit valid, and the output data is a 32-bit data whose highest 24 bits are valid output and the lowest eight bits are padded out with zeros.

To implement the application, configure the sample resolution and slot width as 32 bits. Follow the steps below:

Step 1 For the input register: 0x04 [6:4] sample_res = 3`h7, 0x04 [2:0] slot_width = 3`h7.

The format of the input data: 32'hXXXXXXXX, where, bit [31] is the MSB and X is the valid data bit.

Step 2 For the output register: 0x04 [6:4] sample_res = 3`h7, 0x04 [2:0] slot_width = 3`h7

The format of the output data: 32'hXXXXXX00, where, bit [31] is the MSB, X is the valid data bit, and bit [7:0] are the padded zeros.

4.2.4.2 Converting the Sampling Rate with ASRC

Converting a 48 kHz sampling rate to 16 kHz is the most common scenario in actual applications. Follow the steps below to convert the sampling rate from 48 kHz to 16 kHz for the 32-bit data.

Step 1 Configure the PLL_AUDIO Register

a) Configure PLL_AUDIO_CTRL_REG[31:0] as 0x8814AB01. That is, PLL_AUDIO = 24*(171+1)/ (1+1)/ (1+0)/ (1+20) = 98.286 MHz. According to the relationship among the Fsin, Fsout, and MCLK, the MCLK should be greater than 60 MHz. In the simulation phase, the HOSC frequency is 25 MHz, so the output frequency of PLL_AUDIO should be 25*(171+1)/ (1+1)/ (1+0)/ (1+20) = 102.381 MHz. In the IC test phase, configure the frequency of PLL_AUDIO according to its actual output frequency.

b) It is suggested that you configure the ASRC MCLK as an equal-duty-cycle signal. You can specify an odd number for bit[21:16] (PLL_POST_DIV_P) of PLL_AUDIO_CTRL_REG to get an equal-duty-cycle output clock of PLL_AUDIO.

c) Configure bit[25:24] of I2S3_ASRC_CLK_REG as 0x00 to select the PLL_AUDIO(4X).

Step 2 Configure the I2S Registers

a) Configure bit[7:4] (BCLKDIV) of I2S/PCM_CLKD as 4`h9, that is, the frequency of BCLK will be 98.286 MHz/32 = 3.072 MHz.

b) Configure bit[17:8] (LRCK_PERIOD) of I2S/PCM_FMT0 as 10`h1F. That is, the LRCK_PERIOD width is configured as 32 BLCKs and can generate the ASRC CLKIN with a 48 kHz sampling rate. ($\frac{3.072\text{MHz}}{32*2} = 48\text{kHz}$)

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c) Configure bit[6:4] (Sample Resolution bits) of I2S/PCM_FMT0 as 3`h7 to specify the sample resolution as 32-bit.

d) Configure bit[2:0] (Slot Width bits) of I2S/PCM_FMT0 as 3`h7 to specify the slot width as 32-bit.

Step 3 Configure the ASRC Registers

a) Configure bit[16] (clock gate) of MCLKCFG as 1`h1 to open the clock gating.

b) Configure bit[3:0] (division factor) of MCLKCFG as 1`h1 to specify the division factor as 1.

c) Configure bit[20] (clock gate) of FsoutCFG as 1`h1 to open the clock gating.

d) Configure bit[19:16] (clock select) of FsoutCFG as 4`h0 to select I2S0_ASRC_CLK as the clock source.

e) Configure bit[7:4] (the first division factor) of FsoutCFG as 16`h13 to configure the first division factor as 128.

f) Configure bit[3:0] (the second division factor) of FsoutCFG as 16`h10 to configure the second division factor as 48.

g) Configure the ASRC ratio.

To configure the ASRC ratio manually, configure bit[31] (Manual Configuration of ASRC Ratio Enable) of ASRCMANCFG as 1`h1 to enable the manual configuration of ASRC ratio. Configure bit[25:0] of ASRCMANCFG as 26`h155555 to specify the ratio value as 0x155555. The calculation formula for the ratio value: Dec2Hex (Fsout/Fsin) *222). In this example, Fsout/Fsin = 16 kHz/48 kHz =1/3, then the ratio is 0x155555.

To configure the ASRC ratio automatically, configure bit[31] (Manual Configuration of ASRC Ratio Enable) of ASRCMANCFG as 1`h0 to enable the automatic configuration of ASRC ratio. Then the system will automatically calculate the ratio value based on the MCLK, Fsout, and Fsin.

4.2.5 Register List

Module Name	Base Address	Comments
I2S|PCM0	0x07112000	Use for Speech Input.
I2S|PCM1	0x07113000	I2S|PCM1 register is the same with I2S|PCM0 .
I2S|PCM2	0x07114000	I2S|PCM2 register is the same with I2S|PCM0.
I2S|PCM3	0x07115000	I2S|PCM3 register is the same with I2S|PCM0.

Register Name	Offset	Description
I2S|PCM_CTL	0x0000	I2S|PCM Control Register
I2S|PCM_FMT0	0x0004	I2S|PCM Format Register 0
I2S|PCM_FMT1	0x0008	I2S|PCM Format Register 1

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Register Name	Offset	Description
I2S|PCM_ISTA	0x000C	I2S|PCM Interrupt Status Register
I2S|PCM_RXFIFO	0x0010	I2S|PCM RXFIFO Register
I2S|PCM_FCTL	0x0014	I2S|PCM FIFO Control Register
I2S|PCM_FSTA	0x0018	I2S|PCM FIFO Status Register
I2S|PCM_INT	0x001C	I2S|PCM DMA And Interrupt Control Register
I2S|PCM_TXFIFO	0x0020	I2S|PCM TXFIFO Register
I2S|PCM_CLKD	0x0024	I2S|PCM Clock Divide Register
I2S|PCM_TXCNT	0x0028	I2S|PCM TX Sample Counter Register
I2S|PCM_RXCNT	0x002C	I2S|PCM RX Sample Counter Register
I2S|PCM_CHCFG	0x0030	I2S|PCM Channel Configuration Register
I2S|PCM_TX0CHSEL	0x0034	I2S|PCM TX0 Channel Select Register
I2S|PCM_TX1CHSEL	0x0038	I2S|PCM TX1 Channel Select Register
I2S|PCM_TX2CHSEL	0x003C	I2S|PCM TX2 Channel Select Register
I2S|PCM_TX3CHSEL	0x0040	I2S|PCM TX3 Channel Select Register
I2S|PCM_TX0CHMAP0	0x0044	I2S|PCM TX0 Channel Mapping Register0
I2S|PCM_TX0CHMAP1	0x0048	I2S|PCM TX0 Channel Mapping Register1
I2S|PCM_TX1CHMAP0	0x004C	I2S|PCM TX1 Channel Mapping Register0
I2S|PCM_TX1CHMAP1	0x0050	I2S|PCM TX1 Channel Mapping Register1
I2S|PCM_TX2CHMAP0	0x0054	I2S|PCM TX2 Channel Mapping Register0
I2S|PCM_TX2CHMAP1	0x0058	I2S|PCM TX2 Channel Mapping Register1
I2S|PCM_TX3CHMAP0	0x005C	I2S|PCM TX3 Channel Mapping Register0
I2S|PCM_TX3CHMAP1	0x0060	I2S|PCM TX3 Channel Mapping Register1
I2S|PCM_RXCHSEL	0x0064	I2S|PCM RX Channel Select Register
I2S|PCM_RXCHMAP0	0x0068	I2S|PCM RX Channel Mapping Register0
I2S|PCM_RXCHMAP1	0x006C	I2S|PCM RX Channel Mapping Register1
I2S|PCM_RXCHMAP2	0x0070	I2S|PCM RX Channel Mapping Register2
I2S|PCM_RXCHMAP3	0x0074	I2S|PCM RX Channel Mapping Register3
MCLKCFG	0x0080	I2S|PCM ASRC MCLK Configure Register
FsoutCFG	0x0084	I2S|PCM ASRC Out Sample Configure Register
FsinEXTCFG	0x0088	I2S|PCM In Sample Pluse Extend Configure Register
ASRCEN	0x008C	I2S|PCM ASRC Enable Configure Register
ASRCMANCFG	0x0090	I2S|PCM ASRC Manual Configure Register
ASRCRATIOSTAT	0x0094	I2S|PCM ASRC Ratio State Configure Register
ASRCFIFOSTAT	0x0098	I2S|PCM ASRC FIFO State Configure Register
ASRCMBISTCFG	0x009C	I2S|PCM ASRC MBIST Test Configure Register
ASRCMBISTSTA	0x00A0	I2S|PCM ASRC MBIST Test State Configure Register

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