V851S

Intelligent Professional IP Camera SoC

Overview

V851S is a new generation of high-performance H.264/H.265 encoding SoC targeted for the field of IP Camera. It integrates the single Cortex-A7 core@900MHz, RISC-V@600MHz and 0.5 Tops NPU and supports various intelligent application such as human detection and crossing alarm. V851S is also designed with a new generation of high-performance ISP image processor and video encoder with professional encoding quality, low encoding bit rate and mainstream-level image processing capability. In addition, V851S supports 64MB DDR2 and rich peripheral interfaces, such as USB, SDIO, and Ethernet, to meet the requirements of various IP Camera products.

Features

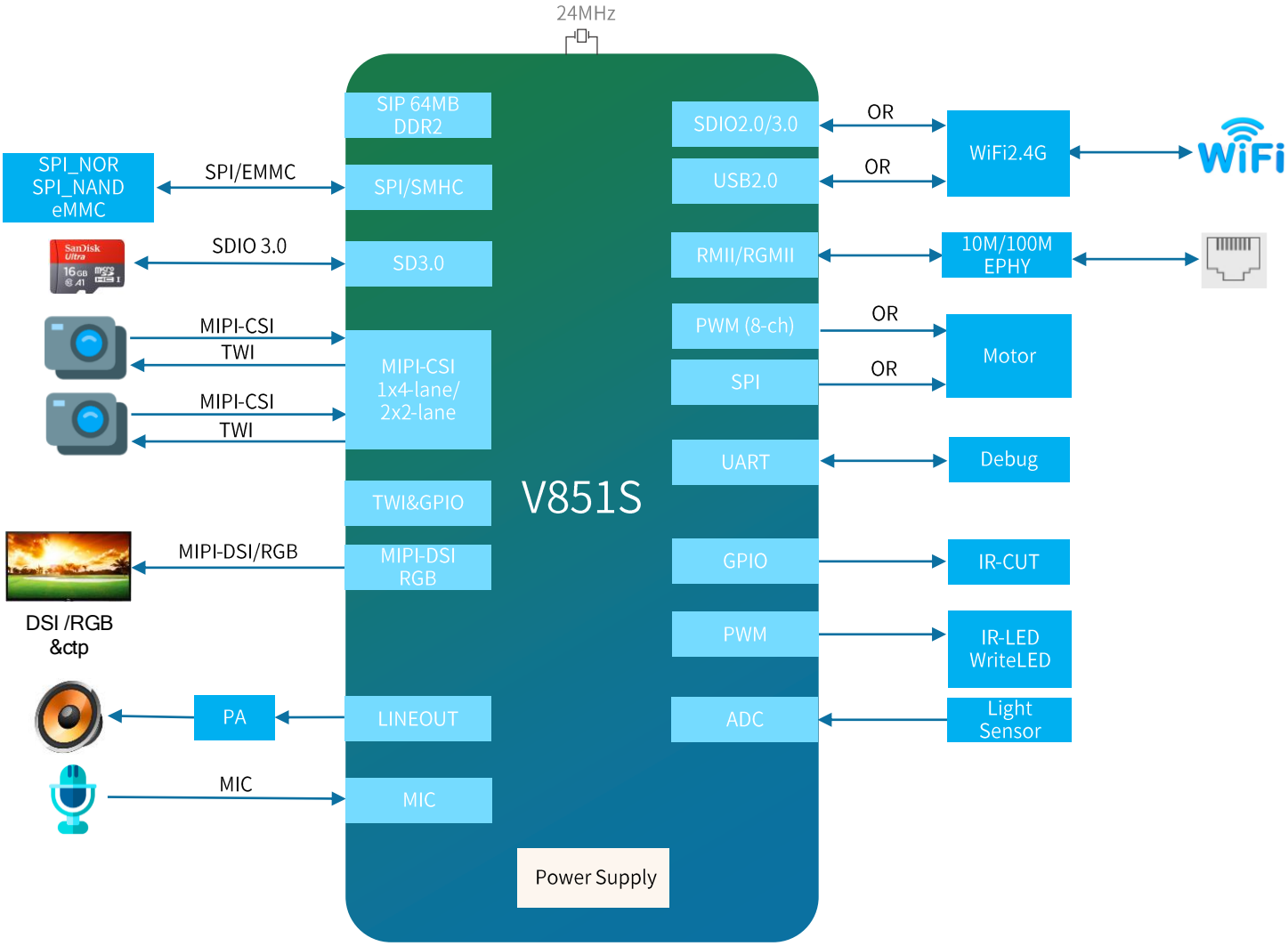
CPU	• Cortex-A7@900MHz CPU core, supporting 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache • RISC-V@600 MHz core, supporting 16 KB I-cache and 16 KB D-cache
NPU	• Maximum performance up to 0.5 Tops • Embedded 128KB internal buffer • Supports deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, and so on
Memory	• SIP 64 MB DDR2 • SD3.0/eMMC 4.5 interface • SPI Nor/SPI Nand Flash
Video Engine	Video encoder • H.264/H.265 up to or 4M@30fps • JPEG up to 1080p@60fps Video decoder • Supports H.264 BP/MP/HP, JPEG • Real-time multiple streams H.264 encoding capability: 4M@30fps • JPEG snapshot performance of 1080p@60fps independently
Display Engine	• Allwinner SmartColor post processing for an excellent display experience • Supports 2 video channels and 1 UI channel • Supports G2D hardware accelerator including rotate, mixer, and scaler functions
Audio	• 1 DAC and 1 ADCs • Analog audio interfaces: MICIN1P/N, LINEOUTP • Digital audio interfaces: I2S/PCM x 1, DMIC x 1

Features

Video OUT	• RGB LCD output interface up to 320 x 240@60fps • 1*2-lane MIPI DSI interface up to 1280x720@60fps
Video Input	ISP • Maximum performance of 4M@30fps and maximum resolution of 2560x1440 • Supports 3A (AE, AWB, and AF), 3DNR, and 2F-WDR. 3A parameters are adjustable. • Provides ISP tuning tools for the PC • Supports Lens Distortion Correction (LDC) and Fish Eye Correction (FEC) VIPP • Four VIPP YUV422 or YUV420 outputs • Maximum performance of 4M@30fps and maximum resolution of 2560x1440 10-bit parallel CSI interface • Maximum video capture resolution up to 4M@30fps 1*4-lane MIPI CSI interface • Supports DOL WDR mode and splitting into 2*2-lane MIPI CSI • Supports 4-ch VC de-interleaver function • Maximum video capture resolution up to 4M@30fps
Security System	• AES, DES, 3DES encryption and decryption algorithms • RSA/ECC signature verification algorithm • MD5/SHA and HMAC tamper proofing • PRNG/TRNG hardware random number generator • Integrated 2 Kbits OTP storage space
Connectivity	• USB2.0 DRD, SDIO 3.0, SPI x 4, UART x 4, TWI x 5, WIEGAND IN • PWM (11-ch), GPADC (1-ch) • 10/100 M EMAC with RMII interfaces
Package	• QFN88, 9 mm x 9 mm body size, 0.35 mm ball pitch

Block Diagram

Application Diagram



ABOUT ALLWINNER

Allwinner Technology, founded in 2007, is a outstanding designer dedicated to intelligent application SoC, high performance analog component and wireless connectivity IC. It is headquartered in Zhuhai China, with other R&D centers and offices in Shenzhen, HongKong, Xi'an, Beijing and Shanghai. Listed on the GEM of the Shenzhen Stock Exchange in 2015, with the stock code 300458.

Motivated by customer-oriented strategy, Allwinner aligns remarkable R&D teams with long-term core-technology investment in UHD video processing, high-performance multi-core CPU/GPU integration with AI and advanced manufacturing process in terms of high integration , ultra-low power consumption and full-stack integration platform, providing competitive turnkey solutions with considerate services. The products powered by Allwinner spread across from smart hardware, smart home, consumer electronics, HD media, smart video, connected car, industry control, wireless communication to analog products.

CONTACT US

Email: service@allwinnertech.com