AXP2585 Single Cell NVDC BMU with E-gauge

1. Features

- 3.9V–5.5 Input Operating Range and Support single Cell Battery
- Battery charge and discharge coulomb counter & E-gauge 2.x
- Support TWSI(Two Wire Serial Interface) and RSB(Reduced Serial Bus)
- High efficiency 3A, 1uH inductor buck mode switch charger
- Boost mode operation with adjustable output from 4.5V to 5.5V, and with current limit
- Integrated control to switch between charge and boost mode
- Single input to support USB input
- Resistance compensation(IRCOMP) from charger output to cell terminal
- High battery discharge efficiency with 11mohm battery discharge MOSFET up to 6A
- BATFET control to support shipping mode, wake up and full system reset
- Flexible autonomous and TWSI mode for optimal system performance
- High integration includes all MOSFETS, current sensing and loop compensation
- Support BC1.2 and CC logic
- Protection
  - Input Over-Voltage Protection
  - Battery Thermistor Sense Hot/Cold Charge Suspend
  - Programmable Safety Timer for Charger
  - Die Thermal Balance for Charger
  - Thermal Shutdown

2. Applications

- Portable devices
- Wireless bluetooth speaker

3. Description

AXP2585 is a highly integrated BMU with NVDC power path management and E-gauge for single cell Li-battery. AXP2585 can be used with other PMU together to provide an easy and flexible power management solution for SOC. AXP2585 also can be used independently to provide battery management solutions for various portable devices

AXP2585 supports high output current up to 3A for fast charging. Besides, AXP2585 supports OTG mode with current limit. To ensure the security and stability of the system, AXP2585 provides multiple channels 12-bit ADC for voltage/current/temperature monitor and integrates protection circuits such as over-voltage protection(OVP), over-current protection(OCP) and over-temperature protection(OTP). Moreover, AXP2585 features a unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

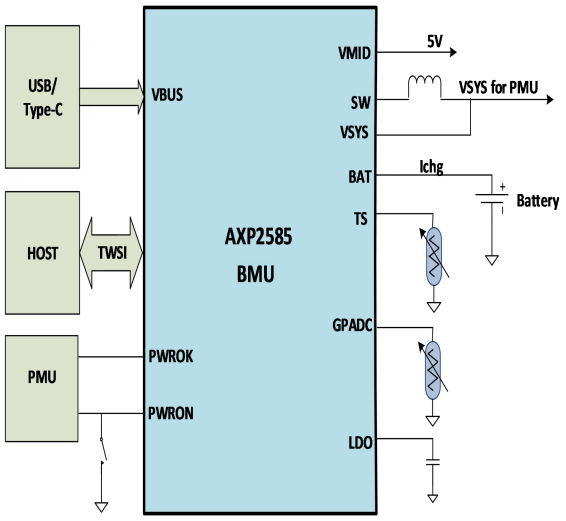
AXP2585 supports type-C cc logic and BC1.2 protocol. It can automatically detect different adapters and adjust the input current limit.

AXP2585 supports TWSI and RSB for system to dynamically adjust output voltages, charge current and configurate interrupt condition.

Device Information

Part Number	Package	Body Size
AXP2585	QFN-32	5mm * 5mm

Simplified Application Diagram

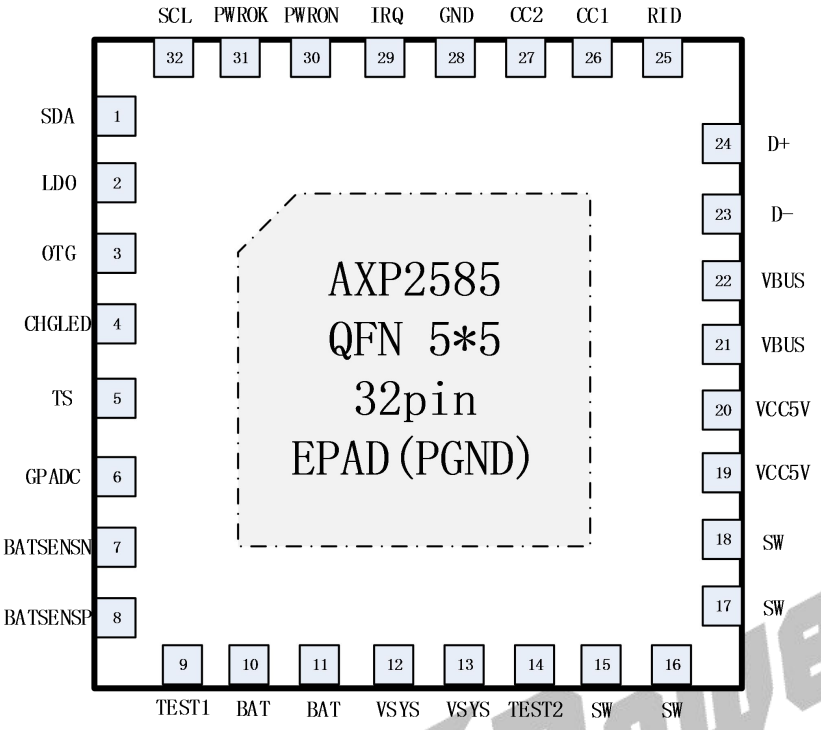


4. Revision History

Revision	Date	Description
V 1.0	May 10,2018	Initial version
V 1.1	Aug.7,2018	1. Add ESD Ratings, Recommended Operating Conditions, Thermal Information, Application Information , PCB Layout Guideline, Storage and Baking.
V 1.2	Mar.18,2019	1. Update Electrical Characteristics and Register.

Contents

5. Pin Configuration and Functions



Pin Description

Pin		I/O[1]	Description
NO.	Name		
1	SDA	DIO	Data pin for serial interface. Connect SDA to the logic rail through a 4.7kΩ resistor.
2	LDO	PO	LDO output. It is used to provide power for RTC and so on. Voltage can be customized as 1.8V,2.5V,2.8V and 3.3V.
3	OTG	DI	Active high enable pin during boost mode. The boost mode is activated when BOOST_EN =1 and OTG pin is high.
4	CHGLED	DO	Charge status output to indicate various charger operation.
5	TS	AI	Temperature qualification voltage input. Connect a negative temperature coefficient thermistor from TS to GND. A current source is injected to TS pin and convert TS voltage to a digital code. Charging suspends when TS pin is out of range. Besides, TS can be connected to external input signal. Refer to REG81H.
6	GPADC	AI	General purpose ADC input. A current source is injected to GPADC pin and convert voltage to a digital code. If not used, it can be floating.

7	BATSENSN	AI	Current sense input. It is connected to one terminal of 10mohm current sense resistor and battery.
8	BATSENSP	AI	Current sense input. It is connected to the other terminal of 10mohm current sense resistor and BAT pin.
9,14	TEST	/	Test pin.Be connected to GND.
10,11	BAT	P	Battery connection point. The internal BATFET is connected between BAT and SYS. Connect a 10uF capacitor closely to the BAT pin.
12,13	VSYS	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. Connect two 22uF capacitors closely to the SYS pin.
15,16,17,18	SW	P	Switching node connecting to output inductor.
19,20	VCC5V	P	Boost mode output.
21,22	VBUS	P	Charger Input.
23	D-	DIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2
24	D+	DIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2
25	RID	DI	The ID pin of USB port.
26	CC1	DIO	Type-C connector configuration channel pin.
27	CC2	DIO	Type-C connector configuration channel pin.
28	GND	G	Analog ground for interrupt analog and digital circuits.
29	IRQ	DIO	Open-drain interrupt Output. Connect the IRQ to a logic rail via a 4.7kΩ resistor. The IRQ pin sends a low level signal to host to report charger device status and fault.
30	PWRON	DIO	BATFET enable/BMU reset control input. Connect a key between PWRON and GND. The pin contains an interrupt pull-up to maintain default high logic.
31	PWROK	DI	Used for system power ON/OFF management. It can be connected to PWROK pin of PMU or directly pulled up to above 1.8V.
32	SCL	DI	Clock pin for serial interface. Connect SCL to the logic rail through a 4.7kΩ resistor.
EP	EP	G	Exposed PAD. Be connected to the power ground.

(1)**O** for output, **I** for input, **IO** for input/output, **D** for digital, **A** for analog, **P** for power, and **G** for ground.

6. Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range(unless otherwise noted)

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBUS	Voltage range(with respect to GND)	-0.3	12	V
VCC5V,BAT,VSYS		-0.3	7	V
SW,SDA,SCL,IRQ,OTG,LDO, TS,GPADC,PWRON,PWROK, D+,D-,RID,CC1,CC2,CHGLED, BATSENSN,BATSENSP		-0.3	7	V
PGND to GND		-0.3	0.3	V
Ta	Operating Temperature Range	-40	85	℃
T_J	Junction Temperature Range	-40	125	℃
Ts	Storage Temperature Range	-65	150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)		300	℃

(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model(HBM)(1)	±4000	V
	Charged device model(CDM)(2)	±750	V

(1) Reference:ESDA/JEDEC JS-001-2014. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) Reference:ESDA/JEDEC JS-002-2014. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
V_{IN}	Input voltage(VBUS)	3.9	5.5	V
I_{IN}	Input current(VBUS)		3.25	A
I_{SYS}	Output current		3	A
V_{BAT}	Battery voltage		4.608	V
I_{BAT}	Fast charging current		3	A

6.4 Thermal Information

Thermal Metric(1)		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	20.1	℃/W
θ_{JB}	Junction-to-board thermal resistance	10.8	

θ_{JC}	Junction-to-case(top) thermal resistance	22.8	

(1)Thermal metrics are calculated refer to JEDEC document JESD51.

6.5 Electrical Characteristics

V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} > V_{SLEEP}, T_J = –40°C to 125°C and T_J = 25°C for typical values (unless otherwise noted)

Parameters		Test Conditions	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.2V, VBUS =0V, leakage between BAT and VBUS			5	uA
		no VBUS, BATFET Disabled, Battery detection Disabled, T_j<85°C		35		uA
		no VBUS, BATFET Enabled, Battery detection Disabled, T_j<85°C		85		uA
I_{VBUS}	Input supply current (VBUS) in buck mode	VBUS = 5V, BAT = 3.8V, converter switching, BATFET Disabled, I_{SYS} = 0A		1.2		mA
I_{BOOST}	Battery discharge current in boost mode	V_{BAT}=4.2V, boost mode, I_{VBUS}= 0A, converter switching		1		mA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		5.5	V
V_{VBUS_UVLOZ}	VBUS for active TWSI, no battery		3.4	3.8	4.1	V
V_{SLEEP}	Sleep mode falling threshold		75	85	90	mV
V_{SLEEPZ}	Sleep mode rising threshold		220	251	273	mV
V_{ACOV}	VBUS over-voltage rising threshold		6.3	6.4	6.5	V
V_{ACOV}	VBUS over-voltage falling threshold		180	189	207	mV
V_{BAT_UVLOZ}	Battery for active TWSI, no VBUS		2.2	2.5	2.7	V
V_{BAT_DPL}	Battery depletion falling threshold		2.0	2.3	2.5	V
V_{BAT_DPLZ}	Battery depletion rising threshold		2.1	2.5	2.7	V
$V_{VBUSMIN}$	Bad adapter detection threshold		3.7	3.7	3.8	V
I_{BADBUS}	Bad adapter detection current source		20	30	44	mA
T_{BADSRC}	Bad adapter detection current source pull down duration			28		ms
POWER-PATH MANAGEMENT						
V_{SYS}	Typical system regulation	Isys = 0A, V_{BAT}> V_{SYS_MIN}, BATFET Disabled		V_{BAT}+		V

	voltage			50mV		
		Isys= 0A, V_{BAT}<V_{SYS_MIN}, BATFET Disabled		Vsys_min +150mV		V
V_{SYS_min}	Minimum DC System Voltage Output	V_{BAT}< V_{SYS_MIN}, V_{SYS_MIN} = 3.5V, I_{SYS}= 0A		3.65		V
V_{SYS_max}	Maximum DC System Voltage Output	V_{BAT}=4.25V, V_{SYS_MIN} = 3.5V, I_{SYS}= 0A		4.3		V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET(RBFET) on-resistance between VBUS and VMID	TJ = -40°C - 85°C		60.2		mΩ
		TJ = -40°C - 125°C		60.2		mΩ
$R_{ON(HSFET)}$	Top switching MOSFET (HSFET) on-resistance between VMID and SW	TJ = -40°C - 85°C	25	36	40	mΩ
		TJ = -40°C - 125°C	25	36	42	mΩ
$R_{ON(LSFET)}$	Bottom switching MOSFET (LSFET) on-resistance between SW and GND	TJ = -40°C - 85°C	20	36	41	mΩ
		TJ = -40°C - 125°C	20	36	46	mΩ
V_{FWD}	BATFET forward voltage in supplement mode	BATFET forward voltage in supplement mode		22		mV
V_{BATGD}	Battery good comparator falling threshold	V_{BAT} falling	3.7	3.8	3.8	V
V_{BATGD_HYST}	Battery good comparator rising threshold	V_{BAT} rising	3.8	3.9	4	mV
Battery Charger						
V_{BATREG_RANGE}	Typical Charge voltage range		3.84		4.608	V
V_{BATREG_STEP}	Typical charge voltage step			16		mV
V_{BATREG}	Charge voltage resolution accuracy	V_{BAT} = 4.208V (REG8C[7:2]=010111) or V_{BAT} = 4.352V (REG8C[7:2]=100000) TJ = -40°C - 85°C	-0.5%		0.5%	
$I_{CHG\_REG\_RANGE}$	Typical Fast charge current regulation range		0		3072	mA
$I_{CHG\_REG\_STEP}$	Typical Fast charge current regulation step			64		mA
$I_{CHG\_REG\_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.1V or 3.8V, I_{CHG}=256mA,TJ = -40°C-85°C	-40%		40%	
		V_{BAT} = 3.1V or 3.8V, I_{CHG}=1792mA,TJ = -40°C-85°C	-10%		10%	
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, BATLOWV(REG06[1])=1	2.5	2.8	3.1	V
	Battery LOWV rising threshold	Precharge to fast charge, BATLOWV(REG8C[1])=1 (Typical 200-mV hysteresis)	2.7	3.0	3.3	V
I_{PRECHG_RANGE}	Precharge current range		64		1024	mA
I_{PRECHG_STEP}	Typical precharge current step			64		mA
I_{PRECHG_ACC}	Precharge current accuracy	V_{BAT}=2.6V, I_{PRECHG} = 256mA	-40%		40%	
I_{TERM_RANGE}	Termination current range		64		1024	mA
I_{TERM_STEP}	Typical Termination current			64		mA

	step					
I_{TERM_ACC}	Termination current accuracy	I_{TERM} = 128mA	-40%		40%	
V_{SHORT}	Battery short voltage	V_{BAT} falling		2		V
I_{SHORT}	Battery short current	V_{BAT} < 2.2 V		10		mA
V_{RECHG}	Recharge Threshold below VBATREG	V_{BAT} falling, V_{RECHG} (REG8C[0]=0) = 0		138		mV
		V_{BAT} falling, V_{RECHG} (REG8C[0]=1) = 1		234		mV
FSW	PWM Switching Frequency, and digital clock	Oscillator frequency	1.2	1.5	1.87	MHz
$I_{BATLOAD}$	Battery Discharge Load Current	V_{BAT} = 4.2V	3			mA
I_{PFM}	PWM TO PFM transition threshold			416		mA
$R_{ON(BATFET)}$	SYS-BAT MOSFET (BATFET) on-resistance	TJ = 25°C		18		mΩ
		TJ = -40°C - 125°C		18		mΩ
Input Voltage / Current Regulation						
V_{INDPM_RANGE}	Typical Input voltage regulation range		3.88		5.08	V
V_{INDPM_STEP}	Typical Input voltage regulation step			80		mV
V_{INDPM_ACC}	Input voltage regulation accuracy		-4%		4%	
I_{INDPM_RANGE}	Typical Input current regulation range		100		3250	mA
I_{INDPM_STEP}	Typical Input current regulation step			50		mA
I_{INDPM_ACC}	Input current regulation accuracy V_{BAT} = 5V, current pulled from SW	USB500, I_{INLIM} =500mA	400		500	mA
		USB900, I_{INLIM} =900mA	750		900	mA
		Adapter 1.5A, I_{INLIM} =1500mA	1300		1500	mA
I_{IN_START}	Input Current regulation during system start up	V_{SYS} = 2.2V, I_{INLIM} (REG10[5:0])>=200mA		200		mA
D+/D- DETECTION						
V_{0P6_VSRC}	D+/D- voltage source (0.6V)		0.5	0.6	0.7	V
I_{10UA_ISRC}	D+ connection check current source		7	10	14	uA
I_{100UA_ISINK}	D+/D- current sink (100μA)		50	100	150	uA
I_{DPDM_LKG}	D+/D- Leakage current	D–, switch open	-1		1	uA
		D+, switch open	-1		1	uA
V_{0P4_VTH}	D+/D- low comparator threshold		250		400	mV
V_{0P8_VTH}	D+ low comparator threshold				0.8	V
R_{D-_DWN}	D– pulldown for connection check		14.25		24.8	kΩ

BAT OVER-VOLTAGE/CURRENT PROTECTION						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104%* V_{BAT_REG}		V
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	REG18[7:6] = 10		100		°C
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature rising	135	140	146	°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis	Temperature falling		20		°C
Boost Mode Operation						
$V_{BST\_REG\_RANGE}$	Typical Boost mode regulation voltage range		4.58		5.48	V
$V_{BST\_REG\_STEP}$	Typical Boost Mode Regulation voltage step			60		mV
$V_{BST\_REG\_ACC}$	Boost mode regulation voltage accuracy	$I_{(VMID)}$ = 0A, V_{BST}=5.126V (REG13[7:4] = 1001)	-3%		3%	
$V_{BST\_BAT\_LOWV}$	Battery voltage exiting boost mode	BAT falling	2.5	2.8	3.0	V
I_{BST}	Boost mode output current range				1.5	A
V_{BST_OVP}	Boost mode over-voltage threshold	Rising threshold	5.9	6	6.0	V
$V_{BST\_OVP\_HYS}$	Boost mode over-voltage threshold hysteresis	Falling threshold	185	215	240	mV
V_{BST_OCP}	Boost mode over-current threshold	Rising threshold	2.1	2.5	3.1	A
FSW	PWM Switching Frequency, and digital clock	Oscillator frequency	1.2	1.5	1.87	MHz
D_{MAX}	Maximum PWM Duty Cycle					
Analog-to-Digital Converter (ADC)						
RES	Resolution	Rising threshold		12		bits
V_{BAT_RANGE}	Typical battery voltage range	V_{VBUS} > V_{BAT} + V_{SLEEP} or boost mode is enabled			4.914	V
		V_{VBUS} < V_{BAT} + V_{SLEEP} and boost mode is disabled			4.914	V
V_{BAT_RES}	Typical battery voltage resolution			1.2		mV
I_{BAT_RANGE}	Typical battery charge current range	V_{VBUS} > V_{BAT} + V_{SLEEP} and V_{BAT} > $V_{BATSHORT}$			4.08	A
I_{BAT_RES}	Typical battery charge current resolution			1		mA
T_{jRANGE}	Typical IC Tj range		-267.7		167.4	℃
T_{jRES}	Typical IC Tj resolution			0.10625		℃

V_{GPADC_RANGE}	Typical GPADC voltage range			3.276		V
V_{GPADC_RES}	Typical GPADC voltage resolution			0.8		mV
V_{TS_RANGE}	Typical TS voltage range			3.276		V
V_{TS_RES}	Typical TS voltage resolution			0.8		mV
Logic I/O pin Characteristics (OTG/IRQ/PWRON/PWROK)						
V_{IH}	Input high threshold level			1.3		V
V_{IL}	Input low threshold level			0.8		V
I_{IN_BIAS}	High Level Leakage Current	Pull-up rail 1.8V		1		uA
TWSI INTERFACE (SCL, SDA)						
V_{CC}	Input Supply Voltage			3.3		V
ADDRESS	TWSI Slave Address (7 bits)			0x34		
f_{SCK}	Clock Operating Frequency			400		kHZ
t_f	Clock Data Fall Time	2.2Kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2Kohm Pull High		100		ns
V_{IH}	Input high threshold level, SCL and SDA	Pull-up rail 1.8V		1.3		V
V_{IL}	Input low threshold level	Pull-up rail 1.8V		0.8		V
V_{OL}	Output low threshold level	Sink Current = 5mA, sink current		0.8		V
I_{BIAS}	High Level Leakage Current	Pull-up rail 1.8V		1		uA
RSB						
ADDRESS	Slave Address			0x01D1		

6.6 Typical Characteristics

Table 6-1 Typical Characteristics

BUCK Efficiency VS System Load Current	Figure 6-1
Charger Efficiency VS Charger Current	Figure 6-2
BOOST Mode Efficiency VS VMID Load Current	Figure 6-3

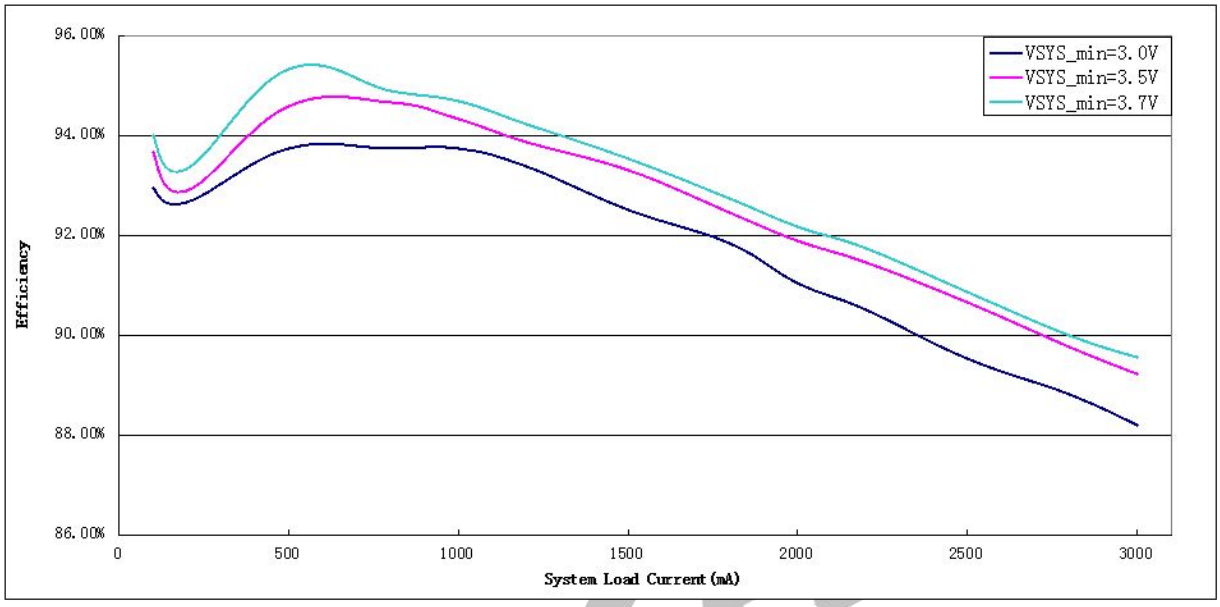


Figure 6-1.BUCK Efficiency VS System Load Current （VBUS=5V）

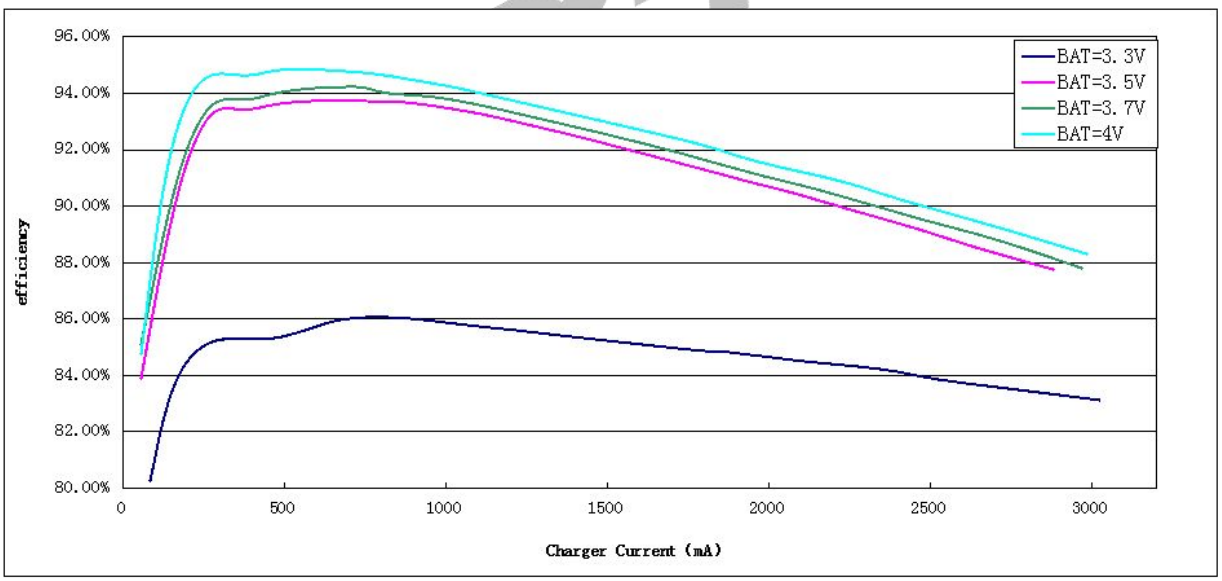


Figure 6-2.Charger Efficiency VS Charger Current （VBUS=5V）

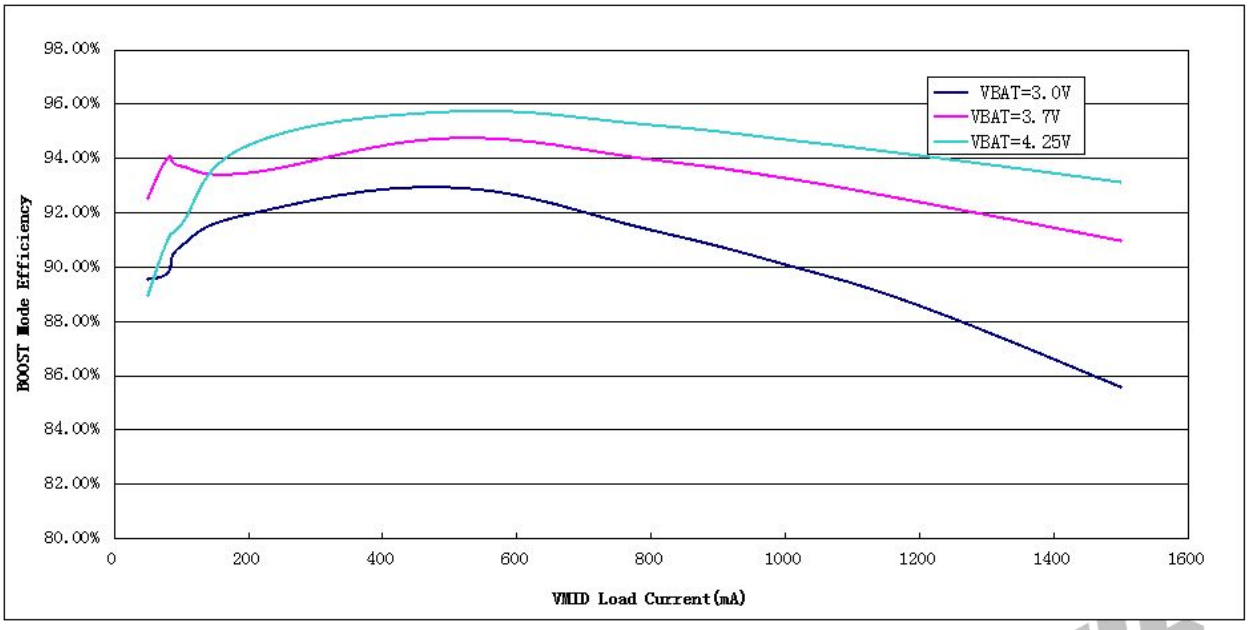


Figure 6-3. BOOST Mode Efficiency VS VMID Load Current （VMID=5V）

7. Detail Description

7.1 Overview

AXP2585 is a highly integrated BMU with NVDC power path management and E-gauge for single cell Li-battery. AXP2585 can be used with other PMU together to provide an easy and flexible power management solution for SOC. AXP2585 also can be used independently to provide battery management solutions for various portable devices

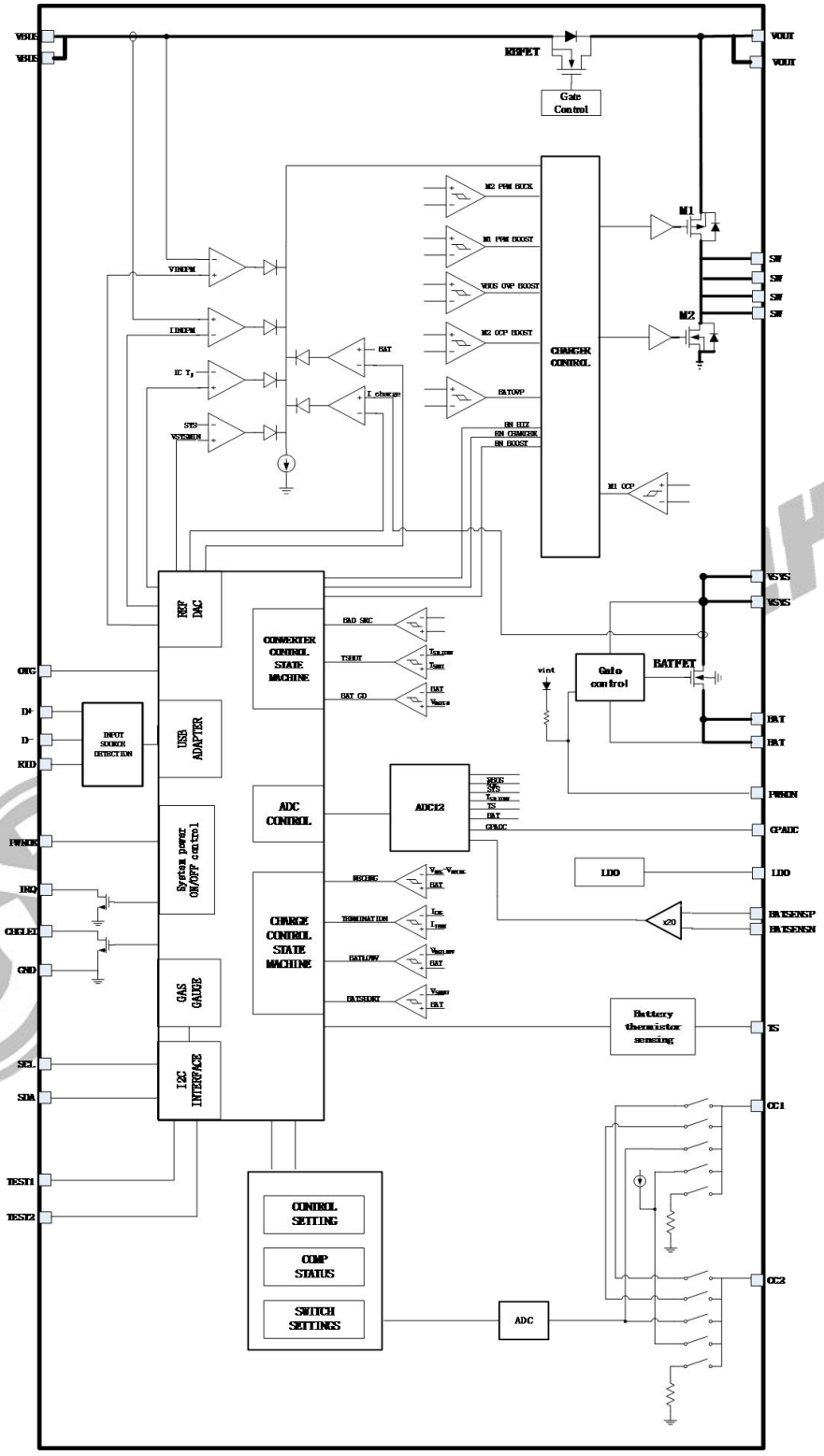
AXP2585 supports high output current up to 3A for fast charging. Besides, AXP2585 supports OTG mode with current limit. To ensure the security and stability of the system, AXP2585 provides multiple channels 12-bit ADC for voltage/current/temperature monitor and integrates protection circuits such as over-voltage protection(OVP), over-current protection(OCP) and over-temperature protection(OTP). Moreover, AXP2585 features a unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

AXP2585 supports type-C cc logic and BC1.2 protocol. It can automatically detect different adapters and adjust the input current limit.

AXP2585 provides a fast interface(Two Wire Serial Interface, TWSI) for system to dynamically adjust output voltages, charge current and configure interrupt condition.

AXP2585 is available in 5mm x 5mm 32-pin QFN package.

7.2 Function Block Diagram



7.3 Serial Interface Communication

AXP2585 supports TWSI protocol and performs as a TWSI slave device with default address 0x68/0x69. When AXP2585 powers on, SCK/SDA pin of TWSI will be pulled up to IO Power and then Host can adjust and monitor AXP2585 with rich feedback information.
Besides, AXP2585 supports RSB for Allwinner platform with address 0x01D1 or 0x0273 by customer.
Note: "Host" here refers to system processor.

7.4 NVDC

AXP2585 uses Narrow VDC(NVDC) architecture with BATFET connecting system and battery.

VBUS as the charger input, connecting to VSYS pin through a switch mode buck charger, provides power to system and charges battery through BATFET. Charge current can be adjusted automatically according to the feedback current which is detected with an external 10mΩ resistor. When system current(I_{SYS}) changes, the detected current will change, and then the current change signal will feed back to charge loop to adjust the charge current to the setting value.

AXP2585 starts up when an adapter is inserted and the input voltage meets the condition. System voltage(V_{SYS}) will rise up to minimum system voltage(V_{SYS_min}). if V_{SYS} does not reach V_{SYS_min}, the charging process does not start up. V_{SYS_min} can be configured by reg12H[2:0]. When V_{SYS} is higher than V_{SYS_min}, charger enabled signal will be sent.

When it is charging, if battery voltage is below V_{SYS_min}, BATFET operates in linear mode(LDO mode) to keep V_{SYS} at V_{SYS_min}. As battery voltage rises above V_{SYS_min}, BATFET is fully on.

When battery voltage is above V_{SYS}, BATFET is turned on and BMU enters supplement mode. When in supplement mode, if the discharge current is lower than 2A, BMU controls the voltage(V_{DS}) between system and battery and keeps V_{DS} at 20mV to avoid entering and exiting supplement mode repeatedly. As discharge current increases, BMU adjusts BATFET to be fully on and V_{DS} increases linearly. If an adapter is not inserted, system current is provided only by battery. At this time, BATFET is at fully on state.

7.5 Power On/Off and reset

7.5.1 Power on reset(POR)

AXP2585 is powered from the higher voltage between VBUS and BAT. When VBUS voltage(V_{VBUS}) is higher than V_{VBUS_UVLOZ} or BAT voltage(V_{BAT}) is higher than V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator and BATFET driver are active. All registers are reset to the default value. TWSI communication is active and Host can communicate with BMU.

7.5.2 Power up from BAT

If only battery is present and V_{BAT} is higher than depletion threshold(V_{BAT_DPLZ}), BATFET, connecting battery to system, is off by default and need to be turned on by pressing the PWRON key or inserting an adapter.

7.5.3 Power up from VBUS

When VBUS is inserted, BMU detects the input voltage to start up the reference voltage and the bias circuit. When V_{VBUS} is higher than V_{VBUS_UVLOZ}, the VBUS insertion IRQ is sent and the register bit reg02H[1] is set to 1 to indicate VBUS is inserted. Then BMU detects the input source whether it is good or not. If D+/D- automatic detection enabled bit(AUTO_DPDM_EN,reg23H[6]) is active, BMU detects the input source type and set the input current limit(I_{INLIM}) automatically, and then the buck converter starts up.

7.5.3.1 Good source condition

BMU needs to check the current capability of the input source. Only when the input source meets the following requirements can it start the buck converter.

a. VBUS voltage lower than V_{ACOV}
b. VBUS voltage higher than $V_{VBUSMIN}$ when pulling I_{BADBUS}(typical 30mA)

Once the input source meets the requirements above,the register bit reg00H[1](VBUS_GD) is set to 1 to indicate the input source is good. If the input source does not meet the requirements, detection will be done repeatedly every 2 seconds.

7.5.3.2 Input source type detection

AXP2585 integrates USB Charging Specification 1.2(BC1.2) and Type C(cc logic) detection. The type and the power supply capability of the input source can be detected and I_{INLIM} can be set automatically.

After the VBUS_GD bit is set to 1, if D+/D- automatic detection enabled bit (AUTO_DPDM_EN, reg23H[6]) or CC pin automatic detection enabled bit (AUTO_CC_EN,reg23H[4]) is active, BMU starts input source type detection automatically. BC1.2 detection and CC logic detection are independent and they work in parallel, but the detection result of CC logic has higher priority level than that of BC1.2. When the two kinds of detection are both under way, if CC logic detection finishes first and I_{INLIM} is set, I_{INLIM} can not be changed by the BC1.2 detection result. However, if BC1.2 detection finishes first and I_{INLIM} is set, I_{INLIM} can be changed by the CC logic detection result.

After input source type detection finishes, BMU sends IRQ to Host and sets the register bits reg00H[5:0] to set I_{INLIM} according to the detection result.

7.5.3.3 Set input voltage limit(V_{INDPM})

AXP2585 supports wide range of input voltage(3.9V~5.5V). V_{INDPM} can be set through reg11H[3:0]. The range of V_{INDPM} is from 3.88V to 5.08V and the step is 80mV.

When VBUS voltage reaches V_{INDPM}, the charge current will decrease automatically until the current is zero. If I_{SYS} is over the input power supply capability, V_{SYS} will drop. If V_{BAT} is above V_{SYS}, BMU will enter the supplement mode.

7.5.3.4 Buck converter start up

After I_{INLIM} is set, the buck converter is enabled. If battery charging is disabled,BATFET is in off state. Otherwise BATFET is in on state and the buck converter charges the battery.

AXP2585 integrates soft-start function.When V_{SYS} is lower than 2.2V, I_{INLIM} is forced to the lower one between 200mA and I_{INLIM} register value. When V_{SYS} is higher than 2.2V, I_{INLIM} is set through register value. The working

condition of buck converter can switch between PWM and PFM automatically according to the load.

7.5.4 System power on/off management

AXP2585 has system power on/off management function. It can be used with other PMU together to complete the function through PWRON pin and PWROK pin. PWRON pin is an IO pin. When it is as input, BMU can detect the status of the external key through it to send IRQ and realize power on reset. When it is as output, BMU can sent power on signals to the behind PMU through PWRON pin. PWROK pin is connected to the PWROK signal of the behind PMU to judge the PMU status.

System status is saved in register bit reg14H[0]. BMU sends power on/off signals according to system status and trigger events.

7.5.4.1 PWRON pin

A Key can be connected between PWRON pin and GND. When PWRON pin is as input, its function is as described below:

- If BMU is in shipping mode, when PWRON key is low for longer than ONLEVEL(reg15H[3:2]), BMU exits shipping mode.
- If BMU is not in shipping mode, when PWRON key is pressed, the negative edge is detected and IRQ is sent. When PWRON key is low for less than IRQLEVEL(reg15H[7:6]), BMU sends a short press IRQ and a positive edge IRQ. When PWRON key is low for longer than IRQLEVEL and less than PORLEVEL(reg15H[5:4]), BMU sends a long press IRQ and a positive edge IRQ. When PWRON key is low for longer than PORLEVEL, power on reset(POR) will be done.

7.5.4.2 System power on

When system is power off and one of power on sources is detected , BMU sends power on signal to the behind PMU to power on system.

Power on sources include:

- VBUS insertion(V_{VBU}>V_{VBUS_UVLOZ} & V_{VBUS}<V_{ACOV} & V_{SYS}>3.0V & reg17H[7]=1)
- BAT insertion(V_{BAT}>V_{BAT_UVLOZ} & V_{SYS}>3.0V & reg17H[6]=1)
- BAT is charged to normal(V_{BAT}>3.6V & Is charging & reg17H[5]=1)
- IRQ Low level(IRQ pin is low level for more than 16ms & reg17H[4]=1)

Once one of the power on sources above is detected, BMU sends power on signal. Power on signal has three forms, including low level pulse, special sequence and high/low level, which can be configured by customization.

After the power on signal is sent, BMU monitors the status of PWROK pin. If PWROK pin is high level, it means system is powered on successfully and the system status bit(reg14H[0]) is set to 1. If PWROK pin is low level, it means system is powered on unsuccessfully and the system status bit(reg14H[0]) is set to 0.

When high/low level is chose as power on signal, if the system is powered on unsuccessfully or the system is powered off abnormally, the PWROK pin will be low, the system status bit will be set to 0 and the active level will be changed to unactive level.

7.5.4.3 System power off

When system is power on and one of power off sources is detected , BMU sends power off signal to the behind

PMU to power off system.

Power off sources include:

- Software power off(Write “1” to reg17H[0])
- Watchdog timer out(Watchdog time out & reg17H[2]=1)

Once one of the power off sources above is detected, BMU sends power off signal. Power off signal has two forms, including low level pulse and high/low level. If power on signal is low level pulse or special sequence, power off signal will be low level pulse. If power on signal is high/low level, power off signal will be the opposite level. The system status bit(reg14H[0]) is set to 0 when PWROK signal changes from high level to low level.

7.5.5 Power off

- When VBUS is removed, BMU disables the charger, RBFET and all the bias circuits. The system is supplied by the battery. If the start-up conditions are meet, the associated circuits are enabled again.
- When the die or the battery is over temperature, BMU disables the buck converter, OTG and BATFET.

7.5.6 System reset

AXP2585 has power on reset and system reset.

1. Power on reset(POR)

There are two ways of power on reset.

- VBUS or battery inserts and the voltage meets the start-up conditions.
- PWRON key is low for longer than PORLEVEL(PORLEVEL is set by reg15H[5:4] and the default value is 12s).

2. System reset

System reset method just resets some associated registers. There are three ways of system reset.

- System power off. When the system status bit(reg14H[0]) is set to 0, BMU implements system reset.
- Software reset. Write “1” to reg14H[3].
- Watchdog time out to reset. The function is disabled by default.

7.6 Charger

7.6.1 Characteristics

- Range of input voltage:3.9V~5.5V, PWM charger, supports single cell Li-battery
- High charge efficiency in fast charging mode:>90% @5V(VIN)_2A(I_{CHG})
- Pre-charge current settable($I_{PRE-CHG}$, reg8A[4:1]), default:128mA, range: 64mA~1024mA,step:64mA
- Fast charge current settable(I_{CHG}, reg8B[5:0]), default:1024mA, range: 0mA~3072mA,step:64mA
- Target charge voltage settable(V_{REG}, reg8C[7:2]), default:4.25V, range: 3.840V~4.608V, step:16mV
- Accuracy of target voltage:±0.5%(testing ambient temperature:25℃,target voltage:4.256V)

7.6.2 Charging condition

- VBUS is present and available, $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$

- Input source detection finishes(reg00H[1]=1)
- Charging is enabled(reg8AH[7]=1)
- Die temperature is lower than T_{SHUT}
- When TS pin is used to detect battery temperature, battery temperature is within the chargeable range
- V_{BAT} is lower than V_{BAT_OVP}
- No charger safety timer fault
- BATFET is not forced to be off (BATFET_DIS bit, reg10H[7]=0)

7.6.3 Charging process

When BMU meets all charging conditions, it can complete the whole charging process without the participation of Host. The charging status can be known from the register bits reg00H[4:2]. The default values of charging parameters are shown as following. Host can modify registers to optimize the values through TWSI.

Table 7-1

Parameter	Default value
Charging voltage	4.208V
Charging current	1.024A
Pre-charging current	128mA
Termination current	128mA
Temperature profile	Cold/hot
Safety timer	12hours

1. Pre-charge

When V_{BAT} is lower than $V_{BATLOWV}$(reg8CH[1]), the charger is under pre-charge mode where charging current is limited to a value of $I_{PRE-CHG}$. Safety time is set through reg8EH[6:5] and its default value is 50 minutes. If pre-charge process times out, BMU will stop charging and send a corresponding IRQ to Host. The function of safety timer can be disabled through reg8EH[7].

2. Constant current charge

Once V_{BAT} is higher than $V_{BATLOWV}$ and lower than V_{REG}, the charger is under constant current charge mode. It will charge with constant current I_{CHG}.

3. Constant voltage charge

When V_{BAT} reaches target voltage(V_{REG}), the charger enters constant voltage charge mode. In this stage, the charger keeps the output voltage constant and step down charging current gradually, in order to fully charge battery.

When V_{BAT} is above V_{RECHG} and the charging current reduces under termination current(I_{TERM}), AXP2585 reports charger done, stops charging(charger enable bit is still 1) and turns off BATFET. Meanwhile, IRQ is sent to Host. After the charging process is completed, a charging cycle can be started again by writing 0 to reg8AH[7] first and then writing 1.

When AXP2585 is in regulation of input current, input voltage or temperature, the function of charging termination configured through reg8DH[7] is temporarily disabled and the speed of safety timer slows down. Whether to set safety timer during DPM or thermal regulation depends on reg8EH[4].

4. Re-charge

After charge done, if V_{BAT} falls below V_{RECHG}, BMU will automatically enable charger without reinserting adapter.

No matter whether V_{BAT} is above V_{RECHG} or not, the charger is enabled when an adapter is inserted.

5. Battery detection

As long as an AC adapter is present and usable, battery detection will be enabled to detect whether battery is connected. Battery detection function is enabled by default and can be disabled through reg8EH[3]. If the function is disabled, BMU considers that battery is always present. The detection result is saved in reg02H[4:3.]

7.6.4 Charging protection

1. charger safety timer

Once starting pre-charge mode, BMU will enable timer1. If BMU can not enter constant current charge mode from pre-charge within 50min(set through reg8EH[6:5]), BMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

When the charger enters into constant current charge mode, BMU will enable timer2. If BMU can not finish the whole charge cycle within 12 hours(set through reg8DH[2:1]), BMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

Timing speed of timer1 or timer2 is relevant with actual charge current. The smaller the actual charge current, the slower timing speed is.

2. Battery safe mode

In battery safe mode, the charger always charges with 10mA current. BMU can quit battery safe mode with one of the following methods:

- $V_{BAT}>V_{RECHG}$
- Adapter removal
- Charger enable bit(reg8AH[7]) is set to 0
- Safety timer1 enable bit(reg8EH[7]) or safety timer2 enable bit(reg8DH[0])is set to 0

3. BMU die temperature protection

AXP2585 has built-in temperature protection function through ADC to monitor internal temperature.

Under charging mode, the temperature point of thermal regulation can be set through reg18H[7:6]. When die temperature rises up to the setting point, the charging current will be decreased to decrease heat. When thermal regulation works, actual charge current is lower than the setting value and thermal regulation status(reg02H[2]) is set to 1. If die temperature rises up to T_{SHUT}(140℃), the buck converter is disabled and BATFET is turned off. Then charge fault status(reg04H[5:4]) is set to "10" to indicate over temperature protection and IRQ is sent . When die temperature falls below hysteretic threshold(120℃), BATFET will not be turned on automatically.

4. Battery temperature protection

AXP2585 can monitor battery temperature, when TS pin is used to detect battery temperature and parallel with charger(reg81H[7]=0). The battery temperature sensitive resistor is connected between TS pin and GND. The suggestion resistance should be 10Kohm at 25℃ ambient temperature. Through TS pin, BMU outputs constant current which can set through reg81H[2:1] to adapt different resistance. When the resistance is 10Kohm, the current should be set to 60uA. The enable bit of TS current source is configured through reg81H[4:3]. When current passes through the temperature sensitive resistor, BMU gets a detected voltage and calculates its value through ADC circuit. Take for example, TH11-3H103F temperature sensitive resistor of Mitsubishi Company. Using 60uA current source, the relationship among temperature, equivalent resistance, detected voltage and ADC data is as following.

Table 7-2

Temperature	equivalent resistance	detected voltage	ADC 12bit data
-16~-17℃	54.60Kohm	3.276V	FFFH
-15℃	50.15Hohm	3.009V	EB1H
-10℃	40.26Kohm	2.416V	BCCH
-5℃	32.55Kohm	1.953V	989H
0℃	26.49Kohm	1.481V	73BH
5℃	21.68Kohm	1.301V	65AH
10℃	17.78Kohm	1.067V	42AH
25℃	10.00Kohm	0.600V	2EEH
40℃	5.839Kohm	0.350V	1B5H
45℃	4.924Kohm	0.295V	170H
50℃	4.171Kohm	0.250V	138H
55℃	3.549Kohm	0.213V	10AH
60℃	3.032Kohm	0.182V	0E3H

During battery charging process, if TS pin voltage is lower than VHTF-CHG or higher than VLTF-CHG(VHTF-CHG and VLTF-CHG can be set through reg84H and reg85H. The default value of VLTF-CHG is set around 0℃ and VHTF-CHG around 45℃), which indicates battery temperature is too high or too low, then the charger is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the charger will recovery automatically.

During boost mode, if TS pin voltage is lower than VHTF-WORK or higher than VLTF-WORK(VHTF-WORK and VLTF-WORK can be set through reg86H and reg87H. The default value of VLTF-WORK is set around -10℃ and VHTF-WORK around 55℃), which indicates battery temperature is too high or too low, then the boost is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the boost will recovery automatically.

High temperature protection threshold hysteresis for VHTF-CHG and VHTF-WORK can be set through reg83H(default 50mV, ADC data 40H). Low temperature protection threshold hysteresis for VLTF-CHG and VLTF-WORK can be set through reg82H(default 300mV, ADC data 180H). The range of temperature detection can be expanded by adding more resistors.

Some battery may have no temperature sensitive resistor. Under this situation, TS pin can be pulled down to GND with a 10Kohm resistor externally or set as external input of ADC through register.

Use TS pin current source and obtain TS pin data according to the following table:

Table 7-3

Usage condition	setting
Not need temperature protection	reg81H[7]=1
Temperature protection when in charger	reg81H[7]=0, reg81H[4:3]=01
Temperature protection when in charging and discharging	reg81H[7]=0, reg81H[4:3]=10
Use TS pin current source to drive other device	reg81H[4:3]=11 when need current source reg81H[4:3]=00 when not need current source

7.6.5 Charging indication

CHGLED pin uses open-drain/push-pull output method. It is internally pulled up to LDO. Its output drive capability is above 10mA. Detail function control is shown as the following table.

Table 7-4

REG90H[2:0]= 000 (Type A CHGLED) Open Drain	Hi-Z	No charging(conditions are not met or battery charged)
	25% 1Hz pull low/Hi-Z jump	Charger internal abnormal alarm(including timer out、 die temperature over temperature、 battery temperature out of charging range)
	25% 4Hz pull low/Hi-Z jump	Input source or battery over voltage
	Pull low	Charging
REG90H[2:0]= 001 (Type B CHGLED) Open Drain	Hi-Z	No VBUS, and power supply by battery
	25% 1Hz pull low/Hi-Z jump	Charging
	25% 4Hz pull low/Hi-Z jump	Alarm, including input source or battery over voltage, battery temperature out of charging range, timer out,die temperature over temperature
	Pull low	No battery or charge finished, and power supply by VBUS
REG90H[2:0]= 010 (Breath CHGLED) Open Drain	Hi-Z	No VBUS, and power supply by battery
	Breath LED output(*note1)	Charging
	Pull low	No battery or charge finished, and power supply by VBUS
REG90H[2:0]= 011 (Breath Lamp) Open Drain	Breath LED output, enable bit: REG90H[6] Breath frequency and luminance are controlled by REG91H~REG9AH	
REG90H[2:0]= 100 (Tri-state CHGLED) Push Pull	Hi-Z	No VBUS, and power supply by battery
	Pull high	Charging
	Pull low	No battery or charge finished, and power supply by VBUS
REG90H[2:0]= 101 (PWM function) Push Pull	PWM output, enable bit: REG90H[6] The frequency and duty-cycle are controlled by REG95H~99H	
REG90H[2:0]=110/111 (GPO) Push Pull	The output status is controlled by REG90H[5:3]	

Note: LED is on when CHGLED is low.

7.7 BATFET

BATFET connects system and battery. The on-resistance is low to 30mohm(point to point).

7.7.1 Enter shipping mode

In order to increase the life of battery and reduce consumption during transportation, system is allowed to turn off BATFET automatically. When BMU is supplied by only battery, V_{SYS} is 0 after BATFET is turned off, which can make the leakage voltage minimum. There are some ways to turn off BATFET to enter shipping mode. Reg00[0] can indicate BATFET status.

BATFET off sources:

- Write "1" to reg10H[7]. Force BATFET off, highest priority.
- Charge done
- VBUS present but charger disabled(reg8AH[7]=0)

7.7.2 Exit shipping mode

BATFT can be enabled again with the following method.

- PWRON key is low for longer than ONLEVEL

7.8 Boost mode

AXP2585 supports boost mode which can provide current from battery to VBUS pin. The boost mode can be enabled when the following conditions are met.

- V_{BAT} is higher than $V_{BATLOWV}$.
- V_{VBUS} is lower than $V_{BAT}+V_{SLEEP}$.
- Boost enable register, (reg12H[7]]=1)||(reg23H[5]=1 & OTG device plugs in).
- OTG pin is high level.
- Battery temperature is in charging range.
- Die temperature is below T_{SHUT}.

In boost mode, the output voltage can be set through reg13H[7:4]. Moreover, output current limit function can be realized through RBFET. The current limit value is set through reg13H[1:0]. The switch frequency of boost converter is 1.5MHz which can not be changed. The maximum output current is up to 1.5A. The efficiency is 90% @3.5V_5V_1A.

There are OCP function and OVP function in boost mode. When over current or over voltage occurs, boost converter will be turned off and IRQ will be sent to Host.

In boost mode, if reg11H[6] is set to 0, BMU pulls down VBUS to avoid VBUS voltage rising due to electric leakage. If reg11H[6] is set to 1, it means the path from VMID and VBUS is available and it is prohibited to pull down VBUS. When charging conditions are met, boost converter will be disabled and then charger will be enabled

7.9 RBFET

RBFET connects VMID and VBUS. The on-resistance is low to 30mohm(point to point). It supports input and output current limit function. In charger mode, the input current limit value of RBFET is set through reg10H[5:0]. In boost mode, the output current limit value of RBFET is set through reg13H[1:0].

7.10 ADC

AXP2585 has a low speed 12Bit SAR ADC for measuring BAT voltage, BAT charge current and BAT discharge current, TS voltage, GPADC voltage and die temperature. No IRQ for ADC output. The ADC sampling frequency can be set to 800/400/200/100Hz. Channel 2 is fixed to 25Hz.

Table 7-5

No.	Channel function	000H	001H	002H	…	FFFH
0	BAT voltage	0mV	1.2mV	2.4mV	…	4.914V
1	Reserved					
2	Die temperature	-267.7℃	+0.10625*xxxH (℃)			167.4℃
3	BAT charge current	0mA	2mA	4mA	…	8.160A
4	BAT discharge current	0mA	2mA	4mA	…	8.160A
5	TS pin input	0mV	0.8mV	1.6mV	…	3.276V
6	GPADC pin Input	0mV	0.8mV	1.6mV	…	3.276V

Note: ADC data is 12 bits. In order to get the complete data, TWSI must read the high 8 bits firstly and then the low 4 bits.

7.11 E-Gauge

The Fuel Gauge comprises of 3 modules: Rdc calculation module; OCV (Open Circuit Voltage) and Coulomb counter module; and calibration module. The Fuel Gauge system is able to export information about battery such as Battery capacity percentage (regB9H), Battery Voltage (reg78H, reg79H), Battery charging current (reg7AH, reg7BH), Battery discharge current (reg7CH, reg7DH), Battery maximum capacity (regE0H, regE1H), Battery Rdc value (regBAH, regBBH). The Fuel Gauge can be enabled or disabled through regB8H. The Battery low warning level can be set in regE6H, and IRQ will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set in regE6H.

Once a default battery is selected for a particular design, it is highly recommended to calibrate the battery to achieve better Fuel Gauge accuracy. Once the calibration data are available, user can write the calibration information to regC0H ~regDFH (OCV percentage table) on each boot. Or user can choose not to do the calibration and use the default OCV percentage value. Additionally, the Fuel Gauge system is capable to learn the battery characteristic on each full charge cycle.Information such as battery maximum capacity (regE0H, regE1H) and Rdc (regBAH, regBBH) will be updated automatically over time.

7.12 IRQ, GPADC, LDO

7.12.1 IRQ

AXP2585 has an IRQ pin which is used to indicate whether there interrupt events occur.
BMU Interrupt Controller monitors the trigger events such as over voltage, over current, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enabled bits are set to 1 (Refer to registers reg40H/41H/42H/43H/44H/45H), corresponding IRQ status will be set to 1 (Refer to registers reg48H/49H/4AH/4BH/4CH/4DH), and IRQ pin will be pulled down. When Host detects triggered IRQ signal, Host

will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing “1” to status bit.

When reg17H[4] is set to 1, IRQ pin can be used as power on source.

7.12.2 GPADC

GPADC pin is a general purpose input pin for ADC. Its circuit realization is the same as that of TS pin.

7.12.3 LDO

AXP2585 has a LDO output. Its features are shown as follows.

- Output voltage range: 1.8V(default)/2.5V/2.8V/3.3V, can be configure by customization.
- IMAX=20mA, Vdropout=0.4V

7.13 Type-C

AXP2585 supports Type-C cc logic and DRP. The function is customizable and is disabled by default.

When BMU is powered from battery, if type-c device is inserted, BMU set in DRP mode can detect device insertion through CC pin and distinguish each side of plug. The detection result is saved in reg37H[3:0] and IRQ is sent to Host.

If the type-c device is DFP, BMU will switch to UFP mode and set I_{INDPM}, waiting for VBUS.

If the type-c device is UFP, BMU will switch to DFP mode, and then enable boost converter and turn on RBFET to supply power to VBUS. When UFP device is removed, BMU can detect device removal through CC pin and turn off RBFET. Whether to disable boost mode depends on application scenarios. Function of automatically turning on boost converter and RBFET can be disabled through reg23H[5].

7.14 Register

7.14.1 Register List

Address	Description	R/W	Default
00	BMU status1	R	
01	BMU status2	R	
02	BMU status3	R	
04	BMU status4	R	
05	BMU status5	R	
06	System power on/off source indication	RW	00H
10	BATFET & input current limit control	RW	48H
11	BATFET & RBFET & input voltage limit control	RW	06H
12	Boost & minimum system voltage control	RW	2DH
13	Boost voltage & RBFET current limit control	RW	94H
14	WATCHDOG timer setting & register reset & system status	RW	00H

Address	Description	R/W	Default
15	POK setting	RW	69H
16	System power on/off control1	RW	10H
17	System power on/off control2	RW	00H
18	Thermal regulation threshold setting	RW	89H
20	BC1.2 detection control1	RW	20H
21	BC1.2 detection control2	RW	20H
22	BC1.2 detection control3	RW	00H
23	DPDM & OTG & CC enable control	RW	70H
31	CC_GLOBAL_CTRL	RW	09H
33	CC_MODE_CTRL	RW	11H
34	CC_TOGGLE_CTRL	RW	00H
37	CC_Status0	R	00H
3A	CC_Status1	R	00H
3E	Interface mode select	RW	00H
40	IRQ Enable1	RW	06H
41	IRQ Enable2	RW	FFH
42	IRQ Enable3	RW	FFH
43	IRQ Enable4	RW	00H
44	IRQ Enable5	RW	F4H
45	IRQ Enable6	RW	C6H
48	IRQ Status1	RW	00H
49	IRQ Status2	RW	00H
4A	IRQ Status3	RW	00H
4B	IRQ Status4	RW	00H
4C	IRQ Status5	RW	00H
4D	IRQ Status6	RW	00H
56	BMU Internal temperature ADC data, high 8 bits	R	00H
57	BMU Internal temperature ADC data, low 4 bits	R	00H
58	Ts pin ADC data, high 8bits	R	00H
59	Ts pin ADC data, low 4 bits	R	00H
5A	GPADC pin ADC data, high 8bits	R	00H
5B	GPADC pin ADC data, low 4 bits	R	00H
78	Average data bit[11:4] for Battery voltage	R	00H
79	Average data bit[3:0] for Battery voltage	R	00H
7A	Average data bit[11:4] for Battery charge current	R	00H
7B	Average data bit[3:0] for Battery charge current	R	00H
7C	Average data bit[11:4] for Battery discharge current	R	00H
7D	Average data bit[3:0] for Battery discharge current	R	00H
80	ADC Enable	RW	F2H
81	TS pin CTRL & ADC speed setting & GPADC mode CTRL	RW	0CH
82	TS/GPADC_HYSL2H setting	RW	18H

Address	Description	R/W	Default
83	TS/GPAC_HYSH2L setting	RW	04H
84	VLTF_CHG setting	RW	74H
85	VHTF_CHG setting	RW	17H
86	VLTF_WORK setting	RW	BDH
87	VHTF_WORK setting	RW	11H
88	VLTF_GPADC setting	RW	BDH
89	VHTF_GPADC setting	RW	0EH
8A	Charger control1	RW	82H
8B	Charger control2	RW	10H
8C	Charger control3	RW	6AH
8D	Charger control4	RW	8DH
8E	Charger control5	RW	B8H
90	CHGLED pin function setting	RW	00H
91	Breath function control1	RW	64H
92	Breath function control2	RW	01H
93	Breath function control3	RW	06H
94	Breath function control4	RW	01H
95	Breath function control5	RW	64H
96	Breath function control6	RW	00H
97	PWM output frequency setting	RW	64H
98	Breath function control7 & Input clock frequency for PWM output	RW	16H
99	PWM function duty setting	RW	32H
9A	CHGLED breath time unit option	RW	65H
B8	Fuel Gauge Control	RW	C0H
B9	Battery capacity percentage for indication	R	64H
BA	RDC 1	RW	80H
BB	RDC 0	RW	55H
BC	OCV 1	R	00H
BD	OCV 0	R	00H
C0	OCV percentage table	RW	00H
C1	OCV percentage table	RW	00H
C2	OCV percentage table	RW	01H
C3	OCV percentage table	RW	02H
C4	OCV percentage table	RW	04H
C5	OCV percentage table	RW	06H
C6	OCV percentage table	RW	08H
C7	OCV percentage table	RW	0AH
C8	OCV percentage table	RW	0CH
C9	OCV percentage table	RW	0FH
CA	OCV percentage table	RW	12H
CB	OCV percentage table	RW	17H

Address	Description	R/W	Default
CC	OCV percentage table	RW	1DH
CD	OCV percentage table	RW	23H
CE	OCV percentage table	RW	29H
CF	OCV percentage table	RW	2FH
D0	OCV percentage table	RW	34H
D1	OCV percentage table	RW	38H
D2	OCV percentage table	RW	3FH
D3	OCV percentage table	RW	46H
D4	OCV percentage table	RW	4CH
D5	OCV percentage table	RW	4FH
D6	OCV percentage table	RW	52H
D7	OCV percentage table	RW	55H
D8	OCV percentage table	RW	57H
D9	OCV percentage table	RW	59H
DA	OCV percentage table	RW	5BH
DB	OCV percentage table	RW	5DH
DC	OCV percentage table	RW	5FH
DD	OCV percentage table	RW	61H
DE	OCV percentage table	RW	62H
DF	OCV percentage table	RW	63H
E0	Battery maximum capacity	RW	00H
E1	Battery maximum capacity	RW	00H
E2	Coulomb meter counter	RW	00H
E3	Coulomb meter counter	RW	00H
E4	OCV Percentage of battery capacity	R	64H
E5	Coulombmeter percentage of battery capacity	R	64H
E6	Battery capacity percentage warning level	RW	A0H
E7	OCV_SOC curve setting	RW	0FH
E8	Fuel gauge tuning control 0	RW	00H
E9	Fuel gauge tuning control 1	RW	00H
EA	Fuel gauge tuning control 2	RW	00H
EB	Fuel gauge tuning control 3	RW	00H
EC	Fuel gauge tuning control 4	RW	00H
ED	Fuel gauge tuning control 5	RW	00H
EE	Fuel gauge tuning control 6	RW	01H
EF	Fuel gauge tuning control 7	RW	00H

7.14.2 Register Description

REG 00H: BMU status1

Reset: power on reset

Bit	Description	R/W
7-5	Reserved	R
4-2	Charging status 000: not charging 001: tri_charge 010: pre_charge 011: fast charging 100: constant voltage(CV) 101: charge termination done others: not used	R
1	VBUS good status(VBUS_GD) 0: not power good 1: power good	R
0	BATFET status 0: BATFET is off state 1: BATFET is on state	R

REG 01H: BMU status2

Reset： Power on reset

Bit	Description	R/W
7-5	USB BC1.2 Detection result 000 : Reserved 001 : SDP 010 : CDP 011 : DCP 100 : ACA – Dock 101 : ACA-A 110 : ACA-B 111 : ACA-C	R
4-0	RID detection result Bit [4] = 1 : rid is float Bit [3] = 1 : rid is Rgnd Bit [2] = 1 : rid is Ra Bit [1] = 1 : rid is Rb Bit [0] = 1 : rid is Rc	R

REG 02H: BMU status3

Reset: Power on reset

Bit	Description	R/W
7	VINDPM status 0: not in VINDPM 1: VINDPM	R
6	IINLIM status 0: Not in current limit	R

	1: In current limit	
5	charge system voltage status 0: Not over voltage 1: over voltage	R
4	battery detection result valid status : 0: Battery detection result is invalid; 1: Battery detection result is valid.	R
3	battery detection result: 0: Battery is absent; 1: Battery is present.	R
2	thermal regulation status 0: Normal 1: In thermal regulation	R
1	VBUS good status (indicate whether VBUS attached or not). 0: Not VBUS attached 1: VBUS attached	R
0	Battery current direction 0: Discharging 1: Charging	R

REG 04H: BMU status4

Reset: Power on reset

Bit	Description	R/W
7	Watchdog fault status 0: Normal 1: Watchdog timer expiration	R
6	Boost mode fault status 0: Normal 1: VBUS overload in OTG, or VBUS OVP, or battery is too low in boost mode	R
5-4	Charge fault status 00: Normal 01: Input fault(VBUS>VACOV or VBAT<VBUS<VBUSMIN(typical 3.8V) 10: Thermal shutdown 11: Charge safety timer expiration	R
3	Battery fault status(OVP) 0: Normal 1: BATOVP(VBAT>VBATOVP)	R
2-0	NTC fault status buck mode: 000: Normal 001: TS cold 010: TS hot boost mode: 000: Normal	R

	101: TS cold 110: TS hot	

REG 05H: BMU status5

Reset: Power on reset

Bit	Description	R/W
7	PMIC have calibrated the OCV-percentage curve 0: have not calibrated 1: have calibrated	R
6	PMIC have calibrated the total battery capacity 0: have not calibrated 1: have calibrated	R
5-0	Reserved	R

REG 06H: System power on/off source indication

Reset: Power on reset

Bit	Description	R/W
7	System power on from VBUS insertion status indication. 0: Negative 1: Active	R
6	System power on from Battery insertion status indication 0: Negative 1: Active	R
5	System power on from Battery charge to normal status indication 0: Negative 1: Active	R
4	System power on from IRQ pin status indication 0: Negative 1: Active	R
3	Reserved	R
2	System power off from watch dog timeout status indication 0: Negative 1: Active	R/W
1	Reserved	R
0	System power off from software status indication 0: Negative 1: Active	R/W

REG 10H: BATFET & input current limit control

Default: 48H

Reset: power on reset

Bit	Description	R/W	Default
7	Force BATFET off to enable ship mode 0: allow BATFET turn on	RW	0

	1: force BATFET off		
6	Reserved	R	1
5-0	Input current limit(I_{INLIM}) offset: 100mA range:100mA(000000)--3.25A(111111) default:001000(500mA) step:50mA IINLIM bits are changed automatically after input source type detection is completed USB Host SDP & OTG=Hi(USB500)=500mA USB Host SDP & OTG=Lo(USB100)=100mA USB CDP/DCP=1.5A USB Type-C Current@3.0A = 3.0A USB Type-C Current@1.5A = 1.5A Others=1.5A	RW	001000

REG 11H: BATFET & RBFET & input voltage limit control

Default: 06H

Reset: bit[6]&[4] are system reset, others are power on reset

Bit	Description	R/W	Default
7	Set BATFET to forced on state. 0: allow BATFE to turn off. 1: force BATFE on.	RW	0
6	Set RBFET to forced on state in OTG mode 0: RBFET at off state, used for power bank 1: RBFET at on state, used for type-C VBUS power output	RW	0
5	Adjust VBUS over-voltage threshold setting(manual setting for apple adapter) 0: VBUS_OV=6.4V 1: VBUS_OV=6.8V	RW	0
4	OTG path can be selected or not: 0: OTG path can not be selected by software. 1: OTG path can be selected whatever, disable VBUS path.	RW	0
3-0	VINDPM threshold offset: 3.88V range: 3.88V(0000)--5.08V(1111) default: 4.36V(0110) step: 80mV	RW	0110

REG 12H: Boost & minimum system voltage control

Default: 2DH

Reset: bit[3] is power on reset, others are system reset

Bit	Description	R/W	Default
7	Boost(OTG)mode configuration(BOOST_EN)	RW	0

	0: OTG disable 1: OTG enable		
6	Reserved	R	0
5	Whether disable boost or not when VOUT is over voltage in boost mode. 0: Not disable boost mode 1: Disable boost mode	RW	1
4	Whether disable boost or not when VOUT is over current in boost mode. 0: Not disable boost mode 1: Disable boost mode	RW	0
3	The output voltage when RBFET is working in LDO mode. 0: 5.2V 1: 5.5V		1
2-0	minimum system voltage limit(VSYS_min) offset: 3.0V range: 3.0V--3.7V default: 3.5V step: 0.1V	RW	101

REG 13H: Boost voltage & RBFET current limit control

Default: 94H

Reset: bit[3-2] are power on reset, others are system reset

Bit	Description	R/W	Default
7-4	Boost mode voltage regulation(low voltage range) offset: 4.55V range: 4.55V--5.51V default: 5.126V step: 64mV	RW	1001
3-2	Boost mode disable threshold(Vbat_low) 00: 2.4V 01: 2.6V 10: 2.8V 11: 3.0V	RW	01
1-0	RBFET current limit in BOOST mode. 00: 500mA 01: 900mA 10:1500mA 11: Disable current limit	RW	00

REG 14H: WATCHDOG timer setting & register reset & system status

Default: 00H

Reset: bit[3-0] are power on reset, others are system reset

Bit	Description	R/W	Default
7	Watchdog timer reset 0: normal	RW	0

	1: reset(back to 0 after timer reset)		
6-4	Watchdog timer setting 000: disable watchdog timer 001: 1s 010: 2s 011: 4s 100: 8s 101: 40 110: 80s	RW	000
3	Register reset 0: keep current register setting 1: reset to default register value and reset safety timer note: the bit will reset to 0 after register reset is completed	RW	0
2-1	Reserved		
0	System status indication: 0: System is power off. 1: System is power on.	R	0

REG 15H: POK setting

Default: 69H

Reset: power on reset

Bit	Description	R/W	Default
7-6	IRQLEVEL setting 00 : 1s 01 : 1.5s 10 : 2s 11 : 2.5s	RW	01
5-4	PORELVEL setting 00 : 4s 01 : 8s 10 : 12s 11 : 16s	RW	10
3-2	ONLEVEL setting 00: 128ms 01 : 512ms 10 : 1s 11 : 2s	RW	10
1-0	OFFLEVEL setting 00 : 4.5s 01 : 6.5s 10 : 8.5s 11 : 10.5s	RW	01

REG 16H: System power on/off control1

Default: 10H

Reset: power on reset

Bit	Description	R/W	Default
7-6	PWRON output type setting: 00: Pull down for ONLEVEL 01:Special sequence 10: High/Low level(inhibit PWRON input function),active level depend on REG16[2]. 11: Inhibit output function	RW	00
5-4	Delay time to turn off BATFET through BATET_DIS function 00:0ms 01:8ms 10:16ms 11:32ms	RW	01
3	Reserved	R	0
2	Active level when PWRON is set as high/low level output: 0: Low level active 1: High level active	RW	0
1	Reserved	R	0
0	System power off clear the IRQ signal enable 0: Does not clear the IRQ signal 1: Clear the IRQ signal	RW	0

REG 17H: System power on/off control2

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	VBUS insertion send power on signal enable: 0: Does not send power on signal 1: Send power on signal	RW	0
6	Battery insertion send power on signal enable: 0: Does not send power on signal 1: Send power on signal	RW	0
5	Battery charge to normal send power on signal enable: 0: Does not send power on signal 1: Send power on signal	RW	0
4	IRQ pin low level send power on signal enable 0: Do not send power on signal 1: Send power on signal	RW	0
3	Reserved	R	0
2	Watch dog time out send power off signal enable 0: Does not send power off signal 1: Send power off signal	RW	0

1	Reserved	R	0
0	Software send power off signal enable 0: Does not send power off signal 1: Send power off signal, then clear itself automatically.	RW	0

REG 18H: Thermal regulation threshold setting

Default: 89H

Reset: power on reset

Bit	Description	R/W	Default
7-6	Thermal regulation threshold 00: 60deg 01: 80deg 10: 100deg 11: 120deg	RW	10
5-0	Reserved	R	001001

REG 20H: BC1.2 detection control1

Default: 20H

Reset: power on reset

Bit	Description	R/W	Default
7	DCD Detection enable during BC detect. 0 : disable 1 : enable	RW	0
6-5	DCD Detection time setting when DCD function enable 00 : 100ms 01 : 300ms 10 : 500ms 11 : 900ms	RW	01
4	The D- VLGC Compare enable during the BC Detect in primary detection 0 : disable 1 : enable	RW	0
3	The BC stays in dead battery status timeout enable when the battery voltage below the dead threshold. 0 : disable 1 : enable Note : the time is 45 min	RW	0
2	BC detection status indication 0 : detect finish 1 : in detecting	R	0
1-0	Reserved	R	0

REG 21H: BC1.2 detection control2

Default: 20H

Reset: power on reset

Bit	Description	R/W	Default
7-6	Reserved	R	0
5	DP/DM floating Detection enable when BC detection is not DCP and CDP. 0 : disable 1 : enable	RW	1
4-0	Reserved	R	0

REG 22H: BC1.2 detection control3

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Reserved	R	0
6	Dead Battery detection enable. 0 : disable 1 : enable. Note : if the battery is not connect, this function will disable.	RW	0
5	Reserved	R	0
4	The control bit for pull up the DP to 0.6V when detection result is DCP 0 : disable 1 : enable	RW	0
3	The detection result can be change when the rid is change after the bc detect finish. 0 : disable 1 : enable	RW	0
2	Reserved	R	0
1	Control bit for CC clock 0 : disable 1 : enable	RW	0
0	Reserved	R	0

REG 23H: DPDM & OTG & CC enable control

Default: 70H

Reset: power on reset

Bit	Description	R/W	Default
7	Force D+/D- detection 0: Not in D+/D- 1: Force D+/D- detection Note : This bit will clear itself.	RW	0
6	automatic D+/D- detection enable(AUTO_DPDM_EN) 0: disable D+/D- when VBUS is plugged-in 1: enable D+/D- when VBUS is plugged-in	RW	1
5	Automatic enable boost and RBFET control: 0: Disable auto control 1: Enable auto control	RW	1

4	automatic CC PIN detection enable(AUTO_CC_EN) 0: disable CC PIN detection when VBUS is plugged-in 1: enable CC PIN detection when VBUS is plugged-in(default)	RW	1
3-0	Reserved	R	0

REG 31H: CC_GLOBAL_CTRL

Default: 09H

Reset: power on reset

Bit	Description	R/W	Default
7-6	Reserved	R	0
5	Audio Accessory Enable. 0: disable 1: enable	RW	0
4	Reserved	RW	0
3	The Configuration Reset for CC Logic. 0: reset 1: disable	RW	1
2-0	Reserved	R	001

REG 33H:CC_MODE_CTRL

Default: 11H

Reset: power on reset

Bit	Description	R/W	Default
7	Reserved	R	0
6	The Current mode of UFP support 0: UFP support current mode of def/1.5A/3.0A 1: UFP only support current mode of def	RW	0
5	DRP port prefer to be SRC. 0: unactive 1: active	RW	0
4	DRP port prefer to be SNK. 0: unactive 1: active	RW	1
3-2	The Current Mode Control. 0x: Default Mode 10: 1.5A Mode 11: 3.0A Mode	RW	00
1-0	The Port Mode Control. 00: Disable 01: SINK 10: SOURCE 11: DRP	RW	01

REG 34H: CC_TOGGLE_CTRL

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-1	Reserved	R	0
0	Toggle Function Enable 0: disable 1: enable	RW	0

REG 37H: CC_Status0

Default: 00H

Reset: power on reset

Bit	Description	R/W
7-6	Reserved	R
5-4	The Power State of Source of CC Logic in HW mode 00: POWER IDLE 01: POWER_DEF 10: POWER_1P5A 11: POWER_3P0A	R
3-0	The State of CC Logic in HW mode 0000: DISABLE 0001: UNATTACH_SNK 0010: ATTACHWAIT_SNK 0011: ATTACH_SNK 0100: UNATTACH_SRC 0101: ATTACHWAIT 0110: ATTACH_SRC 0111: AUDIO_ACSY 1000: Reserved 1001: TRY_SRC 1010: TRYWAIT_SNK 1011: TRY_SNK 1100: TRYWAIT_SRC 1101: Reserved 1110: ERROR_RECOVERY 1111: Reserved	R

REG 3AH: CC_Status1

Default: 00H

Reset: power on reset

Bit	Description	R/W
7	Reserved	R
6	Awake Mode Status in HW mode 0: SINK or DRP in SINK	R

	1: SOURCE or DRP in SOURCE	
5	Awake Finish Flag in HW mode 0: unactive 1: active	R
4-0	Reserved	R

REG 3EH: Interface mode select

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Interface mode select 8'H7C : select RSB Others : select TWSI	RW	00H

REG 40H: IRQ Enable1

Default: 06H

Reset: power on reset

Bit	Description	R/W	Default
7	Battery capacity percentage drop to warning level2 IRQ(WL2IRQ) enable	RW	0
6	Battery capacity percentage drop to warning level1 IRQ(WL1IRQ) enable	RW	0
5	Battery capacity percentage change IRQ enable	RW	0
4	Gauge calculation complete IRQ enable	RW	0
3	battery detection complete IRQ enable	RW	0
2	Boost mode over voltage protection IRQ enable	RW	1
1	Boost mode over current protection IRQ enable	RW	1
0	Reserved	RW	0

REG 41H: IRQ Enable2

Default: FFH

Reset: power on reset

Bit	Description	R/W	Default
7	Battery over temperature in charge mode IRQ (BCOTIRQ) enable	RW	1
6	Quit Battery over temperature in charge mode IRQ (QBCOTIRQ) enable	RW	1
5	Battery under temperature in charge mode IRQ (BCUTIRQ) enable	RW	1
4	Quit Battery under temperature in charge mode IRQ (QBCUTIRQ) enable	RW	1
3	Battery over temperature in work mode IRQ (BWOTIRQ) enable	RW	1
2	Quit Battery over temperature in work mode IRQ (QBWOTIRQ) enable	RW	1
1	Battery under temperature in work mode IRQ (BWUTIRQ) enable	RW	1
0	Quit Battery under temperature in work mode IRQ (QBWUTIRQ) enable	RW	1

REG 42H: IRQ Enable3

Default: FFH

Reset: power on reset

Bit	Description	R/W	Default
7	VBUS insertion IRQ enable	RW	1
6	VBUS removal IRQ enable	RW	1
5	Battery insertion IRQ enable	RW	1
4	Battery removal IRQ enable	RW	1
3	Dead/Weak Battery charge to normal IRQ enable(The voltage threshold is as same as VSYS_min)	RW	1
2	Die over temperature IRQ enable	RW	1
1	Charger safety timer1/2 timeout and battery enters safe mode IRQ enable	RW	1
0	VBUS over voltage protection IRQ enable	RW	1

REG 43H: IRQ Enable4

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	PWRON short press IRQ enable(PWRON push down longer than 32ms, and less than IRQLEVEL)	RW	0
6	PRWON long press IRQ enable(PWRON push down longer than IRQLEVEL, and less than Power-on-reset time)	RW	0
5	PWRON negative edge IRQ enable(PWRON from high go low)	RW	0
4	PWRON positive edge IRQ enable(PWRON from low go high)	RW	0
3	GPADC over temperature IRQ enable	RW	0
2	Quit GPADC over temperature IRQ enable	RW	0
1	GPADC under temperature IRQ enable	RW	0
0	Quit GPADC under temperature IRQ enable	RW	0

REG 44H: IRQ Enable5

Default: F4H

Reset: power on reset

Bit	Description	R/W	Default
7	Charger begin charging IRQ enable	RW	1
6	Battery charge done IRQ enable	RW	1
5	BC1.2 detect finished IRQ enable	RW	1
4	BC1.2 detect result change IRQ enable	RW	1
3	RID detect result change IRQ enable	RW	0
2	BAT over voltage protection IRQ enable	RW	1
1-0	Reserved	R	0

REG 45H: IRQ Enable6

Default: C6H

Reset: power on reset

Bit	Description	R/W	Default
7	Type-C device removed (unattached) IRQ enable	RW	1

6	Type-C device insert and detection finished IRQ enable	RW	1
5-3	Reserved	R	000
2	Type-C error generated IRQ enable	RW	1
1	Type-C power state changed IRQ enable	RW	1
0	Reserved	R	0

REG 48H: IRQ Status1

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Battery capacity percentage drop to warning level2 IRQ(WL2IRQ) status. Writing 1 to this bit ,or percentage rise up the level2, or no battery connect will clear it.	RW	0
6	Battery capacity percentage drop to warning level1 IRQ(WL1IRQ) status. Writing 1 to this bit , or percentage rise up the level1, or no battery connect will clear it.	RW	0
5	Battery capacity percentage change IRQ status. Writing 1 to this bit, or no battery connect will clear it.	RW	0
4	Gauge calculation complete IRQ status. Writing 1 to this bit, or no battery connect, or Gauge disable will clear it.	RW	0
3	battery detection complete IRQ status. Writing 1 to this bit will clear it.	RW	0
2	Boost mode over voltage protection IRQ status. "1" is active, writing 1 to this bit will clear it.	RW	0
1	Boost mode over current protection IRQ status. "1" is active, writing 1 to this bit will clear it.	RW	0
0	Reserved	RW	0

REG 49H: IRQ Status2

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Battery over temperature in charge mode IRQ (BCOTIRQ) status. Writing 1 to this bit, or temperature go to normal will clear it.	RW	0
6	Quit Battery over temperature in charge mode IRQ (QBCOTIRQ) status. Writing 1 to this bit, or battery temperature rise to over temperature will clear it.	RW	0
5	Battery under temperature in charge mode IRQ (BCUTIRQ) status. Writing 1 to this bit, or temperature go to normal will clear it.	RW	0
4	Quit Battery under temperature in charge mode IRQ (QBCUTIRQ) status. Writing 1 to this bit, or battery temperature drop to under temperature will clear it.	RW	0
3	Battery over temperature in work mode IRQ (BWOTIRQ) status. Writing 1 to this bit, or temperature go to normal will clear it.	RW	0

2	Quit Battery over temperature in work mode IRQ (QBWOTIRQ) status. Writing 1 to this bit, or battery temperature rise to over temperature will clear it	RW	0
1	Battery under temperature in work mode IRQ (BWUTIRQ) status. Writing 1 to this bit, or temperature go to normal will clear it.	RW	0
0	Quit Battery under temperature in work mode IRQ (QBWUTIRQ) status. Writing 1 to this bit, or battery temperature drop to under temperature will clear it.	RW	0

REG 4AH: IRQ Status3

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	VBUS insertion IRQ status, Writing 1 to this bit , or VBUS Remove will clear it.	RW	0
6	VBUS removal IRQ status. Writing 1 to this bit, or VBUS insert will clear it.	RW	0
5	Battery insertion IRQ status. Writing 1 to this bit, or Battery remove will clear it.	RW	0
4	Battery removal IRQ status. Writing 1 to this bit, or Battery insert will clear it.	RW	0
3	Dead/Weak Battery charge to normal IRQ(The voltage threshold is as same as VSYS_min) status.Writing 1 to this bit, or no battery connect will clear it.	RW	0
2	Die over temperature IRQ status. Writing "1" , or the temperature drop to the normal will clear it.	RW	0
1	Charger safety timer1/2 timeout and battery enters safe mode IRQ status. Writing "1" will clear it.	RW	0
0	VBUS over voltage protection IRQ status. Writing "1" or VBUS turn to normal will clear it.	RW	0

REG 4BH: IRQ Status4

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	PWRON short press IRQ status. Writing 1 to this bit, or system shutdown will clear it	RW	0
6	PWRON long press IRQ status. Writing 1 to this bit, or system shutdown will clear it	RW	0
5	PWRON negative edge IRQ status. Writing 1 to this bit , or system shutdown will clear it.	RW	0
4	PWRON positive edge IRQ status. Writing 1 to this bit, or system shutdown , or QON negative will clear it.	RW	0
3	GPADC over temperature IRQ status. Writing 1 to this bit, or temperature go to normal will clear it.	RW	0
2	Quit GPADC over temperature IRQ status. Writing 1 to this bit, or Battery temperature rise to over temperature will clear it.	RW	0
1	GPADC under temperature IRQ status. Writing 1 to this bit, or temperature go	RW	0

	to normal will clear it.		
0	Quit GPADC under temperature IRQ status. Writing 1 to this bit, or temperature drop to under temperature will clear it.	RW	0

REG 4CH: IRQ Status5

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Charger begin charging IRQ status. Writing 1 to this bit, or charger charge done, or charging stop will clear it.	RW	0
6	Battery charge done IRQ status. Writing 1 to this bit, or charger charging will clear it.	RW	0
5	BC1.2 detect finished IRQ status. Writing 1 to this bit , or VBUS remove , or bc1.2 detect again will clear it.	RW	0
4	BC1.2 detect result change IRQ status. Writing 1 to this bit , or VBUS remove will clear it.	RW	0
3	RID detect result change IRQ status. Writing 1 to this bit will clear it.	RW	0
2	BAT over voltage protection IRQ status. Writing "1" or VBAT turn to normal will clear it.	RW	0
1-0	Reserved	R	0

REG 4DH: IRQ Status6

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Type-C device removed (unattached) IRQ status. Writing 1 to this bit , or type C insert will clear it.	RW	0
6	Type-C device insert and detection finished IRQ status. Writing 1 to this bit , or type C remove will clear it.	RW	0
5-3	Reserved	R	0
2	Type-C error generated IRQ status. Writing 1 to this bit will clear it.	RW	0
1	Type-C power state changed IRQ status. Writing 1 to this bit will clear it.	RW	0
0	Reserved	R	0

REG 56H: BMU Internal temperature ADC data, high 8 bits

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	BMU Internal temperature ADC data high 8 bits	RW	0

REG 57H: BMU Internal temperature ADC data, low 4 bits

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default

7-0	BMU Internal temperature ADC data low 4 bits (Unit: 0.10625℃， temp=-267.7℃+0.10625℃*xxxH)	RW	0

REG 58H: Ts pin ADC data, high 8bits

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Ts pin ADC data high 8bits	RW	0

REG 59H: Ts pin ADC data, low 4 bits

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Ts pin ADC data low 4 bits (Unit: 0.8mV)	RW	0

REG 5AH: GPADC pin ADC data, high 8bits

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	GPADC pin ADC data high 8bits	RW	0

REG 5BH: GPADC pin ADC data, low 4 bits

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	GPADC pin ADC data low 4 bits (Unit: 0.8mV)	RW	0

REG 78H: Average data bit[11:4] for Battery voltage

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery voltage	RW	0

REG 79H: Average data bit[3:0] for Battery voltage

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Average data bit[3:0] for Battery voltage (Unit: 1.2mV)	RW	0

REG 7AH: Average data bit[11:4] for Battery charge current

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery charge current	RW	0

REG 7BH: Average data bit[3:0] for Battery charge current

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Average data bit[3:0] for Battery charge current (Unit:2mA)	RW	0

REG 7CH: Average data bit[11:4] for Battery discharge current

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery discharge current	RW	0

REG 7DH: Average data bit[3:0] for Battery discharge current

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Average data bit[3:0] for Battery discharge current (Unit:2mA)	RW	0

REG 80H: ADC Enable

Default: F2H

Reset: power on reset

Bit	Description	R/W	Default
7	Die temperature measure ADC channel enable 0: disable 1: enable	RW	1
6	BATFET current measure ADC channel enable 0: disable 1: enable	RW	1
5	TS pin voltage measure ADC channel enable 0: disable 1: enable	RW	1
4	battery voltage measure ADC channel enable 0: disable 1: enable	RW	1
3-2	Reserved	R	0
1	BATFET discharge current measure ADC channel enable 0: disable 1: enable	RW	1
0	GPADC pin voltage measure ADC channel enable 0: disable 1: enable	RW	0

REG 81H: TS pin CTRL & ADC speed setting & GPADC mode CTRL

Default: 0CH

Reset: power on reset

Bit	Description	R/W	Default
7	TS PIN function select: 0 : TS pin is the battery temperature sensor input and will affect the charger 1 : TS pin is the external input for ADC and doesn't affect the charger	RW	0
6-5	ADC conversion clock selection 00: 100Hz 01: 200Hz 10: 400Hz 11: 800Hz	RW	00
4-3	TS current source on/off enable bit 00: off 01: always on when TS input ADC is enabled, not affected by ADC phase or charger 10: on in the ADC phase and off when ADC is off 11: always on	RW	01
2-1	current source to TS pin setting 00: 20uA 01: 40uA 10: 60uA 11: 80uA	RW	10
0	GPADC work mode: 0: output current 1:not output current	RW	0

REG 82H: TS/GPADC_HYSL2H setting

Default: 18H

Reset: power on reset

Bit	Description		R/W	Default
7-0	TS/GPADC_HYSL2H setting, M	hysteresis set for TS from low temperature go to normal, M*10H*0.8mV,default 307.2mV, ADC data 18h	RW	18H

REG 83H: TS/GPADC_HYSH2L setting

Default: 04H

Reset: power on reset

Bit	Description		R/W	Default
7-0	TS/GPADC_HYSH2L setting, M	hysteresis set for TS from high temperature go to normal, M*10H*0.8mV,default 51.2mV, ADC data 04h	RW	04H

REG 84H: VLTF_CHG setting

Default: 74H

Reset: power on reset

Bit	Description		R/W	Default
7-0	VLTF_CHG setting, M	VLTF setting, M*10H*0.8mV, M=74h when VTS=1.485V(about 0deg)	RW	74H

REG 85H: VHTF_CHG setting

Default: 17H

Reset: power on reset

Bit	Description		R/W	Default
7-0	VHTF_CHG setting, M	VHTF setting, M*10H*0.8mV, M=17h when VTS=0.294V(about 45deg)	RW	17H

REG 86H: VLTF_WORK setting

Default: BDH

Reset: power on reset

Bit	Description		R/W	Default
7-0	VLTF_WORK setting, M	VLTF setting, M*10H*0.8mV, M=BDh when VTS=2.419V(about -10deg)	RW	BDH

REG 87H: VHTF_WORK setting

Default: 11H

Reset: power on reset

Bit	Description		R/W	Default
7-0	VHTF_WORK setting, M	VHTF setting, M*10H*0.8mV, M=11h when VTS=0.218V(about 55deg)	RW	11H

REG 88H: VLTF_GPADC setting

Default: BDH

Reset: power on reset

Bit	Description		R/W	Default
7-0	VLTF_GPAD setting, M	VLTF_GPADC, M*10H*0.8mV,M=BDh when VTS=2.419V(about -10deg)	RW	BDH

REG 89H: VHTF_GPADC setting

Default: 0EH

Reset: power on reset

Bit	Description		R/W	Default
7-0	VHTF_GPADC setting, M	VHTF_GPADC, M*10H*0.8mV, M=0Eh when VTS=0.179V(about 60deg)	RW	0EH

REG 8AH: Charger control1

Default: 82H

Reset: bit[7] is system reset, others are power on reset

Bit	Description	R/W	Default
7	Charger enable configuration	RW	1

	0: charge disable 1: charge enable		
6-5	charge mode frequency selection 00: 1.5MHz 01: 1.0MHz 10: 2.5MHz 11: 2.0MHz	RW	00
4-1	Pre_charge current limit offset:64mA range: 64mA--1024mA default:128mA step: 64mA	RW	0001
0	Reserved	R	0

REG 8BH: Charger control2

Default: 10H

Reset: power on reset

Bit	Description	R/W	Default
7	Reserved	R	0
6	After charge done, then enter 10mA current charge process. 0:disable 1:enable	RW	0
5-0	Fast charge current limit offset: 0mA range: 0mA(000000)--3072mA(101111) default: 1024mA(010000) step: 64mA note: ICHG=000000(0mA) disables charge ICHG>101111(3072mA)is clamped to register value 101111(3072mA)	RW	010000

REG 8CH: Charger control3

Default: 6AH

Reset: power on reset

Bit	Description	R/W	Default
7-2	Charge voltage limit offset:3.840V range:3.840V--4.608V(110000) default:4.256V(011010) step: 16mV note: VREG>110000(4.608V)is clamped to register value 110000(4.608V)	RW	011010
1	battery pre_charge to fast charge threshold 0: 2.8V 1: 3.0V(default)	RW	1

0	battery recharge threshold offset(below charge voltage limit) 0: 100mV(VRECHG)below VREG(REG8C[7:2]) 1: 200mV(VRECHG)below VREG(REG8C[7:2])	RW	0

REG 8DH: Charger control4

Default: 8DH

Reset: bit[6-3] are power on reset, others are system reset

Bit	Description	R/W	Default
7	Charging termination enable 0: disable 1: enable	RW	1
6-3	Termination current limit offset:64mA range: 64mA--1024mA default:128mA(0001) step: 64mA	RW	0001
2-1	Timer 2 setting 00: 5hrs 01: 8hrs 10: 12hrs 11: 20hrs	RW	10
0	Safety timer2 enable 0: disable 1: enable	RW	1

REG 8EH: Charger control5

Default: B8H

Reset: bit[1-0] are power on reset, others are system reset

Bit	Description	R/W	Default
7	pre_charger safe timer enable 0: timer disabled 1: timer enabled	RW	1
6-5	pre_charger timer setting 00: 40min 01: 50min 10: 60min 11: 70min	RW	01
4	safety timer1/2 setting during DPM or thermal regulation 0: safety timer not showed during input DPM or thermal regulation 1: safety timer showed during input DPM or thermal regulation	RW	1
3	battery detection enable 0: disable battery detection function 1: enable battery detection function	RW	1
2	Battery Load($I_{batload}$)enable	RW	0

	0: Disabled 1: Enabled		
1	Battery detection charge/discharge current time: 0: 1s 1:128ms	RW	0
0	Reserved	R	0

REG 90H: CHGLED pin function setting

Default: 00H

Reset: bit[2-0] are power on reset, others are system reset

Bit	Description	R/W	Default
7	CHGLED pin disable 0: enable CHGLED pin function 1: disable CHGLED pin function	RW	0
6	Breath and PWM function enable control when reg90[2:0] is set to 011 or 101 0 : disable 1 : enable	RW	0
5-3	CHGLED pin output when reg90[2:0] is set to 110-111; 000 : Hiz; 001 : high level 25% duty 1Hz; 010 : high level 25% duty 4Hz; 011 : drive low; 100 : drive high; 101-111 : Hiz.	RW	000
2-0	CHGLED pin display function setting 000 : display with type A function, OD; 001 : display with type B function, OD; 010 : display with breath function controlled by charger, OD; 011 : display with breath function not controlled by charger, OD; 100 : display with three state(low/high/Hiz) controlled by charger, Push Pull; 101 : display with PWM function, PushPull; 110-111 : output controlled by reg90[5:3], PushPull.	RW	000

REG 91H: Breath function control1

Default: 64H

Reset: power on reset

Bit	Description	R/W	Default
7-0	CL (the time unit count set for breath function stay in DMIN, the time unit is TUL.) So, TL = CL*TUL, TL should larger than PWM period, and default is 1.6s.	RW	64H

REG 92H: Breath function control2

Default: 01H

Reset: power on reset

Bit	Description	R/W	Default
7-0	CSR (the time unit count set for breath function stay in every step from DMIN rise to DMAX, the time unit is TUS.) So, TSR = TUS*CSR , TSR should larger than PWM period, and default is 16ms. And the total rise time, TR = TSR * NC, default is 1.6s.	RW	01H

REG 93H: Breath function control3

Default: 06H

Reset: power on reset

Bit	Description	R/W	Default
7-0	CH (the time unit count set for breath function stay in DMAX,the time unit is TUH.) So, TH = CH*TUH, TL should larger than PWM period, and default is 96ms.	RW	06H

REG 94H: Breath function control4

Default: 01H

Reset: power on reset

Bit	Description	R/W	Default
7-0	CSF (the time unit count set for breath function stay in every step from DMAX fall to DMIN, the time unit is TUS.) So, TSF =TUS*CSF, TSF should larger than PWM period, and default is 16ms. And the total rise time, TF = TSF * NC, default is 1.6s.	RW	01H

REG 95H: Breath function control5

Default: 64H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Breath function total duty step count setting between DMIN and DMAX, NS. So, the breath Maximal duty(DMAX) is (NMIN+NS)/M, default is 100%. Note: (NMIN+NS) <= M	RW	64H

REG 96H: Breath function control6

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	For breath function Minimal duty setting, NMIN (the high level clock number in every PWM period, the clock frequency is f0). So, the breath Minimal duty(DMIN) is NMIN/M, default is 0%.	RW	00H

REG 97H: Breath function control7

Default: 64H

Reset: power on reset

Bit	Description	R/W	Default

7-0	M(the total clock number in every PWM output period, the clock frequency is f0). So f_{PWM}(the PWM output frequency) is f0/M, default is 5KHz.	RW	64H

REG 98H: Breath function control7 & Input clock frequency for PWM output

Default: 16H

Reset: power on reset

Bit	Description	R/W	Default
7	The CHGLED pin breath step time and the stay high time unit setting selection 0 : the time unit setting by REG98[3:0]; 1 : the time unit setting by REG9A.	RW	0
6-4	f0 (The input clock frequency) setting for PWM output 000 : 1MHz 001 :500KHz 010 : 250KHz 011 : 125KHz 100 : 62.5KHz 101 : 31.2KHz 110 :15.6KHz 111 : 7.8KHz		001
3-0	The CHGLED pin breath time unit for stay at DMIN/DMAX, or every change step between DMIN and DMAX. TUL = TUH = TUS = 2^(n-2) ms, default is 16ms; n <= 8;		0110

REG 99H: PWM function duty setting

Default: 32H

Reset: power on reset

Bit	Description	R/W	Default
7-0	For PWM function duty setting, NPWM (the high level clock number in every PWM period, the clock frequency is f0). So, the PWM function duty DPWM = NPWM/M, default is 50%. Note: NPWM <= M	RW	32H

REG 9AH: CHGLED breath time unit option

Default: 65H

Reset: power on reset

Bit	Description	R/W	Default
7-4	The CHGLED breath time unit option for stay at DMAX; TUH = 2^(n-2) ms; n <= 8;	RW	0110
3-0	The CHGLED breath time unit option for every rise or fall step time; TUS = 2^(n-2) ms; n <= 8;	RW	0101

REG B8H: Fuel Gauge Control

Default: C0H

Reset: power on reset

Bit	Description	R/W	Default
7	Fuel gauge enable control(including OCV and coulombmeter) 0 : disable 1 : enable	RW	1
6	Coulombmeter enable control 0 : disable 1 : enable	RW	1
5	Battery maximum capacity calibration enable control	RW	0

	0 : disable 1 : enable		
4	Battery maximum capacity calibration status 0: not calibrating 1: is calibrating	R	0
3-2	Reserved	R	0
1	Old coulombmeter enable control 0 : disable 1 : enable	RW	0
0	Old coulombmeter clear control 0 : Write 0 to this bit will do nothing 1 : Write 1 to this bit will clear old coulombmeter and then this bit will be cleared automatically	RW	0

REG B9H: Battery capacity percentage for indication

Default: 64H

Reset: power on reset

Bit	Description	R/W	Default
7	Indicating if battery capacity percentage for indication is valid: 0 : is not valid 1 : is valid	R	0
6-0	Battery capacity percentage for indication	R	64H

REG BAH: RDC 1

Default: 80H

Reset: power on reset

Bit	Description	R/W	Default
7	RDC calculation control 0 : disable 1 : enable	RW	1
6	RDC was right detected or not flag: 1: Yes 0: Not	RW	0
5	Reserved	R	0
4-0	RDC value high 5 bits (Unit:1.17mΩ)	RW	00000

REG BBH: RDC 0

Default: 55H

Reset: power on reset

Bit	Description	R/W	Default
7-0	RDC value low 8 bits (Unit:1.17mΩ)	RW	55H

REG BCH: OCV 1

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	OCV value high 8 bits	R	00H

REG BDH: OCV 0

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-4	Reserved	R	0
3-0	OCV value low 4 bits	R	0000

REG C0H~DFH: OCV percentage table

REG E0H: Battery maximum capacity

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Indicating if battery maximum capacity is valid 0 : Not valid 1 : Is valid	RW	0
6-0	Battery maximum capacity bit[14:8]	RW	00H

REG E1H: Battery maximum capacity

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	battery maximum capacity bit[7:0](Unit: 1.456mAh)	RW	00H

REG E2H: Coulomb meter counter

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Indicating if coulombmeter counter is valid 0 : Not valid 1 : Is valid	RW	0
6-0	Coulombmeter counter[14:8]	RW	00H

REG E3H: Coulomb meter counter

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-0	Coulombmeter counter[7:0] (Unit: 1.456mAh)	RW	00H

REG E4H: OCV Percentage of battery capacity

Default: 64H

Reset: power on reset

Bit	Description	R/W	Default
7	Indicating if OCV percentage of battery capacity is valid 0 : Not valid 1 : Is valid	R	0
6-0	OCV percentage of battery capacity	R	64H

REG E5H: Coulombmeter percentage of battery capacity

Default: 64H

Reset: power on reset

Bit	Description	R/W	Default
7	Indicating if coulombmeter percentage of battery capacity is valid: 0 : Not valid 1 : Is valid	R	0
6-0	Coulombmeter percentage of battery capacity	R	64H

REG E6H: Battery capacity percentage warning level

Default: A0H

Reset: power on reset

Bit	Description	R/W	Default
7-4	Warning level 1: Warning threshold, 5-20%, 1% per step	RW	1010
3-0	Warning level 2: Shutting down threshold, 0-15%, 1% per step	RW	0000

REG E7H: OCV_SOC curve setting

Default: 0FH

Reset: power on reset

Bit	Description	R/W	Default
7-5	Reserved	R	0
4	The battery voltage limit control bit in the battery internal resistor calculation stop charge status. 0 : no limit 1 : limit as the charge status(setting in regEC[4:3])	RW	0
3-0	The OCV VS Battery SOC curve setting 0000 : Selection the charge voltage target 4.10V curve. 0001 : Selection the charge voltage target 4.15V curve. 0010 : Selection the charge voltage target 4.20V curve. 0011 : Selection the charge voltage target 4.25V curve. 0100 : Selection the charge voltage target 4.35V curve. 0101 : Selection the charge voltage target 4.40V curve. 0110 : Selection the charge voltage target 4.45V curve. 0111 : Selection the charge voltage target 4.50V curve. 1000 : Selection the charge voltage target 4.60V curve. 1001 ~1111 : Depend on the charge voltage target setting Vtarget <= 4.112V Selection the charge voltage target 4.10V curve. 4.112V <Vtarget <= 4.160V,Selection the charge voltage target 4.15V curve. 4.160V <Vtarget <= 4.208V,Selection the charge voltage target 4.20V curve. 4.208V <Vtarget <= 4.256V,Selection the charge voltage target 4.25V curve. 4.256V <Vtarget <= 4.352V,Selection the charge voltage target 4.35V curve. 4.352V <Vtarget <= 4.416V,Selection the charge voltage target 4.40V curve. 4.416V <Vtarget <= 4.464V,Selection the charge voltage target 4.45V curve. 4.464V <Vtarget <= 4.512V,Selection the charge voltage target 4.50V curve.	RW	1111

	4.512V <Vtarget Selection the charge voltage target 4.60V curve.		

REG E8H: Fuel gauge tuning control 0

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	When the available signal of external power supply is changed or not, reset ADC filter or not 0: Yes, reset the ADC filter 1: No	RW	0
6	When the charging circuit on or off, reset ADC filter or not 0: Yes, reset the ADC filter 1: No	RW	0
5	When the battery voltage ADC channels open or closed, reset ADC filter or not 0: Yes, reset the ADC filter 1: No	RW	0
4	When the battery rechargeable battery ADC channels open or closed, reset ADC filter or not 0: Yes, reset the ADC filter 1: No	RW	0
3	When the battery discharge current ADC channels open or closed, reset ADC filter or not 0: Yes, reset the ADC filter 1: No	RW	0
2-0	Battery capacity percentage for indication update minimum interval 000: 30s 001: 60s 010: 120s 011: 164s 100: immediately update when changed 101: 5s 110: 10s 111: 20s	RW	000

REG E9H: Fuel gauge tuning control 1

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-6	OCV Percentage calibrate the Coulomb meter percentage, maximum time interval 00: 60s 01: 120s 10: 15s	RW	00

	11: 30s		
5-3	Wait for the stability for charge when in RDC calculation 000: 180s 001: 240s 010: 300s 011: 600s 100: 30s 101: 60s 110: 90s 111: 120s	RW	000
2-0	Wait for the stability for discharge when in RDC calculation 000: 180s 001: 240s 010: 300s 011: 600s 100: 30s 101: 60s 110: 90s 111: 120s	RW	000

REG EAH: Fuel gauge tuning control 2

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7-6	OCV Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00: 4 01: 8 10: 1 11: 2	RW	00
5-4	Coulomb meter Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00: 4 01: 8 10: 1 11: 2	RW	00
3	Battery maximum capacity and OCV-SoC curve calibration start condition: 0: OCV percentage < (REG E6H[3:0] + 3) 1: OCV percentage < (REG E6H[3:0] + 6)	RW	0
2	Battery maximum capacity calibration end condition 0 0: OCV percentage ≥ 95% 1: OCV percentage = 100%	RW	0

1	Battery maximum capacity calibration end condition 1 0: wait for charge finished 1: do not wait for charge finished	RW	0
0	Battery maximum capacity calibration end condition 2 (wait N ms for the charge finished indication signal after REG 01H[6] clear to 0,N: 0: 68 1: 120	RW	0

REG EBH: Fuel gauge tuning control 3

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	When charge status bit REG 01H[6] = 1,the percentage of indication can be decrease or not 0: decrease enable 1: decrease disable	RW	0
6-4	When REG 01H[6] = 1， percentage of indication decrease hysteresis(N) setting 000: 4% 001: 5% 010: 6% 011: 7% 100: 0% 101: 1% 110: 2% 111: 3%	RW	000
3	Calculation RDC current condition setting 0: ≥300mA 1: ≥150mA	RW	0
2-0	Calibrate RDC percentage changed threshold setting 000: 4% 001: 5% 010: 6% 011: 7% 100: 0% 101: 1% 110: 2% 111: 3% calibration： △OCVPCT > N	RW	000

REG ECH: Fuel gauge tuning control 4

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default

7-5	Reserved	R	0
4-3	The minimum battery voltage for RDC calculation 00: 3.5V 01: 3.6V 10: 3.7V 11: 3.4V	RW	00
2-0	Coulomb counter calibration threshold， relative with REG_E6_[3:0] 000: REG_E6H[3:0]+7(default) 001: REG_E6H[3:0]+8 010: REG_E6H[3:0]+9 011: REG_E6H[3:0]+10 100: REG_E6H[3:0]+3 101: REG_E6H[3:0]+4 110: REG_E6H[3:0]+5 111: REG_E6H[3:0]+6	RW	000

REG EDH: Fuel gauge tuning control 5

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	OCV percentage relative with the charge/discharge rate control 0: Disable 1: Enable	RW	0
6	Update time when rate > 0.5C 0: 30S 1: 15S	RW	0
5-4	Update time when rate < 0.5C and rate > 0.1C 00: 60S 01: 75S 10: 30S 11: 45S	RW	00
3-2	Update time when rate < 0.1C 00: 120S 01: 180S 10: 240S 11: 60S	RW	00
1-0	Fixed update time 00: 30S 01: 45S 10: 60S 11: 15S	RW	00

REG EEH: Fuel gauge tuning control 6

Default: 01H

Reset: power on reset

Bit	Description	R/W	Default
7	OCV capacity curve and battery capacity calibration control in charge or discharge status 0: Charging calibration 1: Discharging calibration	RW	0
6-5	Reserved	R	0
4	The debounce number of battery OCV reached 0 0: 3 1:4	RW	0
3	Whether hold charge accumulation or regressive when Coulometer value in 100% or OCV in 0%, or OCV curve in calibration period 0: Normal accumulation or regressive 1: Hold, do not accumulation or regressive	RW	0
2	OCVPCT update control 0: Old ocvpct update which not depend on charge ratio 1: New ocvpct update which depend on charge ratio	RW	0
1-0	The OCV debounce time setting at every OCV level during the BMU doing OCV percent curve calibration 00: 2s 01: 4s 10: 6s 11: 8s	RW	01

REG EFH: Fuel gauge tuning control 7

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
7	Reserved	R	0
6	In the charging state, the smooth ocv-percentage less than coulomb calibration threshold and the instantaneous ocv-percentage equal 0%, then it will clear the coulomb counter or not. 0 : clear the coulomb 1 : not clear the coulomb	RW	0
5	The battery total calibration has completely and the ocv percent calibration doesn't complete , the ocv percent calibration processing will stop or not. 0 : stop 1 : don't stop	RW	0
4	The indication of battery charge percentage can go to 100% or not before charge done 0 : disable 1 : enable	RW	0
3	Reserved	R	0
2	The battery charge percent for ocv percent curve calibration selection. 0 : the instantaneous charge percent 1 : the smooth charge percent	RW	0
1	The battery charge percent for battery capacity calibration selection.	RW	0

	0 : the instantaneous charge percent 1 : the smooth charge percent		
0	The battery charge percent for the battery discharge ocv percent curve and capacity calibration start. 0 : must equal 100% 1 : no limit	RW	0

8. Application Information

8.1 Charger

1. A 10mohm resistor is used to sample current. Accuracy of the resistor is 1% at least.
2. 1uF capacitor parallel with the sampling resistor can not be omitted, and must be close to the resistor in layout.
3. BATSENSP and BATSENSN should be differential lines to avoid interference.
4. TS pin is used to detect battery temperature. It is recommended to use 10K NTC resistor. If TS pin is not used, the function can be disabled by software.
5. CHGLED pin is used to indicate charging status. If CHGLED is set to be push-pull output, just connect indicator light between this pin and GND. If CHGLED is set to be open drain output, connect indicator light between this pin and VBUS by a pull-up resistor. If CHGLED pin is not used, it just stays floating.
6. Use 1uH inductor. Its saturation current should be 50% higher than the setting value and its internal resistance should be less than 30mohm.
7. Place battery to BAT connection points as close as possible to reduce wire length. Use thick line to reduce line impedance and voltage drop.

8.2 BUCK/LDO

1. Connect two 22uF capacitors to VSYS pin.
2. Output capacitance of LDO is not smaller than 4.7uF.
3. Input capacitance of VBUS is not smaller than 10uF.
4. Layout: Inductor is close to BMU, output capacitors are close to inductors and input capacitors are close to input pin of BMU.

8.3 BOOST

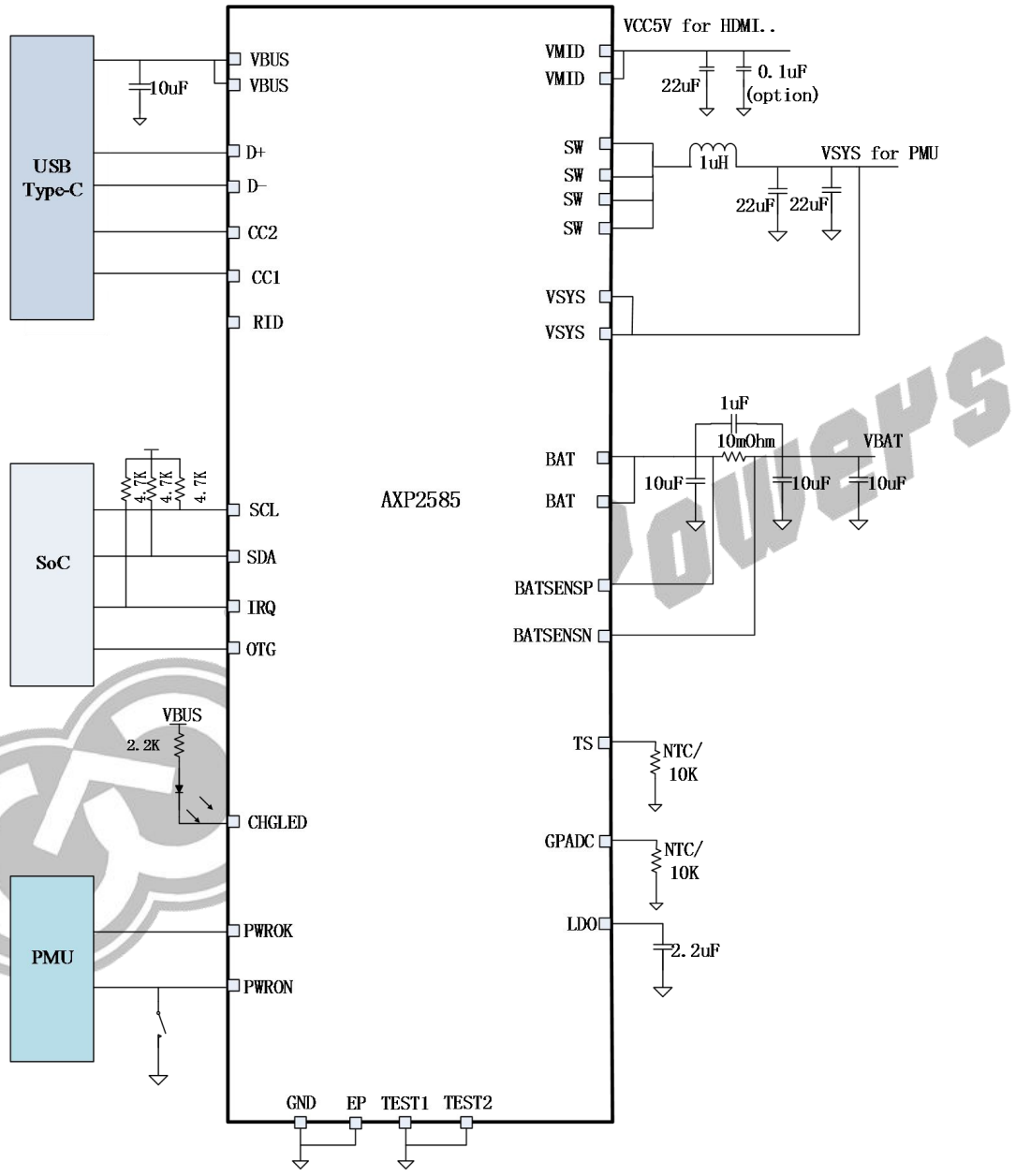
1. If only battery is present and V_{BAT} is higher than depletion threshold(V_{BAT_DPLZ}), BATFET, connecting battery to system, is off by default and need to be turned on by pressing the PWRON key.
2. If only battery is present and BATFET is on, the output voltage of VMID has two possibilities:(1) BOOST enable. In BOOST mode, the output voltage of VMID is 5V by default. (2)BOOST disable. Because of the HS-MOS body diode, the output voltage of VMID is equal to the result of the subtraction of VSYS and Vdiode. The BOOST mode can be enabled or disabled by Host.
3. In BOOST mode, OTG pin must be high.
4. Connect a 22uF capacitor to VMID pin.
5. When BMU is powered by battery, if the insertion of OTG device is detected through RID pin(USB2.0) or CC pin(type-c), BOOST mode will be enabled automatically and RBFET is turned on to supply power to VBUS. The whole process can be controlled by Host.
6. if the removal of OTG device is detected through RID pin(USB2.0) or CC pin(type-c), RBFET will be turned off

automatically, and whether to disable boost mode depends on application scenarios. The whole process can be controlled by Host.

8.4 IO

1. TWSI: Pull up SDA/SCK to a source, such as LDO.
2. Pull up IRQ with a 4.7kΩ resistor to a source, such as LDO.
3. When operating with PMIC, the PWROK pin of AXP2585 is connected to the PWROK signal of PMIC to detect the PMIC's power on/off status.
4. Connect the PWRON key between PWRON pin and GND directly.
5. As a general purpose ADC input pin, GPADC pin can be used to detect board-level temperature. Its circuit implementation is the same as that of TS pin.
6. If connected to Host, DP/DM should be differential lines and a impedance matching is needed.

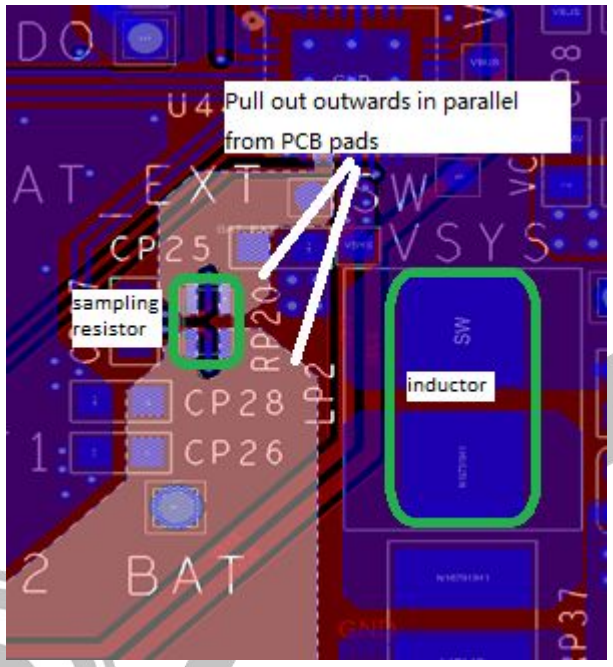
8.5 Typical Application



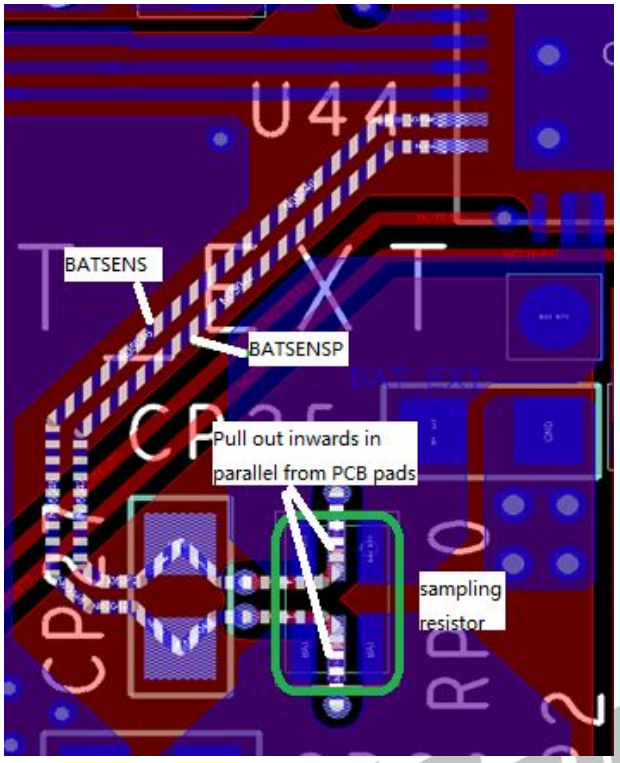
9. PCB Layout Guideline

9.1 Charging and Discharging Part

1、BAT charging path: VBUS->VMID->SW->inductor->VSYS->sampling resistor->battery, line width>=200mil; BAT discharging path: battery->sampling resistor->VSYS->inductor->SW->VMID, line width>=200mil. Lead wire of sampling resistor must be pulled out outwards in parallel from PCB pads. Place battery to BMU as close as possible, as shown in the following figure.



2、Wire between BATSENSN/BATSENSP and sampling resistor uses 8-10mil. Lead wire of sampling resistor must be pulled out inwards in parallel from PCB pads, as shown in the following figure.



9.2 High Current Path

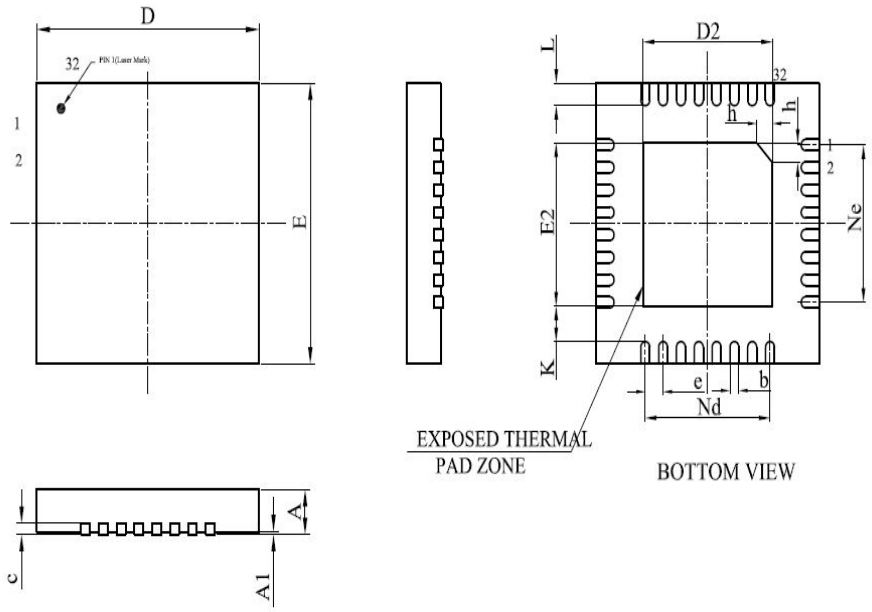
Line width of high current path such as power input and output need to be widened to reduce line impedance, voltage drop and loss.

1. Line width of VBUS, VSYS,VMID: >=200mil；
2. Line width of LDO output depends on load current.
3. Place battery to BAT connection points as close as possible to reduce wire length. Use thick line to reduce line impedance and voltage drop.

10. Package and Ordering Information

10.1 Package Information

AXP2585 package is QFN5*5, 32-pin. Figure 10-1 shows AXP2585 package.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	2.80	2.90	3.00
e	0.40BSC		
Nd	2.80BSC		
E	4.90	5.00	5.10
E2	2.80	2.90	3.00
Ne	2.80BSC		
L	0.35	0.40	0.45
K	0.20	--	--
h	0.30	0.35	0.40
载体尺寸 (Mil)	150*150		

Figure 10-1 Package Information

10.2 Marking information

Figure 10-2 shows AXP2585 marking.

Figure 10-2 AXP2585 Marking

Table 10-1 describes AXP2585 marking information.

Table 10-1 AXP2585 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP2585	Product name	Fixed
2	LLLLLCB	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

10.3 Carrier

Table 10-2 shows AXP2585 tray carrier information

Table 10-2 Tray Carrier Information

Item	Color	Size
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm
Pearl cotton cushion (The Gap between vacuum bag and inside box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm
Inside Box	White	396mm x 196mm x 96mm
Outside Box	White	420mm x 410mm x 320mm

Figure 10-3 shows tray dimension drawing of AXP2585.

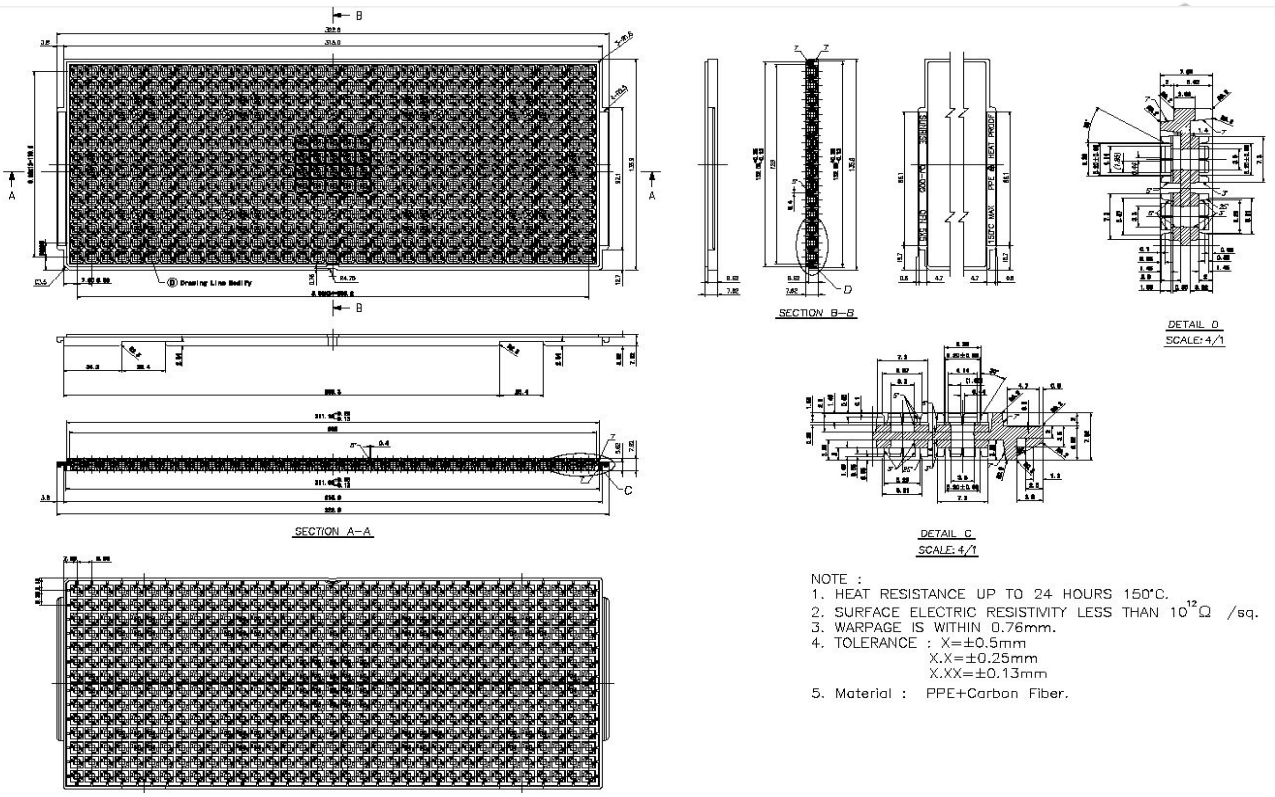


Figure 10-3 Tray Dimension Drawing

Table 10-3 shows AXP2585 packing quantity.

Table 10-3 Packing Quantity Information

Type	Quantity	Part Number
Tray	490pcs/Tray 10Trays/package	AXP2585

10.4 Storage

10.4.1 Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in

Table 10-4.

Table 10-4 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30℃/85%RH
2	1 year	≤30℃/60%RH
2a	4 weeks	≤30℃/60%RH
3	168 hours	≤30℃/60%RH
4	72 hours	≤30℃/60%RH
5	48 hours	≤30℃/60%RH
5a	24 hours	≤30℃/60%RH
6	Time on Label(TOL)	≤30℃/60%RH

AXP2585 device samples are classified as MSL3.

10.4.2 Bagged Storage Conditions

The shelf life of AXP2585 are defined in Table 10-5.

Table 10-5

Packing mode	Vacuum packing
Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Shelf life	6 months

10.4.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP2585 is as follows.

Table 10-6 Out-of-bag Duration

Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

10.5 Baking

It is not necessary to bake AXP2585 if the conditions specified in Section 10.4.2 and Section 10.4.3 have not been exceeded. It is necessary to bake AXP2585 if any condition specified in Section 10.4.2 and Section 10.4.3 have been exceeded.

It is necessary to bake AXP2585 if the storage humidity condition has been exceeded. We recommend that the device sample removed from its vacuum bag more than 2 days should be baked to guarantee production.

Table 10-7 Baking Conditions

Surrounding	Bake@125℃	Note
Nitrogen	8 hours	Recommended condition. Not exceed 3 times.
Air	2 hours	Acceptable condition. Not exceed 3 times.
CAUTION： If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature		

11. Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

Figure 11-1 shows the typical reflow profile of AXP2585 device sample.

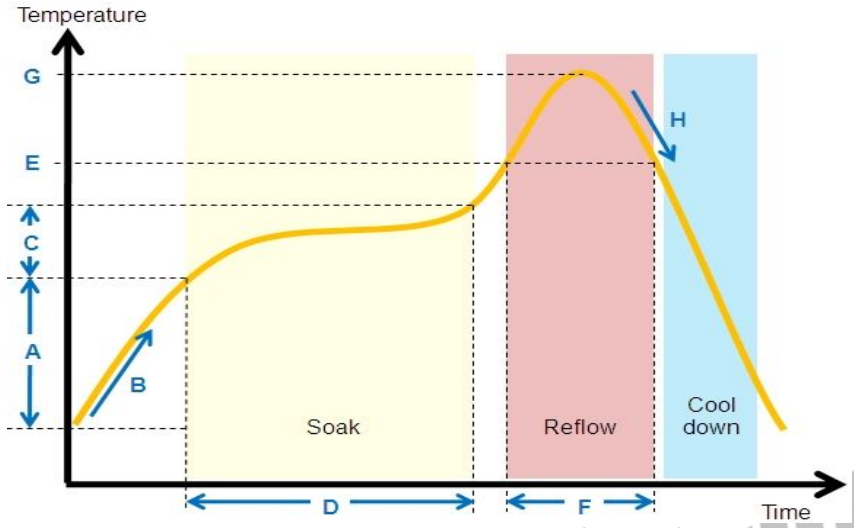


Figure 11-1 AXP2585 Typical Reflow Profile

Reflow profile conditions of AXP2585 device sample is given in Table 11-1.

Table 11-1 AXP2585 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25℃ -> 150℃
B	Preheat ramp up rate	1.5~2.5 ℃/sec
C	Soak temperature range	150℃ -> 190℃
D	Soak time	80~110 sec
E	Liquidus temperature	217℃
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250℃
H	Cool down temperature rate	≤4℃/sec

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