H133
Low Cost 4K Decoding Open Platform

Features

- Dual-core ARM Cortex™-A7
- Memories
  - Three SD/MMC host controller (SMHC) interfaces: SD3.0/SDIO3.0/eMMC5.0
  - DDR2/DDR3 SDRAM
- Video Engine
  - H.265/H.264/H.263/MPEG-1/2/4/JPEG/Xvid/Sorenson Spark decoding, up to 4K@30fps
  - JPEG/MJPEG encoding, up to 1080p@60fps
- Video and Graphics
  - Allwinner SmartColor2.0 post processing for an excellent display experience
  - Supports de-interlacer (DI) up to 1080p@60fps
  - Supports Graphic 2D (G2D) hardware accelerator including rotate, mixer, LBC decompression functions
- Video Output
  - Single link LVDS interface up to 1366 x 768@60fps
  - 4-lane MIPI DSI up to 1920 x 1200@60fps
  - HDMI V1.4 output interface up to 4K@30fps
- Analog Audio Codec
  - 2 DACs
  - Analog audio interfaces: HPOUTL/R
- Two I2S/PCM external interfaces (I2S1, I2S2)
- Maximum 8 digital PDM microphones (DMIC)
- OWA TX, compliance with S/PDIF interface
- Security System
  - AES, DES, 3DES, RSA, MD5, SHA, HMAC
  - Integrated 2 Kbits OTP storage space
- External Peripherals
  - USB 2.0 DRD (USB0) and USB 2.0 HOST (USB1)
  - 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces
  - Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
  - Up to 2 SPI controllers (SPI0, SPI1)
  - Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
  - CIR RX and CIR TX
  - 8 independent PWM channels (PWM0 to PWM7)
  - 1-ch GPADC
  - LEDC
- Package
  - LFBGA 196 balls, 10 mm x 10 mm body size, 0.65 mm ball pitch, 0.35 mm ball size

Revision History

Revision	Date	Author	Description
1.0	May 28, 2021	AWA0330	Initial release version
1.1	August 27, 2021	XRA0041	Refresh the specifications.
1.2	April 22, 2022	KPA0570	Update table 5-1, table 5-2, table 5-12, figure 5-24, table 5-29, section 2.8.4, figure 3-1, table 4-3, table 4-4, figure 5-26, table 5-33, section 2.3, table 5-1, table 5-2; delete table 5-3
1.3	September 20, 2022	KPA0570	**Chapter 5 Electrical Characteristics** Modified the section 5.11.1 EMAC AC Electrical Characteristics.

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package, and part reliability of the H133 processor. For details about register descriptions of each module, see the *H133_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	Indicates potential risk of injury or death exists if the instructions are not obeyed.
CAUTION	Indicates potential risk of equipment damage, data loss, performance degradation, or unexpected results exists if the instructions are not obeyed.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1 Overview

H133 is an advanced application processor designed for 4K decoding platform. It integrates the high-performance dual-core Cortex™-A7 to provide the most-efficient computing power. H133 supports full format decoding such as H.265, H.264, MPEG-1/2/4, JPEG, VC1, and so on. The independent encoder can encode in JPEG or MJPEG. Integrated multi ADCs/DACs and I2S/PCM/DMIC/OWA audio interfaces can work seamlessly with the CPU to accelerate multimedia algorithms and improve the user experience. H133 supports HDMI/LVDS/MIPI DSI display output interfaces to meet the requirements of the screen display. H133 comes with extensive connectivity and interfaces, such as USB, SDIO, EMAC, TWI, UART, SPI, PWM, GPADC, IR TX&RX, and so on. Besides, H133 can connect with other different peripherals like WiFi and BT via SDIO and UART.

2 Features

2.1 CPU Architecture

- Dual-core ARM Cortex™-A7
- 32 KB L1 I-cache + 32 KB L1 D-cache per core, 256 KB L2 cache

2.2 Memory Subsystem

2.2.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
  - SD card
  - eMMC
  - SPI NOR Flash
  - SPI NAND Flash
- Supports mandatory upgrade process through USB and SD card
- Supports GPIO pin and eFuse module to select the boot media type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Secure BROM ensures that the secure boot is a trusted environment

2.2.2 SDRAM

- Supports DDR2/DDR3 SDRAM
- Maximum capacity up to 2 GB
- Supports clock frequency up to 533 MHz for DDR2
- Supports clock frequency up to 800 MHz for DDR3

2.2.3 SMHC

- Three SD/MMC host controller (SMHC) interfaces
- The SMHC0 controls the devices that comply with the protocol Secure Digital Memory (SD mem-version 3.0)
- The SMHC1 controls the device that complies with the protocol Secure Digital I/O (SDIO-version 3.0)
- The SMHC2 controls the device that complies with the protocol Multimedia Card (eMMC-version 5.0)
- Maximum performance:
  - SDR mode 150 MHz@1.8 V IO pad

  - DDR mode 50 MHz@1.8 V IO pad
  - DDR mode 50 MHz@3.3 V IO pad
- Supports 1-bit or 4-bit data width
- Supports block size of 1 to 65535 bytes
- Internal 1024-Bytes RX FIFO and 1024-Bytes TX FIFO
- Supports card insertion and removal interrupt
- Supports hardware CRC generation and error detection
- Supports descriptor-based internal DMA controller

2.3 Video Engine

- Video decoding
  - H.265 MP@L5.0 up to 4K@30fps
  - H.264 BP/MP/HP@L5.0 up to 4K@24fps
  - H.263 BP up to 1080p@60fps
  - MPEG-4 SP/ASP L5.0 up to 1080p@60fps
  - MPEG-2 MP/HL up to 1080p@60fps
  - MPEG-1 MP/HL up to 1080p@60fps
  - JPEG/Xvid/Sorenson Spark up to 1080p@60fps
  - MJPEG up to 1080p@30fps
- Video encoding
  - JPEG/MJPEG up to 1080p@60fps
  - Supports input picture scaler up/down

2.4 Video and Graphics

2.4.1 Display Engine (DE)

- Output size up to 2048 x 2048
- Supports two alpha blending channels for main display and one channel for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports LBC buffer decoder
- Supports dither output to TCON
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565/palette
- Supports SmartColor2.0 for excellent display experience

  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports write back for aux display

2.4.2 De-interlacer (DI)

- Supports YUV420 (Planar/NV12/NV21) and YUV422 (Planar/NV16/NV61) data format
- Supports video resolution from 32x32 to 2048x1280 pixel
- Supports Inter-field interpolation/motion adaptive de-interlace method
- Performance: module clock 600M for 1080p@60Hz YUV420

2.4.3 Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer
- Supports horizontal flip, clockwise 0/90/270 degree rotate for LBC buffer

2.5 Video Output

2.5.1 LVDS LCD

- Supports LVDS interface with single link, up to 1366 x 768@60fps

2.5.2 MIPI DSI

- Compliance with MIPI DSI v1.01

- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous lane clock modes
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes

2.5.3 HDMI

- Compatible with HDMI 1.4
- Supports DDC
- Integrated CEC hardware engine
- Optional color space converter (CSC): RGB (4:4:4) to/from YCbCr (4:4:4 or 4:2:2)
- Video formats:
  - Optional HDMI 1.4b video formats
  - All CEA-861-E video formats up to 1080p at 120 Hz
  - HDMI 1.4b 4K x 2K video formats
  - HDMI 1.4b 3D video modes with up to 340 MHz (TMDS clock)
- Audio formats:
  - Uncompressed audio formats: IEC60985 L-PCM audio samples, up to 192 kHz
  - Compressed audio formats: IEC61937 compressed audio, up to 768 kHz

2.6 System Peripherals

2.6.1 Timer

- The timer module implements the timing and counting functions, which includes timer0, timer1, watchdog, and audio video synchronization (AVS)
- The timer0/timer1 is a 32-bit down counter. The timer0 and timer1 are completely consistent
- The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system
- The AVS is used to synchronize the audio and video. The AVS sub-block includes AVS0 and AVS1, which are completely consistent

2.6.2 High Speed Timer (HSTimer)

- The HSTimer module consists of HSTimer0 and HSTimer1. HSTimer0 and HSTimer1 are down counters that implement timing and counting functions. They are completely consistent.

- Configurable 56-bit down timer
- Supports 5 prescale factors
- The clock source is synchronized with AHB0 clock, much more accurate than other timers
- Supports 2 working modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

2.6.3 GIC

- Supports 16 Software Generated Interrupts (SGIs), 16 Private Peripheral Interrupts (PPIs), and 192 Shared Peripheral Interrupts (SPIs)
- Software-configurable interrupts can be:
    - Enabled or disabled
    - Assigned to one of two groups: Group 0 or Group 1
    - Prioritized
    - Signaled to different processors in multiprocessor implementations
    - Either level-sensitive or edge-triggered
- GIC security extensions
    - Uses Group 0 interrupts as Secure interrupts, and Group 1 interrupts as Non-secure interrupts
    - Uses the FIQ interrupt request to signal Secure interrupts to a connected processor. The GIC-400 always signals Group 1 interrupts using the IRQ interrupt request

2.6.4 DMAC

- Up to 16-ch DMA
- Provides 32 peripheral DMA requests for data reading and 32 peripheral DMA requests for data writing
- Flexible data width of 8/16/32/64-bit
- Programmable DMA burst length
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transferring data with a linked list
- DRQ response includes waiting mode and handshake mode
- DMA channel supports pause function
- Memory devices support non-aligned transform

2.6.5 Clock Controller Unit (CCU)

- 8 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.6.6 Thermal Sensor Controller (THS)

- One thermal sensor located in CPU
- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

2.6.7 LDO Power

- Integrated 2 LDOs (LDOA, LDOB)
- LDOA: 1.8 V power output, LDOB: 1.35 V/1.5 V/1.8 V power output
- LDOA for IO and analog module, LDOB for SDRAM
- Input voltage is 2.4 V to 3.6 V

2.6.8 RTC

- Implements time counter and timing wakeup
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing power-off information

2.6.9 I/O Memory Management Unit (IOMMU)

- Supports virtual address to physical address mapping by hardware implementation
- Supports VE, DE, G2D, DI parallel address mapping
- Supports VE, DE, G2D, DI bypass function independently

- Supports VE, DE, G2D, DI pre-fetch independently
- Supports VE, DE, G2D, DI interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.6.10 Spinlock

- Provides hardware synchronization mechanism in multi-core systems
- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

2.7 Audio Subsystem

2.7.1 Audio Codec

- Two audio digital-to-analog converter (DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- One audio output:
  - One stereo headphone output: HPOUTL/R
- Supports Dynamic Range Controller adjusting the DAC playback
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA
- Internal HPLDO output for HPVCC
- Internal ALDO output for AVCC

2.7.2 I2S/PCM

- Two I2S/PCM external interfaces (I2S1, I2S2) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format

- Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

2.7.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.7.4 One Wire Audio (OWA)

- One OWA TX
- Compliance with S/PDIF interface
- IEC-60958 transmitter functionality
- Supports 16-bit, 20-bit, and 24-bit data formats
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Supports TX DMA slave interface
- Function clock includes 24.576 MHz and 22.579 MHz frequency
- Hardware parity generation on the transmitter
- Supports channel status insertion for the transmitter
- Supports interrupts and DMA

2.8 Security System

2.8.1 Crypto Engine (CE)

- Supports Symmetrical algorithm for encryption and decryption: AES, DES, TDES
  - Supports ECB, CBC, CTS, CTR, CFB, OFB mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports ECB, CBC, CTR mode for DES/TDES
- Supports Hash algorithm for tamper proofing: MD5, SHA, HMAC
  - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
  - Supports multi-package mode for MD5/SHA1/SHA224/SHA256/SHA384/SHA512
- Supports Asymmetrical algorithm for signature verification: RSA
  - RSA supports 512/1024/2048-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal DMA controller for data transfer with memory
- Supports secure and non-secure interfaces respectively

2.8.2 Security ID (SID)

- Supports 2 Kbits eFuse for chip ID and security application
- The eFuse has secure zone and non-secure zone
- Backup eFuse information by using SID_SRAM
- Burning the key to the SID
- Reading the key status in the SID
- Loading the key to the CE

2.8.3 Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Sets secure area of DRAM
- Sets secure property that Master accesses to DRAM

2.8.4 Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Sets secure property of peripherals

2.9 External Peripherals

2.9.1 USB DRD

- One USB 2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports USB Host function
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root port shared between EHCI and OHCI
- Supports USB Device function
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
  - Supports bi-directional endpoint0 (EP0) for Control transfer
  - Up to 10 user-configurable endpoints (EP1+, EP1-, EP2+, EP2-, EP3+, EP3-, EP4+, EP4-, EP5+, EP5-) for Bulk transfer, Isochronous transfer and Interrupt transfer
  - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
  - Support interface to an external Normal DMA controller for every EP
- Support an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral modes
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Device and host controller share a 8K SRAM and a physical PHY

2.9.2 USB HOST

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Supports USB2.0 Host function
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a

- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
- Supports only 1 USB Root port shared between EHCI and OHCI

- An internal DMA Controller for data transfer with memory

2.9.3 EMAC

- One EMAC interface for connecting external Ethernet PHY
- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operations
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
  - Supports linked-list descriptor list structure
  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
  - Comprehensive status reporting for normal operation and transfers with errors
- 4 KB TXFIFO for transmission packets and 16 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.9.4 UART

- Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
- UART0, UART4, UART5: 2-wire; UART1, UART2, UART3: 4-wire
- Compatible with industry-standard 16450/16550 UARTs
- Supports IrDA-compatible slow infrared (SIR) format
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes (For UART0)
  - Each of them is 256 bytes (For UART1, UART2, UART3, UART4, and UART5)
- The working reference clock is from the APB bus clock
  - Speed up to 4 Mbit/s with 64 MHz APB clock
  - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 characters, or 9 bits RS-485 format

- 1, 1.5 or 2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports RX DMA Master interface (Only for UART1)
- Supports auto-flow by using CTS & RTS (Only for UART1/2/3)

2.9.5 SPI and SPI_DBI

- Up to 2 SPI controllers (SPI0, SPI1)
- The SPI0 only supports SPI mode; The SPI1 supports SPI mode and display bus interface (DBI) mode
- SPI mode:
  - Full-duplex synchronous serial interface
  - Master/slave configurable
  - Mode0 to Mode3 are supported for both transmit and receive operations
  - 8-bit wide by 64-entry FIFO for both transmit and receive data
  - Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
  - Supports 3-wire/4-wire SPI
  - Supports programmable serial data frame length: 1-bit to 32-bit
  - Supports Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI
- DBI mode:
  - Supports DBI Type C 3 Line/4 Line Interface Mode
  - Supports 2 Data Lane Interface Mode
  - Supports RGB111/444/565/666/888 video format
  - Maximum resolution of RGB666 240 x 320@30Hz with single data lane
  - Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
  - Supports Tearing effect
  - Supports software flexible control video frame rate

2.9.6 Two Wire Interface (TWI)

- Up to 4 TWI controllers (TWI0, TWI1, TWI2, TWI3)
- Compliant with I2C bus standard
- Supports standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s)
- Supports 7-bit and 10-bit device addressing modes
- Supports master mode or slave mode

- Master mode features:
  - Supports the bus arbitration in the case of multiple master devices
  - Supports clock synchronization and bit and byte waiting
  - Supports packet transmission and DMA
- Slave mode features:
  - Interrupt on address detection
- The TWI controller includes one TWI engine and one TWI driver. And the TWI driver supports packet transmission and DMA mode when TWI works in master mode

2.9.7 CIR Receiver (CIR_RX)

- One CIR_RX interface (IR-RX)
- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.9.8 CIR Transmitter (CIR_TX)

- One CIR_TX interface (IR-TX)
- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer

2.9.9 PWM

- Supports 8 independent PWM channels (PWM0 to PWM7)
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range: 0 to 24 MHz or 100 MHz
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Supports 4 complementary pairs output
  - PWM01 pair (PWM0 + PWM1), PWM23 pair (PWM2 + PWM3), PWM45 pair (PWM4 + PWM5), PWM67 pair (PWM6 + PWM7)

- Supports dead-zone generator, and the dead-zone time is configurable

- Supports 4 group of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Supports 8 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

2.9.10 General Purpose ADC (GPADC)

- 1-ch successive approximation register (SAR) analog-to-digital converter (ADC)
- 12-bit sampling resolution and 8-bit precision
- 64 FIFO depth of data register
- Power reference voltage: AVCC, analog input voltage range: 0 to AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

2.9.11 LEDC

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s

2.10 Package

LFBGA 196 balls, 10 mm x 10 mm body size, 0.65 mm ball pitch, 0.35 mm ball size

3 Block Diagram

Figure 3-1 shows the system block diagram of the H133.

Figure 3-1 H133 System Block Diagram

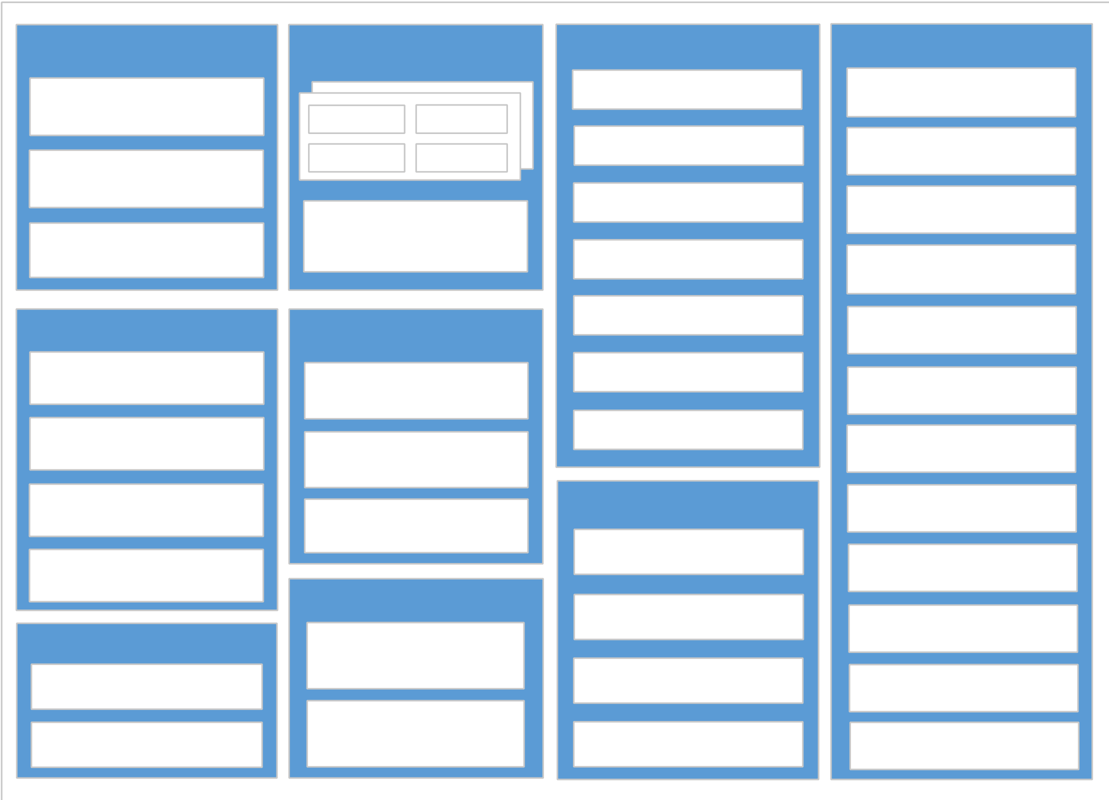
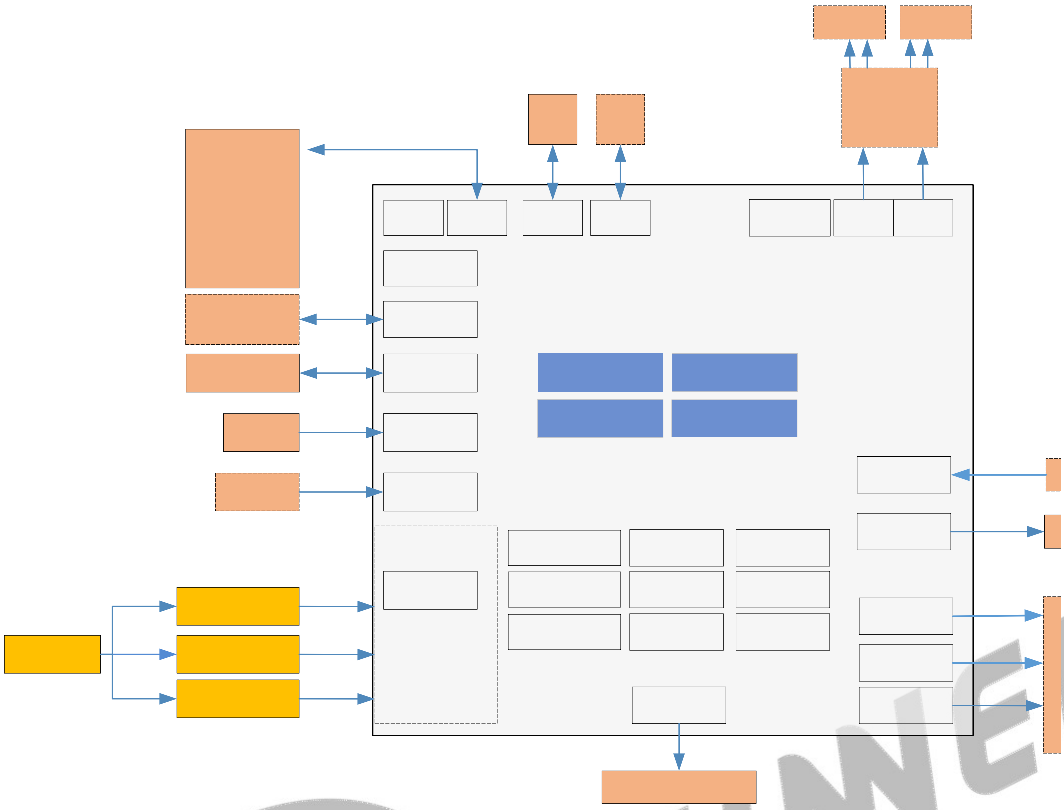


Figure 3-2 shows the typical solution diagram of the H133.

Figure 3-2 Intelligent Speaker with Screen Solution of the H133



4 Pin Description

4.1 Pin Quantity

Table 4-1 lists the pin quantity of the H133.

Table 4-1 H133 Pin Quantity

Pin Type	Quantity
I/O	128
Power	23
Ground	40
DDR Power	5
Total	196

4.2 Pin Characteristics

Table 4-2 lists the characteristics of the H133 pins from the following seven aspects.

[1].**Ball#**: Package ball numbers associated with each signal.

[2].**Pin Name**: The name of the package pin.

[3].**Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

[4].**Ball Reset State**: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].**Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

[6].**Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

[7].**Power Supply**: The voltage supply for the IO buffers of the terminal.

Table 4-2 Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
SDRAM						
N11	SA0	O	NA	NA	NA	VCC-DRAM
M11	SA1	O	NA	NA	NA	VCC-DRAM
M10	SA2	O	NA	NA	NA	VCC-DRAM
L10	SA3	O	NA	NA	NA	VCC-DRAM
L11	SA4	O	NA	NA	NA	VCC-DRAM
R13	SA5	O	NA	NA	NA	VCC-DRAM
M9	SA6	O	NA	NA	NA	VCC-DRAM
P13	SA7	O	NA	NA	NA	VCC-DRAM
P12	SA8	O	NA	NA	NA	VCC-DRAM
P11	SA9	O	NA	NA	NA	VCC-DRAM
N10	SA10	O	NA	NA	NA	VCC-DRAM
P10	SA11	O	NA	NA	NA	VCC-DRAM
R14	SA12	O	NA	NA	NA	VCC-DRAM
L12	SA13	O	NA	NA	NA	VCC-DRAM
P15	SA14	O	NA	NA	NA	VCC-DRAM
M12	SA15	O	NA	NA	NA	VCC-DRAM
L7	SBA0	O	NA	NA	NA	VCC-DRAM
P9	SBA1	O	NA	NA	NA	VCC-DRAM
N8	SBA2	O	NA	NA	NA	VCC-DRAM
R8	SCKE0	O	NA	NA	NA	VCC-DRAM
N7	SCKN	O	NA	NA	NA	VCC-DRAM
P7	SCKP	O	NA	NA	NA	VCC-DRAM
P8	SCS0	O	NA	NA	NA	VCC-DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
L4	SDQ0	I/O	NA	NA	NA	VCC-DRAM
M4	SDQ1	I/O	NA	NA	NA	VCC-DRAM
M5	SDQ2	I/O	NA	NA	NA	VCC-DRAM
M6	SDQ3	I/O	NA	NA	NA	VCC-DRAM
N4	SDQ4	I/O	NA	NA	NA	VCC-DRAM
N5	SDQ5	I/O	NA	NA	NA	VCC-DRAM
P5	SDQ6	I/O	NA	NA	NA	VCC-DRAM
P4	SDQ7	I/O	NA	NA	NA	VCC-DRAM
R3	SDQ8	I/O	NA	NA	NA	VCC-DRAM
M1	SDQ9	I/O	NA	NA	NA	VCC-DRAM
P2	SDQ10	I/O	NA	NA	NA	VCC-DRAM
M2	SDQ11	I/O	NA	NA	NA	VCC-DRAM
N3	SDQ12	I/O	NA	NA	NA	VCC-DRAM
N2	SDQ13	I/O	NA	NA	NA	VCC-DRAM
R2	SDQ14	I/O	NA	NA	NA	VCC-DRAM
M3	SDQ15	I/O	NA	NA	NA	VCC-DRAM
L6	SDQM0	O	NA	NA	NA	VCC-DRAM
R4	SDQM1	O	NA	NA	NA	VCC-DRAM
P6	SDQS0N	I/O	NA	NA	NA	VCC-DRAM
R6	SDQS0P	I/O	NA	NA	NA	VCC-DRAM
P1	SDQS1N	I/O	NA	NA	NA	VCC-DRAM
N1	SDQS1P	I/O	NA	NA	NA	VCC-DRAM
M7	SODT0	O	NA	NA	NA	VCC-DRAM
L9	SRAS	O	NA	NA	NA	VCC-DRAM
P14	SRST	O	NA	NA	NA	VCC-DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
R10	SWE	O	NA	NA	NA	VCC-DRAM
R12	SCAS	O	NA	NA	NA	VCC-DRAM
K10	SZQ	AI	NA	NA	NA	VCC-DRAM
K11	SVREF	P	NA	NA	NA	VCC-DRAM
J7, J8, K7 ,K8	VCC_DRAM	P	NA	NA	NA	NA
GPIOB						
D15	PB0	I/O	Z	PU/PD	4	VCC-IO
D14	PB1	I/O	Z	PU/PD	4	VCC-IO
D13	PB8	I/O	Z	PU/PD	4	VCC-IO
C14	PB9	I/O	Z	PU/PD	4	VCC-IO
C13	PB10	I/O	Z	PU/PD	4	VCC-IO
B15	PB11	I/O	Z	PU/PD	4	VCC-IO
B14	PB12	I/O	Z	PU/PD	4	VCC-IO
GPIOC						
F3	PC2	I/O	Z	PU/PD	4	VCC-PC
F2	PC3	I/O	PU	PU/PD	4	VCC-PC
F1	PC4	I/O	PU	PU/PD	4	VCC-PC
G3	PC5	I/O	PU	PU/PD	4	VCC-PC
G2	PC6	I/O	Z	PU/PD	4	VCC-PC
H3	PC7	I/O	Z	PU/PD	4	VCC-PC
F5	VCC-PC	P	NA	NA	NA	NA
GPIOD						
N15	PD0	I/O	Z	PU/PD	4	VCC-PD
N14	PD1	I/O	Z	PU/PD	4	VCC-PD
M15	PD2	I/O	Z	PU/PD	4	VCC-PD

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
M14	PD3	I/O	Z	PU/PD	4	VCC-PD
L15	PD4	I/O	Z	PU/PD	4	VCC-PD
L14	PD5	I/O	Z	PU/PD	4	VCC-PD
K15	PD6	I/O	Z	PU/PD	4	VCC-PD
K14	PD7	I/O	Z	PU/PD	4	VCC-PD
J15	PD8	I/O	Z	PU/PD	4	VCC-PD
J14	PD9	I/O	Z	PU/PD	4	VCC-PD
G11	VCC-LVDS	P	NA	NA	NA	NA
J11	VCC-PD	P	NA	NA	NA	NA
GPIOF						
B1	PF0	I/O	Z	PU/PD	4	VCC-PF
C3	PF1	I/O	Z	PU/PD	4	VCC-PF
C2	PF2	I/O	Z	PU/PD	4	VCC-PF
D3	PF3	I/O	Z	PU/PD	4	VCC-PF
D2	PF4	I/O	Z	PU/PD	4	VCC-PF
D1	PF5	I/O	Z	PU/PD	4	VCC-PF
E2	PF6	I/O	Z	PU/PD	4	VCC-PF
E5	VCC-PF	P	NA	NA	NA	NA
GPIOG						
B8	PG0	I/O	Z	PU/PD	4	VCC-PG
C9	PG1	I/O	Z	PU/PD	4	VCC-PG
A8	PG2	I/O	Z	PU/PD	4	VCC-PG
B7	PG3	I/O	Z	PU/PD	4	VCC-PG
A6	PG4	I/O	Z	PU/PD	4	VCC-PG
C7	PG5	I/O	Z	PU/PD	4	VCC-PG

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
B4	PG6	I/O	Z	PU/PD	4	VCC-PG
A3	PG7	I/O	Z	PU/PD	4	VCC-PG
B3	PG8	I/O	Z	PU/PD	4	VCC-PG
A2	PG9	I/O	Z	PU/PD	4	VCC-PG
C4	PG10	I/O	Z	PU/PD	4	VCC-PG
B6	PG11	I/O	Z	PU/PD	4	VCC-PG
C6	PG12	I/O	Z	PU/PD	4	VCC-PG
B5	PG13	I/O	Z	PU/PD	4	VCC-PG
C5	PG14	I/O	Z	PU/PD	4	VCC-PG
A4	PG15	I/O	Z	PU/PD	4	VCC-PG
B2	PG16	I/O	Z	PU/PD	4	VCC-PG
C10	PG17	I/O	Z	PU/PD	4	VCC-PG
B9	PG18	I/O	Z	PU/PD	4	VCC-PG
D5	VCC-PG	P	NA	NA	NA	NA
System						
L3	RESET	I, OD	NA	NA	NA	VCC-RTC
GPADC						
C11	GPADC0	AI	NA	NA	NA	AVCC
USB						
A10	USB0-DM	A I/O	NA	NA	NA	VCC-IO
B10	USB0-DP	A I/O	NA	NA	NA	VCC-IO
A11	USB1-DM	A I/O	NA	NA	NA	VCC-IO
V11	USB1-DP	A I/O	NA	NA	NA	VCC-IO
HDMI						
J13	HCEC	I/O	NA	NA	NA	VCC-HDMI

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
K13	HHPD	O	NA	NA	NA	VCC-HDMI
F13	HSCL	I/O	NA	NA	NA	VCC-HDMI
G13	HSDA	AO	NA	NA	NA	VCC-HDMI
G15	HTX0N	AO	NA	NA	NA	VCC-HDMI
G14	HTX0P	AO	NA	NA	NA	VCC-HDMI
F15	HTX1N	AO	NA	NA	NA	VCC-HDMI
F14	HTX1P	AO	NA	NA	NA	VCC-HDMI
E15	HTX2N	AO	NA	NA	NA	VCC-HDMI
E14	HTX2P	AO	NA	NA	NA	VCC-HDMI
H15	HTXCN	AO	NA	NA	NA	VCC-HDMI
H14	HTXCP	AO	NA	NA	NA	VCC-HDMI
H11	VCC_HDMI	P	NA	NA	NA	NA
Audio Codec						
A12	HPOUTR	AO	NA	NA	NA	HPVCC
C12	HPOUTL	AO	NA	NA	NA	HPVCC
B12	HPOUTFB	AI	NA	NA	NA	HPVCC
E11	HPVCC	P	NA	NA	NA	NA
B13	VRA1	AO	NA	NA	NA	AVCC
A14	VRA2	AO	NA	NA	NA	AVCC
D12	AVCC	P	NA	NA	NA	NA
A13	AGND	G	NA	NA	NA	NA
RTC & PLL						
K1	X32KIN	AI	NA	NA	NA	VCC-RTC
K2	X32KOUT	AO	NA	NA	NA	VCC-RTC
H5	VCC-RTC	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
G5	VCC-PLL	P	NA	NA	NA	NA
DCXO						
J2	DXIN	AI	NA	NA	NA	VCC-PLL
J3	DXOUT	AO	NA	NA	NA	VCC-PLL
H1	REFCLK-OUT	AO	NA	NA	NA	VCC-PLL
Power						
K5	LDO-IN	P	NA	NA	NA	NA
J5	LDOA-OUT	P	NA	NA	NA	NA
K6	LDOB-OUT	P	NA	NA	NA	NA
F11	VCC-IO	P	NA	NA	NA	NA
D9,D10,E9,E10,	VDD-SYS	P	NA	NA	NA	NA
D6,D7,E6,E7	VDD-CPU	P	NA	NA	NA	NA
D8	VDD-CPUFB	P	NA	NA	NA	NA
GND						
A1,A15,C8,D11,E3,E8,E13,F6,F7,F8,F9,F10,G6,G7,G8,G9,G10,H2,H6,H7,H8,H9,H10,H13,J6,J9,J10,K3,K12,L2,L5,L8,L13,N6,N9,N12,P3,R1,R15	GND	G	NA	NA	NA	NA

4.3 GPIO Multiplex Function

The following table provides a description of the H133 GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

Table 4-3 GPIO Multiplex Function

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PB0	GPIOB	I/O	PWM3	IR-TX	TWI2-SCK	SPI1-WP/ DBI-TE	UART0-TX	UART2-TX	OWA-OUT	PB-EINT0
PB1		I/O	PWM4	I2S2-DOUT3	TWI2-SDA	I2S2-DIN3	UART0-RX	UART2-RX	IR-RX	PB-EINT1
PB8		I/O	DMIC-DATA3	PWM5	TWI2-SCK	SPI1-HOLD/ DBI-DCX/ DBI-WRX	UART0-TX	UART1-TX		PB-EINT8
PB9		I/O	DMIC-DATA2	PWM6	TWI2-SDA	SPI1-MISO/ DBI-SDI/ DBI-TE/ DBI-DCX	UART0-RX	UART1-RX		PB-EINT9
PB10		I/O	DMIC-DATA1	PWM7	TWI0-SCK	SPI1-MOSI/ DBI-SDO	CLK-FANOUT0	UART1-RTS		PB-EINT10
PB11		I/O	DMIC-DATA0	PWM2	TWI0-SDA	SPI1-CLK/ DBI-SCLK	CLK-FANOUT1	UART1-CTS		PB-EINT11
PB12		I/O	DMIC-CLK	PWM0		SPI1-CS/ DBI-CSX	CLK-FANOUT2	IR-RX		PB-EINT12
PC2		I/O	SPI0-CLK	SDC2-CLK						PC-EINT2
PC3		I/O	SPI0-CS0	SDC2-CMD						PC-EINT3
PC4		I/O	SPI0-MOSI	SDC2-D2	BOOT-SEL0					PC-EINT4
PC5		I/O	SPI0-MISO	SDC2-D1	BOOT-SEL1					PC-EINT5
PC6		I/O	SPI0-WP	SDC2-D0	UART3-TX	TWI3-SCK	DBG-CLK			PC-EINT6
PC7		I/O	SPI0-HOLD	SDC2-D3	UART3-RX	TWI3-SDA	TCON-TRIG			PC-EINT7
PD0	GPIOD	I/O		LVDS0-V0P	DSI-D0P	TWI0-SCK				PD-EINT0
PD1		I/O		LVDS0-V0N	DSI-D0N	UART2-TX				PD-EINT1
PD2		I/O		LVDS0-V1P	DSI-D1P	UART2-RX				PD-EINT2
PD3		I/O		LVDS0-V1N	DSI-D1N	UART2-RTS				PD-EINT3
PD4		I/O		LVDS0-V2P	DSI-CKP	UART2-CTS				PD-EINT4
PD5		I/O		LVDS0-V2N	DSI-CKN	UART5-TX				PD-EINT5
PD6		I/O		LVDS0-CKP	DSI-D2P	UART5-RX				PD-EINT6
PD7		I/O		LVDS0-CKN	DSI-D2N	UART4-TX				PD-EINT7
PD8		I/O		LVDS0-V3P	DSI-D3P	UART4-RX				PD-EINT8
PD9		I/O		LVDS0-V3N	DSI-D3N	PWM6				PD-EINT9
PF0	GPIOF	I/O	SDC0-D1	JTAG-MS		I2S2-DOUT1	I2S2-DIN0			PF-EINT0

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PF1		I/O	SDC0-D0	JTAG-DI		I2S2-DOUT0	I2S2-DIN1			PF-EINT1
PF2		I/O	SDC0-CLK	UART0-TX	TWI0-SCK					PF-EINT2
PF3		I/O	SDC0-CMD	JTAG-DO		I2S2-BCLK				PF-EINT3
PF4		I/O	SDC0-D3	UART0-RX	TWI0-SDA	PWM6	IR-TX			PF-EINT4
PF5		I/O	SDC0-D2	JTAG-CK		I2S2-LRCK				PF-EINT5
PF6		I/O		OWA-OUT	IR-RX	I2S2-MCLK	PWM5			PF-EINT6
PG0		I/O	SDC1-CLK	UART3-TX	RGMII-RXCTRL/ RMII-CRS-DV	PWM7				PG-EINT0
PG1		I/O	SDC1-CMD	UART3-RX	RGMII-RXD0/ RMII-RXD0	PWM6				PG-EINT1
PG2		I/O	SDC1-D0	UART3-RTS	RGMII-RXD1/ RMII-RXD1	UART4-TX				PG-EINT2
PG3		I/O	SDC1-D1	UART3-CTS	RGMII-TXCK/ RMII-TXCK	UART4-RX				PG-EINT3
PG4		I/O	SDC1-D2	UART5-TX	RGMII-TXD0/ RMII-TXD0	PWM5				PG-EINT4
PG5		I/O	SDC1-D3	UART5-RX	RGMII-TXD1/ RMII-TXD1	PWM4				PG-EINT5
PG6		I/O	UART1-TX	TWI2-SCK	RGMII-TXD2	PWM1				PG-EINT6
PG7		I/O	UART1-RX	TWI2-SDA	RGMII-TXD3					PG-EINT7
PG8	GPIOG	I/O	UART1-RTS	TWI1-SCK	RGMII-RXD2	UART3-TX				PG-EINT8
PG9		I/O	UART1-CTS	TWI1-SDA	RGMII-RXD3	UART3-RX				PG-EINT9
PG10		I/O	PWM3	TWI3-SCK	RGMII-RXCK	CLK-FANOUT0	IR-RX			PG-EINT10
PG11		I/O	I2S1-MCLK	TWI3-SDA	EPHY-25M	CLK-FANOUT1	TCON-TRIG			PG-EINT11
PG12		I/O	I2S1-LRCK	TWI0-SCK	RGMII-TXCTRL/ RMII-TXEN	CLK-FANOUT2	PWM0	UART1-TX		PG-EINT12
PG13		I/O	I2S1-BCLK	TWI0-SDA	RGMII-CLKIN/ RMII-RXER	PWM2	LEDC-DO	UART1-RX		PG-EINT13
PG14		I/O	I2S1-DIN0	TWI2-SCK	MDC	I2S1-DOUT1	SPI0-WP	UART1-RTS		PG-EINT14
PG15		I/O	I2S1-DOUT0	TWI2-SDA	MDIO	I2S1-DIN1	SPI0-HOLD	UART1-CTS		PG-EINT15
PG16		I/O	IR-RX	TCON-TRIG	PWM5	CLK-FANOUT2		LEDC-DO		PG-EINT16
PG17		I/O	UART2-TX	TWI3-SCK	PWM7	CLK-FANOUT0	IR-TX	UART0-TX		PG-EINT17
PG18		I/O	UART2-RX	TWI3-SDA	PWM6	CLK-FANOUT1	OWA-OUT	UART0-RX		PG-EINT18

4.4 Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.

[1].Signal Name: The name of every signal.

[2].Description: The detailed function description of every signal.

[3].Type: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

Table 4-4 Detailed Signal Description

Signal Name[1]	Description[2]	Type[3]
DRAM		
SA[15:0]	DRAM Address Signal to the Memory Device	O
SBA[2:0]	DRAM Bank Address Signal to the Memory Device	O
SCKE0	DRAM Clock Enable Signal to the Memory Device	O
SCKN	DRAM Active-Low Clock Signal to the Memory Device	O
SCKP	DRAM Active-High Clock Signal to the Memory Device	O
SCS0	DRAM Chip Select Signal to the Memory Device	O
SDQ[15:0]	DRAM Bidirectional Data line to the Memory Device	I/O
SDQM[1:0]	DRAM Data Mask Signal to the Memory Device	O
SDQS[1:0]N	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SDQS[1:0]P	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O

Signal Name[1]	Description[2]	Type[3]
SODT0	DRAM On-Die Termination Output Signal	O
SCAS	DRAM Column Address Strobe	O
SRAS	DRAM Row Address Strobe	O
SRST	DRAM Reset Signal to the Memory Device	O
SVREF	DRAM Reference Voltage	P
SWE	DRAM Write Enable	O
SZQ	DRAM External Reference Resistor for Impedance Calibration	AI
VCC-DRAM	DRAM Power Supply	P
System Control		
BOOT-SEL[1:0]	Boot Media Select	I
RESET	Reset Signal (low active)	I, OD
Clock		
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
VCC-RTC	RTC Power	P
VCC-PLL	PLL Power Supply	P
DCXO		
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
USB		
USB0-DM	USB DRD Data Signal DM	A I/O
USB0-DP	USB DRD Data Signal DP	A I/O
USB1-DM	USB HOST Data Signal DM	A I/O
USB1-DP	USB HOST Data Signal DP	A I/O

Signal Name[1]	Description[2]	Type[3]
GPADC		
GPADC0	General Purpose ADC Input Channel 0	AI
AUDIO CODEC		
HPOUTR	Headphone Right Output	AO
HPOUTL	Headphone Light Output	AO
HPOUTFB	Pseudo Differential Headphone Ground Reference	AI
HPVCC	Headphone Power	P
VRA1	Internal Reference Voltage	AO
VRA2	Internal Reference Voltage	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
HDMI		
HCEC	HDMI Consumer Electronics Control	I/O
HHPD	HDMI Hot Plug Detection Signal	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO

Signal Name[1]	Description[2]	Type[3]
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
VCC_HDMI	HDMI Power	P
LVDS		
LVDS0-CKP	LVDS0 Positive Port of Clock	O
LVDS0-CKN	LVDS0 Negative Port of Clock	O
LVDS0-V[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	O
LVDS0-V[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	O
DSI		
DSI-D[3:0]P	DSI Differential Data [3:0] Positive Signal	O
DSI-D[3:0]N	DSI Differential Data [3:0] Negative Signal	O
DSI-CKP	DSI Differential Clock Positive Signal	O
DSI-CKN	DSI Differential Clock Negative Signal	O
SMHC		
SDC0-CMD	Command Signal for SD Card	I/O, OD
SDC0-CLK	Clock for SD Card	O
SDC0-D[3:0]	Data Input and Output for SD Card	I/O
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	I/O
SDC2-CMD	Command Signal for eMMC	I/O, OD
SDC2-CLK	Clock for eMMC	O
SDC2-D[3:0]	Data Input and Output for eMMC	I/O
I2S/PCM		

Signal Name[1]	Description[2]	Type[3]
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S2-DOUT[1:0], I2S2-DOUT3	I2S2/PCM2 Serial Data Output Channel [1:0], and Channel 3	O
I2S2-DIN[1:0], I2S2-DIN3	I2S2/PCM2 Serial Data Input Channel [1:0], and Channel 3	I
DMIC		
DMIC-CLK	Digital Microphone Clock Output	O
DMIC-DATA[3:0]	Digital Microphone Data Input	I
EMAC		
RGMII-RXD3	RGMII Receive Data3	I
RGMII-RXD2	RGMII Receive Data2	I
RGMII-RXD1/RMII-RXD1	RGMII/RMII Receive Data1	I
RGMII-RXD0/RMII-RXD0	RGMII/RMII Receive Data0	I
RGMII-RXCK	RGMII Receive Clock	I
RGMII-RXCTRL/ RMII-CRS-DV	RGMII Receive Control/RMII Carrier Sense Receive Data Valid	I
RGMII-CLKIN/RMII-RXER	RGMII Transmit Clock from External/RMII Receive Error	I
RGMII-TXD3	RGMII Transmit Data3	O
RGMII-TXD2	RGMII Transmit Data2	O

Signal Name[1]	Description[2]	Type[3]
RGMII-TXD1/RMII-TXD1	RGMII/RMII Transmit Data1	O
RGMII-TXD0/RMII-TXD0	RGMII/RMII Transmit Data0	O
RGMII-TXCK/RMII-TXCK	RGMII/RMII Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII-TXCTRL/ RMII-TXEN	RGMII Transmit Control/RMII Transmit Enable	O
MDC	RGMII/RMII Management Data Clock	O
MDIO	RGMII/RMII Management Data Input/Output	I/O
EPHY-25M	25MHz Output for EMAC PHY	O
OWA		
OWA-OUT	One Wire Audio Output	O
LEDC		
LEDC-DO	Intelligent Control LED Signal Output	O
Interrupt		
PB-EINT[12:8], PB-EINT[1:0]	GPIO B Interrupt	I
PC-EINT[7:2]	GPIO C Interrupt	I
PD-EINT[9:0]	GPIO D Interrupt	I
PF-EINT[6:0]	GPIO F Interrupt	I
PG-EINT[18:0]	GPIO G Interrupt	I
CIR Receiver		
IR-RX	Consumer Infrared Receiver	I
CIR Transmitter		
IR-TX	Consumer Infrared Transmitter	O
PWM		

Signal Name[1]	Description[2]	Type[3]
PWM[7:0]	Pulse Width Modulation Output Channel [7:0]	I/O
SPI&SPI_DBI		
SPI0-CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal Provides serial interface timing.	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI0-HOLD	SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal Provides serial interface timing.	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-HOLD	SPI1 Hold Signal Pauses any serial communication with the device without resetting it. It also can be used for serial data input and output for	I/O

Signal Name[1]	Description[2]	Type[3]
	SPI Quad Input or Quad Output mode.	
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
UART		
UART0-TX	UART0 Data Transmit	O
UART0-RX	UART0 Data Receive	I
UART1-TX	UART1 Data Transmit	O
UART1-RX	UART1 Data Receive	I
UART1-CTS	UART1 Data Clear to Send	I
UART1-RTS	UART1 Data Request to Send	O
UART2-TX	UART2 Data Transmit	O
UART2-RX	UART2 Data Receive	I
UART2-CTS	UART2 Data Clear to Send	I
UART2-RTS	UART2 Data Request to Send	O
UART3-TX	UART3 Data Transmit	O

Signal Name[1]	Description[2]	Type[3]
UART3-RX	UART3 Data Receive	I
UART3-CTS	UART3 Data Clear to Send	I
UART3-RTS	UART3 Data Request to Send	O
UART4-TX	UART4 Data Transmit	O
UART4-RX	UART4 Data Receive	I
UART5-TX	UART5 Data Transmit	O
UART5-RX	UART5 Data Receive	I
TWI		
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O
JTAG		
JTAG-MS	A7 JTAG Mode Select	I
JTAG-CK	A7 JTAG Clock Signal	I
JTAG-DO	A7 JTAG Data Output	O
JTAG-DI	A7 JTAG Data Input	I

5 Electrical Characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.3, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Symbol	Parameter	Min(1)	Max(1)	Unit

Symbol	Parameter	Min[1]	Max[1]	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
HPVCC	Headphone Power	-0.3	2.16	V
VCC-PC	Digital GPIO C Power	-0.3	3.96	V
VCC-PD	Digital GPIO D Power	-0.3	3.96	V
VCC-PF	Digital GPIO F Power	-0.3	3.96	V
VCC-PG	Digital GPIO G Power	-0.3	3.96	V
VCC-IO	Power Supply for 3.3 V Digital Part	-0.3	3.96	V
VCC-RTC	Power Supply for RTC	-0.3	2.16	V
VCC-PLL	Power Supply for System PLL	-0.3	2.16	V
VCC-LVDS	Power Supply for LVDS	-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM IO and DDR3	-0.3	2.16	V
VDD-CPU	Power Supply for CPU	-0.3	1.3	V
VCC-HDMI	Power Supply for HDMI	-0.3	2.16	V
VDD-SYS	Power Supply for System	-0.3	1.3	V
LDO-IN	Internal LDOA/B Input Voltage	-0.3	3.96	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO	-0.3	2.16	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM	-0.3	2.16	V
T_{STG}	Storage Temperature	-40	150	°C
Tj	Working Junction Temperature	-25	125	°C
V_{ESD}	Electrostatic Discharge[2]: Human Body Model(HBM)[3]	-2000	2000	V
	Electrostatic Discharge[2]: Charged Device Model(CDM)[4]	-250	250	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin[5]	Pass		
	Latch-up over-voltage performance voltage injection on each IO pin[6]	Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3 Recommended Operating Conditions

Table 5-2 describes operating conditions of the H133.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-25	-	75	°C
Tj	Working Junction Temperature Range	-25	-	115[(1)]	°C
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
HPVCC	Headphone Power	1.764	1.8	1.836	V
VCC-PC	Digital GPIO C Power 1.8 V voltage 3.3 V voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC-PD	Digital GPIO D Power 1.8 V voltage 3.3 V voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC-PF	Digital GPIO F Power 1.8 V voltage 3.3 V voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC-PG	Digital GPIO G Power 1.8 V voltage	 1.62	 1.8	 1.98	V

Symbol	Parameter	Min	Typ	Max	Unit
	3.3 V voltage	2.97	3.3	3.63	
VCC-IO	Power Supply for Digital Part 3.3 V voltage	2.97	3.3	3.63	V
VCC-RTC	Power Supply for RTC	1.62	1.8	1.98	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-LVDS	Power Supply for LVDS	1.62	1.8	1.98	V
VCC-DRAM	DDR2 IO Domain Power	1.7	1.8	1.9	V
	DDR3 IO Domain Power	1.425	1.5	1.575	V
	DDR3L IO Domain Power	1.283	1.35	1.45	V
VDD-CPU	Power Supply for CPU	0.85	0.9[(2)]	1.1	V
VCC-HDMI	Power Supply for HDMI	1.62	1.8	1.98	V
VDD-SYS	Power Supply for System	0.85	0.9	0.99	V
LDO-IN	Internal LDOA/B Input Voltage	2.4	3.3	3.6	V
LDOA-OUT	Internal LDOA Output Voltage for Analog Device and IO	1.764	1.8	1.836	V
LDOB-OUT	Internal LDOB Output Voltage for VCC-DRAM	1.31 1.455 1.746	1.35[(3)] 1.5 1.8	1.39 1.545 1.854	V

(1) The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.

(2) To avoid damage to the chip, this voltage value is based on its electrical characteristics. In actual use, since voltage and frequency are correlated, the specific voltage value is subject to the DVFS table.

(3) The default voltage of LDOB-OUT is 1.35 V.

5.4 DC Electrical Characteristics

Table 5-4 summarizes the DC electrical characteristics of the H133. For the interfaces of GPIO function port, refer to the DC parameters in Table 5-4 unless otherwise stated.

Table 5-3 DC Electrical Characteristics

(VCC-IO/VCC-PC/VCC-PD/VCC-PE/VCC-PF/VCC-PG)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	PC3 to PC7, PF3, PF6	12	15	18	kΩ
		PG0 to PG5	26	33	40	kΩ
		Other GPIOs	80	100	120	kΩ
R_{PD}	Input Pull-down Resistance	PC3 to PC7, PF3, PF6	12	15	18	kΩ
		PG0 to PG5	26	33	40	kΩ
		Other GPIOs	80	100	120	kΩ
I_{IH}	High-Level Input Current		-	-	10	uA
I_{IL}	Low-Level Input Current		-	-	10	uA
V_{OH}	High-Level Output Voltage		VCC-IO – 0.3	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

5.5 SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

Figure 5-1 SDIO Voltage Waveform

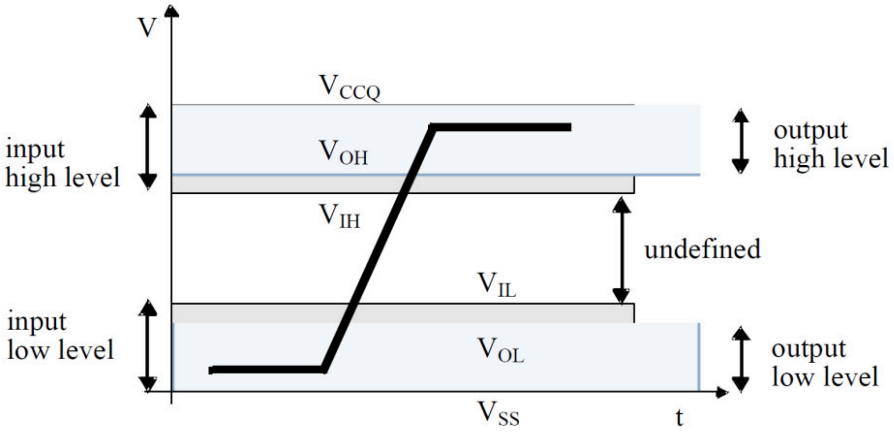


Table 5-5 shows 3.3 V SDIO electrical parameters.

Table 5-4 3.3 V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-6 shows 1.8 V SDIO electrical parameters.

Table 5-5 1.8 V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7	-	1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V

Symbol	Parameter	Min	Typ	Max	Unit
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6 GPADC Electrical Characteristics

The GPADC contains a 1-ch analog-to-digital (ADC) converter. The GPADC is a type of successive approximation register (SAR) converter. Table 5-7 lists GPADC electrical characteristics.

Table 5-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Quantizing Error	-	8	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

5.7 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, Input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-7 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DAC to HPOUTL or HPOUTR**					
	Full-scale	0dBFS 1 kHz	-	540	-	Vrms
	SNR (A-weighted)	0data	-	95	-	dB
	THD+N	0dBFS 1 kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1 kHz L_0dB_R_0data 1 kHz	-	-80	-	dB

5.8 External Clock Source Characteristics

5.8.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-8 High-speed 24 MHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of H133. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 5-9 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.

- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance (C_{pkg} + C_{PCB}) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

NOTE

For the above capacitances of 24 MHz crystal circuit, refer to the capacitance recommended in the *H133_Schematic_Diagram*.

5.8.2 Low-speed Crystal/Ceramic Resonator Characteristics

The H133 contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.

The H133 also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-10 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X32K_IN}	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C (1)	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	1.1	-	pF

1. The H133 has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.
2. The 1.1 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

NOTE

For capacitances of 32.768 kHz crystal circuit, refer to the capacitance recommended in the *H133_Schematic_Diagram*.

5.9 Internal Reset Electrical Characteristics

Table 5-11 Internal Reset Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Power-on threshold voltage of VDD-SYS on which the reset signal is excited	Ta= -25°C to 75°C	-	0.4	-	V
Reset active timeout period	Ta= -25°C to 75°C	-	64	-	ms
Reset open-drain output voltage	Ta= -25°C to 75°C, pull up 3.3 V	-0.3	-	0.3*VCC	V

5.10 External Memory Electrical Characteristics

5.10.1 SMHC AC Electrical Characteristics

5.10.1.1 HS-SDR Mode

NOTE

IO voltage is 1.8 V or 3.3 V.

Figure 5-2 SMHC HS-SDR Mode Output Timing Diagram

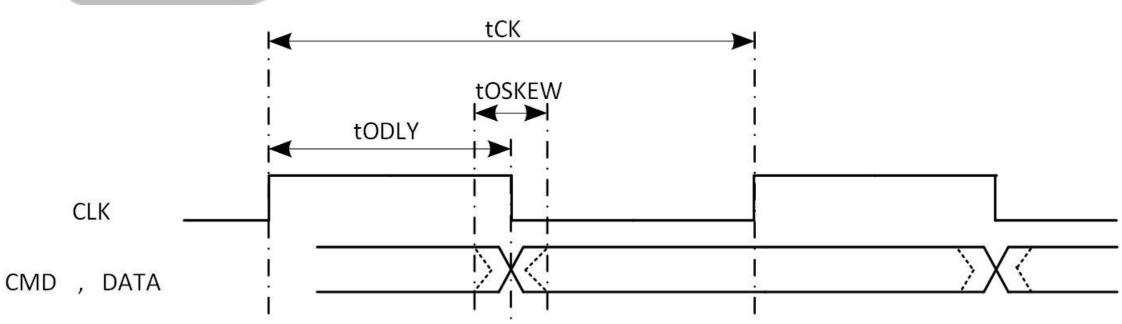


Table 5-12 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.5	ns
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. **(2). The driver strength level of GPIO is 2 for test.**					

Figure 5-3 SMHC HS-SDR Mode Input Timing Diagram

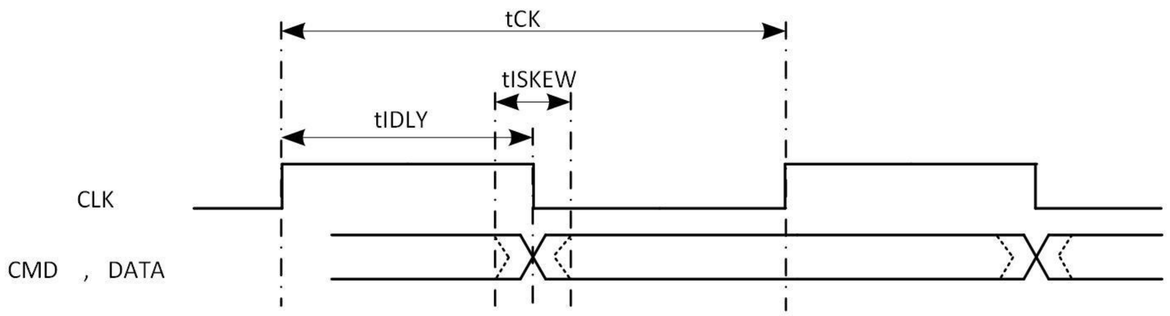


Table 5-13 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50 MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of	tIDLY	-	-	14	ns

Parameter	Symbol	Min	Typ	Max	Unit
Device					
Data input skew time in SDR mode	tISKEW	-	-	4	ns
(1). The driver strength level of GPIO is 2 for test.					

5.10.1.2 HS-DDR Mode

Figure 5-4 SMHC HS-DDR Mode Output Timing Diagram

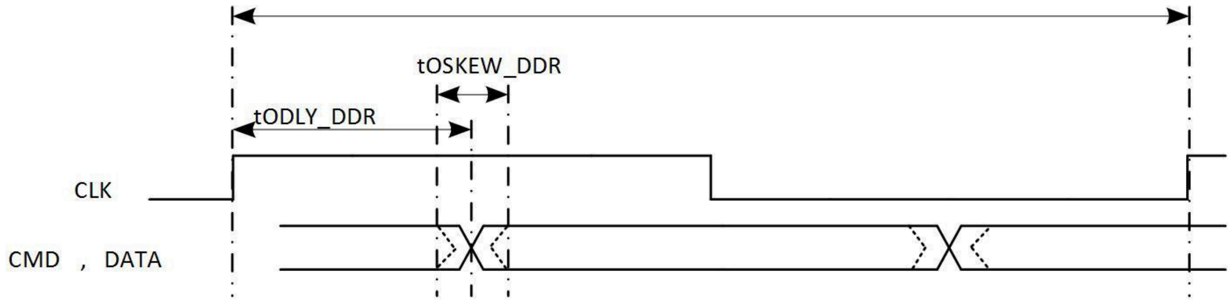


Table 5-14 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD output delay time in DDR mode	tODLY_DDR	0.12	0.25	0.5	UI
Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.5	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.5	ns
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. **(2). The driver strength level of GPIO is 2 for test.**					

Figure 5-5 SMHC HS-DDR Mode Input Timing Diagram

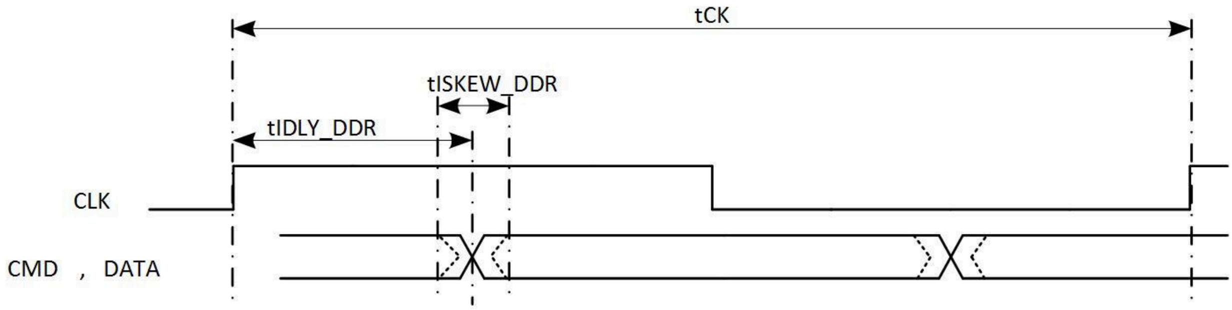


Table 5-15 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA (referenced to CLK 50 MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY_DDR	-	-	7	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	1.5	ns
(1). The driver strength level of GPIO is 2 for test.					

5.10.1.3 HS200 Mode

Figure 5-6 SMHC HS200 Mode Output Timing Diagram

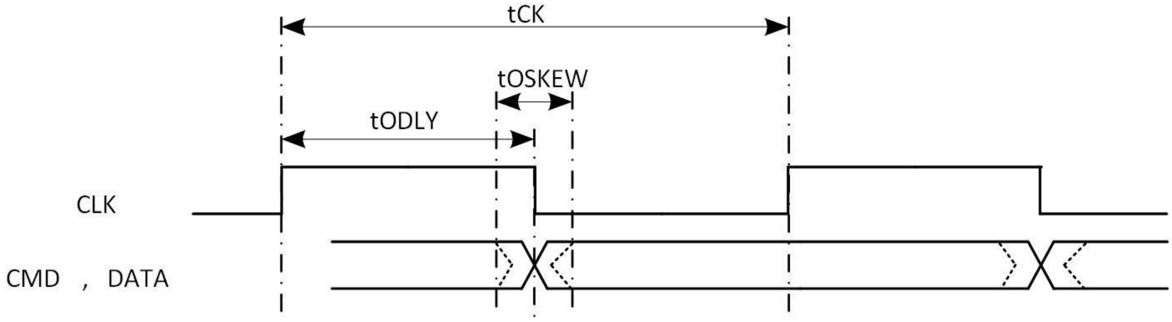


Table 5-16 SMHC HS200 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	0.5	-	0.8	ns
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. **(2). The driver strength level of GPIO is 3 for test.**					

Figure 5-7 SMHC HS200 Mode Input Timing Diagram

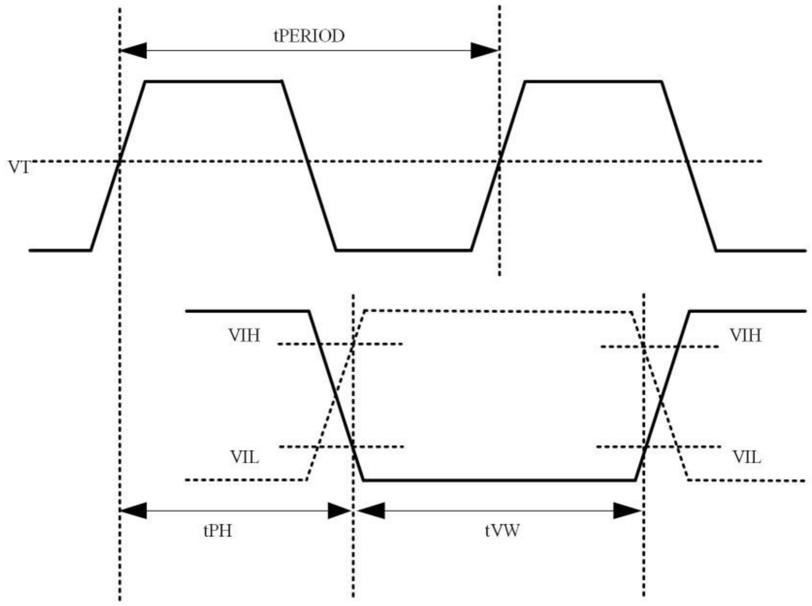


Table 5-17 SMHC HS200 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max: 150 MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA (referenced to CLK)						
Input delay	tPH	0	-	2	UI	
Input delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, Data valid window	tVW	0.575	-	-	UI	
(1). The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. **(2). The driver strength level of GPIO is 3 for test.** **(3). Temperature variation: -20ºC.**						

Parameter	Symbol	Min	Typ	Max	Unit	Remark
(4). Temperature variation: 90°C.						

5.11 External Peripheral Electrical Characteristics

5.11.1 EMAC AC Electrical Characteristics

5.11.1.1 RMII

Figure 5-8 RMII Interface Transmit Timing

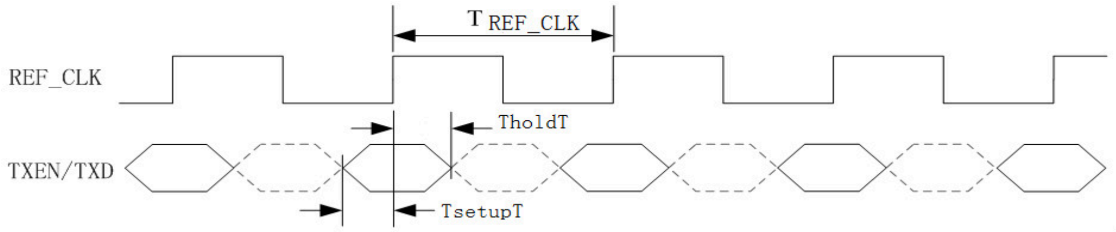


Figure 5-9RMII Interface Receive Timing

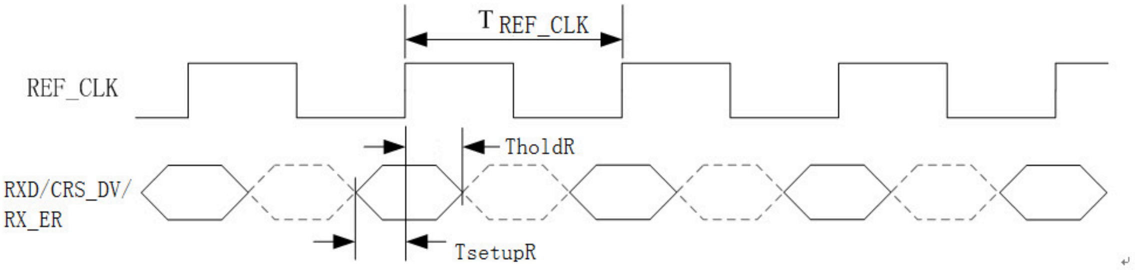


Table 5-18 RMII Timing Constants

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

5.11.1.2 RGMII

Figure 5-10 RGMII Interface Transmit Timing

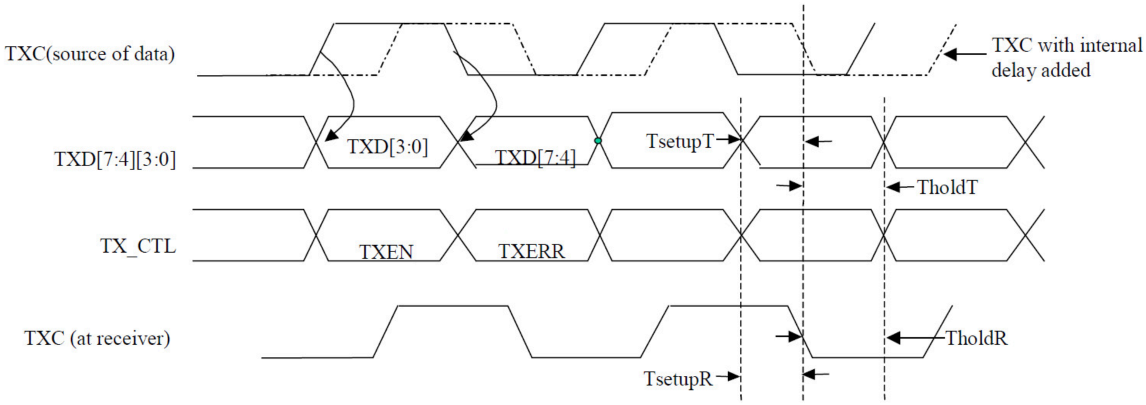


Figure 5-11 RGMII Interface Receive Timing

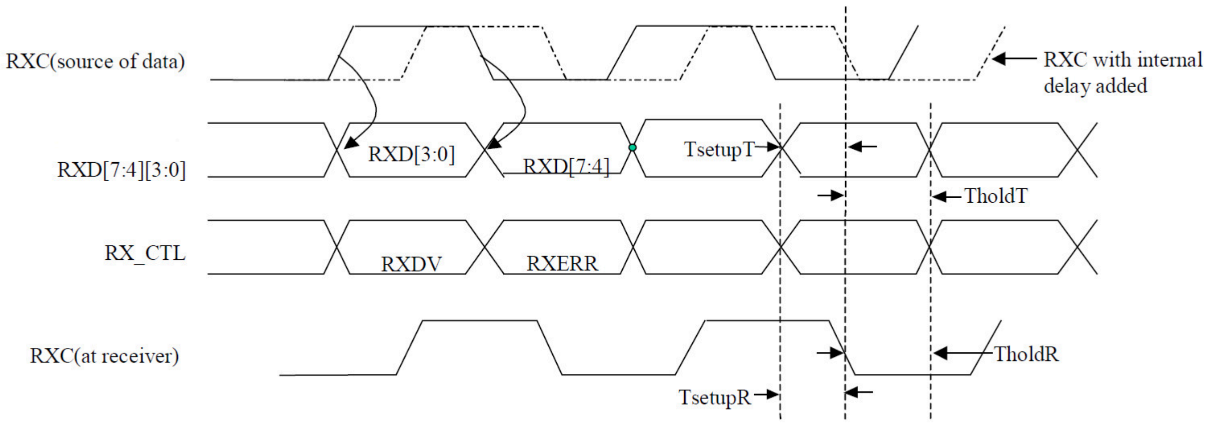


Table 5-19 RGMII Timing Constants

Parameter	Description	Min	Typical	Max	Unit
Tcyc	Clock Cycle Duration[1]	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to clock output setup(at Transmitter integrated delay)	1.2	2.0		ns
TholdT	Data to clock output hold(at Transmitter integrated delay)	1.2	2.0		ns
TsetupR	Data to clock input setup(at Receiver integrated delay)	1.0	2.0		ns
TholdR	Data to clock input hold(at Receiver integrated delay)	1.0	2.0		ns

Note: For 10Mbps and 100Mbps, Tcyc will scale 400ns±40ns and 40ns±4ns.

5.11.2 SPI AC Electrical Characteristics

Figure 5-12 SPI Writing Timing

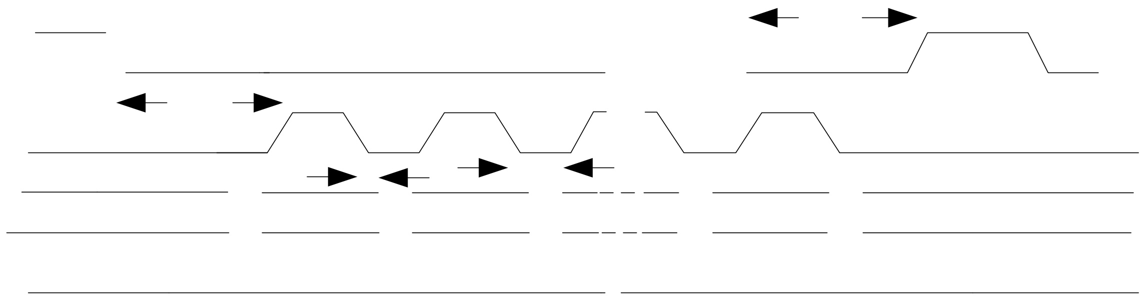


Figure 5-13 SPI Reading Timing

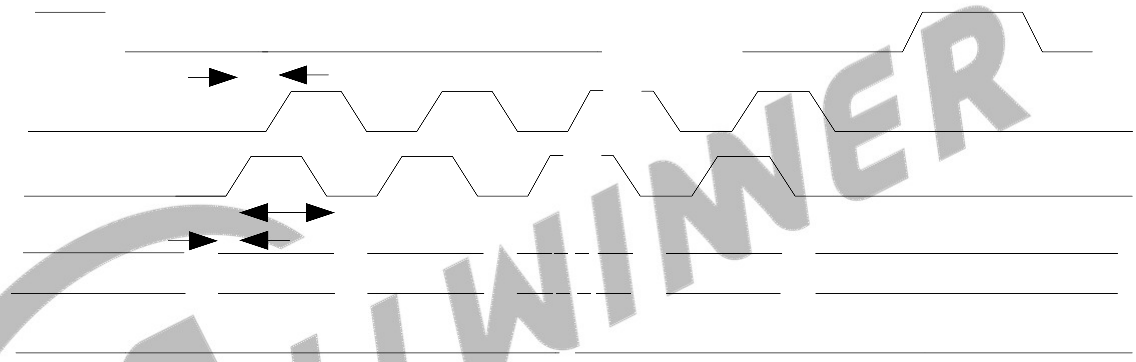


Table 5-20 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	$t_s(cs)$	-	$2T^{(1)}$	-	ns
CS# active hold time	$t_h(cs)$	-	$2T^{(1)}$	-	ns
Data output delay time	$t_d(mo)$	-	$T^{(1)}/2-3$	-	ns
Data output hold time	$t_h(mo)$	-	$T^{(1)}/2-3$	-	ns
Data input setup time	$t_s(mi)$	0.2	-	-	ns
Data input hold time	$t_h(mi)$	0.2	-	-	ns
(1).T is the cycle of clock.					

5.11.3 SPI_DBI AC Electrical Characteristics

Figure 5-14 DBI 3-line Serial Interface Timing

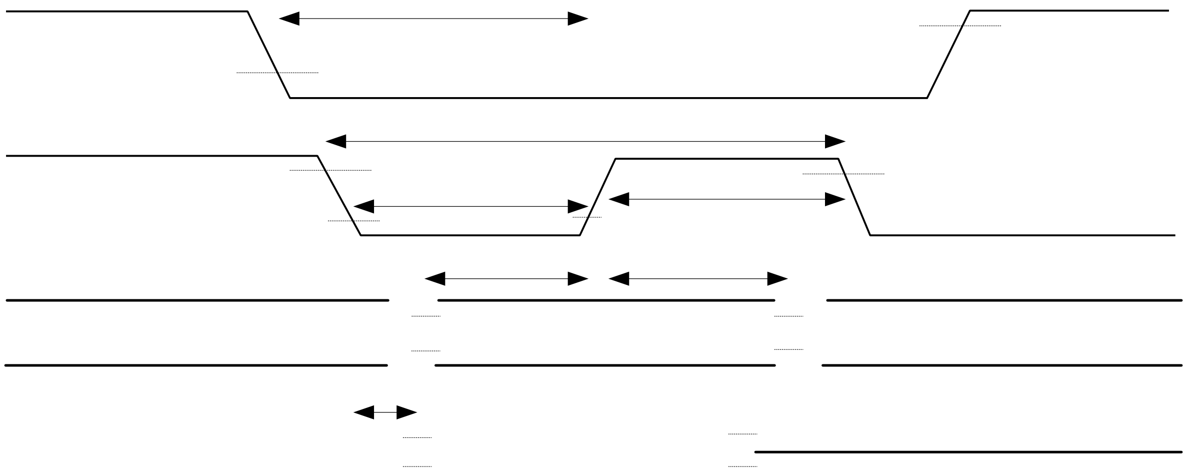


Table 5-21 DBI 3-line Serial Interface Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time (Write)	t_{css}	15		ns
	Chip select setup time (Read)	t_{csh}	60		ns
SCL (write)	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SCL (read)	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO (write)	Data setup time	t_{ds}	7		ns
	Data hold time	t_{dt}	7		ns
SDI/SDO (read)	Read access time	t_{racc}	10	50	ns
	Output disable time	t_{od}	15	50	ns

Figure 5-15 DBI 4-line Serial Interface Timing

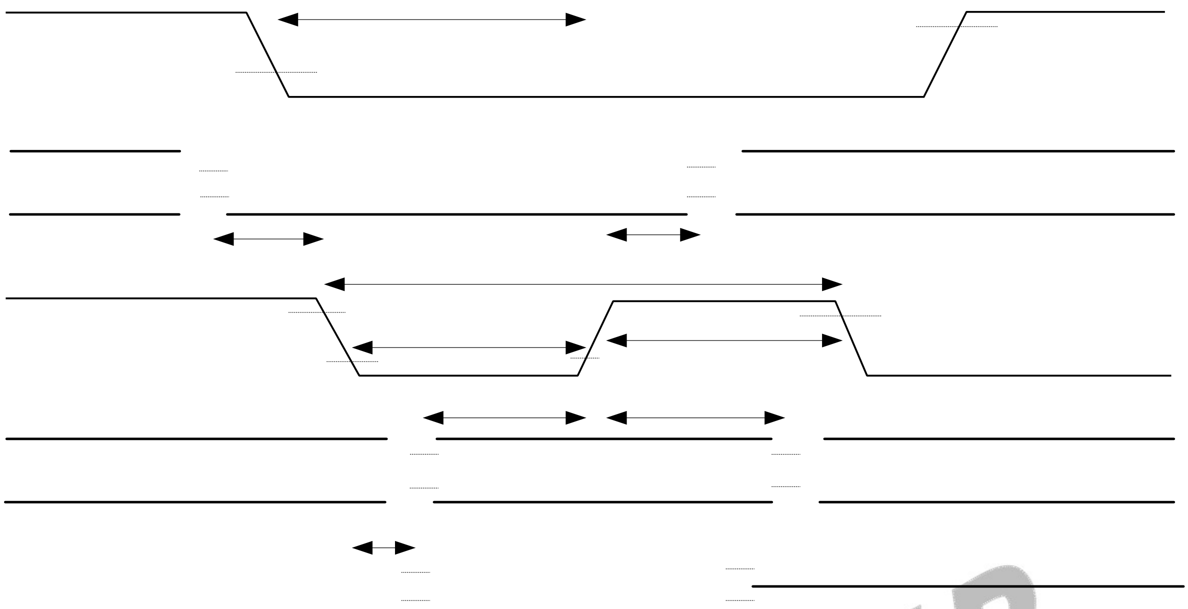


Table 5-22 DBI 4-line Serial Interface Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time (Write)	t_{css}	15		ns
	Chip select setup time (Read)	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time (Write/Read)	t_{ah}	10		ns
SCL (write)	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SCL (read)	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO (write)	Data setup time	t_{ds}	7		ns
	Data hold time	t_{dt}	7		ns
SDI/SDO (read)	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15	50	ns

5.11.4 UART AC Electrical Characteristics

Figure 5-16 UART RX Timing

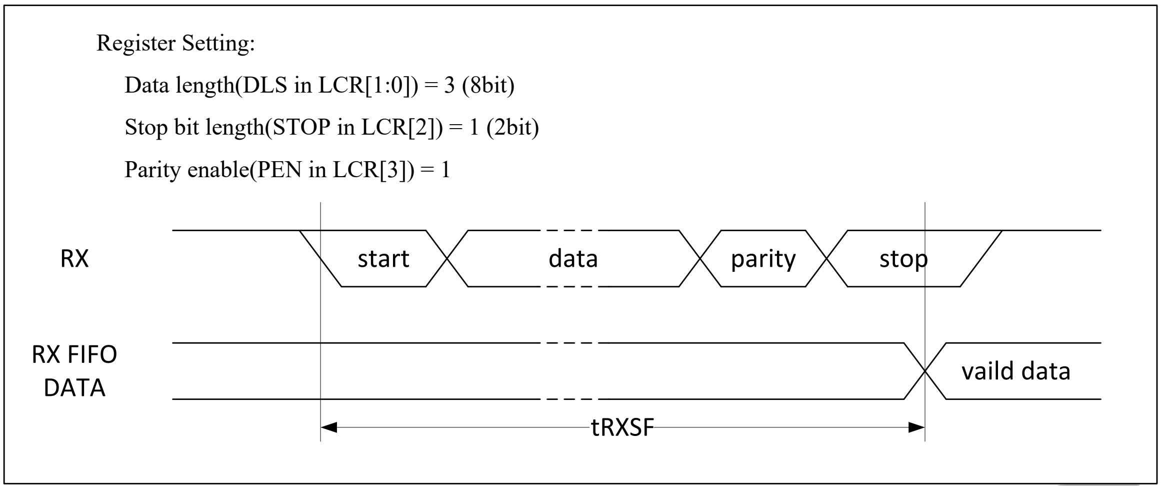


Figure 5-17 UART nCTS Timing

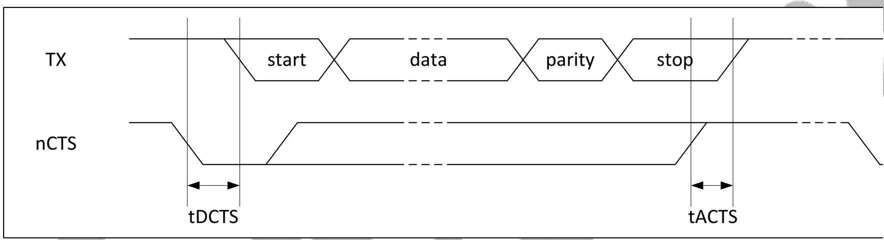


Figure 5-18 UART nRTS Timing

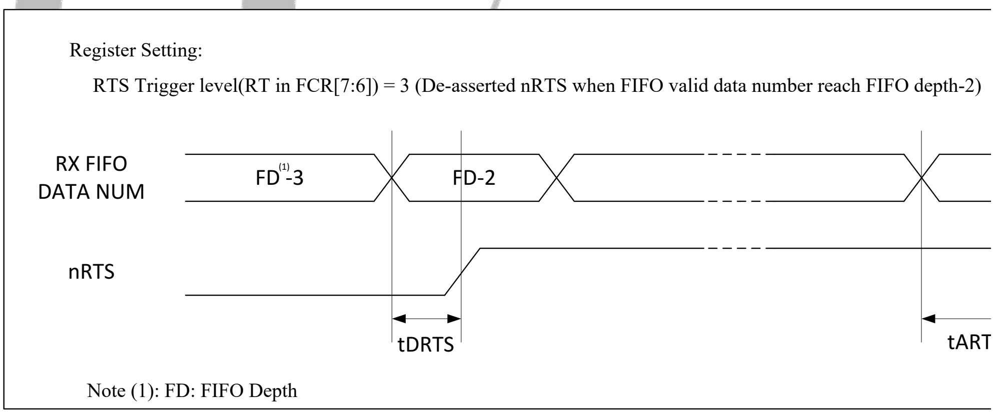


Table 5-23 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5 * BRP(1)	-	11 * BRP(1)	ns
Delay time of de-asserted	tDCTS	-	-	BRP(1)	ns

Parameter	Symbol	Min	Typ	Max	Unit
nCTS to TX start					
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1). BRP: Baud-Rate Period.					

5.11.5 TWI AC Electrical Characteristics

Figure 5-19 TWI Timing

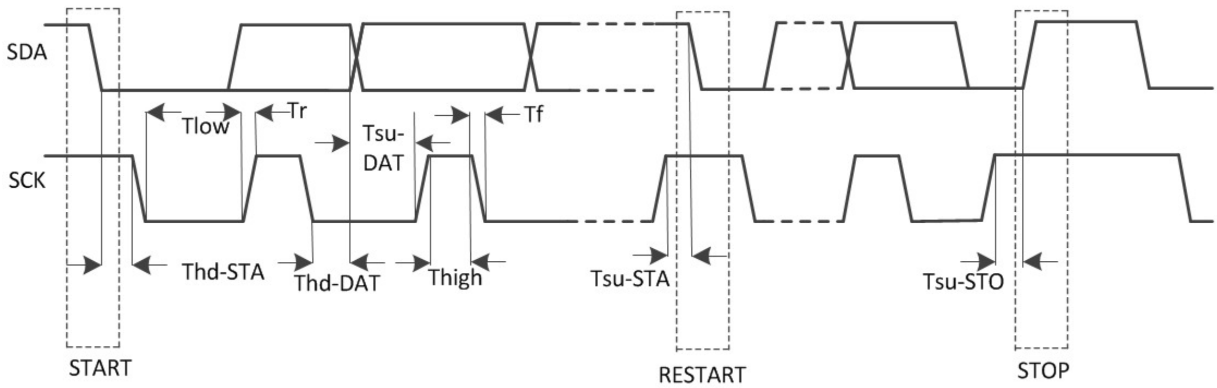


Table 5-24 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us

Parameter	Symbol	Standard mode		Fast mode		Unit
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

5.11.6 I2S/PCM AC Electrical Characteristics

Figure 5-20 I2S/PCM Timing in Master Mode

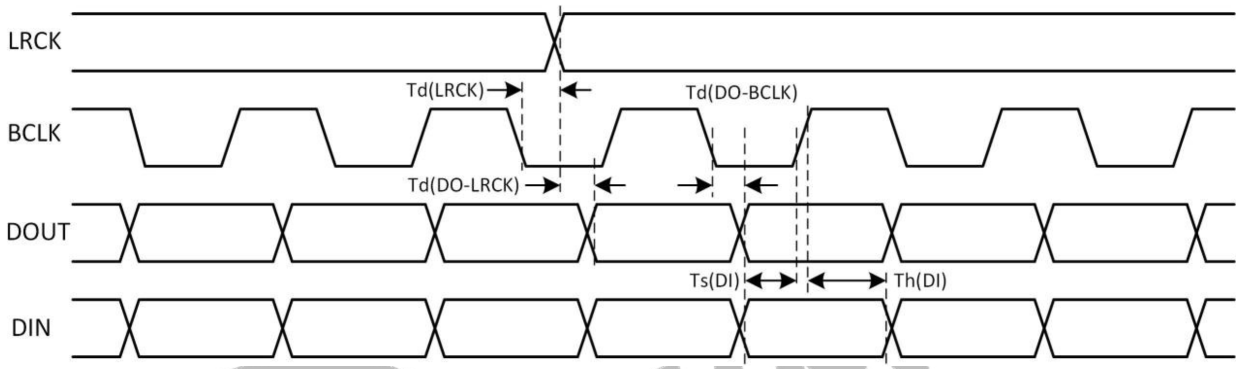


Table 5-25 I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

Figure 5-21 I2S/PCM Timing in Slave Mode

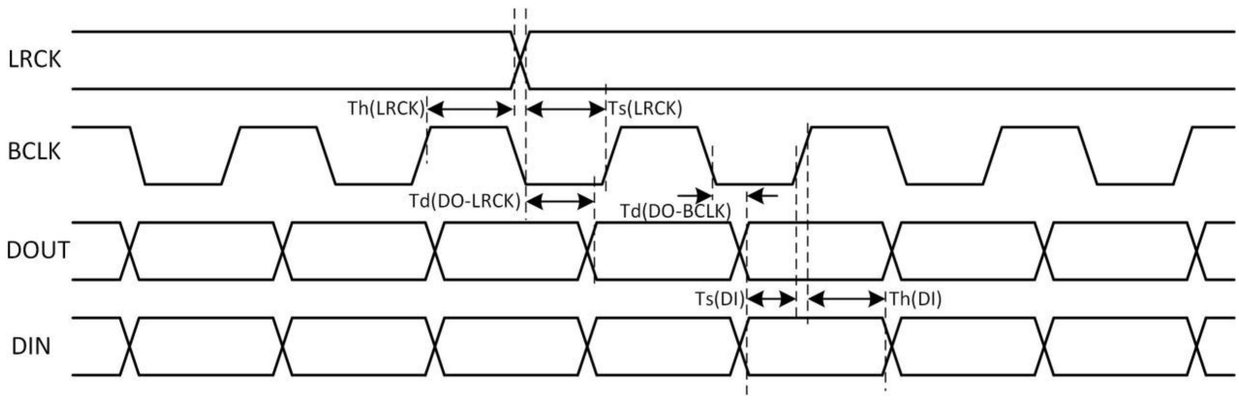


Table 5-26 I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.11.7 DMIC AC Electrical Characteristics

Figure 5-22 DMIC Timing

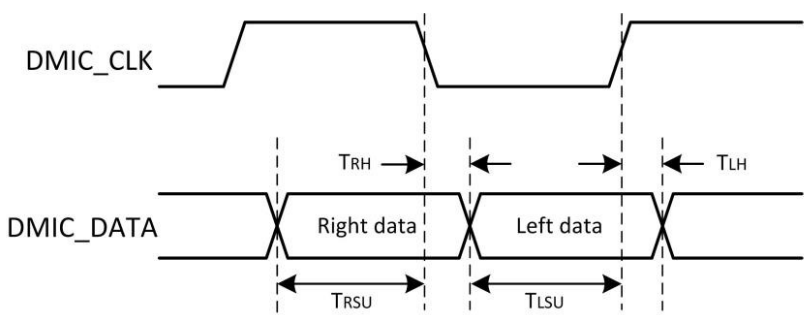


Table 5-27 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA (Right) setup time to falling edge of DMIC_CLK	TRSU	15	-	-	ns
DMIC_DATA (Right) hold time from falling edge of DMIC_CLK	TRH	0	-	-	ns
DMIC_DATA (Left) setup time to rising edge of DMIC_CLK	TLSU	15	-	-	ns
DMIC_DATA (Left) hold time from rising edge of DMIC_CLK	TLH	0	-	-	ns

5.11.8 OWA AC Electrical Characteristics

Figure 5-23 OWA Timing

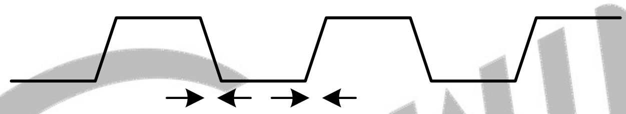


Table 5-28 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns

5.11.9 CIR_RX AC Electrical Characteristics

Figure 5-24 CIR_RX Timing

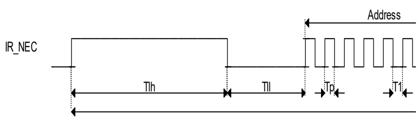


Table 5-29 CIR_RX Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

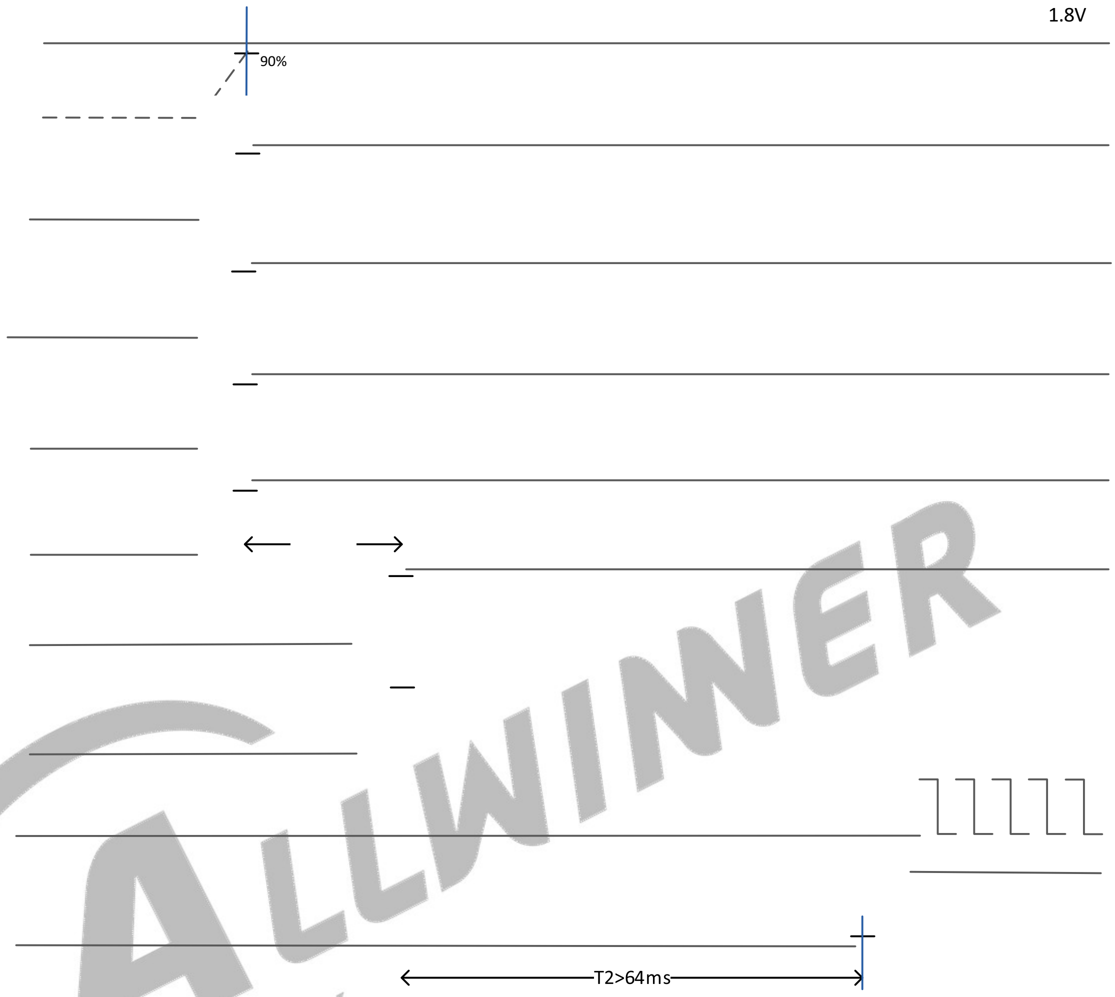
5.12 Power-On and Power-Off Sequence

5.12.1 Power-On Sequence

Figure 5-28 shows an example of the power-on sequence for the H133 device. The description of the power-on sequence is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90–110% of their nominal voltage, unless stated otherwise.
- VCC-RTC must be ramped no later than other power rails.
- VCC-IO must be ramped before VDD-SYS and VDD-CPU with a minimum delay of 2 ms.
- VCC-DRAM needs be stable before SDRAM driver initialization.
- During the entire power on sequence, the RESET signal must be held on low until all other power rails (except 24 MHz CLK) are stable for more than 64 ms.
- 24MHz clock starts oscillating after the RESET signal is released.

Figure 5-25 Power-On Timing

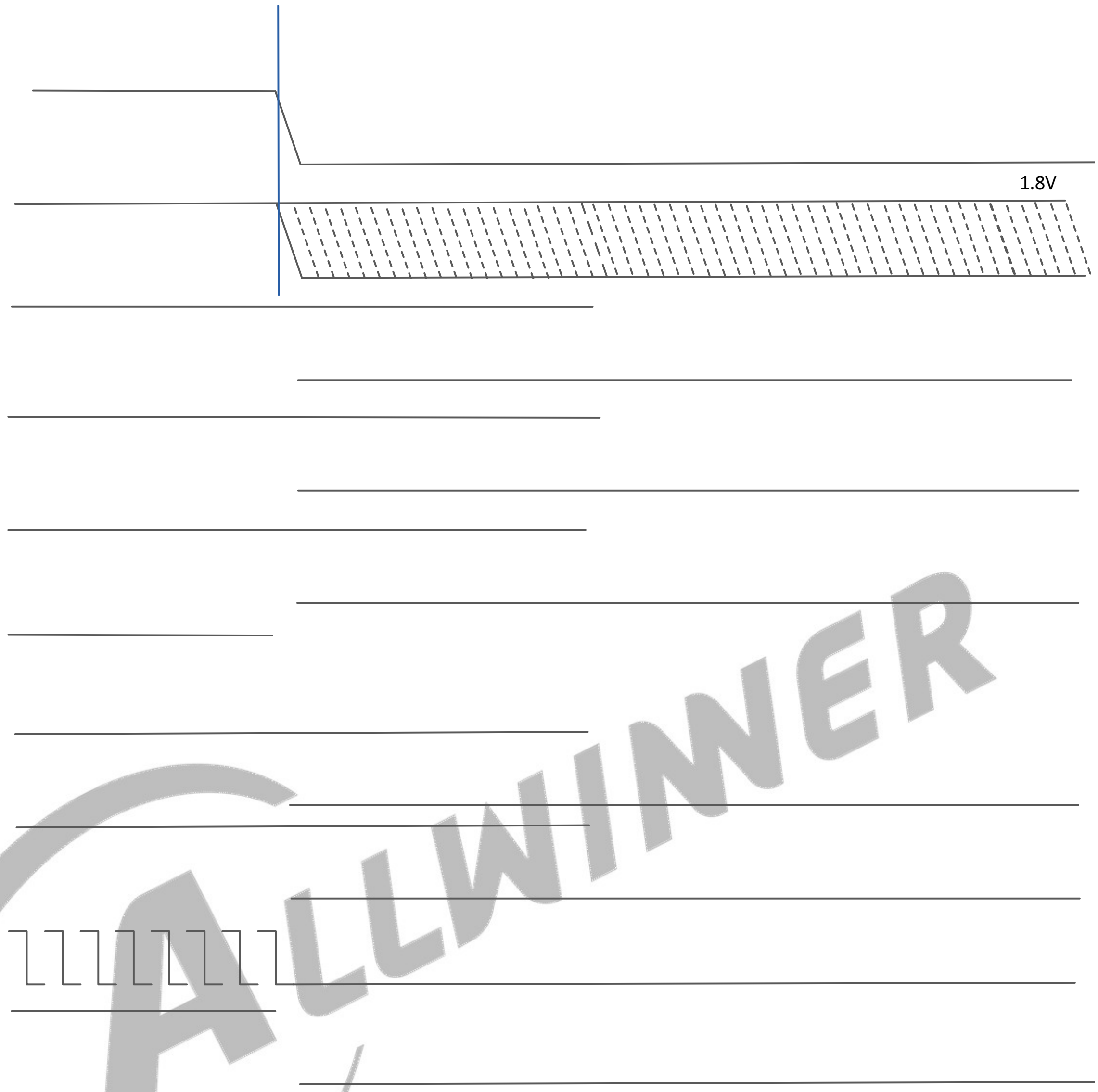


5.12.2 Power-Off Sequence

The power-off requirements are as follows.

- After the RESET signal goes low, the 24 MHz clock starts to stop oscillating.

Figure 5-26 Power-Off Timing



6 Package Thermal Characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in *Table 5-2 Recommended Operating Conditions*.

The maximum chip-junction temperature T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_a max + (P_D max x θ_{JA})

Where:

T_a max is the maximum ambient temperature in °C.

P_D max is the maximum power dissipation.

θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W.

°C/W = degrees Celsius per watt.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the H133. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-1 H133 Package Thermal Characteristics

Symbol	Parameter	Min	Typ[1]	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	TBD	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	TBD	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	TBD	-	°C/W

1. Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

7 Pin Assignment

7.1 Pin Map

The following figure shows the pin map of the H133.

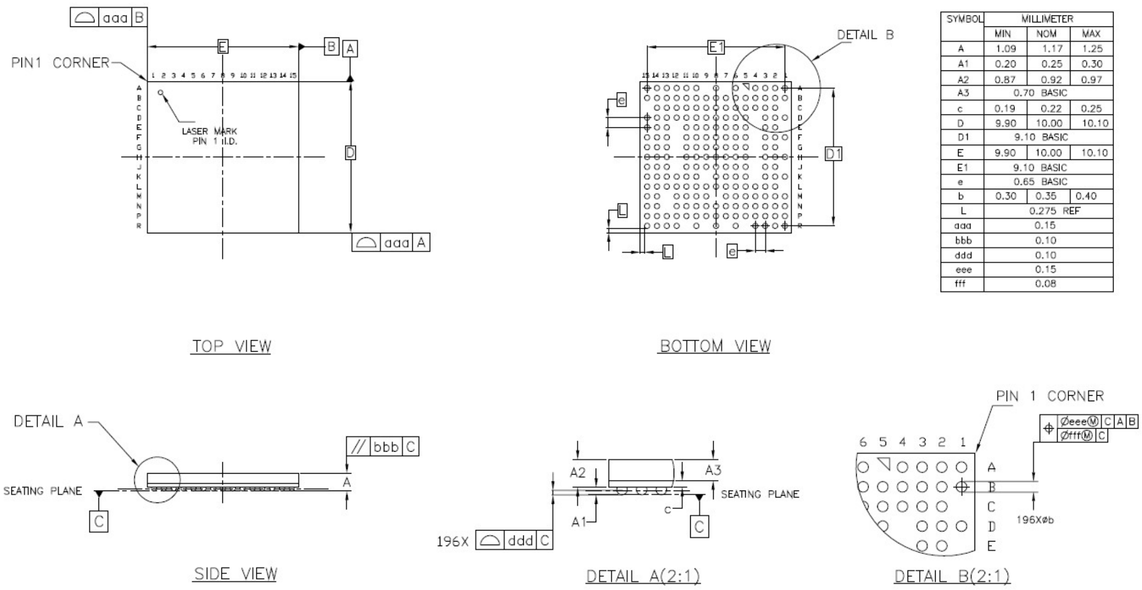
Figure 7-1 H133 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	GND	PG9	PG7	PG15		PG4		PG2		USB0_DM	USB1_DM	HPOUTR	AGND	VRA2	GND
B	PF0	PG16	PG8	PG6	PG13	PG11	PG3	PG0	PG18	USB0_DP	USB1_DP	HPOUTFB	VRA1	PB12	PB11
C		PF2	PF1	PG10	PG14	PG12	PG5	GND	PG1	PG17	GPADC0	HPOUTL	PB10	PB9	
D	PF5	PF4	PF3		VCC_PG	VDD_CPU	VDD_CPU	VDD_CPUFB	VDD_SYS	VDD_SYS	GND	AVCC	PB8	PB1	PB0
E		PF6	GND		VCC_PF	VDD_CPU	VDD_CPU	GND	VDD_SYS	VDD_SYS	HPVCC		GND	HTX2P	HTX2N
F	PC4	PC3	PC2		VCC_PC	GND	GND	GND	GND	GND	VCC_IO		HSCL	HTX1P	HTX1N
G		PC6	PC5		VCC_PLL	GND	GND	GND	GND	GND	VCC_LVDS		HSDA	HTX0P	HTX0N
H	REFCLK_OUT	GND	PC7		VCC_RTC	GND	GND	GND	GND	GND	VCC_HDMI		GND	HTXCP	HTXCN
J		DXIN	DXOUT		LDOA_OUT	GND	VCC_DRAM	VCC_DRAM	GND	GND	VCC_PD		HCEC	PD9	PD8
K	X32KIN	X32KOUT	GND		LDO_IN	LDOB_OUT	VCC_DRAM	VCC_DRAM		SZQ	SVREF	GND	HHPD	PD7	PD6
L		GND	RESET	SDQ0	GND	SDQM0	SBA0	GND	SRAS	SA3	SA4	SA13	GND	PD5	PD4
M	SDQ9	SDQ11	SDQ15	SDQ1	SDQ2	SDQ3	SODT0		SA6	SA2	SA1	SA15		PD3	PD2
N	SDQS1P	SDQ13	SDQ12	SDQ4	SDQ5	GND	SCKN	SBA2	GND	SA10	SA0	GND		PD1	PD0
P	SDQS1N	SDQ10	GND	SDQ7	SDQ6	SDQS0N	SCKP	SCS0	SBA1	SA11	SA9	SA8	SA7	SRST	SA14
R	GND	SDQ14	SDQ8	SDQM1		SDQS0P		SCKE0		SWE		SCAS	SA5	SA12	GND

7.2 Package Dimension

Figure 7-2 shows the top, bottom, and side views of H133 package dimension.

Figure 7-2 H133 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.09	1.17	1.25
A1	0.20	0.25	0.30
A2	0.87	0.92	0.97
A3	0.70 BASIC		
c	0.19	0.22	0.25
D	9.90	10.00	10.10
D1	9.10 BASIC		
E	9.90	10.00	10.10
E1	9.10 BASIC		
e	0.65 BASIC		
b	0.30	0.35	0.40
L	0.275 REF		
aaa	0.15		
bbb	0.10		
ddd	0.10		
eee	0.15		
fff	0.08		

8 Carrier, Storage and Baking Information

8.1 Carrier

8.1.1 Matrix Tray Information

Table 8-1 shows the H133 matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 136 mm x 7.62 mm	240
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

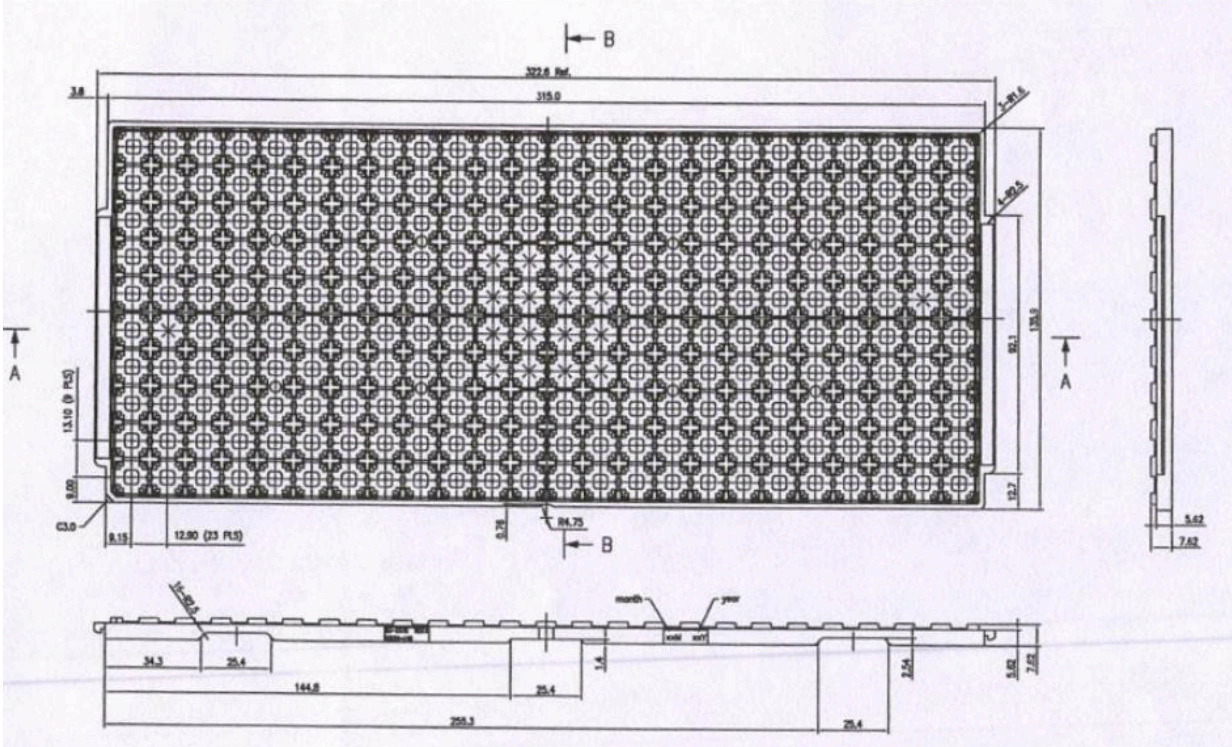
Table 8-2 shows the H133 packing quantity.

Table 8-2 H133 Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
H133	10 x 10	240	10	2400	6	14400

Figure 8-1 shows tray dimension drawing of the H133.

Figure 8-1 H133 Tray Dimension Drawing



8.2 Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-4 defines all MSL.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH

MSL	Out-of-bag floor life	Comments
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The H133 device samples are classified as MSL3.

8.2.2 Bagged Storage Conditions

Table 8-5 defines the shelf life of the H133 device samples.

Table 8-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20–26°C
Storage humidity	40%–60%RH
Shelf life	12 months

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of the H133 is as follows.

Table 8-5 Out-of-bag Duration

Storage temperature	20–26°C
Storage humidity	40%–60%RH
Moisture sensitive level (MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, refer to the latest ***IPC/JEDEC J-STD-020C***.

8.3 Baking

It is not necessary to bake the H133 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the H133 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake the H133 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

Figure 9-1 shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

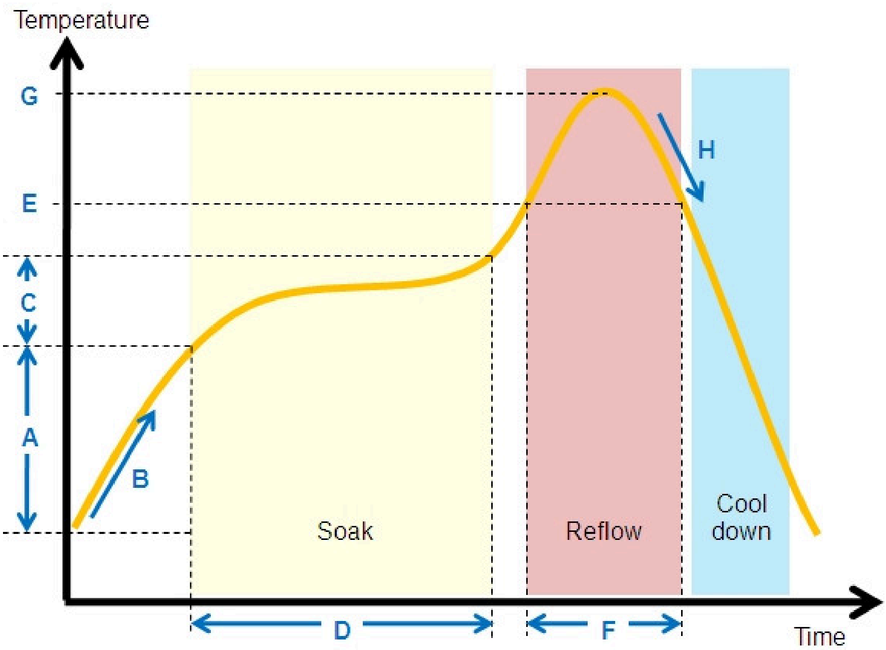


Table 9-1 Lead-free Reflow Profile Conditions

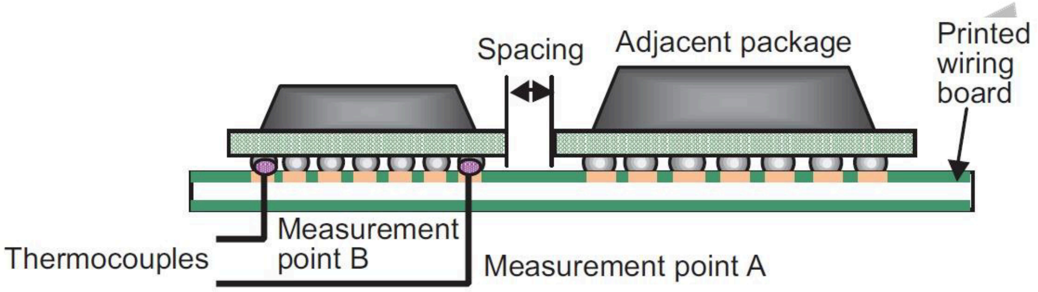
	QTI typical SMT reflow profile conditions (for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5–2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	**Reflow condition**
G	Peak temperature	240–250 °C
H	Cool down temperature rate	≤4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

Figure 9-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 FT/QA/QC Test

10.1 FT Test

FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.

10.2 QA Test

QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

10.3 QC Test

QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

11 Part Marking

Figure 11-1 shows the H133 marking.

Figure 11-1 H133 Marking

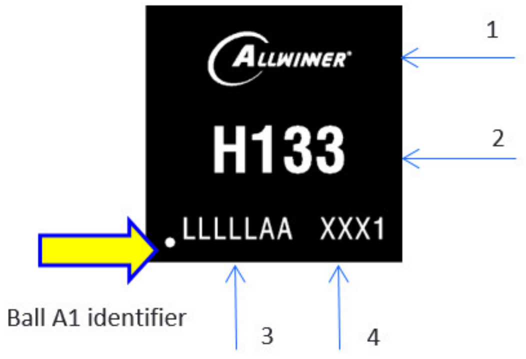


Table 11-1 describes the H133 marking definitions.

Table 11-1 H133 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	H133	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

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