V851S&V851SE
Datasheet

Revision 1.0

July 27, 2022

Revision History

Revision	Date	Author	Description
1.0	July 27, 2022	AWA1896	Initial release

About This Document

Purpose and Scope

This document describes the features, logical structures, functions, operating modes, and related registers of each module about V851S/V851SE This document also describes interface timings and related parameters, pins, pin usages, performance parameters, and package dimension of V851S/V851SE in detail.

CAUTION

The document defines two devices: V851S and V851SE. Unless other stated, their contents are consistent.

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Reset Value Conventions

In the register definition tables:

If other column value in the row of a bit or multiple bits is "/", this bit of these multiple bits are unused.

If the default value of a bit or multiple bits is "UDF", this default value is undefined.

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression, X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

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1 Product Description

1.1 Overview

V851S/V851SE is a new generation of high-performance H.264/H.265 encoding SoC targeted for the field of IP Camera. It integrates the single Cortex-A7 core@900MHz, RISC-V@600MHz and 0.5 Tops NPU and supports various intelligent application such as human detection and crossing alarm. V851S/V851SE is also designed with a new generation of high-performance ISP image processor and video encoder with professional encoding quality, low encoding bit rate and mainstream-level image processing capability. In addition, V851S/V851SE supports 64MB DDR2 and rich peripheral interfaces, such as USB, SDIO and Ethernet, to meet the requirements of various IP Camera products.

1.2 Device Differences

The V851S/V851SE is configured with different sets of features in different devices. The feature differences across different devices are shown in the following table. For detailded pins, see the ***V851S_PINOUT.xlsx*** and ***V851SE_PINOUT.xlsx***

Table 1-1 Device Feature Differences

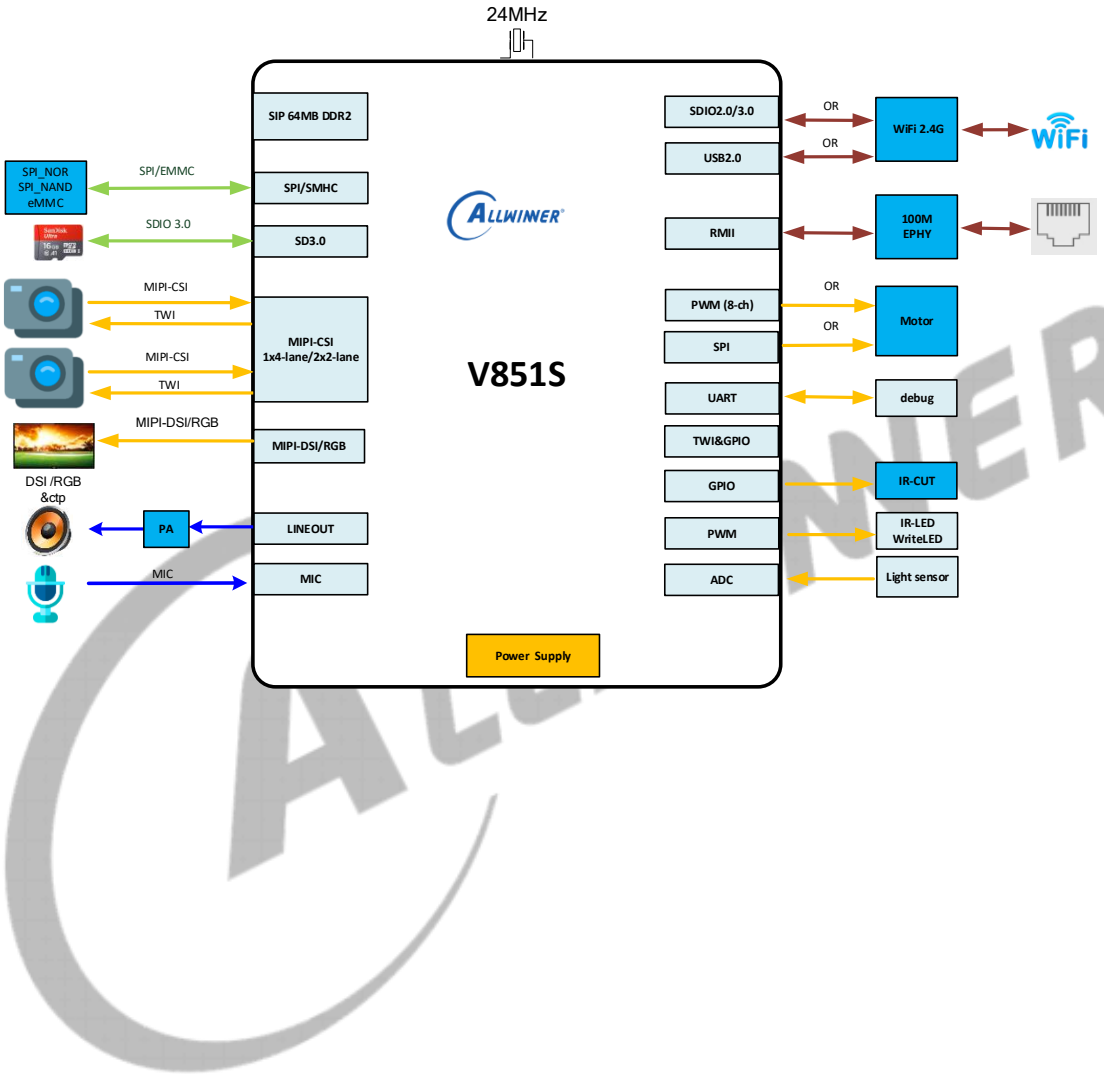
Contents	V851S	V851SE
Ethernet	10/100 Mbit/s Ethernet port with RMII interface	SIP 100M EPHY
GPIOs	6 ports (PA,PC,PD,PE,PF,PH)	5 ports (PA,PC,PE,PF,PH)
LCD	Parallel RGB, Serial RGB, i8080, BT656	Not supplort
SPI	SPI x4 (SPI0, SPI1, SPI2, SPI3)	SPI x3 (SPI0, SPI2, SPI3)
SPI_DBI	Support	Not support
MIPI DSI	1 x 2-lane	Not support

1.3 Application Scenarios

1.3.1 V851S

The following figure shows the application scenarios of V851S.

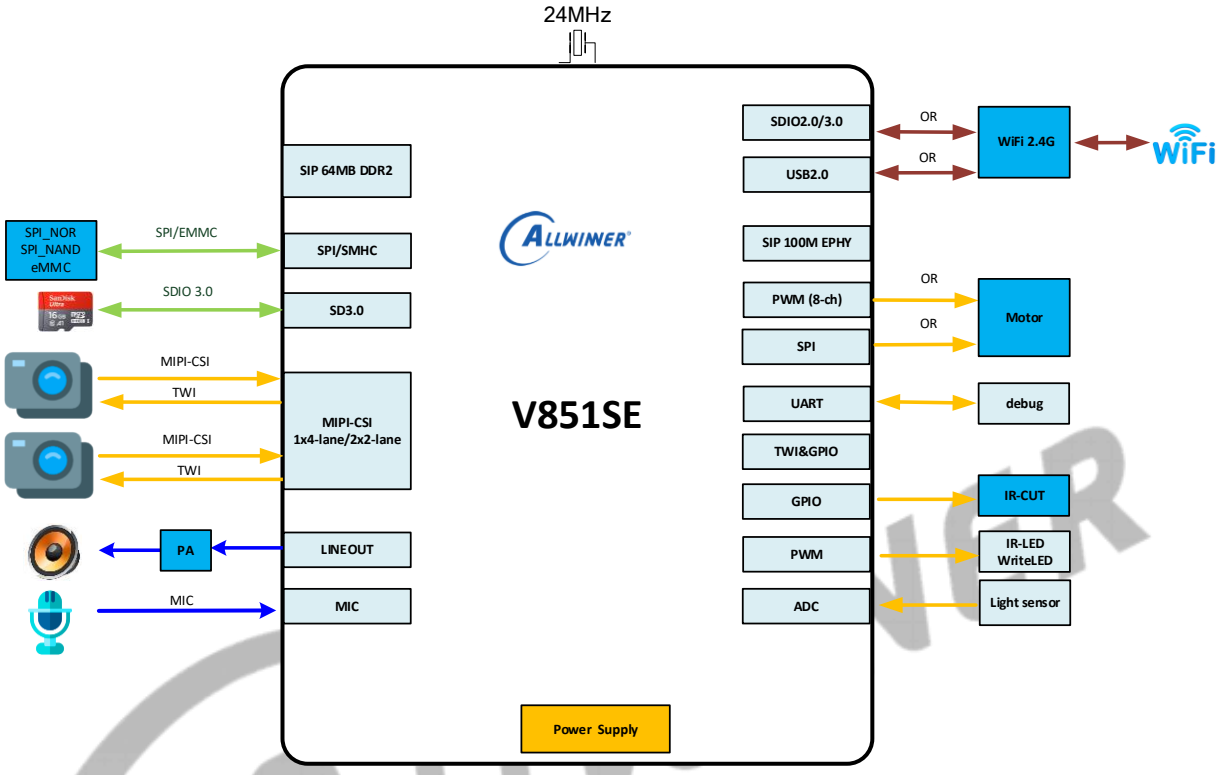
Figure 1-1 V851S HD IP Camera Solution



1.3.2 V851SE

The following figure shows the application scenarios of V851SE.

Figure 1-2 V851SE HD IP Camera Solution



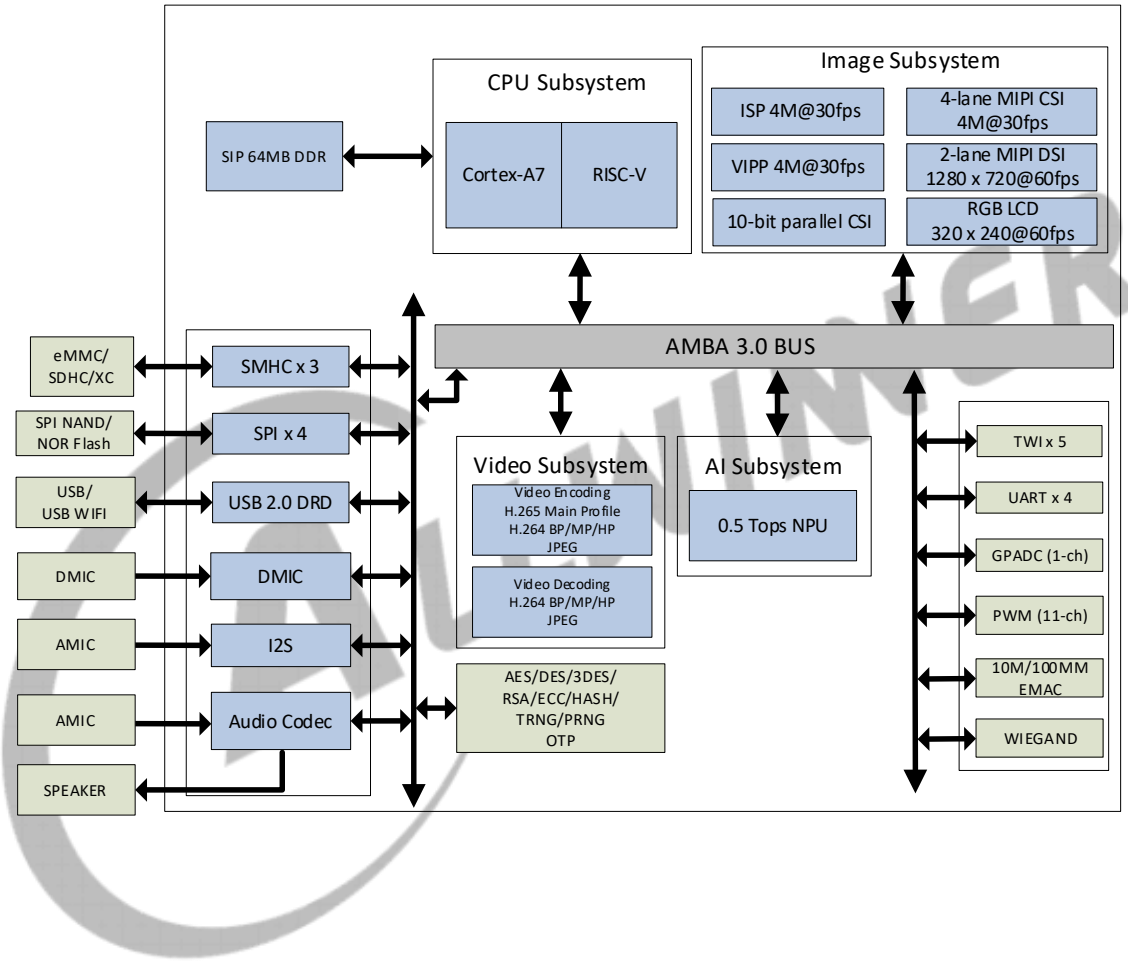
1.4 Architecture

1.4.1 Block Diagram

1.4.1.1 V851S

The following figure shows the logic block diagram of the V851S.

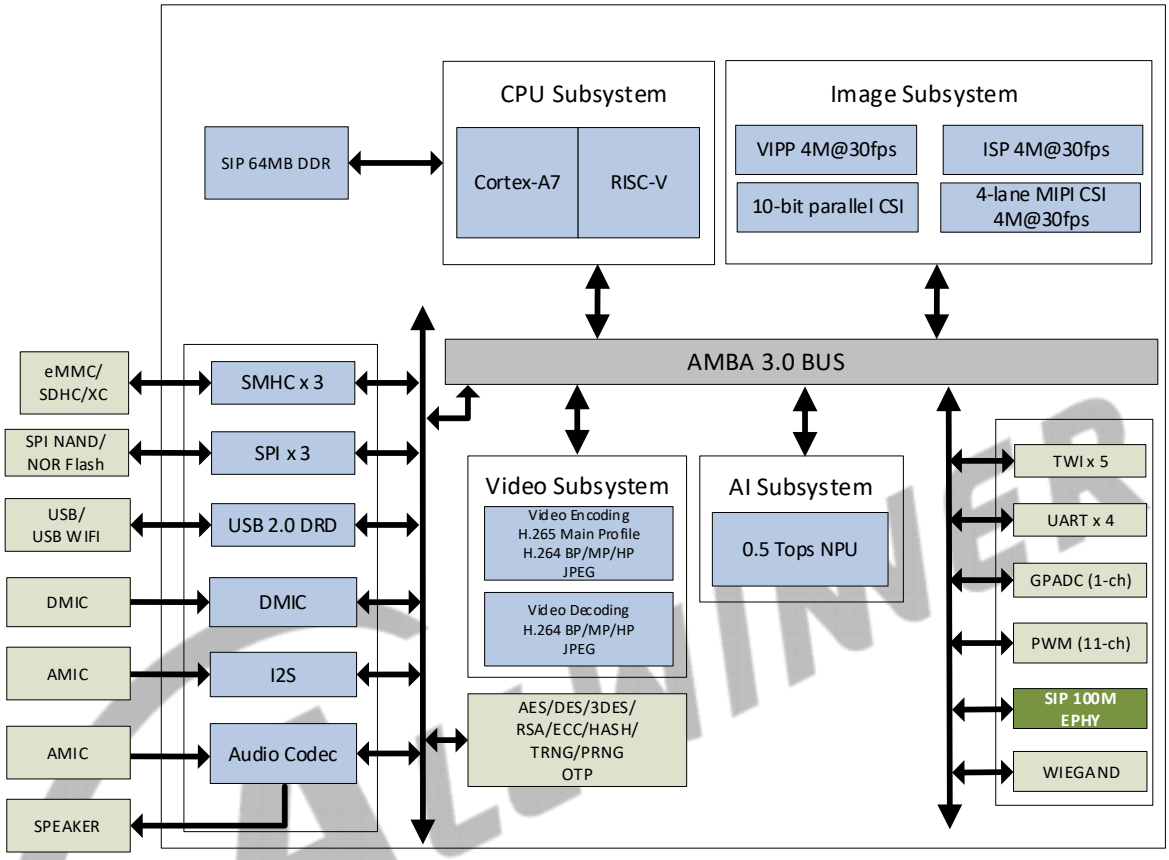
Figure 1-3 V851S Logic Block Diagram



1.4.1.2 V851SE

The following figure shows the logic block diagram of the V851SE.

Figure 1-4 V851SE Logic Block Diagram



1.4.2 CPU Architecture

- Cortex-A7 CPU core, up to 900 MHz

  Supports 32 KB I-cache, 32 KB D-cache, and 128 KB L2 cache

- RISC-V core, up to 600MHz

  Supports 16 KB I-cache and 16 KB D-cache

1.4.3 NPU Architecture

- Maximum performance up to 0.5 Tops
- Embedded 128KB internal buffer
- Supports deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, and so on

1.4.4 Video and Graphics Processing

- Supports horizontal flip, vertical flip, and clockwise 0/90/180/270 degree image rotation

- Supports 2 Video channels, one up to 1080p@60fps, the other up to 720p@60fps
- Supports 1 UI channel, up to 1080p@60fps
- Blending of 2 Video channels and 1 UI channel
- Supports SmartColor for excellent display experience

1.4.5 Video Encoding/Decoding Performance

- H.264 BP/MP/HP encoding
- H.265 MP encoding
- H.264/H.265 supports I/P frame type
- MJPEG/JPEG baseline encoding
- H.264/JPEG decoding
- Maximum resolution for H.264/H.265 decoding is 16 megapixels (4096x4096)
- A maximum of eight ROIs
- CBR, VBR and FIXEDQP modes
- JPEG encder supports 1080p@60fps@400MHz
- H.264/H.265 encoder supports 3840x2160@20fps@400MHz
- H.264/H.265 multi-stream real-time encoding capability: 5M@25fps + 720p@25fps

1.4.6 Video Output

NOTE

V851SE does not support MIPI DSI and LCD.

1.4.6.1 MIPI DSI

- Compliance with MIPI DSI V1.02 and MIPI DPHY V1.0
- Supports 2-lane MIPI DSI, up to 1280x720@60fps
- Supports normal mode and burst mode
- Up to 1.0 Gbps/Lane

1.4.6.2 TCONLCD

- i8080 interface, up to 800 x 480@60fps

- Serial RGB interface, up to 800 x 480@60fps
- RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- supports BT656 interface

1.4.7 Video Input

1.4.7.1 ISP

- Supports 1 individual image signal processor(ISP), with maximum resolution of 2560 x 1440 (online mode)
- Maximum frame rate of 4M@30fps
- Supports offline mode
- Supports WDR spilt, 2F-WDR line-based stitch, dynamic range compression (DRC), tone mapping, digital gain, gamma correction, defect pixel correction (DPC), cross talk correction (CTC), and chromatic aberration correction (CAC)
- Supports 2D/3D noise reduction, bayer interpolation, sharpen, white balance, and color enhancement
- Adjustable 3A funtions: automatic white balance (AWB), automatic exposure (AE), and automatic focus (AF)
- Supports anti-flick detection statistics, and histogram statistics
- Supports graphics mirror and flip
- Supports Lens Distortion Correction(LDC) and Fish Eye Correction(FEC)

1.4.7.2 VIPP

- Four VIPP YUV422 or YUV420 outputs
- Maximum resolution of 2560x1440
- Each VIPP has one sub-VIPP in online mode
- Each VIPP has maximum four sub-VIPPs for time division multiplexing in offline mode
- Functions for each Sub-VIPP
  - Crop
  - 1 to 1/16 scaling for height and width
  - 16 ORLs

1.4.7.3 Parallel CSI

- Supports 10-bit width

- Supports BT.601 and BT.656 interface
- Maximum pixel clock for parallel to 148.5MHz
- Supports ITU-R BT.656 up to 4*720P@30fps

1.4.7.4 MIPI CSI

- Supports one 4-lane MIPI CSI input or two 2-lane MIPI CSI inputs
- Compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00.00
- Up to 1. 2 Gbps/Lane
- maximum video capture resolution for serial interface up to 4M@30fps

1.4.8 Audio Subsystem

1.4.8.1 Audio Codec

- One audio digital-to-analog converter (DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N
- One audio analog-to-digital converter (ADC) channel
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 48 kHz ADC sample rate
  - 95 ± 3dB SNR@A-weight, -80 ± 3dB THD+N
- One audio input:
  - One differential microphone input: MICIN1P/N
- One audio output:
  - One single-ended lineout output: LINEOUTLP
- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA

1.4.8.2 I2S

- One I2S/PCM external interface (I2S1) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA Slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

1.4.8.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

1.4.9 External Peripherals

- Five TWI interfaces: TWI0, TWI1, TWI2, TWI3, and TWI4
- Four UART interfaces: UART0, UART1, UART2, and UART3
- Four SPI interfaces for V851S: SPI0, SPI1, SPI2, and SPI3
- Three SPI interfaces for V851SE: SPI0, SPI2, and SPI3
- Six groups of GPIO pins for V851S: PA, PC, PD, PE, PF and PH
- Five groups of GPIO pins for V851S: PA, PC, PE, PF and PH

- One channel general purpose analog-to-digital converter(GPADC): GPADC0
- One PWM controller(11-ch)

1.4.10 Security System

1.4.10.1 Crypto Engine (CE)

- Supports symmetrical algorithm for encryption and decryption: AES, DES, 3DES
  - Supports ECB, CBC, CTS, CFB, OFB, CBC-MAC, GCM mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports ECB, CBC, CTR, CBC-MAC mode for DES
- Supports hash algorithm for tamper proofing: MD5, SHA, HMAC
  - Supports SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - Supports HMAC-SHA1, HMAC-SHA256 for HMAC
  - Supports multi-package mode for HMAC/SHA1/SHA224/SHA256/SHA384/SHA512
  - Supports hardware padding
- Supports public key algorithm: RSA, ECC
  - RSA supports 512/1024/2048/3072/4096-bit width
  - ECC supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG with 15-bit seed
- Supports 256-bit hardware TRNG
- Supports secure and non-secure interfaces respectively, each world issues task request through its own interface
- Supports word-aligned address for all configurations

1.4.10.2 Security ID (SID)

- Supports 2048 bit eFuse
- Backs up eFuse information by using SID_SRAM
- Burning the key to the SID
- Reading the key use status in the SID
- Loading the key to the CE

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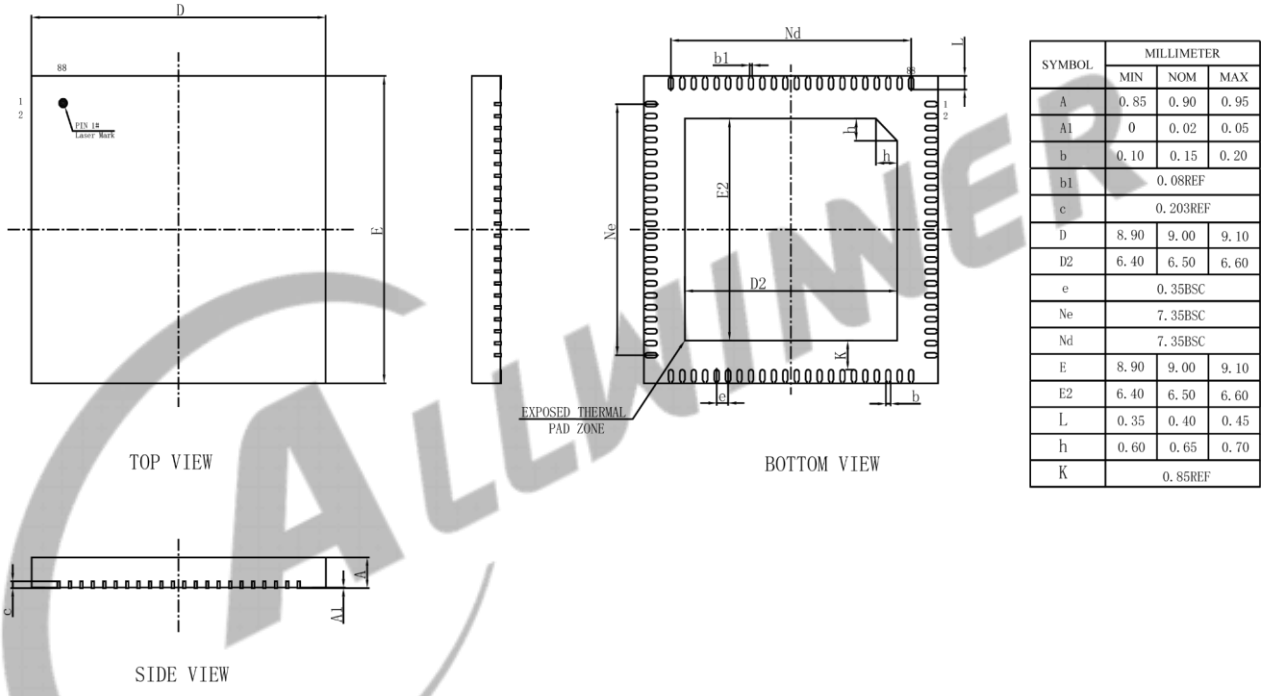
2 Hardware

2.1 Package and Pinout

2.1.1 Package

The V851S/V851SE uses the QFN88 package, it has 88 pins, its body size is 9 mm x 9 mm, and its ball pitch is 0.35 mm. The following figure shows the top, the bottom, and the side views of the V851S/V851SE package dimension.

Figure 2-1 V851S/V851SE Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.203REF		
D	8.90	9.00	9.10
D2	6.40	6.50	6.60
e	0.35BSC		
Ne	7.35BSC		
Nd	7.35BSC		
E	8.90	9.00	9.10
E2	6.40	6.50	6.60
L	0.35	0.40	0.45
h	0.60	0.65	0.70
K	0.85REF		

2.1.2 Pin Quantity

2.1.2.1 V851S

The following table lists the pin quantity of the V851S.

Table 2-1 V851S Pin Quantity

Pin Type	Quantity
I/O	67
Power	17
GND	1
DDR Power	3
Total	88

2.1.2.2 V851SE

The following table lists the pin quantity of the V851SE.

Table 2-2 V851SE Pin Quantity

Pin Type	Quantity
I/O	62
Power	21
GND	2
DDR Power	3
Total	88

2.2 Pin Description

For details about pin description of the V851S/V851SE, see the ***V851S_PINOUT.xlsx*** and ***V851SE_PINOUT.xlsx.***

2.3 Electrical Characteristics

2.3.1 Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

2.3.2 Absolute Maximum Ratings

The device will be damaged if the stresses are beyond the absolute maximum ratings. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 2-3 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device in these or any other conditions beyond the values in the Section 2.3.3 Recommended Operating Conditions is not implied. Exposure to the absolute maximum rated conditions for extended periods may affect the device reliability.

Table 2-3 Absolute Maximum Ratings

Symbol	Parameter	Min(1)	Max(1)	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-PA&VCC-MCSI	Digital GPIO A Power/ MIPI CSI Power	-0.3	2.16	V
VCC-PC	Digital GPIO C Power	-0.3	3.96	V
VCC-PD (Only for V851SE)	Digital GPIO D Power	-0.3	3.96	V

Symbol	Parameter		Min(1)	Max(1)	Unit
VCC-PE	Digital GPIO E Power		-0.3	3.96	V
VCC33-PF (Only for V851SE)	3.3V Digital GPIO F Power		-0.3	3.96	V
VCC33-PF&PD (Only for V851S)	3.3V Digital GPIO F Power 3.3V Digital GPIO D Power		-0.3	3.96	V
VCC-IO	Power Supply for 3.3 V Digital Part		-0.3	3.96	V
VCC-LDOA&PLL	Internal LDOA Output Voltage for Analog Device and IO/Power Supply for System PLL		-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM IO and DDR2		-0.3	2.16	V
VCC-MDSI (Only for V851S)	MIPI DSI Power		-0.3	2.16	V
VCC33-USB	USB Analog Power		-0.3	3.96	V
VDD33	Power Supply for 3.3 V Analog Part		-0.3	3.96	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
VDD-SYS	Power Supply for System		-0.3	1.08	V
V_{ESD}	Electrostatic Discharge(2)	Human Body Model(HBM)(3)	-2000	2000	V
		Charged Device Model(CDM)(4)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(6)		Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

2.3.3 Recommended Operating Conditions

The following table describes the operating conditions of the V851S/V851SE.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 2-4 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
VCC-IO	Power Supply for 3.3V Digital Part	2.97	3.3	3.63	V

Symbol	Parameter	Min	Typ	Max	Unit
VCC-PA&VCC-MCSI	Power Supply for Port A/ MIPI CSI Power 1.8V voltage	1.62	1.8	1.98	V
VCC-PC	Power Supply for Port C 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PD (Only for V851SE)	Power Supply for Port D 3.3V voltage	2.97	3.3	3.63	V
VCC-PE	Power Supply for Port E 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC33-PF (Only for V851SE)	Power Supply for Port F 3.3V voltage	2.97	3.3	3.63	V
VCC33-PF&PD(Only for V851S)	Power Supply for Port F/D 3.3V voltage	2.97	3.3	3.63	V
VCC-LDOA&PLL	Internal LDOA Output Voltage for Analog Device and IO/Power Supply for System PLL	1.746	1.8	1.854	V
VCC-MDSI (Only for V851S)	MIPI DSI Power	1.71	1.8	1.89	V
VCC-DRAM	Power Supply for DDR2 IO Domain	1.425 1.7	1.5 1.8	1.575 1.9	V
VCC33-USB	3.3V Power Supply for USB	2.97	3.3	3.63	V
VDD33	Power Supply for 3.3V Analog Part	2.97	3.3	3.63	V
VDD-SYS	Power Supply for System	0.9	-	1.05	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power	1.7	1.8	1.95	V

2.3.4 Temperature and Thermal Resistance Parameters

2.3.4.1 Temperature

The following tables describe the temperature of V851S and V851SE.

Table 2-5 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
Ta	Ambient Operating Temperature	-20	75	°C
T_{STG}	Storage Temperature	-40	150	°C

Table 2-6 Junction Temperature

Chip	Working Junction Temperature (T_j)		Destructive Junction Temperature(2)	Unit
	Min	Max(1)		
V851S V851SE	-20	115	125	°C

(1) The junction temperature of the chip should be less than or equal to this value under normal operating conditions.

(2) The junction temperature of chip should not be more than this value under any conditions.

2.3.4.2 Thermal Resistance Parameters

The following table shows thermal resistance parameters. The following thermal resistance characteristics is based on JEDEC JESD51 standard, because the actual system design could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board (2s2p), natural convection, no air flow.

Table 2-7 V851S Thermal Resistance Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	-	21.1	-	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	-	6.5	-	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	-	4.15	-	°C/W

Table 2-8 V851SE Thermal Resistance Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	-	21.212	-	°C/W
Junction-to-Board Thermal Resistance	θ_{JB}	-	6.3	-	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	-	4.2	-	°C/W

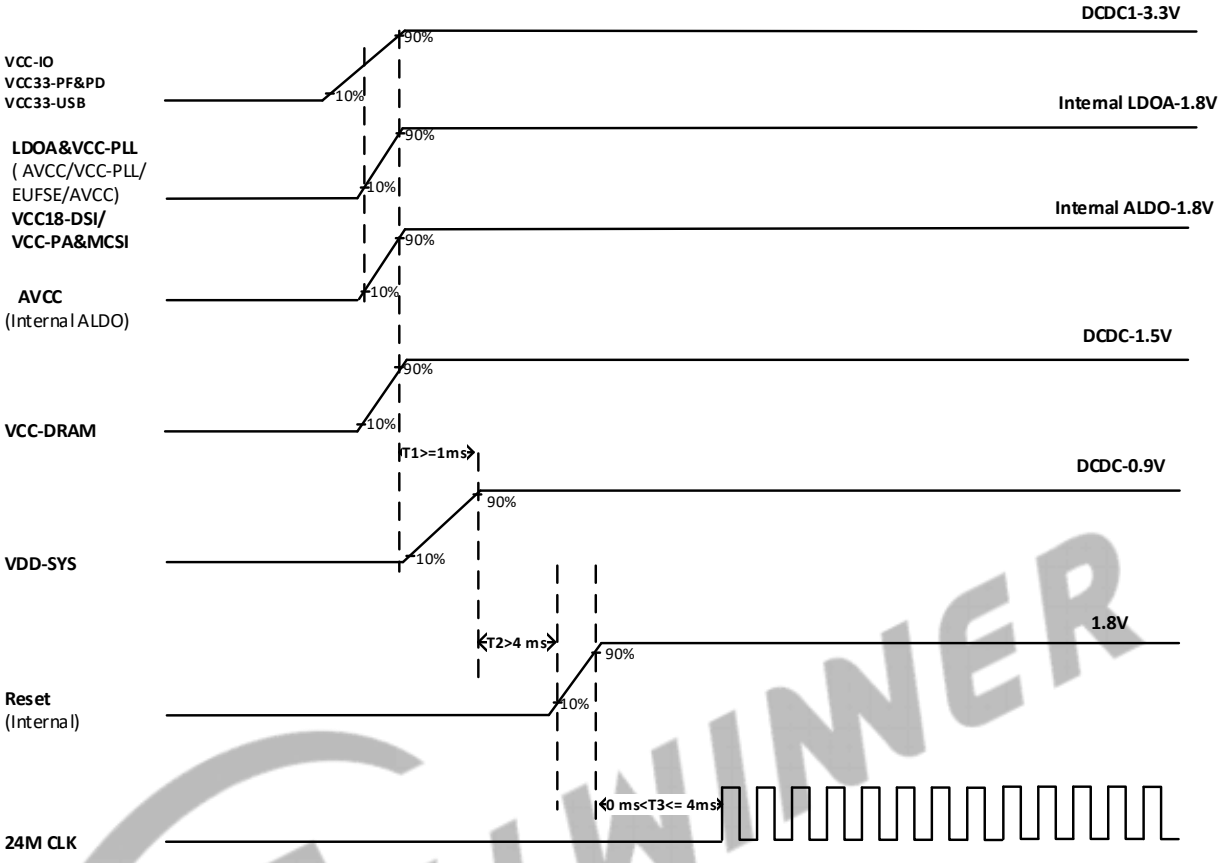
2.3.5 Power-On and Power-Off Sequences

The following figure shows an example of the sequence for V851S/V851SE device.

The description of the power-on sequence for V851S/V851SE is as follows:

- VCC33-PF&PD starts to ramp first
- VDD-SYS must be ramped at least 1ms after LDOA&VCC-PLL is stable and at least 8ms before reset signal starts to ramp.
- 24MHz clock starts oscillatIng 4 ms after the reset signal is released.

Figure 2-2 V851S/V851SE Power on Sequence



During power-off, all powers start to ramp down at the same time, and the ramp rate of each power rail is generated by the load on the power.

2.3.6 DC Electrical Parameters

The following table summarizes the DC electrical characteristics of the V851S.

Table 2-9 DC Electrical Characteristics

(VCC-IO/VCC-PA/VCC-PC/VCC-PD/VCC-PE/VCC-PF)

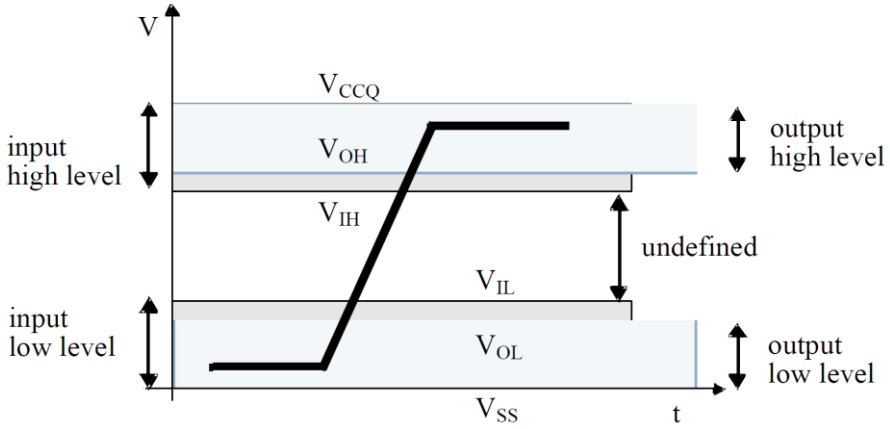
Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	PC1 to PC10, PF3	12	15	18	kΩ
		Other GPIOs	80	100	120	kΩ
R_{PD}	Input Pull-down Resistance	PC1 to PC10, PF3	12	15	18	kΩ
		Other GPIOs	80	100	120	kΩ
I_{IH}	High-Level Input Current		-		10	uA
I_{IL}	Low-Level Input Current		-	-	10	uA

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	High-Level Output Voltage	VCC-IO - 0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

2.3.7 SDIO Electrical Parameters

The SDIO electrical parameters are related to the different supply voltage.

Figure 2-3 SDIO Voltage Waveform



The following table shows 3.3V SDIO electrical parameters.

Table 2-10 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7	3.3	3.6	V
V_{OH}	Output high-level voltage	0.75* V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS}- 0.3	-	0.25* V_{CCQ}	V

The following table shows 1.8V SDIO electrical parameters.

Table 2-11 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7	1.8	1.95	V
V_{OH}	Output HIGH voltage	V_{CCQ} -0.45	-	-	V
V_{OL}	Output LOW voltage	-	-	0.45	V
V_{IH}	Input HIGH voltage	0.625* V_{CCQ} (1)	-	V_{CCQ} + 0.3	V

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input LOW voltage	V_{SS} - 0.3	-	0.35* V_{CCQ} (2)	V

NOTE

0.7 * VDD for MMC4.3 or lower. 0.3 * VDD for MMC4.3 or lower.

2.3.8 GPADC Electrical Characteristics

The GPADC contains a 1-ch analog-to-digital (ADC) converter. The GPADC is a type of the successive approximation register (SAR) converter.

Table 2-12 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Quantizing Error	-	8	-	bits
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

2.3.9 Audio Codec Electrical Parameters

The following table shows audio codec electrical parameters.

Test Conditions:

VDD-SYS = 0.9V , AVCC= 1.8V , Ta= 25°C , 1kHz sinusoid signal, DAC fs = 48 KHz, ADC fs = 16 KHz, input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 2-13 Audio Codec Electrical Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DAC to LINEOUTLP (48 KHz)**					
	Full-scale	0dBFS 1kHz	-	0.54	-	Vrms
	SNR(A-weighted)	0data	-	96	-	dB
	THD+N	0dBFS 1kHz	-	-85	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-	-	dB
ADC Path	**MIC via ADC (16 KHz)**					
	Output Level	MICP=3.3Vpp/2,MICN=3.3Vpp/2,1kHz,0dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	97	-	dB
	THD+N		-	-88	-	dB
	Output Level	MICP=1.695Vpp/2,MICN=1.695Vpp/2,1kHz,6d	-	880	-	mFFS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	SNR(A-weighted)	B Gain	-	96	-	dB
	THD+N		-	-90	-	dB
	Output Level	MICP=0.788Vpp/2,MICN=0.788Vpp/2,1kHz,12 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	94	-	dB
	THD+N		-	-85	-	dB
	Output Level	MICP=0.392Vpp/2,MICN=0.392Vpp/2,1kHz,18 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	92	-	dB
	THD+N		-	-83	-	dB
	Output Level	MICP=0.197Vpp/2,MICN=0.197Vpp/2,1kHz,24 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	88	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=0.101Vpp/2,MICN=0.101Vpp/2,1kHz,30 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	83	-	dB
	THD+N		-	-74	-	dB
	Output Level	MICP=0.053Vpp/2,MICN=0.053Vpp/2,1kHz,36 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	76	-	dB
	THD+N		-	-68	-	dB

2.3.10 High Speed External Clock Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator.

Table 2-14 High-speed 24 MHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency		24		MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-30		+30	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	6.5	-	pF

1. The 30 ppm frequency stability and tolerance can meet the requirement of V851S/V851SE. It is recommended to select 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for the Wi-Fi chip, the crystal uses the recommended specification or the specified model for the Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 2-15 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

The frequency stability mainly requires that the total load capacitance (C_L) is constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/(C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excepts the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance (C_{pkg} + C_{PCB}) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize the output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details about the resonator characteristics.

2.4 Interface Timings

2.4.1 SMHC Interface Timing

2.4.1.1 HS-SDR/HS-DDR Mode

NOTE

IO volatage is 1.8V or 3.3V.

Figure 2-4 SMHC HS-SDR Mode Output Timing Diagram

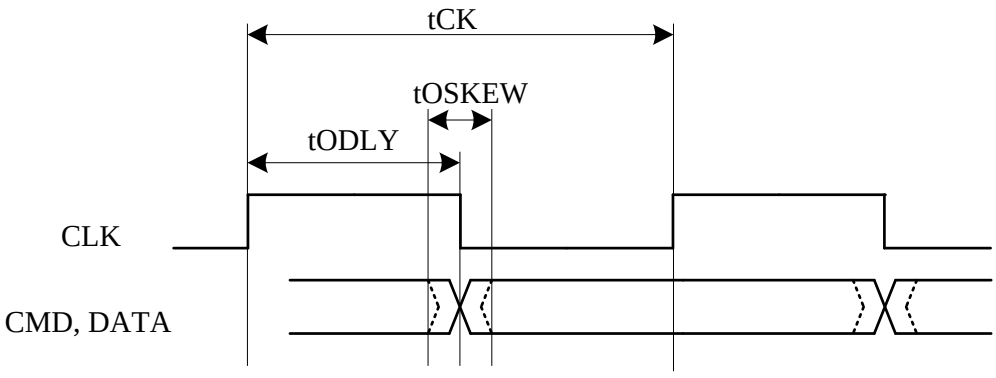


Figure 2-5 SMHC HS-DDR Mode Output Timing Diagram

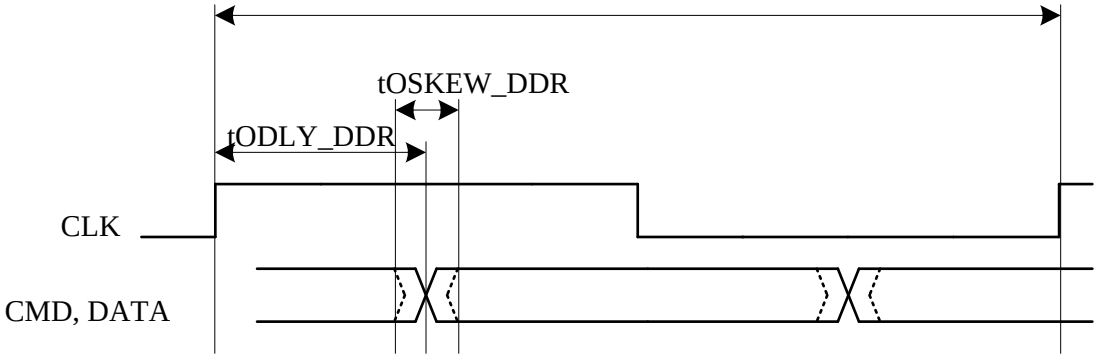


Table 2-16 SMHC HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-		ns	
NOTE Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz. The GPIO's driver strength level is 2 for test.						

Figure 2-6 SMHC HS-SDR Mode Input Timing Diagram

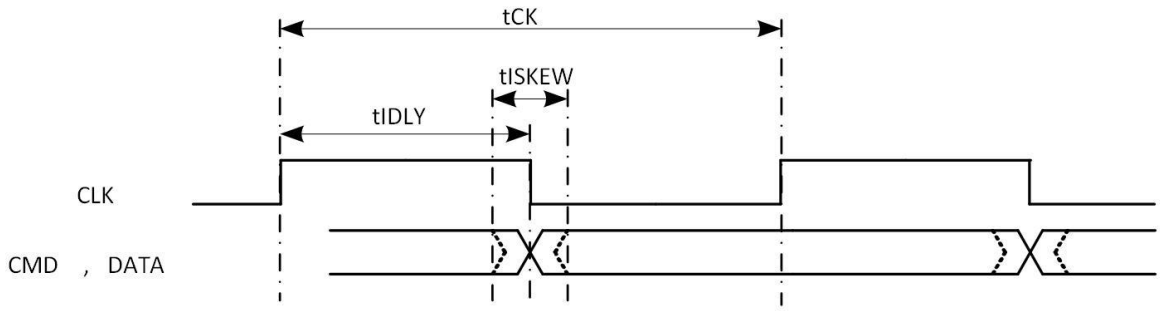


Figure 2-7 SMHC HS-DDR Mode Input Timing Diagram

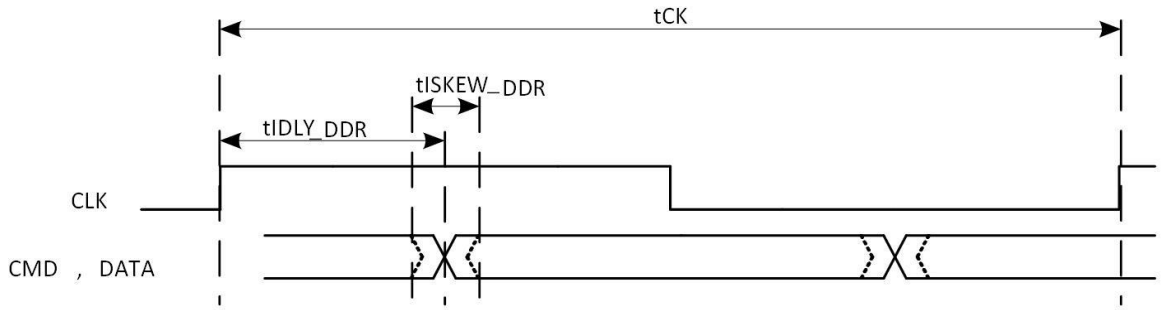


Table 2-17 SMHC HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-		ns	
Data input delay in DDR mode.It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-		ns	
Data input skew time in SDR mode	tISKEW	-	-		ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-		ns	
NOTE The GPIO's driver strength level is 2 for test.						

2.4.1.2 HS200 Mode

Figure 2-8 SMHC HS200 Mode Output Timing Diagram

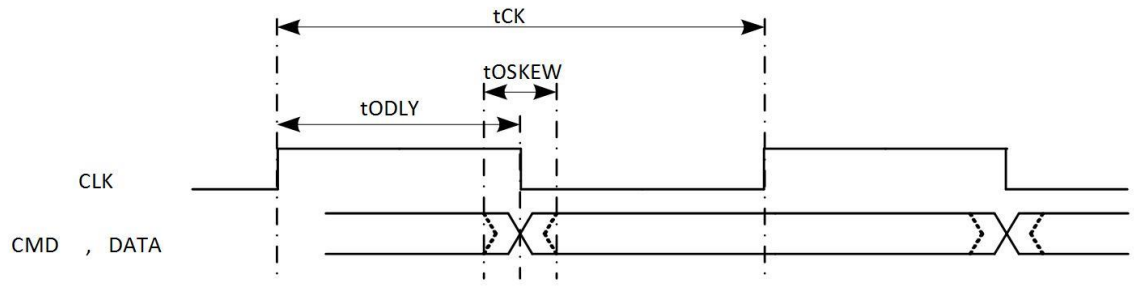


Table 2-18 SMHC HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-		ns	
NOTE Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. The GPIO's driver strength level is 3 for test.						

Figure 2-9 SMHC HS200 Mode Input Timing Diagram

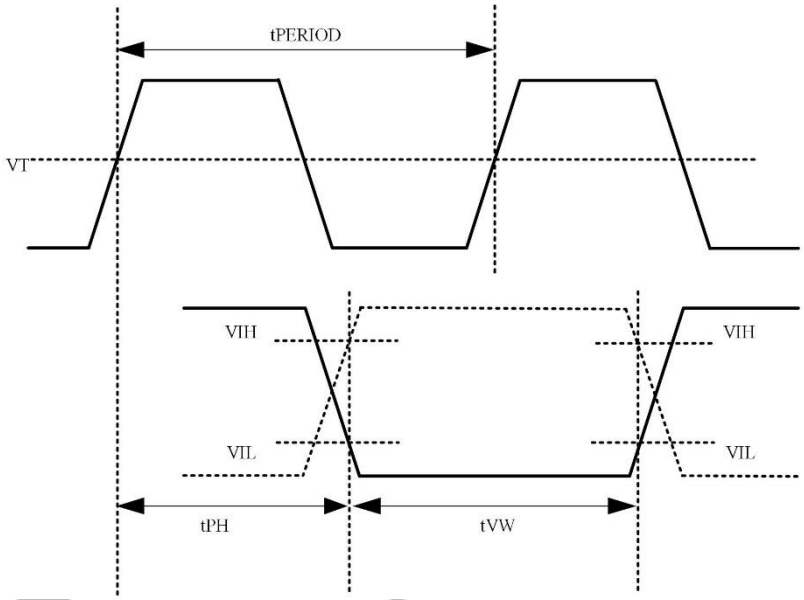


Table 2-19 SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
NOTE (1): Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2)**: The GPIO's driver strength level is 3 for test. **NOTE (3)**: Temperature variation: -20°C. **NOTE (4)**: Temperature variation: 90°C.						

2.4.1.3 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 2-10 SMHC HS400 Mode Data Output Timing Diagram

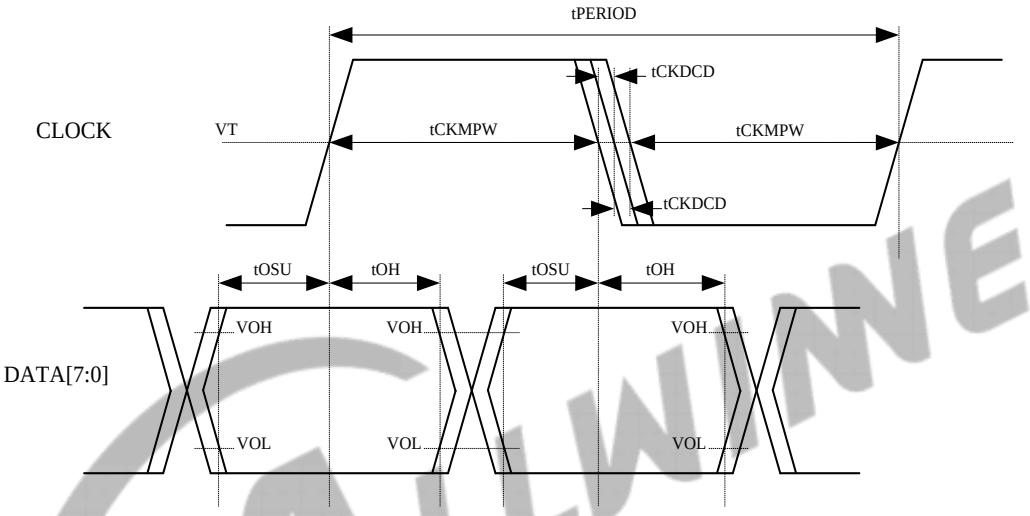


Table 2-20 SMHC HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
NOTE Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. The GPIO's driver strength level is 3 for test.						

Figure 2-11 SMHC HS400 Mode Data Input Timing Diagram

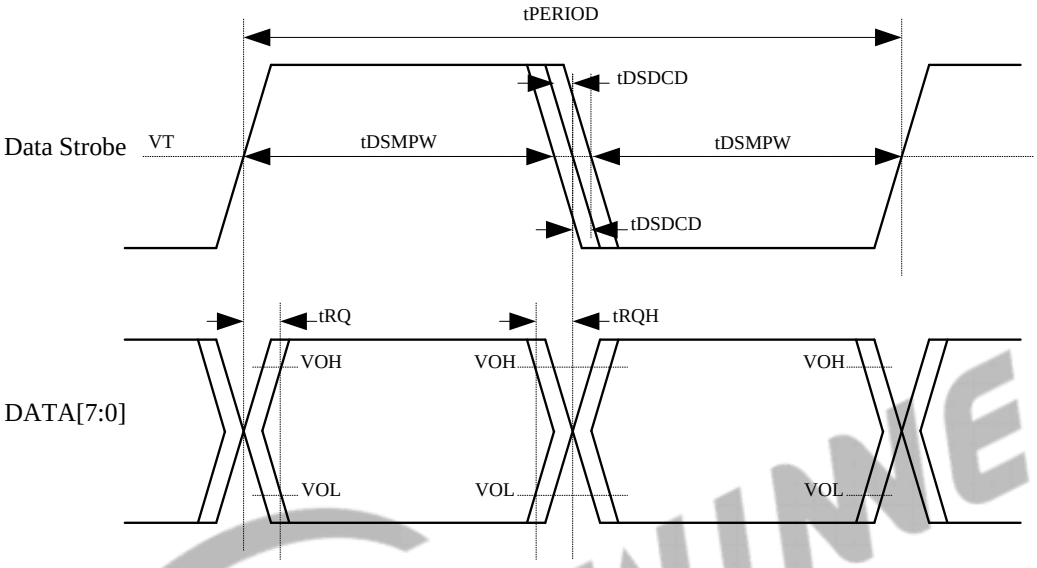


Table 2-21 SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
NOTE Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. The GPIO's driver strength level is 3 for test.						

2.4.2 LCD Interface Timing

Figure 2-12 HV_IF Interface Vertical Timing

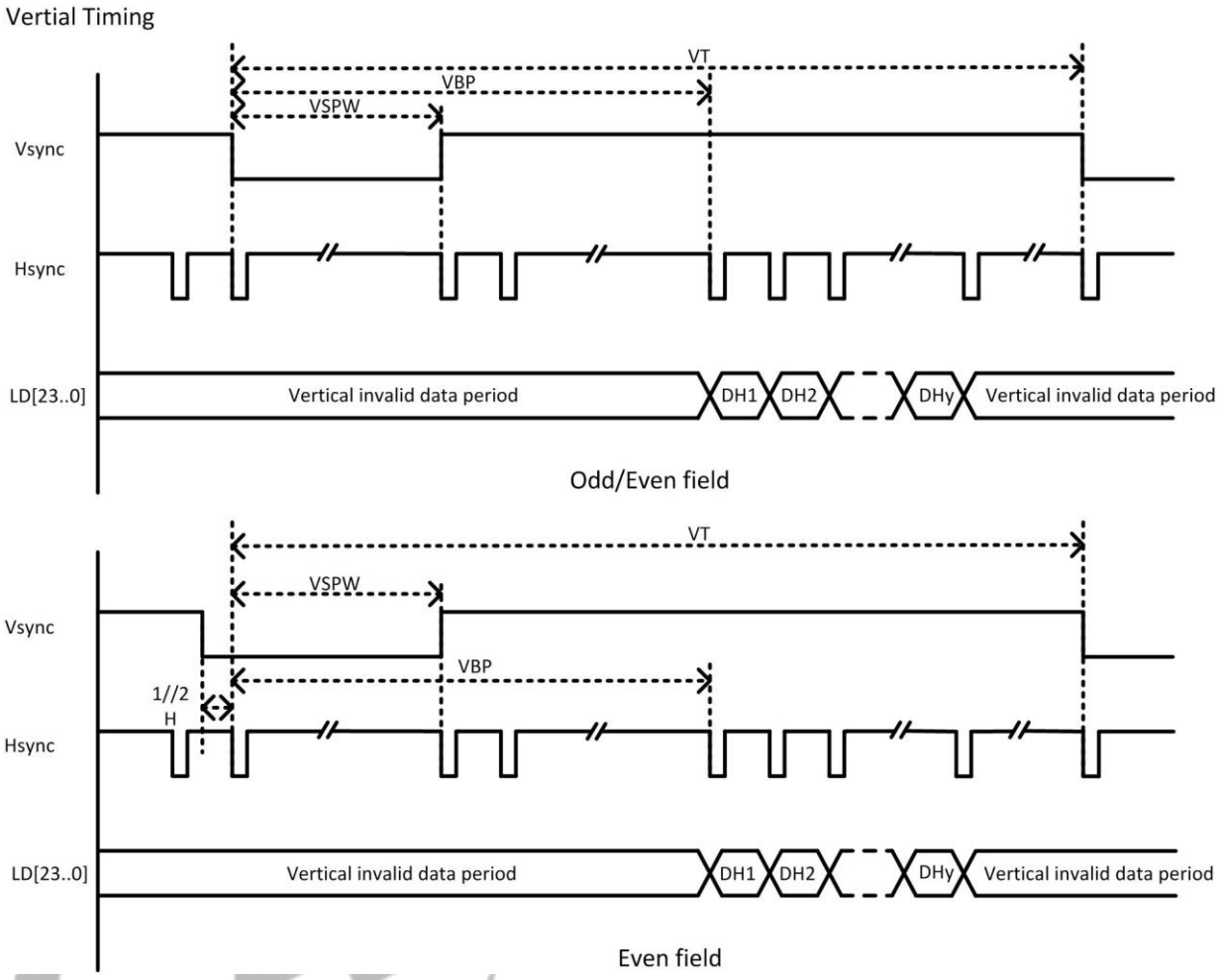


Figure 2-13 HV Interface Horizontal Timing

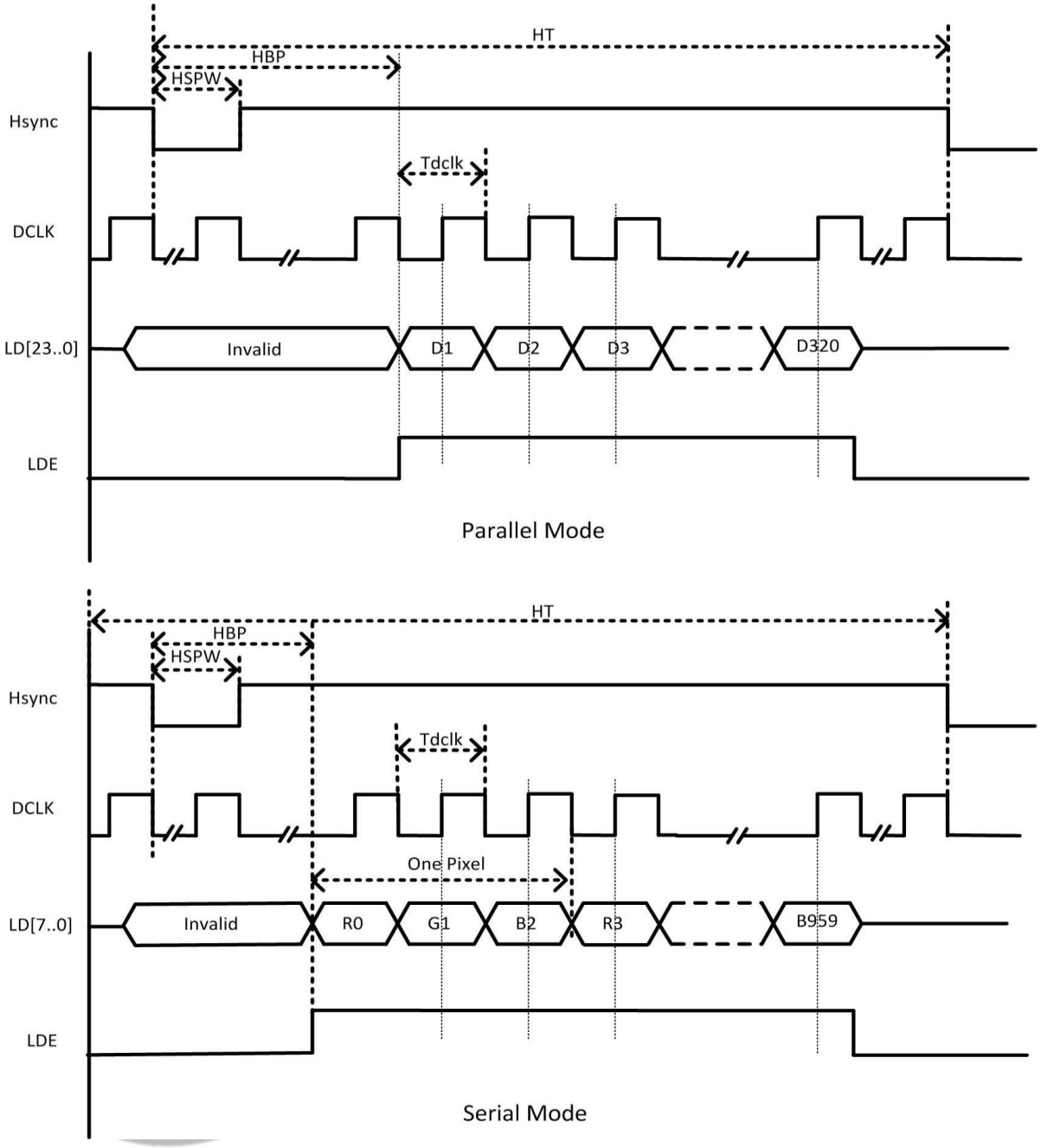


Table 2-22 HV Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
NOTE Vsync: Vertical sync, indicates one new frame Hsync: Horizontal sync, indicates one new scan line DCLK: Dot clock, pixel data are sync by this clock LDE: LCD data enable LD[23..0]: 24Bit RGB/YUV output for panel					

2.4.3 CSI Interface Timing

Figure 2-14 CSI Interface Timing

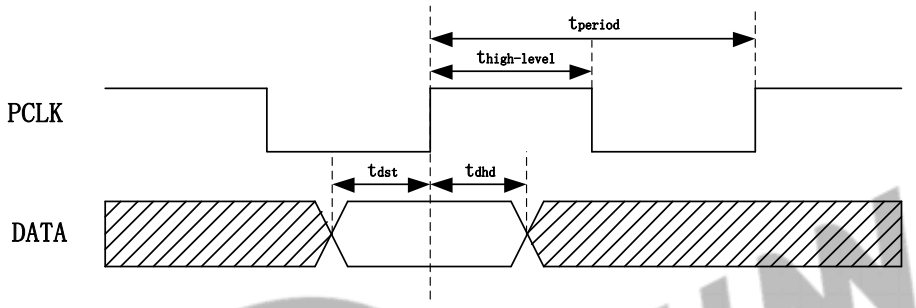


Table 2-23 CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.7	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	150	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

2.4.4 EMAC Interface Timing

Figure 2-15 RMII Transmit Timing

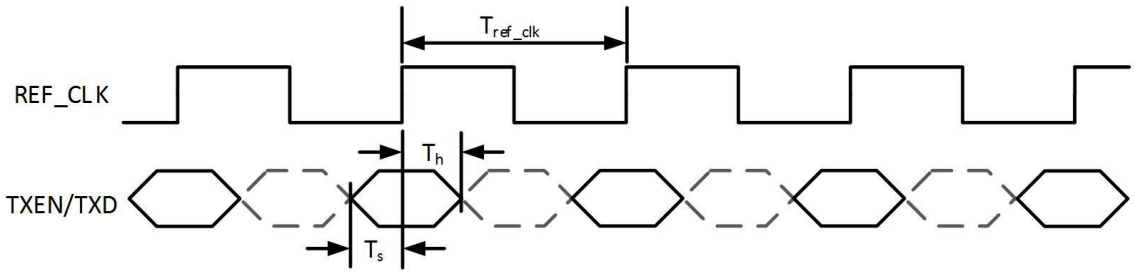


Table 2-24 RMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock Period	T_{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	T_s	4	-	T_h	TXD/TXEN to REF_CLK hold time

Figure 2-16 Receive Timing

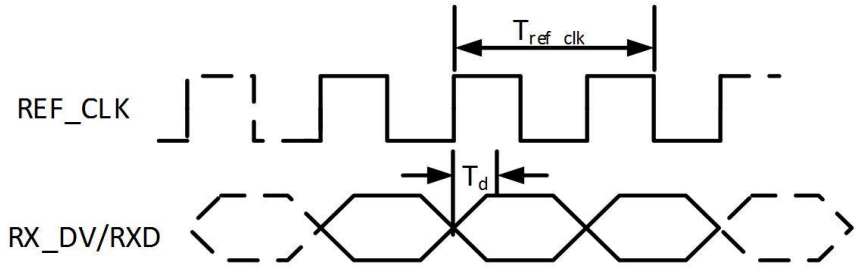


Table 2-25 RMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock Period	T_{ref_clk}	-	20	-	ns
REF_CLK rising edge to RX_DV/RXD	T_d	-	10	12	ns

2.4.5 I2S/PCM Interface Timing

Figure 2-17 I2S/PCM in Master Mode Timing

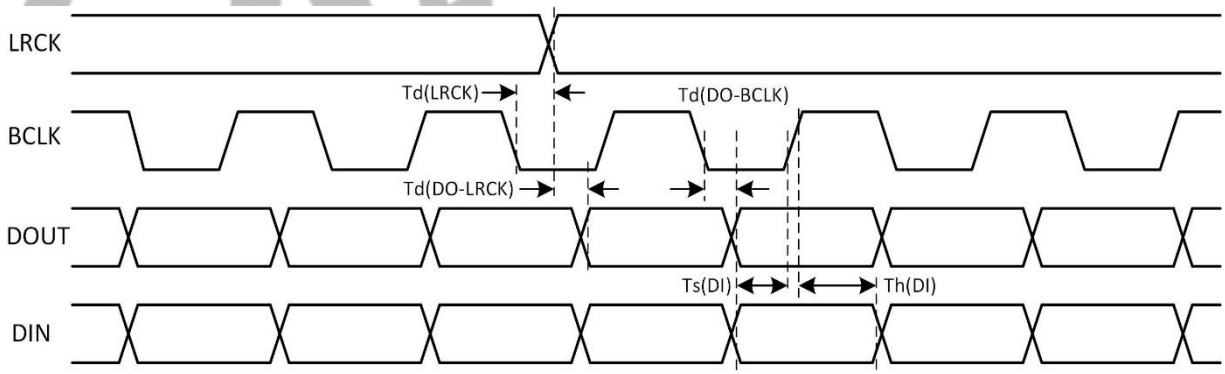


Table 2-26 I2S/PCM in Master Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)	-	-	10	ns
DIN Setup	T_s(DI)	4	-	-	ns
DIN Hold	T_h(DI)	4	-	-	ns
BCLK Rise Time	T_r	-	-	8	ns
BCLK Fall Time	T_f	-	-	8	ns

Figure 2-18 I2S/PCM in Slave Mode Timing

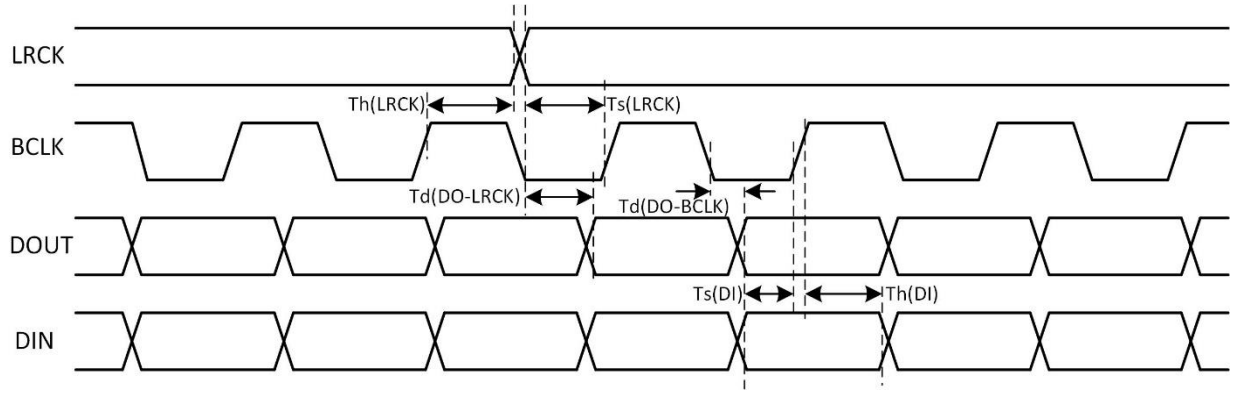


Table 2-27 I2S/PCM in Slave Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Setup	T_s(LRCK)	4	-	-	ns
LRCK Hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)	-	-	10	ns
DIN Setup	T_s(DI)	4	-	-	ns
DIN Hold	T_h(DI)	4	-	-	ns
BCLK Rise Time	T_r	-	-	4	ns
BCLK Fall Time	T_f	-	-	4	ns

2.4.6 DMIC Interface Timing

Figure 2-19 DMIC Timing

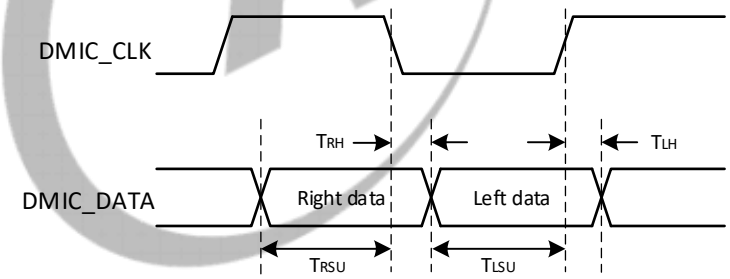


Table 2-28 DMIC Timing Constants

PARAMETER		MIN	MAX	UNITS
TRSU	DMIC_DATA(Right) setup time to falling DMIC_CLK edge	15		ns
TRH	DMIC_DATA(Right) hold time from falling DMIC_CLK edge	0		ns
TLSU	DMIC_DATA(Left) setup time to rising DMIC_CLK edge	15		ns
TLH	DMIC_DATA(Left) hold time from rising DMIC_CLK edge	0		ns

2.4.7 SPI Interface Timing

Figure 2-20 SPI MOSI Timing

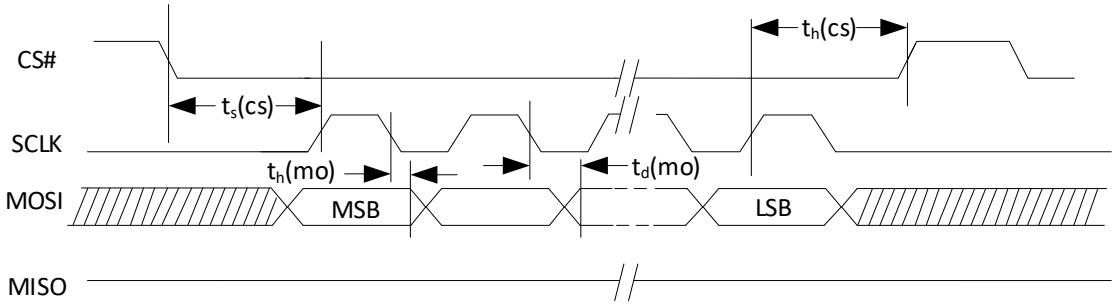


Figure 2-21 SPI MISO Timing

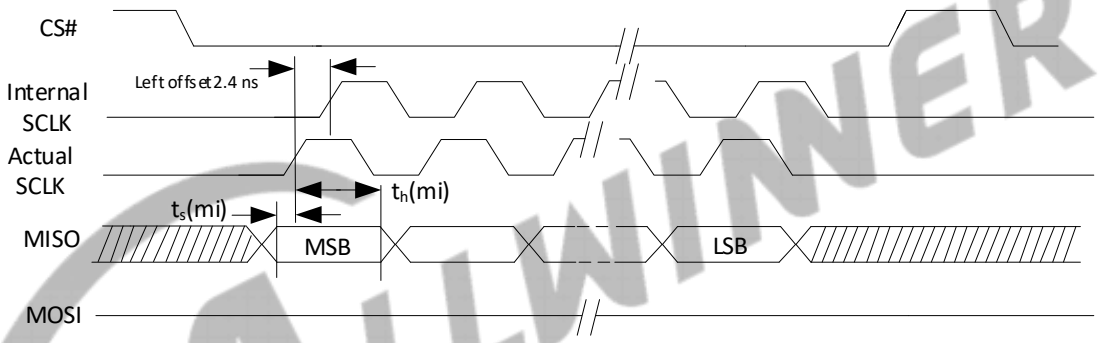


Table 2-29 SPI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CS# Active Setup Time	$t_s(cs)$	-	2T(1)	-	ns
CS# Active Hold Time	$t_h(cs)$	-	2T(1)	-	ns
Data output delay time	$t_d(mo)$	-	T(1)/2-3	-	ns
Data output hold time	$t_h(mo)$	-	T(1)/2-3	-	ns
Data In Setup Time	$t_s(mi)$	0.2	-	-	ns
Data In Hold Time	$t_h(mi)$	0.2	-	-	ns

NOTE

T is the cycle of clock.

2.4.8 UART Interface Timing

Figure 2-22 UART RX Timing

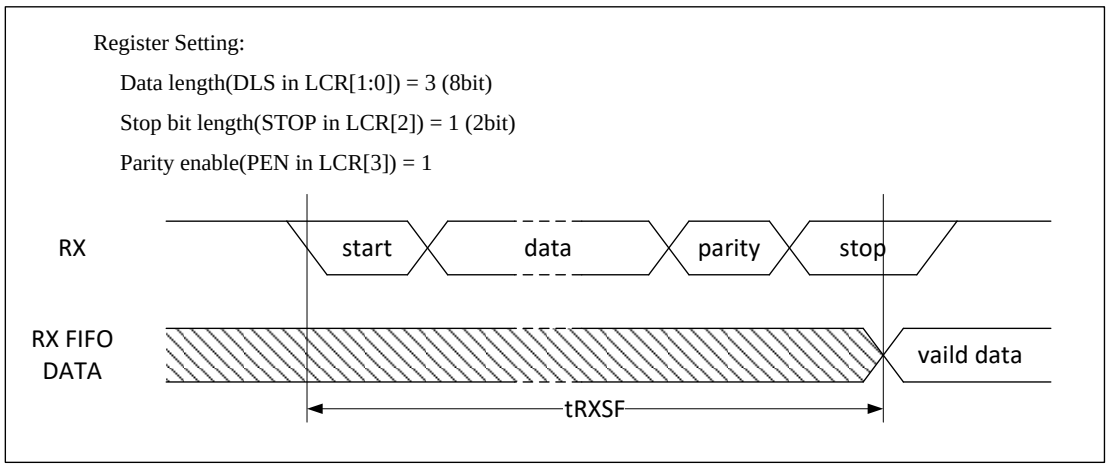


Figure 2-23 UART nCTS Timing

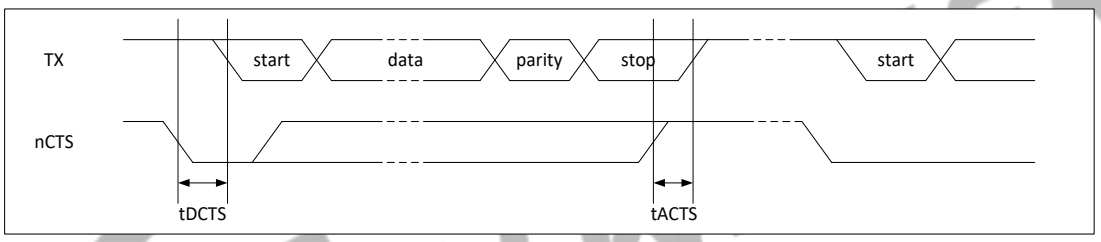


Figure 2-24 UART nRTS Timing

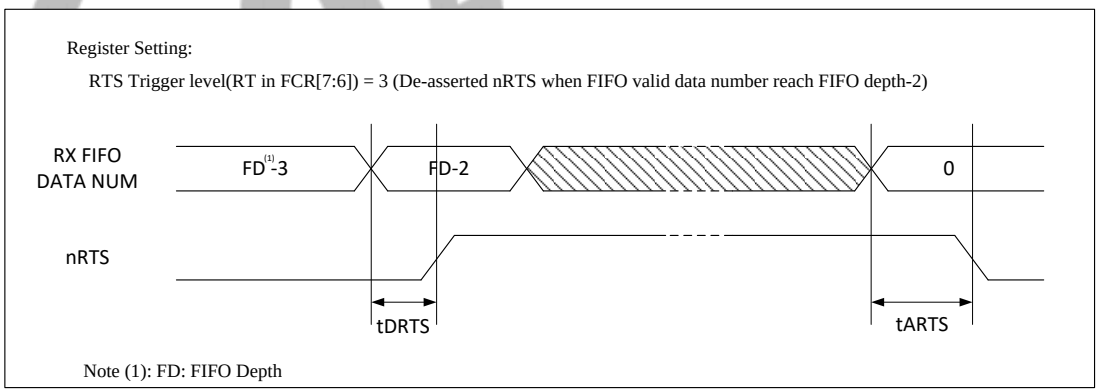


Table 2-30 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP	ns
Delay time of asserted nRTS	tARTS	-	-	BRP	ns

Parameter	Symbol	Min	Typ	Max	Unit
NOTE BRP: Baud-Rate Period.					

2.4.9 TWI Interface Timing

Figure 2-25 TWI Timing

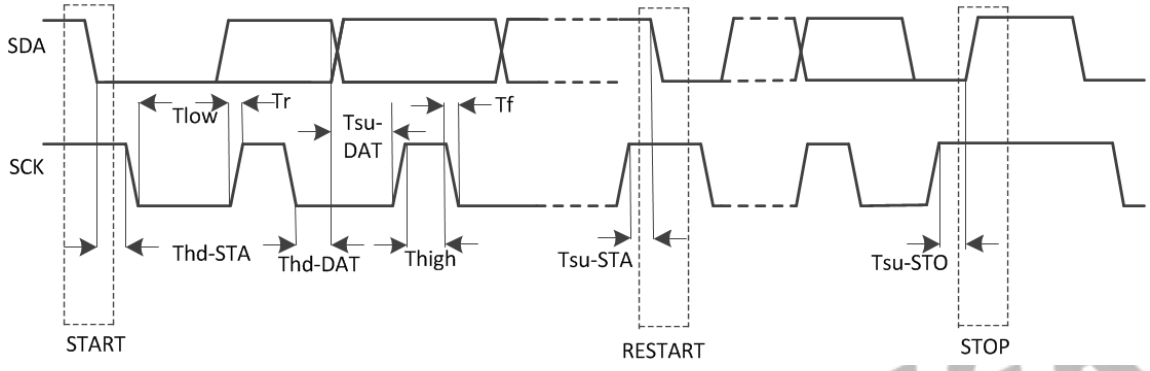


Table 2-31 TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in start	Tsu-STA	4.7	-	0.6	-	us
Hold time in start	Thd-STA	4.0	-	0.6	-	us
Setup time in data	Tsu-DAT	250	-	100	-	ns
Hold time in data	Thd-DAT	5.0	-	-	-	ns
Setup time in stop	Tsu-STO	4.0	-	0.6	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	us
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

2.4.10 MIPI DSI Interface Timing

Figure 2-26 MIPI DSI Timing Diagram

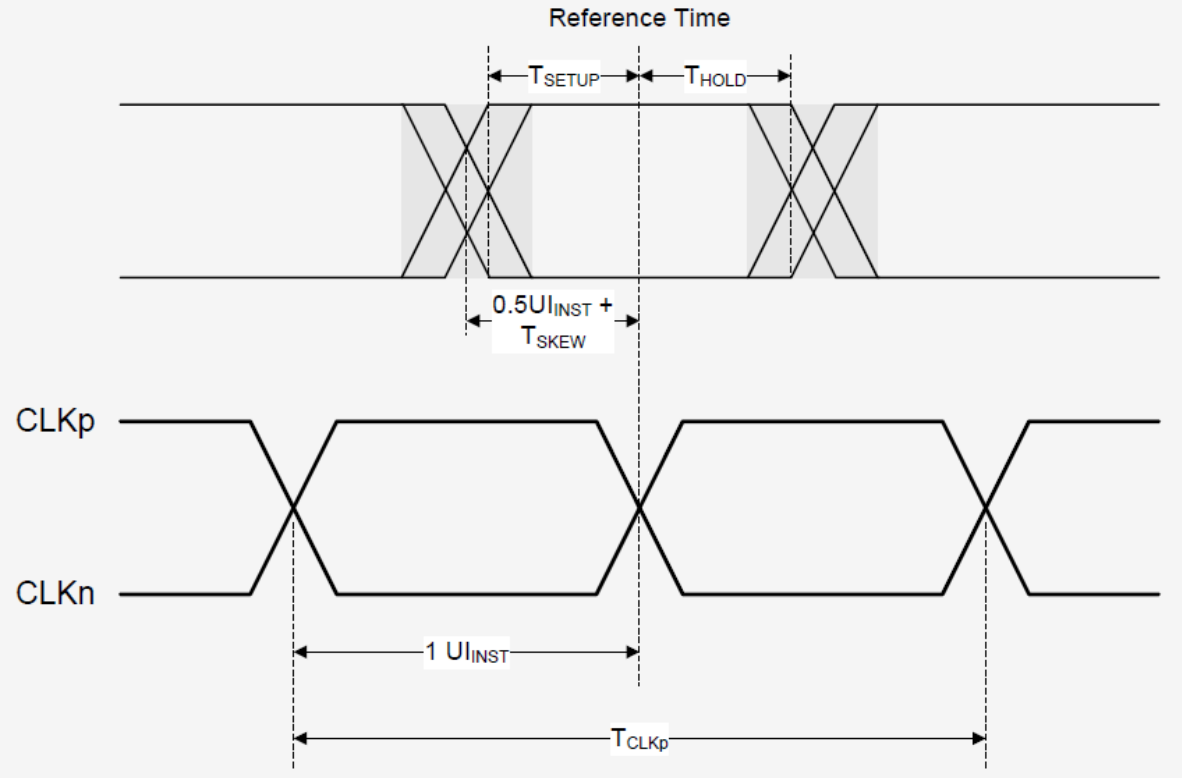


Table 2-32 MIPI DSI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Data to Clock Skew	T_{skew}	-0.15	-	0.15	UI_{INST}
Data to Clock Setup Time	T_{setup}	0.15	-	-	UI_{INST}
Clock to Data Hold Time	T_{hold}	0.15	-	-	UI_{INST}

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3 System

3.1 Memory mapping

Module	RISCV Address	Size (Bytes)
BROM & SRAM		
N-BROM	0x0000 0000—0x0000 DFFF	56KB
SRAM C	0x0002 0000---0x0004 0FFF	132K (Using ISP SRAM)
VE_SYS		
VE	0x01C0 E000---0x01C0 FFFF	8K
SP0		
GPIO	0x0200 0000---0x0200 07FF	2K
PWM	0x0200 0C00---0x0200 0FFF	1K
CCMU	0x0200 1000---0x0200 1FFF	4K
GPADC	0x0200 9000---0x0200 93FF	1K
THS	0x0200 9400---0x0200 97FF	1K
IOMMU	0x0201 0000---0x0201 FFFF	64K
WIREGAND	0x0202 0000---0x0202 03FF	1K
Audio_Codec	0x0203 0000---0x0203 0FFF	4K
DMIC	0x0203 1000---0x0203 13FF	1K
I2S1	0x0203 3000---0x0203 3FFF	4K
TIMER	0x0205 0000---0x0205 0FFF	4K
SP1		
UART0	0x0250 0000---0x0250 03FF	1K
UART1	0x0250 0400---0x0250 07FF	1K
UART2	0x0250 0800---0x0250 0BFF	1K
UART3	0x0250 0C00---0x0250 0FFF	1K
TWI0	0x0250 2000---0x0250 23FF	1K
TWI1	0x0250 2400---0x0250 27FF	1K
TWI2	0x0250 2800---0x0250 2BFF	1K
TWI3	0x0250 2C00---0x0250 2FFF	1K
TWI4	0x0250 3000---0x0250 33FF	1K
SH0		
SYSCTRL	0x0300 0000---0x0300 0FFF	4K
DMAC	0x0300 2000---0x0300 2FFF	4K
CPUX_MSGBOX	0x0300 3000---0x0300 3FFF	4K
SPINLOCK	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 6FFF	4K
HSTIMER	0x0300 8000---0x0300 8FFF	4K
DCU	0x0301 0000---0x0301 FFFF	64K (Only external AHB access)
CPU_GIC	0x0302 0000---0x0302 FFFF	64K
CE_NS	0x0304 0000---0x0304 07FF	2K

Module	RISCV Address	Size (Bytes)
NPU	0x0305 0000---0x0305 0FFF	4K
MSI+MEMC	0x0310 2000---0x0330 1FFF	2M
SH2		
SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
SPI0	0x0402 5000---0x0402 5FFF	4K
SPI1	0x0402 6000---0x0402 6FFF	4K
SPI2	0x0402 7000---0x0402 7FFF	4K
SPI3	0x0402 8000---0x0402 8FFF	4K
USB0	0x0410 0000---0x041F FFFF	1M
EMAC	0x0450 0000---0x0450 FFFF	64K
VIDEO_OUT_SYS		
DE	0x0500 0000---0x053F FFFF	4M
G2D	0x0541 0000---0x0544 FFFF	256K
DSI0	0x0545 0000---0x0545 1FFF	8K
DISPLAY_TOP	0x0546 0000---0x0546 0FFF	4K
TCON_LCD0	0x0546 1000---0x0546 1FFF	4K
VIDEO_IN_SYS		
CSI	0x0580 0000---0x058F FFFF	1M
ISP	0x0590 0000---0x05CF FFFF	4M
RISCV_SYS		
RISCV_CFG	0x0601 0000---0x0601 0FFF	4K
RISCV_WDG	0x0601 2000---0x0601 2FFF	4K
RISCV_TIMESTAMP	0x0601 4000---0x0601 4FFF	4K
RISCV_TIMER	0x0601 5000---0x0601 53FF	1K
RISCV_MSGBOX1	0x0602 0000---0x0602 0FFF	4K (only RISC CPU access)
APBS0		
R_CPUCFG	0x0700 0400---0x0700 0BFF	2K
R_PPU	0x0700 1000---0x0700 13FF	1K
R_SPC	0x0700 2000---0x0700 23FF	1K
R_PRCM	0x0701 0000---0x0701 FFFF	64K
R_TWD	0x0702 0800 – 0x0702 0BFF	1K
AHBS		
RTC	0x0709 0000---0x0709 03FF	1K
CPUX Related		
CPU_SYS_CFG	0x0810 0000---0x0810 03FF	1K
TIMESTAMP_STA	0x0811 0000---0x08011 0FFF	4K
TIMESTAMP_CTRL	0x0812 0000---0x0812 0FFF	4K
IDC	0x0813 0000---0x0813 0FFF	4K
C0_CPUX_CFG	0x0901 0000---0x0901 03FF	1K
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K

Module	RISCV Address	Size (Bytes)
RISC CPU Interrupts (Only RISC CPU access)		
RISCV_CLINT	0x3000 0000---0x3000 FFFF	
RISCV_CLIC	0x3080 0000---0x3080 4FFF	
RESERVE	0x3080 5000---0x3FFF FFFF	
DRAM Space		
DRAM SPACE	0x4000 0000---0xBFFF FFFF	2G

3.2 CPUX Configuration

3.2.1 Overview

The CPUX Configuration(CPUX_CFG) module is used to configure CLUSTER0 control, including power on, reset, cache, debug, and check the status of CPU. It will be used when you want to disable/enable the CPU, cluster switch, CPU status check, and debug, etc.

The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as GIC-400, JTAG.

The CPUX configuration includes the following features:

- CPU reset system: CORE reset, debug circuit reset and other reset function
- CPU related control: interface control, CP15 control, power on and power down control
- CPU status check: idle status, SMP status, interrupt status and so on
- CPU debug related register for control and status

3.2.2 CPUX Power Block Diagram

Figure 3-1 CPUX Power Domain Diagram

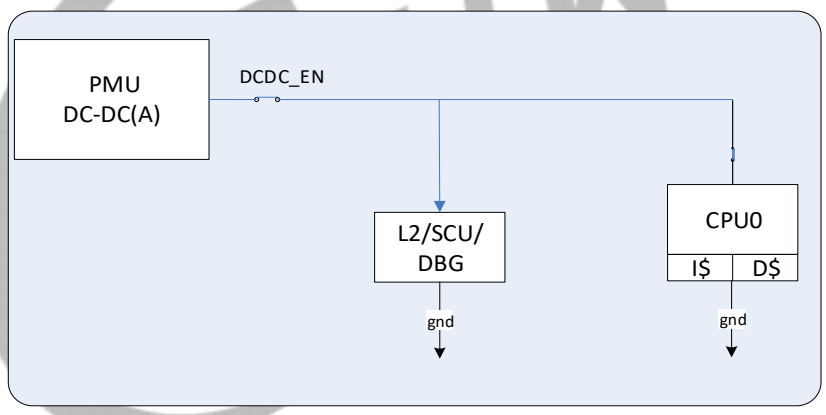


Figure 3-1 above lists the power domain of CLUSTER in default. All power switch of CPU core are default to power on.All CPU pwron_rst is de-asserted, core reset of CPU0 is de-asserted,core reset of CPU1 is asserted.

Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

CPU_SUBSYS_CTRL belongs to system power domain. The power domains of CPU related module are as follows.

Table 3-1 Power Attributes

Power Domain	Modules	Description
Cluster0	Cluster0/C0_CPUX_CFG/C0_MBIST	Cluster0 circuit, C0_CPUX_CFG module and CPU reset/power/mbist

Power Domain	Modules	Description
System	Timestamp/GIC/CPU_SUBSYS_CTRL/Clock	Provide system source of CPU sub-system

3.2.3 Operations and Functional Descriptions

3.2.3.1 Signal Description

For the detail of CPUX signal, please refer to ***ARM Cortex-A7 TRM***.

3.2.3.2 L2 Idle Mode

When the L2 of Cluster needs to enter WFI mode, firstly make sure the CPU0/1 of Cluster enter WFI mode, which can be checked through the bit[17:16] of **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing 1 to the bit0 of **Cluster Control Register1** , and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Remember to set the **ACINACTM** to low when exiting the L2 idle mode.

3.2.3.3 CPUX Reset System

The CPUX reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**. The description of all reset signal in CPUX Reset System is as follows.

Table 3-2 Reset Signal Description

Reset signal	Description
CORE_RST	This is the primary reset signal which resets the corresponding core logic that includes NEON and VFP, Debug, ETM, breakpoint and watchpoint logic. This maps to a warm reset that covers reset of the processor logic.
PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. This maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Reset all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/C0_CPUX_CFG.
CPU_SUBSYS_RST	Including C0_H_RST/GIC-400/CPU_SUBSYS_CTRL.

3.2.3.4 Operation Principle

The CPU-related operation needs proper configuration of CPUCFG related register, as well as related system control resource including BUS, clock , reset and power control.

3.2.4 Cluster Configuration Register List

Module Name	Base Address	Comments
C0_CPUX_CFG	0x09010000	Cluster0 CPUX configuration register

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1
C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
CACHE_CFG_REG	0x0024	Cache Configuration Register
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	L2 Status Register

3.2.5 Cluster Configuration Register Description

3.2.5.1 0x0000 Cluster 0 Reset Control Register (Default Value:0x13FF_0101)

Offset:0x0000			Register Name:C0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: Assert 1: De-Assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal for test 0: Assert 1: De-Assert
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: Assert 1: De-Assert

Offset:0x0000			Register Name:C0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0xF	ETM_RST Cluster ETM Reset Assert 0: Assert 1: De-Assert
19:16	R/W	0xF	DBG_RST Cluster Debug Reset Assert 0: Assert 1: De-Assert
15:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: Assert 1: De-Assert.
7:1	/	/	/
0	R/W	0x1	CORE_RESET Core Reset Cluster CPU0 Reset Assert 0: Assert 1: De-Assert

3.2.5.2 0x0010 Cluster 0 Control Register0 (Default Value:0x8000_0000)

Offset:0x0010			Register Name:C0_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus: 0: Barriers are broadcast onto system bus, this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus. This is compatible with an AXI3 interconnect.
30	R/W	0x0	BROADCAST_INNER Enable broadcasting of Inner Shareable transactions: 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.
29	R/W	0x0	BROADCAST_OUTER Enable broadcasting of outer shareable transactions: 0: Outer Shareable transactions are not broadcasted externally. 0: Outer Shareable transactions are broadcasted externally.

Offset:0x0010			Register Name:C0_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches: 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:24	/	/	/
23:12	/	/	/
11:8	R/W	0x0	CP15S_DISABLE Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset: 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3:1	/	/	/
0	R/W	0x0	L1_RST_DISABLE L1 Cache Reset Disable Disable automatic Cluster CPU0 L1 cache invalidate at reset: 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.2.5.3 0x0014 Cluster 0 Control Register1 (Default Value:0x0000_0000)

Offset:0x0014			Register Name:C0_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CRM_SEL_EN CRM Auto Select Slow Frequency En 0: Disable auto select 1 : Enable auto select
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepting requests. 0: Snoop interface is active 1: Snoop interface is inactive

3.2.5.4 0x0018 Cluster 0 Control Register2 (Default Value:0x0000_0010)

Offset:0x0018			Register Name:C0_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake up from WFE state This bit must remain HIGH for at least one clock cycle to be visible by the cores.
23:21	/	/	/
20	R/W	0x0	EXM_CLR Clear the status of interface EXM_CLR
19:0	R/W	0x10	Reserved

3.2.5.5 0x0024 Cache Configuration Register (Default Value:0x0018_001A)

Offset: 0x0024			Register Name: CACHE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:19	R/W	0x3	EMA_L2D L2 Cache SRAM EMA Control Port
18:17	R/W	0x0	EMAW_L2D L2 Cache SRAM EMAW Control Port
16	R/W	0x0	EMAS_L2D L2 Cache SRAM EMAS Control Port
15:12	/	/	/
11:8	R/W	0x0	DVS FARADAY SRAM Delay Signal
7	R/W	0x0	DVSE FARADAY SRAM Delay Enable Signal
6	R/W	0x0	STOV STOV
5:3	R/W	0x3	EMA Cache SRAM EMA Control Port
2:1	R/W	0x1	EMAW Cache SRAM EMAW Control Port
0	R/W	0x0	EMAS Cache SRAM EMAS Control Port

3.2.5.6 0x0080 Cluster 0 CPU Status Register (Default Value:0x000E_0000)

Offset:0x0080			Register Name:C0_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	SMP_AMP AMP Mode or SMP Mode CPU0 is in Symmetric Multiprocessing mode or Asymmetric Multiprocessing mode. 0: AMP mode 1: SMP mode
23:17	/	/	/
16	R	0xE	STANDBYWFI WFI Standby Mode Indicates if Cluster CPU0 is in WFI standby mode. 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:9	/	/	/
8	R	0x0	STANDBYWFE WFE Standby Mode Indicates if Cluster CPU0 is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2 L2 WFI Standby Mode Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

3.2.5.7 0x0084 L2 Status Register (Default Value:0x0000_0000)

Offset:0x0084			Register Name:L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R	0x0	EVENTO Event Output This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8:0	/	/	/

3.2.6 CPU Subsystem Control Register List

Module Name	Base Address	Comments
CPU_SUBSYS_CTRL	0x08100000	CPU subsystem control

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GIC_JTAG_RST_CTRL	0x000C	GIC and Jtag reset control Register
C0_INT_EN	0x0010	CLUSTER_0 Interrupt Enable Register
IRQ_FIQ_STATUS	0x0014	GIC IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2

3.2.7 CPU Subsystem Control Register Description

3.2.7.1 0x0000 General Control Register0 (Default Value:0x0000_0000)

Offset:0x0000			Register Name:GENER_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	C0_corepll_SEL Cluster 0 Corepll Select Register width state: 0: CCU clock; 1: DISP PLL clock.
1	R/W	0x0	IDC_CLK_EN IDC clock enable 0: Disable IDC clock; 1: Enable IDC clock.
0	R/W	0x0	GIC_CFGSDISABLE Disables write access to some secure GIC registers.

3.2.7.2 0x000C GIC and Jtag reset control Register (Default Value:0x0000_0F07)

Offset:0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EXM_CLR Clear the status of interface for debug EXM_CLR
15:12	/	/	/

Offset:0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W	0x1	CS_RST CoreSight Reset 0: Assert 1: De-assert.
10	R/W	0x1	DAP_RST DAP Reset 0: Assert 1: De-assert.
9	R/W	0x1	PORTRST JTAG PORTRST 0: assert 1: de-assert.
8	R/W	0x1	TRST JTAG TRST 0: Assert 1: De-assert.
7:3	/	/	/
2	R/W	0x1	Reserved
1	R/W	0x1	IDC_RST Interrupt Delay Controller Reset 0: Assert 1: de-assert.
0	R/W	0x1	GIC_RST GIC_RESET_CPU_REG 0: Assert 1: De-assert.

3.2.7.3 0x0010 CLUSTER_0 Interrupt Enable Register (Default Value:0x0000_FFFF)

Offset:0x0010			Register Name:C0_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	C0_GIC_EN Interrupt Enable Control Register Mask IRQ_OUT/FIRQ_OUT to system domain.

3.2.7.4 0x0014 GIC IRQ/FIQ Status Register (Default Value:0x0000_FFFF)

Offset:0x0014			Register Name: IRQ_FIQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0000	FIQ_OUT FIQ interrupt FIQ_OUT[15:0]
15:0	R/W	0xFFFF	IRQ_OUT IRQ interrupt IRQ_OUT[15:0]

3.2.7.5 0x0018 General Control Register2 (Default Value:0x0000_0000)

Offset:0x0018			Register Name:GENER_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CDBGRSTACK Debug Reset ACK.
15:2	/	/	/
0	R/W	0x0	C0_TSCLKCHANGE Cluster 0 Time Stamp change bit.

3.3 RISC System

3.3.1 Overview

The RISC system includes RISC IP core and related peripheral devices (RISC_CFG, RISC_TIMESTAMP, Watchdog, PSENSOR, BROM, and so on), which are interconnected by BUS Matrix.

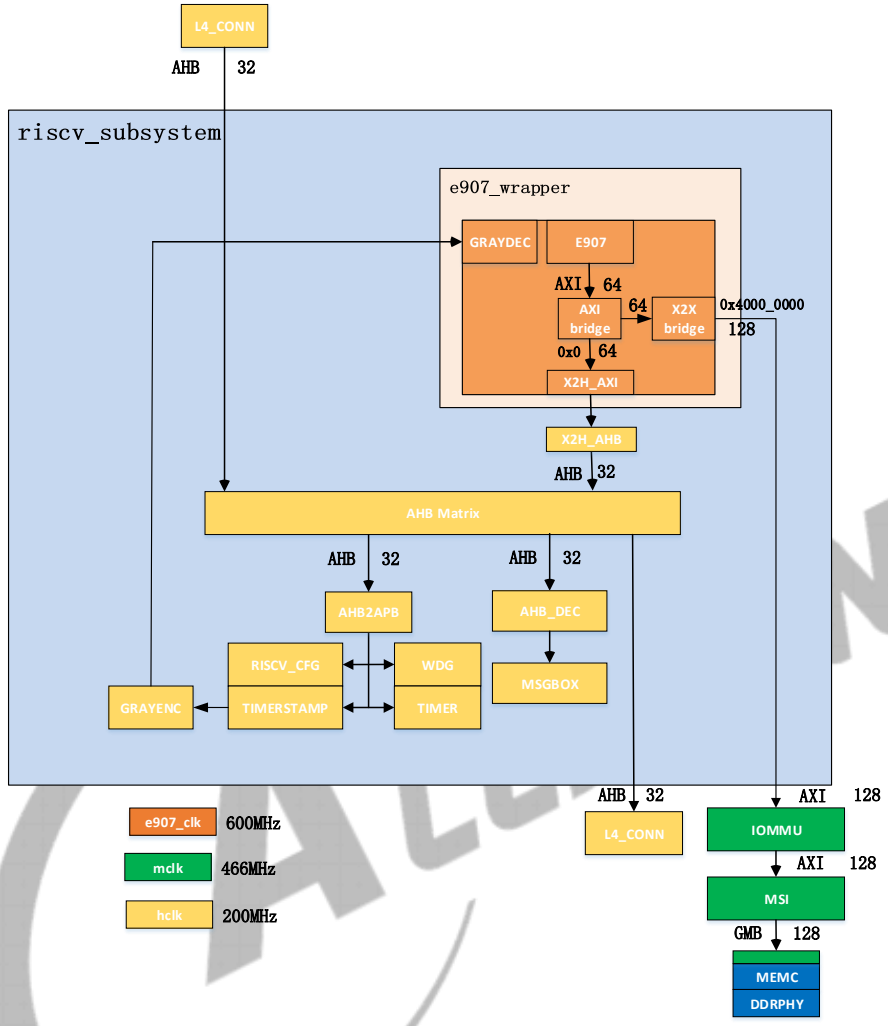
The RISC system has the following features:

- RISC 64GCV instruction architecture
- configurable base address via software
- combined with PPU module, supporting standby in low-power mode and wake-up through external interrupts
- separate timerstamp supports timing immediatly after reset is released
- separate watchdog supports preventing system from malfunctioning
- separate message box supports communicating with other modules
- supports separate PMU check module

3.3.2 Block Diagram

The following figure shows the block diagram of RISC system.

Figure 3-2 RISC System Block Diagram



3.3.3 Register List

Module Name	Base Address	Comments
RISCV_CFG	0x0601_0000	

Register Name	Offset	Description
RF1P_CFG_REG	0x0010	RF1P Configuration Register
TS_TMODE_SEL_REG	0x0040	Timestamp Test Mode Select Register
RISC_STA_ADD_REG	0x0204	RISC Start Address Register
RISC_WAKEUP_EN_REG	0x0220	RISC Wakeup Enable Register
RISC_WAKEUP_MASK0_REG	0x0224	RISC Wakeup Mask0 Register
RISC_WAKEUP_MASK1_REG	0x0228	RISC Wakeup Mask1 Register

Register Name	Offset	Description
RISC_WAKEUP_MASK2_REG	0x022C	RISC Wakeup Mask2 Register
RISC_WAKEUP_MASK3_REG	0x0230	RISC Wakeup Mask3 Register
RISC_WAKEUP_MASK4_REG	0x0234	RISC Wakeup Mask4 Register
RISC_WORK_MODE_REG	0x0248	RISC Work Mode Register
RISC_AXI_PMU_CTRL	0x0304	RISC AXI PMU Control Register
RISC_AXI_PMU_PRD	0x0308	RISC AXI PMU Period Register
RISC_AXI_PMU_LAT_RD	0x030C	RISC AXI PMU Read Latency Register
RISC_AXI_PMU_LAT_WR	0x0310	RISC AXI PMU Write Latency Register
RISC_AXI_PMU_REQ_RD	0x0314	RISC AXI PMU Read Request Register
RISC_AXI_PMU_REQ_WR	0x0318	RISC AXI PMU Write Request Register
RISC_AXI_PMU_BW_RD	0x031C	RISC AXI PMU Read Bandwidth Register
RISC_AXI_PMU_BW_WR	0x0320	RISC AXI PMU Write Bandwidth Register

3.3.4 Register Description

3.3.4.1 0x0010 RF1P Configuration Register (Default Value: 0x0000_0013)

Offset:0x0010			Register Name: RF1P_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x13	RF1P_CFG. RF1P Configuration.

3.3.4.2 0x0040 Timestamp Test Mode Select Register (Default Value: 0x0000_0000)

Offset:0x0040			Register Name: TS_TMODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	E907_TS_TEST_MODE_EN. E907 Timestamp Test Mode Enable. 0: Normal Mode 1:Test Mode
0	/	/	/

3.3.4.3 0x0204 E907 Start Address Register (Default Value: 0x0000_0000)

this register is the running PC address after RISC releases reset. Before releasing reset, this register should be configured. This register does not support dynamic configuration.

Offset:0x0204			Register Name: E907_STA_ADD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00000000	STA_ADD. Start Address. The bit0 is fixed as 0 and can not be written.

3.3.4.4 0x0220 E907 Wakeup Enable Register (Default Value: 0x0000_0000)

Offset:0x0220			Register Name: E907_WAKEUP_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WP_EN. Wakeup Enable.

3.3.4.5 0x0224 E907 Wakeup Mask0 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x0224			Register Name: E907_WAKEUP_MASK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00000000	WP_MASK0. Wakeup Mask0.

3.3.4.6 0x0228 E907 Wakeup Mask1 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x0228			Register Name: E907_WAKEUP_MASK1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK1. Wakeup Mask1.

3.3.4.7 0x022C E907 Wakeup Mask2 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x022C			Register Name: E907_WAKEUP_MASK2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK2. Wakeup Mask2.

3.3.4.8 0x00230 E907 Wakeup Mask3 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x00230			Register Name: E907_WAKEUP_MASK3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK3. Wakeup Mask3.

3.3.4.9 0x0234 E907 Wakeup Mask4 Register (Default Value: 0x0000_0000)

The 0x0224 to 0x0234 registers corresponds to the wakeup enable bits of 160 interrupts. These wakeup enable bits are disabled by default. When some interrupt needs to be waken-up, the corresponding bit needs to be set to 1.

Offset:0x0234			Register Name: E907_WAKEUP_MASK4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	WP_MASK4. Wakeup Mask4.

3.3.4.10 0x0248 E907 Work Mode Register (Default Value: 0x0000_000B)

Offset: 0x0248			Register Name: E907_WORK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset: 0x0248			Register Name: E907_WORK_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R	0x1	LOCKUP_STA. Lockup Status. 0: Not Lockup 1: Lockup Note: if CPU has a lockup, CPU will stop accessing data and fetching, and clear the pipeline. Reset processor unit and debug unit to unlock.
2	R	0x0	DM_STA. Debug Mode Status. 0: Normal Mode 1: Debug Mode
1:0	R	0x3	LP_STA. Low Power Status. 00: Low Power Mode 01: Reserved 10: Reserved 11: Normal Mode Reserved

3.3.4.11 0x0304 E907 AXI PMU Control Register (Default Value: 0x0000_0000)

Offset:0x0304			Register Name: E907_AXI_PMU_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	WC	0x0	PMU_CLR. PMU Clear. 0 No operation. 1 PMU cleared.
0	R/W	0x0	PMU_EN. PMU Enable. 0 PMU disabled. 1 PMU Enabled.

3.3.4.12 0x0308 E907 AXI PMU Period Register (Default Value: 0x0000_0000)

Offset:0x0308			Register Name: E907_AXI_PMU_PRD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PRD. Period. Suggest that the field is in units of 1 us (1 ms).

3.3.4.13 0x030C E907 AXI PMU Read Latency Register (Default Value: 0x0000_0000)

Offset:0x030C			Register Name: E907_AXI_PMU_LAT_RD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD_LAT. Read Latency. Monitor the total latency of read-channel durning period

3.3.4.14 0x0310 E907 AXI PMU Write Latency Register (Default Value: 0x0000_0000)

Offset:0x0310			Register Name: E907_AXI_PMU_LAT_WR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	WR_LAT. Write Latency. Monitor the total latency of read-channel durning period

3.3.4.15 0x0314 E907 AXI PMU Read Request Register (Default Value: 0x0000_0000)

Offset:0x0314			Register Name: E907_AXI_PMU_REQ_RD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD_REQ. Read Request. Monitor the total command numbers of read-channel durning period

3.3.4.16 0x0318 E907 AXI PMU Write Request Register (Default Value: 0x0000_0000)

Offset:0x0318			Register Name: E907_AXI_PMU_REQ_WR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	WR_REQ. Write Request. Monitor the total latency of write-channel durning period

3.3.4.17 0x031C E907 AXI PMU Read Bandwidth Register (Default Value: 0x0000_0000)

Offset:0x031C			Register Name: E907_AXI_PMU_BW_RD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD_BW. Read Bandwidth. Monitor the total data (KB) of read-channel durning period

3.3.4.18 0x0320 E907 AXI PMU Write Bandwidth Register (Default Value: 0x0000_0000)

Offset:0x0320			Register Name: E907_AXI_PMU_BW_WR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	WR_BW. Write Bandwidth. Monitor the total data (KB) of write-channel durning period

3.4 Clock Controller Unit (CCU)

3.4.1 Overview

The clock controller unit (CCU) controls the PLL configurations and most of the clock generation, division, distribution, synchronization, and gating. The input signals of the CCU include the external clock for the reference frequency (24 MHz). The outputs from the CCU are mostly clocks to other blocks in the system.

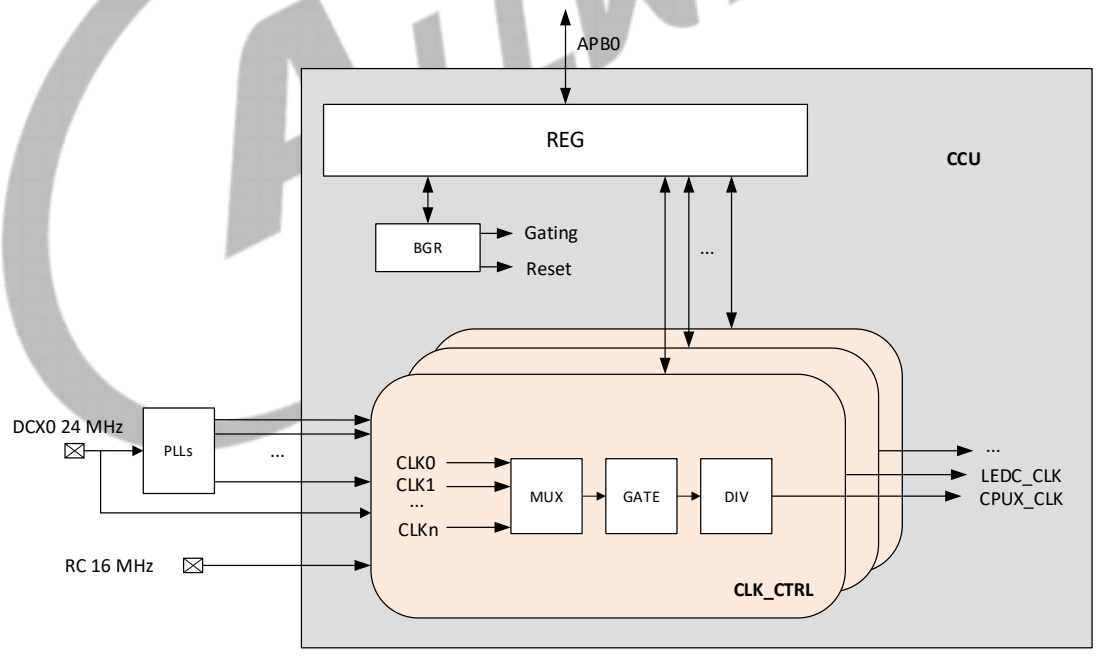
The CCU includes the following features:

- Bus Source and Divisions
- Clock Output Control
- Configuring Modules Clock
- Bus Clock Gating
- Bus Software Reset

3.4.2 Block Diagram

The following figure shows the functional block diagram of the CCU.

Figure 3-3 CCU Block Diagram



3.4.3 Functional Description

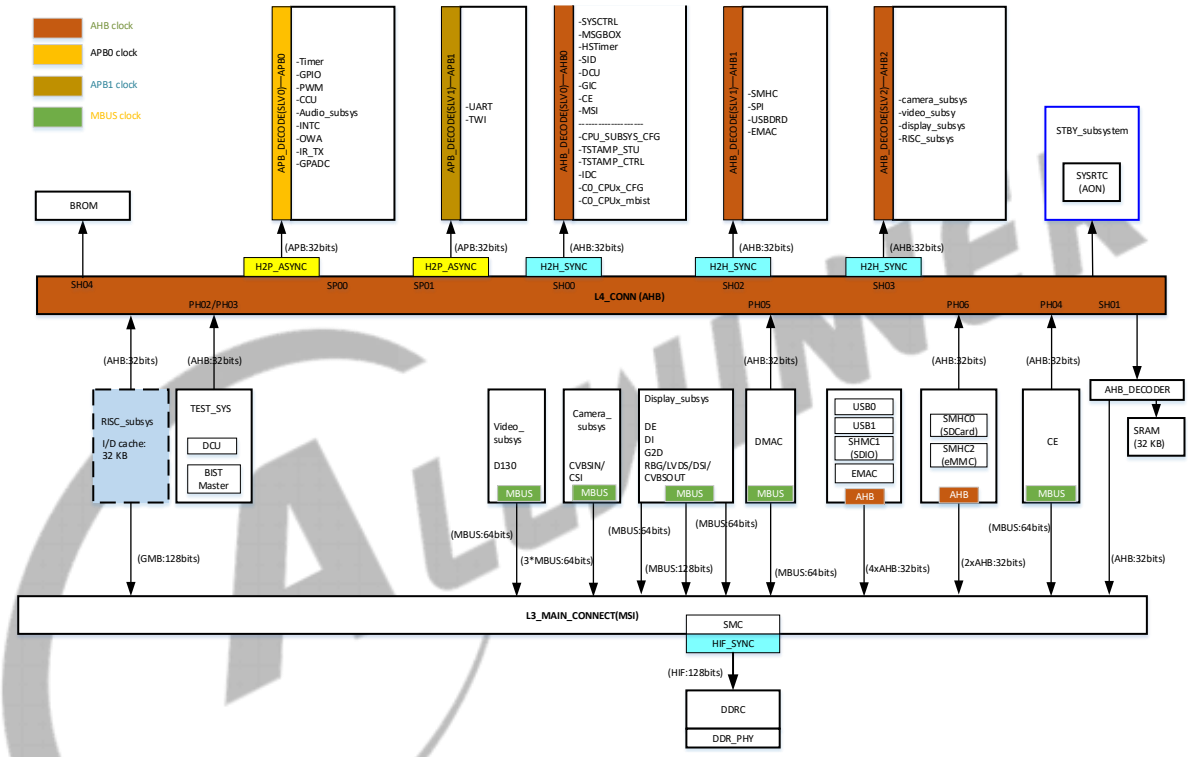
3.4.3.1 System Bus Tree

The system buses include advanced high-performance buses (AHBs), advanced peripheral buses (APBs), and MBUS.

All devices mounted at the bus should use the related bus clocks, and the gating signals for the bus are from the CCU module.

The following figure shows the diagram of the System Bus Tree.

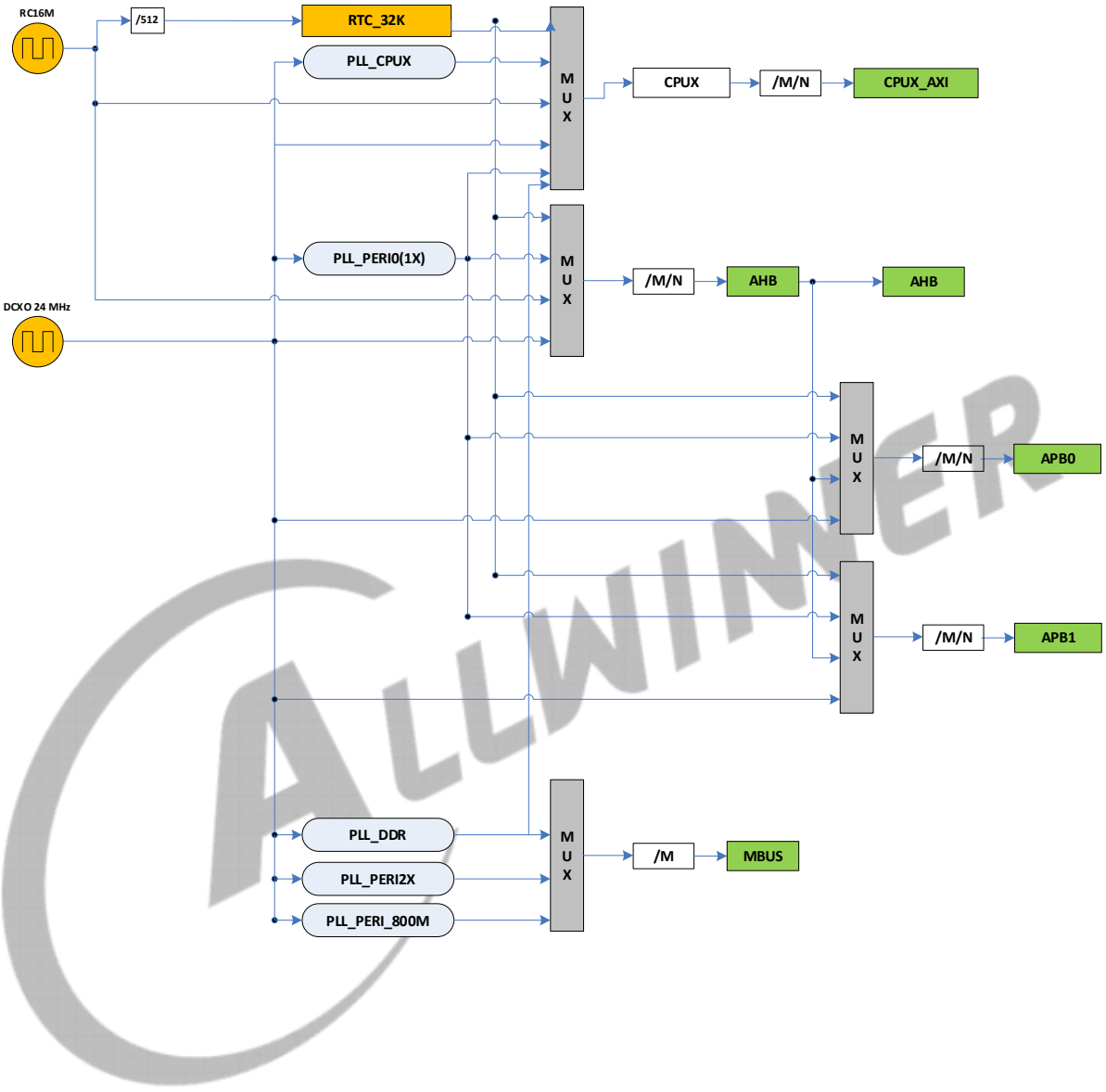
Figure 3-4 System Bus Tree



3.4.3.2 Bus Clock Generation

The following figure describes module clock generation.

Figure 3-5 Bus Clock Generation



3.4.3.3 PLL Distribution

The following figure shows the block diagram of the PLL distribution.

Figure 3-6 PLL Distribution

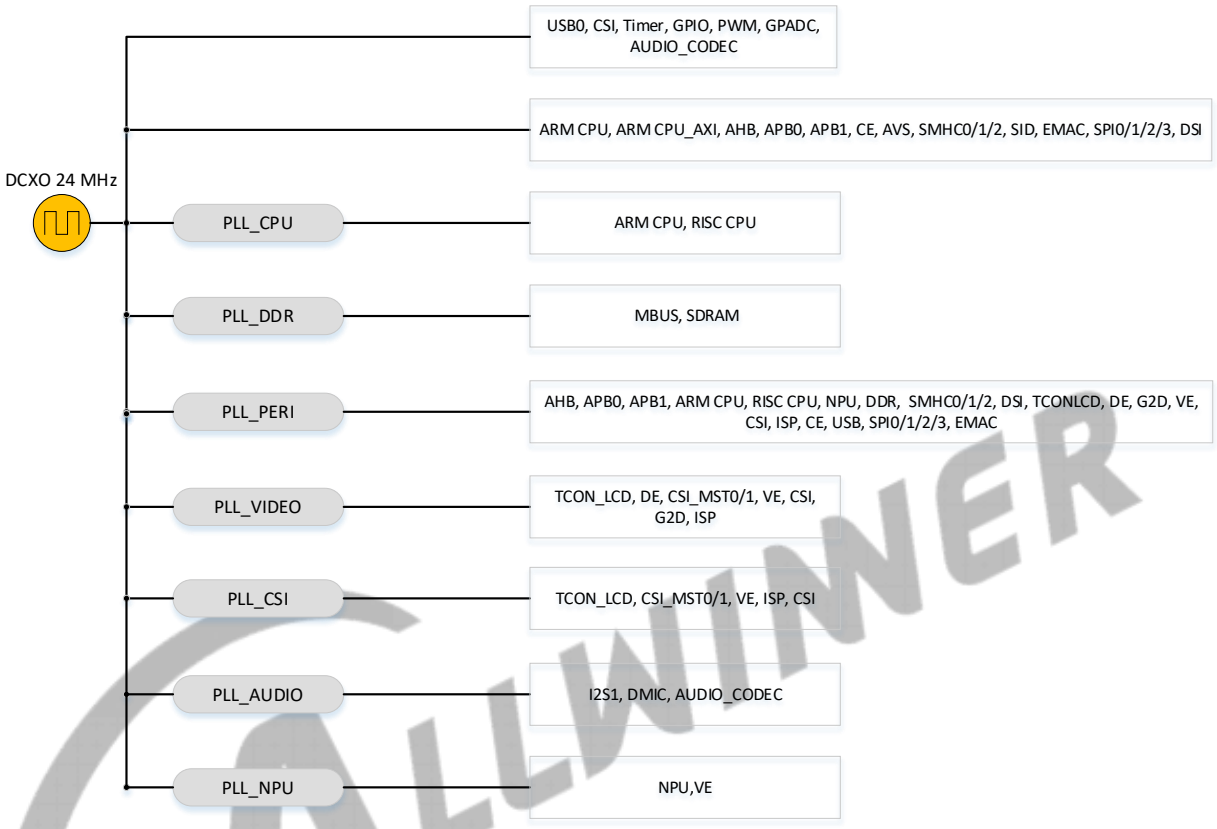


Table 3-3 PLL Typical Application

PLL Type	Application Module	Notes
PLL_CPU	ARM CPU, RISC CPU	Support DVFS
PLL_DDR	MBUS, SDRAM	Support spread spectrum No support linear FM
PLL_PERI	AHB, APB0, APB1, ARM CPU, RISC CPU, NPU, DDR, SMHC0/1/2, DSI, TCONLCD, DE, G2D, VE,CSI, ISP, CE, USB, SPI0/1/2/3, EMAC	No support dynamic FM
PLL_VIDEO	TCONLCD, DE, CSI_MST0/1, VE, CSI, G2D, ISP	No support DVFS
PLL_CSI	TCON_LCD, CSI_MST0/1, VE, ISP, CSI	No support DVFS
PLL_AUDIO	I2S1, DMIC, AUDIO_CODEC	No support DVFS
PLL_NPU	NPU, VE	No support DVFS

3.4.3.4 PLL Features

The following table shows the PLL features.

Table 3-4 PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Default Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Lock Time
PLL_CPU	288 MHz to 3.0 GHz (24*N)	288 MHz to 1.8 GHz	408 MHz	No	Yes	No	< 200 ps	1.5 ms
PLL_AUDIO	80 MHz to 3.0 GHz (24MHz*N.x/M1/M0/P)	24.576 MHz 22.5792 MHz 24.576*4 MHz 22.5792*4 MHz	24.576 MHz	Yes	No	No	< 200 ps	500 us
PLL_PERI	180 MHz to 3.2 GHz (24*N/M1/M0)	Fvco/Div (Div:1–8)	1/2x: 1.2 GHz 1/3x: 800 MHz 1/5x: 480MHz	Yes	No	No	< 200 ps	500 us
PLL_Video(4X)	252 MHz to 3.0 GHz (24*N/M)	192 MHz to 2400 MHz	1x: 297 MHz 2x:594 MHz 4x:1188 MHz	Yes	No	No	< 200 ps	500 us
PLL_CSI (4X)	252 MHz to 3.0 GHz (24*N/M)	192 MHz to 2400 MHz	1x: 297 MHz 2x:594 MHz 4x:1188 MHz	Yes	No	No	< 200 ps	500 us
PLL_DDR	180 MHz to 3.0 GHz (24*N/M1/M0)	192 MHz to 2.0 GHz	432 MHz	Yes	No	No	200 MHz to 800 MHz (< 200 ps) 800 MHz to 1.3 GHz (< 140 ps) 1.3 GHz to 2.0 GHz (< 100 ps)	500us
PLL_NPU	180 MHz to 3.0 GHz (24*N/M1/M0)	500 MHz to 2.1 GHz	504MHz	Yes	No	No	< 200 ps	500 us

3.4.4 Programming Guidelines

3.4.4.1 Configuring the Frequency of PLL_CPU

The frequency configuration formula of PLL_CPU is shown below:

PLL_C0_CPU= 24MHz*N/P

The parameter N is the frequency-doubling factor of PLL. The next parameter can only be configured after the PLL relocks.

The parameter P is a digital post-frequency-division factor. It can be dynamically switched in real-time, without affecting the normal work of PLL.

NOTE

PLL_CPU supports the dynamic adjustment (modifying the value of N). However, for the system stability, if you need to configure the frequency of the PLL_CPU from a higher value to a lower one, switch the CPU frequency to a medium one first, and then configure PLL_CPU to the target low frequency.

Follow the steps below to adjust the frequency of PLL_CPU:

1. Before you configure PLL_CPU, switch the clock source of CPU to PLL_PERI(1X).
2. Modify the parameters N and P of PLL_CPU.
3. Write the PLL Lock Enable bit (bit[29]) of PLL_CPU_CTRL_REG (Offset: 0x0000) to 0 and then to 1.
4. Wait until the Lock bit (bit[28]) of PLL_CPU_CTRL_REG (Offset: 0x0000) changes to 1.
5. Switch the clock source of the CPU to PLL_CPU.

3.4.4.2 Configuring the Frequency of PLL_AUDIO

The frequency configuration formula of PLL_AUDIO is shown below:

PLL_AUDIO = 24MHz*N/M0/M1/P

Changing any parameter of N, M0, M1, and P will make PLL be relocked, so PLL_AUDIO does not support the dynamic adjustment.

Generally, the frequency of PLL_AUDIO is either 24.576*4 MHz or 22.5792*4 MHz, and the two frequency points have the recommended configuration values. To implement the desired frequency point of PLL_AUDIO, follow the steps below:

1. Configure the N, M1, M0, and P factors.
2. Configure PLL_SDM_EN (bit[24])of PLL_AUDIO_CTRL_REG (Offset: 0x0078) to 1.
3. Configure PLL_AUDIO_PAT0_CTRL_REG (Offset: 0x0178) to enable the digital spread spectrum
4. Write the PLL_LOCK_ENABLE bit (bit[29]) of PLL_AUDIO_CTRL_REG (Offset: 0x0078) to 0 and then to 1.
5. Wait until the LOCK bit (bit28) of PLL_AUDIO_CTRL_REG (Offset: 0x0078) changes to 1.

NOTE

When the P factor of PLL_AUDIO is an odd number, the clock output is an unequal-duty-cycle signal.

The recommended values for configuration factors of PLL_AUDIO are as follows.

Table 3-5 Recommended Values for Configuration Factors of PLL_AUDIO

Mode	Clock Source (MHz)	Frequency-doubling N	VCO (MHz)	Post Frequency-Division	PLL Output (MHz)	Divisor	Actual Operating Frequency (MHz)	Description
Integer divider	24	128	3072	2	1536	4	384	Provide clock source for peripherals
						8	192	
						16	96	
						……		
				5	614.4	25	24.576	For audio-related modules
Decimal divider	24	98.304	2359.296	2	1179.648	2	589.824	Provides clock source for peripheral devices
						3	393.216	
						6	196.608	
						12	98.304	
						48	24.576	For audio-related modules
				5	471.8592			

3.4.4.3 Configuring the Frequency of General PLLs

1. Make sure the PLL is enabled. If not, refer to section 3.4.4.4 Enabling the PLL to enable the PLL.
2. Configure the PLL_OUTPUT_GATE bit (bit[27]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) as 0 to disable the output gate of the PLL, because general PLLs are unavailable in the process of the frequency modulation.
3. Configure the N and M factors. (It is not suggested to configure the M1 factor)
4. Write the LOCK_ENABLE bit (bit[29]) of the PLL_CPU_CTRL_REG (Offset: 0x000) to 0 and then to 1.
5. Wait until the LOCK bit (bit[28]) of the PLL_CPU_CTRL_REG (Offset: 0x000) changes to 1.
6. Configure PLL_OUTPUT_GATE bit (bit[27]) of the PLL_CPU_CTRL_REG (Offset: 0x000) to 1.

3.4.4.4 Enabling the PLL

Follow the steps below to enable the PLL:

1. Configure the N, M, and P factors of the PLL control register.
2. Write the PLL_OUTPUT_GATE bit (bit[27]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) to 0.
3. Write the PLL_ENABLE bit (bit[31]) and the LDO_EN bit (bit[30]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) to 1.
4. Write the LOCK_ENABLE bit (bit[29]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) to 1.
5. Wait for the status of the Lock to change to 1.
6. Delay 20 us.
7. Write the PLL_OUTPUT_GATE bit (bit[27]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) to 1 and then the PLL will be available.

3.4.4.5 Disabling the PLL

Follow the steps below to disable the PLL:

1. Write the PLL_ENABLE bit (bit[31]) and the LDO_EN bit (bit[30]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) to 0.
2. Write the LOCK_ENABLE bit (bit[29]) of the PLL_CPU_CTRL_REG (Offset: 0x0000) to 0.

CAUTION

In the normal use of PLLs, it is unsuggested to enable and disable the PLLs frequently. Turning on and off the PLLs will cause mutual interference between PLLs, which will affect the stability of the system. When the clock is unnecessary, you can write 0 to the PLL_OUTPUT_GATE bit of the PLL control register to disable the output gate of the PLL, instead of writing 0 to the Enable bit to disable the PLL.

3.4.4.6 Configuring Bus Clock

The bus clock supports the dynamic switching, but remember to follow the two rules below during the switching process.

- From a higher frequency to a lower one: switch the clock source first, and then set the frequency division factor;
- From a lower frequency to a higher one: configure the frequency division factor first, and then switch the clock source.

3.4.4.7 Configuring Module Clocks

For the Bus Gating Reset register of a module, the reset bit is de-asserted first, and then the clock gating bit is enabled to avoid the potential problems caused by the asynchronous release of the reset signal.

For all module clocks except the DDR clock, configure the clock source and frequency division factor first, and then release the clock gating (sets it to 1). For the configuration order of the clock source and the frequency division factor, follow the rules below:

- With the increasing of the clock source frequency, configure the frequency division factor before the clock source;
- With the decreasing of the clock source frequency, configure the clock source before the frequency division factor.

3.4.4.8 Implementing Spread Spectrum

The spread spectrum technology is to convert a narrowband signal into a wideband signal. It helps to reduce the effect of electromagnetic interference (EMI) associated with the fundamental frequency of the signal.

For the general PLL frequency, the calculation formula is as follows:

$$f = \frac{N+1+X}{P \cdot (M0+1) \cdot (M1+1)} \cdot 24MHz, 0 < X < 1$$

Where,

P is the frequency division factor of module or PLL;

M0 is the post-frequency division factor of PLL;

M1 is the pre-frequency division factor of PLL;

N is the frequency doubling factor of PLL;

X is the amplitude coefficient of the spread spectrum.

The parameters N, P, M1, and M0 are for the frequency division.

When M1 = 0, M0 = 0, and P = 1 (no frequency division), the calculation formula of PLL frequency can be simplified as follows:

$$f = (N+1+X) \cdot 24MHz, \ 0 < X < 1$$

$$[f_1, f_2] = (N+1+[X_1, X_2]) \cdot 24MHz$$

$$SDM\_BOT = 2^{17} \cdot X_1$$

$$\text{WAVE\_STEP} = 2^{17} \cdot (X_2 - X_1) / (24\text{MHz} / PREQ) \cdot 2$$

Where, SDM_BOT and WAVE_STEP are bits of the PLL pattern control register, and PREQ is the frequency of the spread spectrum.

NOTE

Different PLLs have different calculate formulas, refer to the CTRL register of the corresponding PLL in section 3.4.6 Register Description

Configuration Procedure

Follow the steps below to implement the spread spectrum:

1. Configure the control register of the corresponding PLL
   a) Calculate the factor N and decimal value X according to the PLL frequency and PLL frequency formula. Refer to the control register of the corresponding PLL (named PLL_xxx_CTRL_REG, where xxx is the module name) in 3.4.6 Register Description for the corresponding PLL frequency formula.
   b) Write M0, M1, N, and PLL frequency to the PLL control register.
   c) Configure the SDM_ENABLE bit (bit[24]) of the PLL control register to 1 to enable the spread spectrum function.
2. Configure the pattern control register of the corresponding PLL

a) Calculate the SDM_BOT and WAVE_STEP of the pattern control register according to decimal value X and spread spectrum frequency (the bit[18:17] of the PLL_PAT register)

b) Configure the spread spectrum mode (SPR_FREQ_MODE, bit[30:29] of the PLL_PAT register) to 2 or 3.

c) If the PLL_INPUT_DIV2 of the PLL control register is 1, configure the spread spectrum clock source select bit (SDM_CLK_SEL, bit[19] of the PLL_PAT register) to 1. Otherwise, configure SDM_CLK_SEL to the default value 0.

d) Write SDM_BOT, WAVE_STEP, PREQ, SPR_FREQ_MODE, and SDM_CLK_SEL to the PLL pattern control register, and configure the SIG_DELT_PAT_EN bit (bit[31]) of this register to 1.

3. Delay 20 us

Configuration Example

The following example shows how to configure the spread spectrum frequency as 605.3 MHz to 609.7 MHz.

If M1 = 0, M0 = 0, P = 1, according to the formula $[f_1, f_2] = (N + 1 + [X_1, X_2]) \cdot 24MHz$, you can get:

$$N + 1 + [X_1, X_2] = \frac{[605.3, 609.7]}{24} = \frac{600 + [5.3, 9.7]}{24} = 24 + 1 + [5.3/24, 9.7/24]$$

Obviously,

N = 24, X1 = 5.3/24, X2 = 9.7/24

SDM_BOT = 217 * X1 = 0x7111

WAVE_STEP = 217 * (X2 – X1) /(24M/PREQ)*2 = 0x3f; PREQ = 31.5 kHz

If M0 = 1, M1=0, P = 1, then total frequency division factor is (M0 + 1) *1 = 2, so the actual output frequency of PLL is 1212.1 MHz to 1219.4 MHz.

Similarly, you can get:

N = 49, X1 = 12.1/24, X2 = 19.4/24

Then calculate the values of SDM_BOT and WAVE_STEP according to the formulas, and follow the steps described in Configuration Procedure.

3.4.5 Register List

Module Name	Base Address	Comments
CCMU	0x02001000	

Register Name	Offset	Description
PLL_CPU_CTRL_REG	0x0000	PLL_CPU Control Register
PLL_DDR_CTRL_REG	0x0010	PLL_DDR Control Register
PLL_PERI_CTRL_REG	0x0020	PLL_PERI Control Register
PLL_VIDEO_CTRL_REG	0x0040	PLL_VIDEO Control Register
PLL_CSI_CTRL_REG	0x0048	PLL_CSI Control Register
PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_NPU_CTRL_REG	0x0080	PLL_NPU Control Register
PLL_DDR_PAT0_CTRL_REG	0x0110	PLL_DDR Pattern0 Control Register
PLL_DDR_PAT1_CTRL_REG	0x0114	PLL_DDR Pattern1 Control Register
PLL_PERI_PAT0_CTRL_REG	0x0120	PLL_PERI Pattern0 Control Register
PLL_PERI_PAT1_CTRL_REG	0x0124	PLL_PERI Pattern1 Control Register
PLL_VIDEO_PAT0_CTRL_REG	0x0140	PLL_VIDEO Pattern0 Control Register
PLL_VIDEO_PAT1_CTRL_REG	0x0144	PLL_VIDEO Pattern1 Control Register
PLL_CSI_PAT0_CTRL_REG	0x0148	PLL_CSI Pattern0 Control Register
PLL_CSI_PAT1_CTRL_REG	0x014C	PLL_CSI Pattern1 Control Register
PLL_AUDIO_PAT0_CTRL_REG	0x0178	PLL_AUDIO Pattern0 Control Register
PLL_AUDIO_PAT1_CTRL_REG	0x017C	PLL_AUDIO Pattern1 Control Register
PLL_NPU_PAT0_CTRL_REG	0x0180	PLL_NPU Pattern0 Control Register
PLL_NPU_PAT1_CTRL_REG	0x0184	PLL_NPU Pattern1 Control Register
PLL_CPU_BIAS_REG	0x0300	PLL_CPU Bias Register
PLL_DDR_BIAS_REG	0x0310	PLL_DDR Bias Register
PLL_PERI_BIAS_REG	0x0320	PLL_PERI Bias Register
PLL_VIDEO_BIAS_REG	0x0340	PLL_VIDEO Bias Register
PLL_CSI_BIAS_REG	0x0348	PLL_CSI Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_NPU_BIAS_REG	0x0380	PLL_NPU Bias Register
PLL_CPU_TUN_REG	0x0400	PLL_CPU Tuning Register
CPU_CLK_REG	0x0500	CPU Clock Register
CPU_GATING_REG	0x0504	CPU Gating Configuration Register
AHB_CLK_REG	0x0510	AHB Clock Register
APB0_CLK_REG	0x0520	APB0 Clock Register
APB1_CLK_REG	0x0524	APB1 Clock Register
MBUS_CLK_REG	0x0540	MBUS Clock Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
NPU_CLK_REG	0x06E0	NPU Clock Register

Register Name	Offset	Description
NPU_BGR_REG	0x06EC	NPU Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
MSGBOX_BGR_REG	0x071C	MSGBOX Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	SPINLOCK Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HSTIMER Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
IOMMU_BGR_REG	0x07BC	IOMMU Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MAT_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPI3_CLK_REG	0x094C	SPI3 Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
EMAC_25M_CLK_REG	0x0970	EMAC_25M Clock Register
EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
I2S1_CLK_REG	0x0A14	I2S1 Clock Register
I2S_BGR_REG	0x0A20	I2S Bus Gating Reset Register
DMIC_CLK_REG	0x0A40	DMIC Clock Register
DMIC_BGR_REG	0x0A4C	DMIC Bus Gating Reset Register
AUDIO_CODEC_DAC_CLK_REG	0x0A50	AUDIO_CODEC_DAC Clock Register
AUDIO_CODEC_ADC_CLK_REG	0x0A54	AUDIO_CODEC_ADC Clock Register
AUDIO_CODEC_BGR_REG	0x0A5C	AUDIO_CODEC Bus Gating Reset Register
USB0_CLK_REG	0x0A70	USB0 Clock Register
USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
DPSS_TOP_BGR_REG	0x0ABC	DPSS_TOP Bus Gating Reset Register
DSI_CLK_REG	0x0B24	DSI Clock Register
DSI_BGR_REG	0x0B4C	DSI Bus Gating Reset Register
TCONLCD_CLK_REG	0x0B60	TCONLCD Clock Register
TCONLCD_BGR_REG	0x0B7C	TCONLCD Bus Gating Reset Register
CSI_CLK_REG	0x0C04	CSI Clock Register

Register Name	Offset	Description
CSI_MASTER0_CLK_REG	0x0C08	CSI Master0 Clock Register
CSI_MASTER1_CLK_REG	0x0C0C	CSI Master1 Clock Register
CSI_MASTER2_CLK_REG	0x0C10	CSI Master2 Clock Register
CSI_BGR_REG	0x0C2C	CSI Bus Gating Reset Register
WIEGAND_BGR_REG	0x0C7C	WIEGAND Bus Gating Reset Register
RISCV_CLK_REG	0x0D00	RISCV Clock Register
RISCV_GATING_RST_REG	0x0D04	RISCV Gating and Reset Configuration Register
RISCV_CFG_BGR_REG	0x0D0C	RISCV_CFG Bus Gating Reset Register
PLL_PRE_DIV_REG	0x0E00	PLL Pre Divider Register
AHB_GATE_EN_REG	0x0E04	AHB Gate Enable Register
PERIPLL_GATE_EN_REG	0x0E08	PERIPLL Gate Enable Register
CLK24M_GATE_EN_REG	0x0E0C	CLK24M Gate Enable Register
CCMU_SEC_SWITCH_REG	0x0F00	CCMU Security Switch Register
GPADC_CLK_SEL_REG	0x0F04	GPADC Clock Select Register
FRE_DET_CTRL_REG	0x0F08	Frequency Detect Control Register
FRE_UP_LIM_REG	0x0F0C	Frequency Up Limit Register
FRE_DOWN_LIM_REG	0x0F10	Frequency Down Limit Register
CCMU_FAN_GATE_REG	0x0F30	CCMU FANOUT CLOCK GATE Register
CLK27M_FAN_REG	0x0F34	CLK27M FANOUT Register
CLK_FAN_REG	0x0F38	CLK FANOUT Register
CCMU_FAN_REG	0x0F3C	CCMU FANOUT Register

3.4.6 Register Description

3.4.6.1 0x0000 PLL_CPU Control Register (Default Value: 0x4A00_1000)

Offset: 0x0000			Register Name: PLL_CPU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The CPUPLL= InputFreq*N. **Note: The PLL_CPU output frequency must be in the range from 200 MHz to 3 GHz. And the default value of PLL_CPUX is 408 MHz when the crystal oscillator is 24 MHz.**
30	R/W	0x1	PLL_LDO_EN LDO Enable 0: Disable 1: Enable

Offset: 0x0000			Register Name: PLL_CPU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock info 0: Unlocked 1: Locked (It indicates that the PLL has been stable)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:24	R/W	0x2	PLL_LOCK_TIME PLL lock time The bit indicates the step amplitude from one frequency to another.
23:16	/	/	/
15:8	R/W	0x10	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254 In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1:0	R/W	0x0	PLL_M PLL_M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3 **Note: The M factor is only for testing.**

3.4.6.2 0x0010 PLL_DDR Control Register (Default Value: 0x4800_2301)

Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable The DDRPLL= InputFreq*N/M1/M0 **Note: The default value of PLL_DDR is 432 MHz when the crystal oscillator is 24 MHz.**
30	R/W	0x1	PLL_LDO_EN LDO enable 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable 0: Disable 1: Enable The bit is used to control the output enable of the PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN PLL SDM Enable 0: Disable 1:Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_N PLL N N= PLL_N +1 PLL_N is from 0 to 254 In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Offset: 0x0010			Register Name: PLL_DDR_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2 PLL Input Div M1. M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2 PLL Output Div M0. M0=PLL_OUTPUT_DIV2 + 1 PLL_OUTPUT_DIV2 is from 0 to 1.

3.4.6.3 0x0020 PLL_PERI Control Register (Default Value: 0x4821_6310)

Offset: 0x0020			Register Name: PLL_PERI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN. PLL Enable 0: Disable 1: Enable PERIPLL2X = 24MHz*N/M/P0 PERI_800M = 24MHz*N/M/P1 PERI_480M = 24MHz*N/M/P2 PERI_600M = 24MHz*N/M/P0/2 PERI_400M = 24MHz*N/M/P0/3 PERI_300M = PERI_600M/2 PERI_200M = PERI_400M/2 PERI_160M = PERI_480M/3 PERI_150M = PERI_300M/2 When the crystal oscillator is 24 MHz, the default frequency of PLL_PERI(2X) is 1.2 GHz, the default frequency of PLL_PERI(1X) is 480 MHz, and the default frequency of PLL_PERI(800M) is 800 MHz. **Note: The output clock of PLL_PERI(2X) is fixed to 1.2 GHz and not suggested to change the parameter.**
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable

Offset: 0x0020			Register Name: PLL_PERI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable. Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x2	PLL_P1. PLL Output Div P1. P1=PLL_OUTPUT_DIV_P1 + 1 PLL_OUTPUT_DIV_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0. PLL Output Div P0. P0=PLL_OUTPUT_DIV_P0 + 1 PLL_OUTPUT_DIV_P0 is from 0 to 7.
15:8	R/W	0x63	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 12.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Offset: 0x0020			Register Name: PLL_PERI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	R/W	0x4	PLL_P2. PLL Output Div P2. P2=PLL_OUTPUT_DIV_P2 + 1 PLL_OUTPUT_DIV_P2 is from 0 to 7.
1	R/W	0x0	PLL_INPUT_DIV2. PLL Input Div M. M1=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	/	/	/

3.4.6.4 0x0040 PLL_VIDEO Control Register (Default Value: 0x4800_6203)

Offset: 0x0040			Register Name: PLL_VIDEO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. For application, VIDEOPLL4X = InputFreq *N/M. VIDEOPLL2X = InputFreq *N/M/2. VIDEOPLL1X = InputFreq *N/M/4. When the HOSC is 24 MHz, the default frequency of PLL_VIDEO0(4X) is 1188 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)

Offset: 0x0040			Register Name: PLL_VIDEO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x62	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV2. PLL Input Div M. M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2. PLL Output Div D. D=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. (The factor is only for testing) For test, VIDEOPLL4X = 24MHz*N/M/D

3.4.6.5 0x0048 PLL_CSI Control Register (Default Value: 0x4800_6203)

Offset: 0x0048			Register Name: PLL_CSI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable. 1: Enable. CSIPLL4X = InputFreq*N/M. CSIPLL2X = InputFreq*N/M/2. CSIPLL1X = InputFreq*N/M/4. When the HOSC is 24 MHz, the default frequency of PLL_CSI(4X) is 1188 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable.
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.

Offset: 0x0048			Register Name: PLL_CSI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV2. PLL Input Div M. M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2. PLL Output Div D. D=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. (The factor is only for testing) For test, CSIPLL4X =24MHz*N/M/D

3.4.6.6 0x0078 PLL_AUDIO Control Register (Default Value: 0x4841_7F00)

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable The AUDIOPLL_DIV2 = 24MHz*N/M /P0 The AUDIOPLL_DIV5 = 24MHz*N/M /P1 The AUDIOPLL4X = AUDIOPLL_DIV2/AUDIOPLL4X_DIV(0x0E00). The AUDIOPLL1X = AUDIOPLL_DIV5/AUDIOPLL1X_DIV(0x0E00) The working frequency range of 24MHz/M*N is from 180 MHz to 3.0 GHz. AUDIOPLL_DIV2 default is 1536MHz， AUDIOPLL_DIV5 default is 614.4MHz(24.576Mhz*25).
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0: Unlocked 1: Locked (It indicates that the PLL has been stable) **Note: The bit is only valid when the bit29 is set to 1.**
27	R/W	0x1	PLL_OUTPUT_GATE. PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable. Enable spread spectrum and decimal division.
23	/	/	/
22:20	R/W	0x4	PLL_P1. PLL Output Div P1. P1=PLL_OUTPUT_DIV_P1 + 1 PLL_OUTPUT_DIV_P1 is from 0 to 7.
19	/	/	/
18:16	R/W	0x1	PLL_P0. PLL Output Div P0. P0=PLL_OUTPUT_DIV_P0 + 1 PLL_OUTPUT_DIV_P0 is from 0 to 7.
15:8	R/W	0x7F	PLL_FACTOR_N PLL Factor N. N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. Enable spread spectrum and decimal division.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles

Offset: 0x0078			Register Name: PLL_AUDIO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2. PLL Input Div M. M=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	/	/	/

3.4.6.7 0x0080 PLL_NPU Control Register (Default Value: 0x4800_2901)

Offset: 0x0080			Register Name: PLL_NPU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_EN. PLL Enable. 0: Disable 1: Enable The NPUPLL4X = 24MHz*N/M. The NPUPLL2X = 24MHz*N/M/2. The NPUPLL1X = 24MHz*N/M/4. The working frequency range of PLL_NPU(4X) is from 180 MHz to 3.5 GHz. The default frequency of PLL_NPU(4X) is 3072 MHz.
30	R/W	0x1	PLL_LDO_EN. LDO enable. 0: Disable 1: Enable
29	R/W	0x0	LOCK_ENABLE Lock Enable. 0: Disable 1: Enable
28	R	0x0	LOCK PLL Lock Info. 0:Unlocked 1: Locked (It indicates that the PLL has been stable.) **Note: The bit is only valid when the bit29 is set to 1.**

Offset: 0x0080			Register Name: PLL_NPU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27	R/W	0x1	PLL_OUTPUT_GATE PLL Output Gating Enable. 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. PLL SDM Enable. 0: Disable. 1: Enable. Enable spread spectrum and decimal division.
23:16	/	/	/
15:8	R/W	0x29	PLL_N PLL N. N= PLL_N +1 PLL_N is from 0 to 254. In application, PLL_N shall be more than or equal to 11.
7:6	R/W	0x0	PLL_UNLOCK_MDSEL PLL Unlock Level. 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
5	R/W	0x0	PLL_LOCK_MDSEL PLL Lock Level. 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
4:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV2. PLL Input Div M. M=PLL_INPUT_DIV2 + 1 PLL_INPUT_DIV2 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV2. PLL Output Div D. D=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. (The factor is only for testing) For test, NPUPLL4X = 24MHz*N/M/D

3.4.6.8 0x0110 PLL_DDR Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz **Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.**
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.9 0x0114 PLL_DDR Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PLL_DDR_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.10 0x0120 PLL_PERI Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PLL_PERI_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz **Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.**
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.11 0x0124 PLL_PERI Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PLL_PERI_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.12 0x0140 PLL_VIDEO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz **Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.**
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.13 0x0144 PLL_VIDEO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.14 0x0148 PLL_CSI Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_CSI_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz **Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.**
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.15 0x014C PLL_CSI Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PLL_CSI_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.16 0x0178 PLL_AUDIO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz **Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.**
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.17 0x017C PLL_AUDIO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PLL_AUDIO_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.18 0x0180 PLL_NPU Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PLL_NPU_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select. 0: 24MHz 1: 12MHz **Note: When the PLL_INPUT_DIV2 is 1, the bit needs to be set to 1.**
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.4.6.19 0x0184 PLL_NPU Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: PLL_NPU_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN. Dither Enable.
23:21	/	/	/
20	R/W	0x0	FRAC_EN. Fraction Enable.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN. Fraction In.

3.4.6.20 0x0300 PLL_CPU Bias Register (Default Value: 0x8010_0000)

Offset: 0x0300			Register Name: PLL_CPU_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	PLL_VCO_RST_IN. VCO reset in.
30:21	/	/	/
20:16	R/W	0x10	PLL_CP. PLL current bias control.
15:0	/	/	/

3.4.6.21 0x0310 PLL_DDR Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.22 0x0320 PLL_PERI Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control .
15:0	/	/	/

3.4.6.23 0x0340 PLL_VIDEO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control .
15:0	/	/	/

3.4.6.24 0x0348 PLL_CSI Bias Register (Default Value: 0x0003_0000)

Offset: 0x0348			Register Name: PLL_CSI_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.25 0x0378 PLL_AUDIO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.26 0x0380 PLL_NPU Bias Register (Default Value: 0x0003_0000)

Offset: 0x0380			Register Name: PLL_NPU_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x3	PLL_CP. PLL bias control.
15:0	/	/	/

3.4.6.27 0x0400 PLL_CPU Tuning Register (Default Value: 0x4440_4000)

Offset: 0x0400			Register Name: PLL_CPU_TUN_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x4	PLL_VCO. VCO range control.
27	/	/	/
26:24	R/W	0x4	PLL_VCO_GAIN. KVCO gain control.
23	/	/	/
22:16	R/W	0x40	PLL_CNT_INT. Counter initial control.
15	R/W	0x0	PLL_REG_OD. PLL REG OD0 for verify.

Offset: 0x0400			Register Name: PLL_CPU_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
14:8	R/W	0x40	PLL_B_IN. PLL B IN for verify.
7	R/W	0x0	PLL_REG_OD1. PLL REG OD1 for verify.
6:0	R	0x0	PLL_B_OUT. PLL B OUT for verify.

3.4.6.28 0x0500 CPU Clock Register (Default Value: 0x0000_0301)

Offset: 0x0500			Register Name: CPU_CLK_REG:
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CPU_CLK_SEL. Clock Source Select. 000: HOSC 001: CLK32K 010: CLK16M_RC 011: CPUPLL/P 100: PERI_600M_BUS 101: PERI_800M CPU_CLK = Clock Source. CPU_AXI Clock = CPU_CLK/M. CPU_APB Clock= CPU_CLK/N. **Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.**
23:18	/	/	/
17:16	R/W	0x0	PLL_CPU_OUT_EXT_DIVP. Factor P. 00:1 01:2 10:4 11: \ **Note: when the output clock is less than 288 MHz, use PLL_OUT_EXT_DIVP to output the required clock frequency.**
15:10	/	/	/
9:8	R/W	0x3	CPU_APB_DIV_CFG. Factor N. (N = FACTOR_N +1) FACTOR_M is from 0 to 3 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:2	/	/	/

Offset: 0x0500			Register Name: CPU_CLK_REG:
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	CPU_AXI_DIV_CFG. Factor M:(M= FACTOR_M +1) FACTOR_M is from 1 to 3 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**

3.4.6.29 0x0504 CPU Gating Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0504			Register Name: CPU_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:16	W	0x0	CPU_GATING_FIELD. CPU Gating Field. If CPU_GATING_FIELD == 16'h16AA, bit[15:0] can be configured.
15:1	/	/	/
0	R/W	0x1	CPU_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

3.4.6.30 0x0510 AHB Clock Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: AHB_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI_600M_BUS AHB_CLK = Clock Source/M/N. **Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.**
23:10	/	/	/

Offset: 0x0510			Register Name: AHB_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1 FACTOR_M is from 0 to 31. **Note: This clock divider can be glitch-freely switched, and supports the dynamic configuration.**

3.4.6.31 0x0520 APB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI_600M_BUS APB0_CLK = Clock Source/M/N. **Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.**
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:5	/	/	/

Offset: 0x0520			Register Name: APB0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1 FACTOR_M is from 0 to 31. **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**

3.4.6.32 0x0524 APB1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: APB1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 00: HOSC 01: CLK32K 10: CLK16M_RC 11: PERI_600M_BUS APB1_CLK = Clock Source/M/N. **Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.**
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31. **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**

3.4.6.33 0x0540 MBUS Clock Register (Default Value: 0x4000_0000)

Offset: 0x0540			Register Name: MBUS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x1	MBUS_RST. MBUS Reset. 0: Assert 1: De-assert
29:0	/	/	/

3.4.6.34 0x0600 DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DE_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: PERI_300M 1: VIDEOPLL1X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.35 0x060C DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DE_RST. DE Reset. 0: Assert 1: De-assert
15:1	/	/	/

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DE_GATING. Gating Clock For DE. 0: Mask 1: Pass

3.4.6.36 0x0630 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG:
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	G2D_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON G2D_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: PERI_300M 1: VIDEOPLL1X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.37 0x063C G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	G2D_RST. G2D Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING. Gating Clock For G2D. 0: Mask 1: Pass

3.4.6.38 0x0680 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CE_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 001: PERI_400M 010: PERI_300M
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.39 0x068C CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	CE_SYS_RST. CE_SYS Reset. 0: Assert 1: De-assert
16	R/W	0x0	CE_RST. CE Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	CE_SYS_GATING. Gating Clock For CE_SYS. 0: Mask 1: Pass
0	R/W	0x0	CE_GATING. Gating Clock For CE. 0: Mask 1: Pass

3.4.6.40 0x0690 VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VE_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON VE_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: PERI_300M 001: PERI_400M 010: PERI_480M 011: NPUPLL4X 100: VIDEOPLL4X 101: CSIPLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.41 0x069C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VE_RST. VE Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING. Gating Clock for VE. 0: Mask 1: Pass

3.4.6.42 0x06E0 NPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x06E0			Register Name: NPU_CLK_REG:
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	NPU_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON NPU_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: PERI_480M 001: PERI_600M 010: PERI_800M 011: NPUPLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.43 0x06EC NPU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06EC			Register Name: NPU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NPU_RST. NPU Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	NPU_GATING. Gating Clock For NPU. 0: Mask 1: Pass

3.4.6.44 0x070C DMA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	DMA_RST. DMA Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING. Gating Clock For DMA. 0: Mask 1: Pass

3.4.6.45 0x071C MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: MSGBOX_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	MSGBOX1_RST. RISCV MSGBOX Reset. 0: Assert 1: De-assert
16	R/W	0x0	MSGBOX0_RST. CPU MSGBOX0 Reset. 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	MSGBOX1_GATING. Gating Clock For MSGBOX1 RISCV. 0: Mask 1: Pass
0	R/W	0x0	MSGBOX0_GATING. Gating Clock For MSGBOX0 CPU. 0: Mask 1: Pass

3.4.6.46 0x072C SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	SPINLOCK_RST. SPINLOCK Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SPINLOCK_GATING. Gating Clock For SPINLOCK. 0: Mask 1: Pass

3.4.6.47 0x073C HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST. HSTIMER Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HSTIMER_GATING. Gating Clock For HSTIMER. 0: Mask 1: Pass

3.4.6.48 0x0740 AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	AVS_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON AVS_CLK = HOSC.
30:0	/	/	/

3.4.6.49 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST. DBGSYS Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING. Gating Clock For DBGSYS. 0: Mask 1: Pass

3.4.6.50 0x07AC PWM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PWM_RST. PWM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING. Gating Clock For PWM. 0: Mask 1: Pass

3.4.6.51 0x07BC IOMMU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07BC			Register Name: IOMMU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	IOMMU_GATING. Gating Clock For IOMMU. 0: Mask 1: Pass

3.4.6.52 0x0800 DRAM Clock Register (Default Value: 0x8000_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	DRAM_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DRAM_CLK = Clock Source/M/N.
30:28	/	/	/
27	R/WAC	0x0	DRAM_UPD. SDRCLK Configuration 0 update. 0:Invalid 1:Valid Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. Here supports dram req/ack signal. When dram_update is set to 1, dram_clk_sel/dram_div2/dram_clk1 will be updated.
26:24	R/W	0x0	DRAM_CLK_SEL. Clock Source Select. 000: DDRPLL 001: PERIPLL2X 010: PEREIPLL_800M **Note: This clock switching multiplexer is glitch-free, and supports the dynamic configuration.**
23:10	/	/	/
9:8	R/W	0x0	DRAM_DIV2. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	DRAM_DIV1. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31. **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**

3.4.6.53 0x0804 MBUS Master Clock Gating Register (Default Value: 0x003F_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x1	NPU_MBUS_GATE_SW_CFG. NPU MBUS Clock Gate Enable. 0:Disable 1:Enable
20	R/W	0x1	VID_IN_MBUS_GATE_SW_CFG. VID_IN MBUS Clock Gate Enable. 0:Disable 1:Enable
19	R/W	0x1	VID_OUT_MBUS_GATE_SW_CFG. VID_OUT MBUS Clock Gate Enable. 0:Disable 1:Enable
18	R/W	0x1	CE_MBUS_GATE_SW_CFG. CE MBUS Clock Gate Enable. 0:Disable 1:Enable
17	R/W	0x1	VE_MBUS_GATE_SW_CFG. VE MBUS Clock Gate Enable. 0:Disable 1:Enable
16	R/W	0x1	DMA_MBUS_GATE_SW_CFG. DMA MBUS Clock Gate Enable. 0:Disable 1:Enable
15:11	/	/	/
10	R/W	0x0	G2D_MCLK_EN. Gating MBUS Clock For G2D. 0: Mask 1: Pass
9	R/W	0x0	ISP_MCLK_EN. Gating MBUS Clock For ISP. 0: Mask 1: Pass
8	R/W	0x0	CSI_MCLK_EN. Gating MBUS Clock For CSI. 0: Mask 1: Pass
7:3	/	/	/

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	CE_MCLK_EN. Gating MBUS Clock For CE. 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_EN. Gating MBUS Clock For VE. 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_EN. Gating MBUS Clock For DMA. 0: Mask 1: Pass

3.4.6.54 0x080C DRAM Bus Gating Reset Register (Default Value: 0x0000_0001)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DRAM_RST. DRAM Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x1	DRAM_GATING. Gating Clock For DRAM. 0: Mask 1: Pass

3.4.6.55 0x0830 SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SMHC0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC0_CLK = Clock Source/M/N.
30:27	/	/	/

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_400M 010: PERI_300M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.56 0x0834 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SMHC1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_400M 010: PERI_300M
23:10	/	/	/

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.57 0x0838 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SMHC2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SMHC2_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_600M 010: PERI_400M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.58 0x084C SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	SMHC2_RST. SMHC2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST. SMHC1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST. SMHC0 Reset. 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING. Gating Clock For SMHC2. 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING. Gating Clock For SMHC1. 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING. Gating Clock For SMHC0. 0: Mask 1: Pass

3.4.6.59 0x090C UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19	R/W	0x0	UART3_RST. UART3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST. UART2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST. UART1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST. UART0 Reset. 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	UART3_GATING. Gating Clock For UART3. 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING. Gating Clock For UART2. 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING. Gating Clock For UART1. 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING. Gating Clock For UART0. 0: Mask 1: Pass

3.4.6.60 0x091C TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
20	R/W	0x0	TWI4_RST. TWI4 Reset. 0: Assert 1: De-assert
19	R/W	0x0	TWI3_RST. TWI3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST. TWI2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	TWI4_GATING. Gating Clock For TWI4. 0: Mask 1: Pass
3	R/W	0x0	TWI3_GATING. Gating Clock For TWI3. 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING. Gating Clock For TWI2. 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING. Gating Clock For TWI1. 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING. Gating Clock For TWI0. 0: Mask 1: Pass

3.4.6.61 0x0940 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SPI0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000:HOSC 001:PERI_300M 010:PERI_200M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.62 0x0944 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SPI1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI1_CLK = Clock Source/M/N.
30:27	/	/	/

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_300M 010: PERI_200M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.63 0x0948 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SPI2_CLK_REG:
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SPI2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI2_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_300M 010: PERI_200M
23:10	/	/	/

Offset: 0x0948			Register Name: SPI2_CLK_REG:
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.64 0x094C SPI3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x094C			Register Name: SPI3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SPI3_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON SPI3_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: PERI_300M 010: PERI_200M
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8 **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:4	/	/	/

Offset: 0x094C			Register Name: SPI3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.65 0x096C SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	SPI3_RST. SPI3 Reset. 0: Assert 1: De-assert
18	R/W	0x0	SPI2_RST. SPI2 Reset. 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST. SPI1 Reset. 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST. SPI0 Reset. 0: Assert 1: De-assert
15:3	/	/	/
3	R/W	0x0	SPI3_GATING. Gating Clock For SPI3. 0: Mask 1: Pass
2	R/W	0x0	SPI2_GATING. Gating Clock For SPI2. 0: Mask 1: Pass
1	R/W	0x0	SPI1_GATING. Gating Clock For SPI1. 0: Mask 1: Pass

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	SPI0_GATING. Gating Clock For SPI0. 0: Mask 1: Pass

3.4.6.66 0x0970 EMAC_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970			Register Name: EMAC_25M_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EMAC_25M_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON EMAC_25M_CLK =PERI_150M/6=25M
30	R/W	0x0	EMAC_25M_CLK_SRC_GATING. Gating the Source Clock For Low Power Design. 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

3.4.6.67 0x097C EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EMAC_RST. EMAC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMAC_GATING. Gating Clock For EMAC. 0: Mask 1: Pass

3.4.6.68 0x09EC GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	Read/Write	Default/Hex	Description
16	R/W	0x0	GPADC_RST. GPADC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC_GATING. Gating Clock For GPADC. 0: Mask 1: Pass

3.4.6.69 0x09FC THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			Register Name: THS_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	THS_RST. THS Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING. Gating Clock For THS. 0: Mask 1: Pass

3.4.6.70 0x0A14 I2S1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A14			Register Name: I2S1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	I2S1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON I2S1_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/

Offset: 0x0A14			Register Name: I2S1_CLK_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.71 0x0A20 I2S Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A20			Register Name: I2S_BGR_REG:
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	I2S1_RST. I2S1 Reset. 0: Assert 1: De-assert
16:2	/	/	/
1	R/W	0x0	I2S1_GATING. Gating Clock For I2S1. 0: Mask 1: Pass
0	/	/	/

3.4.6.72 0x0A40 DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A40			Register Name: DMIC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMIC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DMIC_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0:AUDIOPLL1X 1:AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.73 0x0A4C DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A4C			Register Name: DMIC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMIC_RST. DMIC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING. Gating Clock For DMIC. 0: Mask 1: Pass

3.4.6.74 0x0A50 AUDIO_CODEC_DAC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A50			Register Name: AUDIO_CODEC_DAC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	AUDIO_CODEC_DAC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_DAC_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.75 0x0A54 AUDIO_CODEC_ADC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A54			Register Name: AUDIO_CODEC_ADC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	AUDIO_CODEC_ADC_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON AUDIO_CODEC_ADC_CLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 0: AUDIOPLL1X 1: AUDIOPLL4X
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.76 0x0A5C AUDIO_CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A5C			Register Name: AUDIO_CODEC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST. AUDIO_CODEC Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING. Gating Clock For AUDIO_CODEC. 0: Mask 1: Pass

3.4.6.77 0x0A70 USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	USB0_CLKEN. Gating Clock For OHCI0. 0: Clock is OFF 1: Clock is ON

Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0x0	USBPHY0_RSTN. USB PHY0 Reset. 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	USB0_CLK12M_SEL OHCI0 12M Source Select. 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: RTC_32K 11: /
23:0	/	/	/

3.4.6.78 0x0A8C USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	USBOTG0_RST. USBOTG0 Reset. 0: Assert 1: De-assert
23:21	/	/	/
20	R/W	0x0	USBEHCI0_RST. USBEHCI0 Reset. 0: Assert 1: De-assert
19:17	/	/	/
16	R/W	0x0	USBOHCI0_RST. USBOHCI0 Reset. 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USBOTG0_GATING. Gating Clock For USBOTG0. 0: Mask 1: Pass
7:5	/	/	/

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	USBEHCI0_GATING. Gating Clock For USBEHCI0. 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	USBOHCI0_GATING. Gating Clock For USBOHCI0. 0: Mask 1: Pass

3.4.6.79 0x0ABC DPSS_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0ABC			Register Name: DPSS_TOP_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DPSS_TOP_RST. DPSS_TOP Reset. 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DPSS_TOP_GATING. Gating Clock For DPSS_TOP. 0: Mask 1: Pass

3.4.6.80 0x0B24 DSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: DSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DSI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON DSI_CLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000:HOSC 001:PERI_200M 010:PERI_150M
23:4	/	/	/

Offset: 0x0B24			Register Name: DSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.81 0x0B4C DSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: DSI_BGR_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	DSI_RST. DSI Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	DSI_GATING. Gating Clock For DSI. 0: Mask 1: Pass

3.4.6.82 0x0B60 TCONLCD Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCONLCD_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCONLCD_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON TCONLCD_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000:VIDEOPLL4X 001:PERIPLL2X 010:CSIPLL4X
23:10	/	/	/

Offset: 0x0B60			Register Name: TCONLCD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 15.

3.4.6.83 0x0B7C TCONLCD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCONLCD_BGR_REG:
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCONLCD_RST. TCON LCD Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	TCONLCD_GATING. Gating Clock For TCON LCD. 0: Mask 1: Pass

3.4.6.84 0x0C04 CSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_CLK = Clock Source/M.
30:27	/	/	/

Offset: 0x0C04			Register Name: CSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: PERI_300M 001: PERI_400M 010: VIDEOPLL4X 011: CSIPLL4X
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.85 0x0C08 CSI Master0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI_MASTER0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI_MASTER0_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER0_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: CSIPLL4X 010: VIDEOPLL4X 011: PERIPLL2X
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.86 0x0C0C CSI Master1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI_MASTER1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI_MASTER1_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER1_CLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: CSIPLL4X 010: VIDEOPLL4X 011: PERIPLL2X
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.87 0x0C10 CSI Master2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C10			Register Name: CSI_MASTER2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CSI_MASTER2_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CSI_MASTER2_CLK = Clock Source/M/N.
30:27	/	/	/

Offset: 0x0C10			Register Name: CSI_MASTER2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select. 000: HOSC 001: CSIPLL4X 010: VIDEOPLL4X 011: PERIPLL2X
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.88 0x0C2C CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C2C			Register Name: CSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI_RST. CSI Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING. Gating Clock For CSI. 0: Mask 1: Pass

3.4.6.89 0x0C7C WIEGAND Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C7C			Register Name: WIEGAND_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/

Offset: 0x0C7C			Register Name: WIEGAND_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	WIEGAND_RST. WIEGAND Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	WIEGAND_GATING. Gating Clock For WIEGAND. 0: Mask 1: Pass

3.4.6.90 0x0D00 RISCV Clock Register (Default Value: 0x0000_0100)

Offset: 0x0D00			Register Name: RISCV_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	RISCV_CLK_SEL. Clock Source Select. 000: HOSC 001: CLK32K 010: CLK16M_RC 011: PERI_600M 100: PERI_480M 101: CPUPLL RISCV_CLK = Clock Source/M. RISCV_AXI_CLK = RISCV_CLK/N.
23:10	/	/	/
9:8	R/W	0x1	RISCV_AXI_DIV_CFG. Factor N. N = FACTOR_N +1). FACTOR_N is from 1 to 3. **Note: This clock divider can be switched glitch-freely, and supports the dynamic configuration.**
7:5	/	/	/
4:0	R/W	0x0	RISCV_DIV_CFG. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.91 0x0D04 RISCV Gating and Reset Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0D04			Register Name: RISCV_GATING_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	RISCV_GATING_RST_FIELD. RISCV Gating and Reset Field. If RISCV_GATING_RST_FIELD == 16'h16AA, the bit[15:0] can be configured.
15:3	/	/	/
2	R/W	0x0	RISCV_SYS_APB_SOFT_RSTN. Reset for RISCV Debug Bus. 0: Assert 1: De-assert
1	R/W	0x0	RISCV_SOFT_RSTN. Reset for RISCV. 0: Assert 1: De-assert
0	R/W	0x0	RISCV_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON

3.4.6.92 0x0D0C RISCV_CFG Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0D0C			Register Name: RISCV_CFG_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	RISCV_CFG_RST. RISCV Reset. 0: Assert 1: DE-assert
15:1	/	/	/
0	R/W	0x0	RISCV_CFG_GATING. Gating Clock For RISCV. 0: Mask 1: Pass

3.4.6.93 0x0E00 PLL Pre Divider Register (Default Value: 0x0000_0000)

Offset: 0x0E00			Register Name: PLL_PRE_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/

Offset: 0x0E00			Register Name: PLL_PRE_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9:5	R/W	0x0	AUDIOPLL4X_DIV. Factor N. Source is AUDIOPLL_DIV2. N= FACTOR_N +1. FACTOR_N is from 0 to 31.
4:0	R/W	0x0	AUDIOPLL1X_DIV. Factor M. Source is AUDIOPLL_DIV5. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.94 0x0E04 AHB Gate Enable Register (Default Value: 0x1000_3FFF)

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	AHB_MONITOR_EN AHB bus auto clock gating function enable. 1: enable auto clock gate 0: disable auto clock gate
30	/	/	/
29	R/W	0x0	SD_MONITOR_EN SD bus auto clock gating function enable. 1: enable auto clock gate 0: disable auto clock gate
28	R/W	0x1	CPUS_HCLK_GATE_SW_CFG. CPUS AHB Clock Gate Enable. 0:Disable 1:Enable
27:14	/	/	/
13	R/W	0x1	EMAC_MBUS_AHB_GATE_SW_CFG. EMAC MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
12	R/W	0x1	SMHC2_MBUS_AHB_GATE_SW_CFG. SMHC2 MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
11	R/W	0x1	SMHC1_MBUS_AHB_GATE_SW_CFG. SMHC1 MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
10	R/W	0x1	SMHC0_MBUS_AHB_GATE_SW_CFG. SMHC0 MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
9	R/W	0x1	USB_MBUS_AHB_GATE_SW_CFG. USB MBUS_AHB Clock Gate Enable. 0: Disable 1: Enable
8	R/W	0x1	EMAC_AHB_GATE_SW_CFG. EMAC AHB Clock Gate Enable. 0: Disable 1: Enable
7	R/W	0x1	SMHC2_AHB_GATE_SW_CFG. SMHC2 AHB Clock Gate Enable. 0: Disable 1: Enable
6	R/W	0x1	SMHC1_AHB_GATE_SW_CFG. SMHC1 AHB Clock Gate Enable. 0: Disable 1: Enable
5	R/W	0x1	SMHC0_AHB_GATE_SW_CFG. SMHC0 AHB Clock Gate Enable. 0: Disable 1: Enable
4	R/W	0x1	USB_AHB_GATE_SW_CFG. USB AHB Clock Gate Enable. 0: Disable 1: Enable
3	R/W	0x1	VID_OUT_AHB_GATE_SW_CFG. Video Out AHB Clock Gate Enable. 0: Disable 1: Enable
2	R/W	0x1	VID_IN_AHB_GATE_SW_CFG. Video in AHB Clock Gate Enable. 0: Disable 1: Enable
1	R/W	0x1	VE_AHB_GATE_SW_CFG. VE AHB Clock Gate Enable. 0: Disable 1: Enable

Offset: 0x0E04			Register Name: AHB_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x1	NPU_AHB_GATE_SW_CFG. NPU AHB Clock Gate Enable. 0: Disable 1: Enable

3.4.6.95 0x0E08 PERIPLL Gate Enable Register (Default Value: 0x0FFF_0FFF)

Offset: 0x0E08			Register Name: PERIPLL_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	PERIPLL2X_GATE_SW_CFG. PERIPLL2X Clock Gate Enable. 0:Disable 1:Enable
26	R/W	0x1	PERI_800M_GATE_SW_CFG. PERI 800M Clock Gate Enable. 0:Disable 1:Enable
25	R/W	0x1	PERI_600M_GATE_SW_CFG. PERI 600M Clock Gate Enable. 0:Disable 1:Enable
24	R/W	0x1	PERI_480M_GATE_ALL_CFG. PERI 480M Clock Gate Enable. 0:Disable 1:Enable
23	R/W	0x1	PERI_480M_GATE_SW_CFG. PERI 480M Clock Gate Enable. 0:Disable 1:Enable
22	R/W	0x1	PERI_160M_GATE_SW_CFG. PERI 160M Clock Gate Enable. 0:Disable 1:Enable
21	R/W	0x1	PERI_300M_GATE_ALL_CFG. PERI 300M Clock Gate Enable. 0:Disable 1:Enable
20	R/W	0x1	PERI_300M_GATE_SW_CFG. PERI 300M Clock Gate Enable. 0:Disable 1:Enable

Offset: 0x0E08			Register Name: PERIPLL_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19	R/W	0x1	PERI_150M_GATE_SW_CFG. PERI 150M Clock Gate Enable. 0:Disable 1:Enable
18	R/W	0x1	PERI_400M_GATE_ALL_CFG. PERI 400M Clock Gate Enable. 0:Disable 1:Enable
17	R/W	0x1	PERI_400M_GATE_SW_CFG. PERI 400M Clock Gate Enable. 0:Disable 1:Enable
16	R/W	0x1	PERI_200M_GATE_SW_CFG. PERI 200M Clock Gate Enable. 0:Disable 1:Enable
15:12	/	/	/
11	R/W	0x1	PERIPLL2X_AUTO_GATE_EN. PERIPLL2X Clock Auto Gate Enable. 0:Auto 1:No-Auto
10	R/W	0x1	PERI_800M_AUTO_GATE_EN. PERI 800M Clock Auto Gate Enable. 0:Auto 1:No-Auto
9	R/W	0x1	PERI_600M_AUTO_GATE_EN. PERI 600M Clock Auto Gate Enable. 0:Auto 1:No-Auto
8	R/W	0x1	PERI_480M_AUTO_GATE_EN_ALL. PERI 480M Clock Auto Gate Enable. 0:Auto 1:No-Auto
7	R/W	0x1	PERI_480M_AUTO_GATE_EN. PERI 480M Clock Auto Gate Enable. 0:Auto 1:No-Auto
6	R/W	0x1	PERI_160M_AUTO_GATE_EN. PERI 160M Clock Auto Gate Enable. 0:Auto 1:No-Auto

Offset: 0x0E08			Register Name: PERIPLL_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x1	PERI_300M_AUTO_GATE_EN_ALL. PERI 300M Clock Auto Gate Enable. 0:Auto 1:No-Auto
4	R/W	0x1	PERI_300M_AUTO_GATE_EN. PERI 300M Clock Auto Gate Enable. 0:Auto 1:No-Auto
3	R/W	0x1	PERI_150M_AUTO_GATE_EN. PERI 150M Clock Auto Gate Enable. 0:Auto 1:No-Auto
2	R/W	0x1	PERI_400M_AUTO_GATE_EN_ALL. PERI 400M Clock Auto Gate Enable All. 0:Auto 1:No-Auto
1	R/W	0x1	PERI_400M_AUTO_GATE_EN. PERI 400M Clock Auto Gate Enable. 0:Auto 1:No-Auto
0	R/W	0x1	PERI_200M_AUTO_GATE_EN. PERI 200M Clock Auto Gate Enable. 0:Auto 1:No-Auto

3.4.6.96 0x0E0C CLK24M Gate Enable Register (Default Value: 0x0000_000F)

Offset: 0x0E0C			Register Name: CLK24M_GATE_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x1	RES_DCAP_24M_GATE_EN. RES_DCAP 24M Clock Gate Enable. 0:Disable 1:Enable
2	R/W	0x1	GPADC_24M_GATE_EN. GPADC 24M Clock Gate Enable. 0:Disable 1:Enable
1	R/W	0x1	WIEGAND_24M_GATE_EN. WIEGAND 24M Clock Gate Enable. 0:Disable 1:Enable

Offset: 0x0E0C			Register Name: CLK24M_GATE_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	USB_24M_GATE_EN. USB 24M Clock Gate Enable. 0:Disable 1:Enable

3.4.6.97 0x0F00 CCMU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCMU_SEC_SWITCH_REG:
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MBUS_SEC. MBUS clock register security. 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC. Bus relevant registers security. 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC. PLL relevant registers security. 0: Secure 1: Non-secure

3.4.6.98 0x0F04 GPADC Clock Select Register (Default Value: 0x0000_0000)

Offset: 0x0F04			Register Name: GPADC_CLK_SEL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Reserved
30:23	/	/	/
22:20	R/W	0x0	GPADC_24M_CLK_SEL GPADC 24M Clock Source Select. 000:HOSC/32 001:HOSC/16 010:HOSC/8 011:HOSC/4 100:HOSC/2 101:HOSC
19:0	/	/	/

3.4.6.99 0x0F08 Frequency Detect Control Register (Default Value: 0x0000_0020)

Offset: 0x0F08			Register Name: FRE_DET_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W0C	0x0	ERROR_FLAG. Error Flag. 0: Write 0 to clear 1: Error
30:9	/	/	/
8:4	R/W	0x2	DET_TIME Detect Time Time=1/32k*(2^RegValue) **Note： RegValue is form 0 to 16.**
3:2	/	/	/
1	R/W	0x0	FRE_DET_IRQ_EN. Frequency Detect IRQ Enable. 0: Disable 1: Enable
0	R/W	0x0	FRE_DET_FUN_EN. Frequency Detect Function Enable. 0: Disable 1: Enable

3.4.6.100 0x0F0C Frequency Up Limit Register (Default Value: 0x0000_0000)

Offset: 0x0F0C			Register Name: FRE_UP_LIM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRE_UP_LIM. Frequency Up Limit. **Note: The value of the register must be an integral multiple of 32. The unit is kHz.**

3.4.6.101 0x0F10 Frequency Down Limit Register (Default Value: 0x0000_0000)

Offset: 0x0F10			Register Name: FRE_DOWN_LIM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FRE_DOWN_LIM. Frequency Down Limit. **Note: The value of the register must be an integral multiple of 32. The unit is kHz.**

3.4.6.102 0x0F30 CCMU FANOUT CLOCK GATE Register (Default Value:0x0000_0000)

Offset: 0x0F30			Register Name: CCMU_FAN_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	CLK25M_EN. Gating for CLK25M . 0: Clock is OFF 1: Clock is ON
2	R/W	0x0	CLK16M_EN. Gating for CLK16M . 0: Clock is OFF 1: Clock is ON
1	R/W	0x0	CLK12M_EN. Gating for CLK12M . 0: Clock is OFF 1: Clock is ON
0	R/W	0x0	CLK24M_EN. Gating for CLK24M . 0: Clock is OFF 1: Clock is ON

3.4.6.103 0x0F34 CLK27M FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F34			Register Name: CLK27M_FAN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK27M_EN. Gating for CLK27M. 0: Clock is OFF 1: Clock is ON SCLK=Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK27M_SCR_SEL. Clock Source Select. 000: VIDEOPLL1X 001: CSIPLL1X 010: PERI_300M 011: /
23:10	/	/	/

Offset: 0x0F34			Register Name: CLK27M_FAN_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x0	CLK27M_DIV1. Factor N. 00: 1 01: 2 10: 4 11: 8
7:5	/	/	/
4:0	R/W	0x0	CLK27M_DIV0. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.104 0x0F38 CLK FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F38			Register Name: CLK_FAN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCLK_DIV_EN. Gating for PCLK. 0: Clock is OFF 1: Clock is ON PCLK = APB0_CLK/M/N.
30:10	/	/	/
9:5	R/W	0x0	PCLK_DIV1. Factor N. N= FACTOR_N +1. FACTOR_N is from 0 to 31.
4:0	R/W	0x0	PCLK_DIV. Factor M. M= FACTOR_M +1. FACTOR_M is from 0 to 31.

3.4.6.105 0x0F3C CCMU FANOUT Register (Default Value:0x0000_0000)

Offset: 0x0F3C			Register Name: CCMU_FAN_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	Reserved
23	R/W	0x0	CLK_FANOUT2_EN. Gating for CLK_FANOUT2. 0: Clock is OFF 1: Clock is ON

Offset: 0x0F3C			Register Name: CCMU_FAN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
22	R/W	0x0	CLK_FANOUT1_EN. Gating for CLK_FANOUT1. 0: Clock is OFF 1: Clock is ON
21	R/W	0x0	CLK_FANOUT0_EN. Gating for CLK_FANOUT0. 0: Clock is OFF 1: Clock is ON
20:18	/	/	/
17:9	R/W	0x0	Reserved
8:6	R/W	0x0	CLK_FANOUT2_SEL. Clock Fanout2 Select. 000:CLK32K_FANOUT(From SYSRTC) 001:CLK12M(From DCXO/2) 010:CLK16M(From PERI_160M/10) 011:CLK24M(From DCXO) 100:CLK25M(From PERI_150M/6) 101:CLK27M 110:PCLK CLK_FANOUT2 can be selected to output from the above seven sources.
5:3	R/W	0x0	CLK_FANOUT1_SEL. Clock Fanout1 Select. 000:CLK32K_FANOUT(From SYSRTC) 001:CLK12M(From DCXO/2) 010:CLK16M(From PERI_160M/10) 011:CLK24M(From DCXO) 100:CLK25M(From PERI_150M/6) 101:CLK27M 110:PCLK CLK_FANOUT1 can be selected to output from the above seven sources.

Offset: 0x0F3C			Register Name: CCMU_FAN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x0	CLK_FANOUT0_SEL. Clock Fanout0 Select. 000:CLK32K_FANOUT(From SYSRTC) 001:CLK12M(From DCXO/2) 010:CLK16M(From PERI_160M/10) 011:CLK24M(From DCXO) 100:CLK25M(From PERI_150M/6) 101:CLK27M 110:PCLK CLK_FANOUT0 can be selected to output from the above seven sources.

3.5 BROM System

3.5.1 Overview

The system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) that is considered the primary program-loader. On the startup process, the V851S/V851SE starts to fetch the first instruction from address 0x0, where is the BROM located at.

The BROM system is divided into two parts: the firmware exchange launch (FEL) module and the Medium Boot module. FEL is responsible for writing the external data to the local NVM, and Medium Boot is responsible for loading an effective and legitimate BOOT0 from NVM and running.

- The BROM system includes the following features:
- Supports CPU0 boot process
- Supports mandatory upgrade process through USB or SMHC0
- Supports eFuse to select the boot medium type
- Supports normal booting and secure booting
- Secure BROM loads only certified firmware
- Ensures that the Secure Boot is in a trusted environment

3.5.2 Functional Descriptions

The BROM configurations mainly select the boot medium and the boot mode.

3.5.2.1 Selecting the Boot Medium

The BROM system supports the following boot media:

- SD/EMMC
- SPI NOR
- SPI NAND

There are two ways to select the boot medium: GPIO Pin Select and eFuse Select. The BROM will read the state of BOOT_MODE first, and then select the boot medium according to the state of BOOT_MODE. The BOOT_MODE is the BROM_Config in the eFuse mapping.

The following table shows the BOOT_MODE setting:

Table 3-6 BOOT_MODE Setting

BOOT_MODE[0]	Boot Select Type
0	GPIO Pin Select
1	eFuse Select

GPIO Boot Select

If the state of the BOOT_MODE is 0, the boot medium is decided by the value of the GPIO pin. The following table shows the boot medium priority. The boot medium priority describes the possibility that each medium to be selected as the boot medium. The BROM reads the boot0 of the medium with the highest priority first. If the medium does not exist or has any problems, the BROM will try the next medium. Otherwise, the medium will be selected as the boot medium.

Table 3-7 GPIO Boot Select

Pin_Boot_Select[1:0]	Boot Medium Priority
00	SPI0 NAND->SPI0 NOR(4 wire)-> SPI NOR(1 wire)->USB
01	SPI0 NOR(4 wire)-> SPI0 NOR(1 wire)->SPI0 NAND->USB
10	SDC0->SPI0 NAND->SPI0 NOR(4 wire)-> SPI0 NOR(1 wire)->UART BRUN->USB
11	SDC0->SPI0 NOR(4 wire)-> SPI0 NOR(1 wire) -> EMMC2-> SPI0 NAND->UART BRUN->USB

NOTE

The status of the GPIO boot select pin can be read by the bit[12:11] of the system configuration module (register: 0x03000024).

eFuse Boot Select

If the state of the BOOT_MODE is 1, the boot medium is decided by the value of eFuse_Boot_Select_Cfg. The eFuse_Boot_Select_Cfg is divided into 4 groups and each group is 3-bit. The following table shows the groups of eFUSE_Boot_Select.

Table 3-8 Groups of eFuse_Boot_Select

eFuse_Boot_Select_Cfg[11:0]	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

These four groups take effect with the following priority:

eFuse_Boot_Select_1 -> eFuse_Boot_Select_2 -> eFuse_Boot_Select_3 -> eFuse_Boot_Select_4

For example, eFuse_Boot_Select_2 will not take effect unless eFuse_Boot_Select_1 is set as 0x111, eFuse_Boot_Select_3 will not take effect unless eFuse_Boot_Select_2 is set as 0x111(skip), etc.

The following table shows the boot medium priority for the different values of eFuse_Boot_Select_n, where n = [4:1]. The eFuse_Boot_Select_1 to eFuse_Boot_Select_3 are the same setting. But for eFuse_Boot_Select_4,

if its value is 0x111, the BROM will select the boot medium in the Try mode. The BROM in the Try mode follows the order below to select the boot medium:

SMHC0 -> SPI NOR -> SPI NAND -> SMHC2

Table 3-9 eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot Medium Priority
000	Try
001	reserved
010	EMMC2_USER-> EMMC2_BOOT
011	SPI0 NOR(4 wire)-> SPI0 NOR(1 wire)
100	SPI0 NAND
101	SPI0 NOR(1 wire)-> SPI0 NOR(4 wire)
110	EMMC2_BOOT-> EMMC2_USER
111	When n is 1 to 3: The boot medium is decided by the value of **eFuse_Boot_Select_(n + 1).** When n is 4: Select the boot medium in Try mode.

3.5.2.2 Selecting the Boot Mode

For SoCs that have implemented and enabled the ARM TrustZone technology, there are two boot modes: Normal BROM Mode and Secure BROM Mode.

Secure BROM Mode is designed to protect against attackers modifying the code or data areas in the programmable memory.

During the startup process, the BROM will select the boot mode according to the value of the Secure Enable bit. If the value of Secure Enable bit is 0, the system will boot in Normal BROM Mode. Otherwise, it will boot in Secure BROM Mode.

NOTE

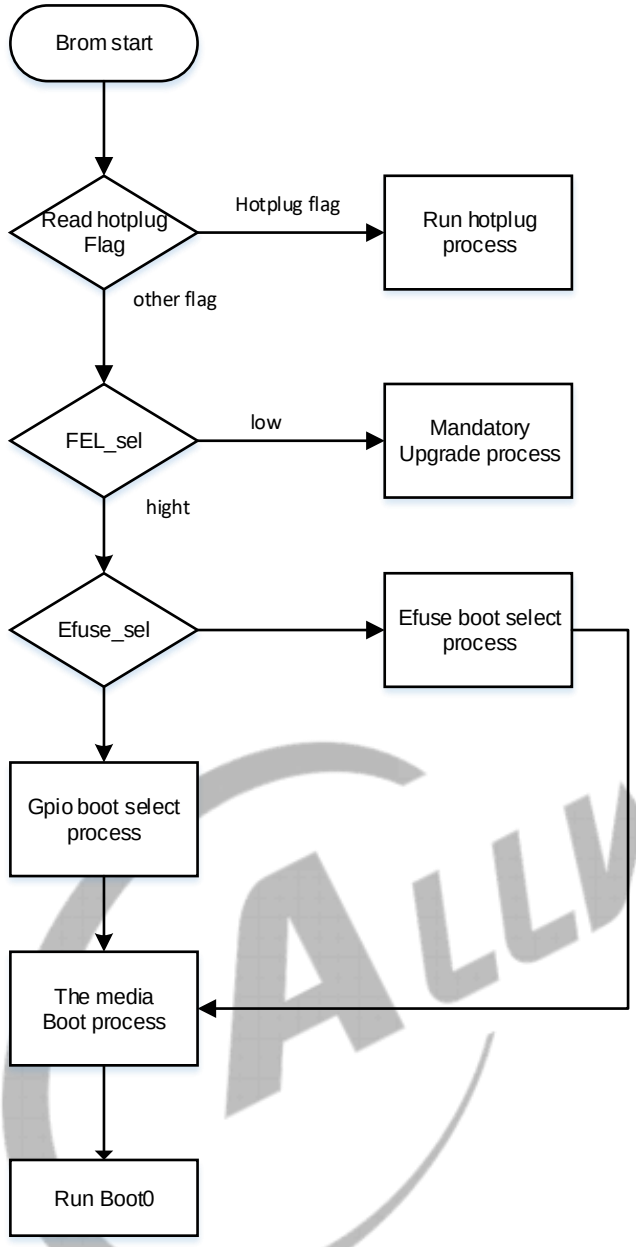
The System on Chip (SoC) supports the ARM TrustZone technology. If the Secure Enable Bit is enabled, the BROM will be safely booted based on this ARM TrustZone technology.

Normal BROM Mode

In Normal BROM Mode, the system boot starts from CPU0, and then BROM will read the state of the FEL Pin. If the FEL Pin signal is high, then the system will jump to the boot process, or jump to the mandatory upgrade process.

The following figure shows the boot process in Normal BROM Mode.

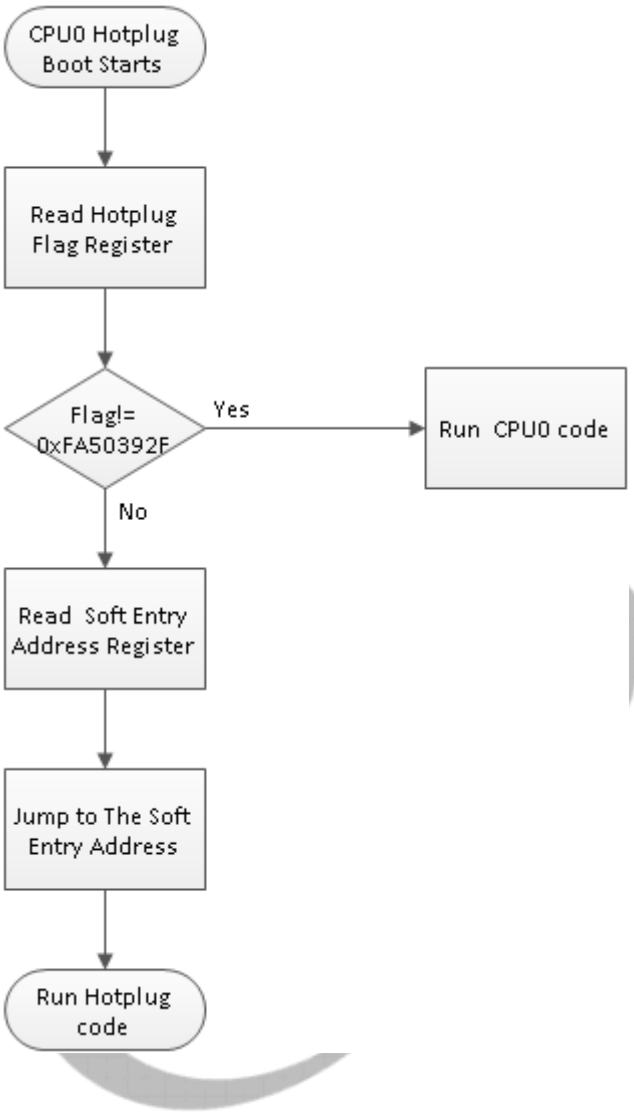
Figure 3-7 Boot Process in Normal BROM Mode



Hotplug Process

The Hotplug Flag determines whether the system will do Hotplug boot, if the CPU Hotplug Flag value is equal to 0xFA50392F, then read the Soft Entry Register and the system will jump to the Soft Entry Address. The following figure shows the CPU0 Hotplug Process.

Figure 3-8 CPU0 Hotplug Process Diagram



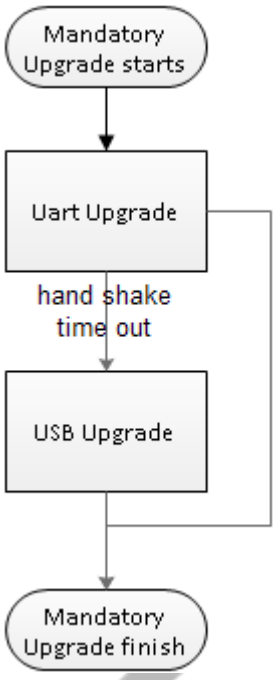
NOTE

The Hotplug Flag Register is 0x070005C0.
The Soft Entry Address Register is 0x070005C4.

Mandatory Upgrade Process

If the FEL pin is detected to pull low, the system will jump to the mandatory upgrade process. The following figure shows the mandatory upgrade process.

Figure 3-9 Mandatory Upgrade Process



NOTE

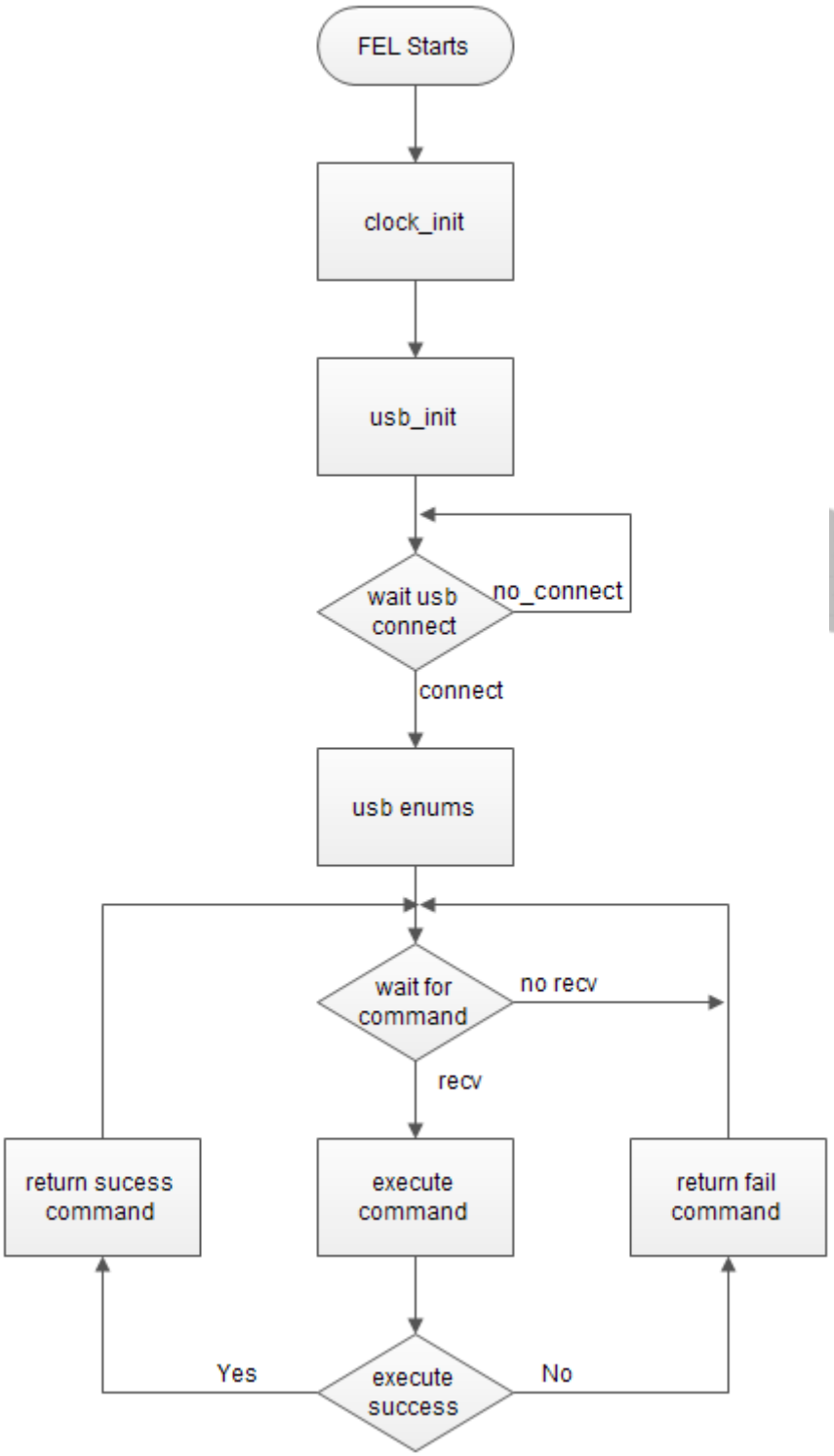
The FEL Address of the BROM is 0x20.

The status of the FEL pin is the bit[8] of the system configuration module (register: 0x03000024).

FEL Process

When the system chooses to enter the Mandatory Upgrade Process, the system will jump to the FEL process. The following figure shows the FEL upgrade process.

Figure 3-10 USB FEL Process

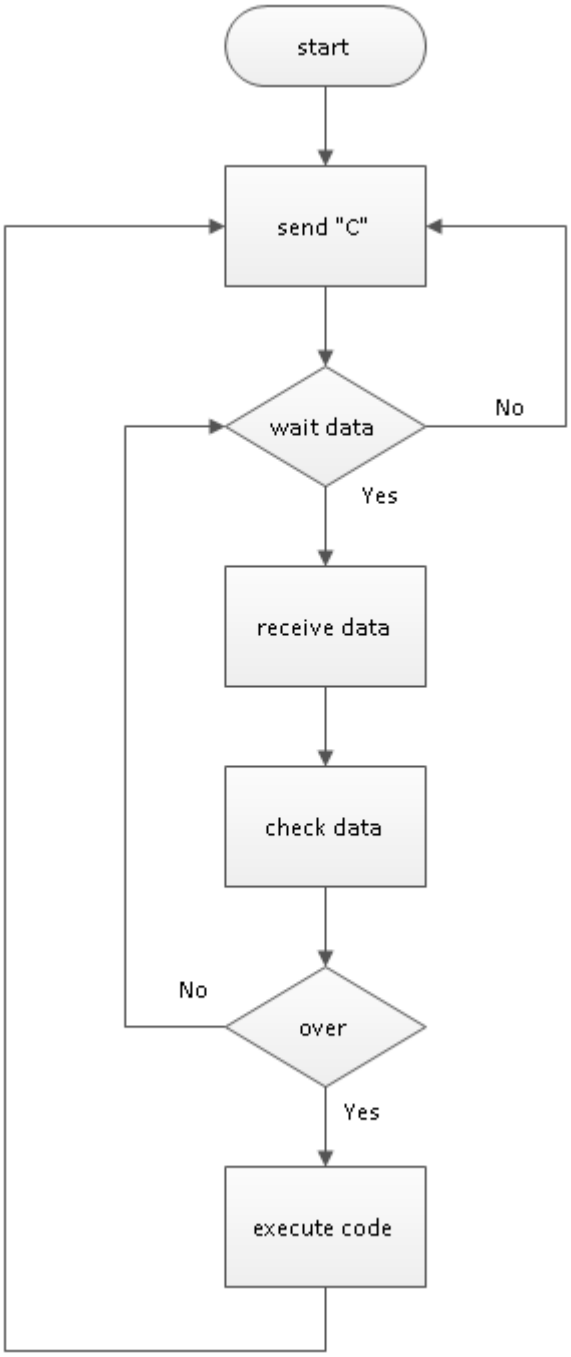


UART Upgrade Process

When the system chooses to enter Mandatory Upgrade Process,if the boot_select2 pin signal is detected to pulled to low level,then the system will jump to the Uart Upgrade Process.

The following figure shows the Uart Upgrade Process:

Figure 3-11 Uart Boot Process Diagram



Fast Boot Process

If the value of the Fast Boot register (0x07090120) in RTC module is not zero, the system will enter the Fast Boot Process. The following table shows the boot medium priority for different values of the Fast Boot register.

Table 3-10 Fast Boot Select Setting

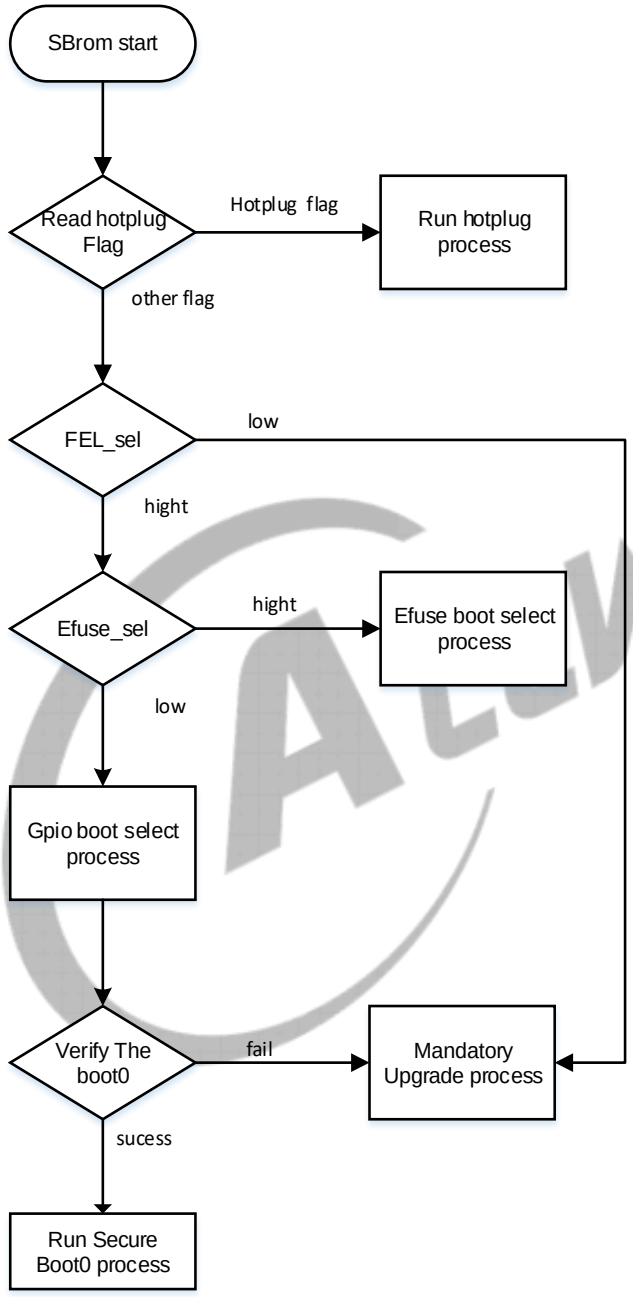
Reg_bit[31:28]	Boot Select type
1	reserve
2	EMMC2_USR->EMMC2_BOOT
3	SPI NOR(1 wire)-> SPI NOR(4 wire)
4	SPI NAND
5	EMMC2_BOOT->EMMC2_USR
6	reserve
7	reserve
8	SPI NOR(4 wire)-> SPI NOR(1 wire)

Secure BROM Mode

In Security boot mode, By comparison with Normal BROM,after the Try Media Boot process finishes, the system will go to run Security BROM software.

The following figure shows the Secure BROM Process:

Figure 3-12 Security BROM Process Diagram



3.6 System Configuration

3.6.1 Overview

The system configuration module is used to configure parameters for system domain, such as SRAM, CPU, PLL, BROM, and so on.

3.7 Timer

3.7.1 Overview

The timer module implements the timing and counting functions. The timer module includes timer0 to time3, watchdog and audio video synchronization (AVS).

The main features for timer0 to timer3 are as follows:

- Alternative count clock: CLK32K or OSC24M
- Supports 8 prescale factors
- Programmable 32-bit down timer
- Supports two timing modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transmit a reset signal to reset the entire system when an exception occurs in the system. The main features for the watchdog are as follows:

- Single clock source: OSC24M/750
- Supports 12 initial values
- Supports the generation of timeout interrupts
- Supports the generation of reset signals
- Supports Watchdog Restart

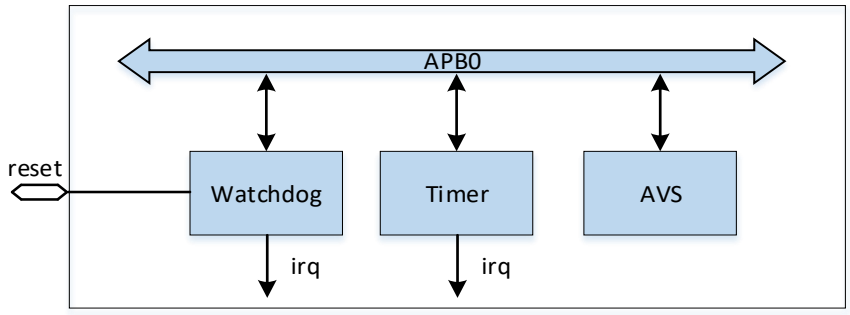
The AVS is used to synchronize the audio and video. The AVS module includes AVS0 and AVS1, which are completely consistent. The main features for the AVS are as follows:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Supports updating the initial value anytime
- 12-bit frequency divider factor
- Supports Pause/Start function

3.7.2 Block Diagram

The following figure shows the functional block diagram of the timer module.

Figure 3-13 Timer Block Diagram



The watchdog, timer (including timer0, timer1, timer2 and timer3), and AVS are all mounted at the APB0 bus. The system configures the parameters of these configure registers via APB0 bus.

The timer and watchdog are both down counters and support generating interrupts after the counting value reaches 0.

For watchdog, the system is responsible for configuring the interval value. If the system fails to restart the watchdog regularly because of some exceptional situations, such as the bus hang, the watchdog will send out a Watchdog Reset External signal to reset the system. And the signal will be transmitted to the Reset pad to reset the PMIC.

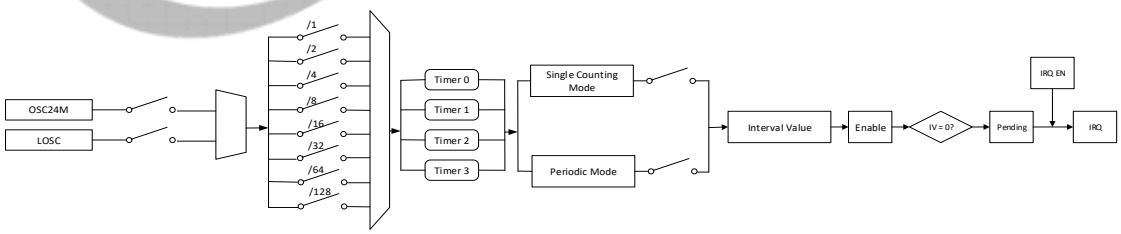
3.7.3 Functional Description

3.7.3.1 Timer

The timer (including timer0, timer1, timer2 and timer3), is a 32-bit down counter. The counter value is decremented by 1 on each rising edge of the timer clock.

The following figure shows the block diagram for the timer.

Figure 3-14 Block Diagram for the Timer



The clock source for the timer can be either OSC24M or CLK32K

Each timer has a prescale that divides the working clock frequency by 1, 2, 4, 8, 16, 32, 64, or 128. And each timer can generate independent interrupts.

Timing Modes

The timer has two timing modes: the single counting mode and periodic mode. You can configure the timing mode via the bit[7] of TMRn_CTRL_REG (n = 0, 1, 2 or 3). The value 0 is for the period mode and value 1 is for the single counting mode.

- Single Counting Mode

In the single counting mode, the timer starts counting from the interval value and generates an interrupt after the counter decreases to 0, and then stops counting. It starts to count again only when a new interval value is loaded.

- Periodic Mode

In the periodic mode, the timer restarts another round of counting after generating the interrupt. It reloads data from the TMRn_INTV_VALUE_REG and then continues to count.

Formula for Calculating the Timer Time

The following formula decribes the relationship among timer parameters.

$$T_{timer} = \frac{TMRn\_INTV\_VALUE\_REG - TMRn\_CUR\_VALUE\_REG}{TMRn\_CLK\_SRC} \times TMRn\_CLK\_PRES$$

Where,

The parameter n is either 0, 1, 2, or 3;

Ttimer is the remaining time of the timer;

TMRn_INTV_VALUE_REG is the interval value of the timer;

TMRn_CUR_VALUE_REG is the current value of the timer;

TMRn_CLK_SRC is the frequency of the timer clock source;

TMRn_CLK_PRES is the prescale ratio of the timer clock.

Initializing the Timer

Follow the steps below to initialize the timer:

1. Configure the timer parameters clock source, prescale factor, and timing mode by writing TMRn_CTRL_REG. There is no sequence requirement of configuring the parameters.
2. Write the interval value.
   a) Write TMRn_INTV_VALUE_REG to configure the interval value for the timer.
   b) Write bit[1] of TMRn_CTRL_REG to load the interval value to the timer. The value of the bit will be cleared automatically after loading the interval value.

3. Write bit[0] of TMRn_CTRL_REG to start the timer. To get the current value of the timer, read TMRn_CUR_VALUE_REG.

Processing the Interrupt

Follow the steps below to process the interrupt:

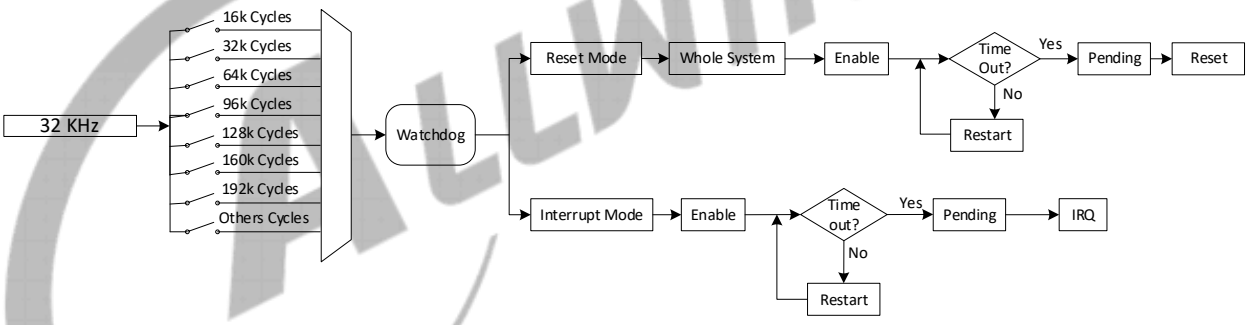
1. Enable interrupts for the timer: write the enable bit of the corresponding interrupt in TMR_IRQ_EN_REG for the timer. The timer will generate an interrupt everytime the count value reaches 0.
2. After entering the interrupt process, write the pending bit of the corresponding interrupt in TMR_IRQ_STA_REG to clear the interrupt pending, and execute the process of waiting for the interrupt.
3. Resume the interrupt and continue to execute the interrupted process.

3.7.3.2 Watchdog

The watchdog is a 32-bit down counter. The counter value is decremented by 1 on each rising edge of the count clock.

The following figure shows the block diagram for the watchdog.

Figure 3-15 Block Diagram for the Watchdog



The clock source of the watchdog is OSC24M/750. There are 12 configurable initial count values.

Operating Modes

The watchdog has two operating modes: the interrupt mode and reset mode.

- In the interrupt mode, when the counter value reaches 0 and WDOG_IRQ_EN_REG is enabled, the watchdog generates an interrupt.
- In the reset mode, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

You can configure the operating mode for the watchdog via the bit[1:0] of the WDOG_CFG_REG. The value 0x2 is for the interrupt mode and the value 0x1 is for the reset mode.

Both the interrupt mode and reset mode support Watchdog Restart. You can make the watchdog to count from the initial value at any time by configuring the WDOG_CTRL_REG: write 0xA57 to bit[12:1], then write 1 to bit[0].

Initializing the Watchdog

Follow the steps below to initialize the watchdog:

1. Write the bit[1:0] of WDOG_CFG_REG to configure the watchdog operating mode so that the watchdog can generate interrupts or output reset signals.
2. Write the bit[7:4] of WDOG_MODE_REG to configure the initial count value.
3. Write the bit[0] of WDOG_MODE_REG to enable the watchdog.

Processing the Interrupt

In the interrupt mode, the watchdog is used as a counter. It generates an interrupt everytime the count value reaches 0.

Follow the steps below to process the interrupt:

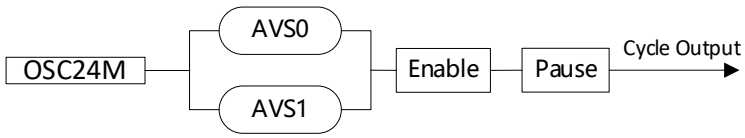
1. Write the enable bit of WDOG_IRQ_EN_REG to enable the interrupt.
2. After entering the interrupt process, write the pending bit of WDOG_IRQ_STA_REG to clear the interrupt pending and execute the process of waiting for the interrupt.
3. Resume the interrupt and continue to execute the interrupted process.

3.7.3.3 AVS

The AVS is a 33-bit up counter. The counter value is increased by 1 on each rising edge of the count clock. There is a clock gate in section 3.4 Clock Controller Unit (CCU) to control the output of the AVS counter. To operate the AVS, open the clock gate first.

The following figure shows the block diagram for the AVS.

Figure 3-16 Block Diagram for the AVS



The clock source of the AVS is OSC24M. There is a 12-bit division factor for each AVS, N0 for AVS0 and N1 for AVS1. When the timer increases from 0 to N1 or N2, the AVS counter adds 1. When the counter reaches 33-bit upper limit, the AVS will start to count from the initial value again.

The AVS supports changing the initial value and division factor at anytime. And the AVS supports restarting from the initial value or pausing at anytime.

Starting or Pausing the AVS

Follow the steps below:

1. Write AVS_CNT_DIV_REG to configure the division factor.
2. Write AVS_CNTn_REG (n = 0 or 1) to configure the initial value.
3. Write AVS_CNT_CTL_REG to enable the AVS. You can pause the AVS at any time.

3.7.4 Programming Guidelines

3.7.4.1 Configuring the Timer

The following example shows how to make a one-millisecond delay with the clock source selected as OSC24M, the operating mode sets as single counting mode, and the pre-scale sets as 2.

```
writel(0x2EE0, TMR_0_INTV);                    //Set the interval value
writel(0x94, TMR_0_CTRL);                      //Select Single mode, 24 MHz clock source, 2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);  //Set the Reload bit
while((readl(TMR_0_CTRL)>>1)&1);               //Waiting the Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);  //Enable Timer0
```

3.7.4.2 Resetting the Watchdog

The following example shows how to make the watchdog to generate a reset signal to the whole system after 1 second. The clock source for the watchdog is OSC24M/750.

```
writel(0x1, WDOG_CONFIG);                      //Set the operating mode as the reset mode.
writel(0x10, WDOG_MODE);                       //Set the interval value as 1 s.
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);    //Enable the Watchdog.
```

3.7.4.3 Restarting the Watchdog

The following example shows how to restart the watchdog. In this example, the clock source is OSC24M/750, the interval value is 1 second, and the watchdog operating mode is the reset mode.

If the execution time of “other codes” is shorter than 1 second, the watchdog will restart from the interval value before it count to zero and generates the reset signal. Otherwise, the watchdog will reset the whole system before the code “writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0), WDOG_CTRL)” is executed.

```
writel(0x1, WDOG_CONFIG);                      //To whole system
```

```
writel(0x10, WDOG_MODE);                          //Interval Value set 1s

writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);       //Enable Watchdog

----other codes---

writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0), WDOG_CTRL); //Write 0xA57 at Key Field and Restart Watchdog
```

3.7.5 Register List

Module Name	Base Address
Timer	0x0205 0000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer IRQ Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
TMR2_CTRL_REG	0x0030	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x0034	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x0038	Timer 2 Current Value Register
TMR3_CTRL_REG	0x0040	Timer 3 Control Register
TMR3_INTV_VALUE_REG	0x0044	Timer 3 Interval Value Register
TMR3_CUR_VALUE_REG	0x0048	Timer 3 Current Value Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_SOFT_RST_REG	0x00A8	Watchdog Software Reset Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register
WDOG_OUTPUT_CFG_REG	0x00BC	Watchdog Output Configuration Register
AVS_CNT_CTL_REG	0x00C0	AVS Counter Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Counter Divisor Register

3.7.6 Register Description

3.7.6.1 0x0000 Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	TMR3_IRQ_EN. Timer 3 Interrupt Enable. 0: disable 1: enable
2	R/W	0x0	TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: disable 1: enable
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: disable 1: enable
0	R/W	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: disable 1: enable

3.7.6.2 0x0004 Timer IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	TMR3_IRQ_PEND. Timer 3 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.
2	R/W1C	0x0	TMR2_IRQ_PEND. Timer 2 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W1C	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.
0	R/W1C	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. 0: No effect 1: Pending, indicates that the interval value of the timer 1 is reached. Write 1 to clear the pending status.

3.7.6.3 0x0010 Timer 0 Control Register (Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Periodic mode. When the interval value of the timer 0 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 0 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the prescale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer0 Clock Source. 00: CLK32K 01: OSC24M 10: / 11: /

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

3.7.6.4 0x0014 Timer 0 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE. Timer 0 Interval Value.

NOTE

Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.5 0x0018 Timer 0 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer0 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.6 0x0020 Timer 1 Control Register (Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Periodic mode. When the interval value of the timer 1 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 1 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the prescale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer1 Clock Source. 00: CLK32K 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

3.7.6.7 0x0024 Timer 1 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value.

NOTE

Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.8 0x0028 Timer 1 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer1 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.9 0x0030 Timer 2 Control Register (Default Value: 0x0000_0004)

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR2_MODE. Timer 2 mode. 0: Periodic mode. When the interval value of the timer 1 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 1 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR2_CLK_PRES. Select the prescale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer2 Clock Source. 00: CLK32K 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR2_EN. Timer 2 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

3.7.6.10 0x0034 Timer 2 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TMR2_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_INTV_VALUE. Timer 2 Interval Value.

NOTE

Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.11 0x0038 Timer 2 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name:TMR2_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_CUR_VALUE. Timer2 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.12 0x0040 Timer 3 Control Register (Default Value: 0x0000_0004)

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR3_MODE. Timer 3 mode. 0: Periodic mode. When the interval value of the timer 1 is reached, the timer will restart another round of counting automatically. 1: Single counting mode. When the interval value of the timer 1 is reached, the timer will stop counting.
6:4	R/W	0x0	TMR3_CLK_PRES. Select the prescale of timer 3 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR3_CLK_SRC. Timer3 Clock Source. 00: CLK32K 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR3_RELOAD. Timer 3 Reload. 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it's cleared automatically.

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR3_EN. Timer 3 Enable. 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start to down-count from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the single counting mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

3.7.6.13 0x0044 Timer 3 Interval Value Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: TMR3_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR3_INTV_VALUE. Timer 3 Interval Value.

NOTE

Take the system clock and timer clock source into consideration when setting the interval value.

3.7.6.14 0x0048 Timer 3 Current Value Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name:TMR3_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR3_CUR_VALUE. Timer3 current value is a 32-bit down-counter (from interval value to 0).

3.7.6.15 0x00A0 Watchdog IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: WDOG_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: disable 1: enable.

3.7.6.16 0x00A4 Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: WDOG_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ_PEND. Watchdog IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, indicates that the interval value of the watchdog is reached.

3.7.6.17 0x00A8 Watchdog Software Reset Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: WDOG_SOFT_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field To change the value of bit[0], this field should be filled with 0x16AA.
15:1	/	/	/
0	R/W1C	0x0	Soft Reset Enable 0: De-assert 1: Reset the system **Note: To use the bit to reset the system, the watchdog first needs to be disabled.**

3.7.6.18 0x00B0 Watchdog Control Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/

Offset: 0x00B0			Register Name: WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12:1	W	0x0	WDOG_KEY_FIELD Watchdog Key Field It should be written to 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART Watchdog Restart 0: No effect 1: Restart the watchdog

3.7.6.19 0x00B4 Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name: WDOG_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field To change the value of bit[15:0], this field should be filled with 0x16AA.
15:9	/	/	/
8	R/W	0x0	WDOG_CLK_SRC Select the clock source for the watchdog. 0: HOSC_32K, that is, OSC24M/750. It is a 32 KHz clock divided from the OSC24M. 1: CLK32K. A clock provided by It is a 32 KHz clock divided from the internal RC 16MHz.
7:2	/	/	/
1:0	R/W	0x1	WDOG_MODE Configure the operating mode for the watchdog 00: / 01: To whole system 10: Only interrupt mode 11: /

3.7.6.20 0x00B8 Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field To change the value of bit[15:0], this field should be filled with 0x16AA.

Offset: 0x00B8			Register Name: WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE Watchdog Interval Value 0000: 16000 cycles (0.5 s) 0001: 32000 cycles (1 s) 0010: 64000 cycles (2 s) 0011: 96000 cycles (3 s) 0100: 128000 cycles (4 s) 0101: 160000 cycles (5 s) 0110: 192000 cycles (6 s) 0111: 256000 cycles (8 s) 1000: 320000 cycles (10 s) 1001: 384000 cycles (12 s) 1010: 448000 cycles (14 s) 1011: 512000 cycles (16 s) Others: Reserved **Note: The corresponding clock cycles for the interval value (IV) depends on the frequency of the clock: Cycles = F_{CLK} * IV.** For example, to get a interval value of 0.5 second, if the clock source is HOSC_32K (whose frequency is 32 KHz), the cycle number is 16,000; if the clock source is CLK32K (whose frequency is 32.768 kHz), the cycle number is 16,384.
3:1	/	/	/
0	R/W	0x0	WDOG_EN Watchdog Enable 0: No effect 1: Enable the Watchdog

3.7.6.21 0x00BC Watchdog Output Configuration Register (Default Value: 0x0000_001F)

Offset: 0x00BC			Register Name: WDOG_OUTPUT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x1F	WDOG OUTPUT CONFIG Configure the valid time for the watchdog reset signal. T = 1/32ms*(N + 1) The default value is 1 ms.

3.7.6.22 0x00C0 AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Do not pause. 1: Pause the AVS counter1.
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Do not pause. 1: Pause the AVS counter0.
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/Disable The clock source is OSC24M. 0: Disabled 1: Enabled
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 0 Enable/Disable The clock source is OSC24M. 0: Disabled 1: Enabled

3.7.6.23 0x00C4 AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0 The higher 32 bits of AVS counter0. AVS counter0 is a 33-bit up counter. The initial value consists of two parts: this register forms the bit[32:1] of AVS counter0 and the bit[0] is zero. You can set the initial value of the AVS counter0 by software. The initial value can be updated at anytime. You can also pasuse the counter by setting AVS_CNT0_PS to ”1”. The counter value will not increase when it is paused.

3.7.6.24 0x00C8 AVS Counter 1 Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1 The higher 32 bits of AVS counter1. AVS counter1 is a 33-bit up counter. The initial value consists of two parts: this register forms the bit[32:1] of AVS counter0 and the bit[0] is zero. You can set the initial value of the AVS counter1 by software. The initial value can be updated at anytime. You can also pasuse the counter by setting AVS_CNT1_PS to ”1”. The counter value will not increase when it is paused.

3.7.6.25 0x00CC AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset: 0x00CC			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D N1, the divisor factor for AVS1. The clock for AVS1 is 24 MHz/N1. N1 = Bit[27:16] + 1. The valid value for N1 is from 1 to 0x7ff. There is an internal 12-bit counter maintained by the engine of the 33-bit AVS1. The 12-bit counter is used for counting the cycle number of the clock OSC24M. When the value of the 12-bit counter reaches N1, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. You can change the value of N1 via the software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D N0, the divisor factor for AVS0. The clock for AVS0 is 24MHz/N0. N0 = Bit[11:0] + 1. The valid value for N0 is from 1 to 0x7ff. There is an internal 12-bit counter maintained by the engine of the 33-bit AVS0. The 12-bit counter is used for counting the cycle number of the clock OSC24M. When the value of the 12-bit counter reaches N0, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. You can change the value of N0 via the software at any time.

3.8 High Speed Timer

3.8.1 Overview

The high speed timer (HSTimer) module implements more precise timing and counting functions.

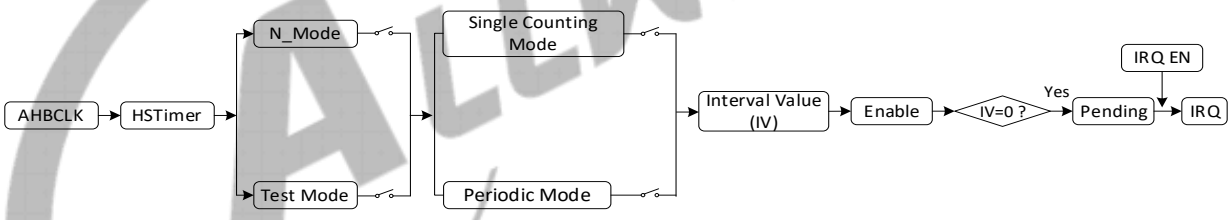
The HSTimer has the following features:

- Single clock source: AHB0
- Supports 5 prescale factors
- Configurable 56-bit down timer
- Supports 2 timing modes: periodic mode and one-shot mode
- Supports the test mode
- Generates an interrupt when the count is decreased to 0

3.8.2 Block Diagram

The following figure shows the block diagram of the HSTimer.

Figure 3-17 HSTimer Block Diagram



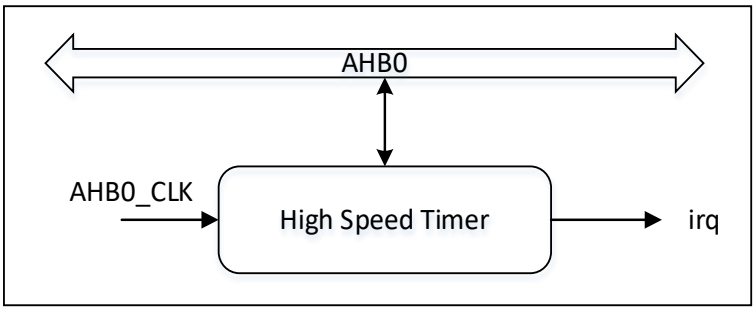
3.8.3 Functional Description

The HSTimers are 56-bit down counters. The counter value is decremented by 1 on each rising edge of the count clock. Each HSTimer has a prescaler that divides the working clock frequency of each working timer by 1, 2, 4, 8, or 16.

3.8.3.1 Typical Application

The following figure shows a typical application of HSTimer module.

Figure 3-18 Typical Application for HSTimer



The HSTimer module is mounted at AHB0, and can control the registers via AHB0. AHB0 is the clock source of the HSTimer. When the count value reaches zero, the HSTimer generates an interrupt.

3.8.3.2 Count Modes

The HSTimer has two count modes: one-shot mode and periodic mode. You can configure the timing mode via the bit[7] of HS_TMRn_CTRL_REG (n = 0 or 1). The value 0 is for the period mode and value 1 is for the one-shot mode.

- One-shot Mode

  When the count value of the HSTimer reaches 0, the HSTimer stops counting. The HSTimer starts to count again only when a new value is loaded.

- Periodic Mode

  The HSTimer counts continuously. When the count value of the HSTimer reaches 0, the HSTimer reloads an initial value from HS_TMRn_INTV_LO_REG and HS_TMRn_INTV_HI_REG and then continues to count.

3.8.3.3 Operating Modes

The HSTimer has two operating modes: the normal mode and test mode. You can configure the operating mode via the bit[31] of HS_TMRn_CTRL_REG. The value 0 is for the normal mode and value 1 is for the test mode.

- Normal Mode

  In the normal mode, the HSTimer is used as a 56-bit down counter, which can finish one-shot counting and periodic counting. The interval value for the HSTimer consists of two parts: HS_TMRn_INTV_LO_REG forms the bit[31:0] and HS_TMRn_INTV_HI_REG forms the bit[55:32]. To read or write the interval value, HS_TMRn_INTV_LO_REG should be done before HS_TMRn_INTV_HI_REG.

- Test Mode

  In the test mode, the HSTimer is used as a 24-bit down counter. HS_TMRn_INTV_LO_REG must be set to 0x1, and HS_TMRn_INTV_HI_REG acts as the initial value for the HSTimer.

3.8.3.4 HSTimer Formula

The following formula describes the relationship among HSTimer parameters in the normal mode.

$$T_{HSTimer} = \frac{(HS\_TMRn\_INTV\_HI\_REG<<32 + HS\_TMRn\_INTV\_LO\_REG) - (HS\_TMRn\_CURNT\_HI\_REG<<32 + HS\_TMRn\_CURNT\_LO\_REG)}{AHB0CLK} \times HS\_TMRn\_CLK$$

Where,

The parameter n is either 0 or 1;

$T_{HSTimer}$ is the remaining time of the timer;

HS_TMRn_INTV_HI_REG is bit[55:32] of the HSTimer interval value;

HS_TMRn_INTV_LO_REG is bit[31:0] of the HSTimer interval value;

HS_TMRn_CURNT_HI_REG is bit[55:32] of the HSTimer current value;

HS_TMRn_CURNT_LO_REG is bit[31:0] of the HSTimer current value;

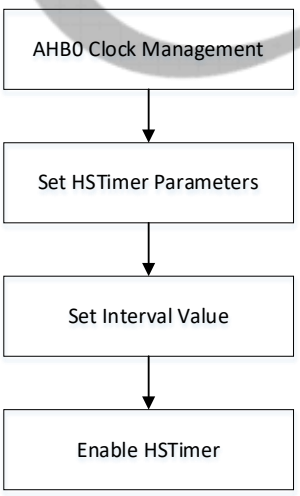
AHB0CLK is the frequency of AHB0 Clock (the HSTimer clock source);

HS_TMRn_CLK is the prescale ratio of the HSTimer clock.

3.8.3.5 Initializing the HSTimer

The following figure shows the process of HSTimer initialization.

Figure 3-19 HSTimer Initialization Process



1. AHB0 clock management: Open the clock gate of AHB0 and de-assert the soft reset of AHB0 in CCU.

2. Configure the corresponding parameters of the HSTimer: clock source, prescaler factor, operating mode, and timing mode. There is no sequence requirement when writing the above parameters to HS_TMRn_CTRL_REG.
3. Write the initial value: Write the lower 32 bits of the initial value to HS_TMRn_INTV_LO_REG first, and then the higher 24 bits to HS_TMRn_INTV_HI_REG. Normally, write the bit[1] of HS_TMRn_CTRL_REG to load the initial value. If the HSTimer is in the timing stop stage, write 1 to the bit[1] and bit[0] of HS_TMRn_CTRL_REG at the same time to reload the initial value.
4. Enable HSTimer: Write the bit[0] of HS_TMRn_CTRL_REG to enable HSTimer to count.
5. Reading HS_TMRn_CURNT_LO_REG and HS_TMRn_CURNT_HI_REG can get current counting value.

3.8.3.6 Processing the HSTimer Interrupt

Follow the steps below to process the HSTimer interrupt:

1. Enable interrupt: Write the corresponding interrupt enable bit of HS_TMR_IRQ_EN_REG, when the counting time of HSTimer reaches, the corresponding interrupt generates.
2. After entering the interrupt process, write HS_TMR_IRQ_STAS_REG to clear the interrupt pending.
3. Resume the interrupt and continue to execute the interrupted process.

3.8.3.7 Programming Guidelines

The following example shows how to make a 1 us delay with HSTimer0. The frequency of the AHB0 clock is 100 MHz, the operating mode is the normal mode, the timing mode is single counting mode, and the pre-scale is 2.

```
writel(0x32, HS_TMR0_INTV_LO);                  //Set bit[31:0] of the interval value as 0x32.
writel(0x0, HS_TMR0_INTV_HI);                   //Set bit[55:32] of the interval value as 0x0.
writel(0x90, HS_TMR0_CTRL);
//Set the operating mode as Normal Mode, the pre-scale as 2, and the timing mode as Single Counting Mode.
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL);   //Set the reload bit.
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL);   //Enable HSTimer0.
while(!(readl(HS_TMR_IRQ_STAS)&1));             //Wait for HSTimer0 to generate pending.
writel(1, HS_TMR_IRQ_STAS);                     //Clear HSTimer0 pending.
```

3.8.4 Register List

Module Name	Base Address
HSTIMER	0x0300 8000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer IRQ Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0040	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0044	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0048	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x004C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0050	HS Timer 1 Current Value High Register

3.8.5 Register Description

3.8.5.1 0x0000 HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	HS_TMR1_INT_EN HSTimer1 Interrupt Enable 0: Disabled 1: Enabled
0	R/W	0x0	HS_TMR0_INT_EN HSTimer0 Interrupt Enable 0: Disabled 1: Enabled

3.8.5.2 0x0004 HS Timer IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	HS_TMR1_IRQ_PEND HSTimer1 IRQ Pending The IRQ pending bit for HSTimer1. Write 1 to clear the pending status. 0: No effect 1: Pending, indicates that the initial value of the HSTimer is reached.

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W1C	0x0	HS_TMR0_IRQ_PEND HSTimer0 IRQ Pending The IRQ pending bit for HSTimer0. Write 1 to clear the pending status. 0: No effect 1: Pending, indicates that the initial value of the HSTimer is reached.

3.8.5.3 0x0020 HS Timer0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST Select the operating mode for HSTimer0 0: Normal mode 1: Test mode In the test mode, the **HS_TMR0_INTV_LO_REG** must be set to 0x1, and **HS_TMR0_INTV_HI_REG** acts as the initial value for HSTimer0.
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE Select the timing mode for HSTimer0 0: Periodic mode. When the count value is decreased to 0, the timer will restart another round of counting automatically. 1: One-shot mode. When the count value is decreased to 0, the timer will stop counting.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale for the HSTimer0 clock sources 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR0_RELOAD HSTimer0 Reload 0: No effect 1: Reload the interval value of the HSTimer0

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	HS_TMR0_EN HSTimer0 Enable 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the one-shot mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

3.8.5.4 0x0024 HS Timer0 Interval Value Low Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HS_TMR0_INTV_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO Bit[31:0] of the HSTimer0 interval value.

3.8.5.5 0x0028 HS Timer0 Interval Value High Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: HS_TMR0_INTV_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI Bit[55:32] of the HSTimer0 interval value.

NOTE

HSTimer0 is a 56-bit counter. The interval value consists of two parts: HS_TMR0_INTV_VALUE_LO acts as the bit[31:0] and HS_TMR0_INTV_VALUE_HI acts as the bit[55:32]. To read or write the interval value, HS_TMR0_INTV_LO_REG should be done before HS_TMR0_INTV_HI_REG.

3.8.5.6 0x002C HS Timer0 Current Value Low Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO Bit[31:0] of the HSTimer0 current value.

3.8.5.7 0x0030 HS Timer0 Current Value High Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI Bit[55:32] of the HSTimer0 current value.

NOTE

HSTimer0 is a 56-bit counter. The current value consists of two parts: HS_TMR0_CUR_VALUE_LO acts as the bit[31:0] and HS_TMR0_CUR_VALUE_HI acts as the bit[55:32]. To read or write the current value, HS_TMR0_CUR_VALUE_LO should be done before HS_TMR0_CUR_VALUE_HI.

3.8.5.8 0x0040 HS Timer1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR1_TEST Select the operating mode for HSTimer1. 0: Normal mode 1: Test mode In the test mode, the **HS_TMR1_INTV_LO_REG** must be set to 0x1, and **HS_TMR1_INTV_HI_REG** acts as the interval value for HSTimer1.
30:8	/	/	/

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	HS_TMR1_MODE Select the timing mode for HSTimer1. 0: Periodic mode. When the count value is decreased to 0, the timer will restart another round of counting automatically. 1: One-shot mode. When the count value is decreased to 0, the timer will stop counting.
6:4	R/W	0x0	HS_TMR1_CLK Select the pre-scale of the HSTimer1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR1_RELOAD HSTimer1 Reload 0: No effect 1: Reload the HSTimer1 interval value.
0	R/W	0x0	HS_TMR1_EN HSTimer1 Enable 0: Stop/Pause 1: Start By setting the bit to 1, the timer will be started. It reloads the interval value register and then counts from the interval value to 0. By setting the bit to 0 before the timer counts to 0, the timer will be paused. The bit will be locked to 0 for at least 2 cycles. Within the 2 cycles, you cannot set the bit to 1 to restart the timer. The timer supports updating the interval value in the pause state. To start from the updated interval value, set both the reload bit and enable bit to 1. Additionally, in the one-shot mode, after the count value reaches 0, the system will automatically change the bit to 0 to stop the timer.

3.8.5.9 0x0044 HS Timer1 Interval Value Low Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO Bit[31:0] of the HSTimer1 interval value

3.8.5.10 0x0048 HS Timer1 Interval Value High Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: HS_TMR1_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI Bit[55:32] of the HSTimer1 interval value

NOTE

HSTimer1 is a 56-bit counter. The interval value consists of two parts: HS_TMR1_INTV_VALUE_LO acts as the bit[31:0] and HS_TMR1_INTV_VALUE_HI acts as the bit[55:32]. To read or write the interval value, HS_TMR1_INTV_LO_REG should be done before HS_TMR1_INTV_HI_REG.

3.8.5.11 0x004C HS Timer1 Current Value Low Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO Bit[31:0] of the HSTimer1 current value

3.8.5.12 0x0050 HS Timer1 Current Value Hi Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI Bit[55:32] of the HSTimer1 current value

NOTE

HSTimer1 is a 56-bit counter. The current value consists of two parts: HS_TMR1_CUR_VALUE_LO acts as the bit[31:0] and HS_TMR1_CUR_VALUE_HI acts as the bit[55:32]. To read or write the current value, HS_TMR1_CUR_VALUE_LO should be done before HS_TMR1_CUR_VALUE_HI.

3.9 Generic Interrupt Controller (GIC)

The following table describes the details of interrupt sources.

Table 3-11 Interrupt Sources

Interrupt Number	Interrupt Source	Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	CPUX_MBOX_ CPUX	0x80	CPUX MSGBOX READ IRQ FOR CPUX
33	CPUX _MBOX_RISCV	0x84	CPUX MSGBOX WRITE IRQ FOR RISCV
34	UART0	0x88	
35	UART1	0x8C	

Interrupt Number	Interrupt Source	Vector	Description
36	UART2	0x90	
37	UART3	0x94	
38		0x98	
39		0x9C	
40		0xA0	
41	TWI0	0xA4	
42	TWI1	0xA8	
43	TWI2	0xAC	
44	TWI3	0xB0	
45	TWI4	0xB4	
46		0xB8	
47	SPI0	0xBC	
48	SPI1	0xC0	
49	SPI2	0xC4	
50	PWM	0xC8	
51	SPI_FLASH	0xCC	
52	WIEGAND	0xD0	
53	SPI3	0xD4	
54		0xD8	
55		0xDC	
56	DMIC	0xE0	
57	AUDIO_CODEC	0xE4	
58		0xE8	
59	I2S_PCM1	0xEC	
60		0xF0	
61	USB_OTG	0xF4	
62	USB_EHCI	0xF8	
63	USB_OHCI	0xFC	
64		0x100	
65		0x104	
66		0x108	
67		0x10C	
68		0x110	
69		0x114	
70		0x118	
71		0x11C	
72	SMHC0	0x120	
73	SMHC1	0x124	
74	SMHC2	0x128	
75	MSI	0x12C	
76	SMC	0x130	

Interrupt Number	Interrupt Source	Vector	Description
77		0x134	
78	EMAC	0x138	
79		0x13C	
80	CCU_FERR	0x140	
81	AHB_HREADY_TIME_OUT	0x144	
82	DMA_CPUX_NS	0x148	
83	DMA_ CPUX_S	0x14C	
84	CE_NS	0x150	
85	CE_S	0x154	
86	SPINLOCK	0x158	
87	HSTIMER0	0x15C	
88	HSTIMER1	0x160	
89	GPADC	0x164	
90	THS	0x168	
91	TIMER0	0x16C	
92	TIMER1	0x170	
93	TIMER2	0x174	
94	TIMER3	0x178	
95	WDG	0x17C	
96	IOMMU	0x180	
97	NPU	0x184	
98	VE	0x188	
99	GPIOA_NS	0x18C	
100	GPIOA_S	0x190	
101		0x194	
102		0x198	
103	GPIOC_NS	0x19C	
104	GPIOC_S	0x1A0	
105	GPIOD_NS	0x1A4	
106	GPIOD_S	0x1A8	
107	GPIOE_NS	0x1AC	
108	GPIOE_S	0x1B0	
109	GPIOF_NS	0x1B4	
110	GPIOF_S	0x1B8	
111	GPIOG_NS	0x1BC	
112	GPIOG_S	0x1C0	
113	GPIOH_NS	0x1C4	
114	GPIOH_S	0x1C8	
115	GPIOI_NS	0x1CC	
116	GPIOI_S	0x1D0	
117	DMAC_RISCV_NS	0x1D4	

Interrupt Number	Interrupt Source	Vector	Description
118	DMAC_RISCV_S	0x1D8	
119	DE	0x1DC	
120		0x1E0	
121	G2D	0x1E4	
122	LCD	0x1E8	
123		0x1EC	
124	DSI	0x1F0	
125		0x1F4	
126		0x1F8	
127	CSI_DMA0	0x1FC	
128	CSI_DMA1	0x200	
129	CSI_DMA2	0x204	
130	CSI_DMA3	0x208	
131		0x20C	
132	CSI_PARSER0	0x210	
133	CSI_PARSER1	0x214	
134	CSI_PARSER2	0x218	
135		0x21C	
136	CSI_CMB	0x220	
137	CSI_TDM	0x224	
138	CSI_TOP_PKT	0x228	
139		0x22C	
140	ISP0	0x230	
141	ISP1	0x234	
142	ISP2	0x238	
143	ISP3	0x23C	
144	VIPP0	0x240	
145	VIPP1	0x244	
146	VIPP2	0x248	
147	VIPP3	0x24C	
148		0x250	
149		0x254	
150		0x258	
151		0x25C	
152		0x260	
153		0x264	
154		0x268	
155		0x26C	
156		0x270	
157		0x274	
158		0x278	

Interrupt Number	Interrupt Source	Vector	Description
159		0x27C	
160	RISCV_MBOX_RISCV	0x280	RISCV MSGBOX READ IRQ FOR RISCV
161	RISCV_MBOX_CPUX	0x284	RISCV MSGBOX WRITE IRQ FOR CPUX
162	RISCV_WDG	0x288	
163	RISCV_TIMER0	0x28C	
164	RISCV_TIMER1	0x290	
165	RISCV_TIMER2	0x294	
166	RISCV_TIMER3	0x298	
167		0x29C	
168	NMI	0x2A0	
169	PPU	0x2A4	
170	ALARM	0x2A8	
171	AHBS_HREADY_TIME_OUT	0x2AC	CPUS AHB READY TIME OUT IRQ
172	PMC	0x2B0	
173	GIC_C0	0x2B4	Debug
174	TWD	0x2B8	
175		0x2BC	
176		0x2C0	
177		0x2C4	
178		0x2C8	
179		0x2CC	
180		0x2D0	
181		0x2D4	
182		0x2D8	
183		0x2DC	
184		0x2E0	
185		0x2E4	
186		0x2EC	
187		0x2F0	
188		0x2F4	
189		0x2F8	
190		0x2FC	
191		0x300	
CPUX Related			
192	C0_CTI0	0x304	C0_CTI0 interrupt
193	C0_CTI1	0x308	C0_CTI1 interrupt
194		0x30C	
195		0x310	
196	C0_COMMTX0	0x314	C0_COMMTX0 interrupt
197	C0_COMMTX1	0x318	C0_COMMTX1 interrupt

Interrupt Number	Interrupt Source	Vector	Description
198		0x31C	
199		0x320	
200	C0_COMMRX0	0x324	C0_COMMRX0 interrupt
201	C0_COMMRX1	0x328	C0_COMMRX1 interrupt
202		0x32C	
203		0x330	
204	C0_PMU0	0x334	C0_PMU0 interrupt
205	C0_PMU1	0x338	C0_PMU1 interrupt
206		0x33C	
207		0x340	
208	C0_AXI_ERROR	0x344	C0_AXI_ERROR interrupt
209		0x348	
210	AXI_WR_IRQ	0x34C	
211	AXI_RD_IRQ	0x350	
212	DBGPWRUPREQ_out[0]	0x354	
213	DBGPWRUPREQ_out[1]	0x358	
214		0x35C	
215		0x360	
216		0x364	
217		0x368	
218		0x36C	
219		0x370	
220		0x374	
221		0x378	
222		0x37C	
223		0x380	

3.10 Direct Memory Access Controller (DMAC)

3.10.1 Overview

The direct memory access (DMA) is a method of transferring data between peripherals and memories (including the SRAM and DRAM) without using the CPU. It is an efficient way to offload data transfer duties from the CPU. Without DMA, the CPU has to control all the data transfers. While with DMA, the DMAC directly transfers data between a peripheral and a memory, between peripherals, or between memories.

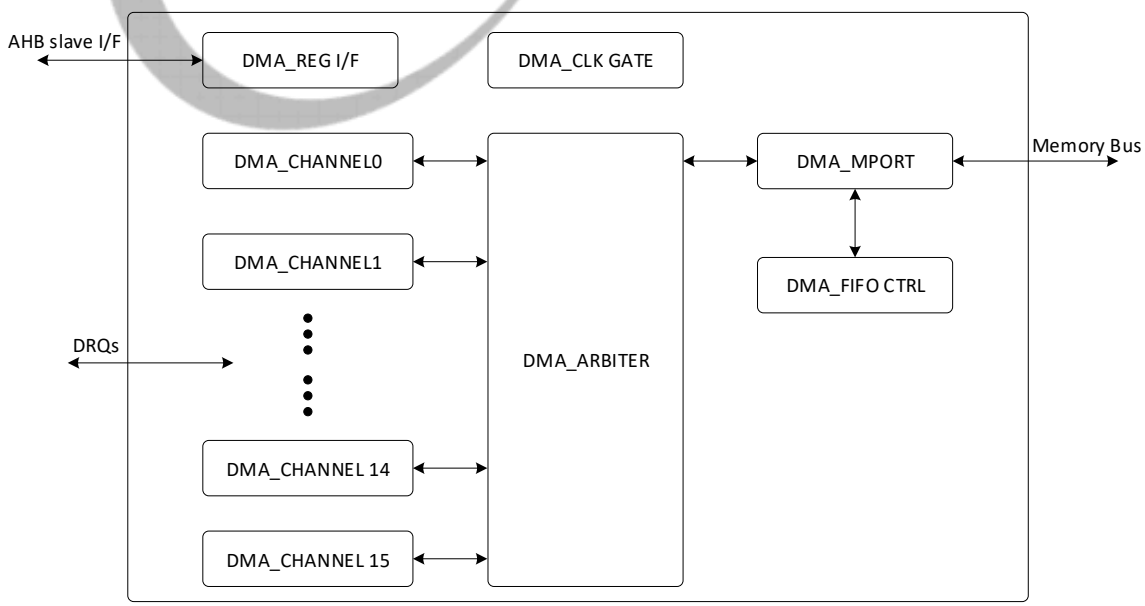
The DMAC has the following features:

- Up to 16 DMA channels
- Provides 32 peripheral DMA requests for data reading and 32 peripheral DMA requests for data writing
- Supports transferring data with a linked list
- Supports programmable 8-bit, 16-bit, 32-bit, and 64-bit data width
- Supports programmable DMA burst length
- DRQ response includes the waiting mode and handshake mode
- DMA channel supports pause function
- Memory devices support non-aligned transform

3.10.2 Block Diagram

The following figure shows a block diagram of DMAC.

Figure 3-20 DMAC Block Diagram



DMAC contains the following sub-blocks:

Table 3-12 DMAC Sub-blocks

Sub-block	Description
DMA_ARBITER	Arbitrates the DMA read/write requests from all channels, and converts the requests to the read/write requests of ports.
DMA_CHANNELs	DMA transfer engine. Each channel is independent. When the DMA requests from multiple peripherals are valid simultaneously, the channel with the highest priority starts data transfer first. The system uses the polling mechanism to decide the priorities of DMA channels. When DMA_ARBITER is idle, channel 0 has the highest priority, whereas channel 15 has the lowest priority. When DMA_ARBITER is busy processing the request from channel n, channel (n+1) has the highest priority. For n = 15, the channel (n + 1) should be channel 0.
DRQs	DMA requests. Peripherals use the DMA request signals to request a data transfer.
DMA_MPORT	Receives the read/write requests from DMA_ARBITER, and converts the requests to the corresponding MBUS access requests. It is mainly used for accessing the DRAM.
DMA_HPORT	The port for accessing the AHB Master. It is mainly used for accessing the SRAM and IO devices.
DMA_FIFO CTRL	Internal FIFO cell control module.
DMA_REG Interface	DMA_REG is the common register module that is mainly used to resolve AHB demands.
DMA_CLKGATE	The control module for hardware auto clock gating.

The DMAC integrates 16 independent DMA channels and each channel has an independent FIFO controller. When the DMA channel starts, the DMAC gets a DMA descriptor from the DMA_DESC_ADDR_REG and uses it as the configuration information for the data transfer of the current DMA package. Then the DMAC can transfer data between the specified devices. After transferring a DMA package, the DMAC judges if the current channel transfer is finished via the linked address in the descriptor. If the linked address shows all the packages are transferred, the DMAC will end the chain transmission and close the channel.

3.10.3 Functional Description

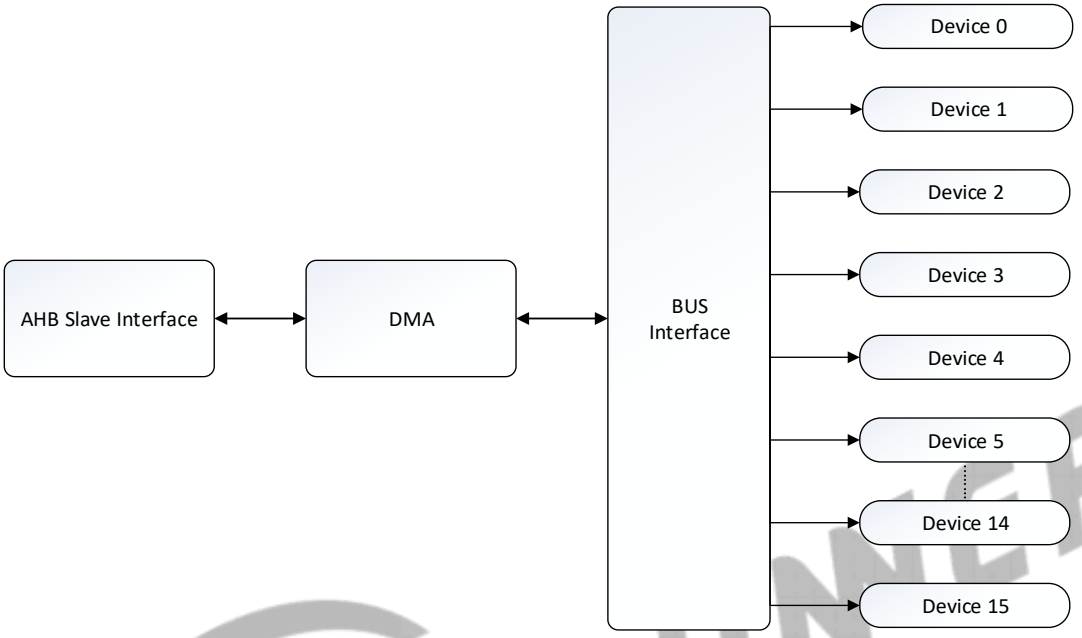
3.10.3.1 Clock

The DMAC is on MBUS. The clock of MBUS influences the transfer efficiency of the DMAC.

3.10.3.2 Typical Application

The following figure shows a typical application of the DMAC.

Figure 3-21 DMAC Typical Application Diagram



3.10.3.3 DRQ Port of Peripherals

The following table shows the source DRQ types and destination DRQ types of different ports.

Table 3-13 DMA DRQ Type

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2		port2	
port3		port3	
port4	I2S1_RX	port4	I2S1_TX
port5		port5	
port6		port6	
port7	AUDIO_CODEC	port7	AUDIO_CODEC
port8	DMIC	port8	
port9		port9	
port10		port10	
port11		port11	
port12	GPADC	Port12	
port13		port13	
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX

Source DRQ Type		Destination DRQ Type	
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX
port18		port18	
port19		port19	
port20		Port20	
port21		port21	
port22	SPI0-RX	port22	SPI0-TX
port23	SPI1-RX	port23	SPI1-TX
port24	SPI2-RX	port24	SPI2-TX
port25	SPI3-RX	port25	SPI3-TX
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	OTG0_EP1	Port30	OTG0_EP1
Port31	OTG0_EP2	Port31	OTG0_EP2
Port32	OTG0_EP3	Port32	OTG0_EP3
Port33	OTG0_EP4	Port33	OTG0_EP4
Port34	OTG0_EP5	Port34	OTG0_EP5
Port35		Port35	
Port36		Port36	
Port37		Port37	
Port38		Port38	
Port39		Port39	
Port40		Port40	
Port41		Port41	
Port42		Port42	
Port43	TWI0	Port43	TWI0
Port44	TWI1	Port44	TWI1
Port45	TWI2	Port45	TWI2
Port46	TWI3	Port46	TWI3
Port47	TWI4	Port47	TWI4
Port48		Port48	
Port49		Port49	
Port50		Port50	
Port51		Port51	
Port52		Port52	
Port53		Port53	

3.10.3.4 DMA Descriptor

The DMAC descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words: Configuration, Source Address, Destination Address, Byte Counter, Parameter, and Link. The following figure shows the structure of the DMA descriptor.

Figure 3-22 DMA Descriptor

1. **Configuration:** Configure the following information by DMA_CFG_REG.

- DRQ type: DRQ type of the source and destination devices.
- Address counting mode: For both the source and destination devices, there are two address counting modes: the IO mode and linear mode. The IO mode is for IO devices whose address is fixed during the data transfer and the linear mode is for the memory whose address is increasing during the data transfer.
- Transferred block length: The amount of data that non-memory peripherals can transfer in a valid DRQ. The block length supports 1 bit, 4 bits, 8 bits, and 16 bits.
- Transferred data width: The data width of operating the non-memory peripherals. The data width supports 8 bits, 16 bits, 32 bits, and 64 bits.

NOTE

The configuration supports BMODE mode. The BMODE is used in the following scenario: the source is an IO device, and the destination is a memory device. Setting the BMODE mode can limit the amount of block data transferred in DMA block transmission to the amount of data transferred when the DRQ threshold of the source IO device is 1. For example,

2. **Source Address:** Configure the address of the source device.
3. **Destination Address:** Configure the address of the destination device.

   DMA reads data from the source address and then writes data to the destination address.

   Both the DMA source and destination addresses have 34 bits. In the descriptor, because there are only 32 bits in the **Source/Destination Address** field, another 2 bits are stored in the **Parameter** field.

The following table shows the details of the related fields in the descriptor.

Table 3-14 Source/Destination Address Distribution

Descriptor Group	Bit	Description
Source Address	31:0	DMA transfers the lower 32 bits of the 34-bit source address
Destination Address	31:0	DMA transfers the lower 32 bits of the 34-bit destination address
Parameter	31:20	Reserved
	19:18	DMA transfers the higher 2 bits of the 34-bit destination address
	17:16	DMA transfers the high 2 bits of the 34-bit source address
	15:8	Reserved
	7:0	Wait Clock Cycles Set the waiting time in DRQ mode
Link	31:2	The address of the next group descriptor, the lower 30 bits of the word address
	1:0	The address of the next group descriptor, the higher 2 bits of the word address

From the above table, you can get:

Real DMA source address (in byte mode) = {Parameter [17:16], Source Address [31:0]};

Real DMA destination address (in byte mode) = {Parameter [19:18], Destination Address [31:0]};

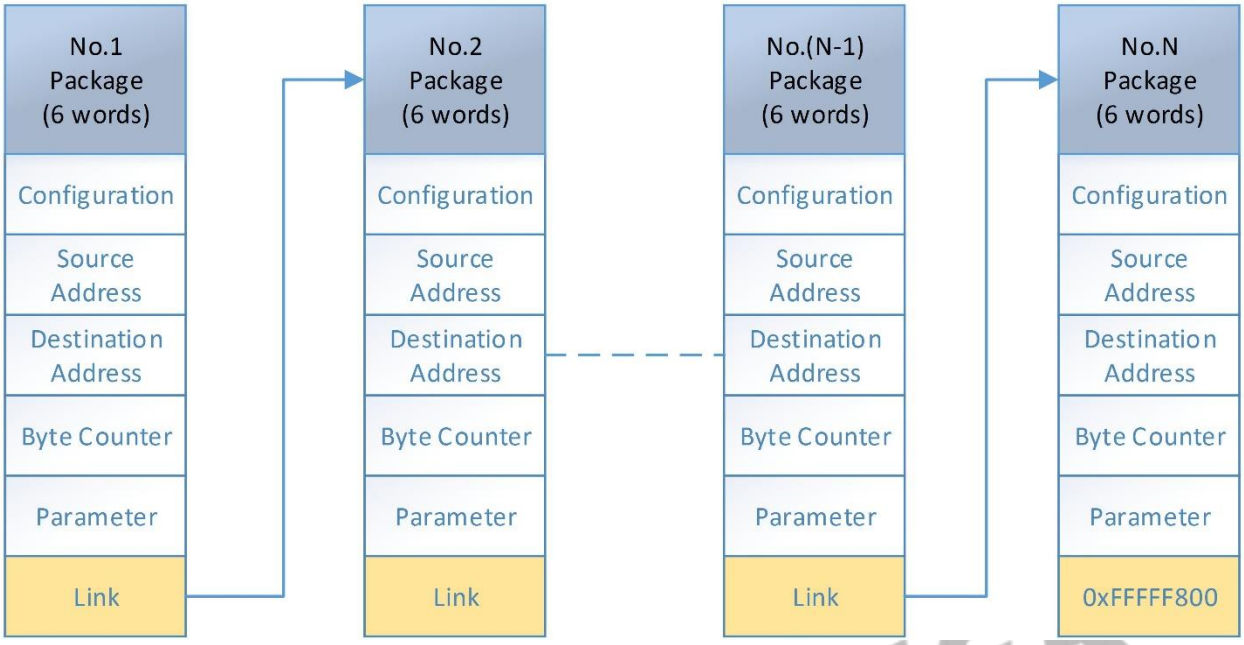
Real link address (in byte mode) = {Link[1:0], Link[31:2], 2'b00}.

4. **Byte counter:** Configure the data amount of a package. The maximum value is (2^25-1) bytes. If the data amount of the package reaches the maximum value, DMA will stop the current transfer even if DRQ is valid.

5. **Parameter:** Configure the interval between the data block. The parameter is valid for the non-memory peripherals. When DMA detects the high DRQ, it transfers the data block and ignores the status changes of the DRQ until the data transfer finishes. After that, DMA waits for certain clock cycles (WAIT_CYC) and executes the next DRQ detection.

6. **Link:** If the link value is 0xFFFFF800, the current package is at the end of the linked list. The DMAC will stop the data transfer after transferring the package; otherwise, the value of the link is considered as the descriptor address of the next package.

Figure 3-23 DMA Chain Transfer



3.10.3.5 Interrupts

There are three kinds of DMA interrupts: the half package interrupt, package end interrupt, and queue end interrupt.

Half package interrupt: When enabled, the DMAC sends out a half package interrupt after transferring half of a package.

Package end interrupt: When enabled, the DMAC sends out a package end interrupt after transferring a complete package.

Queue end interrupt: When enabled, the DMAC sends out a queue end interrupt after transferring a complete queue.

Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts are generated very closely, the later interrupt may override the former one. That is, from the perspective of the CPU, the DMAC has only a system interrupt source.

NOTE

The DMAC has 16 channels and 2 groups of interrupts. The channel [7:0] corresponds to one group of interrupt, the channel [15:8] corresponds to anther group of interrupt.

3.10.3.6 Clock Gating

The DMA_CLK_GATE module is a hardware module for controlling the clock gating automatically. It provides clock sources for sub-modules in DMAC and the module local circuits.

The DMA_CLK_GATE module consists of two parts: the channel clock gate and the common clock gate.

Channel clock gate: Controls the DMA clock of the DMA channels. When the system accesses the register of the current DMA channel and the DMA channel is enabled, the channel clock gate automatically opens the DMA clock. With a 16-HCLK-cycle delay after the system finishes accessing the register or the DMA data transfer is completed, the channel clock gate automatically closes the DMA clock. Also, the clock for the related circuits, such as for the channel control and FIFO control modules, will be closed.

Common clock gate: Controls the clocks of the DMA common circuits. The common circuits include the common circuit of the FIFO control module, MPORT module, and MBUS. When all the DMA channels are enabled, the common clock gate automatically closes the clocks for the above circuits.

The DMA clock gating can support all the functions stated above or not by software.

3.10.3.7 Transfer Mode

DMAC supports two data transfer modes: the waiting mode and the handshake mode.

Waiting Mode

- When DMAC detects a valid external request signal, it starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ pulls low automatically.
- The internal DRQ holds low for certain clock cycles (WAIT_CYC), and then DMAC restarts to detect the external requests. If the external request signal is valid, the next transfer starts.

Handshake Mode

- When DMAC detects a valid external request signal, it starts to operate the peripheral device. The internal DRQ always holds high before the transferred data amount reaches the transferred block length.
- When the transferred data amount reaches the transferred block length, the internal DRQ will be pulled down automatically. For the last data transfer of the block, the DMAC sends a DMA Last signal with the DMA commands to the peripheral device. The DMA Last signal will be packed as a part of the DMA commands and transmitted on the bus. It is used to inform the peripheral device that it is the end of the data transfer for the current DRQ.
- When the peripheral device receives the DMA Last signal, it can judge that the data transfer for the current DRQ is finished. To continue the data transfer, it sends a DMA Active signal to the DMAC.

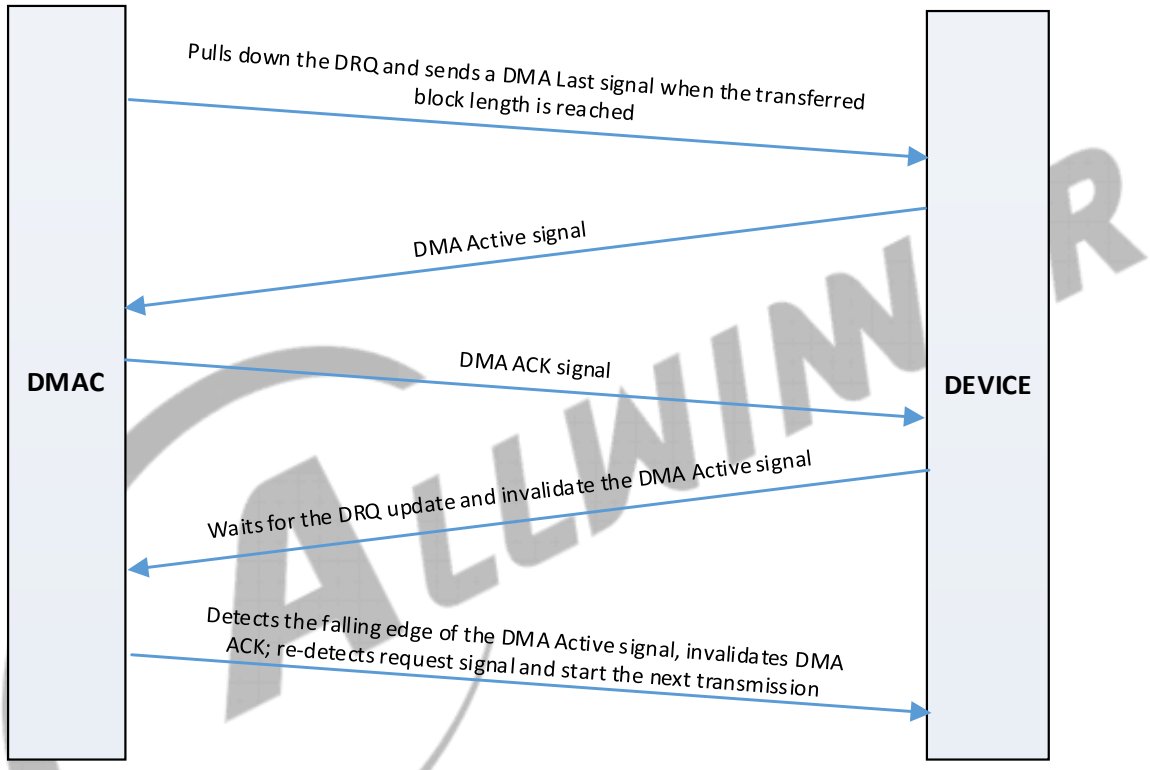
NOTE

One DMA Active signal will be converted to one DRQ signal in the DMA module. To generate multiple DRQs, the peripheral device needs to send out multiple DMA Active signals via the bus protocol.

- When the DMAC received the DMA Active signal, it sends back a DMA ACK signal to the peripheral device.
- When the peripheral device receives the DMA ACK signal, it waits for all the operations on the local device completed, and both the FIFO and DRQ status refreshed. Then it invalidates the DMA Active signal.
- When the DMAC detects the falling edge of the DMA Active signal, it invalidates the corresponding DMA ACK signal, and restarts to detect the external request signals. If a valid request signal is detected, the next data transfer starts.

The following figure shows the workflow of the handshake mode.

Figure 3-24 Workflow of the DMAC Handshake Mode



3.10.3.8 Address Auto-Alignment

For the non-IO devices whose start address is not 32-byte-aligned, the DMAC will adjust the address to 32-byte-aligned through the burst transfer within 32 bytes. Adjusting address to 32-byte-aligned improves the DRAM access efficiency.

The following example shows how the DMAC adjusts the address: when the peripheral device of a DMA channel is a non-IO device whose start address is 0x86 (not 32-byte-aligned), the DMAC firstly uses a 26-byte burst transfer to align the address to 0xA0 (32-byte-aligned), and then transfers data by 64-byte burst (the maximum transfer amount that MBUS allows).

The IO devices do not support address alignment, so the bit width of IO devices must match the address offset; otherwise, the DMAC will ignore the inconsistency and directly transmit data of the corresponding bit width to the address.

The address of the DMA descriptor does not support the address auto-alignment. Make sure the address is word-aligned; otherwise the DMAC cannot identify the descriptor.

3.10.3.9 DMAC Clock Control

- The DMAC clock is synchronous with the AHB0 clock. Make sure that the DMAC gating bit of AHB0 clock is enabled before accessing the DMAC register.
- The reset input signal of the DMAC is asynchronous with AHB0 and is low valid by default. Make sure that the reset signal of the DMAC is de-asserted before accessing the DMA register.
- To avoid the indefinite state within registers, de-assert the reset signal first, and then open the gating bit of AHB0.
- The DMAC supports Clock Auto Gating function to reduce power consumption, the system will automatically disable the DMAC clock in the DMAC idle state. Clock Auto Gating is enabled by default.

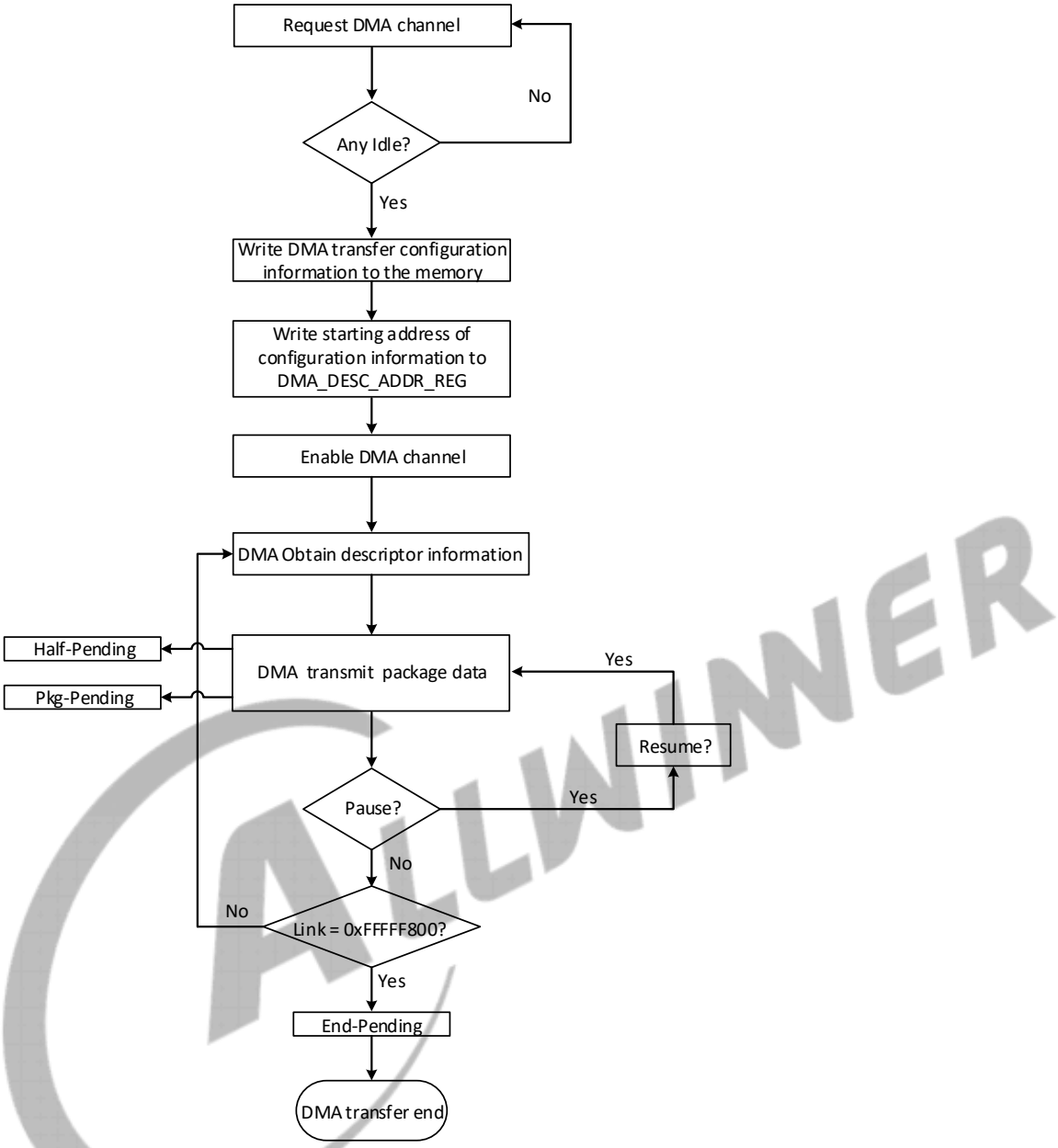
3.10.4 Programming Guidelines

3.10.4.1 Using DMAC Transfer Process

The DMAC transfer process is as follows.

1. Request DMA channel, and check if the DMA channel is idle by checking if it is enabled. A disabled channel indicates it is idle, while an enabled channel indicates it is busy.
2. Write the descriptor with 6 words into the memory. The descriptor must be word-aligned. For more details, refer to section 3.10.3.4 DMA Descriptor
3. Write the start address of the descriptor to DMA_DESC_ADDR_REGN.
4. Enable the DMA channel, and write the corresponding channel to DMAC_EN_REGN.
5. The DMA obtains the descriptor information.
6. Start to transmit a package. When half of the package is completed, the DMA sends a Half Package Transfer Interrupt; when a total package is completed, the DMA sends a Package End Transfer Interrupt. These interrupt status can be read by DMAC_IRQ_PEND_REG0.
7. Set DMAC_PAU_REGN to pause or resume the data transfer.
8. After completing a total package transfer, the DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; otherwise, the next package starts to transmit. When the transfer ends, the DMA sends a Queue End Transfer Interrupt.
9. Disable the DMA channel.

Figure 3-25 DMAC Transfer Process



3.10.4.2 Processing DMAC Interrupt

Follow the steps below to process the DMAC interrupt:

1. Enable interrupt: write the corresponding interrupt enable bit of DMA_IRQ_EN_REG0. The system generates an interrupt when the corresponding condition is satisfied.
2. After entering the interrupt process, write DMA_IRQ_PEND_REG0 to clear the interrupt pending and execute the interrupt process.
3. Resume the interrupt and continue to execute the interrupted process.

3.10.4.3 Configuring DMAC

Refer to the guidelines below to configure the DMAC:

- Make sure the transfer bit width of IO devices is consistent with the offset of the start address.
- The MBUS protocol does not support the read operation of non-integer words. For the devices whose bit width is not word-aligned, after receiving the read command, they should resolve the read command according to their FIFO bit width instead of the command bit width, and ignore the redundant data caused by the inconsistency of the bit width.
- When the DMA transfer is paused, DRQ is invalid. Because there is a certain time delay between DMA transfer commands, the DMAC will not stop data transfer until the DMAC finishes processing the current command and the commands in Arbiter (at most 32-byte data).

DMAC application example:

```
writel(0x00000000, mem_address + 0x00);   //Sets configurations. The mem_address must be word-aligned.
writel(0x00001000, mem_address + 0x04);    // Sets the start address for the source device.
writel(0x20000000, mem_address + 0x08);   //Sets the start address for the destination device.
writel(0x00000020, mem_address + 0x0C);   // Sets the data package size.
writel(0x00000000, mem_address + 0x10);   //Sets the parameters.
writel(0xFFFFF800, mem_address + 0x14);    //Sets the start address for the next descriptor.
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Sets the start address for the DMA channel0 descriptor.
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure that the writing operation is valid.
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);      // Enables DMA channel0 transfer.
```

The DMAC supports increasing data package in the transfer, pay attention to the following points:

- The 0xFFFFF800 value of DMA_FDESC_ADDR_REG indicates that the DMA channel has got back the descriptor of the last package. The DMA channel will automatically stop the data transfer after transferring the current package.
- To add a package during the data transfer, check if the DMA channel has got back the descriptor of the last package. If yes, do not add any package in the current queue. Request another DMA channel with a new DRQ to transfer the package. Otherwise, add the package by modifying the DMA_FDESC_ADDR_REG of the last package from 0xFFFFF800 to the start address of the to-be-added package.

- To ensure that the modification is valid, read the value of DMA_FDESC_ADDR_REG after the modification. The value 0xFFFFF800 indicates the modification failure and other values indicate you have successfully added packages to the queue.
- Another problem is, the system needs some time to process the modification, during which the DMA channel may get back the descriptor of the last package. You can read the value of DMA_CUR_SRC_REG and DMA_CUR_DEST_REG and check whether the increasing memory address is in accordance with the information of the added package. If yes, the package is added successfully; otherwise, the modification failed.
- To ensure a higher rate of success, it is recommended to add the package before the half package interrupt of the penultimate package.

3.10.5 Register List

Module Name	Base Address	Comments
DMA	0x0300 2000	DMA configuration register

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register 1
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Status Register 0
DMA_IRQ_PEND_REG1	0x0014	DMA IRQ Pending Status Register 1
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+0x0000+N*0x0040 (N=0~15)	DMA Channel Enable Register
DMA_PAU_REG	0x0100+0x0004+N*0x0040 (N=0~15)	DMA Channel Pause Register
DMA_DESC_ADDR_REG	0x0100+0x0008+N*0x0040 (N=0~15)	DMA Channel Descriptor Address Register
DMA_CFG_REG	0x0100+0x000C+N*0x0040 (N=0~15)	DMA Channel Configuration Register
DMA_CUR_SRC_REG	0x0100+0x0010+N*0x0040 (N=0~15)	DMA Channel Current Source Address Register
DMA_CUR_DEST_REG	0x0100+0x0014+N*0x0040 (N=0~15)	DMA Channel Current Destination Address Register
DMA_BCNT_LEFT_REG	0x0100+0x0018+N*0x0040 (N=0~15)	DMA Channel Byte Counter Left Register
DMA_PARA_REG	0x0100+0x001C+N*0x0040 (N=0~15)	DMA Channel Parameter Register
DMA_MODE_REG	0x0100+0x0028+N*0x0040 (N=0~15)	DMA Mode Register

Register Name	Offset	Description
DMA_FDESC_ADDR_REG	0x0100+0x002C+N*0x0040 (N=0~15)	DMA Former Descriptor Address Register
DMA_PKG_NUM_REG	0x0100+0x0030+N*0x0040 (N=0~15)	DMA Package Number Register

3.10.6 Register Description

3.10.6.1 0x0000 DMAC IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.6.2 0x0004 DMAC IRQ Enable Register1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
18	R/W	0x0	DMA12_QUEUE_IRQ_EN DMA 12 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA9 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA9 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA9 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.6.3 0x0010 DMAC IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

3.10.6.4 0x0014 DMAC IRQ Pending Status Register 1 (Default Value: 0x0000_0000)

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND. DMA 15 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_PEND DMA 15 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_PEND DMA 14 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
21	R/W1C	0x0	DMA13_PKG_IRQ_PEND DMA 13 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND. DMA 13 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_PEND DMA 12 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_PEND DMA 10 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_PEND DMA 9 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA8 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W1C	0x0	DMA8_PKG_IRQ_PEND DMA 8 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA8 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending

3.10.6.5 0x0028 DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

NOTE

When the DMA Controller is initialized, the bit[2] should be set up.

3.10.6.6 0x0030 DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0	MBUS_FIFO_STATUS MBUS FIFO Status 0: Empty 1: Not Empty
30:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status. 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle 1: Busy

3.10.6.7 0x0100 + N*0x0040 DMAC Channel Enable Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0000+N*0x0040 (N=0~15)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

Offset:0x0100+0x0000+N*0x0040 (N=0~15)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

3.10.6.8 0x0104 + N*0x0040 DMAC Channel Pause Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0004+N*0x0040 (N=0~15)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

3.10.6.9 0x0108 + N*0x0040 DMAC Channel Descriptor Address Register N (Default Value: 0x0000_0000)

Offset: 0x0100+0x0008+N*0x0040 (N = 0 to 15)			Register Name: DMAC_DESC_ADDR_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	R/W	0x0	DMA_DESC_ADDR Lower 30 bits of DMA channel descriptor address The descriptor address must be word-aligned.
1:0	R/W	0x0	DMA_DESC_HIGH_ADDR Higher 2 bits of DMA channel descriptor high address The real address is as follows. DMA Channel Descriptor Address = {bit[1:0], bit[31:2], 2'b00}

3.10.6.10 0x010C + N*0x0040 DMAC Channel Configuration Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x000C+N*0x0040 (N=0~15)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	BMODE_SEL Mode select 0: Normal Mode 1: BMODE

Offset:0x0100+0x000C+N*0x0040 (N=0~15)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
29:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	R	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.10.6.11 0x0110 + N*0x0040 DMAC Channel Current Source Address Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0010+N*0x0040 (N=0~15)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

3.10.6.12 0x0114 + N*0x0040 DMA Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+0x0014+N*0x0040 (N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

3.10.6.13 0x0118 + N*0x0040 DMAC Channel Byte Counter Left Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0018+N*0x0040 (N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

3.10.6.14 0x011C + N*0x0040 DMAC Channel Parameter Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x001C+N*0x0040 (N=0~15)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

3.10.6.15 0x0128 + N*0x0040 DMAC Mode Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0028+N*0x0040 (N=0~15)			Register Name: DMA_MODE_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:4	/	/	/

Offset:0x0100+0x0028+N*0x0040 (N=0~15)			Register Name: DMA_MODE_REG
Bit	**R/W**	**Default/Hex**	**Description**
3	R/W	0x0	DMA_DST_MODE. Destination communication Mode Select 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. Source communication Mode Select 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

3.10.6.16 0x012C + N*0x0040 DMAC Former Descriptor Address Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x002C+N*0x0040 (N=0~15)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to storing the former value of DMA Channel Descriptor Address Register.

3.10.6.17 0x0130 + N*0x0040 DMAC Package Number Register N (Default Value: 0x0000_0000)

Offset:0x0100+0x0030+N*0x0040 (N=0~15)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

3.11 Thermal Sensor Controller (THS)

3.11.1 Overview

The thermal sensors are common elements in wide range of modern system on chips (SoCs) platform. The thermal sensors are used to constantly monitor the temperature on the chip.

The thermal sensor controller (THS) embeds three thermal sensors located in the CPU. When the temperature reaches a certain thermal threshold, the thermal sensor can generate interrupts to the software to lower the temperature via the dynamic voltage and frequency scaling (DVFS) technology.

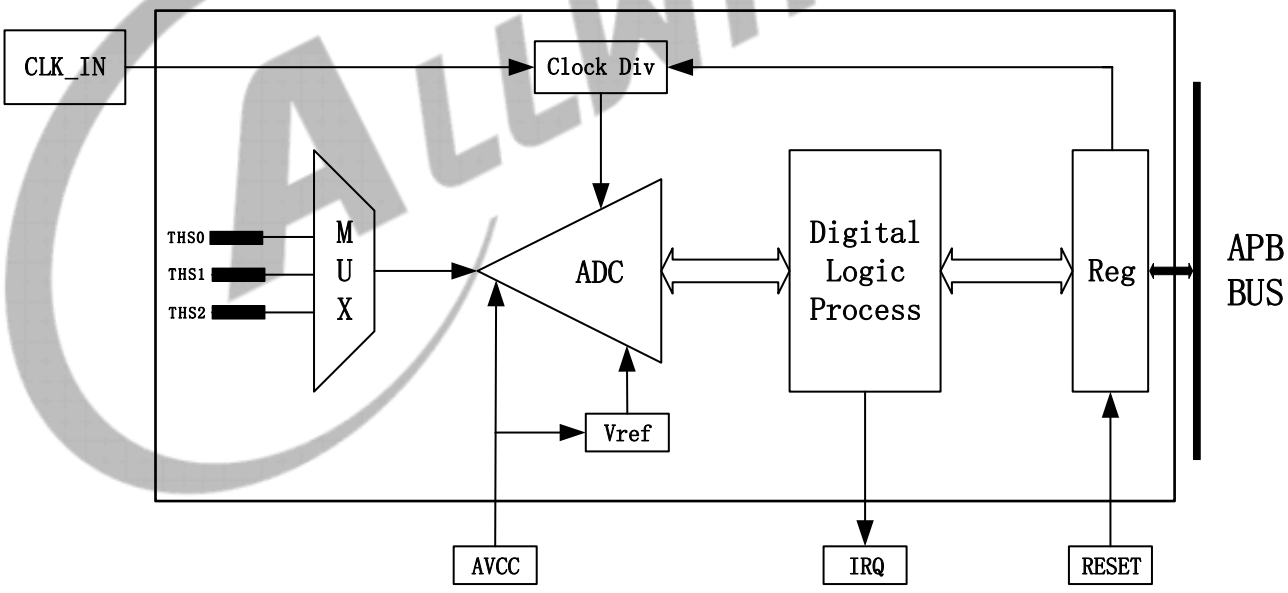
The THS has the following features:

- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.11.2 Block Diagram

The following figure shows a block diagram of the THS.

Figure 3-26 THS Block Diagram



3.11.3 Functional Description

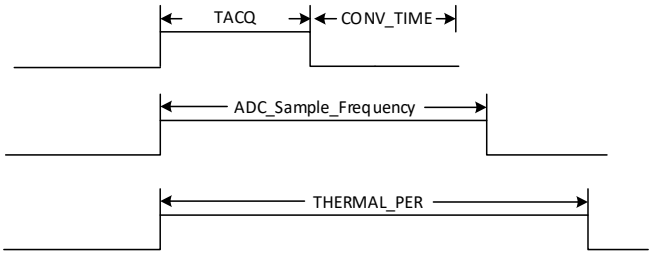
3.11.3.1 Clock Source

The THS gets one clock source: OSC24M. For details about clock configurations, refer to section 3.4 Clock Controller Unit (CCU).

3.11.3.2 Timing Requirements

The following figure shows the timing requirements for the THS.

Figure 3-27 Thermal Sensor Timing Requirement



CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/24 MHz x 14 Cycles = 0.583 us

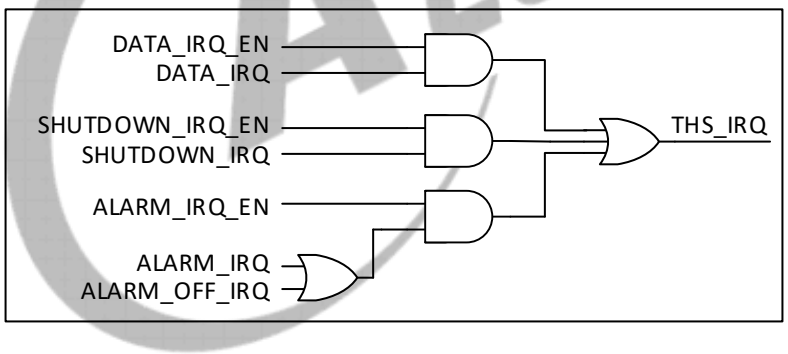
TACQ > 1/24 MHz x 24 Cycles

THERMAL_PER > ADC_Sample_Frequency > TACQ + CONV_TIME

3.11.3.3 Interrupts

The THS has four interrupt sources: DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ, and ALARM_OFF_IRQ. The following figure shows thermal sensor interrupt sources.

Figure 3-28 Thermal Sensor Controller Interrupt Source



DATA_IRQ: The interrupt is generated when the measured sensor_data is updated.

SHUTDOWN_IRQ: The interrupt is generated when the temperature is higher than the shutdown threshold.

ALARM_IRQ: The interrupt is generated when the temperature is higher than the Alarm_Threshold.

ALARM_OFF_IRQ: The interrupt is generated when the temperature drops to lower than the Alarm_Off_Thershold. It is triggered at the fall edge.

3.11.3.4 THS Temperature Conversion Formula

Sensor_data > 1869: T = (sensor_data - 2796)/(-14.26)

Sensor_data $\leqslant$ 1869: T = (sensor_data - 2822)/(-14.60)

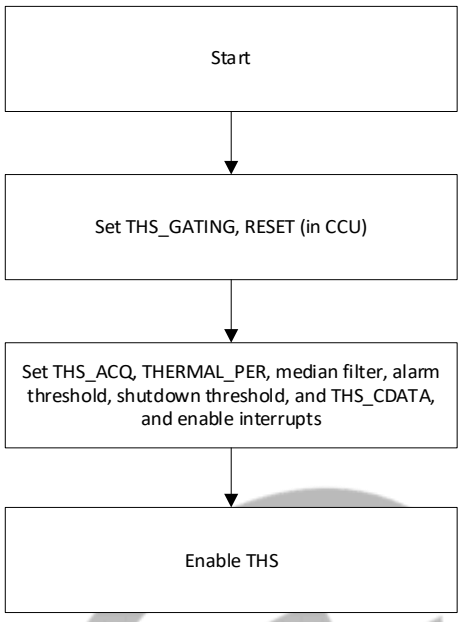
Unit of T: Celsius degree (°C).

The sensor_data is read from the sensor data register.

3.11.4 Programming Guidelines

The initial process of the THS is as follows.

Figure 3-29 THS Initial Process



In the final test (FT) stage, the THS is calibrated through the ambient temperature, and the calibration value is written in the SID module. The following table shows the THS information in the SID.

Table 3-15 THS Information in the SID

Base Address: 0x14	Register Name: THS
Bit	**Description**
31:28	The highest 4 bits of the Audio_bias calibration value.
27:16	The calibration value of the T-sensor.
15:12	The lowest 4 bits of the Audio_bias calibration value.
11:0	The value of the ambient temperature.

Before enabling THS, read eFuse value and write the value to THSn_CDATA (n = 0,1 or 2).

Query Mode

1. Write 0x1 to the bit[16] of THS_BGR_REG to dessert the reset.
2. Write 0x1 to the bit[0] of THS_BGR_REG to open the THS clock.
3. Write 0x2F to the bit[15:0] of THS_CTRL to set the ADC acquire time.
4. Write 0x1DF to the bit[31:16] of THS_CTRL to set the ADC sample frequency divider.
5. Write 0x3A to the bit[31:12] of THS_PER to set the THS work period.

6. Write 0x1 to the bit[2] of THS_FILTER to enable the temperature convert filter.
7. Write 0x1 to the bit[1:0] of THS_FILTER to select the filter type.
8. Read THS eFuse value from SID, then write the eFuse value to THSn_CDATA (n = 0,1 or 2) to calibrate THS.
9. Write 0x1 to the bit[0] of THS_EN to enable THS.
10. Read the bit[0] of THS_DATA_INTS. If it is 1, the temperature conversion is complete.
11. Read the bit[11:0] of THSn_DATA (n = 0,1 or 2), and calculate the THS temperature based on section 3.11.3.4 THS Temperature Conversion Formula

Interrupt Mode

1. Write 0x1 to the bit16 of THS_BGR_REG to dessert the reset.
2. Write 0x1 to the bit0 of THS_BGR_REG to open the THS clock.
3. Write 0x2F to the bit[15:0] of THS_CTRL to set the ADC acquire time.
4. Write 0x1DF to the bit[31:16] of THS_CTRL to set the ADC sample frequency divider.
5. Write 0x3A to the bit[31:12] of THS_PER to set the THS work period.
6. Write 0x1 to the bit2 of THS_FILTER to enable the temperature convert filter.
7. Write 0x1 to the bit[1:0] of THS_FILTER to select the filter type.
8. Read THS eFuse value from SID, and then write the eFuse value to THSn_CDATA (n = 0,1 or 2)) to calibrate THS.
9. Write 0x1 to the bit[0] of THS_DATA_INTC to enable the interrupt of THS.
10. Set interrupt based on PLIC module.
11. Put the interrupt handler address into the interrupt vector table.
12. Write 0x1 to the bit[0] of THS_EN to enable THS.
13. Read the bit[0] of THS_DATA_INTS. If it is 1, the temperature conversion is complete.
14. Read the bit[11:0] of THSn_DATA (n = 0,1 or 2), and calculate the THS temperature based on section 3.11.3.4 THS Temperature Conversion Formula

3.11.5 Register List

Module Name	Base Address
THS	0x02009400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register

Register Name	Offset	Description
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
THS0_ALARM_CTRL	0x0040	THS0 Alarm threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm threshold Control Register
THS0&THS1_SHUTDOWN_CTRL	0x0080	THS0 & TH1 Shutdown threshold Control Register
THS2_SHUTDOWN_CTRL	0x0084	THS2 Shutdown threshold Control Register
THS0&THS1_CDATA	0x00A0	THS0 & THS1 Calibration Data
THS2_CDATA	0x00A4	THS2 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register

3.11.6 Register Description

3.11.6.1 0x0000 THS Control Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: THS_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x1DF	TACQ ADC acquire time CLK_IN/(n + 1) The default value is 2 us.
15:0	R/W	0x2F	Reserved

3.11.6.2 0x0004 THS Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0:Disable 1:Enable

Offset: 0x0004			Register Name: THS_EN
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	THS1_EN Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_EN Enable temperature measurement sensor0 0:Disable 1:Enable

3.11.6.3 0x0008 THS Period Control Register (Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x3A	THERMAL_PER Temperature measurement period 4096*(n + 1)/CLK_IN The default value is 10 ms.
11:0	/	/	/

3.11.6.4 0x0010 THS Data Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	THS2_DATA_IRQ_EN Selects Temperature measurement data of sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects Temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects Temperature measurement data of sensor0 0:Disable 1:Enable

3.11.6.5 0x0014 THS Shut Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.11.6.6 0x0018 THS Alarm Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS_ALARM_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ALARM_INT2_EN Selects Alarm interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects Alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects Alarm interrupt for sensor0 0:Disable 1:Enable

3.11.6.7 0x0020 THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	THS2_DATA_IRQ_STS Data interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ_STS Data interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ_STS Data interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.8 0x0024 THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.9 0x0028 THS Alarm off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS_ALARMO_INTS
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	ALARM_OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

3.11.6.10 0x002C THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

3.11.6.11 0x0030 Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter enable 0: Disabled 1: Enabled
1:0	R/W	0x1	FILTER_TYPE Averaging filter type 00: 2 01: 4 10: 8 11: 16

3.11.6.12 0x0040 THS0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal sensor0 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal sensor0 Alarm threshold for hysteresis temperature

3.11.6.13 0x0044 THS1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal sensor1 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal sensor1 Alarm threshold for hysteresis temperature

3.11.6.14 0x0048 THS2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: THS2_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal sensor2 Alarm Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal sensor2 Alarm threshold for hysteresis temperature

3.11.6.15 0x0080 THS0 & THS1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: THS0&THS1_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal sensor1 Shutdown Threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal sensor0 Shutdown Threshold for hot temperature

3.11.6.16 0x0084 THS2 Shutdown Threshold Control Register (Default Value: 0x0000_04E9)

Offset: 0x0084			Register Name: THS2_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal sensor2 Shutdown Threshold for hot temperature

3.11.6.17 0x00A0 THS0 & THS1 Calibration Data (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS0&THS1_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

3.11.6.18 0x00A4 THS2 Calibration Data (Default Value: 0x0000_0800)

Offset: 0x00A4			Register Name: THS2_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

3.11.6.19 0x00C0 THS0 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
32:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

3.11.6.20 0x00C4 THS1 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

3.11.6.21 0x00C8 THS2 Data Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: THS2_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

3.12 Spinlock

3.12.1 Overview

The spinlock provides a hardware synchronization mechanism in multi-core systems. With the lock operation, the spinlock prevents multiple processors from handling the sharing data simultaneously and thus ensure the coherence of data.

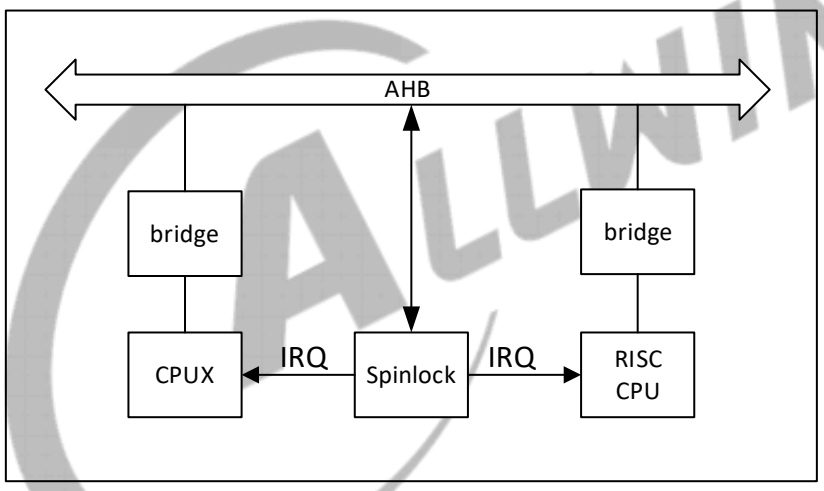
The spinlock has the following features:

- Supports 32 lock units
- wo kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

3.12.2 Block Diagram

The following figure shows the block diagram of the spinlock.

Figure 3-30 Spinlock Block Diagram



3.12.3 Functional Descriptions

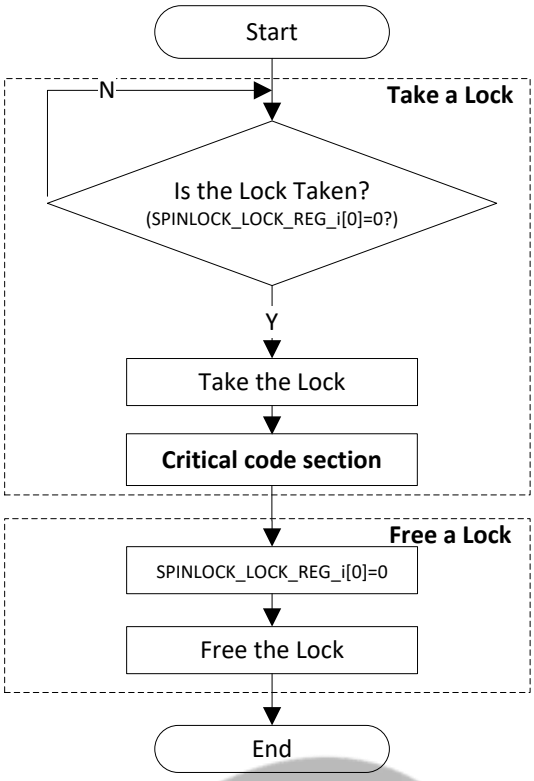
3.12.3.1 Clock and Reset

The spinlock is on AHB. Before accessing the spinlock registers, you need to de-assert the reset signal and then open the corresponding gating signal on AHB.

3.12.3.2 Typical Application

The following figure shows a typical application of the spinlock. A processor locks spinlock0 before executing specific codes, and then unlocks the codes. After the lock is freed, other processors can read or write the data.

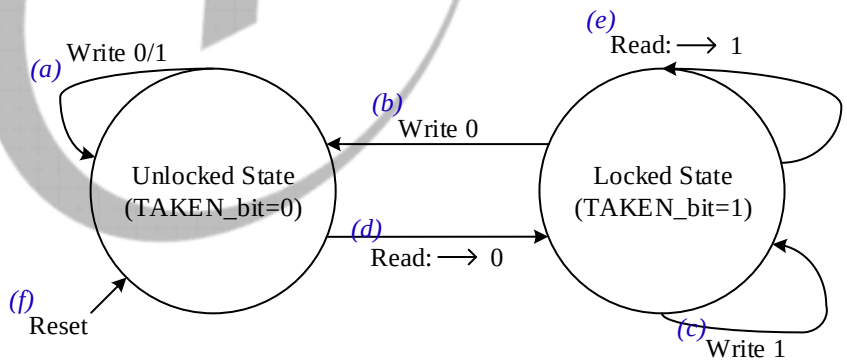
Figure 3-31 Spinlock Typical Application Diagram



3.12.3.3 Spinlock State Machine

When a processor uses spinlock, it needs to acquire the spinlock status through SPINLOCK_STATUS_REG. The following figure shows the spinlock state machine.

Figure 3-32 Spinlock State Machine



1. When spinlock is in the Unlocked state, writing 0/1 has no effect;
2. When spinlock is in the Locked state, writing 0 can convert the corresponding spinlock to the Unlocked state;
3. When spinlock is in the Locked state, writing 1 has no effect;
4. When spinlock is in the Unlocked state, reading the bit can return 0 (it indicates spinlock enters into the Locked state);

5. When spinlock is in the Locked state, reading the bit can return 1 (it indicates spinlock is in the Locked state);
6. After resetting, spinlock is in the Unlock state by default.

3.12.4 Programming Guidelines

3.12.4.1 Switching the Status

Follow the steps below to switch the lock status of a spinlock.

1. When the read value from SPINLOCKN_LOCK_REG is 0, the spinlock comes into the Locked status.
2. Execute the application codes, and the status of SPINLOCK_STATUS_REG is 1.
3. Write 0 to SPINLOCKN_LOCK_REGD, the spinlock converts into the Unlocked status, and the corresponding spinlock is released.

3.12.4.2 Processing the Interrupt

The spinlock generates an interrupt when a lock is freed (the lock status converts from Locked to Unlocked).

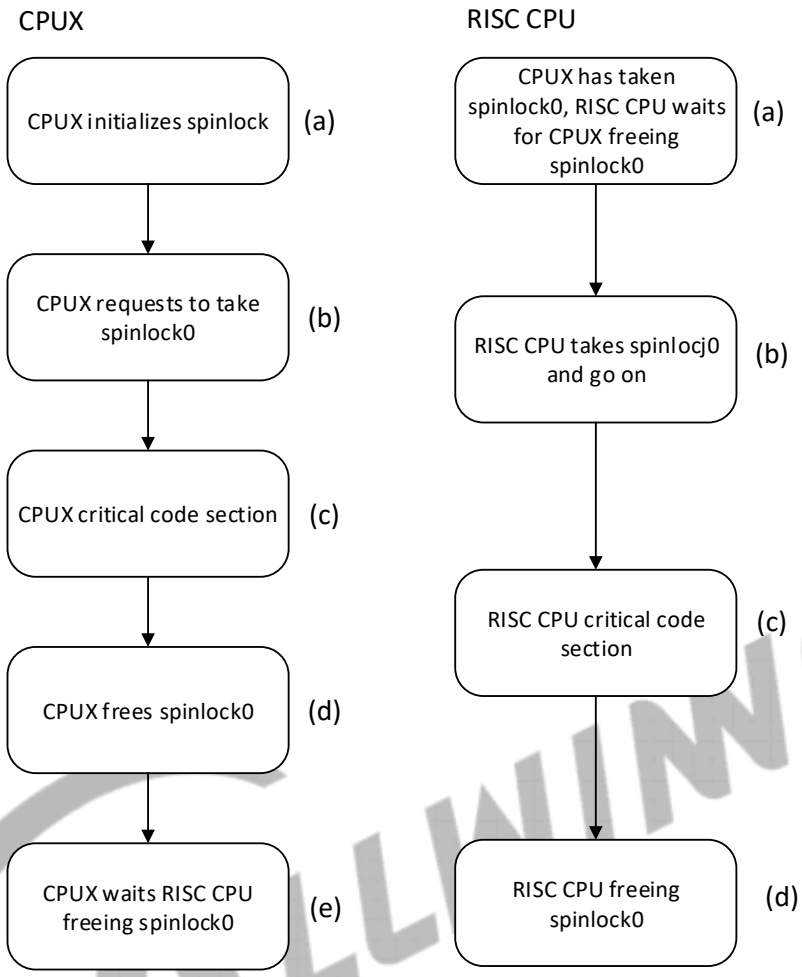
Follow the steps below to process the interrupt:

1. Configure the interrupt enable bit of the corresponding spinlock in SPINLOCK_IRQ_EN_REG to enable the interrupt.
2. The spinlock generates an interrupt when its status converts from Locked to Unlocked, and the corresponding bit of the SPINLOCK_IRQ_STA_REG turns to 1.
3. Execute the interrupt handle function and clear the pending bit.

3.12.4.3 Taking/Freeing Spinlock

Take Spinlock0 as an example, the CPUX takes the spinlock0 firstly in the instance. To take/free spinlock0, the CPUX and RISC CPU perform the following steps:

Figure 3-33 CPUX and RISC CPU Taking/Freeing Spinlock0 Process



CPUX:

1. The CPUX initializes Spinlock.
2. Firstly, check lock register0 (SPINLOCK_STATUS_REG0) status. if it is taken, check till CPUX frees spinlock0. Then request to take spinlock0. Otherwise, retry till lock register0 is taken.
3. Execute CPUX critical code.
4. After executing CPUX critical code, the CPUX frees spinlock0.
5. The CPUX waits for RISC CPU to free spinlock0.

RISC CPU:

1. If the CPUX has taken spinlock0, the RISC CPU waits for CPUX to free spinlock0.
2. The RISC CPU requests to take spinlock0. if fail, retry till lock register0 is taken.
3. Execute RISC CPU critical code.
4. After executing RISC CPU critical code, the RISC CPU frees spinlock0.

The following codes are for reference.

----------**CPUX of Cluster0**----------

1. CPUX initializes Spinlock

```
put_wvalue(SPINLOCK_BGR_REG,0x00010000);
put_wvalue(SPINLOCK_BGR_REG,0x00010001);
```

2. CPUX requests to take spinlock0

```
rdata=readl(SPINLOCK_STATUS_REG0);                  //Check lock register0 status
if(rdata != 0)    writel(0, SPINLOCK_LOCK_REG0);    //If it is taken, check till CPUX frees spinlock0
rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  //If it fails, retry till lock register0 is taken
 ---------- CPUX critical code section ----------
```

3. CPUX free spinlock0

```
writel(0, SPINLOCK_LOCK_REG0);                      //CPUX frees spinlock0
```

4. CPUX waits for RISC CPU' freeing spinlock0

```
writel(readl(SPINLOCK_STATUS_REG0) == 1);           //CPUX waits for RISC CPU' freeing spinlock0
```

----------**RISC CPU**----------

1. CPUX has taken spinlock0, RISC CPU waits for CPUX' freeing spinlock0

```
while(readl(SPINLOCK_STATUS_REG0) == 1);            //RISC CPU waits for CPUX' freeing spinlock0
```

2. RISC CPU takes spinlock0 and go on

```
rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  //If it fails, retry till lock register0 is taken
---------- RISC CPU critical code section ----------
```

3. RISC CPU frees spinlock0

```
writel(0, SPINLOCK_LOCK_REG0);                      //RISC CPU frees spinlock0
```

3.12.5 Register List

Module Name	Base Address
Spinlock	0x03005000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	SpinLock System Status Register
SPINLOCK_STATUS_REG	0x0010	SpinLock Status Register
SPINLOCK_IRQ_EN_REG	0x0020	SpinLock Interrupt Enable Register
SPINLOCK_IRQ_STA_REG	0x0040	SpinLock Interrupt Status Register
SPINLOCK_LOCKID0_REG	0x0080	SpinLock Lockid0 Register
SPINLOCK_LOCKID1_REG	0x0084	SpinLock Lockid1 Register
SPINLOCK_LOCKID2_REG	0x0088	SpinLock Lockid2 Register
SPINLOCK_LOCKID3_REG	0x008C	SpinLock Lockid3 Register
SPINLOCK_LOCKID4_REG	0x0090	SpinLock Lockid4 Register
SPINLOCKN_LOCK_REG	0x0100+N*0x0004 (N=0~31)	SpinLock Register N

3.12.6 Register Description

3.12.6.1 0x0000 Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM. Number of lock registers implemented. 00: This instance has 256 lock registers. 01: This instance has 32 lock registers. 10: This instance has 64 lock registers. 11: This instance has 128 lock registers.
27:9	/	/	/
8	R	0x0	IU0. Use Flag0. In-Use flag0, covering lock register0-31. 0: All lock register 0-31 are in the Not Taken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

3.12.6.2 0x0010 SpinLock Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS SpinLock[i] status (i=0~31) 0: The Spinlock is free 1: The Spinlock is taken

3.12.6.3 0x0020 SpinLock Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPINLOCK_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R/W	0x0	LOCK_IRQ_EN SpinLock[i] interrupt enable. 0: Disable 1: Enable

3.12.6.4 0x0040 SpinLock Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPINLOCK_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R/W1C	0x0	LOCK_IRQ _STATUS SpinLock[i] interrupt status. 0: No effect 1: Pending Writing 1 will clear this bit.

3.12.6.5 0x0100 + N*0x0004 SpinLock Register N (N = 0 to 31) (Default Value: 0x0000_0000)

Offset: 0x0100 + N*0x0004 (N = 0 to 31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TAKEN. Lock State. Read 0x0: The lock was previously Not Taken (free). The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must be retried. Write 0x1: No update to the lock value.

3.13 I/O Memory Management Unit (IOMMU)

3.13.1 Overview

The I/O Memory management unit (IOMMU) is designed for the specific memory requirements of products. It maps the virtual address (sent by peripheral access memory) to the physical address. The IOMMU allows multiple ways to manage the location of physical address, and it can use physical address which has potentially conflict mapping for different processes to allocate memory space, and also allow application of non-continuous address mapping to continuous virtual address space.

Features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports the parallel address mapping of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports the independent bypass function of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports the independent pre-fetch function of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports the independent interrupt handing mechanism of VE+VE_R, CSI, DE, G2D, ISP, RISC CPU, and NPU modules
- Supports 2 levels TLB (level 1 TLB for special using, and level 2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled function
- Triggers the PTW behavior when TLB is missed
- Supports the permission checking

3.13.2 Block Diagram

The internal module of IOMMU mainly includes the following parts.

Micro TLB: Level1 TLB, 64 words. Each peripheral corresponds to a TLB, which caching the level2 page table for the peripheral.

Macro TLB: Level2 TLB, 4K words. Each peripheral shares a level2 TLB for caching the level2 page table.

Pre-fetch Logic: Each Micro TLB corresponds to a Pre-fetch Logic. By monitoring each master device to predict the bus access, the secondary page table corresponding to the address to be accessed can be read from the memory and stored in the secondary TLB to improve the hit ratio.

PTW Logic: Page Table Walk, mainly contains PTW Cache and PTW. The PTW Cache is used to store the level1 page table; when the virtual address is missed in the level1 and level2 TLB, it will trigger the PTW. PTW Cache can store 512 level1 page tables, that is, 512 words.

PMU: Performance Monitoring Unit, which is used to count the hit efficiency and the latency.

APB Interface: IOMMU register instantiation module. CPU reads and writes the IOMMU register by APB bus.

The following figure shows the internal block diagram of IOMMU.

Figure 3-34 IOMMU Block Diagram

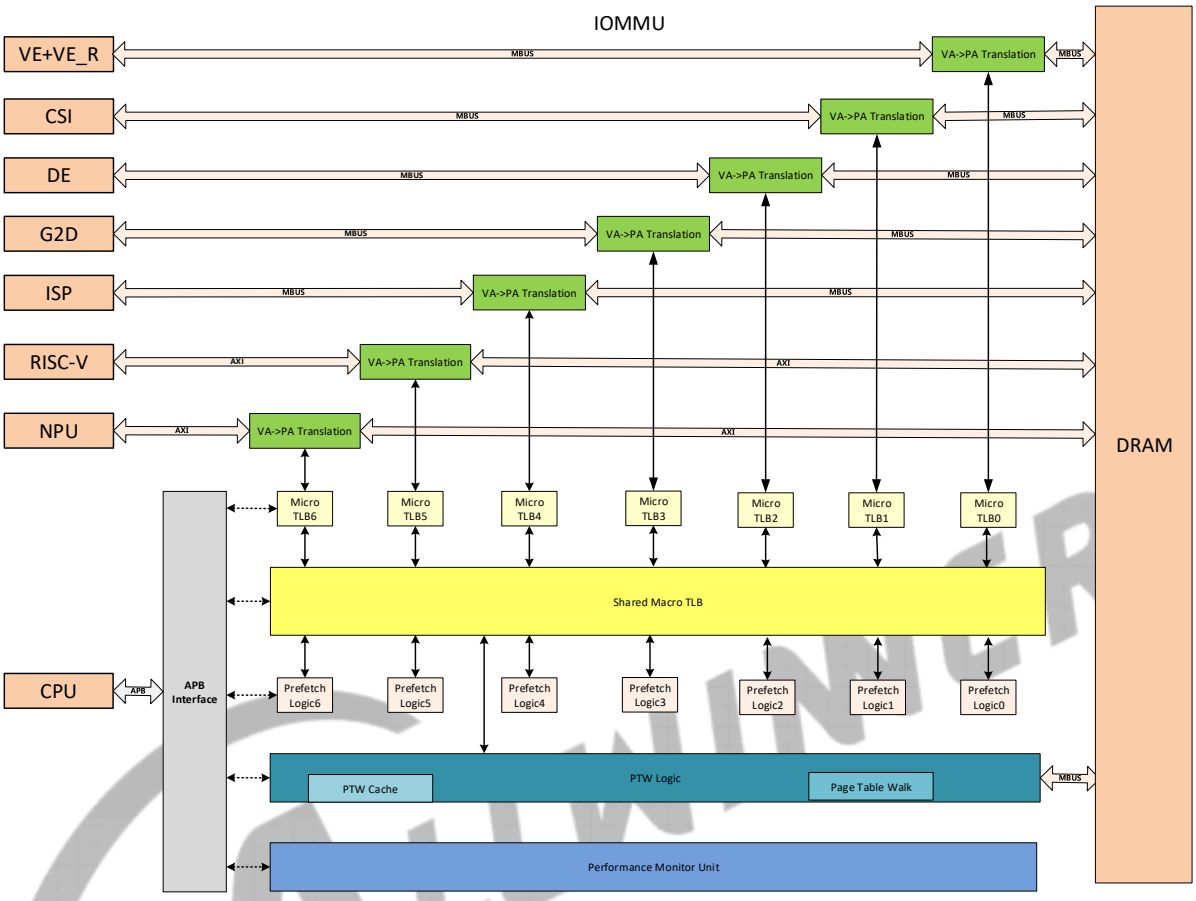


Table 3-16 Correspondence Relation between Master and Module

Master Number	Module
Master0	VE+VE_R
Master1	CSI
Master2	DE
Master3	G2D
Master4	ISP
Master5	RISC-V
Master6	NPU

3.13.3 Function Descriptions

3.13.3.1 Initialization

- Release the IOMMU reset signal by writing 1 to the bit[31] of the IOMMU_RESET_REG (Offset: 0x0010);
- Write the base address of the first TLB to the IOMMU_TTB_REG (Offset: 0x0050);
- Set the IOMMU_INT_ENABLE_REG (Offset: 0x0100);

- Enable the IOMMU by configuring the IOMMU_ENABLE_REG (Offset: 0x0020) in the final.

3.13.3.2 Address Translation

In the process of address mapping, the peripheral virtual address [31:12] are retrieved in the Level1 TLB. When TLB is hit, the mapping is finished. Otherwise, they are retrieved in the Level2 TLB in the same way. If TLB is hit, the hit mapping will be written to the Level1 TLB, and hit in Level1 TLB. If Level1 and Level2 TLB are retrieved fail, the PTW will be triggered. After opening the peripheral bypass function by setting IOMMU_BYPASS_REG (Offset: 0x0030), IOMMU will not map the address typed by this peripheral, and it will output the virtual address as the physical address. The typical applications are as follows.

Micro TLB hit

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is hit, it will return a Level2 page table containing the corresponding physical addresses and the permission Index;
3. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB hit

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is missed, continue to search Macro TLB;
3. If Macro TLB is hit, it will return the Level2 page table to Micro TLB;
4. Micro TLB receives this page table, puts it in Micro TLB (If this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;
5. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache hit

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is missed, continue to search Macro TLB;
3. If Macro TLB is missed, send the request to the PTW to return the corresponding page table;
4. PTW first accesses PTW Cache. If the required Level1 page table exists in the PTW Cache, send the page table to PTW logic;

5. PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;
6. Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;
7. Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;
8. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Micro TLB miss, Macro TLB miss, PTW Cache miss

1. The master device sends a transfer command, and also sends the address to the corresponding Micro TLB to search the Level2 page table related to the virtual address;
2. If Micro TLB is missed, continue to search Macro TLB;
3. If Macro TLB is missed, send the request to the PTW to return the corresponding page table;
4. PTW accesses PTW Cache, there is no necessary Level1 page table;
5. PTW accesses the memory, gets the corresponding Level1 page table and stores it in the PTW Cache (the replace activities may happen);
6. PTW logic returns the corresponding Level2 page table from the memory page table according to the Level1 page table, checks the effectiveness, and sends it to Macro TLB;
7. Macro TLB stores the Level2 page table (the replace activities may happen), and returns the Level2 page table to Micro TLB;
8. Micro TLB receives this page table, puts it in the Micro TLB (if this Micro TLB is full, the replace activities will happen), and sends the page table to the address translation module at the same time;
9. The address translation module converts the virtual address into the physical address, and checks the permissions at the same time. If it is passed, the transfer is completed.

Permission error

1. The permission checking is always performed during the process of translating the address;
2. Once the permission checking makes mistake, the new access of the master suspends, but the access before this checking can be continued;
3. Set the error status register;
4. Trigger the interrupt.

Invalid Level1 page table

1. The invalid Level1 page table is checked when PTW logic reads the new level page table from the memory;
2. The PTW reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the PTW cache;
3. If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in PTW Cache with target page table is found to be invalid after using;

If a page table is invalid, invalidate the total cache line (that is two page tables).

Invalid Level2 page table

1. The invalid Level2 page table is checked when Macro TLB reads the new level page table from the memory;
2. The Macro TLB reads two sequential page table entries from the memory (64-bit data, a complete cache line), and stores them in the Macro TLB;
3. If the current page table is invalid, the error flag is set and the interrupt is triggered. The cache line needs to be invalidated.

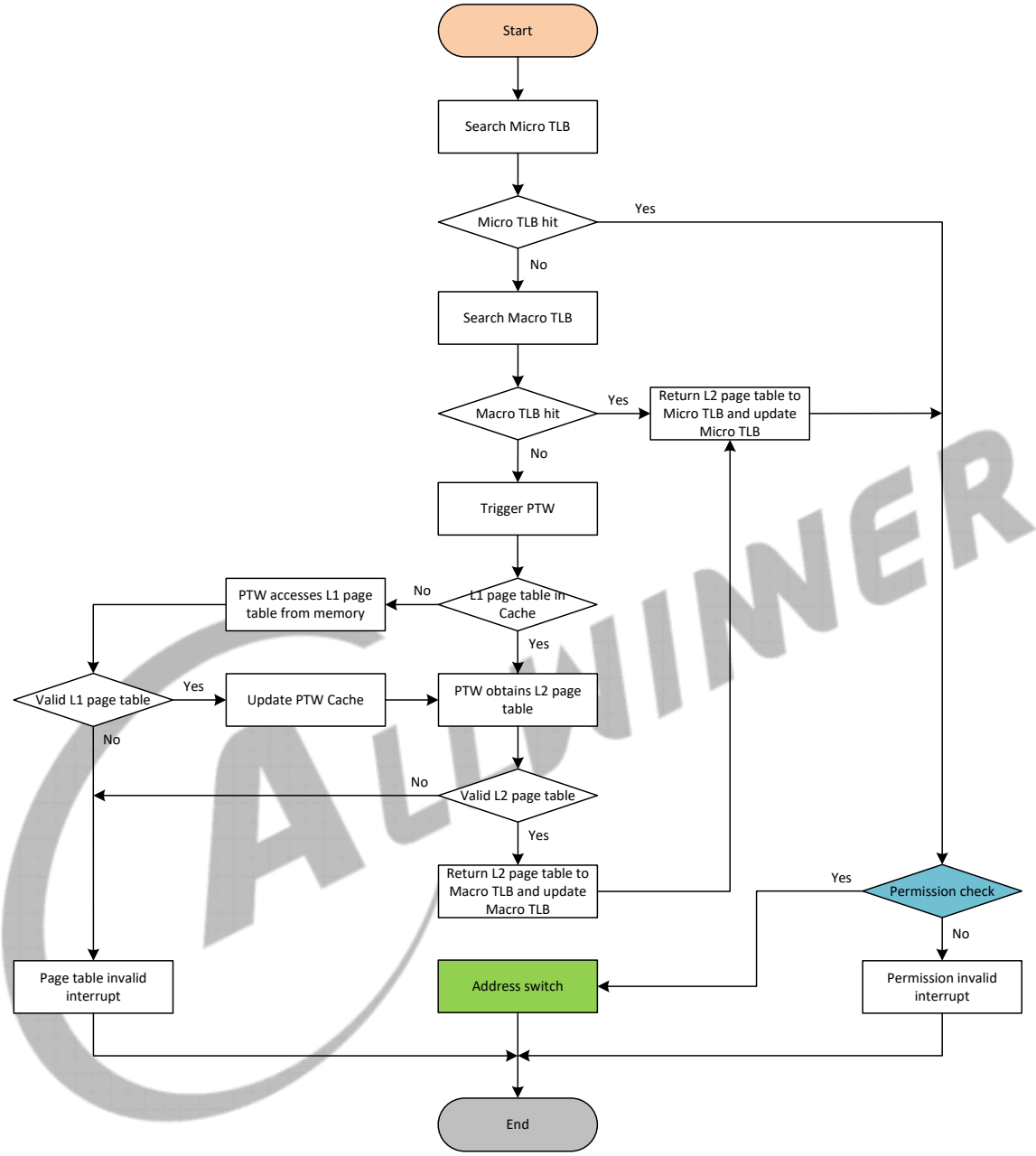
NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid, or the page table stored in Macro TLB with target page table is found to be invalid after using;

If a page table is invalid, invalidate the total cache line (that is two page tables).

The internal address translation process is shown in the following figure.

Figure 3-35 Internal Switch Process



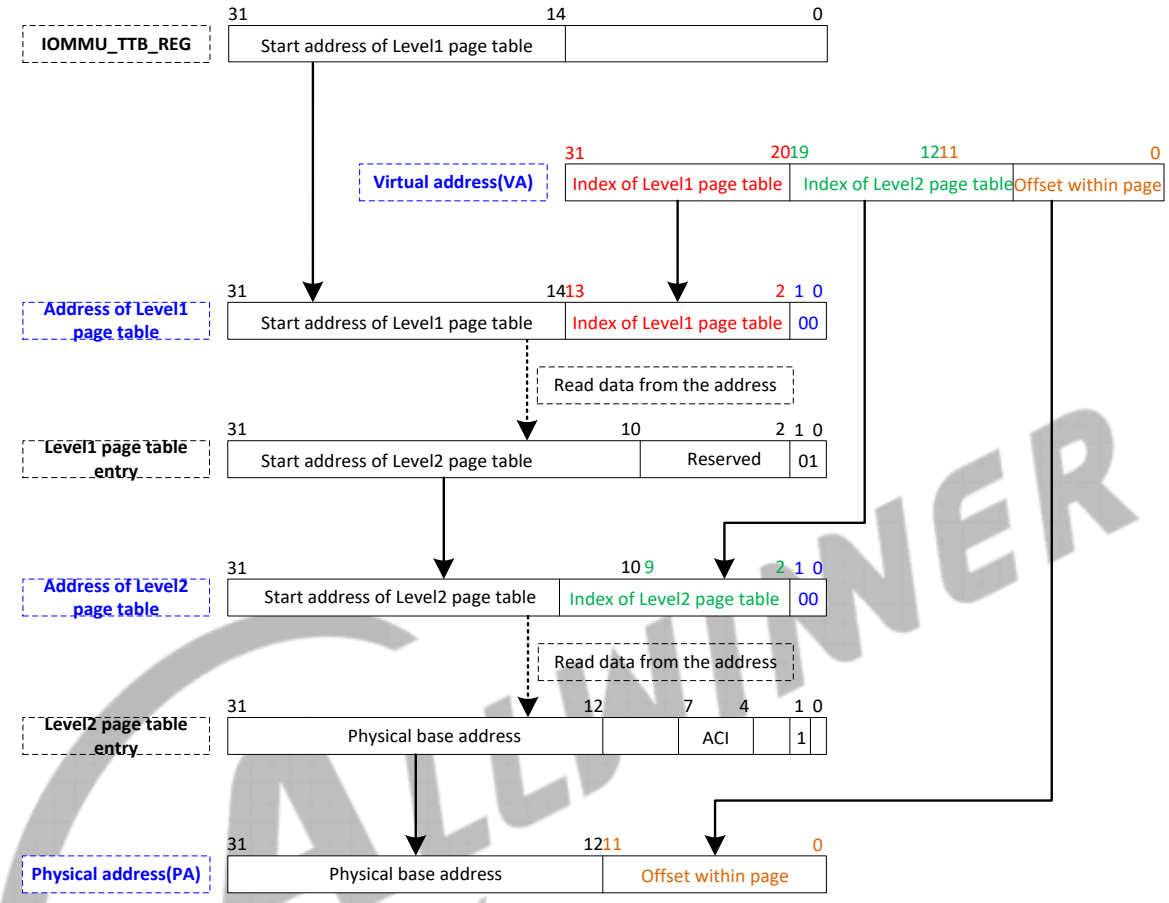
3.13.3.3 VA-PA Mapping

IOMMU page table is defined as the Level2 mapping. The first level is 1M address space mapping, the second level is 4K address space. This version does not support 1K, 16K and other page table sizes. IOMMU only supports a page table, the meaning is:

- All peripherals connected to IOMMU use the same virtual address space;
- The virtual address space of the peripherals can overlap;
- Different virtual addresses can map to the same physical address space;

Base address of this page table is defined by the software, and it needs 16 KB address alignment. The page table of the Level2 table item needs 1 KB address alignment. A complete VA-PA address translation process is shown in the following figure.

Figure 3-36 VA-PA Switch Process



3.13.3.4 Clearing and Invalidating TLB

When multi page table contents are refreshed or table address changes, all VA-PA mappings which have been cached in TLB will be invalid. You need to configure IOMMU_TLB_FLUSH_ENABLE_REG (Offset: 0x0080) to clear the TLB or PTW Cache according to the following steps:

1. Suspend the access to TLB or Cache.
2. Configure the corresponding Flush bit of IOMMU_TLB_FLUSH_ENABLE_REG (Offset: 0x0080).
3. After the operation takes effect, the related peripherals can continue to send the new access memory operations.

When some page table is invalid or the mapping is incorrect, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. The invalid TLB supports the following two modes:

Mode0

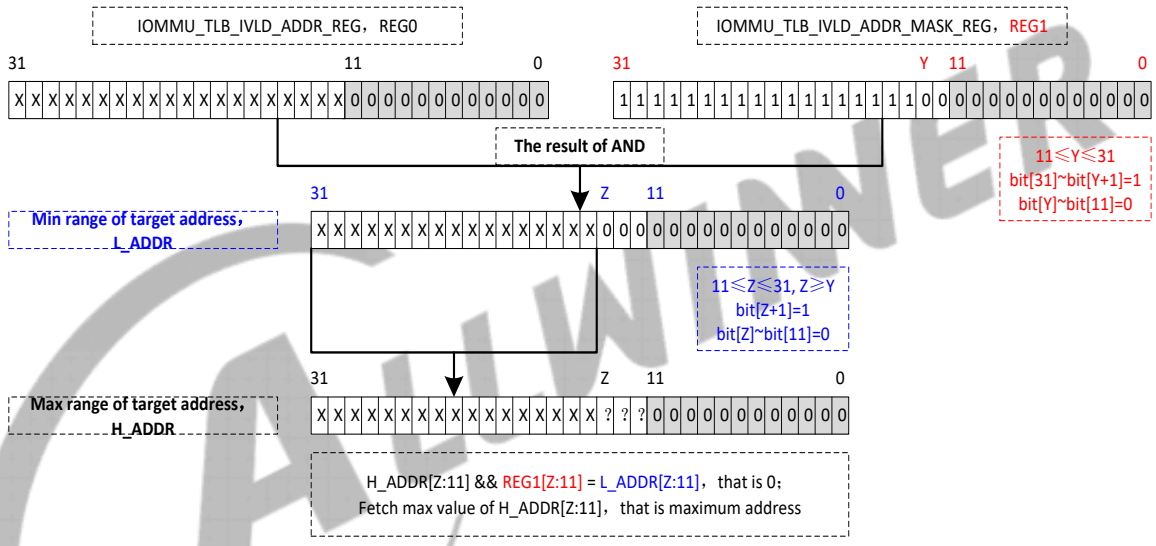
1. Set IOMMU_TLB_IVLD_MODE_SEL_REG (Offset: 0x0084) to 0 and select mode0;
2. Write the target address to IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090);

3. Set the configuration values to IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094), the requirements are as follows:

   - The value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) cannot be less than the IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090).
   - The higher bit of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) must be continuous 1, the lower bit must be continuous 0. For example, 0xFFFFF000, 0xFFFFE000, 0xFFFFC000, 0xFFFF8000, and 0xFFFF0000 are legal values; while 0xFFFFD000, 0xFFFFB000, 0xFFFFA000, 0xFFFF9000, and 0xFFFF7000 are illegal values.

4. Configure IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098) to enable the invalid operation. Among the way to determine the invalid address is to get the maximum valid bit and determine the target address range by the target address AND the mask address. The process is shown as follows.

Figure 3-37 Invalid TLB Address Range



The examples are shown below:

- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFF000 by default, the result of AND is target address. That is, only the target address is invalid.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFF0000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEEF000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFC000, the value of (0x0090) is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEEB000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFF8000, the value of IOMMU_TLB_IVLD_ADDR_REG (0x0090) is 0xEEEEC000, then target address range is from 0xEEEE8000 to 0xEEEEF000.
- When the value of IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094) is 0xFFFFC000, the value of IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090) is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEEE3000.

Mode1

1. Set IOMMU_TLB_IVLD_MODE_SEL_REG (Offset: 0x0084) to 1 and select mode1;
2. Set the starting address and the ending address of the invalid TLB by IOMMU_TLB_IVLD_STA_ADDR_REG (Offset: 0x0088);
3. Configure IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098) to enable the invalid operation, then the TLB invaliding operation can be completed.

3.13.3.5 Clearing and Invalidating PTW Cache

Mode0

1. Set IOMMU_PC_IVLD_MODE_SEL_REG (Offset: 0x009C) to 0 and select mode0.
2. Invalid the IOMMU_PC_IVLD_ADDR_REG (Offset: 0x00A0), 1MB aligned.
3. Configure IOMMU_PC_IVLD_ENABLE_REG (Offset: 0x00A8) to enable the invalid operation, then you can invalid one piece of CacheLine.

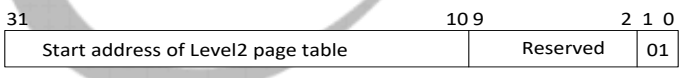
Mode1

1. Set IOMMU_PC_IVLD_MODE_SEL_REG (Offset: 0x009C) to 1 and select mode1.
2. Set the starting address and the ending address of the invalid TLB by IOMMU_PC_IVLD_STA_ADDR_REG (Offset: 0x00A4).
3. Configure IOMMU_PC_IVLD_ENABLE_REG (Offset: 0x00A8) to enable the invalid operation, then you can invalid a period of sections.

3.13.3.6 Level1 Page Table

The format of Level1 page table is as follows.

Figure 3-38 Level1 Page Table Format



Bit[31:10]: Base address of Level2 page table;

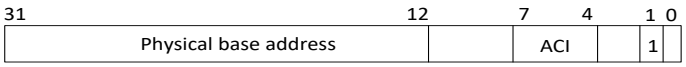
Bit[9:2]: Reserved;

Bit[1:0]: 01 is a valid page table; other values are fault;

3.13.3.7 Level2 Page Table

The format of Level2 page table is as follows.

Figure 3-39 Level2 Page Table Format



Bit[31:12]: Physical address of 4K address;

Bit[11:8]: Reserved;

Bit[7:4]: ACI, permission control index; correspond to permission control bit of **IOMMU Domain Authority Control Register**;

Bit[3:2]: Reserved;

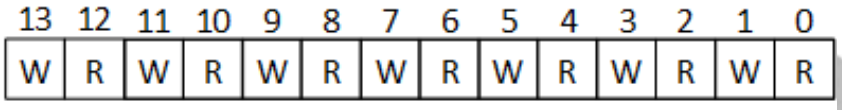
Bit[1]: 1 is a valid page table; 0 is fault;

Bit[0]: Reserved

3.13.3.8 Permission Index

The read/write access control of series register such as **IOMMU Domain Authority Control Register** is as follows.

Figure 3-40 Read/Write Permission Control



Bit[1:0]/Bit[17:16]: Master0 read/write permission control;

Bit[3:2]/Bit[19:18]: Master1 read/write permission control;

Bit[5:4]/Bit[21:20]: Master2 read/write permission control;

Bit[7:6]/Bit[23:22]: Master3 read/write permission control;

Bit[9:8]/Bit[25:24]: Master4 read/write permission control;

Bit[11:10]/Bit[27:26]: Master5 read/write permission control;

Bit[13:12]/Bit[29:28]: Master6 read/write permission control.

The value of **IOMMU Domain Authority Control Register** is read-only by default. Other registers can configure through the system requirement. During the address switch process, the corresponding relation between ACI and Domain is as follows.

Table 3-17 Relation between ACI and Domain

ACI	Domain	Register
0	Domain 0	IOMMU Domain Authority Control Register 0
1	Domain 1	IOMMU Domain Authority Control Register 0
2	Domain 2	IOMMU Domain Authority Control Register 1
3	Domain 3	IOMMU Domain Authority Control Register 1
4	Domain 4	IOMMU Domain Authority Control Register 2
5	Domain 5	IOMMU Domain Authority Control Register 2
6	Domain 6	IOMMU Domain Authority Control Register 3
7	Domain 7	IOMMU Domain Authority Control Register 3

ACI	Domain	Register
8	Domain 8	IOMMU Domain Authority Control Register 4
9	Domain 9	IOMMU Domain Authority Control Register 4
10	Domain 10	IOMMU Domain Authority Control Register 5
11	Domain 11	IOMMU Domain Authority Control Register 5
12	Domain 12	IOMMU Domain Authority Control Register 6
13	Domain 13	IOMMU Domain Authority Control Register 6
14	Domain 14	IOMMU Domain Authority Control Register 7
15	Domain 15	IOMMU Domain Authority Control Register7

After enabled **IOMMU Domain Authority Overwrite Register**, the read/write control permission can override all **IOMMU Domain Authority Control Register**.

3.13.4 Programming Guidelines

3.13.4.1 Resetting IOMMU

Before the IOMMU module software reset operation, make sure IOMMU is never opened, or all bus operations are completed, or DRAM and peripherals already open the corresponding switch, to shield the influence of IOMMU reset.

3.13.4.2 Enabling IOMMU

Before opening the IOMMU address mapping function, IOMMU_TTB_REG (Offset: 0x0050) should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

3.13.4.3 Configuring TTB

Operating the register must close IOMMU address mapping function, namely IOMMU_ENABLE_REG (Offset: 0x0020) is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

3.13.4.4 Clearing TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

3.13.4.5 Reading/Writing VA Data

For the virtual address, read and write the corresponding physical address data to make sure whether IOMMU module address mapping function is normal. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after the operation is finished, check if the results are as expected.

3.13.4.6 PMU Statistics

When PMU function is used for the first time, set IOMMU_PMU_ENABLE_REG (Offset: 0x0200) to enable statistics function; when reading the relevant Register, clear the enable bit of IOMMU_PMU_ENABLE_REG (Offset: 0x0200); when PMU function is used next time, first IOMMU_PMU_CLR_REG (Offset: 0x0210) is set, after counter is cleared, set the enable bit of IOMMU_PMU_ENABLE_REG (Offset: 0x0200).

Given a Level2 page table administers continuous 4KB address, if Micro TLB misses in continuous virtual address, a Level2 page table needs to be returned from Macro TLB to hit; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So the true hit rate calculation is as follows:

Hit Rate = N1/M1 + (1-N1/M1)*N2/M2

N1: Micro TLB hit number
M1: Micro TLB access number
N2: Macro TLB hit number
M2: Macro TLB access number

3.13.5 Register List

Module Name	Base Address
IOMMU	0x0201_0000

Register Name	Offset	Description
IOMMU_RESET_REG	0x0010	IOMMU Reset Register
IOMMU_ENABLE_REG	0x0020	IOMMU Enable Register
IOMMU_BYPASS_REG	0x0030	IOMMU Bypass Register
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto Gating Register
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table Base Register
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB Enable Register
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB Prefetch Register
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_MODE_SEL_REG	0x0084	IOMMU TLB Invalidation Mode Select Register
IOMMU_TLB_IVLD_STA_ADDR_REG	0x0088	IOMMU TLB Invalidation Start Address Register
IOMMU_TLB_IVLD_END_ADDR_REG	0x008C	IOMMU TLB Invalidation End Address Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register
IOMMU_PC_IVLD_MODE_SEL_REG	0x009C	IOMMU PC Invalidation Mode Select Register
IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register

Register Name	Offset	Description
IOMMU_PC_IVLD_STA_ADDR_REG	0x00A4	IOMMU PC Invalidation Start Address Register
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_PC_IVLD_END_ADDR_REG	0x00AC	IOMMU PC Invalidation End Address Register
IOMMU_DM_AUT_CTRL0_REG	0x00B0	IOMMU Domain Authority Control 0 Register
IOMMU_DM_AUT_CTRL1_REG	0x00B4	IOMMU Domain Authority Control 1 Register
IOMMU_DM_AUT_CTRL2_REG	0x00B8	IOMMU Domain Authority Control 2 Register
IOMMU_DM_AUT_CTRL3_REG	0x00BC	IOMMU Domain Authority Control 3 Register
IOMMU_DM_AUT_CTRL4_REG	0x00C0	IOMMU Domain Authority Control 4 Register
IOMMU_DM_AUT_CTRL5_REG	0x00C4	IOMMU Domain Authority Control 5 Register
IOMMU_DM_AUT_CTRL6_REG	0x00C8	IOMMU Domain Authority Control 6 Register
IOMMU_DM_AUT_CTRL7_REG	0x00CC	IOMMU Domain Authority Control 7 Register
IOMMU_DM_AUT_OVWT_REG	0x00D0	IOMMU Domain Authority Overwrite Register
IOMMU_INT_ENABLE_REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR_REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA_REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR0_REG	0x0110	IOMMU Interrupt Error Address 0 Register
IOMMU_INT_ERR_ADDR1_REG	0x0114	IOMMU Interrupt Error Address 1 Register
IOMMU_INT_ERR_ADDR2_REG	0x0118	IOMMU Interrupt Error Address 2 Register
IOMMU_INT_ERR_ADDR3_REG	0x011C	IOMMU Interrupt Error Address 3 Register
IOMMU_INT_ERR_ADDR4_REG	0x0120	IOMMU Interrupt Error Address 4 Register
IOMMU_INT_ERR_ADDR5_REG	0x0124	IOMMU Interrupt Error Address 5 Register
IOMMU_INT_ERR_ADDR6_REG	0x0128	IOMMU Interrupt Error Address 6 Register
IOMMU_INT_ERR_ADDR7_REG	0x0130	IOMMU Interrupt Error Address 7 Register
IOMMU_INT_ERR_ADDR8_REG	0x0134	IOMMU Interrupt Error Address 8 Register
IOMMU_INT_ERR_DATA0_REG	0x0150	IOMMU Interrupt Error Data 0 Register
IOMMU_INT_ERR_DATA1_REG	0x0154	IOMMU Interrupt Error Data 1 Register
IOMMU_INT_ERR_DATA2_REG	0x0158	IOMMU Interrupt Error Data 2 Register
IOMMU_INT_ERR_DATA3_REG	0x015C	IOMMU Interrupt Error Data 3 Register
IOMMU_INT_ERR_DATA4_REG	0x0160	IOMMU Interrupt Error Data 4 Register
IOMMU_INT_ERR_DATA5_REG	0x0164	IOMMU Interrupt Error Data 5 Register
IOMMU_INT_ERR_DATA6_REG	0x0168	IOMMU Interrupt Error Data 6 Register
IOMMU_INT_ERR_DATA7_REG	0x0170	IOMMU Interrupt Error Data 7 Register
IOMMU_INT_ERR_DATA8_REG	0x0174	IOMMU Interrupt Error Data 8 Register
IOMMU_L1PG_INT_REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT_REG	0x0184	IOMMU L2 Page Table Interrupt Register
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE_REG	0x0200	IOMMU PMU Enable Register
IOMMU_PMU_CLR_REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW0_REG	0x0230	IOMMU PMU Access Low 0 Register
IOMMU_PMU_ACCESS_HIGH0_REG	0x0234	IOMMU PMU Access High 0 Register

Register Name	Offset	Description
IOMMU_PMU_HIT_LOW0_REG	0x0238	IOMMU PMU Hit Low 0 Register
IOMMU_PMU_HIT_HIGH0_REG	0x023C	IOMMU PMU Hit High 0 Register
IOMMU_PMU_ACCESS_LOW1_REG	0x0240	IOMMU PMU Access Low 1 Register
IOMMU_PMU_ACCESS_HIGH1_REG	0x0244	IOMMU PMU Access High 1 Register
IOMMU_PMU_HIT_LOW1_REG	0x0248	IOMMU PMU Hit Low 1 Register
IOMMU_PMU_HIT_HIGH1_REG	0x024C	IOMMU PMU Hit High 1 Register
IOMMU_PMU_ACCESS_LOW2_REG	0x0250	IOMMU PMU Access Low 2 Register
IOMMU_PMU_ACCESS_HIGH2_REG	0x0254	IOMMU PMU Access High 2 Register
IOMMU_PMU_HIT_LOW2_REG	0x0258	IOMMU PMU Hit Low 2 Register
IOMMU_PMU_HIT_HIGH2_REG	0x025C	IOMMU PMU Hit High 2 Register
IOMMU_PMU_ACCESS_LOW3_REG	0x0260	IOMMU PMU Access Low 3 Register
IOMMU_PMU_ACCESS_HIGH3_REG	0x0264	IOMMU PMU Access High 3 Register
IOMMU_PMU_HIT_LOW3_REG	0x0268	IOMMU PMU Hit Low 3 Register
IOMMU_PMU_HIT_HIGH3_REG	0x026C	IOMMU PMU Hit High 3 Register
IOMMU_PMU_ACCESS_LOW4_REG	0x0270	IOMMU PMU Access Low 4 Register
IOMMU_PMU_ACCESS_HIGH4_REG	0x0274	IOMMU PMU Access High 4 Register
IOMMU_PMU_HIT_LOW4_REG	0x0278	IOMMU PMU Hit Low 4 Register
IOMMU_PMU_HIT_HIGH4_REG	0x027C	IOMMU PMU Hit High 4 Register
IOMMU_PMU_ACCESS_LOW5_REG	0x0280	IOMMU PMU Access Low 5 Register
IOMMU_PMU_ACCESS_HIGH5_REG	0x0284	IOMMU PMU Access High 5 Register
IOMMU_PMU_HIT_LOW5_REG	0x0288	IOMMU PMU Hit Low 5 Register
IOMMU_PMU_HIT_HIGH5_REG	0x028C	IOMMU PMU Hit High 5 Register
IOMMU_PMU_ACCESS_LOW6_REG	0x0290	IOMMU PMU Access Low 6 Register
IOMMU_PMU_ACCESS_HIGH6_REG	0x0294	IOMMU PMU Access High 6 Register
IOMMU_PMU_HIT_LOW6_REG	0x0298	IOMMU PMU Hit Low 6 Register
IOMMU_PMU_HIT_HIGH6_REG	0x029C	IOMMU PMU Hit High 6 Register
IOMMU_PMU_ACCESS_LOW7_REG	0x02D0	IOMMU PMU Access Low 7 Register
IOMMU_PMU_ACCESS_HIGH7_REG	0x02D4	IOMMU PMU Access High 7 Register
IOMMU_PMU_HIT_LOW7_REG	0x02D8	IOMMU PMU Hit Low 7 Register
IOMMU_PMU_HIT_HIGH7_REG	0x02DC	IOMMU PMU Hit High 7 Register
IOMMU_PMU_ACCESS_LOW8_REG	0x02E0	IOMMU PMU Access Low 8 Register
IOMMU_PMU_ACCESS_HIGH8_REG	0x02E4	IOMMU PMU Access High 8 Register
IOMMU_PMU_HIT_LOW8_REG	0x02E8	IOMMU PMU Hit Low 8 Register
IOMMU_PMU_HIT_HIGH8_REG	0x02EC	IOMMU PMU Hit High 8 Register
IOMMU_PMU_TL_LOW0_REG	0x0300	IOMMU Total Latency Low 0 Register
IOMMU_PMU_TL_HIGH0_REG	0x0304	IOMMU Total Latency High 0 Register
IOMMU_PMU_ML0_REG	0x0308	IOMMU Max Latency 0 Register
IOMMU_PMU_TL_LOW1_REG	0x0310	IOMMU Total Latency Low 1 Register
IOMMU_PMU_TL_HIGH1_REG	0x0314	IOMMU Total Latency High 1 Register
IOMMU_PMU_ML1_REG	0x0318	IOMMU Max Latency 1 Register
IOMMU_PMU_TL_LOW2_REG	0x0320	IOMMU Total Latency Low 2 Register
IOMMU_PMU_TL_HIGH2_REG	0x0324	IOMMU Total Latency High 2 Register

Register Name	Offset	Description
IOMMU_PMU_ML2_REG	0x0328	IOMMU Max Latency 2 Register
IOMMU_PMU_TL_LOW3_REG	0x0330	IOMMU Total Latency Low 3 Register
IOMMU_PMU_TL_HIGH3_REG	0x0334	IOMMU Total Latency High 3 Register
IOMMU_PMU_ML3_REG	0x0338	IOMMU Max Latency 3 Register
IOMMU_PMU_TL_LOW4_REG	0x0340	IOMMU Total Latency Low 4 Register
IOMMU_PMU_TL_HIGH4_REG	0x0344	IOMMU Total Latency High 4 Register
IOMMU_PMU_ML4_REG	0x0348	IOMMU Max Latency 4 Register
IOMMU_PMU_TL_LOW5_REG	0x0350	IOMMU Total Latency Low 5 Register
IOMMU_PMU_TL_HIGH5_REG	0x0354	IOMMU Total Latency High 5 Register
IOMMU_PMU_ML5_REG	0x0358	IOMMU Max Latency 5 Register
IOMMU_PMU_TL_LOW6_REG	0x0360	IOMMU Total Latency Low 6 Register
IOMMU_PMU_TL_HIGH6_REG	0x0364	IOMMU Total Latency High 6 Register
IOMMU_PMU_ML6_REG	0x0368	IOMMU Max Latency 6 Register

3.13.6 Register Description

3.13.6.1 0x0010 IOMMU Reset Register (Default Value: 0x8003_007F)

Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	IOMMU_RESET IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; Or all bus operations are completed; Or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset.
30:18	/	/	/
17	R/W	0x1	PTW_CACHE_RESET PTW Cache address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used to reset PTW Cache individually.
16	R/W	0x1	MACRO_TLB_RESET Macro TLB address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Macro TLB occurs abnormal, the bit is used to reset Macro TLB individually.
15:7	/	/	/

Offset: 0x0010			Register Name: IOMMU_RESET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x1	MASTER6_RESET Master6 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master6 occurs abnormal, the bit is used to reset Master6 individually.
5	R/W	0x1	MASTER5_RESET Master5 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, the bit is used to reset Master5 individually.
4	R/W	0x1	MASTER4_RESET Master4 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, the bit is used to reset Master4 individually.
3	R/W	0x1	MASTER3_RESET Master3 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, the bit is used to reset Master3 individually.
2	R/W	0x1	MASTER2_RESET Master2 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, the bit is used to reset Master2 individually.
1	R/W	0x1	MASTER1_RESET Master1 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master1 occurs abnormal, the bit is used to reset Master1 individually.
0	R/W	0x1	MASTER0_RESET Master0 address converts lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, the bit is used to reset Master0 individually.

3.13.6.2 0x0020 IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU Before opening the IOMMU address mapping function, configure the Translation Table Base register; or ensure all masters are in the bypass status or the status without sending a bus command (such as reset)

3.13.6.3 0x0030 IOMMU Bypass Register (Default Value: 0x0000_007F)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_BYPASS Master6 bypass switch After bypass function is opened, IOMMU cannot map the address of Master6 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
5	R/W	0x1	MASTER5_BYPASS After bypass function is opened, IOMMU cannot map the address of Master5 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
4	R/W	0x1	MASTER4_BYPASS Master4 bypass switch After bypass function is opened, IOMMU cannot map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x1	MASTER3_BYPASS Master3 bypass switch After bypass function is opened, IOMMU cannot map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
2	R/W	0x1	MASTER2_BYPASS Master2 bypass switch After bypass function is opened, IOMMU cannot map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
1	R/W	0x1	MASTER1_BYPASS Master1 bypass switch After bypass function is opened, IOMMU cannot map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
0	R/W	0x1	MASTER0_BYPASS Master0 bypass switch After bypass function is opened, IOMMU cannot map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

NOTE

Operating the register belongs to a non-accurate timing sequence control function. That is, before the function is valid, the master operation will complete the address mapping function. The operation after this will not perform the address mapping. It is suggested that the master is in the reset state or the status without sending a bus command before operating the register.

3.13.6.4 0x0040 IOMMU Auto Gating Register (Default Value: 0x0000_0001)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	IOMMU_AUTO_GATING IOMMU circuit auto gating control. The purpose is decreasing power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

3.13.6.5 0x0044 IOMMU Write Buffer Control Register (Default Value: 0x0000_007F)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_WBUF_CTRL Master6 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**
5	R/W	0x1	MASTER5_WBUF_CTRL Master5 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**
4	R/W	0x1	MASTER4_WBUF_CTRL Master4 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**
3	R/W	0x1	MASTER3_WBUF_CTRL Master3 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x1	MASTER2_WBUF_CTRL Master2 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**
1	R/W	0x1	MASTER1_WBUF_CTRL Master1 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**
0	R/W	0x1	MASTER0_WBUF_CTRL Master0 write buffer control bit 0: Disable write buffer 1: Enable write buffer **Note: the hardware does not have the configuration, this bit is invalid.**

3.13.6.6 0x0048 IOMMU Out of Order Control Register (Default Value: 0x0000_007F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_OOO_CTRL Master6 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
5	R/W	0x1	MASTER5_OOO_CTRL Master5 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
4	R/W	0x1	MASTER4_OOO_CTRL Master4 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
3	R/W	0x1	MASTER3_OOO_CTRL Master3 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x1	MASTER2_OOO_CTRL Master2 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
1	R/W	0x1	MASTER1_OOO_CTRL Master1 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
0	R/W	0x1	MASTER0_OOO_CTRL Master0 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order

3.13.6.7 0x004C IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_007F)

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_4KB_BDY_PRT_CTRL Master6 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect **Note: the hardware does not have the configuration, this bit is invalid.**
5	R/W	0x1	MASTER5_4KB_BDY_PRT_CTRL Master5 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect **Note: the hardware does not have the configuration, this bit is invalid.**
4	R/W	0x1	MASTER4_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect **Note: the hardware does not have the configuration, this bit is invalid.**
3	R/W	0x1	MASTER3_4KB_BDY_PRT_CTRL Master3 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect **Note: the hardware does not have the configuration, this bit is invalid.**

Offset: 0x004C			Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x1	MASTER2_4KB_BDY_PRT_CTRL Master2 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
1	R/W	0x1	MASTER1_4KB_BDY_PRT_CTRL Master1 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
0	R/W	0x1	MASTER0_4KB_BDY_PRT_CTRL Master0 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect

NOTE

When the virtual address sent by master is over the 4KB boundary, the 4KB protection unit will split it into two serial accesses.

3.13.6.8 0x0050 IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: IOMMU_TTB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	R/W	0x0	TTB Level1 page table starting address, aligned to 16 KB. When operating the register, the IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0; Or the Bypass function of all masters is set to 1, or the Bypass function does not transfer the bus commands (such as setting).
13:0	/	/	/

3.13.6.9 0x0060 IOMMU TLB Enable Register (Default Value: 0x0003_007F)

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x1	PTW_CACHE_ENABLE PTW Cache enable bit. 0: Disable 1: Enable
16	R/W	0x1	MACRO_TLB_ENABLE Macro TLB enable bit 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	MICRO_TLB6_ENABLE Micro TLB6 enable bit 0: Disable 1: Enable
5	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable
3	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
1	R/W	0x1	MICRO_TLB1_ENABLE Micro TLB1 enable bit 0: Disable 1: Enable
0	R/W	0x1	MICRO_TLB0_ENABLE Micro TLB0 enable bit 0: Disable 1: Enable

3.13.6.10 0x0070 IOMMU TLB Pre-fetch Register (Default Value: 0x0003_0000)

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x1	PREFETCH_VALID_PAGE_TO_PC 0: Disabled 1: Enabled **Note: If this function is enabled, the pre-fetch operation will not update the invalid level1 page table to the PTW Cache.**
16	R/W	0x1	PREFETCH_VALID_ PAGE_ TO_TLB 0: Disabled 1: Enabled **Note: If this function is enabled, the pre-fetch operation will not update the invalid level2 page table to TLB.**
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_PREFETCH Micro TLB6 pre-fetch enable bit 0: Disabled 1: Enabled

Offset: 0x0070			Register Name: IOMMU_TLB_PREFETCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	MICRO_TLB5_PREFETCH Micro TLB5 pre-fetch enable bit 0: Disabled 1: Enabled
4	R/W	0x0	MICRO_TLB4_PREFETCH Micro TLB4 pre-fetch enable bit 0: Disabled 1: Enabled
3	R/W	0x0	MICRO_TLB3_PREFETCH Micro TLB3 pre-fetch enable bit 0: Disabled 1: Enabled
2	R/W	0x0	MICRO_TLB2_PREFETCH Micro TLB2 pre-fetch enable bit 0: Disabled 1: Enabled
1	R/W	0x0	MICRO_TLB1_PREFETCH Micro TLB1 pre-fetch enable bit 0: Disabled 1: Enabled
0	R/W	0x0	MICRO_TLB0_PREFETCH Micro TLB0 pre-fetch enable bit 0: Disabled 1: Enabled

3.13.6.11 0x0080 IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PTW_CACHE_FLUSH Clear PTW Cache 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
16	R/WAC	0x0	MACRO_TLB_FLUSH Clear Macro TLB 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:7	/	/	/
6	R/WAC	0x0	MICRO_TLB6_FLUSH Clear Micro TLB6 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
5	R/WAC	0x0	MICRO_TLB5_FLUSH Clear Micro TLB5 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
4	R/WAC	0x0	MICRO_TLB4_FLUSH Clear Micro TLB4 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
3	R/WAC	0x0	MICRO_TLB3_FLUSH Clear Micro TLB3 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
2	R/WAC	0x0	MICRO_TLB2_FLUSH Clear Micro TLB2 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.
1	R/WAC	0x0	MICRO_TLB1_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	MICRO_TLB0_FLUSH Clear Micro TLB0 0: No clear operation or clear operation completed 1: Enable the clear operation After the Flush operation completes, the bit can be cleared to 0 automatically.

NOTE

When performing flush operation, all TLB/Cache access will be paused.
Before flush starts, the operation that has entered TLB continues to complete.

3.13.6.12 0x0084 IOMMU TLB Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TLB_IVLD_MODE_SEL 0: invalid TLB with Mask mode 1: invalid TLB with Start and End mode

3.13.6.13 0x0088 IOMMU TLB Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: IOMMU_TLB_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_STA_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.13.6.14 0x008C IOMMU TLB Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: IOMMU_TLB_IVLD_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_END_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.13.6.15 0x0090 IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

Operation:

1. Set the virtual address which needs to be operated in IOMMU_TLB_IVLD_ADDR_REG (Offset: 0x0090).
2. Set the mask of virtual address which needs to be operated in IOMMU_TLB_IVLD_ADDR_MASK_REG (Offset: 0x0094).
3. Write '1' to IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098).
4. Read IOMMU_TLB_IVLD_ENABLE_REG (Offset: 0x0098), when it is '0', indicating that invalidation behavior is finished.

NOTE

Performing the invalidation operation does not affect the TLB/Cache operations.
There is no absolute relationship between operating the Invalidation and converting the same address.

3.13.6.16 0x0094 IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB invalid address mask register, 4KB aligned.
11:0	/	/	/

3.13.6.17 0x0098 IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	TLB_IVLD_ENABLE Enable TLB invalid operation 0: No-operation or operation completed 1: Enable is invalid After the invalidation operation is completed, the bit can be cleared to 0 automatically. **Note: Performing the invalidation operation does not affect the TLB/Cache operations. There is no absolute relationship between operating the Invalidation and converting the same address.**

3.13.6.18 0x009C IOMMU PC Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: IOMMU_PC_IVLD_MODE_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PC_IVLD_MODE_SEL 0: Invalid PTW Cache using the default method 1: Invalid PTW Cache using the Start and End methods

3.13.6.19 0x00A0 IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_ADDR PTW Cache invalid address, 1 MB aligned.
19:0	/	/	/

3.13.6.20 0x00A4 IOMMU PC Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: IOMMU_PC_IVLD_STA_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:20	R/W	0x0	PC_IVLD_STA_ADDR PTW Cache invalid address, 1 MB aligned.
19:0	/	/	/

3.13.6.21 0x00A8 IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: IOMMU_PC_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	PC_IVLD_ENABLE Enable PTW Cache invalid operation 0: No-operation or operation completed 1: Enable is invalid After the invalidation operation is completed, the bit can be cleared to 0 automatically. **Note: Performing the invalidation operation does not affect the TLB/Cache operations. There is no absolute relationship between operating the Invalidation and converting the same address.**

3.13.6.22 0x00AC IOMMU PC Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: IOMMU_PC_IVLD_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	0x0	PC_IVLD_END_ADDR PTW Cache invalid address, 1 MB aligned.
19:0	/	/	/

3.13.6.23 0x00B0 IOMMU Domain Authority Control 0 Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM1_M6_WT_AUT_CTRL Domain1 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM1_M6_RD_AUT_CTRL Domain1 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM1_M5_WT_AUT_CTRL Domain1 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26	R/W	0x0	DM1_M5_RD_AUT_CTRL Domain1 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM1_M4_WT_AUT_CTRL Domain1 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM1_M4_RD_AUT_CTRL Domain1 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM1_M3_WT_AUT_CTRL Domain1 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM1_M3_RD_AUT_CTRL Domain1 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM1_M2_WT_AUT_CTRL Domain1 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM1_M2_RD_AUT_CTRL Domain1 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM1_M1_WT_AUT_CTRL Domain1 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM1_M1_RD_AUT_CTRL Domain1 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM1_M0_WT_AUT_CTRL Domain1 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	DM1_M0_RD_AUT_CTRL Domain1 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R	0x0	DM0_M6_WT_AUT_CTRL Domain0 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R	0x0	DM0_M6_RD_AUT_CTRL Domain0 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R	0x0	DM0_M5_WT_AUT_CTRL Domain0 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R	0x0	DM0_M5_RD_AUT_CTRL Domain0 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R	0x0	DM0_M4_WT_AUT_CTRL Domain0 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R	0x0	DM0_M4_RD_AUT_CTRL Domain0 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R	0x0	DM0_M3_WT_AUT_CTRL Domain0 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R	0x0	DM0_M3_RD_AUT_CTRL Domain0 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R	0x0	DM0_M2_WT_AUT_CTRL Domain0 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R	0x0	DM0_M2_RD_AUT_CTRL Domain0 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R	0x0	DM0_M1_WT_AUT_CTRL Domain0 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R	0x0	DM0_M1_RD_AUT_CTRL Domain0 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R	0x0	DM0_M0_WT_AUT_CTRL Domain0 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R	0x0	DM0_M0_RD_AUT_CTRL Domain0 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

NOTE

- The software can be set up 15 different permission control types, which are set in IOMMU_DM_AUT_CTRL_REG0 ~ 7. The domain0 is a default access control type. The read/write operation of DOMIAN1 ~ 15 is unlimited by default.
- The software needs to set the corresponding permission control domain index of the page table item in the level2 page table entries[7:4]. The default value is 0. Using the domian0 does not control the read/write operation.
- Setting REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All Level2 page table types are covered by the type of REG_ARD_OVWT. The read/write operation is permitted by default.

3.13.6.24 0x00B4 IOMMU Domain Authority Control 1 Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM3_M6_WT_AUT_CTRL Domain3 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM3_M6_RD_AUT_CTRL Domain3 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM3_M5_WT_AUT_CTRL Domain3 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM3_M5_RD_AUT_CTRL Domain3 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM3_M4_WT_AUT_CTRL Domain3 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM3_M4_RD_AUT_CTRL Domain3 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM3_M3_WT_AUT_CTRL Domain3 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM3_M3_RD_AUT_CTRL Domain3 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM3_M2_WT_AUT_CTRL Domain3 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
20	R/W	0x0	DM3_M2_RD_AUT_CTRL Domain3 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM3_M1_WT_AUT_CTRL Domain3 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM3_M1_RD_AUT_CTRL Domain3 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM3_M0_WT_AUT_CTRL Domain3 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM3_M0_RD_AUT_CTRL Domain3 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM2_M6_WT_AUT_CTRL Domain2 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM2_M6_RD_AUT_CTRL Domain2 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM2_M5_WT_AUT_CTRL Domain2 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM2_M5_RD_AUT_CTRL Domain2 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM2_M4_WT_AUT_CTRL Domain2 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	DM2_M4_RD_AUT_CTRL Domain2 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM2_M3_WT_AUT_CTRL Domain2 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM2_M3_RD_AUT_CTRL Domain2 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM2_M2_WT_AUT_CTRL Domain2 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM2_M2_RD_AUT_CTRL Domain2 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM2_M1_WT_AUT_CTRL Domain2 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM2_M1_RD_AUT_CTRL Domain2 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM2_M0_WT_AUT_CTRL Domain2 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM2_M0_RD_AUT_CTRL Domain2 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.25 0x00B8 IOMMU Domain Authority Control 2 Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
29	R/W	0x0	DM5_M6_WT_AUT_CTRL Domain5 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM5_M6_RD_AUT_CTRL Domain5 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM5_M5_WT_AUT_CTRL Domain5 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM5_M5_RD_AUT_CTRL Domain5 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM5_M4_WT_AUT_CTRL Domain5 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM5_M4_RD_AUT_CTRL Domain5 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM5_M3_WT_AUT_CTRL Domain5 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM5_M3_RD_AUT_CTRL Domain5 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM5_M2_WT_AUT_CTRL Domain5 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM5_M2_RD_AUT_CTRL Domain5 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19	R/W	0x0	DM5_M1_WT_AUT_CTRL Domain5 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM5_M1_RD_AUT_CTRL Domain5 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM5_M0_WT_AUT_CTRL Domain5 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM5_M0_RD_AUT_CTRL Domain5 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM4_M6_WT_AUT_CTRL Domain4 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM4_M6_RD_AUT_CTRL Domain4 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM4_M5_WT_AUT_CTRL Domain4 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM4_M5_RD_AUT_CTRL Domain4 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM4_M4_WT_AUT_CTRL Domain4 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM4_M4_RD_AUT_CTRL Domain4 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	DM4_M3_WT_AUT_CTRL Domain4 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM4_M3_RD_AUT_CTRL Domain4 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM4_M2_WT_AUT_CTRL Domain4 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM4_M2_RD_AUT_CTRL Domain4 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM4_M1_WT_AUT_CTRL Domain4 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM4_M1_RD_AUT_CTRL Domain4 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM4_M0_WT_AUT_CTRL Domain4 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM4_M0_RD_AUT_CTRL Domain4 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.26 0x00BC IOMMU Domain Authority Control 3 Register (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM7_M6_WT_AUT_CTRL Domain7 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	DM7_M6_RD_AUT_CTRL Domain7 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM7_M5_WT_AUT_CTRL Domain7 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM7_M5_RD_AUT_CTRL Domain7 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM7_M4_WT_AUT_CTRL Domain7 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM7_M4_RD_AUT_CTRL Domain7 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM7_M3_WT_AUT_CTRL Domain7 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM7_M3_RD_AUT_CTRL Domain7 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM7_M2_WT_AUT_CTRL Domain7 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM7_M2_RD_AUT_CTRL Domain7 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM7_M1_WT_AUT_CTRL Domain7 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
18	R/W	0x0	DM7_M1_RD_AUT_CTRL Domain7 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM7_M0_WT_AUT_CTRL Domain7 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM7_M0_RD_AUT_CTRL Domain7 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM6_M6_WT_AUT_CTRL Domain6 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM6_M6_RD_AUT_CTRL Domain6 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM6_M5_WT_AUT_CTRL Domain6 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM6_M5_RD_AUT_CTRL Domain6 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM6_M4_WT_AUT_CTRL Domain6 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM6_M4_RD_AUT_CTRL Domain6 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM6_M3_WT_AUT_CTRL Domain6 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	DM6_M3_RD_AUT_CTRL Domain6 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM6_M2_WT_AUT_CTRL Domain6 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM6_M2_RD_AUT_CTRL Domain6 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM6_M1_WT_AUT_CTRL Domain6 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM6_M1_RD_AUT_CTRL Domain6 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM6_M0_WT_AUT_CTRL Domain6 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM6_M0_RD_AUT_CTRL Domain6 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.27 0x00C0 IOMMU Domain Authority Control 4 Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM9_M6_WT_AUT_CTRL Domain9 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM9_M6_RD_AUT_CTRL Domain9 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27	R/W	0x0	DM9_M5_WT_AUT_CTRL Domain9 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM9_M5_RD_AUT_CTRL Domain9 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM9_M4_WT_AUT_CTRL Domain9 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM9_M4_RD_AUT_CTRL Domain9 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM9_M3_WT_AUT_CTRL Domain9 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM9_M3_RD_AUT_CTRL Domain9 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM9_M2_WT_AUT_CTRL Domain9 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM9_M2_RD_AUT_CTRL Domain9 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM9_M1_WT_AUT_CTRL Domain9 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM9_M1_RD_AUT_CTRL Domain9 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
17	R/W	0x0	DM9_M0_WT_AUT_CTRL Domain9 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM9_M0_RD_AUT_CTRL Domain9 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM8_M6_WT_AUT_CTRL Domain8 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM8_M6_RD_AUT_CTRL Domain8 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM8_M5_WT_AUT_CTRL Domain8 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM8_M5_RD_AUT_CTRL Domain8 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM8_M4_WT_AUT_CTRL Domain8 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM8_M4_RD_AUT_CTRL Domain8 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM8_M3_WT_AUT_CTRL Domain8 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM8_M3_RD_AUT_CTRL Domain8 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	DM8_M2_WT_AUT_CTRL Domain8 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM8_M2_RD_AUT_CTRL Domain8 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM8_M1_WT_AUT_CTRL Domain8 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM8_M1_RD_AUT_CTRL Domain8 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM8_M0_WT_AUT_CTRL Domain8 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM8_M0_RD_AUT_CTRL Domain8 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.28 0x00C4 IOMMU Domain Authority Control 5 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM11_M6_WT_AUT_CTRL Domain11 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM11_M6_RD_AUT_CTRL Domain11 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM11_M5_WT_AUT_CTRL Domain11 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
26	R/W	0x0	DM11_M5_RD_AUT_CTRL Domain11 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM11_M4_WT_AUT_CTRL Domain11 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM11_M4_RD_AUT_CTRL Domain11 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM11_M3_WT_AUT_CTRL Domain11 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM11_M3_RD_AUT_CTRL Domain11 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM11_M2_WT_AUT_CTRL Domain11 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM11_M2_RD_AUT_CTRL Domain11 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM11_M1_WT_AUT_CTRL Domain11 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM11_M1_RD_AUT_CTRL Domain11 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM11_M0_WT_AUT_CTRL Domain11 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	DM11_M0_RD_AUT_CTRL Domain11 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM10_M6_WT_AUT_CTRL Domain10 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM10_M6_RD_AUT_CTRL Domain10 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM10_M5_WT_AUT_CTRL Domain10 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM10_M5_RD_AUT_CTRL Domain10 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM10_M4_WT_AUT_CTRL Domain10 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM10_M4_RD_AUT_CTRL Domain10 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM10_M3_WT_AUT_CTRL Domain10 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM10_M3_RD_AUT_CTRL Domain10 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM10_M2_WT_AUT_CTRL Domain10 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL5_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	DM10_M2_RD_AUT_CTRL Domain10 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM10_M1_WT_AUT_CTRL Domain10 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM10_M1_RD_AUT_CTRL Domain10 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM10_M0_WT_AUT_CTRL Domain10 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM10_M0_RD_AUT_CTRL Domain10 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.29 0x00C8 IOMMU Domain Authority Control 6 Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	DM13_M6_WT_AUT_CTRL Domain13 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM13_M6_RD_AUT_CTRL Domain13 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM13_M5_WT_AUT_CTRL Domain13 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM13_M5_RD_AUT_CTRL Domain13 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
25	R/W	0x0	DM13_M4_WT_AUT_CTRL Domain13 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
24	R/W	0x0	DM13_M4_RD_AUT_CTRL Domain13 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM13_M3_WT_AUT_CTRL Domain13 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM13_M3_RD_AUT_CTRL Domain13 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM13_M2_WT_AUT_CTRL Domain13 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM13_M2_RD_AUT_CTRL Domain13 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM13_M1_WT_AUT_CTRL Domain13 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM13_M1_RD_AUT_CTRL Domain13 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM13_M0_WT_AUT_CTRL Domain13 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM13_M0_RD_AUT_CTRL Domain13 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
13	R/W	0x0	DM12_M6_WT_AUT_CTRL Domain12 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	DM12_M6_RD_AUT_CTRL Domain12 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM12_M5_WT_AUT_CTRL Domain12 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM12_M5_RD_AUT_CTRL Domain12 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM12_M4_WT_AUT_CTRL Domain12 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM12_M4_RD_AUT_CTRL Domain12 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM12_M3_WT_AUT_CTRL Domain12 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM12_M3_RD_AUT_CTRL Domain12 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM12_M2_WT_AUT_CTRL Domain12 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM12_M2_RD_AUT_CTRL Domain12 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL6_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	DM12_M1_WT_AUT_CTRL Domain12 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	DM12_M1_RD_AUT_CTRL Domain12 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM12_M0_WT_AUT_CTRL Domain12 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM12_M0_RD_AUT_CTRL Domain12 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.30 0x00CC IOMMU Domain Authority Control 7 Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM15_M6_WT_AUT_CTRL Domain15 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation
28	R/W	0x0	DM15_M6_RD_AUT_CTRL Domain15 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
27	R/W	0x0	DM15_M5_WT_AUT_CTRL Domain15 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
26	R/W	0x0	DM15_M5_RD_AUT_CTRL Domain15 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
25	R/W	0x0	DM15_M4_WT_AUT_CTRL Domain15 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
24	R/W	0x0	DM15_M4_RD_AUT_CTRL Domain15 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
23	R/W	0x0	DM15_M3_WT_AUT_CTRL Domain15 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
22	R/W	0x0	DM15_M3_RD_AUT_CTRL Domain15 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
21	R/W	0x0	DM15_M2_WT_AUT_CTRL Domain15 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
20	R/W	0x0	DM15_M2_RD_AUT_CTRL Domain15 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
19	R/W	0x0	DM15_M1_WT_AUT_CTRL Domain15 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation
18	R/W	0x0	DM15_M1_RD_AUT_CTRL Domain15 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
17	R/W	0x0	DM15_M0_WT_AUT_CTRL Domain15 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
16	R/W	0x0	DM15_M0_RD_AUT_CTRL Domain15 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation
15:14	/	/	/
13	R/W	0x0	DM14_M6_WT_AUT_CTRL Domain14 write authority control for Master6 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	DM14_M6_RD_AUT_CTRL Domain14 read authority control for Master6 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	DM14_M5_WT_AUT_CTRL Domain14 write authority control for Master5 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	DM14_M5_RD_AUT_CTRL Domain14 read authority control for Master5 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	DM14_M4_WT_AUT_CTRL Domain14 write authority control for Master4 0: Permits the write operation 1: Prohibits the write operation
8	R/W	0x0	DM14_M4_RD_AUT_CTRL Domain14 read authority control for Master4 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	DM14_M3_WT_AUT_CTRL Domain14 write authority control for Master3 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	DM14_M3_RD_AUT_CTRL Domain14 read authority control for Master3 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	DM14_M2_WT_AUT_CTRL Domain14 write authority control for Master2 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	DM14_M2_RD_AUT_CTRL Domain14 read authority control for Master2 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	DM14_M1_WT_AUT_CTRL Domain14 write authority control for Master1 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL7_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	DM14_M1_RD_AUT_CTRL Domain14 read authority control for Master1 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	DM14_M0_WT_AUT_CTRL Domain14 write authority control for Master0 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	DM14_M0_RD_AUT_CTRL Domain14 read authority control for Master0 0: Permits the read operation 1: Prohibits the read operation

3.13.6.31 0x00D0 IOMMU Domain Authority Overwrite Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DM_AUT_OVWT_ENABLE Domain write/read authority overwrite enable 0: Disabled 1: Enabled
30:14	/	/	/
13	R/W	0x0	M6_WT_AUT_OVWT_CTRL Master6 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
12	R/W	0x0	M6_RD_AUT_OVWT_CTRL Master6 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
11	R/W	0x0	M5_WT_AUT_OVWT_CTRL Master5 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
10	R/W	0x0	M5_RD_AUT_OVWT_CTRL Master5 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
9	R/W	0x0	M4_WT_AUT_OVWT_CTRL Master4 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	M4_RD_AUT_OVWT_CTRL Master4 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
7	R/W	0x0	M3_WT_AUT_OVWT_CTRL Master3 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
6	R/W	0x0	M3_RD_AUT_OVWT_CTRL Master3 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
5	R/W	0x0	M2_WT_AUT_OVWT_CTRL Master2 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
4	R/W	0x0	M2_RD_AUT_OVWT_CTRL Master2 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
3	R/W	0x0	M1_WT_AUT_OVWT_CTRL Master1 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
2	R/W	0x0	M1_RD_AUT_OVWT_CTRL Master1 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation
1	R/W	0x0	M0_WT_AUT_OVWT_CTRL Master0 write authority overwrite control 0: Permits the write operation 1: Prohibits the write operation
0	R/W	0x0	M0_RD_AUT_OVWT_CTRL Master0 read authority overwrite control 0: Permits the read operation 1: Prohibits the read operation

NOTE

Setting the REG_ARD_OVWT can mask the Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All the property of Level2 are covered by the property defined in REG_ARD_OVWT. Allow read and write for all by default.

3.13.6.32 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	R/W	0x0	DBG_PF_L2_PAGE_TABLE_INVALID_EN Debug or Prefetch, the interrupt enable bit for fetching the invalid level1 page table in TLB. 0: Masks interrupt 1: Enables interrupt
19	R/W	0x0	DBG_PF_PC_L1_PAGE_TABLE_INVALID_EN Debug or Prefetch is hit, the interrupt enable bit for fetching the invalid level1 page table in PTW Cache. 0: Masks interrupt 1: Enables interrupt
18	R/W	0x0	DBG_PF_DRAM_L1_PAGE_TABLE_INVALID_EN Debug or Prefetch is not hit, the interrupt enable bit for fetching the invalid level1 page table in DRAM. 0: Masks interrupt 1: Enables interrupt
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN Micro TLB6 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt

Offset: 0x0100			Register Name: IOMMU_INT_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 authority invalid interrupt enable bit. 0: Masks interrupt 1: Enables interrupt

NOTE

- Due to the invalid page table and authority errors, one or more devices in the system will not work properly.
- The authority error usually occurs in Micro TLB. This error generates the interrupt, and waits for the software processing.
- While the invalid page table usually occurs in Macro TLB. This error does not affect the access of other devices. So the error page table needs to be returned in the same way, but it should not be written into TLB at all levels.

3.13.6.33 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR Level2 page table invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 authority invalid interrupt clear bit. 0: Invalid operation 1: Clears interrupt

3.13.6.34 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 authority invalid interrupt status bit 0: Interrupt does not occur or interrupt is cleared 1: Interrupt occurs

3.13.6.35 0x0110 IOMMU Interrupt Error Address 0 Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: IOMMU_INT_ERR_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR0 The virtual address, it makes Micro TLB0 be interrupted

3.13.6.36 0x0114 IOMMU Interrupt Error Address 1 Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR1 The virtual address, it makes Micro TLB1 be interrupted

3.13.6.37 0x0118 IOMMU Interrupt Error Address 2 Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR2 The virtual address, it makes Micro TLB2 be interrupted

3.13.6.38 0x011C IOMMU Interrupt Error Address 3 Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR_REG3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR3 The virtual address, it makes Micro TLB3 be interrupted

3.13.6.39 0x0120 IOMMU Interrupt Error Address 4 Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR4 The virtual address, it makes Micro TLB4 be interrupted

3.13.6.40 0x0124 IOMMU Interrupt Error Address 5 Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR5 The virtual address, it makes Micro TLB5 be interrupted

3.13.6.41 0x0128 IOMMU Interrupt Error Address 6 Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR6 The virtual address, it makes Micro TLB6 be interrupted

3.13.6.42 0x0130 IOMMU Interrupt Error Address 7 Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR7 The virtual address, it makes L1 page table be interrupted

3.13.6.43 0x0134 IOMMU Interrupt Error Address 8 Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR_REG8
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR8 The virtual address, it makes L2 page table be interrupted

3.13.6.44 0x0150 IOMMU Interrupt Error Data 0 Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA0 The corresponding page table of the virtual address that made Micro TLB0 be interrupted

3.13.6.45 0x0154 IOMMU Interrupt Error Data 1 Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA1 The corresponding page table of the virtual address that made Micro TLB1 be interrupted

3.13.6.46 0x0158 IOMMU Interrupt Error Data 2 Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA2 The corresponding page table of the virtual address that made Micro TLB2 be interrupted

3.13.6.47 0x015C IOMMU Interrupt Error Data 3 Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA3 The corresponding page table of the virtual address that made Micro TLB3 be interrupted

3.13.6.48 0x0160 IOMMU Interrupt Error Data 4 Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA4 The corresponding page table of the virtual address that made Micro TLB4 be interrupted

3.13.6.49 0x0164 IOMMU Interrupt Error Data 5 Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA5 The corresponding page table of the virtual address that made Micro TLB5 be interrupted

3.13.6.50 0x0168 IOMMU Interrupt Error Data 6 Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA6 The corresponding page table of the virtual address that made Micro TLB6 be interrupted

3.13.6.51 0x0170 IOMMU Interrupt Error Data 7 Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA7 The corresponding page table of the virtual address that made L1 page table be interrupted

3.13.6.52 0x0174 IOMMU Interrupt Error Data 8 Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_DATA8 The corresponding page table of the virtual address that made L2 page table be interrupted

3.13.6.53 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L1PG_INT L1 page table interrupted caused by the Debug Mode address translation.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT L1 page table interrupted caused by the Master6 address translation.
5	R	0x0	MASTER5_L1PG_INT L1 page table interrupted caused by the Master5 address translation.
4	R	0x0	MASTER4_L1PG_INT L1 page table interrupted caused by the Master4 address translation.
3	R	0x0	MASTER3_L1PG_INT L1 page table interrupted caused by the Master3 address translation.
2	R	0x0	MASTER2_L1PG_INT L1 page table interrupted caused by the Master2 address translation.
1	R	0x0	MASTER1_L1PG_INT L1 page table interrupted caused by the Master1 address translation.

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	Read/Write	Default/Hex	Description
0	R	0x0	MASTER0_L1PG_INT L1 page table interrupted caused by the Master0 address translation.

3.13.6.54 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	DBG_MODE_L2PG_INT L2 page table interrupted caused by the Debug Mode address translation.
30:7	/	/	/
6	R	0x0	MASTER6_L2PG_INT L2 page table interrupted caused by the Master6 address translation.
5	R	0x0	MASTER5_L2PG_INT L2 page table interrupted caused by the Master5 address translation.
4	R	0x0	MASTER4_L2PG_INT L2 page table interrupted caused by the Master4 address translation.
3	R	0x0	MASTER3_L2PG_INT L2 page table interrupted caused by the Master3 address translation.
2	R	0x0	MASTER2_L2PG_INT L2 page table interrupted caused by the Master2 address translation.
1	R	0x0	MASTER1_L2PG_INT L2 page table interrupted caused by the Master1 address translation.
0	R	0x0	MASTER0_L2PG_INT L2 page table interrupted caused by the Master0 address translation.

3.13.6.55 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VA Read/write virtual address

3.13.6.56 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA_DATA Data of read/write virtual address

3.13.6.57 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MODE_ESL 0: Prefetch 1: Debug Mode It is used to choose the prefetch mode or the debug mode.
30:9	/	/	/
8	R/W	0x0	VA_CONFIG 0: Read operation 1: Write operation
7:1	/	/	/
0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation completes 1: Start After the operation completes, the bit can be cleared to 0 automatically.

Read operation process:

1. Write IOMMU_VA _REG[31:0];
2. Write IOMMU_VA_CONFIG _REG[8] to 0;
3. Write IOMMU_VA_CONFIG _REG[0] to 1 to start the read-process;
4. Query IOMMU_VA_CONFIG _REG[0] until it is 0;
5. Read IOMMU_VA_DATA _REG[31:0];

Write operation process:

1. Write IOMMU_VA _REG[31:0];
2. Write IOMMU_VA_DATA _REG[31:0];
3. Write IOMMU_VA_CONFIG _REG[8] to 1；
4. Write IOMMU_VA_CONFIG _REG[0] to 1 to start the read-process;
5. Query IOMMU_VA_CONFIG _REG[0] until it is 0.

3.13.6.58 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disables statistical function 1: Enables statistical function

3.13.6.59 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation completes 1: Clears the counter data After the operation completes, the bit can be cleared to 0 automatically.

3.13.6.60 0x0230 IOMMU PMU Access Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW0 Record the total number of Micro TLB0 access, lower 32-bit register.

3.13.6.61 0x0234 IOMMU PMU Access High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record the total number of Micro TLB0 access, higher 11-bit register.

3.13.6.62 0x0238 IOMMU PMU Hit Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW0 Record the total number of Micro TLB0 hit, lower 32-bit register.

3.13.6.63 0x023C IOMMU PMU Hit High 0 Register (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record the total number of Micro TLB0 hit, higher 11-bit register.

3.13.6.64 0x0240 IOMMU PMU Access Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW1 Record the total number of Micro TLB1 access, lower 32-bit register.

3.13.6.65 0x0244 IOMMU PMU Access High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record the total number of Micro TLB1 access, higher 11-bit register.

3.13.6.66 0x0248 IOMMU PMU Hit Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW1 Record the total number of Micro TLB1 hit, lower 32-bit register.

3.13.6.67 0x024C IOMMU PMU Hit High 1 Register (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record the total number of Micro TLB1 hit, higher 11-bit register.

3.13.6.68 0x0250 IOMMU PMU Access Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW2 Record the total number of Micro TLB2 access, lower 32-bit register.

3.13.6.69 0x0254 IOMMU PMU Access High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record the total number of Micro TLB2 access, higher 11-bit register.

3.13.6.70 0x0258 IOMMU PMU Hit Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW2 Record the total number of Micro TLB2 hit, lower 32-bit register.

3.13.6.71 0x025C IOMMU PMU Hit High 2 Register (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record the total number of Micro TLB2 hit, higher 11-bit register.

3.13.6.72 0x0260 IOMMU PMU Access Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW3 Record the total number of Micro TLB3 access, lower 32-bit register.

3.13.6.73 0x0264 IOMMU PMU Access High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record the total number of Micro TLB3 access, higher 11-bit register.

3.13.6.74 0x0268 IOMMU PMU Hit Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW3 Record the total number of Micro TLB3 hit, lower 32-bit register.

3.13.6.75 0x026C IOMMU PMU Hit High 3 Register (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record the total number of Micro TLB3 hit, higher 11-bit register.

3.13.6.76 0x0270 IOMMU PMU Access Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW4 Record the total number of Micro TLB4 access, lower 32-bit register.

3.13.6.77 0x0274 IOMMU PMU Access High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record the total number of Micro TLB4 access, higher 11-bit register.

3.13.6.78 0x0278 IOMMU PMU Hit Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW4 Record the total number of Micro TLB4 hit, lower 32-bit register.

3.13.6.79 0x027C IOMMU PMU Hit High 4 Register (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record the total number of Micro TLB4 hit, higher 11-bit register.

3.13.6.80 0x0280 IOMMU PMU Access Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW5 Record the total number of Micro TLB5 access, lower 32-bit register.

3.13.6.81 0x0284 IOMMU PMU Access High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record the total number of Micro TLB5 access, higher 11-bit register.

3.13.6.82 0x0288 IOMMU PMU Hit Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW5 Record the total number of Micro TLB5 hit, lower 32-bit register.

3.13.6.83 0x028C IOMMU PMU Hit High 5 Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record the total number of Micro TLB5 hit, higher 11-bit register.

3.13.6.84 0x0290 IOMMU PMU Access Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW6 Record the total number of Micro TLB6 access, lower 32-bit register.

3.13.6.85 0x0294 IOMMU PMU Access High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record the total number of Micro TLB6 access, higher 11-bit register.

3.13.6.86 0x0298 IOMMU PMU Hit Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW6 Record the total number of Micro TLB6 hit, lower 32-bit register.

3.13.6.87 0x029C IOMMU PMU Hit High 6 Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record the total number of Micro TLB6 hit, higher 11-bit register.

3.13.6.88 0x02D0 IOMMU PMU Access Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW7 Record the total number of Macro TLB access, lower 32-bit register.

3.13.6.89 0x02D4 IOMMU PMU Access High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record the total number of Macro TLB access, higher 11-bit register.

3.13.6.90 0x02D8 IOMMU PMU Hit Low 7 Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW7_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW7 Record the total number of Macro TLB hit, lower 32-bit register.

3.13.6.91 0x02DC IOMMU PMU Hit High 7 Register (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH7_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record the total number of Macro TLB hit, higher 11-bit register.

3.13.6.92 0x02E0 IOMMU PMU Access Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ACCESS_LOW8 Record the total number of PTW Cache access, lower 32-bit register.

3.13.6.93 0x02E4 IOMMU PMU Access High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH8 Record the total number of PTW Cache access, higher 11-bit register.

3.13.6.94 0x02E8 IOMMU PMU Hit Low 8 Register (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW8_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_HIT_LOW8 Record the total number of PTW Cache hit, lower 32-bit register.

3.13.6.95 0x02EC IOMMU PMU Hit High 8 Register (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH8_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record the total number of PTW Cache hit, higher 11-bit register.

3.13.6.96 0x0300 IOMMU Total Latency Low 0 Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ TL_LOW0 Record the total latencies of Master0, lower 32-bit register.

3.13.6.97 0x0304 IOMMU Total Latency High 0 Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH0_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record the total latencies of Master0, higher 18-bit register.

3.13.6.98 0x0308 IOMMU Max Latency 0 Register (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML0 Record the maximum latency of Master0.

3.13.6.99 0x0310 IOMMU Total Latency Low 1 Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ TL_LOW1 Record the total latencies of Master1, lower 32-bit register.

3.13.6.100 0x0314 IOMMU Total Latency High 1 Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH1_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record the total latencies of Master1, higher 18-bit register.

3.13.6.101 0x0318 IOMMU Max Latency 1 Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML1 Record the maximum latency of Master1.

3.13.6.102 0x0320 IOMMU Total Latency Low 2 Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ TL_LOW2 Record the total latencies of Master2, lower 32-bit register.

3.13.6.103 0x0324 IOMMU Total Latency High 2 Register (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH2_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record the total latencies of Master2, higher 18-bit register.

3.13.6.104 0x0328 IOMMU Max Latency 2 Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML2 Record the maximum latency of Master2.

3.13.6.105 0x0330 IOMMU Total Latency Low 3 Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ TL_LOW3 Record the total latencies of Master3, lower 32-bit register.

3.13.6.106 0x0334 IOMMU Total Latency High 3 Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: IOMMU_PMU_TL_HIGH3_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record the total latencies of Master3, higher 18-bit register.

3.13.6.107 0x0338 IOMMU Max Latency 3 Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML3_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML3 Record the maximum latency of Master3.

3.13.6.108 0x0340 IOMMU Total Latency Low 4 Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW4 Record the total latencies of Master4, lower 32-bit register.

3.13.6.109 0x0344 IOMMU Total Latency High 4 Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH4_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record the total latencies of Master4, higher 18-bit register.

3.13.6.110 0x0348 IOMMU Max Latency 4 Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML4_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML4 Record the maximum latency of Master4.

3.13.6.111 0x0350 IOMMU Total Latency Low 5 Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW5 Record the total latencies of Master5, lower 32-bit register.

3.13.6.112 0x0354 IOMMU Total Latency High 5 Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH5_REG
Bit	Read/Write	Default/Hex	Description
17:0	R	0x0	PMU_TL_HIGH5 Record the total latencies of Master5, higher 18-bit register.

3.13.6.113 0x0358 IOMMU Max Latency 5 Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML5_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML5 Record the maximum latency of Master5.

3.13.6.114 0x0360 IOMMU Total Latency Low 6 Register (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW6 Record the total latencies of Master6, lower 32-bit register.

3.13.6.115 0x0364 IOMMU Total Latency High 6 Register (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH6_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record the total latencies of Master6, higher 18-bit register.

3.13.6.116 0x0368 IOMMU Max Latency 6 Register (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: IOMMU_PMU_ML6_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML6 Record the maximum latency of Master6.

3.14 RTC

3.14.1 Overview

The Real Time Clock (RTC) is used to implement time counter and timing wakeup functions. The RTC can display the year, month, day, week, hour, minute, and second in real time. The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing the power-off information
- Multiple special registers for recording the BROM information

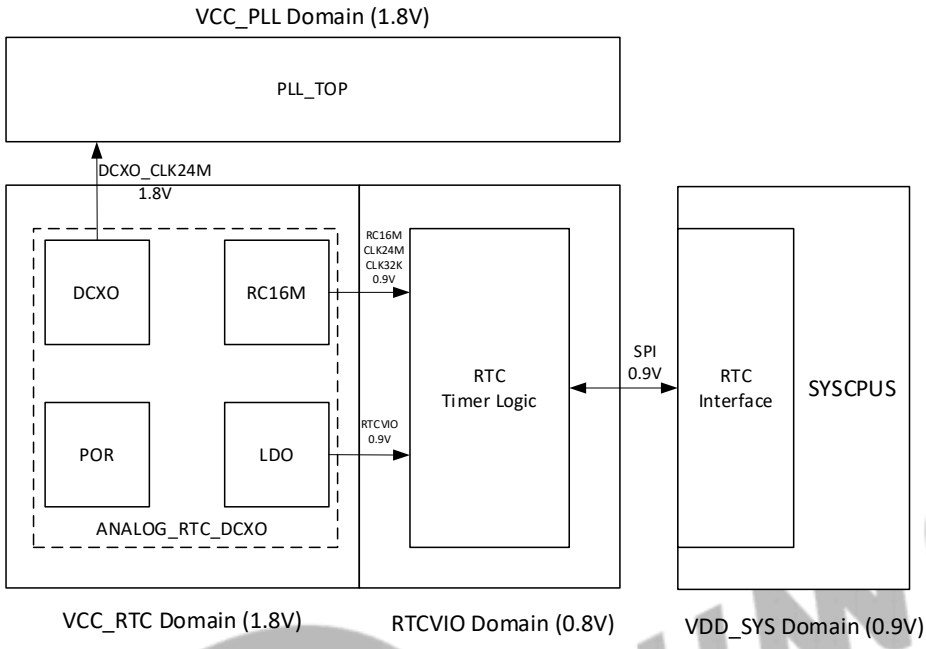
CAUTION

The register configuration of RTC is AHB bus, it only can support word operation, not byte operation and half-word operation.

3.14.2 Block Diagram

The following figure shows the block diagram of the RTC.

Figure 3-41 RTC Block Diagram



3.14.3 Functional Description

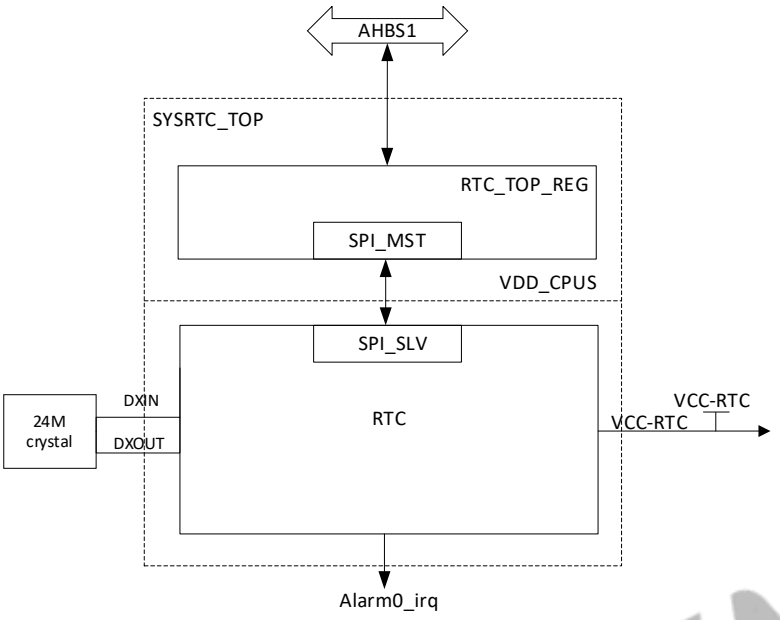
3.14.3.1 External Signals

Table 3-18 RTC External Signals

Signal	Description	Type
DXIN	24MHz oscillator input	I
DXOUT	24MHz oscillator output	O
VCC-RTC	RTC high voltage, generated via external power	IO
GND	Ground	IO

3.14.3.2 Typical Application

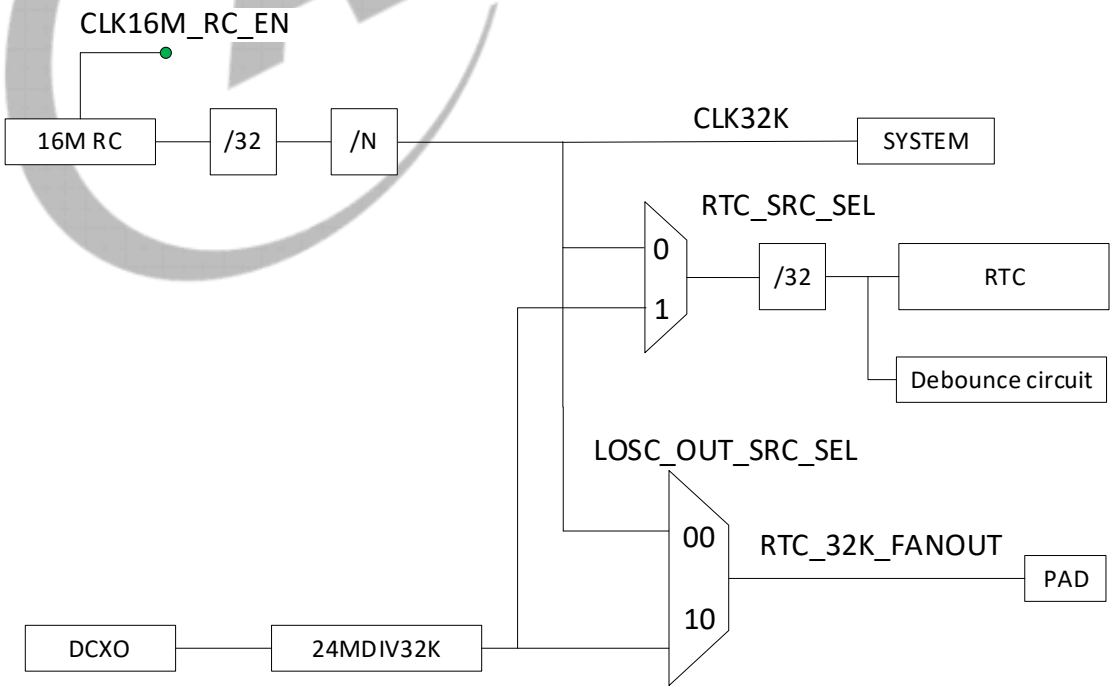
Figure 3-42 RTC Application Diagram



3.14.3.3 Clock Tree

The following figure shows the clock tree of the RTC.

Figure 3-43 RTC Clock Tree



RTC

The clock sources of RTC can be selected by related switches, including 32K divided by internal 16 MHz RC, and 32K divided by external DCXO.

System 32K

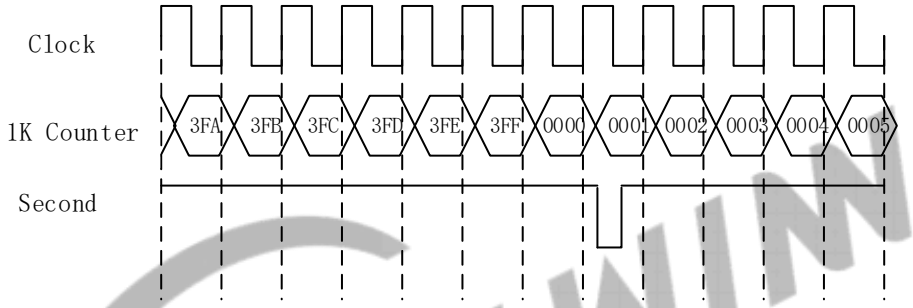
The clock source of system 32K is from 32K divided by the internal 16 MHz RC.

RTC_32K_FANOUT

The clock source of RTC_32K_FANOUT can select CLK32K or 32K divided by external DCXO.

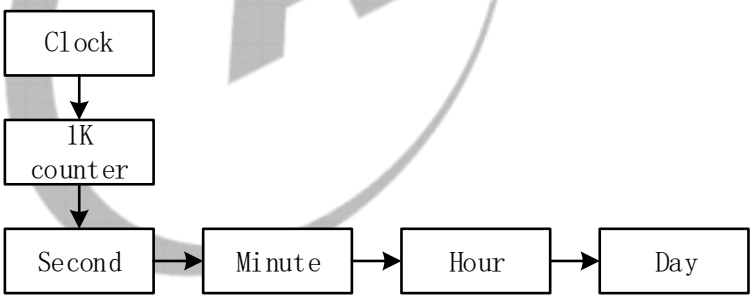
3.14.3.4 Real Time Clock

Figure 3-44 RTC Counter



The 1K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1K counter starts to count again from 0, and the second counter adds 1. The step structure of 1 kHz counter is as follows.

Figure 3-45 RTC 1 kHz Counter Step Structure



According to above implementation, the changing range of each counter is as follows.

Table 3-19 RTC Counter Changing Range

Counter	Range
Second	0 to 59
Minute	0 to 59
Hour	0 to 23
Day	0 to 65535 (The year, month, day need be transformed by software according to day counter)

CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

3.14.3.5 Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC need set a new scheduled time, the next interrupt can be generated.

3.14.3.6 Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.14.3.7 VDD-RTC

The RTC module has a LDO, the input source of the LDO is VCC_RTC, the output of the LDO is RTC_VIO, the value of RTC_VIO is adjustable, the RTC_VIO is mainly used for internal digital logic.

3.14.3.8 RC Calibration Usage Scenario

Power-on: Select non-accurate 32K divided by internal RC.

Normal scenario: Select 32K divided by internal RC.

Standby or power-off scenario: Select 32K divided by internal RC.

3.14.4 Programming Guidelines

3.14.4.1 RTC Calendar

1. Write time initial value: Write the current time to RTC_DAY_REG and RTC_HH_MM_SS_REG.
2. After updated time, the RTC restarts to count again. The software can read the current time anytime.

NOTE

The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.

Ensure the bit[8:7] of LOSC_CTRL_REG is 0 before the next time configuration is performed.

Here is the basic code samples.

For example: set time to 21st, 07:08:09 and read it.

```
RTC_DAY_REG = 0x00000015;
RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)
Read (RTC_DAY_REG);
Read (RTC_HH_MM_SS_REG);
```

3.14.4.2 Alarm0

1. Enable alram0 interrupt by writing ALARM0_IRQ_EN.
2. Set the counter comparator, write the count-down day, hour, minute, second number to ALARM0_DAY_SET_REG and ALARM0_HH-MM-SS_SET_REG.
3. Enable alarm0 function by writing ALARM0_ENABLE_REG, then the software can query alarm count value in real time by ALARM0_DAY_SET_REG and ALARM0_HH-MM-SS_SET_REG. When the setting time reaches, ALARM0_IRQ_STA_REG is set to 1 to generate interrupt.
4. After enter the interrupt process, write ALARM0_IRQ_STA_REG to clear the interrupt pending, and execute the interrupt process.
5. Resume the interrupt and continue to execute the interrupted process.
6. The power-off wakeup is generated via SoC hardware and PMIC, the software only needs to set the pending condition of alarm0, and set ALARM_CONFIG_REG to 1.

3.14.5 Register List

Module Name	Base Address
RTC	0x0709 0000

Register Name	Offset	Description
VDD_RTC Power Domain		
LOSC_CTRL_REG	0x0000	LOSC Control Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MrM_SS_SET_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_DAY_SET_REG	0x0020	Alarm 0 Day Set Register
ALARM0_HH_MM_SS_SET_REG	0x0024	Alarm 0 Hour-Minute-Second Set Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register

Register Name	Offset	Description
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
TIMER_SOFT_RST_REG	0x0040	Timer Software Reset Register
ALARM0_CONFIG_REG	0x0050	Alarm 0 Configuration Register
CLK32K_FOUT_CTR_REG	0x0060	CLK32K Fanout Control register
GP_DATA_REGn	0x0100+N*0x0004 (N=0~7)	General Purpose Register
FBOOT_INFO_REG0	0x0120	Fast Boot Info Register0
FBOOT_INFO_REG1	0x0124	Fast Boot Info Register1
XO_CTRL_WP_REG	0x015C	XO Control Write Protect Register
XO_CTRL_REG	0x0160	XO Control Register
VDD_RTC_REG	0x0190	VDD RTC Regulation Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_OFF_GATING_CTRL_REG	0x01F4	VDD Off Gating Control Register
SP_STDBY_FLAG_REG	0x1F8	Super Standby Flag Register
SP_STDBY_SOFT_ENTRY_REG	0x1FC	Super Standby Software Entry Register
USB_STBY_CTRL_REG	0x0200	USB Standby Control Register
EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
RST_DLY_SEL_REG	0x0234	Reset Delay Select Register
PMC_BYP_ST_REG	0x0238	PMC Bypass Status Register
VDD_SYS Power Domain		
RTC_SPI_CLK_CTRL_REG	0x0310	RTC SPI Clock Control Register

3.14.6 Register Description

3.14.6.1 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	RTC_HHMMSS_ACCE RTC Hour Minute Second access After writing the RTC HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS Register, the RTC HH-MM-SS Register will be refreshed for at most one second. **Note: Make sure that the bit is 0 for time configuration.**

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	RTC_DAY_ACCE RTC DAY access After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second. **Note: Make sure that the bit is 0 for time configuration.**
6:0	/	/	/

NOTE

If the bit[8:7] of LOSC_CTRL_REG is set, the RTC HH-MM-SS, DD and ALARM DD-HH-MM-SS register cannot be written.

3.14.6.2 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL Internal OSC 32K Clock Prescalar value N. The clock output = Internal RC/32/N. 00000: 1 00001: 2 00002: 3 ..... 11111: 32

3.14.6.3 0x0010 RTC Year-Month-DAY Register (Default Value: UDF)

Offset:0x0010			Register Name: RTC_DAY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	UDF	DAY Set Day Range from 0 to 65535.

3.14.6.4 0x0014 RTC Hour-Minute-Second Register (Default Value: UDF)

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Set hour Range from 0 to 23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Set minute Range from 0 to 59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Set second Range from 0 to 59.

3.14.6.5 0x0020 Alarm 0 Day Setting Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: ALARM0_DAY_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is based on Day.

3.14.6.6 0x0024 Alarm0 Hour-Minute-Second Set Register (Default Value: 0x0000_0000)

Offset:0x0024			Register Name: ALARM0_HH_MM_SS_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Current hour Range from 0 to 23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Current minute Range from 0 to 59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Current second Range from 0 to 59.

3.14.6.7 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable 0: Disable 1: Enable

3.14.6.8 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.14.6.9 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 IRQ enable is set to 1, the pending bit will be sent to the interrupt controller.

3.14.6.10 0x0040 Timer Software Reset Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: TIMER_SOFT_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	Key Filed. Write Protect. To configure Timer soft reset write protection on software, first configure bits [31:16] to 0x16AA and write 0xAA16_XXX before writing bits [15:0].
15:1	/	/	/

Offset: 0x0040			Register Name: TIMER_SOFT_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/WAC	0x0	TIMER_SOFT_RST Timer RTC logic software reset. 0: No-effect 1: Reset **Note: Make sure that the bit is 0 for time configuration.**

3.14.6.11 0x0050 Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.14.6.12 0x0060 32K Fanout Control Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: 32K_FOUT_CTRL_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HOSC_TO_32K_DIVIDER_ENABLE HOSC to 32k divider enable 0: Disable the HOSC 24M to 32K divider circuit 1: Enable the HOSC 24M to 32K divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL LOSC output source select 00: RTC_32K (select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01: Reserved 10: HOSC divided 32K
0	R/W	0x0	32K_FANOUT_GATING LOSC out gating enable Configuration of LOSC output, and there is no LOSC output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

3.14.6.13 0x0100+N*0x0004 General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0 to 7)			Register Name: GP_DATA_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	GP_DATA Data [31:0]

NOTE

General purpose register 0 to 7 value can be stored if the RTC-VIO is larger than 0.7 V.

3.14.6.14 0x0120 Fast Boot Information Register0 (Default Value: 0x0000_0000)

Offset:0x0120			Register Name: FBOOT_INFO_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FBOOT_INFO0 Fast Boot info Fast Boot Information 0, refer to section 3.5 BROM System

3.14.6.15 0x0124 Fast Boot Information Register1 (Default Value: 0x0000_0000)

Offset:0x0124			Register Name: FBOOT_INFO_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FBOOT_INFO1 Fast Boot info Fast Boot Information 1, refer to section 3.5 BROM System.

3.14.6.16 0x015C XO Control Write Protect Register (Default Value:0x0000_0000)

Offset: 0x015C			Register Name: XO_CTRL_WP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	Key Field. Write protection for XO_CTRL_REG(0x0160). Write this field as 0x16AA before configuring XO_CTRL_REG(0x0160) and this field will be automatically cleared to 0 after XO_CTRL_REG is configured.

3.14.6.17 0x0160 XO Control Register (Default Value: 0x883F_10F7)

Offset:0x0160			Register Name: XO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CLK_REQ_ENB Clock REQ enable 0: Enable DCXO wake up function 1: Disable DCXO wake up function
30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value The capacity cell is 55 fF.
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: For external CLK input mode 1: For normal mode
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO RFCLK enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5 pF, 0x1 for 10 pF, 0x2 for 15 pF, 0x3 for 20 pF.
3	/	/	/
2	R/W	0x1	RSTO_DLY_SEL For Debug Use Only. It cannot configure to 0 in normal state.
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable

Offset:0x0160			Register Name: XO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x1	CLK16M_RC_EN 1: Enable 0: Disable The related register configuration is necessary to ensure the reset debounce circuit has a stable clock source. The first time SoC starts up, by default, the reset debounce circuit of SoC uses 32K divided by RC16M. In power-off, software reads the related bit to ensure whether EXT32K is working normally, if it is normal, first switch the clock source of debounce circuit to EXT32K, then close RC16M. Without EXT32K scenario or external RTC scenario, software confirms firstly whether EXT32K is working normally before switching, or software does not close RC16M.

3.14.6.18 0x0190 RTC_VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name: RTC_VIO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	V_SEL VDD Select 0: Resistance divider 1: Band gap
3	/	/	/
2:0	R/W	0x4	RTC_VIO_REGU RTC_VIO Voltage Select The RTC-VIO is provided power for RTC digital part. These bits are useful for regulating the RTC_VIO from 0.65 V to 1.3 V. 000: 1.0 V 001: 0.65 V (the configuration can cause RTC reset) 010: 0.7 V 011: 0.8 V 100: 0.9 V 101: 1.1 V 110: 1.2 V 111: 1.3 V

3.14.6.19 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0			Register Name: IC_CHARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	KEY_FIELD Key Field The field should be written as 0x16AA. Writing any other value in this field aborts the write-operation.
15:0	R/W	0x0	ID_DATA Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

3.14.6.20 0x01F4 VDD Off Gating Control Register (Default Value: 0x0000_0021)

Offset:0x01F4			Register Name: VDD_OFF_GATING_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit 15 can be configured.
15	WAC	0x0	PWROFF_GAT_RTC_CFG (For Debug Use Only) Power off gating control signal When use VDD_SYS to RTC isolation software control, write this bit to 1. It will only be cleared by resetb release.
14:12	/	/	/
11:4	R/W	0x2	VCCIO_DET_SPARE Bit [7:5]: Reserved, default=0 Bit [4]: Bypass debounce circuit, defaule=0 Bit [3]: Enable control, defaule=0 0: Disable VCC-IO detection 1: Force the detection output Bit [2:0]: Gear adjustment 000: Detection threshold is 2.5 V 001: Detection threshold is 2.6 V 010: Detection threshold is 2.7 V (default) 011: Detection threshold is 2.8 V 100: Detection threshold is 2.9 V 101: Detection threshold is 3 V 110: N/A 111: N/A
3:1	/	/	/
0	R/W	0x1	VCCIO_DET_BYPASS_EN 0: not bypass 1: bypass

3.14.6.21 0x01F8 Super Standby Flag Register (Default Value: 0x0000_0000)

Offset: 0x01F8			Register Name: SP_STDBY_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SP_STDBY_FLAG. Key Field. Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only fellow the appropriate process, the super standby flag can be written in the lower 16 bits.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA. When system is turned on, the value in the Super Standby Flag Register low 16 bits should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written with 0x16AA at first. Then, software programmer must write 0xAA16XXXX in the Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID.

3.14.6.22 0x01FC Super Standby Software Entry Register (Default Value: 0x0000_0000)

Offset: 0x01FC			Register Name: SP_STDBY_SOFT_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	SP_STBY_SW_ENTRY_ADDR. CPU software entry register when acting from supper standby.

3.14.6.23 0x0200 USB Standby Control Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: USB_STBY_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	USB POWER OFF GATING Gating the VDD_SYS to VDD_USB signal in USB standby mode. It must be set to 1 before entering USB standby mode and set to 0 when exiting Normal mode. 0: disable 1: enable
15:9	/	/	/

Offset: 0x0200			Register Name: USB_STBY_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	USB_STBY_IRQ_POWER_OFF_GATING Gating the USB standby IRQ signal to RTC module when USB module is power off. It must be set to 1 in USB Standby mode and must set to 0 in Other mode. 0: disable 1: enable
7:5	/	/	/
4	R/W	0x0	USB_STBY_IRQ_OUTPUT_GATING Mask the USB standby IRQ output to NMI pad. It must be set to 1 in USB standby mode and set to 0 in other mode. 0: disable IRQ output 1: enable IRQ output
3:0	/	/	/

3.14.6.24 0x0204 Efuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset:0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EFUSE_1.8V_POWER_SWITCH_CONTROL 1: Open power switch 0: Close power switch

3.14.6.25 0x0234 Reset Delay Select Register (Default Value:0x0000_0013)

Offset: 0x0234			Register Name: RST_DLY_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DCXO_DLY_DONE Output a stable flag bit after DCXO is enabled 0: Close 1: Open
30:7	/	/	/

Offset: 0x0234			Register Name: RST_DLY_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
6:4	R/W	0x1	PWRON_DLY_SEL_CFG Options for the time waited between stable power and release from reset: 000: 4ms 001: 8ms 010: 16ms 011: 32ms 100:64ms
3:2	/	/	/
1:0	R/W	0x3	DCXO_DLY_SEL_CFG Options for the time waited before DCXO turning stable after being enabled: 00: 1ms 01: 2ms 10: 3ms 11: 4ms

3.14.6.26 0x0238 PMC Bypass Status Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: PMC_BYP_ST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	Key Field. To configure PMC status write protection on software, first configure bits [31:16] to 0x16AA and write 0xAA16_XXX before writing bits [15:0].
15:2	/	/	/
1	R/W	0x0	PMC_BYP_PULL PMC Bypass pull register. 0: NO PULL-UP 1: PULL-UP
0	R	0x0	PMC_BYP_ST PMC bypass status 0: Bypass 1: PMC

3.14.6.27 0x0310 RTC SPI Clock Control Register (Default Value: 0x0000_0009)

Offset:0x0310			Register Name: RTC_SPI_CLK_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RTC REG CFG SPI Clock Gating 0: Gating 1: Not Gating Before configurating RTC register, the clock divider of SPI needs be configured firstly, then clock gating needs be enabled. **Note: Frequency division and clock gating can not be set at the same time.**
30:5	/	/	/
4:0	R/W	0x9	RTC REG CFG SPI Clock Divider: M Actual SPI Clock = AHBS1/(M+1), (0 to 15) The default frequency of AHBS1 is 200 MHz, and the default frequency of SPI Clock is 20 MHz. **Note: The SPI clock can not exceed 50 MHz, or else the RTC register may be abnormal.**

3.15 Message Box

3.15.1 Overview

The Message Box (MSGBOX) provides the interrupt communication mechanism for the on-chip processor.

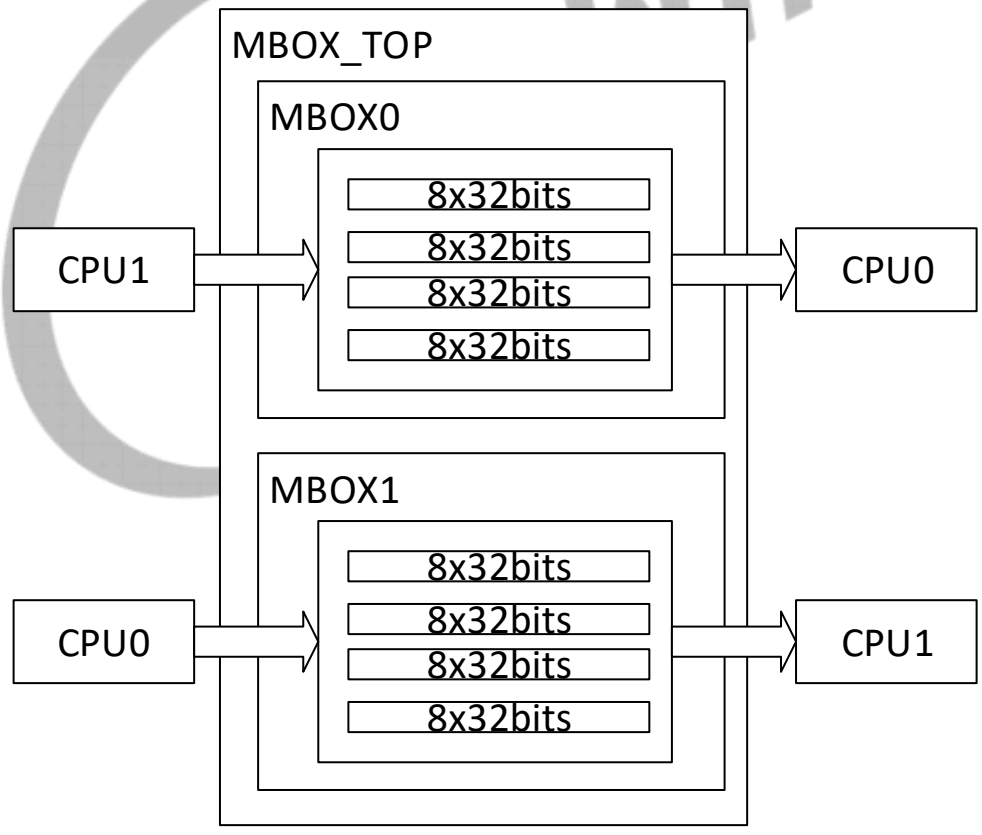
The MSGBOX has the following features:

- Supports communication between two CPUs through one-way channels. Each CPU has one MSGBOX and can only read or write in one communication.
  - CPU 0: ARM CPU
  - CPU 1: RISC CPU
- Supports four channels between the two CPUs and the FIFO depth of the channels is 8 x 32 bits
- Supports interrupts

3.15.2 Block Diagram

The following figure shows the block diagram of the message box.

Figure 3-46 Message Box Block Diagram



For MSGBOX0, CPU1: write; CPU0: read
For MSGBOX1, CPU0: write; CPU1: read

The two message boxes use the same AHB interface.

- Select MSG0 and MSG1 through the bit[11:10].
- Select the CPU used for sending messages through the bit[9:8].
- Visit a register with the fixed address using the FIFO method.
- Use the master ID to distinguish the read and write function. This design sets the user1 as write and the user0 as read.

In the MSGBOX0, RISC CPU is designed for writing, and A7 is designed for reading. In the MSGBOX1, A7 is designed for writing, and RISC CPU is designed for reading. In this way, two CPUs can send message to each other. Each CPU is assigned four channels. The software can make two of them as normal and another two as secure. The two normal channels can be configured as a synchronous box, and the other two channels are working as an asynchronous box.

3.15.3 Functional Descriptions

3.15.3.1 Clock and Reset

The MSGBOX is on AHB. Before accessing the MSGBOX registers, you need to de-assert the MSGBOX reset signal and then open the MSGBOX gating signal.

3.15.3.2 Typical Application

Two different CPUs can build communication by configuring the MSGBOX. The communication parties have 8 bidirectional channels. One CPU acts as a transmitter and the other acts as a receiver. During the communication process, the current status can be judged through the interrupt or FIFO status.

3.15.4 Operation Modes

3.15.4.1 Checking the Transfer Status via the Interrupt Status

1. Interrupt enable bit: configure the interrupt enable bit of transmitter/receiver through MSGBOX_IRQ_EN_REG.
2. When FIFO is not full, an interrupt pending generates to remind the transmitter to transmit data. At this time, write data to FIFO in interrupt handler, clear the pending bit and the enable bit of Transmitter IRQ.
3. When FIFO has new data, an interrupt pending generates to remind the receiver to receive data. At this time, read data from FIFO in interrupt handler, clear the pending bit and the enable bit of Receiver IRQ.

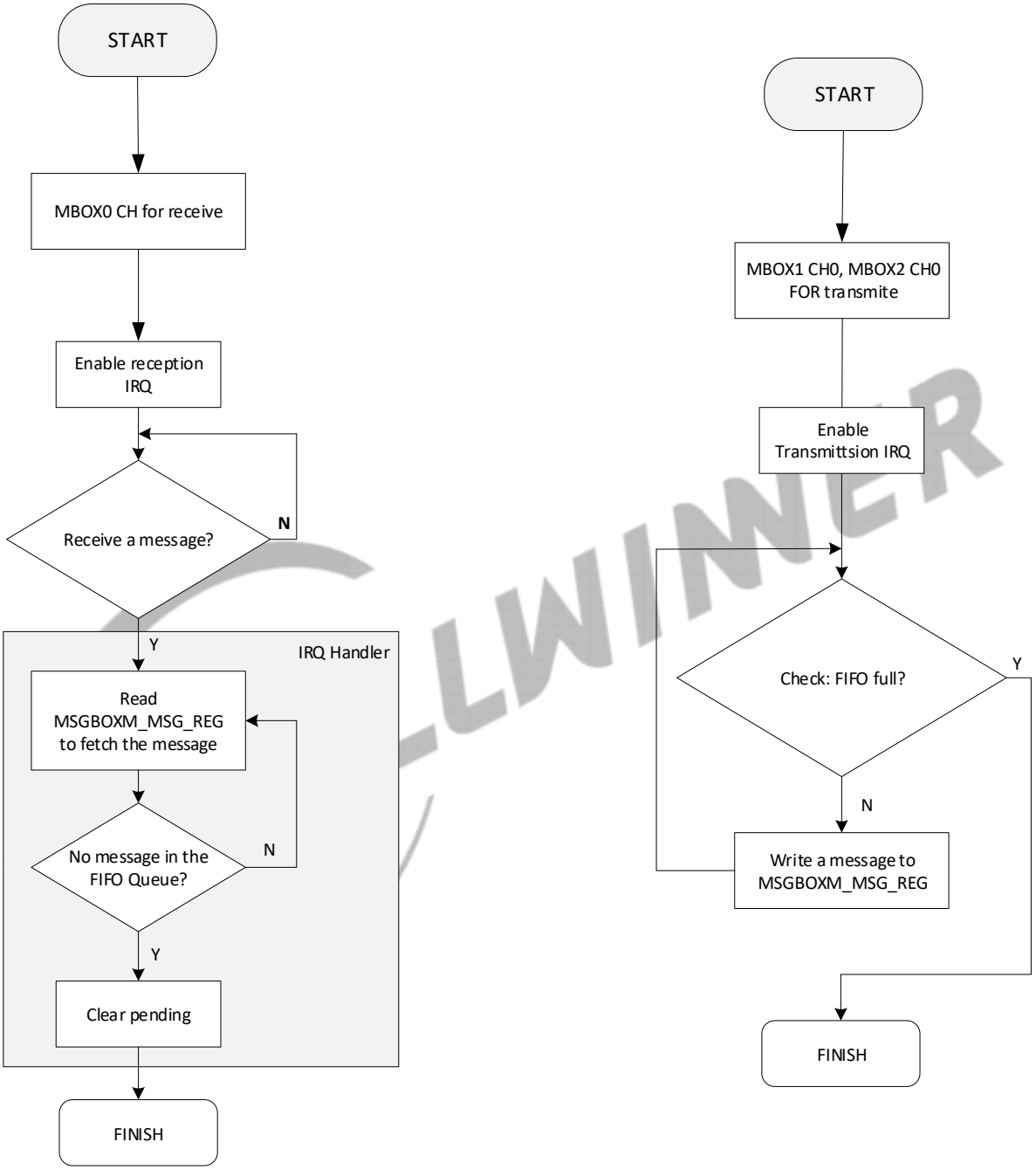
3.15.4.2 Checking the Transfer Status via the FIFO Status

1. When FIFO is not full, the transmitter fills FIFO to 8*32 bits.
2. When the receiver considers FIFO is full, the receiver reads the FIFO data, and reads MSGBOXM_MSG_STATUS_REG to require the current FIFO number.

3.15.5 Programming Guidelines

The working process of CPU0 is as follows:

Figure 3-47 CPU0 Working Process



3.15.6 Register List

Module Name	Base Address	Comments
MBOX(CPUX)	0x0300 3000	base address for CPUX
MBOX(RISC CPU)	0x0602 0000	base address for RISC CPU

Parameter	Description
N	0~1 The number of CPUs communicating with the current CPU. There is only 1 item in V851S/V851SE, so the N value is fixed at 0.
P	0~3 Number of channels between two CPUs.

Register Name	Offset	Description
MSGBOX (CPUX)		
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100(N=0)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100(N=0)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100(N=0)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100(N=0)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100(N=0)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004(N=0)(P=0~3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004(N=0)(P=0~3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004(N=0)(P=0~3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESHOLD_REG	0x0080+N*0x0100+P*0x0004(N=0)(P=0~3)	MSGBOX Write IRQ Threshold Register
MBOX (RISC CPU)		
MSGBOX_RD_IRQ_EN_REG	0x0020+N*0x0100(N=0~1)	MSGBOX Read IRQ Enable Register
MSGBOX_RD_IRQ_STATUS_REG	0x0024+N*0x0100(N=0~1)	MSGBOX Read IRQ Status Register
MSGBOX_WR_IRQ_EN_REG	0x0030+N*0x0100(N=0~1)	MSGBOX Write IRQ Enable Register
MSGBOX_WR_IRQ_STATUS_REG	0x0034+N*0x0100(N=0~1)	MSGBOX Write IRQ Status Register
MSGBOX_DEBUG_REG	0x0040+N*0x0100(N=0~1)	MSGBOX Debug Register
MSGBOX_FIFO_STATUS_REG	0x0050+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX FIFO Status Register
MSGBOX_MSG_STATUS_REG	0x0060+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX Message Status Register
MSGBOX_MSG_REG	0x0070+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX Message Queue Register
MSGBOX_WR_INT_THRESHOLD_REG	0x0080+N*0x0100+P*0x0004(N=0~1)(P=0~3)	MSGBOX Write IRQ Threshold Register

Note:

MBOX	CPU	N Value
MBOX(CPUX)	RISC CPU -> CPUX	N=0

3.15.7 CPUX MSGBOX Register Description

3.15.7.1 0x0020+N*0x0100(N=0) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0020+N*0x0100(N=0)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN. Reception Channel3 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 3 has received a new message.)
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN. Reception Channel2 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 2 has received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN. Reception Channel1 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 1 has received a new message.)
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN. Reception Channel0 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

3.15.7.2 0x0024+N*0x0100(N=0) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0024+N*0x0100(N=0)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:3	/	/	/

Offset:0x0024+N*0x0100(N=0)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND. Reception Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Set one to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. Reception Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Set one to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND. Reception Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Set one to this bit will clear it.
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND. Reception Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Set one to this bit will clear it.

3.15.7.3 0x0030+N*0x0100(N=0) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0030+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN. Transmit Channel3 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 3 empty level reach the configured threshold.)
6	/	/	/

Offset:0x0030+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	**R/W**	**Default/Hex**	**Description**
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN. Transmit Channel2 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 2 empty level reach the configured threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN. Transmit Channel1 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 1 empty level reach the configured threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. Transmit Channel0 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 0 empty level reach the configured threshold.)
0	/	/	/

3.15.7.4 0x0034+N*0x0100(N=0) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0034+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND. Transmit Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configured threshold. Set one to this bit will clear it.
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND. Transmit Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configured threshold. Set one to this bit will clear it.
4	/	/	/

Offset:0x0034+N*0x0100(N=0)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND. Transmit Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configured threshold. Set one to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND. Transmit Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configured threshold. Set one to this bit will clear it.
0	/	/	/

3.15.7.5 0x0040+N*0x0100(N=0) MSGBOX Debug Register (Default Value: 0x0000_0000)

Offset:0x0040+N*0x0100(N=0)			Register Name: MSGBOX_DEBUG_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	FIFO_CTRL. FIFO Control. MQ [7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE. Debug Mode. In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

3.15.7.6 0x0050+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX FIFO Status Register (Default Value: 0x0000_0000)

Offset:0x0050+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31: 1	/	/	/

Offset:0x0050+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
0	R	0x0	FIFO_NOT_AVA_FLAG. FIFO is not available flag. 0: The Message FIFO queue empty level reached the configured threshold 1: The Message FIFO queue empty level is not reached the configured threshold This FIFO status register has the status related to the message queue.

3.15.7.7 0x0060+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset:0x0060+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R	0x0	MSG_NUM. Message Number. Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001~1111:/

3.15.7.8 0x0070+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset:0x0070+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_MSG_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:0	R/W	0x0	MSG_QUE. The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

3.15.7.9 0x0080+N*0x0100+P*0x0004(N=0) (P=0~3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset:0x0080+N*0x0100+P*0x0004(N=0)(P=0~3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Configure the FIFO empty level to trigger the write interrupt for user1. 00: 1 01: 2 10: 4 11: 8

3.15.8 RISC CPU MSGBOX Register Description

3.15.8.1 0x0020+N*0x0100(N=0~1) MSGBOX Read IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0020+N*0x0100(N=0~1)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN. Reception Channel3 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 3 has received a new message.)
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN. Reception Channel2 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 2 has received a new message.)
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN. Reception Channel1 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 1 has received a new message.)
1	/	/	/

Offset:0x0020+N*0x0100(N=0~1)			Register Name: MSGBOX_RD_IRQ_EN_REG
Bit	**R/W**	**Default/Hex**	**Description**
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN. Reception Channel0 Interrupt Enable. 0: Disable 1: Enable (It will notify user 0 by interrupt when Message Queue 0 has received a new message.)

3.15.8.2 0x0024+N*0x0100(N=0~1) MSGBOX Read IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0024+N*0x0100(N=0~1)			Register Name: MSGBOX_RD_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:3	/	/	/
6	R/W	0x0	RECEPTION_MQ3_IRQ_PEND. Reception Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 3 has received a new message. Set one to this bit will clear it.
5	/	/	/
4	R/W	0x0	RECEPTION_MQ2_IRQ_PEND. Reception Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 2 has received a new message. Set one to this bit will clear it.
3	/	/	/
2	R/W	0x0	RECEPTION_MQ1_IRQ_PEND. Reception Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 1 has received a new message. Set one to this bit will clear it.
1	/	/	/
0	R/W	0x0	RECEPTION_MQ0_IRQ_PEND. Reception Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 0 when Message Queue 0 has received a new message. Set one to this bit will clear it.

3.15.8.3 0x0030+N*0x0100(N=0~1) MSGBOX Write IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0030+N*0x0100(N=0~1)			Register Name: MSGBOX_WR_IRQ_EN_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN. Transmit Channel3 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 3 empty level reach the configed threshold.)
6	/	/	/
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN. Transmit Channel2 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 2 empty level reach the configed threshold.)
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN. Transmit Channel1 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 1 empty level reach the configed threshold.)
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN. Transmit Channel0 Interrupt Enable. 0: Disable 1: Enable (It will Notify user 1 by interrupt when Message Queue 0 empty level reach the configed threshold.)
0	/	/	/

3.15.8.4 0x0034+N*0x0100(N=0~1) MSGBOX Write IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0034+N*0x0100(N=0~1)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TRANSMIT_MQ3_IRQ_PEND. Transmit Channel3 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 3 empty level reach the configed threshold. Set one to this bit will clear it.
6	/	/	/

Offset:0x0034+N*0x0100(N=0~1)			Register Name: MSGBOX_WR_IRQ_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
5	R/W	0x0	TRANSMIT_MQ2_IRQ_PEND. Transmit Channel2 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 2 empty level reach the configed threshold. Set one to this bit will clear it.
4	/	/	/
3	R/W	0x0	TRANSMIT_MQ1_IRQ_PEND. Transmit Channel1 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 1 empty level reach the configed threshold. Set one to this bit will clear it.
2	/	/	/
1	R/W	0x0	TRANSMIT_MQ0_IRQ_PEND. Transmit Channel0 Interrupt Pending. 0: No effect, 1: Pending. This bit will be pending for user 1 when Message Queue 0 empty level reach the configed threshold. Set one to this bit will clear it.
0	/	/	/

3.15.8.5 0x0040+N*0x0100(N=0~1) MSGBOX Debug Register(Default Value: 0x0000_0000)

Offset:0x0040+N*0x0100(N=0~1)			Register Name: MSGBOX_DEBUG_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	FIFO_CTRL. FIFO Control. MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode. 1: Disable the corresponding FIFO (Clear FIFO).
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE. Debug Mode. In the Debug Mode, each user can transmit messages to itself through each Message Queue. 0: Normal Mode 1: Debug Mode.

3.15.8.6 0x0050+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX FIFO Status Register(Default Value: 0x0000_0000)

Offset:0x0050+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_FIFO_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31: 1	/	/	/
0	R	0x0	FIFO_NOT_AVA_FLAG. FIFO is not available flag. 0: The Message FIFO queue empty level reached the configed threshold 1: The Message FIFO queue empty level is not reached the configed threshold This FIFO status register has the status related to the message queue.

3.15.8.7 0x0060+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX Message Status Register (Default Value: 0x0000_0000)

Offset:0x0060+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_MSG_STATUS_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R	0x0	MSG_NUM. Message Number. Number of unread messages in the message queue. Here, limited to eight messages per message queue. 0000: There is no message in the message FIFO queue. 0001: There is 1 message in the message FIFO queue. 0010: There are 2 messages in the message FIFO queue. 0011: There are 3 messages in the message FIFO queue. 0100: There are 4 messages in the message FIFO queue. 0101: There are 5 messages in the message FIFO queue. 0110: There are 6 messages in the message FIFO queue. 0111: There are 7 messages in the message FIFO queue. 1000: There are 8 messages in the message FIFO queue. 1001~1111:/

3.15.8.8 0x0070+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX Message Queue Register (Default Value: 0x0000_0000)

Offset:0x0070+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_MSG_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:0	R/W	0x0	MSG_QUE. The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

3.15.8.9 0x0080+N*0x0100+P*0x0004(N=0~1)(P=0~3) MSGBOX Write IRQ Threshold Register (Default Value: 0x0000_0000)

Offset:0x0080+N*0x0100+P*0x0004(N=0~1)(P=0~3)			Register Name: MSGBOX_WR_INT_THRESHOLD_REG
Bit	**R/W**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	MSG_WR_INT_THRESHOLD_CFG Config the FIFO empty level to trigger the write interrupt for user1. 00: 1 01: 2 10: 4 11: 8

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4 Memory

4.1 SDRAM Controller (DRAMC)

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all in-dusty-standard DDR3L. It supports up to a 24G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings. To simplify chip system integration, DDR controller works in the half rate mode.

The DRAMC has the following features:

- Supports 16-bit one channel
- Supports 2 chip select signals
- Supports SIP 64 MB DDR2
- Supports the power voltage of different memory devices: 1.8V
- Supports clock frequency up to 528 MHz for DDR2
- 16 address lines and three bank address lines per channel
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Priority of transferring through multiple ports is programmable
- Supports random read or write operation
- Clock frequency can be changed for different application(MDFS supported)
- Controller clock on/off hardware automatically support
- Auto Self-Refresh Entry(ASRE)/Exit(ASRX) support
- Clock pad enable/disable hardware automatically support when ASRE/ASRX

4.2 SD/MMC Host Controller (SMHC)

4.2.1 Overview

The SMHC controls the read/write operations on the secure digital (SD) cards, multimedia cards (MMC), and various extended devices that is based on the secure digital input/output (SDIO) protocol. The processor provides three SMHC interfaces for controlling the SD cards, MMCs, and SDIO devices.

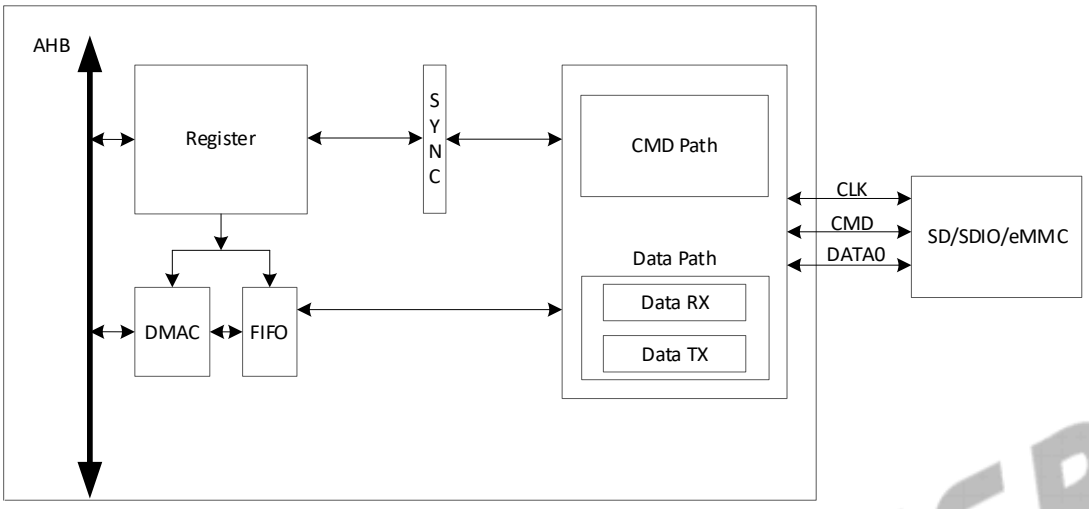
The SMHC has the following features:

- Supports Secure Digital memory protocol commands (up to SD3.0)
- Supports Secure Digital I/O protocol commands (up to SDIO3.0)
- Supports Multimedia Card protocol commands (up to MMC5.1)
- Supports eMMC boot operation and alternative boot operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 5.1)
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports block size of 1 to 65535 bytes
- Supports descriptor based on internal DMA controller
- Internal 1K Bytes FIFO for data transfer
- SMHC0/1 is an instantiation of SMHC v5.30, supports 1-bit and 4-bit data bus width
  - SDR mode 150 Mhz@1.8V IO pad
  - DDR mode 50 Mhz@1.8V IO pad
  - SDR mode 50 Mhz@3.3V IO pad
- SMHC2 is an instantiation of SMHC v5.30, supports 1-bit, 4-bit, and 8-bit data bus width
  - SDR mode 150Mhz@1.8V IO pad
  - DDR mode 150Mhz@1.8V IO pad
  - DDR mode 50Mhz@3.3V IO pad
  - SDR mode 50Mhz@3.3V IO pad

4.2.2 Block Diagram

The following figure shows a block diagram of the SMHC.

Figure 4-1 SMHC Block Diagram



SMHC contains the following sub-blocks:

Table 4-1 SMHC Sub-blocks

Sub-block	Description
Register	Used to configure the control signal for reading or writing the SD/SDIO/eMMC.
DMAC	The DMA controller that controls the data transfer between the memory and SMHC.
FIFO	A buffer for the data stream between the memory and the SMHC asynchronous clock domain.
SYNC	Synchronizes the signals from the AHB clock domain to the SMHC clock domain.
CMD Path	Sends commands to or receives commands from the SD/SDIO/eMMC.
Data Path	Consists of Data TX and Data RX sub-modules. The Data TX sends data blocks and the CRC codes to the SD/SDIO/eMMC. The Data RX receives data blocks and the CRC codes from the SD/SDIO/eMMC.

4.2.3 Functional Descriptions

4.2.3.1 External Signals

The following table describes the external signals of SMHC.

Table 4-2 SMHC External Signals

Signal	Description	Width	Type
SMHC0			

Signal	Description	Width	Type
SDC0-CMD	Command Signal for SD Card	1	I/O, OD
SDC0-CLK	Clock for SD Card	1	O
SDC0-D[3:0]	Data Input and Output for SD Card	4	I/O
SMHC1			
SDC1-CMD	Command Signal for SDIO WIFI	1	I/O, OD
SDC1-CLK	Clock for SDIO WIFI	1	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	4	I/O
SMHC2			
SDC2-CMD	Command Signal for eMMC	1	I/O, OD
SDC2-CLK	Clock for eMMC	1	O
SDC2-D[3:0]	Data Input and Output for eMMC	8	I/O

4.2.3.2 Clock Sources

Table 4-3 SMHC Clock Sources

Module	Module Clock	Source	Description
SMHC0	SMHC0_CLK	CCU	Refer to section 3.4 Clock Controller Unit (CCU) for detailed information.
	AHB2_CLK	CCU	
	CLK32K	CCU	
SMHC1	SMHC1_CLK	CCU	
	AHB2_CLK	CCU	
	CLK32K	CCU	
SMHC2	SMHC2_CLK	CCU	
	AHB2_CLK	CCU	
	CLK32K	CCU	

4.2.3.3 Timing Diagram

Refer to the following relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard (4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard (5.0)

4.2.3.4 Data Path

The SMHC and SD/SDIO/eMMC contains the following interface buses: CLK, CMD, and DATA 1/4. During one clock cycle, the SMHC can transmit one bit command with one or two bits data in 1-ch DATA mode, or four or eight bits data in 4-ch DATA mode. The CMD is a bidirection channel for initializing the SD/SDIO/eMMC and transmitting commands. It can work in both the open-drain mode and push-pull mode. The DATA is also a bidirection channel. It works in the push-pull mode.

Reading Data from the SD/SDIO/eMMC

The register configures the signals for the read operation, and synchronize the signals to the SMHC clock domain. Then the Data RX reads data from the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses and writes the data in the FIFO. After that, the DMAC transfers the data from the FIFO to the memory.

Writing Data to the SD/SDIO/eMMC

The register configures the signals for the write operation, and synchronize the signals to the SMHC clock domain. Then the DMAC reads data from the memory and writes the data to the FIFO. After that, the Data TX reads the data from the FIFO and writes the data to the SD/SDIO/eMMC via the CLK/CMD/DATA interface buses.

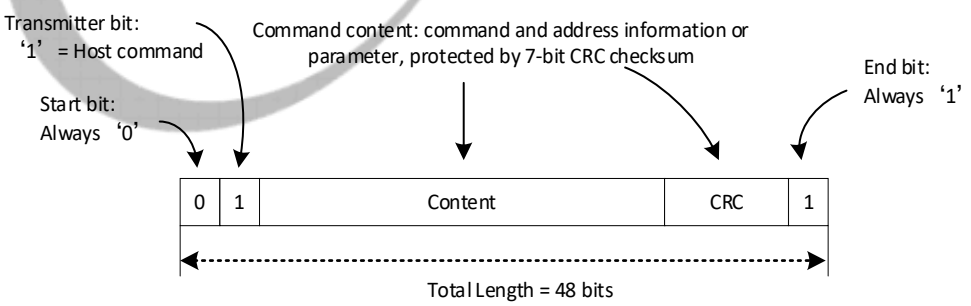
4.2.3.5 Package Format

Data transfer over the SD/eMMC bus is based on command and data bitstreams that are initiated by a start bit and terminated by a stop bit. There are three types of SD/eMMC packets: command token, response token, and data packet.

Command Tokens

The command token starts an operation. A command is sent from the host to a device. It is transferred serially on the CMD line. Command tokens have the following coding scheme:

Figure 4-2 Command Token Format



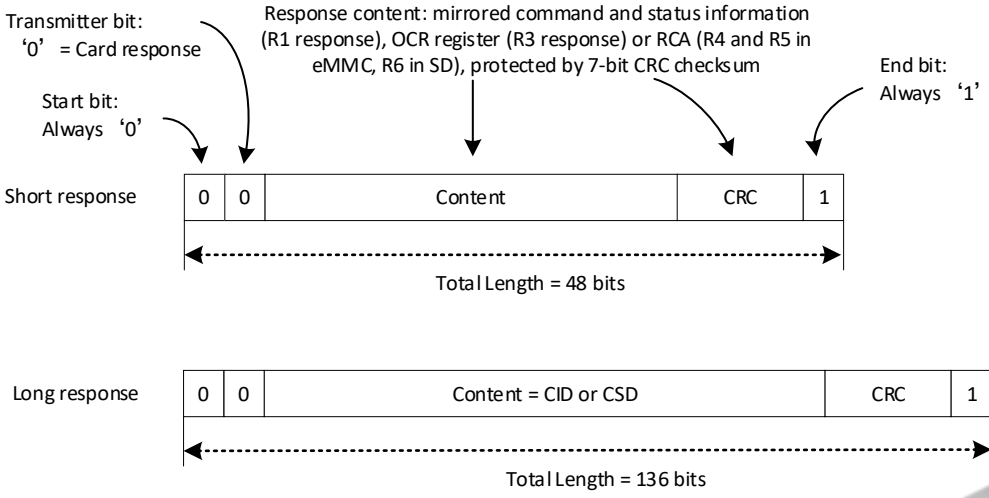
Each command token has 48 bits, preceded by a start bit ('0') and succeeded by an end bit ('1'). To detect transmission errors, each token is protected by CRC bits.

Response Tokens

After receiving a command, the card returns a 48-bit or 136-bit response based on the command type.

A response token is sent from the device to the host as an answer to a previously received command. It is transferred serially on the CMD line.

Figure 4-3 Response Token Format



Data Packets

Data can be transferred from the device to the host or vice versa. Data are transferred via the data lines.

Figure 4-4 Data Packet Format for SDR

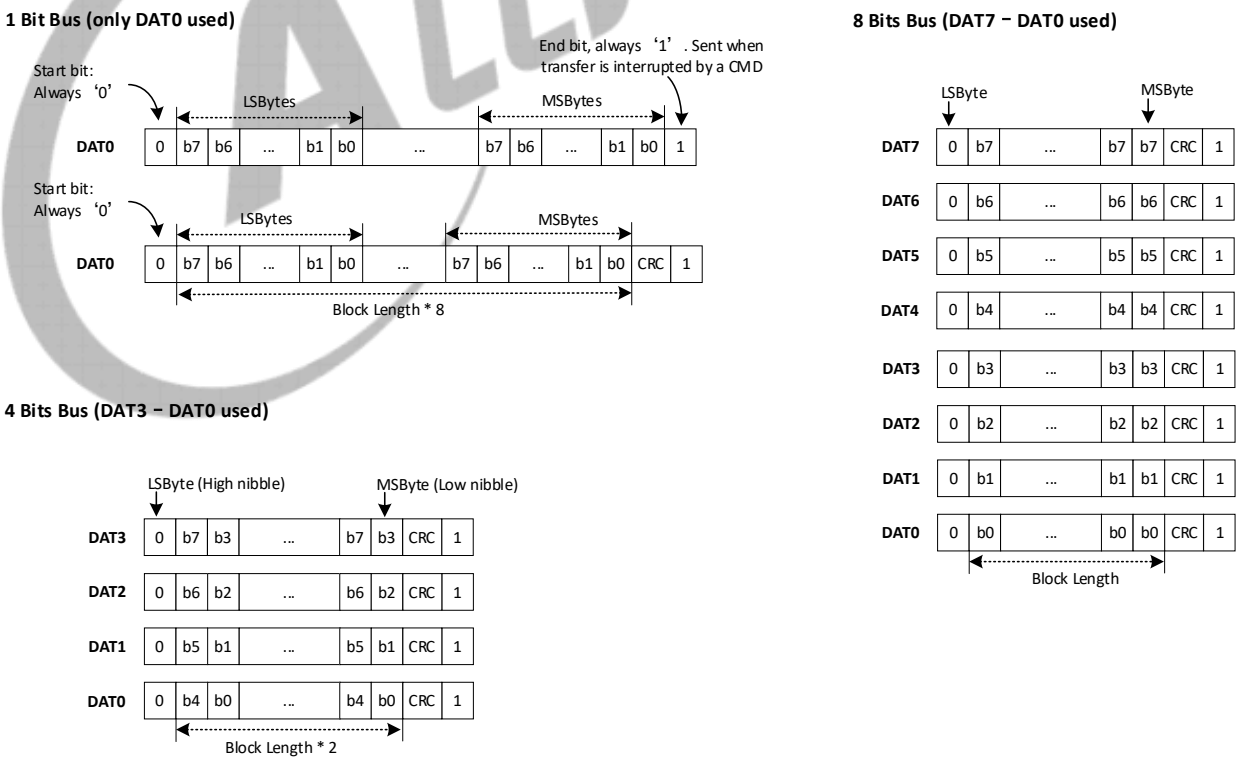
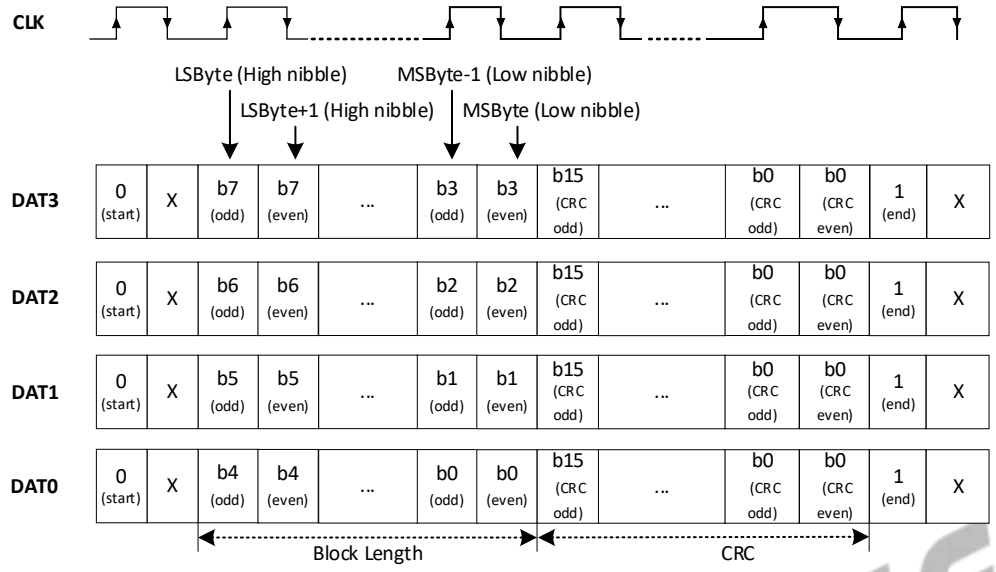
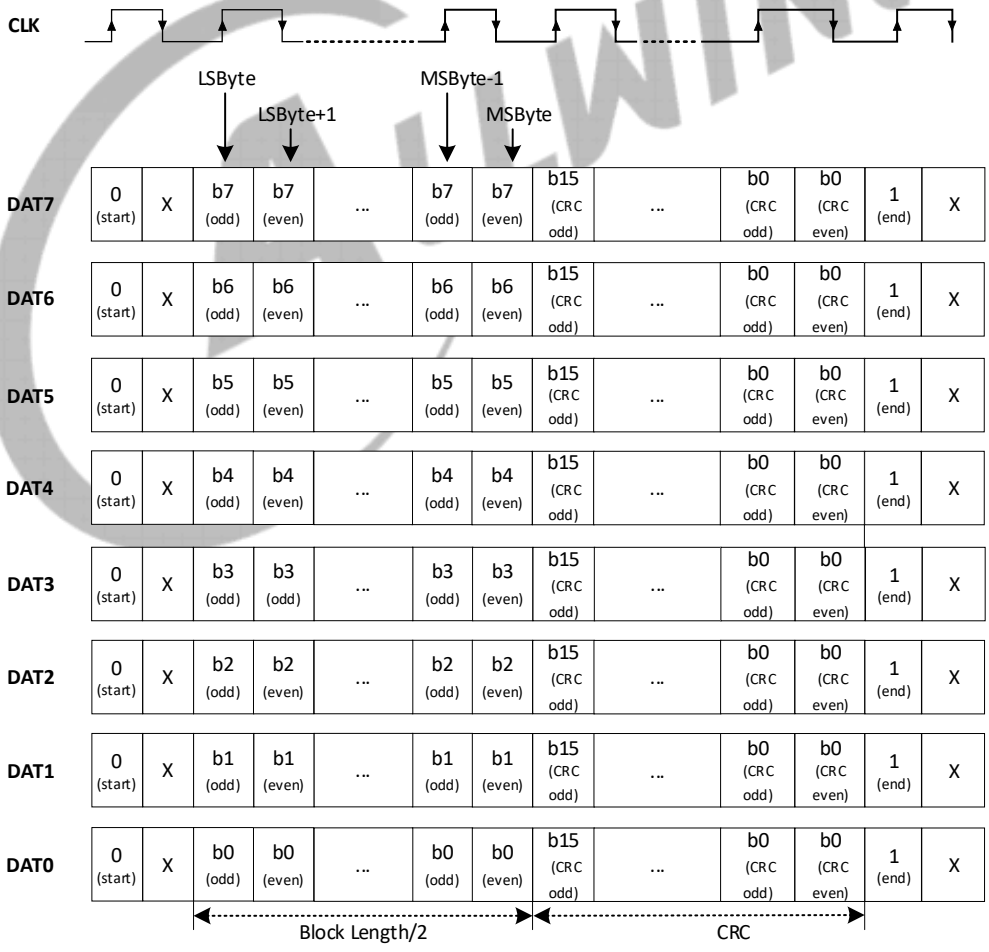


Figure 4-5 Data Packet Format for DDR

4 Bits Bus DDR (DAT3 – DAT0 used)



8 Bits Bus DDR (DAT7 – DAT0 used)

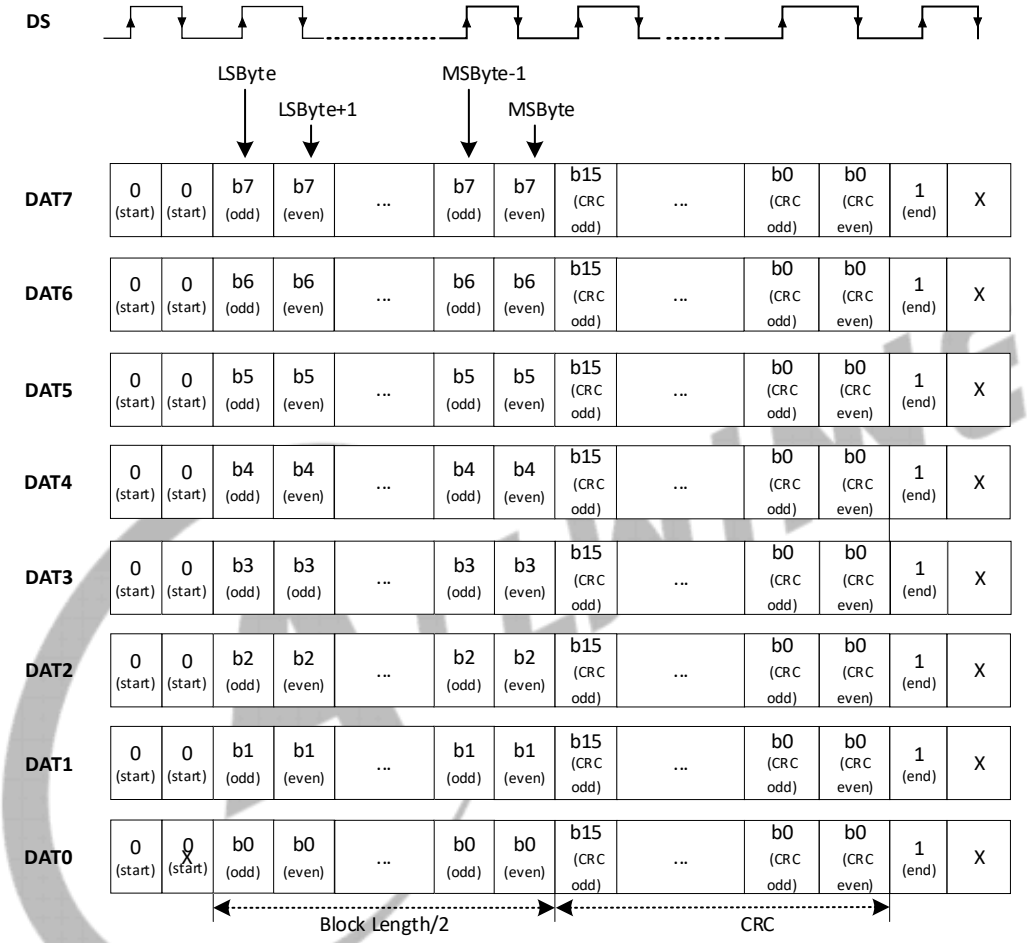


NOTE

Bytes data are not interleaved but CRCs are interleaved.
Start and end bits are only valid on the rising edge (“X” indicates “undefined”).

Figure 4-6 Data Packet Format for DDR in HS400 Mode

8 Bits Bus DDR for HS400 Output (DAT7 – DAT0 used)



NOTE

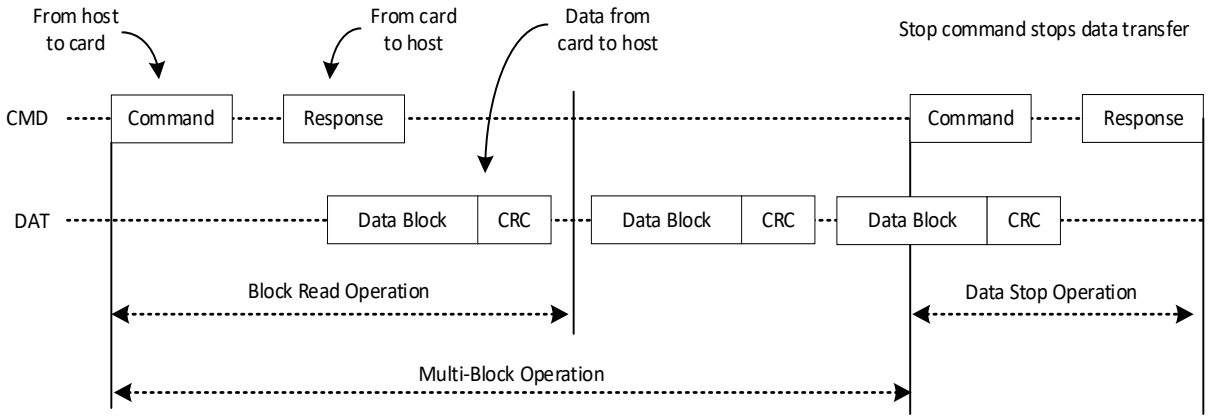
Bytes data are not interleaved but CRCs are interleaved.
Start bits are valid when Data Strobe is High and Low.
End bits are only valid when Data Strobe is High (“X” indicates “undefined”).

Data Transfer

Data transfers to or from the SD/eMMC card are done in blocks. Single and multiple block operations are widely used during data transfer.

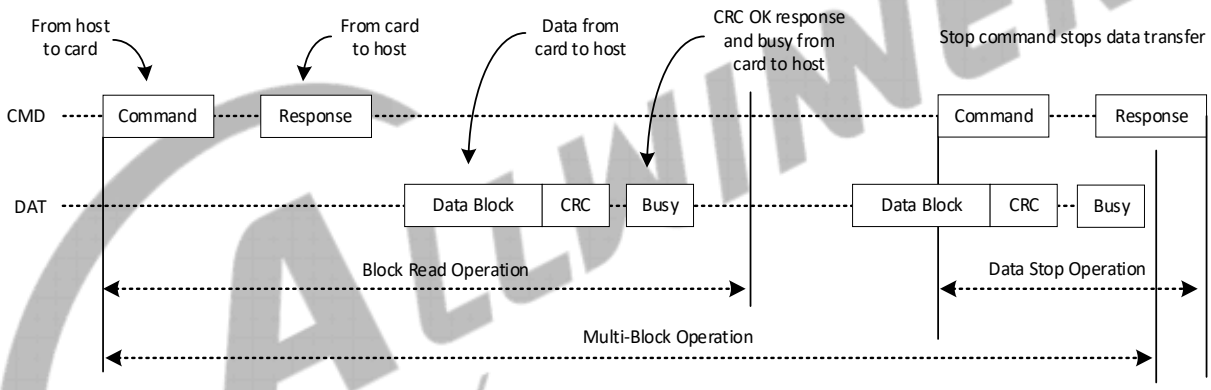
The following figure shows the single-block and multi-block read operation.

Figure 4-7 Single-Block and Multi-Block Read Operation



The following figure shows the single-block and multi-block write operation.

Figure 4-8 Single-Block and Multi-Block Read Operation



4.2.3.6 Internal DMA Controller Description

The SMHC has an internal DMA controller (IDMAC) to transfer data between the host memory and SMHC port. With a descriptor, the IDMAC can efficiently move data from the source to destination by automatically loading the next DMA transfer arguments, which needs less CPU intervention. Before transferring data in the IDMAC, the host driver should construct a descriptor list, configure arguments of every DMA transfer, and then launch the descriptor and start the DMA.

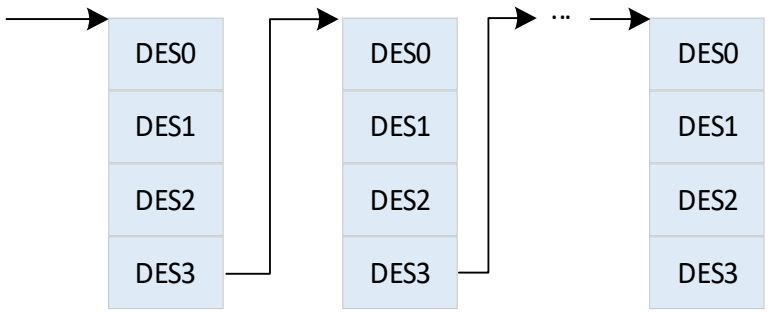
The IDMAC has an interrupt controller. When enabled, it generates an interrupt to the HOST CPU in situations such as data transmission is completed or some error is happened.

IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

The following figure shows the internal formats of a descriptor.

Figure 4-9 IDMAC Descriptor Structure Diagram



This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 corresponds to the [31:0] bits, DES1 corresponds to the [63:32] bits, DES2 corresponds to the [95:64] bits, and DES3 corresponds the [127:96] bits in a descriptor.

The following table shows the bit definition of DES0.

Table 4-4 DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:6	/	/
5	/	Not used
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

The following table shows the bit definition of DES1.

Table 4-5 DES1 Definition

Bits	Name	Descriptor
31:13	/	/
12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

The following table shows the bit definition of DES2.

Table 4-6 DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. It is a word(4byte) address

The following table shows the bit definition of DES3.

Table 4-7 DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present. It is a word(4byte) address.

4.2.3.7 Calibrating the Delay Chain

There are two delay chains in SMHC: data strobe delay chain and sample delay chain.

Data strobe delay chain: used to generate delay to make proper timing between Data Strobe and data signals.

Sample delay chain: used to generate delay to make proper timing between the internal card clock signal and data signals.

Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

Follow the steps below to calibrate the delay chain:

1. Enable SMHC. In order to calibrate the delay chain by the operation registers in SMHC, the SMHC must be enabled through SMHC Bus Gating Reset Register (Offset: 0x084C) and SMHCx Clock Register (Offset: 0x0830).
2. Configure a proper clock for SMHC. The delay chain calibration is based on the clock for SMHC from Clock Control Unit (CCU). The delay chain calibration is an internal function in SMHC and needs no

devices. So it is unnecessary to open the clock signal for devices. The recommended clock frequency is 200 MHz.

3. Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain** (bit[5:0]). Then write 0x0 to **delay control register** to clear the value.
4. Write 0x8000 to **delay control register** to start calibrating the delay chain.
5. Wait until the flag (bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at bit[13:8] in **delay control register**. The delay time generated by these delay cells is equal to the cycle of the SMHC clock nearly. This value is the result of calibration.
6. Calculate the delay time of one delay cell according to the cycle of the SMHC clock and the result of calibration.

4.2.4 Programming Guidelines

4.2.4.1 Initializing SMHC

Before data and commands are exchanged between a card and the SMHC, the SMHC needs to be initialized. Follow the steps below to initialize the SMHC:

1. Configure the corresponding GPIO register as an SMHC by the Port Controller module; reset the clock by writing 1 to SMHC_BGR_REG[SMHCx_RST], and open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING]; select clock sources and set the division factor by configuring the SMHCx_CLK_REG (x = 0, 1) register.
2. Configure SMHC_CTRL (Offset: 0x0000) to reset the FIFO and controller, and enable the global interrupt; configure SMHC_INTMASK (Offset: 0x0030) to 0xFFCE to enable normal interrupts and error abnormal interrupts, and then register the interrupt function.
3. Configure SMHC_CLKDIV (Offset: 0x0004) to open clock for devices; configure SMHC_CMD (Offset: 0x0018) as the change clock command (for example 0x80202000); send the update clock command to deliver clocks to devices.
4. Configure SMHC_CMD (Offset: 0x0018) as a normal command. Configure SMHC_CMDARG (Offset: 0x001C) to set command parameters. Configure SMHC_CMD (Offset: 0x0018) to set parameters like whether to send the response, the response type, and the response length and then send the commands. According to the initialization process in the protocol, you can finish SMHC initialization by sending the corresponding command one by one.

4.2.4.2 Writing a Single Data Block

To write a single data block, follow the steps below:

1. Write 0x1 to SMHC_CTRL (Offset: 0x0000) [DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_DMAC (Offset: 0x0080) to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE (Offset: 0x008C) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

2. Configure SMHC_FIFOTH (Offset: 0x0040) to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH (Offset: 0x0040) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA (Offset: 0x0084) to determine the start address of the DMA descriptor.

3. To write one block data to sector1, configure SMHC_BYTCNT (Offset: 0x0014) [BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD24 (Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD (Offset: 0x0018), and send CMD24 command to write data to the device.

4. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

5. Check whether SMHC_IDST (Offset: 0x0088) [TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST (Offset: 0x0088) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

6. Check whether SMHC_RINTSTS (Offset: 0x0038) [DTC] is 1. If yes, the data transfer and CMD24 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS (Offset: 0x0038) and SMHC_STATUS (Offset: 0x003C) to query the existing abnormity.

7. Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG (Offset: 0x001C) to 0x12340000, write 0x8000014D to SMHC_CMD (Offset: 0x0018), go to step 4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (Offset: 0x0020) (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

4.2.4.3 Reading a Single Data Block

To read a single data block, follow the steps below:

1. Write 0x1 to SMHC_CTRL (Offset: 0x0000) [DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_DMAC (Offset: 0x0080) to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE (Offset: 0x008C) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

2. Configure SMHC_FIFOTH (Offset: 0x0040) to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH (Offset: 0x0040) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA (Offset: 0x0084) to determine the start address of the DMA descriptor.

3. To read one block data from sector1, configure SMHC_BYTCNT (Offset: 0x0014) [BYTE_CNT] to 0x200 and configure the descriptor according to the data size; set the data sector address of CMD17 command (Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD (Offset: 0x0018), and send CMD17 command to read data from the device to DRAM/SRAM.

4. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

5. Check whether SMHC_IDST (Offset: 0x0088) [RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST (Offset: 0x0088) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

6. Check whether SMHC_RINTSTS (Offset: 0x0038) [DTC] is 1. If yes, data transfer and CMD17 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS (Offset: 0x0038) and SMHC_STATUS (Offset: 0x003C) to query the existing abnormity.

4.2.4.4 Writing Open-Ended Multiple Data Blocks (CMD25 + Auto CMD12)

To write open-ended multiple data blocks, follow the steps below:

1. Write 0x1 to SMHC_CTRL (Offset: 0x0000) [DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_DMAC (Offset: 0x0080) to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE (Offset: 0x008C) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

2. Configure SMHC_FIFOTH (Offset: 0x0040) to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH (Offset: 0x0040) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA (Offset: 0x0084) to determine the start address of the DMA descriptor.

3. To write three blocks of data to sectors begin with sector0, configure SMHC_BYTCNT (Offset: 0x0014) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD (Offset: 0x0018), and send CMD25 command to read data from the device to DRAM/SRAM.

4. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

5. Check whether SMHC_IDST (Offset: 0x0088) [RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST (Offset: 0x0088) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

6. Check whether SMHC_RINTSTS (Offset: 0x0038) [ACD] and SMHC_RINTSTS (Offset: 0x0038) [DTC] are both 1. If yes, the data transfer, CMD12 transfer, and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS (Offset: 0x0038) and SMHC_STATUS (Offset: 0x003C) to query the existing abnormity.

7. Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG (Offset: 0x001C) to 0x12340000, write 0x8000014D to SMHC_CMD (Offset: 0x0018), go to step 4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (Offset: 0x0020) (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

4.2.4.5 Reading Open-Ended Multiple Data Blocks (CMD18 + Auto CMD12)

To read open-ended multiple data blocks, follow the steps below:

1. Write 0x1 to SMHC_CTRL (Offset: 0x0000) [DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_DMAC (Offset: 0x0080) to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE (Offset: 0x008C) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure SMHC_FIFOTH (Offset: 0x0040) to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH (Offset: 0x0040) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA (Offset: 0x0084) to determine the start address of the DMA descriptor.
3. To read three blocks of data from sectors begin with sector0, configure SMHC_BYTCNT (Offset: 0x0014) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 command (Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD (Offset: 0x0018), and send CMD18 command to read data to the device. When the data transfer is completed, CMD12 will be sent automatically.
4. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.
5. Check whether SMHC_IDST (Offset: 0x0088) [RX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST (Offset: 0x0088) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.
6. Check whether SMHC_RINTSTS (Offset: 0x0038) [ACD] and SMHC_RINTSTS (Offset: 0x0038) [DTC] are both 1. If yes, data transfer, CMD12 transfer, and CMD18 reading operation are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS (Offset: 0x0038) and SMHC_STATUS (Offset: 0x003C) to query the existing abnormity.

4.2.4.6 Writing Pre-Defined Multiple Data Blocks (CMD23 + CMD25)

To write pre-defined multiple data blocks, follow the steps below:

1. Write 0x1 to SMHC_CTRL (Offset: 0x0000) [DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_DMAC (Offset: 0x0080) to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE (Offset: 0x008C) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.
2. Configure SMHC_FIFOTH (Offset: 0x0040) to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH (Offset: 0x0040) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA (Offset: 0x0084) to determine the start address of the DMA descriptor.
3. To write three blocks of data, configure SMHC_CMDARG (Offset: 0x001C) to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD (Offset: 0x0018) to send the CMD23 command. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

4. Configure SMHC_BYTCNT (Offset: 0x0014) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD25 command (Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD (Offset: 0x0018), and send CMD25 command to write data to the device.

5. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

6. Check whether SMHC_IDST (Offset: 0x0088) [TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST (Offset: 0x0088) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

7. Check whether SMHC_RINTSTS (Offset: 0x0038) [DTC] is 1. If yes, the data transfer and CMD25 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS (Offset: 0x0038) and SMHC_STATUS (Offset: 0x003C) to query the existing abnormity.

8. Send CMD13 command to query whether the device writing operation is completed and returns to the idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG (Offset: 0x001C) to 0x12340000, write 0x8000014D to SMHC_CMD (Offset: 0x0018), go to step 4 to ensure command transfer completed, and then check whether the highest bit of SMHC_RESP0 (Offset: 0x0020) (CMD13 response) is 1. If yes, the device is in the idle status, and the next command can be sent. Otherwise, the device is in the busy status. Continue to send CMD13 to wait for the device to enter the idle status until timeout.

4.2.4.7 Reading Pre-Defined Multiple Data Blocks (CMD23 + CMD18)

To read pre-defined multiple data blocks, follow the steps below:

1. Write 0x1 to SMHC_CTRL (Offset: 0x0000) [DMA_RST] to reset the internal DMA controller; write 0x82 to SMHC_DMAC (Offset: 0x0080) to enable the IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE (Offset: 0x008C) to enable the transfer interrupt, receive interrupt, and abnormal interrupt.

2. Configure SMHC_FIFOTH (Offset: 0x0040) to determine the burst size and TX/RX trigger level. For example, if SMHC_FIFOTH (Offset: 0x0040) is configured as 0x300F00F0, it indicates the burst size is 16, TX_TL is 15, and RX_TL is 240. Configure SMHC_DLBA (Offset: 0x0084) to determine the start address of the DMA descriptor.

3. To read three blocks of data, configure SMHC_CMDARG (Offset: 0x001C) to 0x3 to specify the number of data blocks as three. Then write 0x80000157 to SMHC_CMD (Offset: 0x0018) to send the CMD23 command. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

4. Configure SMHC_BYTCNT (Offset: 0x0014) [BYTE_CNT] to 0x600 and configure the descriptor according to the data size; set the data sector address of CMD18 (Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD (Offset: 0x0018), and send CMD18 command to read data from device to DRAM/SRAM.

5. Check whether SMHC_RINTSTS (Offset: 0x0038) [CC] is 1. If yes, the command is sent successfully; otherwise, continue to wait until timeout, and then exit the process.

6. Check whether SMHC_IDST (Offset: 0x0088) [TX_INT] is 1. If yes, the data transfer for writing DMA is completed. Write 0x337 to SMHC_IDST (Offset: 0x0088) to clear the interrupt flag. Otherwise, continue to wait until timeout, and then exit the process.

7. Check whether SMHC_RINTSTS (Offset: 0x0038) [DTC] is 1. If yes, the data transfer and CMD18 writing operations are completed. Otherwise, abnormity exists. Read SMHC_RINTSTS (Offset: 0x0038) and SMHC_STATUS (Offset: 0x003C) to query the existing abnormity.

4.2.5 Register List

Module Name	Base Address	Comments
SMHC0	0x04020000	
SMHC1	0x04021000	SMHC1 register is the same with SMHC0
SMHC2	0x04022000	SMHC2 register is the same with SMHC0

Register Name	Offset	Description
SMHC_CTRL	0x0000	SMHC Global Control Register
SMHC_CLKDIV	0x0004	SMHC Clock Control Register
SMHC_TMOUT	0x0008	SMHC Timeout Register
SMHC_CTYPE	0x000C	SMHC Bus Width Register
SMHC_BLKSIZ	0x0010	SMHC Block Size Register
SMHC_BYTCNT	0x0014	SMHC Byte Count Register
SMHC_CMD	0x0018	SMHC Command Register
SMHC_CMDARG	0x001C	SMHC Command Argument Register
SMHC_RESP0	0x0020	SMHC Response 0 Register
SMHC_RESP1	0x0024	SMHC Response 1 Register
SMHC_RESP2	0x0028	SMHC Response 2 Register
SMHC_RESP3	0x002C	SMHC Response 3 Register
SMHC_INTMASK	0x0030	SMHC Interrupt Mask Register
SMHC_MINTSTS	0x0034	SMHC Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	SMHC Raw Interrupt Status Register
SMHC_STATUS	0x003C	SMHC Status Register
SMHC_FIFOTH	0x0040	SMHC FIFO Water Level Register
SMHC_FUNS	0x0044	SMHC FIFO Function Select Register
SMHC_TBC0	0x0048	SMHC Transferred Byte Count Register 0
SMHC_TBC1	0x004C	SMHC Transferred Byte Count Register 1
SMHC_CSDC	0x0054	SMHC CRC Status Detect Control Register
SMHC_A12A	0x0058	SMHC Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SMHC New Timing Set Register
SMHC_DMAC	0x0080	SMHC DMAC Control Register
SMHC_DLBA	0x0084	SMHC Descriptor List Base Address Register
SMHC_IDST	0x0088	SMHC DMAC Status Register
SMHC_IDIE	0x008C	SMHC DMAC Interrupt Enable Register

Register Name	Offset	Description
SMHC_THLD	0x0100	SMHC Card Threshold Control Register
SMHC_SFC	0x0104	SMHC Sample FIFO Control Register
SMHC_A23A	0x0108	SMHC Auto Command 23 Argument Register
SMHC_EXT_CMD	0x0138	SMHC Extended Command Register
SMHC_EXT_RESP	0x013C	SMHC Extended Response Register
SMHC_DRV_DL	0x0140	SMHC Drive Delay Control Register
SMHC_SAMP_DL	0x0144	SMHC Sample Delay Control Register
SMHC_DS_DL	0x0148	SMHC Data Strobe Delay Control Register
SMHC_FIFO	0x0200	SMHC FIFO Register

4.2.6 Register Description

4.2.6.1 0x0000 SMHC Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 1: AHB bus 0: DMA bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/

Offset: 0x0000			Register Name: SMHC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x1	CD_DBC_ENB Card Detect (Data [3] status) De-bounce Enable 0: disable de-bounce 1: enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

4.2.6.2 0x0004 SMHC Clock Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DAT0 Mask Data0 0: Do not mask data0 when update clock; 1: Mask data0 when update clock;
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1 : Turn off card clock when FSM in IDLE state

Offset: 0x0004			Register Name: SMHC_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

4.2.6.3 0x0008 SMHC Timeout Register (Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device, this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data, data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command (ACMD51, CMD8,CMD17,CMD18). When Host read multiple block(CMD18),the next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, this value is no effect. Note: Under the following 3 conditions, the timeout limit is half of the set time. 1> DDR8 mode 2> DDR4 and SMHC_NTSR[MODE_SELEC] (0x5C [31]) high 3> HS400 and SMHC_NTSR[HS400_NEW_SAMPLE_EN](0x5C[0]) high
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

4.2.6.4 0x000C SMHC Bus Width Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

4.2.6.5 0x0010 SMHC Block Size Register (Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

4.2.6.6 0x0014 SMHC Byte Count Register (Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

4.2.6.7 0x0018 SMHC Command Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command. This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit will be set in SMHC_RINTSTS register. You should not write any other command before this bit is cleared.
30:29	/	/	/

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge. When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: normal command sending 1: send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the SMHC_RESP1 will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: without data transfer 1: with data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

4.2.6.8 0x001C SMHC Command Argument Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

4.2.6.9 0x0020 SMHC Response 0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

4.2.6.10 0x0024 SMHC Response 1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

4.2.6.11 0x0028 SMHC Response 2 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

4.2.6.12 0x002C SMHC Response 3 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

4.2.6.13 0x0030 SMHC Interrupt Mask Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

4.2.6.14 0x0034 SMHC Masked Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	M_CARD_REMOVAL_INT Card Removed

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R	0x0	M_SDIO_INT SDIO Interrupt
15	R	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token or received CRC status token is negative.
14	R	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R	0x0	M_DSE_BC_INT Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared after the last block.
12	R	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative.
6	R	0x0	M_RCE_INT Response CRC Error

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R	0x0	M_DTC_INT Data Transfer Complete
2	R	0x0	M_CC_INT Command Complete
1	R	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

4.2.6.15 0x0038 SMHC Raw Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status token or received CRC status token is negative. This is write-1-to-clear bits.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error/busy clear When set during receiving data, it means that host controller found an error start bit. It is valid at 4-bit or 8-bit bus mode, when it set, host found start bit at data0, but not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared after the last block. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0(1-bit bus) or data0~data3(4-bit bus) or data0~data7(8-bit bus). This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status token is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

4.2.6.16 0x003C SMHC Status Register (Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA [0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data [3] status level of DATA [3]; checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA Command FSM states: 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn't reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn't reach receive trigger level 1: FIFO reached receive trigger level

4.2.6.17 0x0040 SMHC FIFO Water Level Register (Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD(4Byte). A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: BSIZE_OF_TRANS = 3, MSize = 16, TX_TL = 240, RX_TL = 15 FIFO_DEPTH = 256 FIFO_SIZE = 256 * 32 = 1K
27:24	R	0x0	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. 15 (means greater than 15)
15:8	R	0x0	/

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240) 240(means less than or equal to 240)

4.2.6.18 0x0044 SMHC FIFO Function Select Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

4.2.6.19 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.2.6.20 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.2.6.21 0x0054 SMHC CRC Status Detect Control Register (Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA CRC Detect Para 110: HS400 speed mode 011: Other speed mode Others: Reserved

4.2.6.22 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFF	A12A Auto CMD12 Argument The argument of command 12 automatically send by controller with this field.

4.2.6.23 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SEL Mode Select 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing Default value : 1
30:26	/	/	/
25	R/W	0x0	BOOT_DAT_RX_PHASE_CLR After boot ack, before receive boot data, clear data lines' input phase. 0: Disable 1: Enable
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock operation, clear command line's and data lines' input phase. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, clear data lines' input phase. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data, clear data lines' input phase. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data, clear data lines' input phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command RX phase clear 0: Disable 1: Enable
15:10	/	/	/

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	DAT_SAM_TIM_PHS Data Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Sample timing phase offset 0^0（only for SD2 hs400 mode） Default value: 00
7:6	/	/	/
5:4	R/W	0x0	CMD_SAM_TIM_PHS Command Sample Timing Phase 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore Default value: 00
3:1	/	/	/
0	R/W	0x0	HS400_NEW_SAM_EN HS400 New Sample Enable 1：enable hs400 new sample method 0：disable hs400 new sample method

4.2.6.24 0x0080 SMHC DMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0x0	Reserved

Offset: 0x0080			Register Name: SMHC_DMAC
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

4.2.6.25 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor. It is a word(4byte) address

4.2.6.26 0x0088 SMHC DMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:13	R	0x0	Reserved
12:10	R	0x0	DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (SMHC_ IDST [2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved This bit is read-only.

Offset: 0x0088			Register Name: SMHC_IDST
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W1C	0x0	AIS Abnormal Interrupt Summary. Logical OR of the following: SMHC_IDST [2]: Fatal Bus Interrupt SMHC_IDST [4]: Descriptor unavailable bit Interrupt SMHC_IDST [5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NIS Normal Interrupt Summary. Logical OR of the following: SMHC_IDST [0]: Transmit Interrupt SMHC_IDST [1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (SMHC_IDST [12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.

Offset: 0x0088			Register Name: SMHC_IDST
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a 1 clears this bit.

4.2.6.27 0x008C SMHC DMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	Reserved
8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set, Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set, Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

4.2.6.28 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_WR_THLD Card Read/write Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB Card Write Threshold Enable 0: Card write threshold disable 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG Busy Clear Interrupt Generation 0: Busy Clear Interrupt disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO

4.2.6.29 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be change between 0x0 and 0xF, but actually the available value and the position of stopping clock must be decided by the actual situation. The value increase one in this field is linked to one cycle(two cycle in DDR mode) that the position of stopping clock moved up.

Offset: 0x0104			Register Name: SMHC_SFC
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

4.2.6.30 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

4.2.6.31 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS400_MD_EN HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside host controller based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

4.2.6.32 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	AUTO_CMD23_EN Send CMD23 Automatically When set this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST set, this field will be cleared.

4.2.6.33 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

4.2.6.34 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C[31] is low, 45^0 at DDR4 mode when 0x5C[31] is high, 90^0 at HS400 mode when 0x5C[0] is low, 45^0 at HS400 mode when 0x5C[0] is high. 1: Data drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C[31] is low, 90^0 at DDR4 mode when 0x5C[31] is high, 180^0 at HS400 mode when 0x5C[0] is low, 90^0 at HS400 mode when 0x5C[0] is high.

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is: 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4 mode when 0x5C[31] is low, 45^0 at DDR4 mode when 0x5C[31] is high, 90^0 at HS400 mode 1: Command drive phase offset is: 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4 mode when 0x5C[31] is low, 90^0 at DDR4 mode when 0x5C[31] is high, 180^0 at HS400 mode.
15:0	/	/	/

4.2.6.35 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	Read/Write	Default/Hex	Description
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

4.2.6.36 0x0148 SMHC Data Strobe Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

4.2.6.37 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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5 Video and Graphics

5.1 Display Engine (DE)

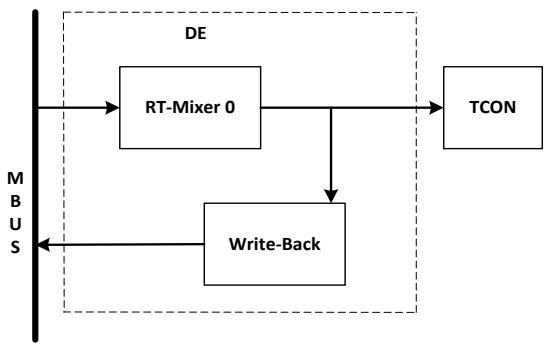
The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports three-channel windows to blend, and supports image post-processing in the video channel.

The DE has the following features:

- Supports output size up to 2048x2048
- Supports three alpha blending channels for main display and each channel has independent scaler
- Supports four overlay layers for each channel
- Supports potter-duff compatible blending operation
- Supports input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Supports input format palette only for UI channel
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive color enhancement (Blue-stretch, Green-stretch and fresh tone correction) and
  - flesh tone protection
  - Hue gain, Saturation gain, and Value gain controlled
  - Fully programmable color matrix
  - Dynamic gamma
- Supports write back only for verification.

The following figure shows the diagram of DE system.

Figure 5-1 DE System Block Diagram



5.2 Graphic 2D Engine (G2D)

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Supports layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer

5.3 Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPGE). The VE supports H.264 and H.265 encoding, and JPGE supports JPEG/MJPEG encoding.

5.3.1 VE

The VE is a CODEC that supports H.264 and H.265 protocol based on ASIC. It is custom-made for the IPC usage and features high compressing rate, low CPU usage, short delay and low power consumption.

The VE has the following features:

- Supports ITU-T H.265 Main Profile @Level 4.1 Main-Tier encoding
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four prediction unit (PU) types of 16x16, 16x8, 8x16 and 8x8 for inter-prediction
  - Three PU types of 16x16, 8x8 and 4x4 for intra-prediction
  - Max merge candidate number is 2
  - Supports three transform uinit size: 16x16, 8x8 and 4x4
  - De-blocking filtering
- Supports ITU-T H.264 high profile /Main Profile/baseline profile @Level 5.0 encoding.
  - Motion compensation with 1/2 or 1/4 pixel precision
  - Four prediction unit (PU) types of 16x16, 16x8, 8x16 and 8x8 for inter-prediction
  - Three PU types of 16x16, 8x8 and 4x4 for intra-frame
  - Transform 4x4 and transform 8x8
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
  - Multi-slice encoding
- Supports QPMap function.
- Supports special functions: variable frame rate (VFR), 2-D filtering, dynamic search window range
- Supports normal functions: Macroblock rate control, 2D and 3D denoising, intra-refresh, inter-only-in-P-frame
- Statistical information output based on 16x16 QP\MAD\SSE
- Supports output picture format of semi-planar YCbCr4:2:0.
- picture resolutions
  - Minimum picture resolution: 64x64 for I frame, 176x32 for P frame.

- Maximum picture resolution: 4096x4096

- Supports region of interest(ROI) encoding.
  - A maximum of eight ROIs
  - Independent enable/disable control for the encoding function of each ROI
- Supports three bit rate control modes: constant bit rate(CBR), variable bit rate(VBR), and FIXEDQP.
- Supports the output bit rate ranging from 2 Kbit/s to 100 Mbit/s.
- Supports loss and lossless compression for reference frame.
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of sixty-four regions
  - OSD overlaying with any size and at any position (within the size and position ranges of the picture)
  - Supports four adaptive anti-color modes and optional width/height of 16, 32 or 64 for anti-color units
  - OSD overlaying control (enabled or disabled)
- input frame supports loss and lossless compression mode

5.3.2 JPEG

The JPGE is a high-performance JPEG encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPGE has the following features:

- ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
  - Supports multiple input picture formats:
    - Semi-planar YCbCr4:2:0
    - YCbCr4:2:2
    - YCbCr4:4:4
  - Supports configurable picture resolutions:
    - Minimum picture resolution: 192x96
    - Maximum picture resolution: 8192x8192
  - Supports configurable quantization tables.
    - An independent quantization table for the Y component, Cb component, and Cr component respectively.
- Supports OSD front-end overlaying.
  - OSD overlaying before encoding for a maximum of sixty-four regions

- OSD overlaying with any size and at any position (within the size and position ranges of the picture)
- Supports four adaptive anti-color modes and optional width/height of 16, 32 or 64 for anti-color units
- OSD overlaying control (enabled or disabled)

- input frame supports loss and lossless compression mode

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6 Video Input Interfaces

6.1 GDC

Geometric Distortion Correction (GDC) is located between the ISP and the Encoder, it is a hardware accelerator for image distortion correction of continuous video images acquired by Sensor. The GDC module include FishEye Correction (FEC), and the Lens Distortion Correction (LDC). The FEC module corrects the fisheye images to fit user habits, and the LDC module removes the image distortion of wide angle lens.

Features

- Supports FEC , including 360 panoramic mode, 180 panoramic mode, 360 split panoramic mode, normal mode and Fish2Wide mode
- Supports LDC and LDC Pro
- Supports BirdsEye Correction
- Supports Perspective Correction
- Supports user mode.to customize the mapping algorithm for pixel-level operations
- Supports hardware acceleration for interpolation
- Supports horizontal flip and 90/180/270 degree rotation

Performance

Supports frame rate of 4K@30fps

Input

- Data format: YUV420p/YUV420sp
- supports the input of images compressed by AW-LBC
- Input resolution
  - Minimum: 64 x 64
  - Maximum: 4080 x 4080
- The width must be 16x-aligned and the height must be 8x-aligned
- The FEC input needs to be a spherical fisheye image with the same width and height

Output

- Data format: YUV420sp
- Only uncompressed image is supported
- Output resolution
  - Minimum: 64x64
  - Maximum: 4096x4096
- The width and height must be 16x-aligned

6.2 CSIC

6.2.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface and store the data in memory directly.

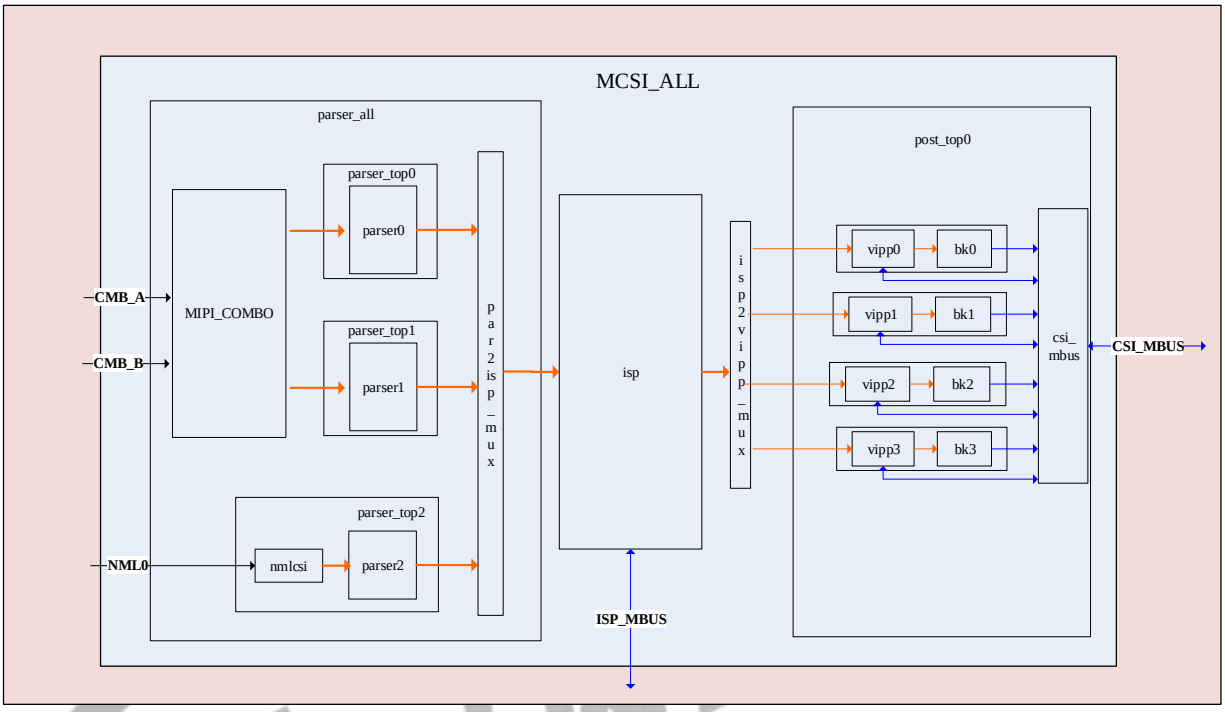
The CSIC includes the following features:

- Supports one 4-lane or two 2-lane MIPI Interface
  - Supports MIPI CSI2 V1.1 and MIPI DPHY V1.1
  - Supports MIPI DPHY V1.1
  - Supports 1.2 Gbps/lane
- Supports 12-bit digital camera interface
- Supports BT656 interface
  - Supports time-multiplexed format
  - Supports dual data rate sample mode with pixel clock up to 148.5MHz
- Supports BT601 Interface
- Supports crop function
- Supports frame rate down
- Supports 4 DMA for 4 video stream storage
  - Supports deinterlacing for interlace video input
  - Supports conversion for YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
  - Supports horizontal and vertical flip

6.2.2 Block Diagram

The following shows block diagram of the CSIC.

Figure 6-1 CSIC Block Diagram



6.2.3 Functional Description

6.2.3.1 External Signals

Table 6-1 CSIC External Signals

Signal	Description	Type
MIPI CSI		
MIPI-CSI-MCLK0	Master Clock for MIPI Sensor	O
MIPI-CSI-MCLK1	Master Clock for MIPI Sensor	O
CSI-SM-VS	MIPI CSI Slave Mode Vertical SYNC	O
MIPIA-CSI-CK0N	MIPI CSI controller A clock negative signal	AI
MIPIA-CSI-CK0P	MIPI CSI controller A clock positive signal	AI
MIPIA-CSI-D0N	MIPI CSI controller A data0 negative signal	AI
MIPIA-CSI-D0P	MIPI CSI controller A data0 positive signal	AI
MIPIA-CSI-D1N	MIPI CSI controller A data1 negative signal	AI
MIPIA-CSI-D1P	MIPI CSI controller A data1 positive signal	AI
MIPIB-CSI-CK0N	MIPI CSI controller B clock negative signal	AI
MIPIB-CSI-CK0P	MIPI CSI controller B clock positive signal	AI

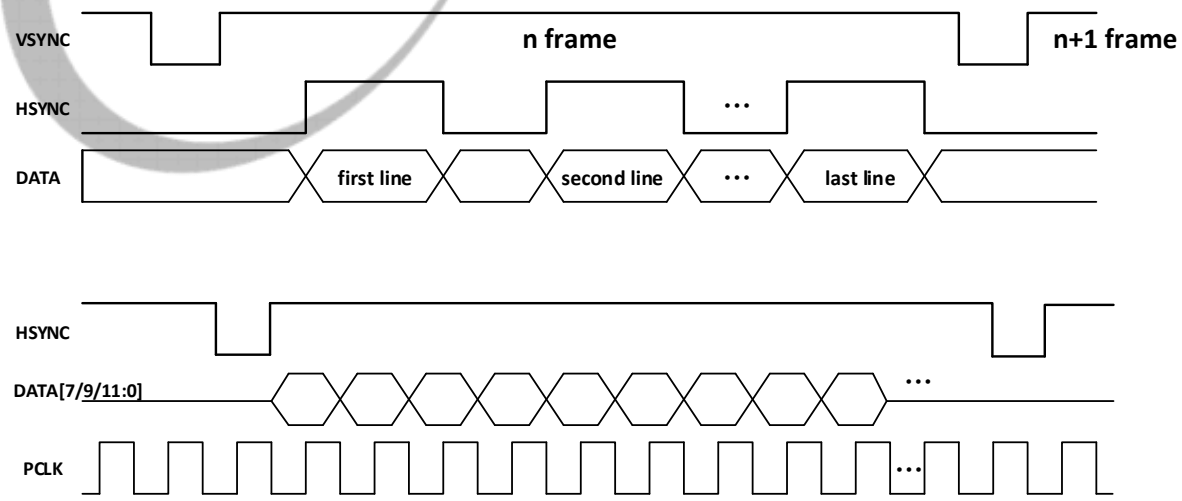
Signal	Description	Type
MIPIB-CSI-D0N/MIPIA-CSI-D2N	MIPI CSI controller B data0 negative signal/ MIPI CSI controller A data2 negative signal	AI
MIPIB-CSI-D0P/MIPIA-CSI-D2P	MIPI CSI controller B data0 positive signal/ MIPI CSI controller A data3 positive signal	AI
MIPIB-CSI-D1N/MIPIA-CSI-D3N	MIPI CSI controller B data1 negative signal/ MIPI CSI controller A data3 negative signal	AI
MIPIB-CSI-D1P/MIPIA-CSI-D3P	MIPI CSI controller B data1 positive signal/ MIPI CSI controller A data3 positive signal	AI
Parallel CSI		
NCSI-D[9:0]	Parallel CSI Data Bit	I
NCSI-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI-MCLK	Parallel CSI Master Clock	O
NCSI-PCLK	Parallel CSI Pixel Clock	I

6.2.3.2 Typical Application

CSIC Input Timing

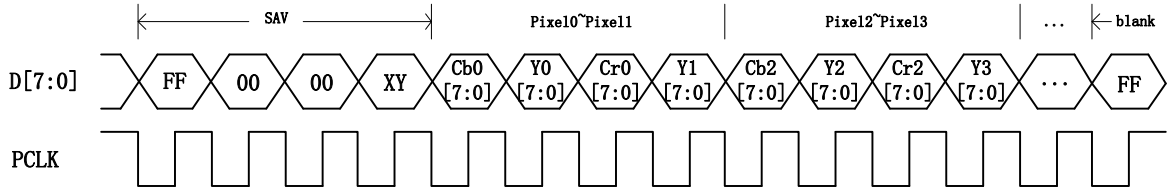
The following figure shows the timing of 8bit CMOS Sensor Interface, in this figure clock active at the rising edge, VSYNC valid at positive, HSYNC valid at positive.

Figure 6-2 8-bit DC Sensor Interface Timing



The following figure shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT656).

Figure 6-3 8-bit YCbCr4:2:2 with embedded syncs (BT656)



The following table shows the header code of BT656.

Table 6-2 BT656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

The following table shows the Header Data Bit Definition of BT656.

Table 6-3 BT656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

CSIC Memory Storage

The following table describes the memory storage of pixel data.

Table 6-4 CSIC Memory Storages

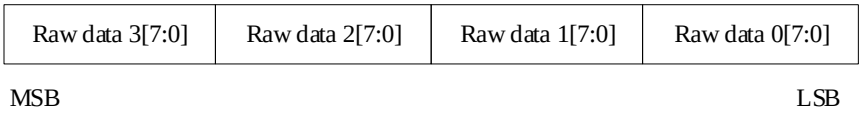
Input format	YUV422/YUV420		Raw
Output format	Planar	UV combined	Raw
FIFO0	Y	Y	All pixels data
FIFO1	Cb (U)	CbCr (UV)	-

Input format	YUV422/YUV420		Raw
FIFO2	Cr (V)	-	-

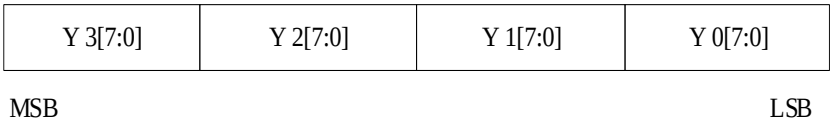
The following figure shows the Pixel Format Arrangement.

Figure 6-4 Pixel Format Arrangement

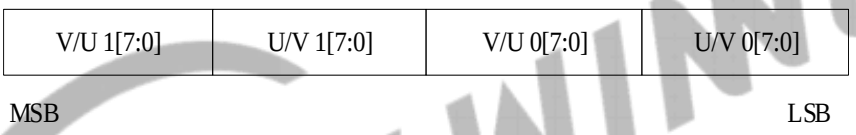
RAW-8:



Y:



UV Combined:



6.2.3.3 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

For YUV422 format, pixel unit is a YU/YV combination.

For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.

For Bayer and RAW format, pixel unit is a R/G/B single component.

For RGB565, pixel unit is 2 bytes of RGB565 package.

For RGB888, pixel unit is 3 bytes of RGB combination.

6.2.3.4 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of Y0U0Y1V1 will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of Y1U0Y0V1 will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

6.2.4 Register List

Module Name	Base Address	Comments
CSIC_CCU	0x05800000	
CSIC_TOP	0x05800800	
CSIC_PARSER0	0x05820000	
CSIC_PARSER1	0x05821000	CSIC_PARSER1 register is the same with CSIC_PARSER0.
CSIC_PARSER2	0x05822000	CSIC_PARSER2 register is the same with CSIC_PARSER0.
CSIC_DMA0	0x05830000	
CSIC_DMA1	0x05831000	CSIC_DMA1 register is the same with CSIC_DMA0.
CSIC_DMA2	0x05832000	CSIC_DMA2 register is the same with CSIC_DMA0.
CSIC_DMA3	0x05833000	CSIC_DMA3 register is the same with CSIC_DMA0.

Register Name	Offset	Description
CSIC_CCU		
CSIC_CCU_CLK_MODE_REG	0x0000	CSIC CCU Clock Mode Register
CSIC_CCU_PARSER_CLK_EN_REG	0x0004	CSIC CCU Parser Clock Enable Register
CSIC_CCU_POST0_CLK_EN_REG	0x000C	CSIC CCU Post0 Clock Enable Register
CSIC_TOP		
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_BIST_CTRL_REG	0x00E0	CSIC BIST Control Register

Register Name	Offset	Description
CSIC_BIST_START_ADDR_REG	0x00E4	CSIC BIST Start Address Register
CSIC_BIST_END_ADDR_REG	0x00E8	CSIC BIST End Address Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_FEATURE_LIST_REG	0x01F0	CSIC Feature List Register
CSIC_PARSER0		
CSIC_PRS_EN_REG	0x0000	CSIC Parser Enable Register
CSIC_PRS_NCSIC_IF_CFG_REG	0x0004	CSIC Parser NCSIC Interface Configuration Register
CSIC_PRS_CAP_REG	0x000C	CSIC Parser Capture Register
CSIC_PRS_SIGNAL_STA_REG	0x0010	CSIC Parser Signal Status Register
CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	CSIC Parser NCSIC BT656 Header Configuration Register
CSIC_PRS_CH0_INFMT_REG	0x0024	CSIC Parser Channel_0 Input Format Register
CSIC_PRS_CH0_OUTPUT_HSIZE_REG	0x0028	CSIC Parser Channel_0 Output Horizontal Size Register
CSIC_PRS_CH0_OUTPUT_VSIZE_REG	0x002C	CSIC Parser Channel_0 Output Vertical Size Register
CSIC_PRS_CH0_INPUT_PARA0_REG	0x0030	CSIC Parser Channel_0 Input Parameter0 Register
CSIC_PRS_CH0_INPUT_PARA1_REG	0x0034	CSIC Parser Channel_0 Input Parameter1 Register
CSIC_PRS_CH0_INPUT_PARA2_REG	0x0038	CSIC Parser Channel_0 Input Parameter2 Register
CSIC_PRS_CH0_INPUT_PARA3_REG	0x003C	CSIC Parser Channel_0 Input Parameter3 Register
CSIC_PRS_CH0_INT_EN_REG	0x0040	CSIC Parser Channel_0 Interrupt Enable Register
CSIC_PRS_CH0_INT_STA_REG	0x0044	CSIC Parser Channel_0 Interrupt Status Register
CSIC_PRS_CH0_LINE_TIME_REG	0x0048	CSIC Parser Channel_0 Line Time Register
CSIC_PRS_CH1_INFMT_REG	0x0124	CSIC Parser Channel_1 Input Format Register
CSIC_PRS_CH1_OUTPUT_HSIZE_REG	0x0128	CSIC Parser Channel_1 Output Horizontal Size Register
CSIC_PRS_CH1_OUTPUT_VSIZE_REG	0x012C	CSIC Parser Channel_1 Output Vertical Size Register
CSIC_PRS_CH1_INPUT_PARA0_REG	0x0130	CSIC Parser Channel_1 Input Parameter0 Register
CSIC_PRS_CH1_INPUT_PARA1_REG	0x0134	CSIC Parser Channel_1 Input Parameter1 Register
CSIC_PRS_CH1_INPUT_PARA2_REG	0x0138	CSIC Parser Channel_1 Input Parameter2 Register
CSIC_PRS_CH1_INPUT_PARA3_REG	0x013C	CSIC Parser Channel_1 Input Parameter3 Register
CSIC_PRS_CH1_INT_EN_REG	0x0140	CSIC Parser Channel_1 Interrupt Enable Register
CSIC_PRS_CH1_INT_STA_REG	0x0144	CSIC Parser Channel_1 Interrupt Status Register
CSIC_PRS_CH1_LINE_TIME_REG	0x0148	CSIC Parser Channel_1 Line Time Register
CSIC_PRS_CH2_INFMT_REG	0x0224	CSIC Parser Channel_2 Input Format Register
CSIC_PRS_CH2_OUTPUT_HSIZE_REG	0x0228	CSIC Parser Channel_2 Output Horizontal Size Register
CSIC_PRS_CH2_OUTPUT_VSIZE_REG	0x022C	CSIC Parser Channel_2 Output Vertical Size Register
CSIC_PRS_CH2_INPUT_PARA0_REG	0x0230	CSIC Parser Channel_2 Input Parameter0 Register
CSIC_PRS_CH2_INPUT_PARA1_REG	0x0234	CSIC Parser Channel_2 Input Parameter1 Register
CSIC_PRS_CH2_INPUT_PARA2_REG	0x0238	CSIC Parser Channel_2 Input Parameter2 Register

Register Name	Offset	Description
CSIC_PRS_CH2_INPUT_PARA3_REG	0x023C	CSIC Parser Channel_2 Input Parameter3 Register
CSIC_PRS_CH2_INT_EN_REG	0x0240	CSIC Parser Channel_2 Interrupt Enable Register
CSIC_PRS_CH2_INT_STA_REG	0x0244	CSIC Parser Channel_2 Interrupt Status Register
CSIC_PRS_CH2_LINE_TIME_REG	0x0248	CSIC Parser Channel_2 Line Time Register
CSIC_PRS_CH3_INFMT_REG	0x0324	CSIC Parser Channel_3 Input Format Register
CSIC_PRS_CH3_OUTPUT_HSIZE_REG	0x0328	CSIC Parser Channel_3 Output Horizontal Size Register
CSIC_PRS_CH3_OUTPUT_VSIZE_REG	0x032C	CSIC Parser Channel_3 Output Vertical Size Register
CSIC_PRS_CH3_INPUT_PARA0_REG	0x0330	CSIC Parser Channel_3 Input Parameter0 Register
CSIC_PRS_CH3_INPUT_PARA1_REG	0x0334	CSIC Parser Channel_3 Input Parameter1 Register
CSIC_PRS_CH3_INPUT_PARA2_REG	0x0338	CSIC Parser Channel_3 Input Parameter2 Register
CSIC_PRS_CH3_INPUT_PARA3_REG	0x033C	CSIC Parser Channel_3 Input Parameter3 Register
CSIC_PRS_CH3_INT_EN_REG	0x0340	CSIC Parser Channel_3 Interrupt Enable Register
CSIC_PRS_CH3_INT_STA_REG	0x0344	CSIC Parser Channel_3 Interrupt Status Register
CSIC_PRS_CH3_LINE_TIME_REG	0x0348	CSIC Parser Channel_3 Line Time Register
CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	CSIC Parser NCSIC RX Signal0 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	CSIC Parser NCSIC RX Signal5 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	CSIC Parser NCSIC RX Signal6 Delay Adjust Register
CSIC_PRS_SYNC_EN_REG	0x0520	CSIC Parser SYNC EN Register
CSIC_PRS_SYNC_CFG_REG	0x0524	CSIC Parser SYNC CFG Register
SIC_PRS_VS_WAIT_N_REG	0x0528	CSIC Parser VS WAIT N Register
CSIC_PRS_VS_WAIT_M_REG	0x052C	CSIC Parser VS WAIT M Register
CSIC_PRS_XSYNC_ENABLE_REG	0x0540	CSIC Parser XSYNC ENABLE Register
CSIC_PRS_XVS_PERIOD_REG	0x0544	CSIC Parser XVS Period Register
CSIC_PRS_XHS_PERIOD_REG	0x0548	CSIC Parser XHS Period Register
CSIC_PRS_XVS_LENGTH_REG	0x054C	CSIC Parser XVS LENGTH Register
CSIC_PRS_XHS_LENGTH_REG	0x0550	CSIC Parser XHS LENGTH Register
CSIC_PRS_SYNC_DLY_REG	0x0554	CSIC Parser SYNC DELAY Register
CSIC_DMA0		
CSIC_DMA_TOP_REG	0x0000	CSIC DMA TOP Register
CSIC_DMA_MUL_CH_CFG_REG	0x0004	CSIC DMA Multi-Channel Configuration Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0010	CSIC DMA Frame Rate Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0014	CSIC DMA Accumulated and Internal Clock Counter Register
CSIC_DMA_FS_FRM_CNT_REG	0x0020	CSIC DMA Fsync Frame Counter Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_VE_FRM_CNT_REG	0x0050	CSIC DMA VE Frame Counter Value Register

Register Name	Offset	Description
CSIC_DMA_VE_LINE_CNT_REG	0x0054	CSIC DMA VE Line Counter Value Register
CSIC_DMA_VE_CUR_FRM_ADDR_REG	0x0058	CSIC DMA VE Current Frame Address Register
CSIC_DMA_VE_LAST_FRM_ADDR_REG	0x005C	CSIC DMA VE Last Frame Address Register
CSIC_DMA_FIFO_STAT_REG	0x0080	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x0084	CSIC DMA FIFO Threshold Register
CSIC_DMA_TOP_INT_EN_REG	0x0100	CSIC DMA TOP Interrupt Enable Register
CSIC_DMA_TOP_INT_STA_REG	0x0104	CSIC DMA TOP Interrupt Status Register
CSIC_DMA_FEATURE_REG	0x01F4	CSIC DMA Feature List Register
CSIC_DMA_CH0_EN_REG	0x0200	CSIC DMA Channel0 Enable Register
CSIC_DMA_CH0_CFG_REG	0x0204	CSIC DMA Channel0 Configuration Register
CSIC_DMA_CH0_FRM_LOST_CNT_REG	0x0208	CSIC DMA Channel0 Frame Lost Counter Register
CSIC_DMA_CH0_HSIZE_REG	0x0210	CSIC DMA Channel0 Horizontal Size Register
CSIC_DMA_CH0_VSIZE_REG	0x0214	CSIC DMA Channel0 Vertical Size Register
CSIC_DMA_CH0_F0_BUFA_REG	0x0220	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH0_F0_BUFA_RESULT_REG	0x0224	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F1_BUFA_REG	0x0228	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH0_F1_BUFA_RESULT_REG	0x022C	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F2_BUFA_REG	0x0230	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH0_F2_BUFA_RESULT_REG	0x0234	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH0_BUF_LEN_REG	0x0238	CSIC DMA Channel0 Buffer Length Register
CSIC_DMA_CH0_FLIP_SIZE_REG	0x023C	CSIC DMA Channel0 Flip Size Register
CSIC_DMA_CH0_CAP_STA_REG	0x024C	CSIC DMA Channel0 Capture Status Register
CSIC_DMA_CH0_INT_EN_REG	0x0250	CSIC DMA Channel0 Interrupt Enable Register
CSIC_DMA_CH0_INT_STA_REG	0x0254	CSIC DMA Channel0 Interrupt Status Register
CSIC_DMA_CH0_LINE_CNT_REG	0x0258	CSIC DMA Channel0 Line Counter Register
CSIC_DMA_CH0_LINE_STAT_REG	0x0268	CSIC DMA Channel0 Line Statistic Register
CSIC_DMA_CH0_PCLK_STAT_REG	0x0270	CSIC DMA Channel0 PCLK Statistic Register
CSIC_LBC_CH0_CONFIG_REG	0x0300	CSIC LBC Channel0 Configure Register
CSIC_LBC_CH0_LINE_TAR_BIT0_REG	0x0304	CSIC LBC Channel0 Line Target Bit0 Register
CSIC_LBC_CH0_LINE_TAR_BIT1_REG	0x0308	CSIC LBC Channel0 Line Target Bit1 Register
CSIC_LBC_CH0_RC_ADV_REG	0x030C	CSIC LBC Channel0 RC ADV Register
CSIC_LBC_CH0_MB_MIN_REG	0x0310	CSIC LBC Channel0 MB MIN Register
CSIC_DMA_CH1_EN_REG	0x0400	CSIC DMA Channel1 Enable Register
CSIC_DMA_CH1_CFG_REG	0x0404	CSIC DMA Channel1 Configuration Register

Register Name	Offset	Description
CSIC_DMA_CH1_FRM_LOST_CNT_REG	0x0408	CSIC DMA Channel1 Frame Lost Counter Register
CSIC_DMA_CH1_HSIZE_REG	0x0410	CSIC DMA Channel1 Horizontal Size Register
CSIC_DMA_CH1_VSIZE_REG	0x0414	CSIC DMA Channel1 Vertical Size Register
CSIC_DMA_CH1_F0_BUFA_REG	0x0420	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH1_F0_BUFA_RESULT_REG	0x0424	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F1_BUFA_REG	0x0428	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH1_F1_BUFA_RESULT_REG	0x042C	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F2_BUFA_REG	0x0430	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH1_F2_BUFA_RESULT_REG	0x0434	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH1_BUF_LEN_REG	0x0438	CSIC DMA Channel1 Buffer Length Register
CSIC_DMA_CH1_FLIP_SIZE_REG	0x043C	CSIC DMA Channel1 Flip Size Register
CSIC_DMA_CH1_CAP_STA_REG	0x044C	CSIC DMA Channel1 Capture Status Register
CSIC_DMA_CH1_INT_EN_REG	0x0450	CSIC DMA Channel1 Interrupt Enable Register
CSIC_DMA_CH1_INT_STA_REG	0x0454	CSIC DMA Channel1 Interrupt Status Register
CSIC_DMA_CH1_LINE_CNT_REG	0x0458	CSIC DMA Channel1 Line Counter Register
CSIC_DMA_CH1_LINE_STAT_REG	0x0468	CSIC DMA Channel1 Line Statistic Register
CSIC_DMA_CH1_PCLK_STAT_REG	0x0470	CSIC DMA Channel1 PCLK Statistic Register
CSIC_LBC_CH1_CONFIG_REG	0x0500	CSIC LBC Channel1 Configure Register
CSIC_LBC_CH1_LINE_TAR_BIT0_REG	0x0504	CSIC LBC Channel1 Line Target Bit0 Register
CSIC_LBC_CH1_LINE_TAR_BIT1_REG	0x0508	CSIC LBC Channel1 Line Target Bit1 Register
CSIC_LBC_CH1_RC_ADV_REG	0x050C	CSIC LBC Channel1 RC ADV Register
CSIC_LBC_CH1_MB_MIN_REG	0x0510	CSIC LBC Channel1 MB MIN Register
CSIC_DMA_CH2_EN_REG	0x0600	CSIC DMA Channel2 Enable Register
CSIC_DMA_CH2_CFG_REG	0x0604	CSIC DMA Channel2 Configuration Register
CSIC_DMA_CH2_FRM_LOST_CNT_REG	0x0608	CSIC DMA Channel2 Frame Lost Counter Register
CSIC_DMA_CH2_HSIZE_REG	0x0610	CSIC DMA Channel2 Horizontal Size Register
CSIC_DMA_CH2_VSIZE_REG	0x0614	CSIC DMA Channel2 Vertical Size Register
CSIC_DMA_CH2_F0_BUFA_REG	0x0620	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH2_F0_BUFA_RESULT_REG	0x0624	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F1_BUFA_REG	0x0628	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH2_F1_BUFA_RESULT_REG	0x062C	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register

Register Name	Offset	Description
CSIC_DMA_CH2_F2_BUFA_REG	0x0630	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH2_F2_BUFA_RESULT_REG	0x0634	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH2_BUF_LEN_REG	0x0638	CSIC DMA Channel2 Buffer Length Register
CSIC_DMA_CH2_FLIP_SIZE_REG	0x063C	CSIC DMA Channel2 Flip Size Register
CSIC_DMA_CH2_CAP_STA_REG	0x064C	CSIC DMA Channel2 Capture Status Register
CSIC_DMA_CH2_INT_EN_REG	0x0650	CSIC DMA Channel2 Interrupt Enable Register
CSIC_DMA_CH2_INT_STA_REG	0x0654	CSIC DMA Channel2 Interrupt Status Register
CSIC_DMA_CH2_LINE_CNT_REG	0x0658	CSIC DMA Channel2 Line Counter Register
CSIC_DMA_CH2_LINE_STAT_REG	0x0668	CSIC DMA Channel2 Line Statistic Register
CSIC_DMA_CH2_PCLK_STAT_REG	0x0670	CSIC DMA Channel2 PCLK Statistic Register
CSIC_LBC_CH2_CONFIG_REG	0x0700	CSIC LBC Channel2 Configure Register
CSIC_LBC_CH2_LINE_TAR_BIT0_REG	0x0704	CSIC LBC Channel2 Line Target Bit0 Register
CSIC_LBC_CH2_LINE_TAR_BIT1_REG	0x0708	CSIC LBC Channel2 Line Target Bit1 Register
CSIC_LBC_CH2_RC_ADV_REG	0x070C	CSIC LBC Channel2 RC ADV Register
CSIC_LBC_CH2_MB_MIN_REG	0x0710	CSIC LBC Channel2 MB MIN Register
CSIC_DMA_CH3_EN_REG	0x0800	CSIC DMA Channel3 Enable Register
CSIC_DMA_CH3_CFG_REG	0x0804	CSIC DMA Channel3 Configuration Register
CSIC_DMA_CH3_FRM_LOST_CNT_REG	0x0808	CSIC DMA Channel3 Frame Lost Counter Register
CSIC_DMA_CH3_HSIZE_REG	0x0810	CSIC DMA Channel3 Horizontal Size Register
CSIC_DMA_CH3_VSIZE_REG	0x0814	CSIC DMA Channel3 Vertical Size Register
CSIC_DMA_CH3_F0_BUFA_REG	0x0820	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH3_F0_BUFA_RESULT_REG	0x0824	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F1_BUFA_REG	0x0828	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH3_F1_BUFA_RESULT_REG	0x082C	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F2_BUFA_REG	0x0830	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH3_F2_BUFA_RESULT_REG	0x0834	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH3_BUF_LEN_REG	0x0838	CSIC DMA Channel3 Buffer Length Register
CSIC_DMA_CH3_FLIP_SIZE_REG	0x083C	CSIC DMA Channel3 Flip Size Register
CSIC_DMA_CH3_CAP_STA_REG	0x084C	CSIC DMA Channel3 Capture Status Register
CSIC_DMA_CH3_INT_EN_REG	0x0850	CSIC DMA Channel3 Interrupt Enable Register
CSIC_DMA_CH3_INT_STA_REG	0x0854	CSIC DMA Channel3 Interrupt Status Register
CSIC_DMA_CH3_LINE_CNT_REG	0x0858	CSIC DMA Channel3 Line Counter Register
CSIC_DMA_CH3_LINE_STAT_REG	0x0868	CSIC DMA Channel3 Line Statistic Register
CSIC_DMA_CH3_PCLK_STAT_REG	0x0870	CSIC DMA Channel3 PCLK Statistic Register

Register Name	Offset	Description
CSIC_LBC_CH3_CONFIG_REG	0x0900	CSIC LBC Channel3 Configure Register
CSIC_LBC_CH3_LINE_TAR_BIT0_REG	0x0904	CSIC LBC Channel3 Line Target Bit0 Register
CSIC_LBC_CH3_LINE_TAR_BIT1_REG	0x0908	CSIC LBC Channel3 Line Target Bit1 Register
CSIC_LBC_CH3_RC_ADV_REG	0x090C	CSIC LBC Channel3 RC ADV Register
CSIC_LBC_CH3_MB_MIN_REG	0x0910	CSIC LBC Channel3 MB MIN Register

6.2.5 CSIC CCU Register Description

6.2.5.1 0x0000 CSIC CCU Clock Mode Register (Default Value:0x8000_0000)

Offset: 0x0000			Register Name: CSIC_CCU_CLK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	CSIC_CCU_CLK_GATING_DISABLE Disable All CSIC CCU Clock Gating 0: CCU Clock Gating Registers(0x0004~0x0010) effect 1:CCU Clock Gating Registers(0x0004~0x0010) not effect
30:0	/	/	/

6.2.5.2 0x0004 CSIC CCU Parser Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE 0: Combo0 clock disable 1: Combo0 clock enable
7:3	/	/	/
2	R/W	0x0	MCSI_PARSER2_CLK_ENABLE 0: CSI Parser2 clock disable 1: CSI Parser2 clock enable
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE Parser0 clock gating 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

6.2.5.3 0x000C CSIC CCU Post0 Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE Post0 clock gating 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0: VIPP1 clock disable 1: VIPP1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE 0: VIPP0 clock disable 1: VIPP0 clock enable, when MCSI_POST0_CLK_ENABLE is 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE 0: BK3 clock disable 1: BK3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE BK1 clock gating 0: BK1 clock disable 1: BK1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE BK0 clock gating 0: BK0 clock disable 1: BK0 clock enable, when MCSI_POST0_CLK_ENABLE is 1

6.2.6 CSIC TOP Register Description

6.2.6.1 0x0000 CSIC TOP Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN CSIC Version Register Read Enable: 0: Disable 1: Enable
30:3	/	/	/
2	R/W	0x0	BIST_MODE_EN CSIC Memory BIST Enable 0: Closed 1: EN BIST TEST
1	/	/	/
0	R/W	0x0	CSIC_TOP_EN CSIC TOP Module Enable 0: Reset and disable the CSIC module 1: Enable the CSIC module

6.2.6.2 0x0004 CSIC Pattern Generation Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:9	/	/	/
7:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software write this bit to “1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to “0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

6.2.6.3 0x0008 CSIC Pattern Control Register (Default Value:0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 010: NCSIC0 011: NCSIC1 100: NCSIC2 101: NCSIC3 110: Combo others: reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH Pattern Generator output data width 00:8bit 01:10bit 10:12bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000: MIPI 1-lane 0001: MIPI 2-lane 0010: MIPI 3-lane 0011: MIPI 4-lane 0100:NCSIC with max 12-bit data （{field,VSYN,HSYN,1'b0,data[11:0]}） 0101:NCSIC with max 16-bit data （{12'h0,field,VSYN,HSYN,1'b0,data[15:0]}） 0110:NCSIC with max 24-bit data （{field,VSYN,HSYN,5'h0,data[23:0]}） 0111: reserved 1000:BT656 8 bits' width 1001:BT656 16 bits' width 1010:BT656 24 bits' width 1011: reserved 1100: BAYER 12 bits for ISPFE 1101: UYVY422 12 bits for ISPFE 1110: UYVY420 12 bits for ISPFE 1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

6.2.6.4 0x0020 CSIC Pattern Generation Length Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

6.2.6.5 0x0024 CSIC Pattern Generation Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

6.2.6.6 0x0028 CSIC Pattern ISP Size Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

6.2.6.7 0X0030 CSIC ISP0 Input0 Select Register (Default Value:0x0000_0000)

Offset :0X0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	ISP0 Input0 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.8 0X0034 CSIC ISP0 Input1 Select Register (Default Value:0x0000_0001)

Offset :0X0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x1	ISP0 Input1 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.9 0X0038 CSIC ISP0 Input2 Select Register (Default Value:0x0000_0002)

Offset :0X0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x2	ISP0 Input2 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.10 0X003C CSIC ISP0 Input3 Select Register (Default Value:0x0000_0003)

Offset :0X003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	ISP0 Input3 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.11 0X0040 CSIC ISP1 Input0 Select Register (Default Value:0x0000_0004)

Offset :0X0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x4	ISP1 Input0 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.12 0X0044 CSIC ISP1 Input1 Select Register (Default Value:0x0000_0005)

Offset :0X0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x5	ISP1 Input1 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.13 0X0048 CSIC ISP1 Input2 Select Register (Default Value:0x0000_0006)

Offset :0X0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x6	ISP1 Input2 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.14 0X004C CSIC ISP1 Input3 Select Register (Default Value:0x0000_0007)

Offset :0X004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x7	ISP1 Input3 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 Others: reserved

6.2.6.15 0X00A0 CSIC DMA0 Input Select Register (Default Value:0x0000_0000)

Offset :0X00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset :0X00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	DMA0 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.2.6.16 0X00A4 CSIC DMA1 Input Select Register (Default Value:0x0000_0000)

Offset :0X00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA1 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.2.6.17 0X00A8 CSIC DMA2 Input Select Register (Default Value:0x0000_0000)

Offset :0X00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

Offset :0X00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	DMA2 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.2.6.18 0X00AC CSIC DMA3 Input Select Register (Default Value:0x0000_0000)

Offset :0X00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA3 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: reserved

6.2.6.19 0x00E0 CSIC BIST Control Register (Default Value:0x0000_0200)

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0:NO effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R	0x1	BIST_STOP BIST STOP 0: running 1:STOP
8	R	0x0	BIST_BUSY BIST Busy 0: idle 1:busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select
4	R/W	0x0	BIST_ADDR_Mode_SEL BIST Address mode select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write data Pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST Enable. A positive will trigger the BIST to start.

6.2.6.20 0x00E4 CSIC BIST Start Address Register (Default Value:0x0000_0000)

Offset:0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST Start Address BIST Start Address. It is 32-bit aligned.

6.2.6.21 0x00E8 CSIC BIST End Address Register (Default Value:0x0000_0000)

Offset:0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST END Address BIST END Address. It is 32-bit aligned.

6.2.6.22 0x00EC CSIC BIST Data Mask Register (Default Value:0x0000_0000)

Offset:0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0: Unmask 1:Mask

6.2.6.23 0x00F0 CSIC MBUS REQ MAX Register (Default Value:0x000f_0f0f)

Offset:0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:21	R	0x000	Reserved
20:16	R/W	0x0f	MISP_MEM_REQ_MAX Maximum of request commands for the master granted in MISP_MEM arbiter is N+1.
15:5	/	0x078	/
4:0	R/W	0x0f	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

6.2.6.24 0x0100 CSIC Multi-Frame Mode Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	MULF_STATUS Multi-Frame Mode Status indicates each DMA in frame done pending or not
23:16	/	/	/
15:8	R/W	0x0	MULF_CS Chip Selection for Multi-Frame Mode indicates which DMA is in selected
7:1	/	/	/
0	R/W	0x0	MULF_EN Multi-Frame Mode Enable

6.2.6.25 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
17	R/W1C	0x0	MULF_ERR_PD Multi-Frame Mode Frame Error Interrupt Pending
16	R/W1C	0x0	MULF_DONE_PD Multi-Frame Mode Frame Done Interrupt Pending
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN Multi-Frame Mode Frame Error Interrupt Enable
0	R/W	0x0	MULF_DONE_EN Multi-Frame Mode Frame Done Interrupt Enable

6.2.6.26 0x01F0 CSIC Feature List Register (Default Value:0x3211_4400)

Offset: 0x01F0			Register Name: CSIC_FEATURE_LIST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R	0x3	PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x2	MCSI_NUM Only can be read when version register read enable is on.
23:20	R	0x1	NCSI_NUM Only can be read when version register read enable is on.
19:16	R	0x1	ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x4	DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

6.2.7 CSIC Parser Register

6.2.7.1 0x0000 CSIC Parser Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	NCSIC_EN NCSI Controller Enable 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN NCSI Pixel Clock Gating 0:Gate pclk input 1:Enable pclk input
14:4	/	/	/
3:2	R/W	0x0	PRS_CH_MODE Parser channel mode 00: Parser output channel 0~3 corresponding from input channel 0~3 01: Parser output channel 0~3 all from input channel 0 10:Parser output channel0 and 2 from input channel 0, output channel1 and 3 from input channel 1 11: Reserved
1	R/W	0x0	PRS_MODE Parser Mode 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN Parser Enable 0: Reset and disable the parser module 1: Enable the parser module

6.2.7.2 0x0004 CSIC Parser NCSIC Interface Configuration Register (Default Value:0x0105_0080)

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER YUV420 Input Line Order 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30	/	/	/
29	R/W	0x0	YUV422_SEP When input format is YUV422 16bit or Bt1120, set this bit to transfer YU,YV(2 components for each clock cycle) to Y,U,Y,V(1 component for each clock cycle)
28	/	/	/

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode,the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:20	R/W	0x0	SRC_TYPE Bit 20~23 corresponding to the Source types for channel0~3 0: Progressed 1: Interlaced
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	Field_DT_MODE only valid when CSI_IF is YUV and source type is interlaced 00:by both field and vsync 01:by field 10:by vsync 11:reserved
13	R/W	0x0	DDR_SAMPLE_MODE_EN Dual Data Rate Sample mode Enable 0:disable 1:enable

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH Input Data Width 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100: 2x8/16bit data bus 101:14 bit data bus 110:20 bit data bus,only for packet generator 111:24 bit data bus,only for packet generator
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	/	/	/

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
4:0	R/W	0x0	CSI_IF YUV(separate syncs): 00000: YUYV422/YUV420 or RAW (All data in one data bus) 00001: 2x8 bit YUYV422 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16bit BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16bit BT656(BT1120 like) 2 channels(All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16bit BT656(BT1120 like) 4 channels(All data interleaved in one data bus) Others: Reserved

6.2.7.3 0x0008 CSIC Parser MCSIC Interface Configuration Register (Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/
7:6	R/W	0X2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	/	/	/

6.2.7.4 0x000C CSIC Parser Capture Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/WAC	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
23:22	/	/	/

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
21:18	R/W	0x0	CH2_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	R/WAC	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
15:14	/	/	/
13:10	R/W	0x0	CH1_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	R/WAC	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.
7:6	/	/	/
5:2	R/W	0x0	CH0_FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
0	R/WAC	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared.

6.2.7.5 0x0010 SIC Parser Signal Status Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	FIFO_FULL Indicates the NCSI IN Async FIFO FULL 0:Not Full 1:Full
30:28	R	0x0	PCLK_CNT Indicates the NCSI Pclk is toggle or not
27	R	0x0	VSYNC_STA Indicates the NCSI Vsync Signal status 0:low 1:high
26	R	0x0	HSYNC_STA Indicates the NCSI Hsync Signal status 0:low 1:high
25	R	0x0	FIELD_STA Indicates the NCSI Field Signal status 0:low 1:high
24	R	0x0	DATA_VALID_STA Indicates the NCSI Data Vliad Signal status(n=0~15),MSB for D15,LSB for D0 0:low 1:high
23:0	R	0x0	DATA_STA Indicates the NCSI Data Signal status(n=0~15),MSB for D15,LSB for D0 0:low 1:high

6.2.7.6 0x0014 CSIC Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

6.2.7.7 0x0024 CSIC Parser Channel_0 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0024			Register Name: CSIC_PRS_CH0_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.2.7.8 0x0028 CSIC Parser Channel_0 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0028			Register Name: CSIC_PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.7.9 0x002C. CSIC Parser Channel_0 Output Vertical Size Register Default Value:0x02d0_0000)

Offset: 0x002C			Register Name: CSIC_PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.7.10 0x0030 CSIC Parser Channel_0 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 0 0:Progress 1:Interlace

6.2.7.11 0x0034. CSIC Parser Channel_0 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_PRS_CH0_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.2.7.12 0x0038 CSIC Parser Channel_0 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: CSIC_PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.2.7.13 0x003C. CSIC Parser Channel_0 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: CSIC_PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.2.7.14 0x0040 CSIC Parser Channel_0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.2.7.15 0x0044 CSIC Parser Channel_0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.2.7.16 0x0048 CSIC Parser Channel_0 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_PRS_CH0_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.2.7.17 0x0124 CSIC Parser Channel_1 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0124			Register Name: CSIC_PRS_CH1_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.2.7.18 0x0128 CSIC Parser Channel_1 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0128			Register Name: CSIC_PRS_CH1_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.7.19 0x012C CSIC Parser Channel_1 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x012C			Register Name: CSIC_PRS_CH1_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.7.20 0x0130 CSIC Parser Channel_1 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0130			Register Name: CSIC_PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 1 0:Progress 1:Interlace

6.2.7.21 0x0134 CSIC Parser Channel_1 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0134			Register Name: CSIC_PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.2.7.22 0x0138 CSIC Parser Channel_1 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0138			Register Name: CSIC_PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.2.7.23 0x013C CSIC Parser Channel_1 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.2.7.24 0x0140 CSIC Parser Channel_1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.2.7.25 0x0144 CSIC Parser Channel_1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0144			Register Name: CSIC_PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.2.7.26 0x0148 CSIC Parser Channel_1 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0148			Register Name: CSIC_PRS_CH1_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.2.7.27 0x0224 CSIC Parser Channel_2 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0224			Register Name: CSIC_PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.2.7.28 0x0228 CSIC Parser Channel_2 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0228			Register Name: CSIC_PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.7.29 0x022C CSIC Parser Channel_2 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.7.30 0x0230 CSIC Parser Channel_2 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_PRS_CH2_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 2 0:Progress 1:Interlace

6.2.7.31 0x0234 CSIC Parser Channel_2 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_PRS_CH2_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.2.7.32 0x0238 CSIC Parser Channel_2 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.2.7.33 0x023C CSIC Parser Channel_2 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x023C			Register Name: CSIC_PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.2.7.34 0x0240 CSIC Parser Channel_2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0240			Register Name: CSIC_PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.2.7.35 0x0244 CSIC Parser Channel_2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

6.2.7.36 0x0248 CSIC Parser Channel_2 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0248			Register Name: CSIC_PRS_CH2_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.2.7.37 0x0324 CSIC Parser Channel_3 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0324			Register Name: CSIC_PRS_CH3_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK 16-bit pixel data masks for every 16-cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

6.2.7.38 0x0328 CSIC Parser Channel_3 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0328			Register Name: CSIC_PRS_CH3_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.7.39 0x032C CSIC Parser Channel_3 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x032C			Register Name: CSIC_PRS_CH3_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.7.40 0x0330 CSIC Parser Channel_3 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0330			Register Name: CSIC_PRS_CH3_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 3 0:Progress 1:Interlace

6.2.7.41 0x0334. CSIC Parser Channel_3 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0334			Register Name: CSIC_PRS_CH3_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

6.2.7.42 0x0338 CSIC Parser Channel_3 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0338			Register Name: CSIC_PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

6.2.7.43 0x033C CSIC Parser Channel_3 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x033C			Register Name: CSIC_PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

6.2.7.44 0x0340 CSIC Parser Channel_3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0:disable 1:enable

6.2.7.45 0x0344 CSIC Parser Channel_3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0344			Register Name: CSIC_PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

6.2.7.46 0x0348 CSIC Parser Channel_3 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0348			Register Name: CSIC_PRS_CH3_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

6.2.7.47 0x0500 CSIC Parser NCSIC RX Signal0 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	Filed_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2ns

6.2.7.48 0x050C CSIC Parser NCSIC RX Signal3 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

6.2.7.49 0x0510 CSIC Parser NCSIC RX Signal4 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

6.2.7.50 0x0514 CSIC Parser NCSIC RX Signal5 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

6.2.7.51 0x0518 CSIC Parser NCSIC RX Signal6 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

6.2.7.52 0X0520 CSIC Parser SYNC EN Register (Default Value:0x0000_0000)

Offset :0X0520			Register Name: CSIC_PRS_SYNC_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
19:16	R/W	0x0	VSYNC_MODE Input vsync singal Source select 0: Vsync signals all from 1 parser 1: Vsync signals from 2 parser 2: Vsync signals from 4 parser others:reserved
15:12	/	/	/
11:8	R/W	0x0	VSYNC_SEL Generate sync singal Benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	VSYNC_USED Parser input vsync singal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	FSYNC_OUT_SEL Parser sent sync singal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	FSYNC_MODE Parser sync singal source select 0: From outside 1: Generate by self
0	R/W	0x0	FSYNC_FUN_EN Enable Parser sent sync singal 0: Disable 1: Enable

6.2.7.53 0X0524 CSIC Parser SYNC CFG Register (Default Value:0x0000_0000)

Offset :0X0524			Register Name: CSIC_PRS_SYNC_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	FSYNC_PUL_WID Sync singal pulse width N*T_{24M} , N*T_{24M} ≥4*Tpclk
15:0	R/W	0x0	FYSNC_DISTANCE The interval of two sync signal

6.2.7.54 0X0528 CSIC Parser VS WAIT N Register (Default Value:0x0000_0000)

Offset :0X0528			Register Name: CSIC_PRS_VS_WAIT_N_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come,the max wait time.

6.2.7.55 0X052C CSIC Parser VS WAIT M Register (Default Value:0x0000_0000)

Offset :0X052C			Register Name: CSIC_PRS_VS_WAIT_M_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode,vsync comes at the different time,these bits indicate the max wait time.

6.2.7.56 0X0540. CSIC Parser XSYNC ENABLE Register (Default Value:0x0000_0000)

Offset:0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0x0	XVS_TO_XHS_T The period of XHS delay to XVS, ${XVS_TO_XHS_T}+1 master clock cycles, no more than XHS_LEN
7:5	/	/	/
4	R/W	0x0	XVS_XHS_OUT_SEL When sensor works in slave mode ,this bit select XVS and XHS to output. 0: XHS0,XVS0 1: XHS1,XVS1

Offset:0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	XVS_POL When sensor works in slave mode ,this bit set polarity of XVS. 0: Negative 1: Positive
2	R/W	0x0	XHS_POL When sensor works in slave mode ,this bit set polarity of XHS. 0: Negative 1: Positive
1	R/W	0x0	XVS_OUT_EN When sensor works in slave mode ,this bit enable output XVS to sensor 0: Disable 1: Enable
0	R/W	0x0	XHS_OUT_EN When sensor works in slave mode ,this bit enable output XHS to sensor 0: Disable 1: Enable

6.2.7.57 0X0544 CSIC Parser XVS Period Register (Default Value:0x0000_0000)

Offset:0X0544			Register Name: CSIC_PRS_XVS_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XVS_T The period of XVS signal, ${XVS_T}+2 master clock cycles

6.2.7.58 0X0548 CSIC Parser XHS Period Register (Default Value:0x0000_0000)

Offset:0X0548			Register Name: CSIC_PRS_XHS_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XHS_T The period of XHS signal, ${XHS_T}+2 master clock cycles

6.2.7.59 0X054C CSIC Parser XVS LENGTH Register (Default Value:0x0000_0000)

Offset:0X054C			Register Name: CSIC_PRS_XVS_LENGTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	XVS_LEN The valid length of XVS signal, ${XVS_LEN}+1 master clock cycles

6.2.7.60 0X0550 CSIC Parser XHS LENGTH Register (Default Value:0x0000_0000)

Offset:0X0550			Register Name: CSIC_PRS_XHS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_LEN The valid length of XHS signal, ${XHS_LEN}+1 master clock cycles

6.2.7.61 0X0554 CSIC Parser SYNC DELAY Register (Default Value:0x0000_0000)

Offset:0X0554			Register Name: CSIC_PRS_SYNC_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SYNC_DLY The XHS/XVS will sent after, ${SYNC_DLY}+1 master clock cycles, no more than XVS_LEN

6.2.8 CSIC DMA Register Description

6.2.8.1 0x0000 CSIC DMA TOP Register (Default Value:0x7000_0000)

Offset:0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_EN CSIC DMA Version Register Read Enable: 0: Disable 1: Enable
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE VFLIP buffer address set by software or calculated by hardware 0: hardware 1: software
29	R/W	0x1	BUF_LENGTH_CFG_MODE buffer length set by software or calculated by hardware 0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:17	/	/	/
16	R/W	0x0	FRM_END_FOR_FRM_DONE_SEL Select BK frame end for frame done interrupt generation 0: Frame end from BK input 1:Frame end generated by self

Offset:0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14:13	R/W	0x0	VE_ONLINE_CH_SEL Select BK Channel for VE Online handshake
12	R/W	0x0	VE_ONLINE_HANDSHAKE_EN Set this bit to Enable frame and line counter for VE online handshake
11:10	/	/	/
9:8	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if HFLIP is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes(not Support For DMA1\2\3)
7	/	/	/
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FS_FRM_CNT_EN When BK_TOP_EN enable, this bit set 1 indicate the Frame counter start to add. 0: Disable 1: Enable
4:3	/	/	/
2	R/W	0x0	FRM_RATE_CNT_SPL Sampling time for CLK counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every VSYNC
1	R/W	0x0	FRM_RATE_CNT_EN CLK count per frame enable
0	R/W	0x0	BK_TOP_EN Module Enable 0: Disable 1: Enable

6.2.8.2 0x0004 CSIC DMA Multi-Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
21:20	R	0x0	CUR_OUT_CH When Multi-Channel enable, this field indicates the Current Output Channel ID
19:18	/	/	/
17:16	R	0x0	CUR_IN_CH When Multi-Channel enable, this field indicates the Current Input Channel ID
15:1	/	/	/
0	R/W	0x0	MUL_CH_EN DMA off-line multi-channel enable 0: disable 1: enable

6.2.8.3 0x0010 CSIC DMA Frame Rate Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	FRM_RATE_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

6.2.8.4 0x0014 CSIC DMA Accumulated and Internal Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or VSYNC comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

6.2.8.5 0x0020 CSIC DMA Fsync Frame Counter Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FS_FRM_CNT_CLR When the bit set to 1,Frame CNT clear to 0
30:16	R/W	0x0	FS_FRM_CNT_CLR_DISTANCE Frame CNT clear cycle $N*T_{SYNC}$
15	/	/	/
14:0	R	0x0	FS_FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the REG full, it cleared to 0 . When parser sent a sync signal, it clear to 0

6.2.8.6 0x0040 CSIC DMA Video Input Timeout Threshold0 Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH0 Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , Time Unit is a 12M clock period.

6.2.8.7 0x0044 CSIC DMA Video Input Timeout Threshold1 Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH1 Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

6.2.8.8 0x0048 CSIC DMA Video Input Timeout Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	VI_TCNT_VAL Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

6.2.8.9 0x0050 CSIC DMA VE Frame Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_VE_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	FRM_DONE_CNT Indicates How Many Frame which Stored in DDR
15:8	/	/	/
7:0	R	0x0	FRM_ST_CNT Indicates the Frame Number which is Storing

6.2.8.10 0x0054 CSIC DMA VE Line Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_VE_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_DONE_CNT Indicates How Many Line which Stored in DDR
15:14	/	/	/
13:0	R	0x0	LINE_ST_CNT Indicates the Line Number which is Storing

6.2.8.11 0x0058 CSIC DMA VE Current Frame Address Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_VE_CUR_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_FRM_ADDR Indicates the FIFO0 Address Which Current Frame is Storing

6.2.8.12 0x005C CSIC DMA VE Last Frame Address Register (Default Value:0x0000_0000)

Offset: 0x005C			Register Name: CSIC_DMA_VE_LAST_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LAST_FRM_ADDR Indicates the FIFO0 Address Which Last Frame is Stored

6.2.8.13 0x0080 CSIC DMA FIFO Statistic Register(Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every VSYNC or framedone. Unit is byte.

6.2.8.14 0x0084 CSIC DMA FIFO Threshold Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change. Unit is byte.

6.2.8.15 0x0100 CSIC DMA TOP Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_DMA_TOP_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
1	R/W	0x0	CLR_FS_FRM_CNT_INT_EN Set a INT When Clear FS Frame CNT.
0	R/W	0x0	FS_PUL_INT_EN Set an INT when a FSYNC signal received

6.2.8.16 0x0104 CSIC DMA TOP Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_DMA_TOP_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time
1	R/W1C	0x0	CLR_FRAME_CNT_INT_PD Set a INT When Clear FS Frame cnt.
0	R/W1C	0x0	FS_PUL_INT_PD Set an INT when a Fsync signal received

6.2.8.17 0x01F4 CSIC DMA Feature List Register (Default Value:0x0000_0002)

Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x1	DMA0_EMBEDDED_LBC LBC Feature Existence 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC FBC Feature Existence 0: No Embedded DMA 1: Embedded FBC

6.2.8.18 0x0200 CSIC DMA Channel0 Enable Register (Default Value:0x0000_0000)

Offset:0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when VSYNC comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable

Offset:0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.2.8.19 0x0204 CSIC DMA Channel0 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence)

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.2.8.20 0x0208 CSIC DMA Channel0 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.2.8.21 0x0210 CSIC DMA Channel0 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0210			Register Name: CSIC_DMA_CH0_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.8.22 0x0214 CSIC DMA Channel0 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0214			Register Name: CSIC_DMA_CH0_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.8.23 0x0220 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: CSIC_DMA_CH0_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.2.8.24 0x0224 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0224			Register Name: CSIC_DMA_CH0_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.25 0x0228 CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0228			Register Name: CSIC_DMA_CH0_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

6.2.8.26 0x022C CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x022C			Register Name: CSIC_DMA_CH0_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.27 0x0230 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_DMA_CH0_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.2.8.28 0x0234 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_DMA_CH0_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.29 0x0238 CSIC DMA Channel0 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0238			Register Name: CSIC_DMA_CH0_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.2.8.30 0x023C CSIC DMA Channel0 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x023C			Register Name: CSIC_DMA_CH0_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.2.8.31 0x024C CSIC DMA Channel0 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.2.8.32 0x0250 CSIC DMA Channel0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO_OF_INT_EN FIFO overflow The bit is set when the FIFO become overflow.

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.8.33 0x0254 CSIC DMA Channel0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO_OF_PD FIFO overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.2.8.34 0x0258 CSIC DMA Channel0 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0258			Register Name: CSIC_DMA_CH0_LINE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.2.8.35 0x0268 CSIC DMA Channel0 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0268			Register Name: CSIC_DMA_CH0_LINE_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.2.8.36 0x0270 CSIC DMA Channel0 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.2.8.37 0x0300 CSIC LBC Channel0 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0300			Register Name: CSIC_LBC_CH0_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.2.8.38 0x0304 CSIC LBC Channel0 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0304			Register Name: CSIC_LBC_CH0_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.2.8.39 0x0308 CSIC LBC Channel0 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0308			Register Name: CSIC_LBC_CH0_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.2.8.40 0x030C CSIC LBC Channel0 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x030C			Register Name: CSIC_LBC_CH0_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

6.2.8.41 0x0310 CSIC LBC Channel0 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0310			Register Name: CSIC_LBC_CH0_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

6.2.8.42 0x0400 CSIC DMA Channel1 Enable Register (Default Value:0x0000_0000)

Offset:0x0400			Register Name: CSIC_DMA_CH1_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.2.8.43 0x0404 CSIC DMA Channel1 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.2.8.44 0x0408 CSIC DMA Channel1 Frame Lost Counter Register (Default Value:0x0001_0000)

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.2.8.45 0x0410 CSIC DMA Channel1 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0410			Register Name: CSIC_DMA_CH1_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.8.46 0x0414 CSIC DMA Channel1 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0414			Register Name: CSIC_DMA_CH1_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.8.47 0x0420 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0420			Register Name: CSIC_DMA_CH1_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.2.8.48 0x0424 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0424			Register Name: CSIC_DMA_CH1_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.49 0x0428 CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0428			Register Name: CSIC_DMA_CH1_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

6.2.8.50 0x042C CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x042C			Register Name: CSIC_DMA_CH1_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.51 0x0430 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0430			Register Name: CSIC_DMA_CH1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.2.8.52 0x0434 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0434			Register Name: CSIC_DMA_CH1_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.53 0x0438 CSIC DMA Channel1 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0438			Register Name: CSIC_DMA_CH1_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.2.8.54 0x043C CSIC DMA Channel1 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x043C			Register Name: CSIC_DMA_CH1_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.2.8.55 0x044C CSIC DMA Channel1 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.2.8.56 0x0450 CSIC DMA Channel1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrriten to buffer. For video capture, the bit is set when the last frame has been wrriten to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.8.57 0x0454 CSIC DMA Channel1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.2.8.58 0x0458 CSIC DMA Channel1 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0458			Register Name: CSIC_DMA_CH1_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.2.8.59 0x0468 CSIC DMA Channel1 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0468			Register Name: CSIC_DMA_CH1_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x0468			Register Name: CSIC_DMA_CH1_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.2.8.60 0x0470 CSIC DMA Channel1 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0470			Register Name: CSIC_DMA_CH1_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.2.8.61 0x0500 CSIC LBC Channel1 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0500			Register Name: CSIC_LBC_CH1_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.2.8.62 0x0504 CSIC LBC Channel1 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0504			Register Name: CSIC_LBC_CH1_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.2.8.63 0x0508 CSIC LBC Channel1 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0508			Register Name: CSIC_LBC_CH1_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.2.8.64 0x050C CSIC LBC Channel1 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x050C			Register Name: CSIC_LBC_CH1_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

6.2.8.65 0x0510 CSIC LBC Channel1 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0510			Register Name: CSIC_LBC_CH1_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

6.2.8.66 0x0600 CSIC DMA Channel2 Enable Register (Default Value:0x0000_0000)

Offset:0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable

Offset:0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.2.8.67 0x0604 CSIC DMA Channel2 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.2.8.68 0x0608 CSIC DMA Channel2 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.2.8.69 0x0610 CSIC DMA Channel2 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0610			Register Name: CSIC_DMA_CH2_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.8.70 0x0614 CSIC DMA Channel2 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.8.71 0x0620 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0620			Register Name: CSIC_DMA_CH2_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.2.8.72 0x0624 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0624			Register Name: CSIC_DMA_CH2_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.73 0x0628 CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0628			Register Name: CSIC_DMA_CH2_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

6.2.8.74 0x062C CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x062C			Register Name: CSIC_DMA_CH2_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.75 0x0630 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0630			Register Name: CSIC_DMA_CH2_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.2.8.76 0x0634 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0634			Register Name: CSIC_DMA_CH2_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.77 0x0638 CSIC DMA Channel2 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0638			Register Name: CSIC_DMA_CH2_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.2.8.78 0x063C CSIC DMA Channel2 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x063C			Register Name: CSIC_DMA_CH2_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.2.8.79 0x064C CSIC DMA Channel2 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x064C			Register Name: CSIC_DMA_CH2_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.2.8.80 0x0650 CSIC DMA Channel2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.8.81 0x0654 CSIC DMA Channel2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.2.8.82 0x0658 CSIC DMA Channel2 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0658			Register Name: CSIC_DMA_CH2_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.2.8.83 0x0668 CSIC DMA Channel2 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0668			Register Name: CSIC_DMA_CH2_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x0668			Register Name: CSIC_DMA_CH2_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.2.8.84 0x0670 CSIC DMA Channel2 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0670			Register Name: CSIC_DMA_CH2_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.2.8.85 0x0700 CSIC LBC Channel2 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0700			Register Name: CSIC_LBC_CH2_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.2.8.86 0x0704 CSIC LBC Channel2 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0704			Register Name: CSIC_LBC_CH2_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.2.8.87 0x0708 CSIC LBC Channel2 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0708			Register Name: CSIC_LBC_CH2_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.2.8.88 0x070C CSIC LBC Channel2 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x070C			Register Name: CSIC_LBC_CH2_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

6.2.8.89 0x0710 CSIC LBC Channel2 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0710			Register Name: CSIC_LBC_CH2_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

6.2.8.90 0x0800 CSIC DMA Channel3 Enable Register (Default Value:0x0000_0000)

Offset:0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable

Offset:0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

6.2.8.91 0x0804 CSIC DMA Channel3 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word

19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 5 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

6.2.8.92 0x0808 CSIC DMA Channel3 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

6.2.8.93 0x0810 CSIC DMA Channel3 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0810			Register Name: CSIC_DMA_CH3_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

6.2.8.94 0x0814 CSIC DMA Channel3 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0814			Register Name: CSIC_DMA_CH3_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.2.8.95 0x0820 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0820			Register Name: CSIC_DMA_CH3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

6.2.8.96 0x0824 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0824			Register Name: CSIC_DMA_CH3_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.97 0x0828 CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0828			Register Name: CSIC_DMA_CH3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address in DMA mode.

6.2.8.98 0x082C CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x082C			Register Name: CSIC_DMA_CH3_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.99 0x0830 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0830			Register Name: CSIC_DMA_CH3_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

6.2.8.100 0x0834 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0834			Register Name: CSIC_DMA_CH3_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

6.2.8.101 0x0838 CSIC DMA Channel3 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0838			Register Name: CSIC_DMA_CH3_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

6.2.8.102 0x083C CSIC DMA Channel3 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x083C			Register Name: CSIC_DMA_CH3_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

6.2.8.103 0x084C CSIC DMA Channel3 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

6.2.8.104 0x0850 CSIC DMA Channel3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.2.8.105 0x0854 CSIC DMA Channel3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.2.8.106 0x0858 CSIC DMA Channel3 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0858			Register Name: CSIC_DMA_CH3_LINE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

6.2.8.107 0x0868 CSIC DMA Channel3 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0868			Register Name: CSIC_DMA_CH3_FIFO_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

Offset: 0x0868			Register Name: CSIC_DMA_CH3_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

6.2.8.108 0x0870 CSIC DMA Channel3 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0870			Register Name: CSIC_DMA_CH3_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

6.2.8.109 0x0900 CSIC LBC Channel3 Configure Register (Default Value:0x8F30_0008)

Offset: 0x0900			Register Name: CSIC_LBC_CH3_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

6.2.8.110 0x0904 CSIC LBC Channel3 Line Target Bit0 Register (Default Value:0x0000_2400)

Offset: 0x0904			Register Name: CSIC_LBC_CH3_LINE_TAR_BIT0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

6.2.8.111 0x0908 CSIC LBC Channel3 Line Target Bit1 Register (Default Value:0x0000_3600)

Offset: 0x0908			Register Name: CSIC_LBC_CH3_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

6.2.8.112 0x090C CSIC LBC Channel3 RC ADV Register (Default Value:0x1010_1010)

Offset: 0x090C			Register Name: CSIC_LBC_CH3_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control adventure 3
23:16	R/W	0x10	Rate control adventure 2
15:8	R/W	0x10	Rate control adventure 1
7:0	R/W	0x10	Rate control adventure 0

6.2.8.113 0x0910 CSIC LBC Channel3 MB MIN Register (Default Value:0x006E_0037)

Offset: 0x0910			Register Name: CSIC_LBC_CH3_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

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7 Video Output Interfaces

7.1 TCON LCD

7.1.1 Overview

The Timing Controller LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

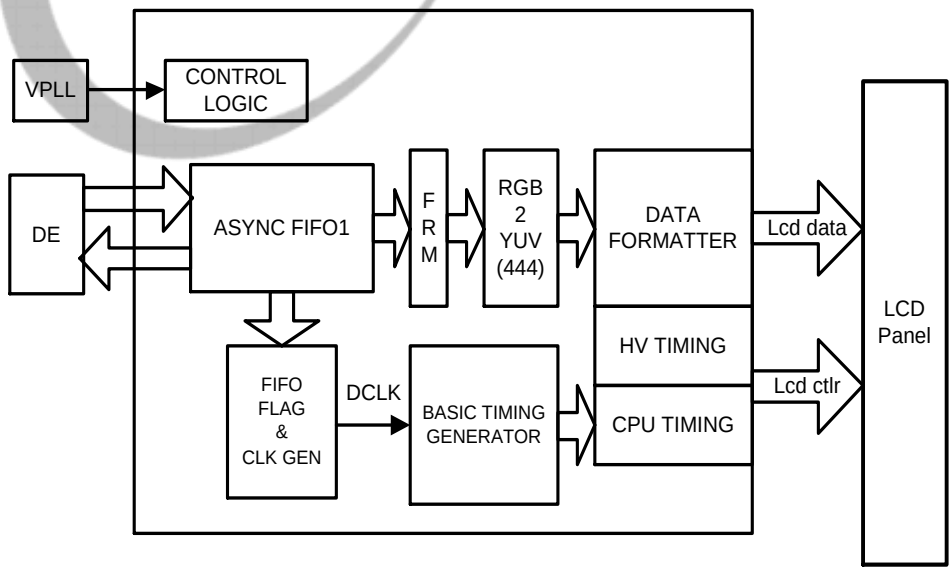
- Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
- Supports i8080 interface, up to 800 x 480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Fsync (Frame Sync.) for camera sensor

NOTE

V851SE does not support LCD

7.1.2 Block Diagram

Figure 7-1 TCON_LCD Block Diagram



7.1.3 Functional Description

7.1.3.1 External Signals

The following table describes the external I/O signals of TCONLCD

Table 7-1 LCD External Signals

Signal	Description	Type
LCD0_CLK	LCD clock, pixel data are sync by this clock	O
LCD0_VSYNC	LCD Vertical sync, indicates one new frame	O
LCD0_HSYNC	LCD Horizontal sync, indicate one new scan line	O
LCD0_DE	LCD data output enable	O
LCD0_D12	LCD data[12] output or input	O/I
LCD0_D11	LCD data[11] output or input	O/I
LCD0_D10	LCD data[10] output or input	O/I
LCD0_D7	LCD data[7] output or input	O/I
LCD0_D6	LCD data[6] output or input	O/I
LCD0_D5	LCD data[5] output or input	O/I
LCD0_D4	LCD data[4] output or input	O/I
LCD0_D3	LCD data[3] output or input	O/I

7.1.3.2 Control Signal and Data Port Mapping

External I/O	Internal pin	SYNC RGB					DC	CPU Cmd	CPU 18-bit	CPU 16bit								CPU 8bit					CPU 9bit	
		Para RGB	Serial RGB			CCIR 656	YUV422		25-6K	256K							65K	256K			65K		256K	
			1st	2nd	3rd					1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd
LCD0_VSYNC	IO0	VSYNC					VSYNC	CS																
LCD0_HSYNC	IO1	HSYNC						RD																
LCD0_CLK	IO2	DCLK					DCLK	WR																
LCD0_DE	IO3	DE					HSYNC	RS																
LCD0_D12	D12	G4	D71	D72	D73	D7	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2
LCD0_D11	D11	G3	D61	D62	D63	D6	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1
LCD0_D10	D10	G2	D51	D52	D53	D5	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0
LCD0_D7	D7	B7	D41	D42	D43	D4	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5
LCD0_D6	D6	B6	D31	D32	D33	D3	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4
LCD0_D5	D5	B5	D21	D22	D23	D2	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3
LCD0_D4	D4	B4	D11	D12	D13	D1	D1	D4	B2								B1				G4	B1	G5	B2
LCD0_D3	D3	B3	D01	D02	D03	D0	D0	D3	B1								B0				G3	B0	G4	B1

7.1.3.3 Clock Sources

Module	Module Clock	Sources	Description
TCONLCD	LCD0_CLK	CCU	Refer to section 3.4 Clock Controller Unit (CCU) for detailed information.
	DE_CLK	CCU	

7.1.3.4 Interface mode

HV interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are defined as:

Table 7-2 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync to this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO to panel	O

The timing diagram of HV interface is as follows.

Figure 7-2 HV Interface Vertical Timing

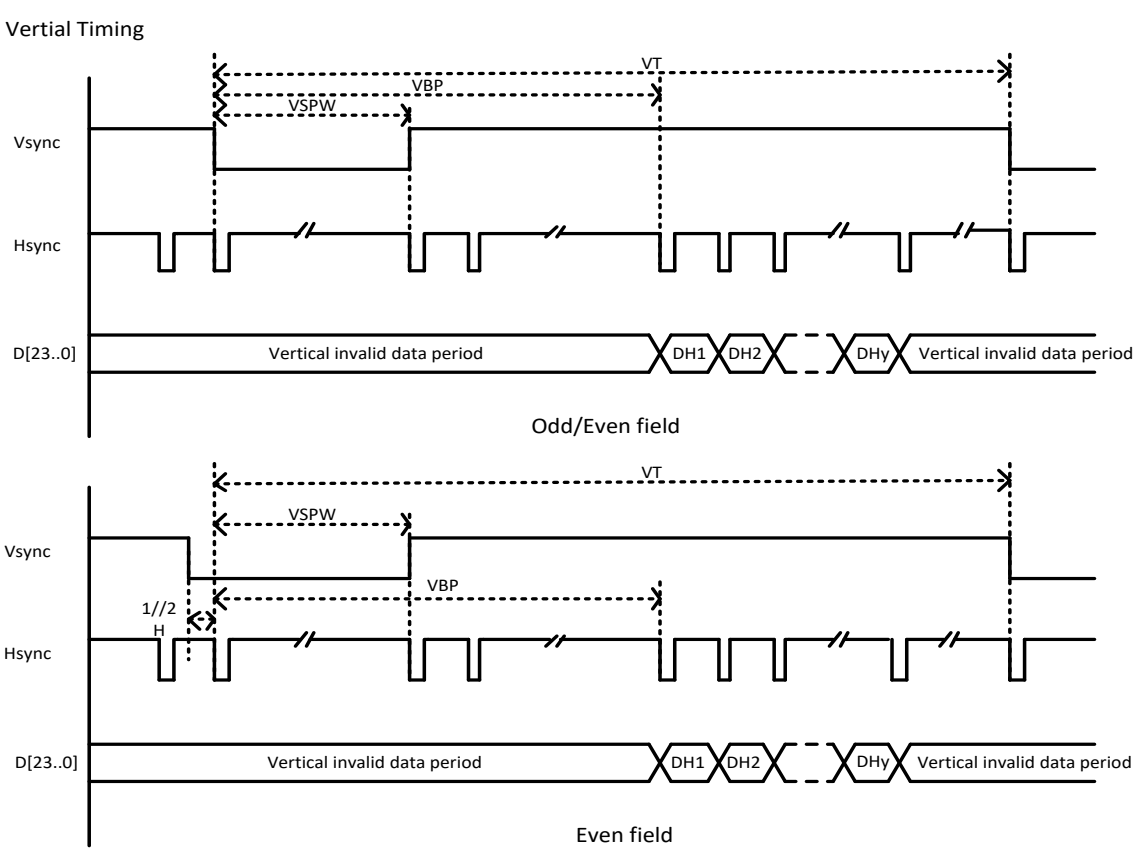
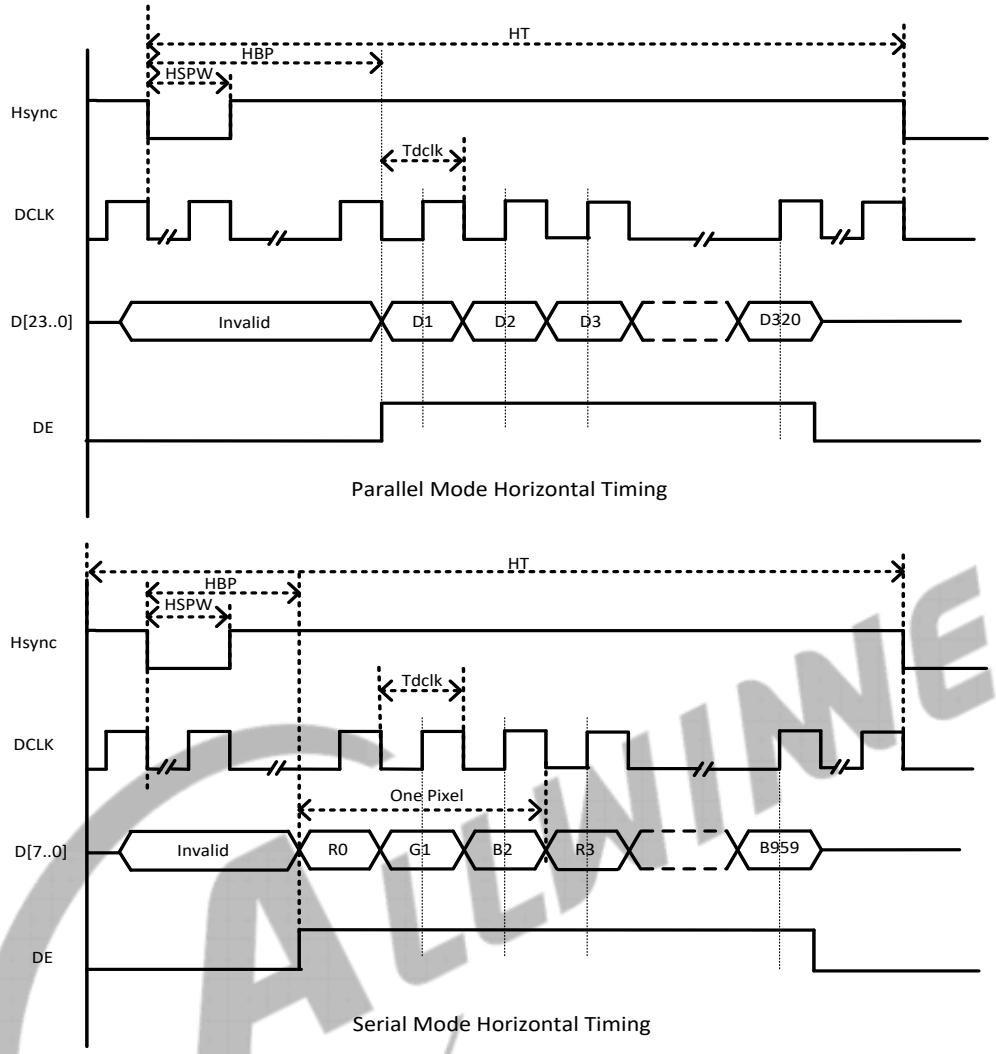


Figure 7-3 HV Interface Horizontal Timing



BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 7-3 BT656 Panel Signals

Signal Name	Description	Type
DCLK	Clock signal	O
DATA[7:0]	Data signal	O

Its logic is:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕ H

P2 = F ⊕ H

P1 = F ⊕ V

P0 = F ⊕ V ⊕ H

Where ⊕ represents the exclusive-OR function.

The 4 byte SAV/EAV sequence is as follows.

Figure 7-4 EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

i8080 Interface

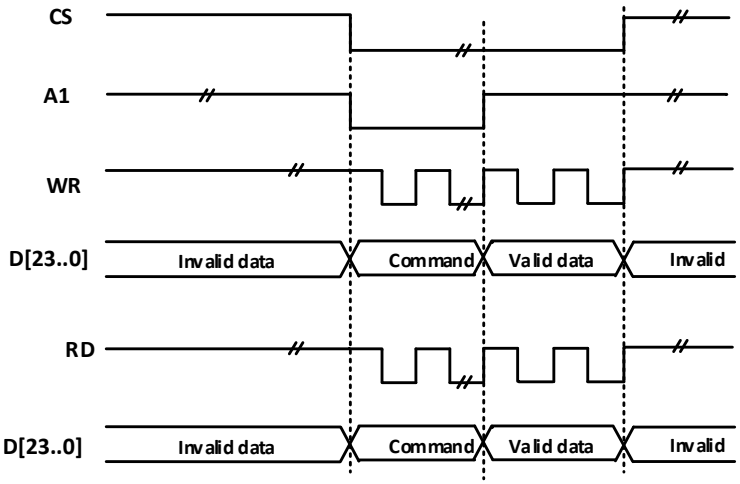
The i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. The CPU control signals are active low.

Table 7-4 CPU Panel Signals

Main Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure shows the relationship between basic timing and CPU timing. WR is 180° delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

Figure 7-5 i8080 Interface Timing



When CPU I/F is in IDLE state, it can generate WR/RD timing by setting “Lcd_CPUI/F”. The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

7.1.3.5 CEU Module

This module enhances color data from DE .

R’ = Rr*R + Rg*G + Rb*B + Rc

G’ = Gr*R + Gg*G + Gb*B + Gc

B’ = Br*R + Bg*G + Bb*B + Bc

NOTE

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb	**s13**	**(-16, 16)**
Rc, Gc, Bc	**s19**	**(-16384, 16384)**
R, G, B	**u8**	**[0-255]**

R’ has the range of [Rmin ,Rmax]

G’ has the range of [Rmin ,Rmax]

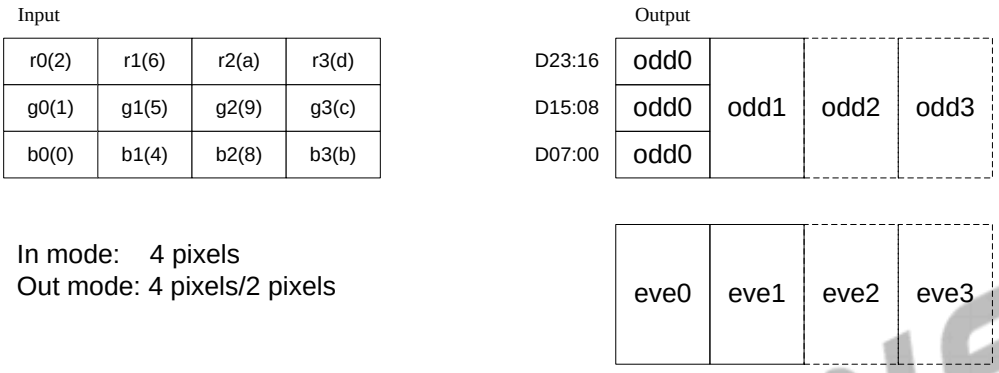
B’ has the range of [Rmin ,Rmax]

7.1.3.6 CMAP Module

Function: This module map color data from DE.

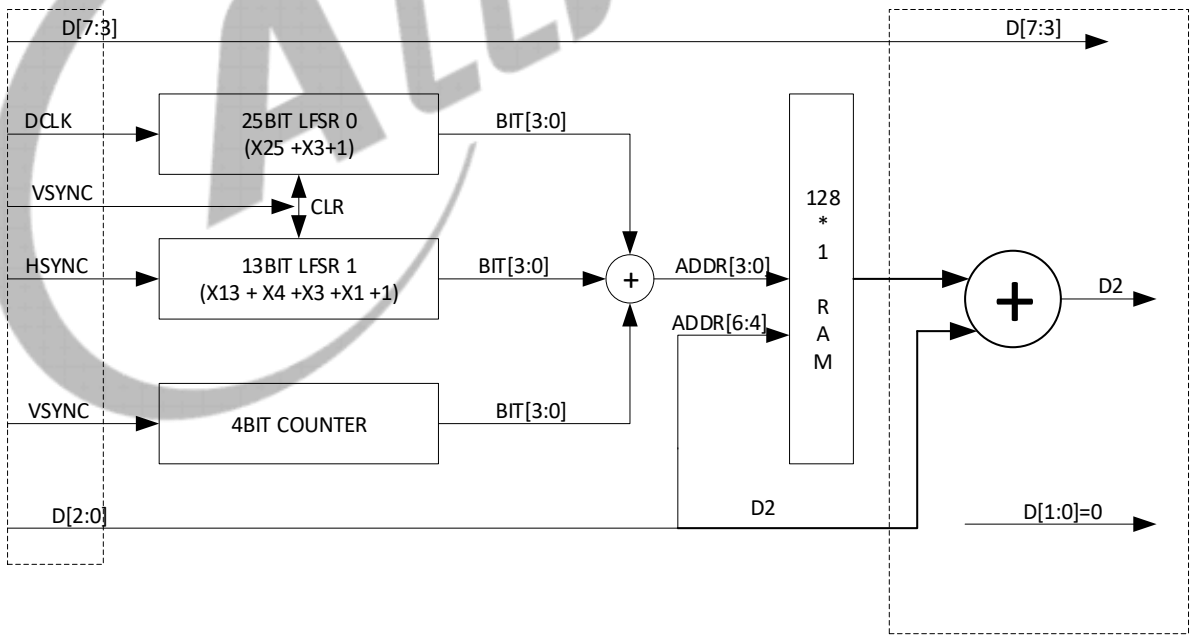
Every 4 input pixels are as a unit. A unit is divided into 12 bytes. Output byte can select one of those 12 bytes. Note that even line and odd line can be different, and output can be 12 bytes (4 pixels) or reduce to 6 bytes (2 pixels).

Figure 7-6 CMAP Module



7.1.3.7 FRM Module

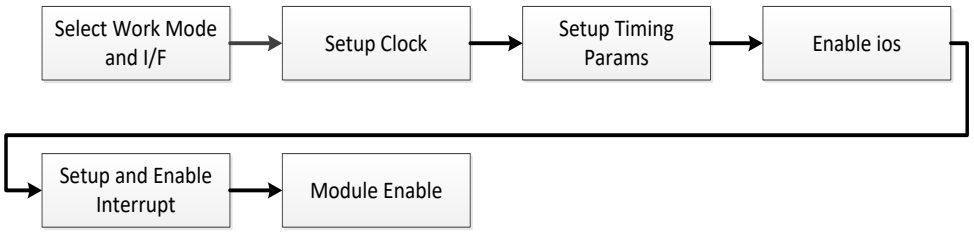
Figure 7-7 FRM Module



7.1.4 Programming Guidelines

7.1.4.1 HV Mode Configuration Process

Figure 7-8 HV Mode Initial Process



- Parallel RGB

1. Select HV interface type

   LCD_CTL_REG[LCD_IF] (reg0x40) to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE] (reg0x58) to 0 to select 24bit/1cycle parallel mode.

   lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

   lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

   lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24bit/1cycle parallel mode;

2. Clock configuration

NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0–2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

   Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

   Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

   lcd_dev[sel]->lcd_dclk.dclk_en = en;

   lcd_dev[sel]->lcd_dclk.dclk_div = div;

3. Set sequence parameters

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASE2_REG.VT needs be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic0.x = x-1;

lcd_dev[sel]->lcd_basic0.y = y-1;

lcd_dev[sel]->lcd_basic1.ht = ht-1;

lcd_dev[sel]->lcd_basic1.hbp = hbp-1;

lcd_dev[sel]->lcd_basic2.vt = vt*2;

lcd_dev[sel]->lcd_basic2.vbp = vbp-1;

lcd_dev[sel]->lcd_basic3.hspw = hspw-1;

lcd_dev[sel]->lcd_basic3.vspw = vspw-1;

4. Open IO output

   Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

   When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0~3_INV (reg0x88).

5. Set and open interrupt function

   The LCD_GINT0_REG (reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG (reg0x8) sets the interrupt line position of Line interrupt mode.

   V interrupt:

   lcd_dev[sel]->lcd_gint0.vb_en = 1;

   Line interrupt:

   lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

   lcd_dev[sel]->lcd_gint0.line_en = 1;

6. Open module enable

   Enable LCD_CTL_REG.LCD_EN (reg0x40) and LCD_GCTL_REG.LCD_EN (reg0x00).

   lcd_dev[sel]->lcd_ctl.lcd_en = 1;

   lcd_dev[sel]->lcd_gctl.lcd_en = 1;

- Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

1. Select HV interface type

Set LCD_CTL_REG.LCD_IF (reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE (reg0x58) to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;

2. Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASE2_REG.VT needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

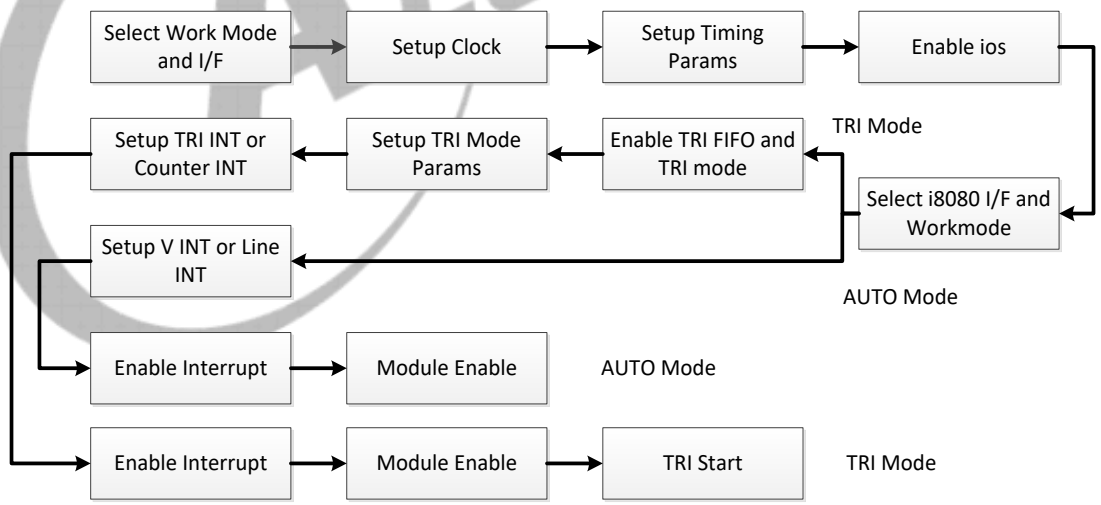
Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;

7.1.4.2 i8080 Mode Configuration Process

Figure 7-9 i8080 Mode Initial Process



1. Select i8080 interface type.
2. The step is the same as HV mode, but pulse adjustment function is invalid.
3. The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.
4. The step is the same as HV mode.

5. Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------For TRI mode----------

6. Open TRI FIFO switch, and TRI mode function.
7. Set parameters of TRI mode, including block size, block space and block number.

NOTE

When output interface is parallel mode, then the setting value of block space parameter is not less than 20.

When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.

When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.

When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

8. Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.
9. Open the total switch of interrupt.
10. Open the total enable of interrupt.
11. Operate “tri start” operation (the bit1 of LCD_CPU_IF_REG is set to "1").

----------For Auto mode----------

6. Set and open V interrupt or Line interrupt, the step is the same as HV mode.
7. Open module total enable.

7.1.5 Register List

Module Name	Base Address
TCONLCD0	0x0546 1000

Register Name	Offset	Description
LCD_GCTL_REG	0x000	LCD Global Control Register

Register Name	Offset	Description
LCD_GINT0_REG	0x004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x014+N*0x04(N=0~5)	LCD FRM Seed Register
LCD_FRM_TAB_REG	0x02C+N*0x04(N=0~3)	LCD FRM Table Register
LCD_CTL_REG	0x040	LCD Control Register
LCD_DCLK_REG	0x044	LCD Data Clock Register
LCD_BASIC0_REG	0x048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x04C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x058	LCD Hv Panel Interface Register
LCD_CPU_IF_REG	0x060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x06C	LCD CPU Panel Read Data Register1
LCD_IO_POL_REG	0x088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x08C	LCD IO Control Register
LCD_DEBUG_REG	0x0FC	LCD Debug Register
LCD_CEU_CTL_REG	0x100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x110+N*0x04(N=0~10)	LCD CEU Coefficient Register0
LCD_CEU_COEF_ADD_REG	0x11C+N*0x10(N=0~2)	LCD CEU Coefficient Register1
LCD_CEU_COEF_RANG_REG	0x140+N*0x04(N=0~2)	LCD CEU Coefficient Register2
LCD_CPU_TRI0_REG	0x160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x16C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x19C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x1F0	LCD Safe Period Register
FSYNC_GEN_CTRL_REG	0x228	LCD FSYNC Generate Control Register
FSYNC_GEN_DLY_REG	0x22C	LCD FSYNC Generate Delay Register
LCD_SYNC_CTL_REG	0x230	LCD Sync Control Register
LCD_SYNC_POS_REG	0x234	LCD Sync Position Register
LCD_SLAVE_STOP_POS_REG	0x238	LCD Slave Stop Position Register

7.1.6 Register Description

7.1.6.1 0x0000 LCD Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN When it is disabled, the module will be reset to idle state. 0: Disable 1: Enable
30:0	/	/	/

7.1.6.2 0x0004 LCD Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_VB_INT_EN Enable the Vb interrupt 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN Enable the line interrupt 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN Enable the trigger finish interrupt 0: Disable 1: Enable
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN Enable the trigger counter interrupt 0: Disable 1: Enable
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 match the current LCD scan line Write 0 to clear it.
12	/	/	/

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when CPU trigger mode finished Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when sync by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W0C	0x0	FSYNC_INT_INV Enable the fsync interrupt to set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the FSYNC signal in every frame Write 0 to clear it.

7.1.6.3 0x0008 LCD Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger (including inactive lines). Setting it for the specified line for trigger0. **Note: SY0 is writable only when LINE_TRG0 is disabled.**
15:0	/	/	/

7.1.6.4 0x0010 LCD FRM Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN Enable the dither function 0: Disable 1: Enable
30:7	/	/	/

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	LCD_FRM_MODE_R The R component output bits in dither function 0: 6-bit FRM output 1: 5-bit FRM output
5	R/W	0x0	LCD_FRM_MODE_G The G component output bits in dither function 0: 6-bit FRM output 1: 5-bit FRM output
4	R/W	0x0	LCD_FRM_MODE_B The B component output bits in dither function 0: 6-bit FRM output 1: 5-bit FRM output
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST Set the test mode of dither function 00: FRM 01: Half 5-/6-bit, half FRM 10: Half 8-bit, half FRM 11: Half 8-bit, half 5-/6-bit

7.1.6.5 0x0014+ N*0x04 (N=0–5) LCD FRM Seed Register (Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04 (N=0–5)			Register Name:
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE Set the seed used in dither function N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B **Note: Avoid setting it to 0.**

7.1.6.6 0x002C+ N*0x04 (N=0–3) LCD FRM Table Register (Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04 (N=0–3)			Register Name: LCD_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function Usually set as follows: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

7.1.6.7 0x0040 LCD Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN It executes at the beginning of the first blank line of LCD timing. 0: Disable 1: Enable
30:26	/	/	/
25:24	R/W	0x0	LCD_IF Set the interface type of LCD controller. 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved
23	R/W	0x0	LCD_RB_SWAP Enable the function to swap red data and blue data in fifo1. 0: Default 1: Swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 **Note: 1 holding time must more than 1 DCLK**
20	R/W	0x0	LCD_INTERLACE_EN This flag is valid only when LCD_EN == 1 0: Disable 1: Enable
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DLY The unit of delay is T_{line}. **Note: Valid only when LCD_EN == 1**
3	/	/	/

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x0	LCD_SRC_SEL LCD Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reversed 111: Gridding Check

7.1.6.8 0x0044 LCD Data Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others: Reversed
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk/DCLKDIV **Note:** **1.If dclk1&dclk2 are used, DCLKDIV >=6** **2.If only dclk is used, DCLKDIV >=1**

7.1.6.9 0x0048 LCD Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	WIDTH_X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_Y Panel height is Y+1

7.1.6.10 0x004C LCD Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel: HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

7.1.6.11 0x0050 LCD Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

7.1.6.12 0x0054 LCD Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT > (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

7.1.6.13 0x0058 LCD HV Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE Set the HV mode of LCD controller 0000: 24-bit/1-cycle parallel mode 1000: 8-bit/3-cycle RGB serial mode (RGB888) 1010: 8-bit/4-cycle Dummy RGB (DRGB) 1011: 8-bit/4-cycle RGB Dummy (RGBD) 1100: 8-bit/2-cycle YUV serial mode (CCIR656)
27:26	R/W	0x0	RGB888_ODD_ORDER Serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7…). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_EVEN_ORDER Serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0x0	YUV_SM Serial YUV mode Output sequence 2-pixel-pair of every scan line. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0x0	YUV_EAV_SAV_F_LINE_DLY Set the delay line mode. 00: F toggle right after active video line 01: delay 2 line (CCIR PAL) 10: delay 3 line (CCIR NTSC) 11: reserved
19	R/W	0x0	CCIR_CSC_DIS LCD convert source from RGB to YUV. 0: Enable 1: Disable Only valid when HV mode is “1100”.
18:0	/	/	/

7.1.6.14 0x0060 LCD CPU Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE Set the CPU interface work mode 0000: 18-bit/256K mode 0010: 16-bit mode0 0100: 16-bit mode1 0110: 16-bit mode2 1000: 16-bit mode3 1010: 9-bit mode 1100: 8-bit 256K mode 1110: 8-bit 65K mode xxx1: 24-bit for DSI
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG The status of write operation. 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG The status of read operation. 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto transfer mode If it is 1, all the valid data during this frame are written to panel. **Note: This bit is sampled by Vsync.**
16	R/W	0x0	FLUSH Direct transfer mode If it is enabled, FIFO1 is regardless of the HV timing, the pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRI_FIFO_BIST_EN Entry address is 0xFF8 0: Disable 1: Enable

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	TRI_FIFO_EN Enable the trigger FIFO 0: Disable 1: Enable
1	R/W1S	0x0	TRI_START Software must make sure that write '1' only when this flag is '0'. Writing '1' starts a frame flush and writing '0' has no effect. This flag indicates the frame flush is running.
0	R/W	0x0	TRI_EN Enable trigger mode 0: Trigger mode disable 1: Trigger mode enable

7.1.6.15 0x0064 LCD CPU Panel Write Data Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus.

7.1.6.16 0x0068 LCD CPU Panel Read Data Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus.

7.1.6.17 0x006C LCD CPU Panel Read Data Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus.

7.1.6.18 0x0088 LCD IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	IO_OUTPUT_SEL When it is set as '1', the d[23:0], io0, io1, io3 are sync to dclk. 0: Normal output 1: Register output
30:28	R/W	0x0	DCLK_SEL Set the phase offset of clock and data in hv mode. 000: Used DCLK0 (normal phase offset) 001: Used DCLK1 (1/3 phase offset) 010: Used DCLK2 (2/3 phase offset) 100: DCLK0/2 phase 0 101: DCLK0/2 phase 90 Others: Reserved
27	R/W	0x0	IO3_INV Enable invert function of IO3 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV Enable invert function of IO2 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV Enable invert function of IO1 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV Enable invert function of IO0 0: Not invert 1: Invert
23:0	R/W	0x0	Data_INV LCD output port D[23:0] polarity control, with independent bit control. 0: Normal polarity 1: Invert the specify output

7.1.6.19 0x008C LCD IO Control Register (Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	RGB_ENDIAN Set the endian of data bits 0: Normal 1: Bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN Enable the output of IO3 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN Enable the output of IO2 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUR_TRI_EN Enable the output of IO1 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN Enable the output of IO0 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D[23:0] output enable, with independent bit control. 1: Disable 0: Enable

7.1.6.20 0x00FC LCD Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	LCD_FIFO_UNDERFLOW The flag shows whether the fifos in underflow status 0: Not underflow 1: Underflow
30	/	/	/
29	R	0x0	LCD_FIELD_POL The flag indicates the current field polarity 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
15:0	/	/	/

7.1.6.21 0x0100 LCD CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CEU_EN Enable CEU function 0: Bypass 1: Enable
30	R/W	0x0	BT656_F_MASK BT656 F Mask 0: Disable 1: Enable
29	R/W	0x0	BT656_F_MASK_VALUE BT656 F Mask Value
28:0	/	/	/

7.1.6.22 0x0110+N*0x04 (N=0–10) LCD CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0–10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13-bit value, range of (-16,16). N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

7.1.6.23 0x011C+N*0x10 (N=0–2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10 (N=0–2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/

Offset: 0x011C+N*0x10 (N=0–2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19-bit value, range of (-16384, 16384). N=0: Rc N=1: Gc N=2: Bc

7.1.6.24 0x0140+N*0x04 (N=0–2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0–2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0, 255].
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0, 255].

7.1.6.25 0x0160 LCD CPU Panel Trigger Register0 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set >20*pixel.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

7.1.6.26 0x0164 LCD CPU Panel Trigger Register1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

7.1.6.27 0x0168 LCD CPU Panel Trigger Register2 (Default Value: 0x0020_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DLY T_{dly} = (Start_Delay +1) * be_clk*8.
15	R/W	0x0	TRANS_START_MODE Select the FIFOs used in CPU mode. 0: ECC_FIFO+TRI_FIFO 1: TRI_FIFO
14:13	R/W	0x0	SYNC_MODE Set the sync mode in CPU interface. 0x: Auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

7.1.6.28 0x016C LCD CPU Panel Trigger Register3 (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE When set as 01, the Tri_Counter_Int occurs in cycle of (Count_N+1)×(Count_M+1)×4 dclk. When set as 10 or 11, the io0 is map as TE input. 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor
7:0	R/W	0x0	COUNTER_M The value of counter factor

7.1.6.29 0x0170 LCD CPU Panel Trigger Register4 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
28	R/W	0x0	PLUG_MODE_EN Enable the plug mode used in dsi command mode. 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x0	A1_First_Valid Valid in first Block.
23:0	R/W	0x0	D23_TO_D0_First_Valid Valid in first Block.

7.1.6.30 0x0174 LCD CPU Panel Trigger Register5 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	A1_NON_First_Valid Valid in Block except first.
23:0	R/W	0x0	D23_TO_D0_NON_First_Valid Valid in Block except first.

7.1.6.31 0x0180 LCD Color Map Control Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: LCD_CMAP_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	COLOR_MAP_EN Enable the color map function. This module only works when X is divided by 4. 0: Bypass 1: Enable
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT Set the pixel output format in color map function. 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1

7.1.6.32 0x0190 LCD Color Map Odd Line Register0 (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_ODD0 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

7.1.6.33 0x0194 LCD Color Map Odd Line Register1 (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_ODD2 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

7.1.6.34 0x0198 LCD Color Map Even Line Register0 (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	OUT_EVEN0 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

7.1.6.35 0x019C LCD Color Map Even Line Register1 (Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	OUT_EVEN2 Indicates the output order of components. bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111: Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved

7.1.6.36 0x01F0 LCD Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, the LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, the LCD controller allow dram controller to change frequency. The fixed line should be set in the blanking area.
3	/	/	/

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x0	SAFE_PERIOD_MODE Select the save mode 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM **(this mode is unavailable in V851S/V851SE)** 011: safe at 2 and safe at sync active 100: safe at line

7.1.6.37 0x0228 LCD FSYNC Generate Control Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:8	R/W	0x0	SENSOR_DIS_TIME Delay 0–2047 Hsync Period When HSYNC_POL_SEL is 0, the actual delay is SENSOR_DIS_TIME-1. When HSYNC_POL_SEL is 1, the actual delay is SENSOR_DIS_TIME.
7	/	/	/
6	R/W	0x0	SENSOR_ACT1_VALUE Sensor Active1 Value 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	SENSOR_ACT0_VALUE Sensor Active0 Value 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	SENSOR_DIS_VALUE Sensor Disable Value 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	HSYNC_POL_SEL Hsync Polarity Select 0: Normal 1: Opposite hsync to hysnc counter
1	R/W	0x0	SEL_VSYNC_EN Select Vsync Enable 0: Select vsync falling edge to start state machine 1: Select vsync rising edge to start state machine

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	FSYNC_GEN_EN Fsync Generate Enable 0: Disable 1: Enable

7.1.6.38 0x022C LCD FSYNC Generate Delay Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	SENSOR_ACT0_TIME Delay 0–4095 Pixel CLK Period The actual delay is sensor_act0_time+1.
15:12	/	/	/
11:0	R/W	0x0	SENSOR_ACT1_TIME Delay 0–4095 Pixel CLK Period The actual delay is sensor_act1_time+1.

7.1.6.39 0x0230 LCD Sync Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: LCD_SYNC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	LCD_CTRL_WORK_MODE LCD Controller Work mode 0: Single DSI mode 1: Dual DSI mode
7:5	/	/	/
4	R/W	0x0	LCD_CYRL_SYNC_MASTER_SLAVE LCD Controller Sync Master Slave 0: Master 1: Slave **Note: Only use in Single DSI mode.**
3:1	/	/	/
0	R/W	0x0	LCD_CTRL_SYNC_MODE LCD Controller Sync Mode 0: Sync in the first time 1: Sync every frame **Note: Only use in Single DSI mode.**

7.1.6.40 0x0234 LCD Sync Position Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_Sync_Pixel_Num Set the pixel number of master LCD controller which is used to trigger the slave LCD controller to start working. This value is the number of pixels between the trigger point and the end of the line. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) **Note: Only use in Single DSI mode.**
15:12	/	/	/
11:0	R/W	0x0	LCD_Sync_Line_Num Set the line number of master LCD controller which is used to trigger the slave LCD controller to start working. **Note: It is only set in master LCD controller. It is not necessarily to set in slave LCD controller.** Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) **Note: Only use in Single DSI mode.**

7.1.6.41 0x0238 LCD Slave Stop Position Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: LCD_SLAVE_STOP_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	STOP_VAL Set the stop position of the slave LCD. This value is the number of pixels between the stop position and the end of the HFP. Stop_pos = HFP - Stop_val. 0<Stop_pos<HFP-2 **Note: Only use in Single DSI mode.**

7.2 MIPI DSI

The Display Serial Interface is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.02 and a D-PHY module which is compliance with MIPI DPHY specification V1.2.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI v1.02
- Up to 2 lanes
- Supports 1280 x 720@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous lane clock mode and non-continuous lane clock mode
- Compliance with MIPI DCS v1.01, bidirectional communication in LP through data lane 0
- Supports bidirectional communication of all generic commands in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and Escape modes
- Hardware checksum capabilities

NOTE

V851SE does not support MIPI DSI

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8 Audio

8.1 I2S/PCM

8.1.1 Overview

The I2S/PCM Controller is designed to transfer the streaming audio-data between the system memory and the codec chip. The controller supports the standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format, and TDM mode format.

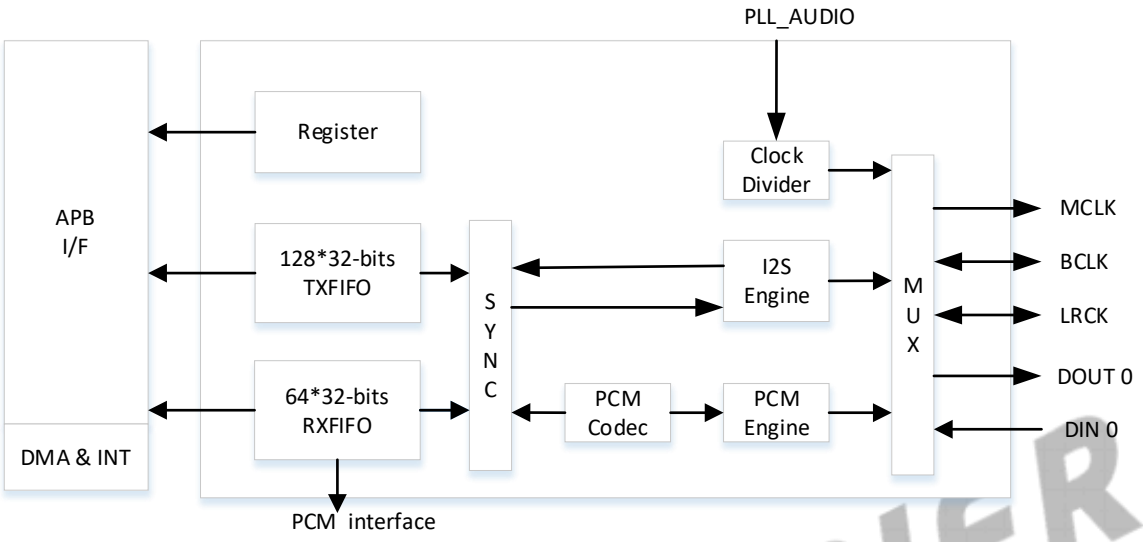
The I2S/PCM controller includes the following features:

- One I2S/PCM external interfaces (I2S1) for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO
- Supports multiple function clock
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA Slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8 kHz to 384 kHz (CHAN = 2)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

8.1.2 Block Diagram

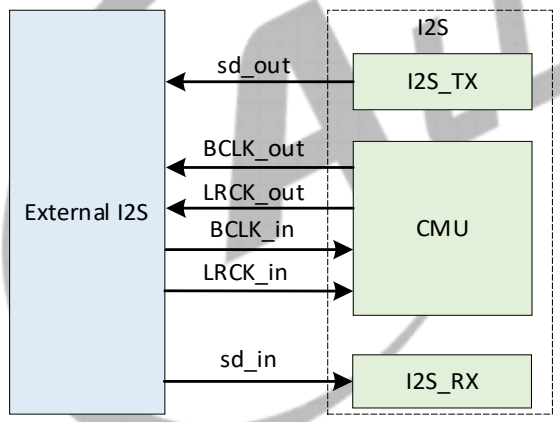
The following figure shows the functional block diagram of the I2S/PCM interface.

Figure 8-1 I2S/PCM Interface System Block Diagram



The following figure shows the typical application of the I2S/PCM interface.

Figure 8-2 Typical Application of I2S/PCM Interface



The I2S/PCM interface system integrates one I2S_TX and one I2S_RX.

- The I2S_TX is for playing music in I2S or PCM format.
- The I2S_RX is for receiving data in I2S or PCM format.
- When the I2S works in the slave mode, the external I2S module provides BCLK_in and LRCK_in for the clock management unit (CMU), and the I2S_TX and I2S_RX work with the two external clocks.
- When the I2S works in the master mode, the CMU provides clocks BCLK_out and LRCK_out for the external I2S module, and the I2S_TX and I2S_RX work with the internal clocks.

8.1.3 Functional Descriptions

8.1.3.1 External Signals

The following table describes the external signals of the I2S/PCM interface.

LRCK and BCLK are bidirectional I/O. When the I2S/PCM interface works in the Master mode, LRCK and BCLK are output pins. When the I2S/PCM interface works in the Slave mode, LRCK and BCLK are input pins.

MCLK is an output pin for external devices. DOUT is a serial data output pin and DIN is an serial data input pin. For details about General Purpose I/O port, refer to section 10.6 GPIO.

Table 8-1 I2S/PCM External Signals

Signal	Description	Type
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Sample Rate Clock	I/O
I2S1-DOUT 0	I2S1/PCM1 Serial Data Output Channel 0	O
I2S1-DIN 0	I2S1/PCM11Serial Data Input Channel 0	I

8.1.3.2 Clock Sources

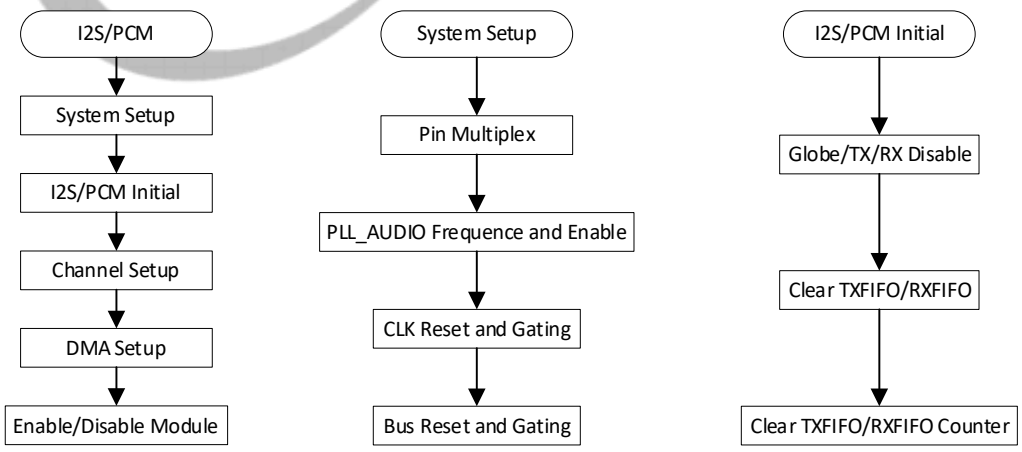
The following table describes the clock sources for I2S/PCM. For clock setting, configurations, and gating information, refer to section 3.4 Clock Controller Unit (CCU)

8.1.4 Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup, and Enable/Disable module.

The following figure shows the whole operation flow of I2S/PCM.

Figure 8-3 I2S/PCM Operation Flow



8.1.4.1 System Setup and I2S/PCM Initialization

The first step in the system setup is properly programming the GPIO. Because the I2S/PCM port is a multiplex pin. You can find the function in the pin multiplex specification.

The clock source for the I2S/PCM should be followed.

1. Disable the PLL_AUDIO though the PLL_ENABLE bit of PLL_AUDIO_CTRL_REG (Offset: 0x0078) in the CCU.
2. Set up the frequency of the PLL_AUDIO in the PLL_AUDIO_CTRL_REG (Offset: 0x0078).
3. Enable PLL_AUDIO.
4. Enable the I2S/PCM gating though the I2SPCMx_CLK_REG (Offset: 0x0A10) when you checkout that the LOCK bit of PLL_AUDIO_CTRL_REG (Offset: 0x0078) becomes to 1.
5. Reset and enable the I2S/PCM bus gating in the I2SPCM_BGR_REG (Offset: 0x0A20).

After the system setup, set up the register of I2S/PCM.

1. Initialize the I2S/PCM. Close the globe enable bit (I2S/PCM_CTL (Offset: 0x0000) [0]), TX enable bit (I2S/PCM_CTL (Offset: 0x0000) [2]), and RX enable bit (I2S/PCM_CTL (Offset: 0x0000) [1]) by writing 0 to it.
2. Clear the TX/RX FIFO by writing 0 to the bit[25:24] of I2S/PCM_FCTL (Offset: 0x0014).
3. Clear the TX/RX FIFO counter by writing 0 to I2S/PCM_TXCNT (Offset: 0x0028) and I2S/PCM_RXCNT (Offset: 0x002C).

8.1.4.2 Channel Setup and DMA Setup

1. Set up the I2S/PCM of mater and slave. The configuration can be referred to the protocol of I2S/PCM.
2. Set up the translation mode, the sample resolution, the wide of slot, the channel slot number, the trigger level, etc. The setup of register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the 3.8 Direct Memory Access Controller (DMAC). In this module, just enable the DRQ.

8.1.4.3 Enabling and Disabling the I2S/PCM

Refer to the following steps to enable this function.

1. Enable TX/RX by writing the I2S/PCM_CTL (Offset: 0x0000) [2:1].
2. Enable I2S/PCM by writing 1 to the Globe Enable bit in the I2S/PCM_CTL (Offset: 0x0000).

If you want to disable this function, write 0 to the Globe Enable bit to disable I2S/PCM.

8.1.5 Register List

Module Name	Base Address	Comments
I2S|PCM1	0x02033000	Use for Bluetooth.

Register Name	Offset	Description
I2S|PCM_CTL	0x0000	I2S|PCM Control Register
I2S|PCM_FMT1	0x0008	I2S|PCM Format Register 1
I2S|PCM_ISTA	0x000C	I2S|PCM Interrupt Status Register
I2S|PCM_RXFIFO	0x0010	I2S|PCM RXFIFO Register
I2S|PCM_FCTL	0x0014	I2S|PCM FIFO Control Register
I2S|PCM_FSTA	0x0018	I2S|PCM FIFO Status Register
I2S|PCM_INT	0x001C	I2S|PCM DMA And Interrupt Control Register
I2S|PCM_TXFIFO	0x0020	I2S|PCM TXFIFO Register
I2S|PCM_CLKD	0x0024	I2S|PCM Clock Divide Register
I2S|PCM_TXCNT	0x0028	I2S|PCM TX Sample Counter Register
I2S|PCM_RXCNT	0x002C	I2S|PCM RX Sample Counter Register
I2S|PCM_CHCFG	0x0030	I2S|PCM Channel Configuration Register
I2S|PCM_TX0CHSEL	0x0034	I2S|PCM TX0 Channel Select Register
I2S|PCM_TX0CHMAP0	0x0044	I2S|PCM TX0 Channel Mapping Register0
I2S|PCM_TX0CHMAP1	0x0048	I2S|PCM TX0 Channel Mapping Register1
I2S|PCM_TX3CHMAP0	0x005C	I2S|PCM TX3 Channel Mapping Register0
I2S|PCM_TX3CHMAP1	0x0060	I2S|PCM TX3 Channel Mapping Register1
I2S|PCM_RXCHSEL	0x0064	I2S|PCM RX Channel Select Register
I2S|PCM_RXCHMAP0	0x0068	I2S|PCM RX Channel Mapping Register0
I2S|PCM_RXCHMAP1	0x006C	I2S|PCM RX Channel Mapping Register1
I2S|PCM_RXCHMAP2	0x0070	I2S|PCM RX Channel Mapping Register2
I2S|PCM_RXCHMAP3	0x0074	I2S|PCM RX Channel Mapping Register3

8.1.6 Register Description

8.1.6.1 0x0000 I2S/PCM Control Register (Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START The bit takes effect only when RX_SYNC_EN is set to 1. I2S1/DMIC Synchronize Enable Start. 0: Disabled 1: Enabled

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
20	R/W	0x0	RX_SYNC_EN I2S RX Synchronize Enable 0: Disabled 1: Enabled
19	/	/	/
18	R/W	0x1	BCLK_OUT Bit Clock Direction Select 0: Input 1: Output
17	R/W	0x1	LRCK_OUT LRCK Direction Select 0: Input 1: Output
16:9	/	/	/
8	R/W	0x0	DOUT0_EN Data0 Output Enable 0: Disabled, Hi-Z State 1: Enabled
7	/	/	/
6	R/W	0x0	OUT_Mute Data Output Mute Enable 0: Normal Transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode (offset 0: Long Frame; offset 1: Short Frame) 01: Left Mode (offset 0: LJ Mode; offset 1: I2S Mode) 10: Right-Justified Mode 11: Reserved
3	R/W	0x0	LOOP Loopback Test 0: Normal Mode 1: Loopback Test When set to '1', the bit indicates that the DOUT is connected to the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disabled 1: Enabled

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	RXEN Receiver Block Enable 0: Disabled 1: Enabled
0	R/W	0x0	GEN Globe Enable 0: Disabled 1: Enabled

8.1.6.2 0x0008 I2S/PCM Format Register 1 (Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

8.1.6.3 0x000C I2S/PCM Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: TXFIFO underrun pending interrupt Write '1' to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No pending interrupt 1: TXFIFO overrun pending interrupt Write '1' to clear this interrupt.
4	R	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No pending IRQ 1: TXFIFO empty pending interrupt when data in TXFIFO are less than TX trigger level
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: RXFIFO underrun pending interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Write '1' to clear this interrupt.
0	R/W	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ when data in RXFIFO are more than RX trigger level

8.1.6.4 0x0010 I2S/PCM RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample The host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

8.1.6.5 0x0014 I2S/PCM FIFO Control Register (Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable The bit takes effect only when TXEN is set to 1. I2S1 Hub Enable. 0: Disabled 1: Enabled
30:26	/	/	/
25	R/WAC	0x0	FTX Write ‘1’ to flush TXFIFO, self clear to ‘0’.
24	R/WAC	0x0	FRX Write ‘1’ to flush RXFIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12’h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12’h0}

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO register 01: Expanding received sample sign bit at MSB of RXFIFO register 10: Truncating received samples at high half-word of RXFIFO register and low half-word of RXFIFO register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO register and high half-word of RXFIFO register is expanded by its sign bit Example for 20-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12'h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

8.1.6.6 0x0018 I2S/PCM FIFO Status Register (Default Value: 0x1080_0080)

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
7	R	0x1	PLACE_HOLDER NO Meaning.
6:0	R	0x0	RXA_CNT RXFIFO available sample word counter

8.1.6.7 0x001C I2S/PCM DMA & Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disabled 1: Enabled
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disabled 1: Enabled
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disabled 1: Enabled When set to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disabled 1: Enabled
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disabled 1: Enabled When set to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disabled 1: Enabled
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disabled 1: Enabled
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disabled 1: Enabled

8.1.6.8 0x0020 I2S/PCM TXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written to this register one by one. The left channel sample data is first and then the right channel sample.

8.1.6.9 0x0024 I2S/PCM Clock Divide Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **Note: Whether in slave or master mode, when this bit is set to '1', MCLK should be output.**
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

8.1.6.10 0x0028 I2S/PCM TX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After being updated by the initial value, the counter register should count on the base of this initial value.

8.1.6.11 0x002C I2S/PCM RX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After being updated by the initial value, the counter register should count on the base of this initial value.

8.1.6.12 0x0030 I2S/PCM Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half-cycle of BCLK in the slot 1: Turn to Hi-Z state for the last half-cycle of BCLK in the slot
8	R/W	0x0	TX_STATE 0: Transfer level 0 in non-transferring slot 1: Turn to Hi-Z State (TDM) in non-transferring slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot number between CPU/DMA and RXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111: 16 channels or slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot number between CPU/DMA and TXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots

8.1.6.13 0x0034 I2S/PCM TX0 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TX0CHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX0_OFFSET TX0 Offset Tune (TX0 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX0_CHSEL TX0 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111: 16 channels or slots
15:0	R/W	0x0	TX0_CHEN TX0 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more slots are disabled, the affected slots are set to the disable state. 0: Disabled 1: Enabled

8.1.6.14 0x0044 I2S/PCM TX0 Channel Mapping0 Register 0 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX0_CH15_MAP TX0 Channel 15 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
27:24	R/W	0x0	TX0_CH14_MAP TX0 Channel 14 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0x0	TX0_CH13_MAP TX0 Channel 13 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
19:16	R/W	0x0	TX0_CH12_MAP TX0 Channel 12 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
15:12	R/W	0x0	TX0_CH11_MAP TX0 Channel 11 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
11:8	R/W	0x0	TX0_CH10_MAP TX0 Channel 10 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
7:4	R/W	0x0	TX0_CH9_MAP TX0 Channel 9 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	TX0_CH8_MAP TX0 Channel 8 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample

8.1.6.15 0x0048 I2S/PCM TX0 Channel Mapping1 Register 1 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH7_MAP TX0 Channel 7 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
27:24	R/W	0x0	TX0_CH6_MAP TX0 Channel 6 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
23:20	R/W	0x0	TX0_CH5_MAP TX0 Channel 5 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0x0	TX0_CH4_MAP TX0 Channel 4 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
15:12	R/W	0x0	TX0_CH3_MAP TX0 Channel 3 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
11:8	R/W	0x0	TX0_CH2_MAP TX0 Channel 2 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
7:4	R/W	0x0	TX0_CH1_MAP TX0 Channel 1 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
3:0	R/W	0x0	TX0_CH0_MAP TX0 Channel 0 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample

8.1.6.16 0x0064 I2S/PCM RX Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S/PCM_RXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX Offset Tune (RX Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111: 16 channels or slots
15:0	/	/	/

8.1.6.17 0x0068 I2S/PCM RX Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	RX_CH15_SELECT RX Channel 15 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
27:24	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
23:22	/	/	/

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
21:20	R/W	0x0	RX_CH14_SELECT RX Channel 14 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
19:16	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH13_SELECT RX Channel 13 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
11:8	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH12_SELECT RX Channel 12 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample

8.1.6.18 0x006C I2S/PCM RX Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH11_SELECT RX Channel 11 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
27:24	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH10_SELECT RX Channel 10 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH9_SELECT RX Channel 9 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
11:8	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH8_SELECT RX Channel 8 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample

8.1.6.19 0x0070 I2S/PCM RX Channel Mapping Register2 (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: I2S/PCM_RXCHMAP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	RX_CH7_SELECT RX Channel 7 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
27:24	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH6_SELECT RX Channel 6 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
19:16	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH5_SELECT RX Channel 5 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved

Offset: 0x0070			Register Name: I2S/PCM_RXCHMAP2
Bit	Read/Write	Default/Hex	Description
11: 8	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH4_SELECT RX Channel 4 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
3:0	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample … 1111: The sixteenth sample

8.1.6.20 0x0074 I2S/PCM RX Channel Mapping Register3 (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH3_SELECT RX Channel 3 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH2_SELECT RX Channel 2 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
19:16	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH1_SELECT RX Channel 1 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
11:8	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0000: The first sample ... 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample
7:6	/	/	/

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	**Read/Write**	**Default/Hex**	**Description**
5:4	R/W	0x0	RX_CH0_SELECT RX Channel 0 Select 00: SDI0 01: Reserved 10: Reserved 11: Reserved
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0000: The first sample … 0111: The eighth sample 1000: The ninth sample ... 1111: The sixteenth sample

8.2 DMIC

8.2.1 Overview

The DMIC controller supports one 8-channel digital microphone interface and can output 128 fs or 64 fs (fs = ADC sample rate).

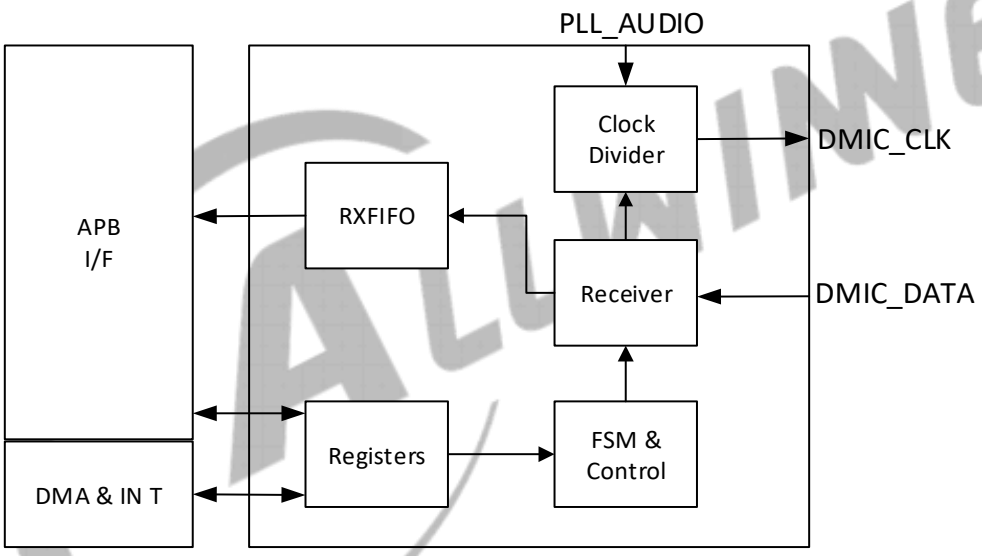
The DMIC controller includes the following features:

- Supports up to 2 channels
- Sample rate from 8 kHz to 48 kHz

8.2.2 Block Diagram

The following figure shows a block diagram of the DMIC.

Figure 8-4 DMIC Block Diagram



8.2.3 Functional Description

8.2.3.1 External Signals

The following table describes the external signals of DMIC.

Table 8-2 DMIC External Signals

Signal	Description	Type
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA0	Digital Microphone Data Input	I

8.2.3.2 Clock Sources

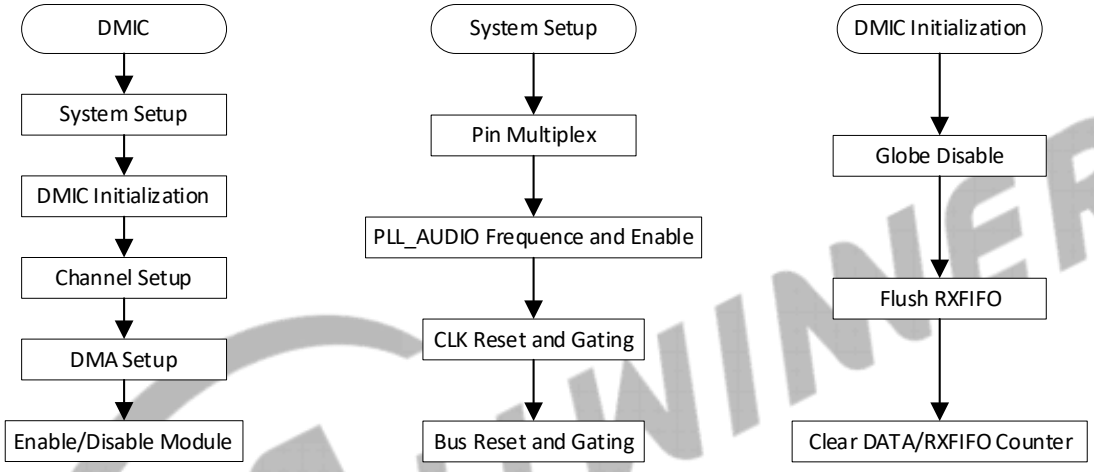
The following table describes the clock source for DMIC. For clock setting, configurations, and gating information, refer to section 3.4 Clock Controller Unit (CCU)

8.2.4 Operation Modes

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, channel setup, DMA setup, and Enable/Disable module.

The following figure shows the flow chart of the whole operation, the system setup, and the DMIC initialization.

Figure 8-5 DMIC Operation Mode



8.2.4.1 System Setup and DMIC Initialization

The first step in the DMIC initialization is properly programming the GPIO. Because the DMIC port is a multiplex pin. You can find the function in the pin multiplex specification.

The clock source for the DMIC should be followed.

1. disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE].
2. set up the frequency of the PLL_AUDIO in PLL_AUDIOx Control Register.
3. Enable PLL_AUDIO
4. Enable the DMIC gating through DMIC_CLK_REG when you checkout that the LOCK bit of PLL_AUDIOx Control Register becomes 1.
5. reset and enable the DMIC bus gating by DMIC_BGR_REG.

After the system setup, set up the register of DMIC.

1. Initialize the DMIC. Close the globe enable bit (DMIC_EN[8]), data channel enable bit (DMIC_EN[1:0]) by writing 0 to it.
2. Flush the RXFIFO by writing 1 to DMIC_RXFIFO_CTR[31].

3. Clear the Data/RXFIFO counter by writing 1 to DMIC_RXFIFO_STA, DMIC_CNT.

8.2.4.2 Channel Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over-sample rate, the channel number, the RXFIFO output mode, the RXFIFO trigger level, and so on. The setup of the register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in section 3.9 “DMAC”. In this module, you just enable the DRQ.

8.2.4.3 Enable and Disable DMIC

Refer to the following steps to enable this function.

1. Enable the data channel enable bit (DMIC_EN[1:0]) by writing 1 to it.
2. enable DMIC by writing 1 to the Globe Enable bit (DMIC_EN[8]).

If you want to disable this function, write 0 to DMIC_EN[8] to disable DMIC.

8.2.5 Register List

Module Name	Base Address	Comments
DMIC	0x02031000	Digital microphone controller

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_DATA	0x0010	DMIC DATA Register
DMIC_INTC	0x0014	DMIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_VOL_CTR	0x0030	DATA0 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register

8.2.6 Register Description

8.2.6.1 0x0000 DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	RX_SYNC_EN_START Audio Subsys RX Synchronize Enable Start Includes Audio codec/I2S1/DMIC The bit takes effect only when RX_SYNC_EN is set to 1. 0: Disabled 1: Enabled
28	R/W	0x0	RX_SYNC_EN DMIC RX Synchronize Enable 0: Disabled 1: Enabled
27:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disabled 1: Enabled
7:2	/	/	/
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel Enable 0: Disabled 1: Enabled
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disabled 1: Enabled

8.2.6.2 0x0004 DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0004			Register Name: DMIC_SR
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

8.2.6.3 0x0008 DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5 ms 01: 10 ms 10: 20 ms 11: 30 ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disabled 1: Enabled
7:5	/	/	/
4	R/W	0x0	DATA0 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Supports 8 kHz to 24 kHz) 1: 64 (Supports 16 kHz to 48 kHz)

8.2.6.4 0x0010 DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMIC_DATA

8.2.6.5 0x0014 DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disabled 1: Enabled
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disabled 1: Enabled
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disabled 1: Enabled

8.2.6.6 0x0018 DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DMIC_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing '1' to clear this interrupt or automatically clear if the interrupt condition fails.
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing '1' to clear this interrupt or automatically clear if the interrupt condition fails.

8.2.6.7 0x001C DMIC RXFIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing '1' to flush RXFIFO, self clear to '0'
30:10	/	/	/
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {RXFIFO_O[20:0], 11'h0} Mode 1: RXDATA[31:0] = {8{RXFIFO_O[20]}, RXFIFO_O[20:0], 3'h0} For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {RXFIFO_O[20:5], 16'h0} Mode 1: RXDATA[31:0] = {16{RXFIFO_O[20]}, RXFIFO_O[20:5]}
8	R/W	0x0	Sample_Resolution 0: 16-bit 1: 24- bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV[7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV[7:0]) WLEVEL represents the number of valid samples in the DMIC RXFIFO

8.2.6.8 0x0020 DMIC RXFIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R	0x1	Reserved
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

8.2.6.9 0x0024 DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x1	DMIC_CH_NUM DMIC enable channel numbers are (N + 1).

8.2.6.10 0x0028 DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel

8.2.6.11 0x002C DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: DMIC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMIC_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is read by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After being updated by the initial value, the counter register should count on the base of this initial value. **Note: It is used for Audio/Video Synchronization.**

8.2.6.12 0x0030 DATA0 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0 _VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

Offset: 0x0030			Register Name: DATA0 _VOL_CTR
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0xA0	DATA0L_VOL Data0 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL Data0 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

8.2.6.13 0x0038 High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disabled 1: Enabled
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disabled 1: Enabled

8.2.6.14 0x003C High Pass Filter Coefficient Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFAA45	HPF_COE High Pass Filter Coefficient

8.2.6.15 0x0040 High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFD522	HPF_GAIN High Pass Filter Gain

8.3 Audio Codec

8.3.1 Overview

The Audio Codec is high-performance audio encoder and decoder module which supports DAC/ADC, dynamic range controller (DRC) and dynamic voltage controller (DVC) functions.

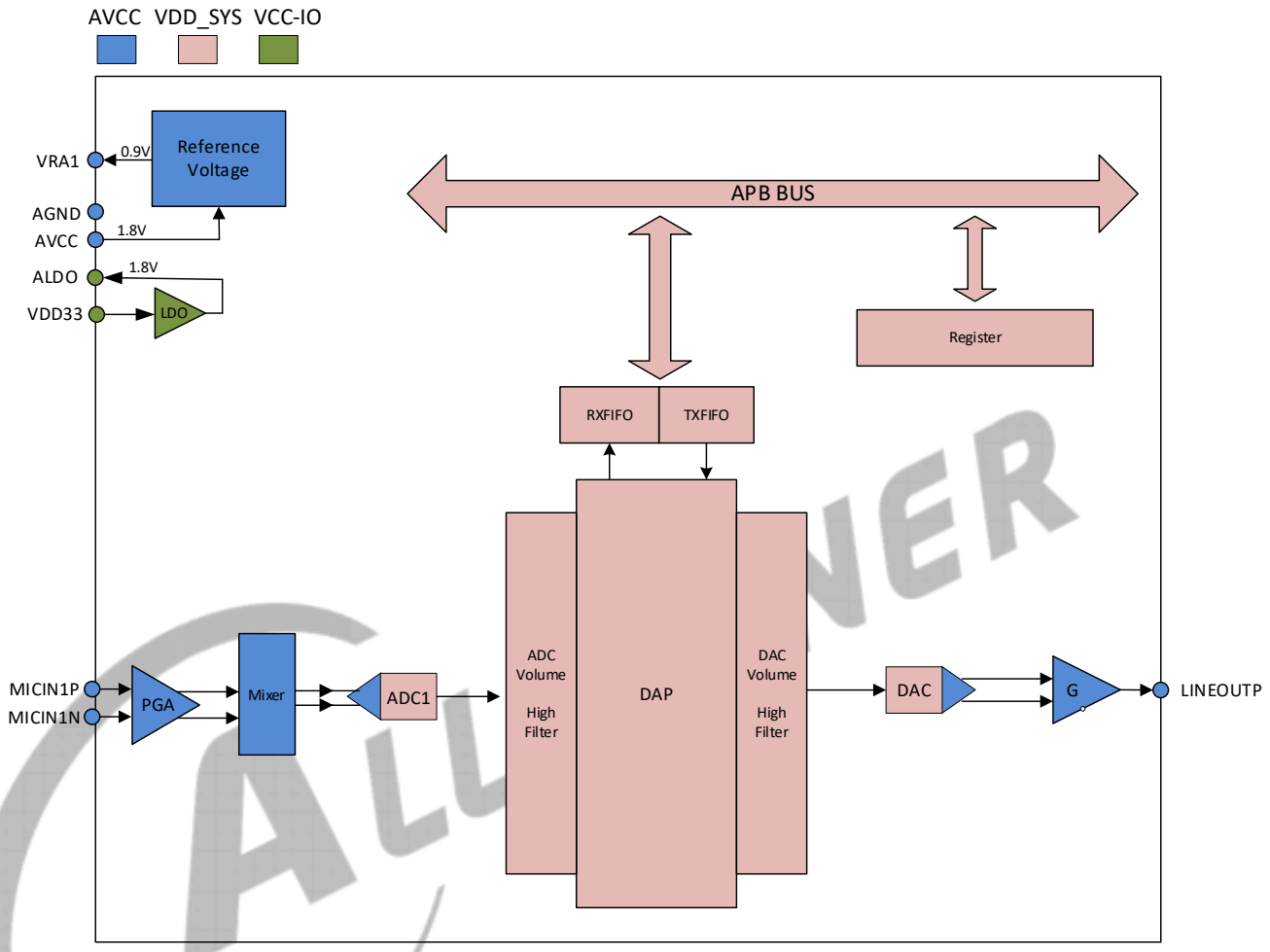
The Audio Codec has the following features:

- One audio digital-to-analog converter (DAC) channels
  - Supports the DAC sample rate from 8 kHz to 192 kHz
  - 95 ± 2 dB SNR@A-weight, -85 ± 3 dB THD + N
  - Supports 16-bit and 20-bit audio sample resolution
- One audio analog-to-digital converter (ADC) channels
  - Supports the ADC sample rate from 8 kHz to 48 kHz
  - 95 ± 3 dB SNR@A-weight, -80 ± 3 dB THD + N
  - Supports 16-bit and 20-bit audio sample resolution
- One audio input:
  - One differential microphone input: MIC1P/N
- One analog audio output:
  - One single-end lineout output (LINEOUTP)
- Supports Dynamic Range Controller (DRC) adjusting the ADC recording and DAC playback
- One 128x20-bit FIFO for DAC data transmit, one 128x20-bit FIFO for ADC data receive
- Programmable FIFO thresholds
- Supports interrupts and DMA

8.3.2 Block Diagram

The following figure shows the block diagram of Audio Codec.

Figure 8-6 Audio Codec Block Diagram



8.3.3 Functional Description

8.3.3.1 External Signals

Table 8-3 Audio Codec analog I/O

Name	Type	Description
MICIN1P	I	Positive differential input for MIC1
MICIN1N	I	Negative differential input for MIC1
LINEOUTP	O	Positive differential output for lineout

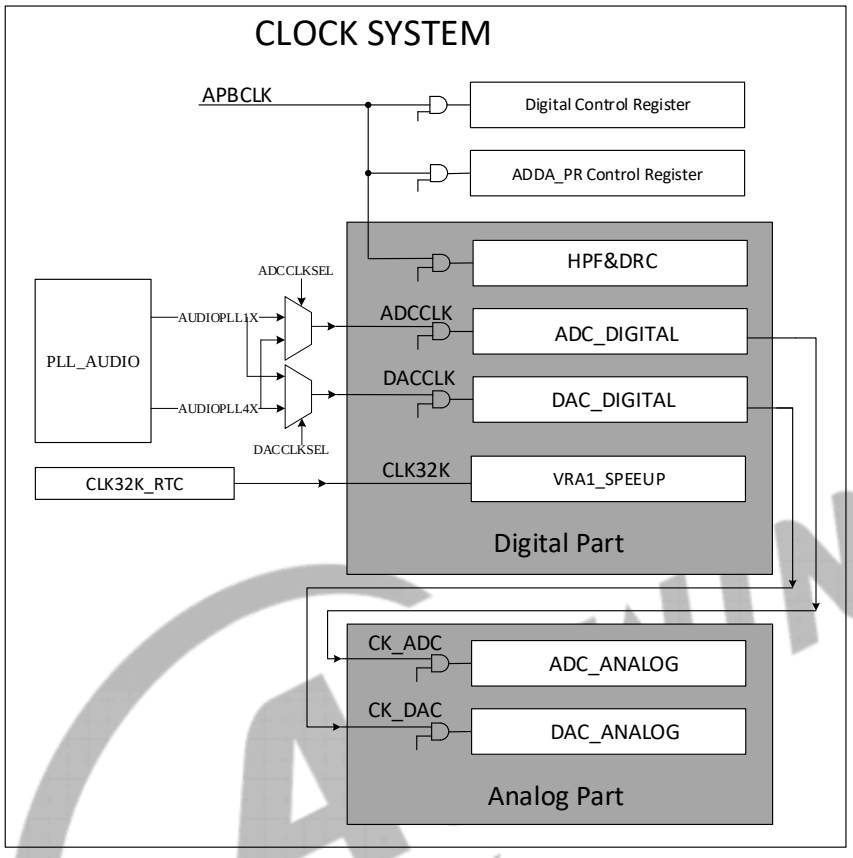
Table 8-4 Audio Codec reference I/O

Name	Type	Description
VRA1	O	Internal reference voltage

8.3.3.2 Clock Sources

The following figure describes the clock source of Audio Codec. For clock setting, configuration, and gating information, refer to section 3.4 Clock Controller Unit (CCU)

Figure 8-7 Audio Codec Clock Diagram



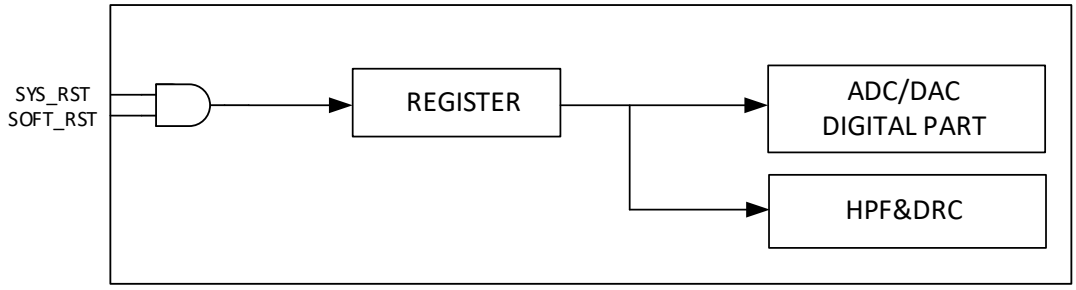
The clock source for the digital part is PLL_AUDIO. For the ADC clock, configure AUDIO_CODEC_ADC_CLK_REG[24] to select the clock source. For the DAC clock, configure AUDIO_CODEC_DAC_CLK_REG[24] to select the clock source. The PK-PK jitter of PLL_AUDIO should be less than 200 ps.

8.3.3.3 Reset System

Digital Part Reset System

The SYS_RST comes from the VDD_SYS domain and produced by the RTC domain which controlled by CCMU when it is powered on. Each domain has the de-bounce to confirm the reset system is strong. The codec register part will be reset by the SYS_RST when being powered on or the system soft is writing the reset control logic. The other parts will be reset by the soft configuration through writing the register. The following figure shows the reset system of the audio codec digital part.

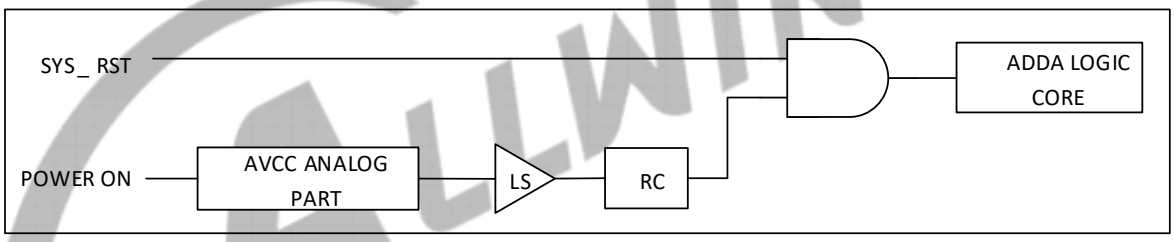
Figure 8-8 Digital Part Reset System



Analog Part Reset System

When AVCC is powered on, it sends the AVCC_POR signal. The AVCC_POR signal passes the level shift and RC filter part to the ADDA logic core. The following figure shows the reset system of the audio codec analog part.

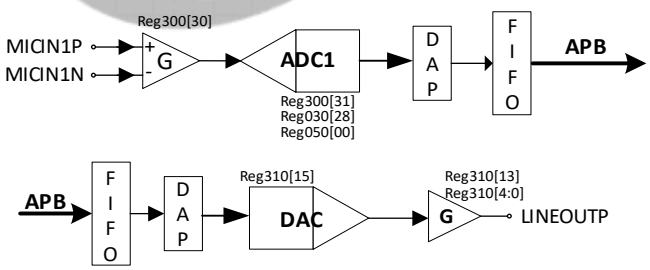
Figure 8-9 Analog Part Reset System



8.3.3.4 Data Path Diagram

The following figure shows a data path of the Audio Codec.

Figure 8-10 Audio Codec Data Path Diagram



8.3.3.5 Mono ADC

The mono ADC is used for recording sound. The sample rates of the mono ADC are independent of the DAC sample rate. The digital ADC part can be enabled or disabled by the bit[28] of the AC_ADC_FIFOC (Offset: 0x0030) .

8.3.3.6 Mono DAC

The mono DAC sample rate can be configured by setting the register. To save power, the analog DAC can be enabled or disabled by setting the bit[15] of the DAC_REG (Offset: 0x0310). The digital DAC part can be enabled or disabled by the bit[31] of the AC_DAC_DPC (Offset: 0x0000).

8.3.3.7 Analog Audio Input Path

The Audio Codec supports one analogue audio input path:

- MICIN1P/N

MICIN1P/N provide differential input that can be mixed into the ADC1 record mixer. MICIN is a high impedance, low capacitance input suitable for connection to various differential microphones of different dynamics and sensitivity. The gain for each pre-amplifier can be set independently.

8.3.3.8 Analog Audio Output Port

The Codec has One type analog output ports:

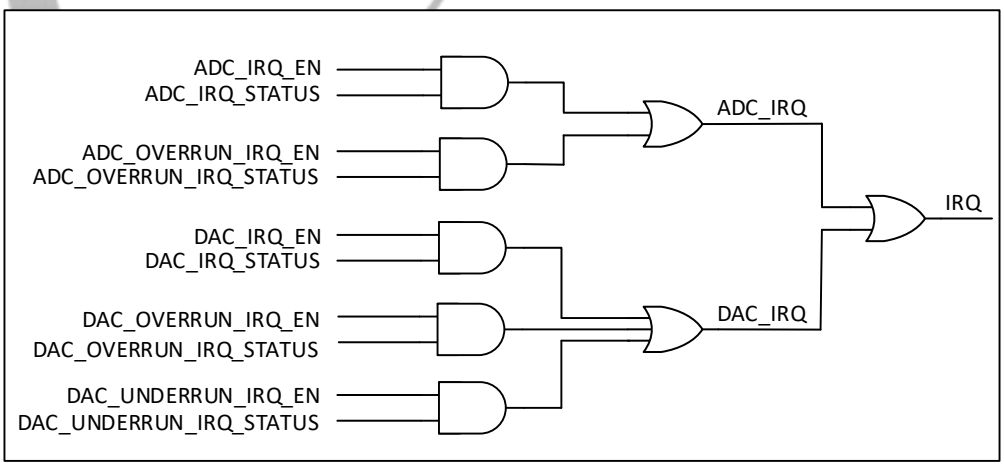
- LINEOUTP

LINEOUTP provides one single-end output to drive line signals to external audio equipment. The LINEOUTP output source from DAC. The volume control is logarithmic with an 43.5 dB rang in 1.5 dB step from -43.5 dB to 0 dB. The LINEOUTP output buffer power up or down by bit[13] or bit[11] of DAC_REG (Offset: 0x0310).

8.3.3.9 Interrupts

The Audio Codec has two interrupts. The following figure describes the Audio Codec interrupt system.

Figure 8-11 Audio Codec Interrupt System

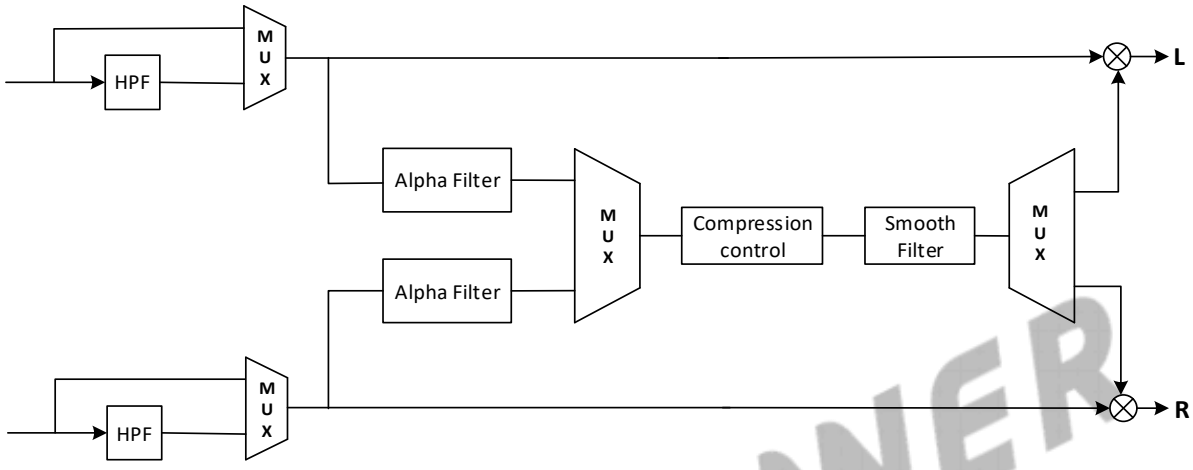


8.3.3.10 Digital Audio Processor (DAP)

The DAP module is used to remove the DC offset and automatically adjusts the volume to a flatten volume level. It mainly consists of two HPF and one DRC.

The following figure shows the DAP data flow.

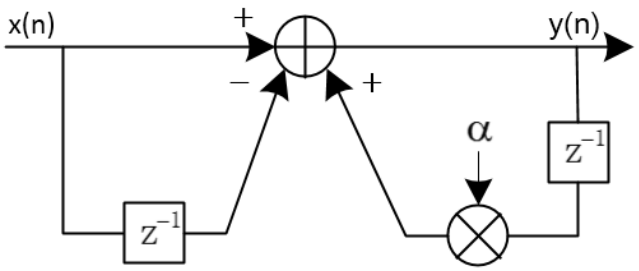
Figure 8-12 DAP Data Flow



HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz that can be removed DC offset from ADC recording. The HPF can also be bypassed.

Figure 8-13 HPF Logic Structure



DRC Function

The DRC scheme has three thresholds, three offsets, and four slopes (all programmable). There is one ganged DRC for the left and right channels. The following figure shows the diagram of DRC input/output.

Figure 8-14 DRC static Curve Parameters

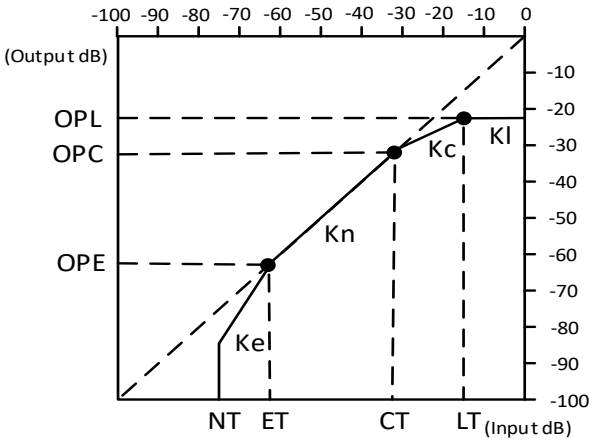
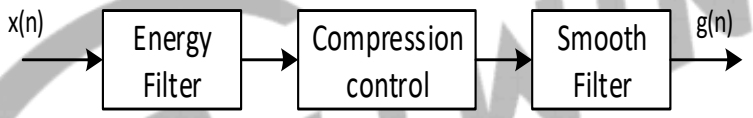


Figure 8-15 DRC Block Diagram



Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

One DRC for left/right and one DRC for subwoofer.

Each DRC has the adjustable threshold, offset, compression levels, programmable energy, attack, and decay time constants.

Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Configure the DRC parameters according to the following guidelines:

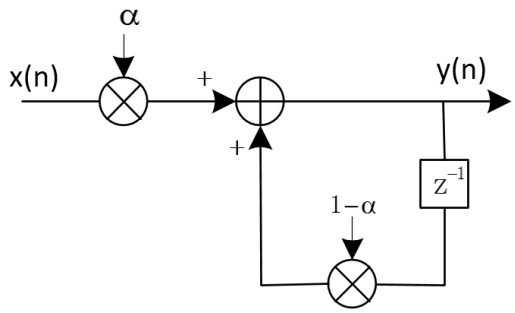
- Number format

The Number format is N.M which means there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 9.23 means that there are 9 bits at the left of the decimal point and 23 bits at the right decimal point.

- Energy Filter

The following figure shows the structure of the energy filter.

Figure 8-16 Energy Filter Structure



The Energy Filter is to estimate of the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by

$\alpha = 1 - e^{-2.2Ts/ta}$

Compression Control

This element has six parameters (ET, CT, LT, Ke, Kn, Kc, Kl, OPL, OPC, OPE), which are all programmable, and the computation will be explained as follows.

- Threshold Parameter Computation (T parameter)

The threshold is the value that determines the signal to be compressed or not. When the signal's RMS is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by $Tin = -\frac{T_{dB}}{6.0206}$

Where, T_{dB} must less than zero, the positive value is illegal.

For example, it is desired to set CT=-40dB, then the Tin require to set CT to -40dB is CTin = - (-40dB)/6.0206 = 6.644, CTin is entered as a 32-bit number in 8.24 format.

Therefore, CTin = 6.644 = 0000 0110.1010 0100 1101 0011 1100 0000 = 0x06A4 D3C0 in 8.24 format.

- Slope Parameter Computation (K parameter)

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB is for n dB RMS input. The k input to the coefficient ram is computed by $K = \frac{1}{n}$

Where, n is from 1 to 50, and must be integer.

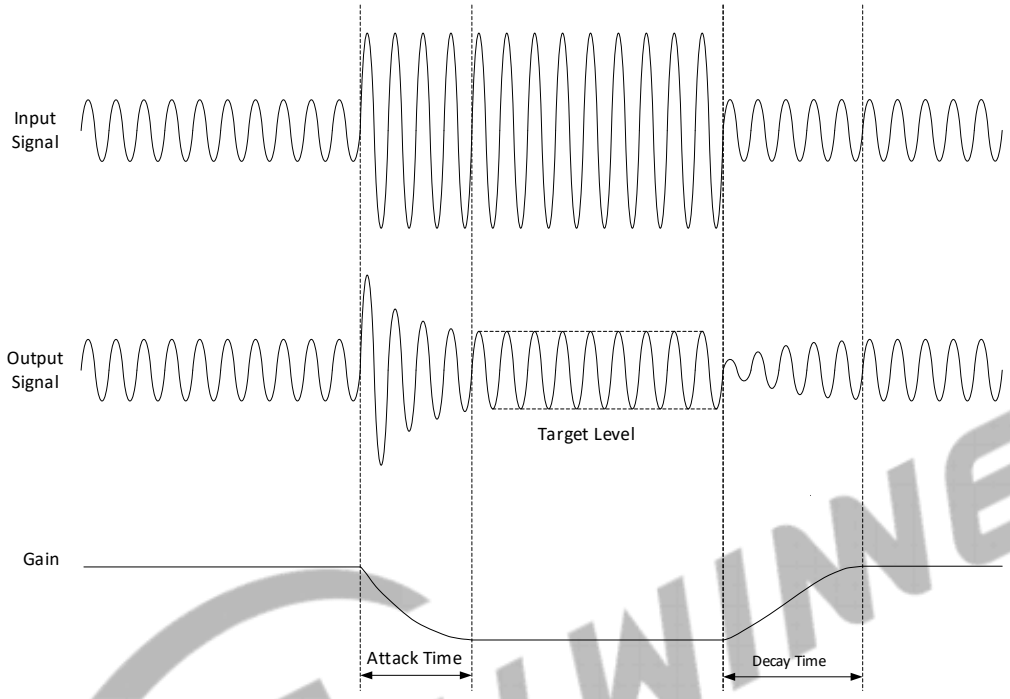
For example, it is desired to set 2:1, then the Kc require to set to 2:1 is Kc = 1/2 = 0.5, Kc is entered as a 32-bit number in 8.24 format.

Therefore, Kc = 0.5 = 0000 0000.1000 0000 0000 0000 0000 0000 = 0x0080 0000 in 8.24 format.

- Gain Smooth Filter

The Gain Smooth Filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 1-17. The structure of the Gain Smooth filter is also the Alpha filter, so the rise time computation is the same as the Energy filter which is $\alpha = 1 - e^{-2.2Ts/ta}$.

Figure 8-17 Gain Smooth Filter



8.3.4 Programming Guidelines

8.3.4.1 Record Process

In recording mode, the analog audio signals are recorded from the microphones at the specified sample rate, processed by the ADC, and then transferred to the DRAM via the DMA.

1. Codec initialization: configure AUDIO_CODEC_BGR_REG to open the audio codec bus clock gating and de-assert bus reset; configure AUDIO_CODEC_ADC_CLK_REG and PLL_AUDIO_CTRL_REG to configure PLL_Audio frequency and enable PLL_Audio. For details, refer to section 3.4 Clock Controller Unit (CCU)
2. Configure the sample rate and data transfer format, then open the ADC.
3. Configure the DMA and DMA request.
4. Enable the ADC DRQ and DMA.

8.3.4.2 Playback Process

In playback mode, the audio data are transferred from the DRAM via DMA, processed by the DAC, and finally output via the analog interface.

1. Codec initialization: configure AUDIO_CODEC_BGR_REG to open the audio codec bus clock gating and de-assert bus reset; configure AUDIO_CODEC_DAC_CLK_REG and PLL_AUDIO_CTRL_REG to configure PLL_Audio frequency and enable PLL_Audio. For details, refer to section 3.4 Clock Controller Unit (CCU)
2. Configure the sample rate and data transfer format, then open the DAC.
3. Configure the DMA and DMA request.
4. Enable the DAC DRQ and DMA.

8.3.5 Register List

Module Name	Base Address	Comments
Audio Codec	0x02030000	ADC/DAC Codec

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
DAC_VOL_CTRL	0x0004	DAC Volume Control Register
AC_DAC_FIFOC	0x0010	DAC FIFO Control Register
AC_DAC_FIFOS	0x0014	DAC FIFO Status Register
AC_DAC_TXDATA	0x0020	DAC TX DATA Register
AC_DAC_CNT	0x0024	DAC TX FIFO Counter Register
AC_DAC_DG	0x0028	DAC Debug Register
AC_ADC_FIFOC	0x0030	ADC FIFO Control Register
ADC_VOL_CTRL1	0x0034	ADC Volume Control1 Register
AC_ADC_FIFOS	0x0038	ADC FIFO Status Register
AC_ADC_RXDATA	0x0040	ADC RX Data Register
AC_ADC_CNT	0x0044	ADC RX Counter Register
AC_ADC_DG	0x004C	ADC Debug Register
ADC_DIG_CTRL	0x0050	ADC Digtial Control Register
VRA1SPEEDUP_DOWN_CTRL	0x0054	VRA1Speedup Down Control Register
AC_DAC_DAP_CTRL	0x00F0	DAC DAP Control Register
AC_ADC_DAP_CTR	0x00F8	ADC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register

Register Name	Offset	Description
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_RPFHRT	0x0124	DAC DRC Right Peak filter High Release Time Coef Register
AC_DAC_DRC_RPFLRT	0x0128	DAC DRC Right Peak filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_RRMSHAT	0x0134	DAC DRC Right RMS Filter High Coef Register
AC_DAC_DRC_RRMSLAT	0x0138	DAC DRC Right RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Threshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Threshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Threshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold
AC_DAC_DRC_HET	0x016C	DAC DRC Expander Threshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Threshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register

Register Name	Offset	Description
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_RPFHAT	0x0214	ADC DRC Right Peak Filter High Attack Time Coef Register
AC_ADC_DRC_RPFLAT	0x0218	ADC DRC Right Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_RPFHRT	0x0224	ADC DRC Right Peak filter High Release Time Coef Register
AC_ADC_DRC_RPFLRT	0x0228	ADC DRC Right Peak filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_RRMSHAT	0x0234	ADC DRC Right RMS Filter High Coef Register
AC_ADC_DRC_RRMSLAT	0x0238	ADC DRC Right RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Threshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Threshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Threshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Threshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Threshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register

Register Name	Offset	Description
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGHS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MNGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
ADC1_REG	0x0300	ADC1 Analog Control Register
DAC_REG	0x0310	DAC Analog Control Register
BIAS_REG	0x0320	BIAS Analog Control Register
POWER_REG	0x0348	POWER Analog Control Register
ADC_CUR_REG	0x034C	ADC Current Analog Control Register

8.3.6 Register Description

8.3.6.1 0x0000 DAC Digital Part Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EN_DA DAC Digital Part Enable 0: Disabled 1: Enabled
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels = [7*(21 + MODQU[3:0])]/128 Default levels = 7*21/128 = 1.15

Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default/Hex**	**Description**
24	R/W	0x0	DWA DWA Function Disable 0: Enabled 1: Disabled
23:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disabled 1: Enabled
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT = DVC[5:0]*(-1.16 dB) 64 steps, -1.16 dB/step
11:1	/	/	/
0	R/W	0x0	HUB_EN Audio Hub Enable The bit takes effect only when the EN_DA is set to 1. System Domain: Audio Codec/I2S1 TXFIFO Hub Enable. 0: Disabled 1: Enabled

8.3.6.2 0x0004 DAC Volume Control Register (Default Value: 0x0000_A0A0)

Offset: 0x0004			Register Name: DAC_VOL_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DAC_VOL_SEL DAC Volume Control Selection Enable 0: Disabled 1: Enabled
15:8	R/W	0xA0	DAC_VOL_L DAC left channel volume (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F = -0.75 dB 0xA0 = 0 dB 0xA1 = 0.75 dB ... 0xFF = 71.25 dB

Offset: 0x0004			Register Name: DAC_VOL_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R/W	0xA0	DAC_VOL_R DAC right channel volume (-119.25 dB To 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F = -0.75 dB 0xA0 = 0 dB 0xA1 = 0.75 dB ... 0xFF = 71.25 dB

8.3.6.3 0x0010 DAC FIFO Control Register (Default Value: 0x0000_4000)

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	DAC_FS Sample Rate of DAC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: 192 kHz 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: 96 kHz 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO underrun 0: Sending zero 1: Sending the last audio sample

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
25:24	R/W	0x0	FIFO_MODE For 20-bit transmitted audio sample: 00/10: FIFO_I[19:0] = {TXDATA[31:12]} 01/11: FIFO_I[19:0] = {TXDATA[19:0]} For 16-bit transmitted audio sample: 00/10: FIFO_I[19:0] = {TXDATA[31:16], 4'b0} 01/11: FIFO_I[19:0] = {TXDATA[15:0], 4'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, the DRQ request will be de-asserted. N is defined here: 00: IRQ/DRQ de-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ generated when WLEVEL ≤ TXTL **Note: WLEVEL represents the number of valid samples in the TX FIFO. Only TXTL[6:0] valid when TXMODE = 0.**
7	/	/	/
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 levels FIFO 1: Mono, 128 levels FIFO When enabled, L & R channel send the same data.
5	R/W	0x0	TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 20 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disabled 1: Enabled
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disabled 1: Enabled

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Underrun IRQ Enable 0: Disabled 1: Enabled
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Overrun IRQ Enable 0: Disabled 1: Enabled
0	R/WC	0x0	FIFO_FLUSH DAC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

8.3.6.4 0x0014 DAC FIFO Status Register (Default Value: 0x0080_8008)

Offset: 0x0014			Register Name: AC_DAC_FIFOS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatically clear if the interrupt condition fails.
2	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

8.3.6.5 0x0020 DAC TX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Write the transmitting left and right channel sample data to this register one by one. Write the left channel sample data first and then the right channel sample.

8.3.6.6 0x0024 DAC TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: AC_DAC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After being updated by the initial value, the counter register should count from this initial value. **Note: It is used for Audio/Video Synchronization.**

8.3.6.7 0x0028 DAC Debug Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT DAC Pattern Select 00: Normal (Audio sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: Silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC clock from PLL 1: CODEC clock from OSC (for Debug)
7	/	/	/

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	DA_SWP DAC Output Channel Swap Enable 0: Disabled 1: Enabled
5:3	/	/	/
2:0	R/W	0x0	ADDA_LOOP_MODE ADDA Loop Mode Select 000: Disabled 001: ADDA LOOP MODE DACL/DACR is connected to ADC1/ADC2 010: ADDA LOOP MODE DACL/DACR is connected to ADC3 Others: Reserved

8.3.6.8 0x0030 ADC FIFO Control Register (Default Value: 0x0000_0400)

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disabled 1: Enabled
27:26	R/W	0x0	ADCFDT ADC FIFO delay time for writing data after EN_AD 00: 5 ms 01: 10 ms 10: 20 ms 11: 30 ms
25	R/W	0x0	ADCDFEN ADC FIFO delay function for writing data after EN_AD 0: Disabled 1: Enabled

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 20-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[19:0], 12'h0} Mode 1: RXDATA[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0]} For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[19:4], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[19]}, FIFO_O[19:4]}
23:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START The bit takes effect only when RX_SYNC_EN is set to 1. System Domain: Audio codec/I2S1/DMIC Synchronize Enable Start. 0: Disabled 1: Enabled
20	R/W	0x0	RX_SYNC_EN Audiocodec RX Synchronize Enable 0: Disabled 1: Enabled
19:17	/	/	/
16	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 20 bits
15:12	/	/	/
11:4	R/W	0x40	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL[5:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ generated when WLEVEL > RXTL[5:0] **Note: WLEVEL represents the number of valid samples in the RX FIFO.**
3	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disabled 1: Enabled
2	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disabled 1: Enabled

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disabled 1: Enabled
0	R/WC	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'.

8.3.6.9 0x0034 ADC Volume Control1 Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: ADC_VOL_CTRL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	Reserved
23:16	R/W	0xA0	ADC3_VOL ADC3 channel volume (-119.25 dB To 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
15:8	R/W	0xA0	ADC2_VOL ADC2 channel volume (-119.25 dB To 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

Offset: 0x0034			Register Name: ADC_VOL_CTRL1
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0xA0	ADC1_VOL ADC1 channel volume (-119.25 dB To 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

8.3.6.10 0x0038 ADC FIFO Status Register (Default Value: 0x0000_0001)

Offset: 0x0038			Register Name: AC_ADC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:17	/	/	/
16:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W1C	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if the interrupt condition fails.
2	/	/	/
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt.
0	R	0x1	Reserved

8.3.6.11 0x0040 ADC RX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample The host can get one sample by reading this register. The left channel sample data comes first and then the right channel sample.

8.3.6.12 0x0044 ADC RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After being updated by the initial value, the counter register should count from this initial value. **Note: It is used for Audio/Video Synchronization.**

8.3.6.13 0x004C ADC Debug Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	AD_SWP1 ADC output channel swap enable (for digital filter) 0: Disabled 1: Enabled **Note: ADC1 swap data.**
23:0	/	/	/

8.3.6.14 0x0050 ADC Digital Control Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ADC_DIG_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/

Offset: 0x0050			Register Name: ADC_DIG_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	ADC1_VOL_EN ADC1 Volume Control Enable 0: Disabled 1: Enabled
15:1	/	/	/
0	R/W	0x0	ADC_CHANNEL_EN ADC1 enabled

8.3.6.15 0x0054 VRA1 Speedup Down Control Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: VRA1SPEEDUP_DOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	VRA1SPEEDUP_DOWN_STATE Only if VAR1SPEEDUP_DOWN_Further_CTRL (0x310[22]) is set 0, VAR1Speedup Down State is valid. 0: VAR1Speedup_Down does not work. 1: VAR1Speedup_Down works.
3:2	/	/	/
1	R/W	0x0	VRA1SPEEDUP_DOWN_CTRL VAR1Speedup Down Manual Control Enable 0: Disabled. VAR1Speedup Down converts to 1 after the bus rst releases 32 ms. 1: Enabled. VAR1Speedup Down converts to 1 immediately.
0	R/W	0x0	VRA1SPEEDUP_DOWN_RST_CTRL VAR1Speedup Down RST Manual Control Enable 0: Disabled. VAR1Speedup Down converts to 1 after the bus rst releases 32 ms. 1: Enabled. VAR1Speedup Down reset 0 immediately.

8.3.6.16 0x00F0 DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDAP_EN DAP for DRC enable 0: Bypassed 1: Enabled
30	/	/	/

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
29	R/W	0x0	DDAP_DRC_EN DRC enable control 0: Disabled 1: Enabled
28	R/W	0x0	DDAP_HPF_EN HPF enable control 0: Disabled 1: Enabled
27:0	/	/	/

8.3.6.17 0x00F8 ADC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_DAP0_EN (control the DAP of ADC1) DAP for ADC enable 0: Bypassed 1: Enabled
30	/	/	/
29	R/W	0x0	ADC_DRC0_EN ADC DRC0 enable control 0: Disabled 1: Enabled
28	R/W	0x0	ADC_HPF0_EN ADC HPF0 enable control 0: Disabled 1: Enabled
27:0	/	/	/

8.3.6.18 0x0100 DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

8.3.6.19 0x0104 DAC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

8.3.6.20 0x0108 DAC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when The DRC delay function is enabled and the DRC function is disabled. After disabling the DRC function and this bit goes to 0, write the DRC delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00: (8x1) fs 6'h01: (8x2) fs 6'h02: (8x3) fs ---------- 6'h2e: (8*47) fs 6'h2f: (8*48) fs 6'h30 -- 6'h3f: (8*48) fs Delay time = 8*(n + 1) fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	DAC_DRC_DELAY_BUF_EN The delay buffer use or not when the DRC is disabled and the DRC buffer data output completely. 0: Do not use the buffer. 1: Use the buffer.
6	R/W	0x0	DAC_DRC_GAIN_MAX_LIMIT_EN DRC gain max limit enable 0: Disabled 1: Enabled

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	DAC_DRC_GAIN_MIN_LIMIT_EN DRC gain min limit enable When this function is enabled, it will overwrite the noise detect function. 0: Disabled 1: Enabled
4	R/W	0x0	DAC_DRC_DETECT_NOISE_EN Control the DRC to detect noise when ET is enabled. 0: Disabled 1: Enabled
3	R/W	0x0	DAC_DRC_SIGNAL_FUNC_SEL Signal function select 0: RMS filter 1: Peak filter When the signal function selects the Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT, AC_DRC_LRMSLAT, AC_DRC_LRMSHAT, AC_DRC_LRMSLAT) When the signal function selects the RMS filter, the Peak filter parameter is unused. (AC_DRC_LPFHAT, AC_DRC_LPFLAT, AC_DRC_RPFHAT, AC_DRC_RPFLAT, AC_DRC_LPFHRT, AC_DRC_LPFLRT, AC_DRC_RPFHRT, and AC_DRC_RPFLRT)
2	R/W	0x0	DAC_DRC_DELAY_FUNC_EN Delay function enable 0: Disabled 1: Enabled When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DAC_DRC_LT_EN DRC LT enable 0: Disabled 1: Enabled When the bit is disabled, KI and OPL parameter is unused.
0	R/W	0x0	DAC_DRC_ET_EN DRC ET enable 0: Disabled 1: Enabled When the bit is disabled, Ke and OPE parameter is unused.

8.3.6.21 0x010C DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x000B	DAC_DRC_LPFHAT The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.22 0x0110 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	DAC_DRC_LPFLAT The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.23 0x0114 DAC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0114			Register Name: AC_DAC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xB	DAC_DRC_RPFHAT The right peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.24 0x0118 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	DAC_DRC_RPFLAT The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.25 0x011C DAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x00FF	DAC_DRC_LPFHRT The left peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.26 0x0120 DAC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	DAC_DRC_LPFLRT The left peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.27 0x0124 DAC DRC Right Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0124			Register Name: AC_DAC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFF	DAC_DRC_RPFHRT The right peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.28 0x0128 DAC DRC Right Peak filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0128			Register Name: AC_DAC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	DAC_DRC_RPFLRT The right peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.29 0x012C DAC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0001	DAC_DRC_LRMSHAT The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.30 0x0130 DAC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_LRMSLAT The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.31 0x0134 DAC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0134			Register Name: AC_DAC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_RRMSHAT The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.32 0x0138 DAC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0138			Register Name: AC_DAC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	DAC_DRC_RRMSLAT The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.33 0x013C DAC DRC Compressor Theshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x06A4	DAC_DRC_HCT The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.34 0x0140 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	DAC_DRC_LCT The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.35 0x0144 DAC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	DAC_DRC_HKC The slope of the compressor, which is determined by the equation that Kc = 1/R. R is the ratio of the compressor, which is always an integer. The format is 8.24. (The default value is 2:1)

8.3.6.36 0x0148 DAC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKC The slope of the compressor, which is determined by the equation that Kc = 1/R. R is the ratio of the compressor, which is always an integer. The format is 8.24. (The default value is 2:1)

8.3.6.37 0x014C DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xF95B	DAC_DRC_HOPC The output of the compressor, which is determined by the equation -OPC/6.0206. The format is 8.24 (The default value is -40 dB)

8.3.6.38 0x0150 DAC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	DAC_DRC_LOPC The output of the compressor, which is determined by the equation OPC/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.39 0x0154 DAC DRC Limiter Theshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	DAC_DRC_HLT The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (The default value is -10 dB)

8.3.6.40 0x0158 DAC DRC Limiter Theshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	DAC_DRC_LLT The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10 dB)

8.3.6.41 0x015C DAC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0005	DAC_DRC_HKl The slope of the limiter which is determined by the equation that Kl = 1/R. R is the ratio of the limiter, which is always an integer. The format is 8.24. (The default value is <50:1>)

8.3.6.42 0x0160 DAC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	DAC_DRC_LKl The slope of the limiter, which is determined by the equation that Kl = 1/R. R is the ratio of the limiter, which is always an integer. The format is 8.24. (The default value is <50:1>)

8.3.6.43 0x0164 DAC DRC Limiter High Output at Limiter Threshold Register (Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	DAC_DRC_HOPL The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25 dB)

8.3.6.44 0x0168 DAC DRC Limiter Low Output at Limiter Threshold Register (Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	DAC_DRC_LOPL The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25 dB)

8.3.6.45 0x016C DAC DRC Expander Theshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0BA0	DAC_DRC_HET The expander threshold setting, which is set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70 dB)

8.3.6.46 0x0170 DAC DRC Expander Theshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	DAC_DRC_LET The expander threshold setting, which is set by the equation that ETin = -ET/6.0206. The format is 8.24. (The default value is -70 dB)

8.3.6.47 0x0174 DAC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0500	DAC_DRC_HKE The slope of the expander, which is determined by the equation that Ke = 1/R. R is the ratio of the expander, which is always an integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

8.3.6.48 0x0178 DAC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKE The slope of the expander, which is determined by the equation that Ke = 1/R. R is the ratio of the expander, which is always an integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

8.3.6.49 0x017C DAC DRC Expander High Output at Expander Threshold Register (Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xF45F	DAC_DRC_HOPE The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70 dB)

8.3.6.50 0x0180 DAC DRC Expander Low Output at Expander Threshold Register (Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	DAC_DRC_LOPE The output of the expander which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70 dB)

8.3.6.51 0x0184 DAC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	DAC_DRC_HKN The slope of the linear, which is determined by the equation that Kn = 1/R. R is the ratio of the linear, which is always an integer. The format is 8.24. (The default value is <1:1>)

8.3.6.52 0x0188 DAC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_LKN The slope of the linear, which is determined by the equation that Kn = 1/R. R is the ratio of the linear, which is always an integer. The format is 8.24. (The default value is <1:1>)

8.3.6.53 0x018C DAC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0002	DAC_DRC_SFHAT The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 5 ms)

8.3.6.54 0x0190 DAC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	DAC_DRC_SFLAT The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 5 ms)

8.3.6.55 0x0194 DAC DRC Smooth Filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	DAC_DRC_SFHRT The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 200 ms)

8.3.6.56 0x0198 DAC DRC Smooth Filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	DAC_DRC_SFLRT The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 200 ms)

8.3.6.57 0x019C DAC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xFE56	DAC_DRC_MXGHS The max gain setting, which is determined by equation MXGin=MXG/6.0206. The format is 8.24 and must -20 dB < MXG < 30 dB (The default value is -10 dB)

8.3.6.58 0x01A0 DAC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	DAC_DRC_MXGLS The max gain setting, which is determined by equation MXGin=MXG/6.0206. The format is 8.24 and must -20 dB < MXG < 30 dB (The default value is -10 dB)

8.3.6.59 0x01A4 DAC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	DAC_DRC_MNGHS The min gain setting, which is determined by equation MXGin=MXG/6.0206. The format is 8.24 and must -60 dB ≤ MNG ≤ -40 dB (The default value is -40 dB)

8.3.6.60 0x01A8 DAC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	DAC_DRC_MNGLS The min gain setting, which is determined by equation MXGin=MNG/6.0206. The format is 8.24 and must -60 dB ≤ MNG ≤ -40 dB (The default value is -40 dB)

8.3.6.61 0x01AC DAC DRC Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0000	DAC_DRC_EPSHC The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 30 ms)

8.3.6.62 0x01B0 DAC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	DAC_DRC_EPSLC The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 30 ms)

8.3.6.63 0x01B8 DAC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	DAC_DRC_HPFHGAIN The gain of HPF coefficient. The format is 3.24. (gain = 1)

8.3.6.64 0x01BC DAC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	DAC_DRC_HPFLGAIN The gain of HPF coefficient. The format is 3.24. (gain = 1)

8.3.6.65 0x0200 ADC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0xFF	ADC_DRC_HHPFC HPF coefficient setting and the data is 3.24 format.

8.3.6.66 0x0204 ADC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

8.3.6.67 0x0208 ADC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ADC_DRC_DELAY_BUF_OUTPUT_STATE DRC delay buffer data output state when The DRC delay function is enabled and the DRC function is disabled. After disabled DRC function and this bit goes to 0, the user should write the DRC delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	ADC_DRC_SIGNAL_DELAY_TIME_SET Signal delay time setting 6'h00: (8x1) fs 6'h01: (8x2) fs 6'h02: (8x3) fs ---------- 6'h2e: (8*47) fs 6'h2f: (8*48) fs 6'h30 -- 6'h3f: (8*48) fs Delay time = 8*(n + 1) fs, n < 6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	ADC_DRC_DELAY_BUF_EN The delay buffer use or not when the DRC is disabled and the DRC buffer data output completely. 0: Do not use the buffer 1: Use the buffer
6	R/W	0x0	ADC_DRC_GAIN_MAX_LIMIT_EN DRC gain max limit enable 0: Disabled 1: Enabled

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	ADC_DRC_GAIN_MIN_LIMIT_EN DRC gain min limit enable When this fuction is enabled, it will overwrite the noise detect function. 0: Disabled 1: Enabled
4	R/W	0x0	ADC_DRC_DETECT_NOISE_EN Control the DRC to detect noise when ET is enabled 0: Disabled 1: Enabled
3	R/W	0x0	ADC_DRC_SIGNAL_FUNC_SEL Signal function select 0: RMS filter 1: Peak filter When the signal function selects the Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT, AC_DRC_LRMSLAT, AC_DRC_LRMSHAT, and AC_DRC_LRMSLAT) When the signal function selects the RMS filter, the Peak filter parameter is unused. (AC_DRC_LPFHAT, AC_DRC_LPFLAT, AC_DRC_RPFHAT, AC_DRC_RPFLAT, AC_DRC_LPFHRT, AC_DRC_LPFLRT, AC_DRC_RPFHRT, and AC_DRC_RPFLRT)
2	R/W	0x0	ADC_DRC_DELAY_FUNC_EN Delay function enable 0: Disabled 1: Enabled When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	ADC_DRC_LT_EN DRC LT enable 0: Disabled 1: Enabled When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	ADC_DRC_ET_EN DRC ET enable 0: Disabled 1: Enabled When the bit is disabled, Ke and OPE parameter is unused.

8.3.6.68 0x020C ADC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x000B	ADC_DRC_LPFHAT The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.69 0x0210 ADC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	ADC_DRC_LPFLAT The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.70 0x0214 ADC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0214			Register Name: AC_ADC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x000B	ADC_DRC_RPFHAT The right peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.71 0x0218 ADC DRC Right Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0218			Register Name: AC_ADC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	ADC_DRC_RPFLAT The right peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/ta). The format is 3.24. (The default value is 1 ms)

8.3.6.72 0x021C ADC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x00FF	ADC_DRC_LPFHRT The left peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.73 0x0220 ADC DRC Left Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	ADC_DRC_LPFLRT The left peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.74 0x0224 ADC DRC Right Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0224			Register Name: AC_ADC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	ADC_DRC_RPFHRT The right peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.75 0x0228 ADC DRC Right Peak Filter Low Release Time Coef Register (Default Value: 0x0000_E1F8)

Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	ADC_DRC_RPFLRT The right peak filter release time parameter setting, which is determined by the equation that RT = exp (-2.2Ts/tr). The format is 3.24. (The default value is 100 ms)

8.3.6.76 0x022C ADC DRC Left RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0001	ADC_DRC_LRMSHAT The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.77 0x0230 ADC DRC Left RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	ADC_DRC_LRMSLAT The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.78 0x0234 ADC DRC Right RMS Filter High Coef Register (Default Value: 0x0000_0001)

Offset: 0x0234			Register Name: AC_ADC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	ADC_DRC_RRMSHAT The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.79 0x0238 ADC DRC Right RMS Filter Low Coef Register (Default Value: 0x0000_2BAF)

Offset: 0x0238			Register Name: AC_ADC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	ADC_DRC_RRMSLAT The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tav). The format is 3.24. (The default value is 10 ms)

8.3.6.80 0x023C ADC DRC Compressor Theshold High Setting Register (Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x06A4	ADC_DRC_HCT The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.81 0x0240 ADC DRC Compressor Slope High Setting Register (Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	ADC_DRC_LCT The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.82 0x0244 ADC DRC Compressor Slope High Setting Register (Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	ADC_DRC_HKC The slope of the compressor which is determined by the equation that Kc = 1/R. R is the ratio of the compressor, which is always an integer. The format is 8.24. (The default value is <2:1>)

8.3.6.83 0x0248 ADC DRC Compressor Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKC The slope of the compressor, which is determined by the equation that Kc = 1/R. R is the ratio of the compressor, which is always an integer. The format is 8.24. (The default value is <2:1>)

8.3.6.84 0x024C ADC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xF95B	ADC_DRC_HOPC The output of the compressor, which is determined by the equation -OPC/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.85 0x0250 ADC DRC Compressor Low Output at Compressor Threshold Register (Default Value: 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	ADC_DRC_LOPC The output of the compressor, which is determined by the equation OPC/6.0206. The format is 8.24. (The default value is -40 dB)

8.3.6.86 0x0254 ADC DRC Limiter Theshold High Setting Register (Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	ADC_DRC_HLT The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10 dB)

8.3.6.87 0x0258 ADC DRC Limiter Theshold Low Setting Register (Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	ADC_DRC_LLT The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10 dB)

8.3.6.88 0x025C ADC DRC Limiter Slope High Setting Register (Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
13:0	R/W	0x0005	ADC_DRC_HKl The slope of the limiter, which is determined by the equation that Kl = 1/R. R is the ratio of the limiter, which is always an integer. The format is 8.24. (The default value is <50:1>)

8.3.6.89 0x0260 ADC DRC Limiter Slope Low Setting Register (Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	ADC_DRC_LKl The slope of the limiter, which is determined by the equation that Kl = 1/R. R is the ratio of the limiter, which is always an integer. The format is 8.24. (The default value is <50:1>)

8.3.6.90 0x0264 ADC DRC Limiter High Output at Limiter Threshold Register (Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	ADC_DRC_HOPL The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25 dB)

8.3.6.91 0x0268 ADC DRC Limiter Low Output at Limiter Threshold Register (Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	ADC_DRC_LOPL The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25 dB)

8.3.6.92 0x026C ADC DRC Expander Theshold High Setting Register (Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0BA0	ADC_DRC_HET The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70 dB)

8.3.6.93 0x0270 ADC DRC Expander Theshold Low Setting Register (Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	ADC_DRC_LET The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70 dB)

8.3.6.94 0x0274 ADC DRC Expander Slope High Setting Register (Default Value: 0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0500	ADC_DRC_HKE The slope of the expander, which is determined by the equation that Ke = 1/R. R is the ratio of the expander, which is always an integer and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

8.3.6.95 0x0278 ADC DRC Expander Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKE The slope of the expander, which is determined by the equation that Ke = 1/R. R is the ratio of the expander, which is always an integer and the ke must be larger than 50. The format is 8.24. (The default value is <1:5>)

8.3.6.96 0x027C ADC DRC Expander High Output at Expander Threshold Register (Default Value: 0x0000_F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xF45F	ADC_DRC_HOPE The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70 dB)

8.3.6.97 0x0280 ADC DRC Expander Low Output at Expander Threshold Register (Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	ADC_DRC_LOPE The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70 dB)

8.3.6.98 0x0284 ADC DRC Linear Slope High Setting Register (Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	ADC_DRC_HKN The slope of the linear, which is determined by the equation that Kn = 1/R. R is the ratio of the linear, which is always an integer. The format is 8.24. (The default value is <1:1>)

8.3.6.99 0x0288 ADC DRC Linear Slope Low Setting Register (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_LKN The slope of the linear, which is determined by the equation that Kn = 1/R. R is the ratio of the linear, which is always an integer. The format is 8.24. (The default value is <1:1>)

8.3.6.100 0x028C ADC DRC Smooth Filter Gain High Attack Time Coef Register (Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0002	ADC_DRC_SFHAT The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 5 ms)

8.3.6.101 0x0290 ADC DRC Smooth Filter Gain Low Attack Time Coef Register (Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	ADC_DRC_SFLAT The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 5 ms)

8.3.6.102 0x0294 ADC DRC Smooth Filter Gain High Release Time Coef Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	ADC_DRC_SFHRT The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 200 ms)

8.3.6.103 0x0298 ADC DRC Smooth Filter Gain Low Release Time Coef Register (Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	ADC_DRC_SFLRT The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 200 ms)

8.3.6.104 0x029C ADC DRC MAX Gain High Setting Register (Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0xFE56	ADC_DRC_MXGHS The max gain setting, which is determined by equation MXGin=MXG/6.0206. The format is 8.24 and must -20 dB < MXG < 30 dB (The default value is -10 dB)

8.3.6.105 0x02A0 ADC DRC MAX Gain Low Setting Register (Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	ADC_DRC_MXGLS The max gain setting, which is determined by equation MXGin=MXG/6.0206. The format is 8.24 and must -20 dB < MXG < 30 dB (The default value is -10 dB)

8.3.6.106 0x02A4 ADC DRC MIN Gain High Setting Register (Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	ADC_DRC_MNGHS The min gain setting, which is determined by equation MXGin=MXG/6.0206. The format is 8.24 and must -60 dB ≤ MNG ≤ -40 dB (The default value is -40 dB)

8.3.6.107 0x02A8 ADC DRC MIN Gain Low Setting Register (Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	ADC_DRC_MNGLS The min gain setting, which is determined by equation MXGin=MNG/6.0206. The format is 8.24 and must -60 dB ≤ MNG ≤ -40 dB (The default value is -40 dB)

8.3.6.108 0x02AC ADC DAP Expander Smooth Time High Coef Register (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
10:0	R/W	0x0000	ADC_DRC_EPSHC The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 30 ms)

8.3.6.109 0x02B0 ADC DRC Expander Smooth Time Low Coef Register (Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	ADC_DRC_EPSLC The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp (-2.2Ts/tr). The format is 3.24. (The default value is 30 ms)

8.3.6.110 0x02B8 ADC DRC HPF Gain High Coef Register (Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	ADC_DRC_HPFHGAIN The gain of HPF coefficient setting, which format is 3.24. (gain = 1)

8.3.6.111 0x02BC ADC DRC HPF Gain Low Coef Register (Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	ADC_DRC_HPFLGAIN The gain of HPF coefficient setting, which format is 3.24. (gain = 1)

8.3.6.112 0x0300 ADC1 Analog Control Register (Default Value: 0x001C_C055)

Offset: 0x0300			Register Name: ADC1_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ADC1_EN ADC1 Channel Enable 0: Disabled 1: Enabled

Offset: 0x0300			Register Name: ADC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0x0	MIC1_PGA_EN MIC1 PGA Enable 0: Disable 1: Enable
29	R/W	0x0	ADC1 Dither Control 0: New Dither Off 1: New Dither On
28	R/W	0x0	MIC1_SIN_EN MIC1 Single Input Enable 0:Disable 1:Enable
27:26	/	/	/
25:24	R/W	0x0	DSM_DITHER_LVL Dither Level Control (Dither level is positive ralated to the ctrl bits) 00: No Level 01: Min Level 10: Middle Level 11: Max Level
23:22	/	/	/
21:20	R/W	0x1	IOPBUFFER PGA Vcm Buffer OP Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
19:18	R/W	0x3	ADC1_PGA_CTRL_RCM ADC1 PGA Common Mode Input Impedance Control for MICIN 00: 100 kΩ 01: 75 kΩ 10: 50 kΩ 11: 25 kΩ
17:16	R/W	0x0	ADC1_PGA_IN_VCM_CTRL ADC1 PGA Common-Mode Voltage Control 00: 900 mV 01: 800 mV 10: 750 mV 11: 700 mV

Offset: 0x0300			Register Name: ADC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	R/W	0x3	IOPADC ADC1-ADC2 Bias Current Select 00: 1 uA 01: 2 uA 10: 3 uA 11: 4 uA
13	R/W	0x0	ADC1_SINGLE_NOISE_CONTROL 0: Disable 1: Enable
12:8	R/W	0x0	ADC1_PGA_GAIN_CTRL ADC1 PGA gain settings: 0x0: 0 dB 0x10: 21 dB 0x1: 6 dB 0x11: 22 dB 0x2: 6 dB 0x12: 23 dB 0x3: 6 dB 0x13: 24 dB 0x4: 9 dB 0x14: 25 dB 0x5: 10 dB 0x15: 26 dB 0x6: 11 dB 0x16: 27 dB 0x7: 12 dB 0x17: 28 dB 0x8: 13 dB 0x18: 29 dB 0x9: 14 dB 0x19: 30 dB 0xA: 15 dB 0x1A: 31 dB 0xB: 16 dB 0x1B: 32 dB 0xC: 17 dB 0x1C: 33 dB 0xD: 18 dB 0x1D: 34 dB 0xE: 19 dB 0x1E: 35 dB 0xF: 20 dB 0x1F: 36 dB
7:6	R/W	0x1	ADC1_IOPAAF ADC1 OP AAF Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1 uA to 4 uA. For example: ADC1_REG<15:14> = 11, IOPADC = 4 uA 00: 1.50*4 uA = 6 uA 01: 1.75*4 uA = 7 uA 10: 2.00*4 uA = 8 uA 11: 2.25*4 uA = 9 uA

Offset: 0x0300			Register Name: ADC1_REG
Bit	Read/Write	Default/Hex	Description
5:4	R/W	0x1	ADC1_IOPSDM1 ADC1 OP SDM Bias Current Select 1 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1 uA to 4 uA.
3:2	R/W	0x1	ADC1_IOPSDM2 ADC1 OP SDM Bias Current Select 2 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1 uA to 4 uA.
1:0	R/W	0x1	ADC1_IOPMIC ADC1 OP MIC Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1 uA to 4 uA.

8.3.6.113 0x0310 DAC Analog Control Register (Default Value: 0x0015_0000)

Offset: 0x0310			Register Name: DAC_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	P_CURRENT_TEST_SELECT Internal Current Sink Test Enable (from LINEOUTP pin) 00: Normal 01: test ip20u_test1 10: test ip20u_test2 11: test ib50u_usb
23:22	R/W	0x0	N_CURRENT_TEST_SELECT Internal Current Sink Test Enable (from LINEOUTP pin) 00: Normal 01: test in10u_test1 10: test inp10u_tvin_cvbsin 11: test two current together
21:20	/	/	/

Offset: 0x0310			Register Name: DAC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
19:18	R/W	0x1	ILINEOUTAMPS LINEOUTLL/R AMP Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
17:16	R/W	0x1	IOPDACS OPDACL/R Bias Current Select 00: 6 uA 01: 7 uA 10: 8 uA 11: 9 uA
15	R/W	0x0	DACL_EN DACL Enable 0: Disabled 1: Enabled
14	/	/	/
13	R/W	0x0	LINEOUTLEN Left Channel LINEOUT Enable 0: Disable 1: Enable
12	R/W	0x0	LMUTE DACL to Left Channel LINEOUT Mute Control 0: Mute 1: Not mute
11:9	/	/	/
8:7	R/W	0x0	VRA2_OPVR_OI_CTRL VRA2 Feedback Buffer Output Current Select 00: 35I 01: 28I 10: 45I 11: 38I I=7uA
6	R/W	0x0	LINEOUTL_DIFFEN Left Channel LINEOUT Output Control 0: Single-End 1: Differential
5	/	/	/
4:0	R/W	0x0	LINEOUT_VOL_CTRL LINEOUT Volume Control. Total 30 level from 0x1F to 0x02 with the volume 0 dB to -43.5 dB, -1.5 dB/step, mute when 00000 & 00001.

8.3.6.114 0x0320 BIAS Analog Control Register (Default Value: 0x0000_0080)

The register is not controlled by the clock and reset of Audio Codec, only controlled by the clock and reset of system bus.

Offset: 0x0320			Register Name: BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x80	BIASDATA Bias Current Register Setting Data

8.3.6.115 0x0348 POWER Analog Control Register (Default Value:0x8000_3019)

The register is not controlled by the clock and reset of Audio Codec, only controlled by the clock and reset of system bus.

Offset: 0x0348			Register Name: POWER_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	ALDO_EN ALDO Enable 0: Disabled 1: Enabled
30	/	/	/
29	R/W	0x0	VAR1SPEEDUP_DOWN_Further_CTRL VAR1 Speedup Down Further Control In Adda Analog 0: The digital logic signal input by the digital-analog interface pin controls the var1_speedup_down function (that is, the var1 signal is rapidly pulled up/down) 1: Writing 1 can finish the var1_speedup_down function (ignore the control of the digital-analog interface pin)
28:16	/	/	/
15	R	0x0	BG_BUFFER_DISABLE BG Output Buffer Disable Control 0: Enable 1: Disable
14:12	R/W	0x3	ALDO_OUTPUT_VOLTAGE ALDO Output Voltage Control 000: 2.03 V 001: 1.95 V 010: 1.87 V 011: 1.80 V 100: 1.73 V 101: 1.67 V 110: 1.61 V 111: 1.56 V

Offset: 0x0348			Register Name: POWER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0x0	BG_ROUGH_TRIM BG Output Voltage Rough Trim Every step is 30mV. Output voltage settings: 0x0: 850mV 0x8: 940mV 0x1: 730mV 0x9: 970mV 0x2: 760mV 0xA: 1000mV 0x3: 790mV 0xB: 1030mV 0x4: 820mV 0xC: 1060mV 0x5: 700mV 0xD: 1090mV 0x6: 880mV 0xE: 1120mV 0x7: 910mV 0xF: 1150mV
7:0	R/W	0x25	BG_FINE_TRIM BG Output Voltage Fine Trim Only low 6-bit is used and every step is 0.8mV. The BG output voltage range is from rough trim value to rough trim value+0.8mV*63. **Note: this register only controlled by system bus clock and reset.**

8.3.6.116 0x034C ADC Current Analog Control Register (Default Value: 0x0000_1515)

Offset: 0x034C			Register Name: ADC_CUR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x1	ADC1_IOPMIC2 ADC1 OP MIC2 Bias Current Select 00: 1.50*IOPADC 01: 1.75*IOPADC 10: 2.00*IOPADC 11: 2.25*IOPADC IOPADC is defined by ADC1_REG<15:14> from 1 uA to 4 uA.
3:2	R/W	0x1	ADC1_OUTPUT_CURRENT ADC1 OP MIC1 Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7 uA

Offset: 0x034C			Register Name: ADC_CUR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x1	ADC1_OUTPUT_CURRENT ADC1 OP MIC2 Output Current Select 00: 15I 01: 20I 10: 35I 11: 40I I=7 uA

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9 EMAC

9.1 Overview

The Ethernet Medium Access Controller (EMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100Mbit/s external PHY with RMII interface in both full and half duplex mode. The Internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 2 KBytes TXFIFO and 8 KBytes RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC has the following features:

- Supports 10/100Mbit/s data transfer rates
- Supports RMII PHY interface
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KBytes
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KBytes of data
- Supports 2KB TXFIFO for transmission packets and 8KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions
- Support MDIO Interface

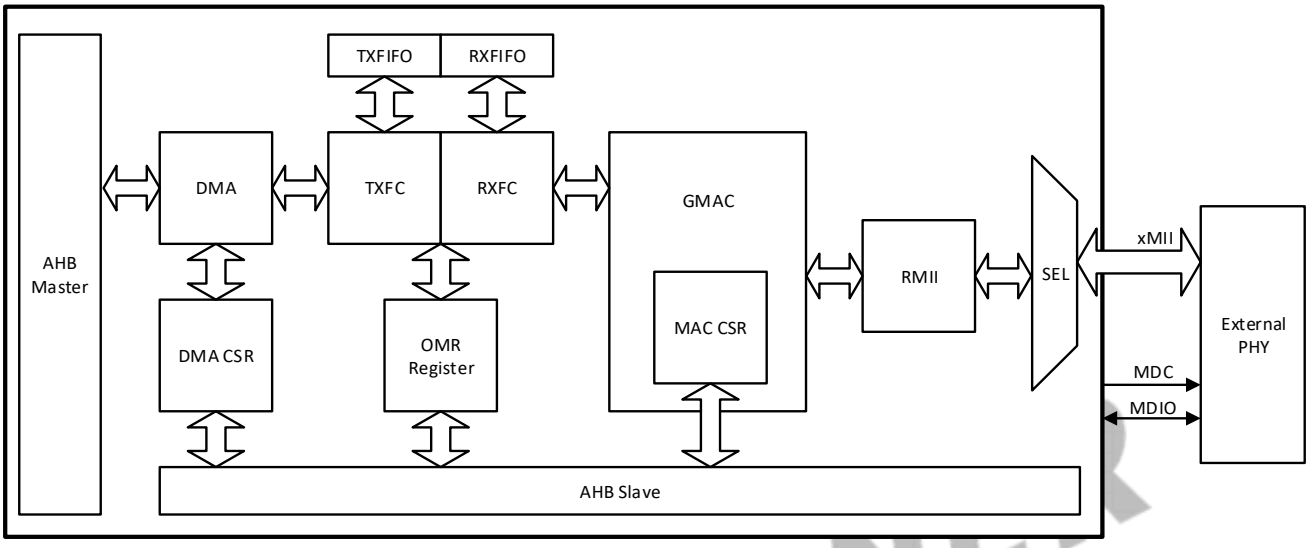
NOTE

V851SE is embedded with 100M EPHY and has no external pins for EMAC signals

9.2 Block Diagram

The EMAC block diagram is shown below.

Figure 9-1 EMAC Block Diagram



9.3 Functional Description

9.3.1 External Signals

The following table describes the external signals of EMAC for V851S.

Table 9-1 EMAC External Signals

Signal	Description	Type
RMII_RXD1	EMAC Receive Data	I
RMII_RXD0	EMAC Receive Data	I
RMII_CRS_DV	EMAC RMII Receive Data Valid	I
RMII_TXD1	EMAC Transmit Data	O
RMII_TXD0	EMAC Transmit Data	O
RMII_TXCK	EMAC Transmit Clock, 5MHz/50MHz input for RMII	I
RMII_TXEN	EMAC RMII Transmit Enable	O
RMII_RXER	EMAC RMII Receive Error	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O

The following table describes the pin list of internal Ethernet PHY for V851SE.

Table 9-2 Ethernet PHY Pin list

Pin Name	Description	Type
EPHY-RXN	EPHY Transceiver Negative Output/Input	AI/O
EPHY-RXP	EPHY Transceiver Positive Output/Input	AI/O
EPHY-GND	EPHY Ground	G
EPHY-TXN	EPHY Transceiver Negative Output/Input	AI/O
EPHY-TXP	EPHY Transceiver Positive Output/Input	AI/O
EPHY-RTX	EPHY External Resistance to Ground	AI
SPD-LED	EPHY Speed LED	O
LINK-LED	EPHY Link/Activity LED	O
VCC33-EPHY	3.3V EPHY Power Supply	P
VDD-EPHY	1.8V EPHY Power Supply	P

9.3.2 Clock Sources

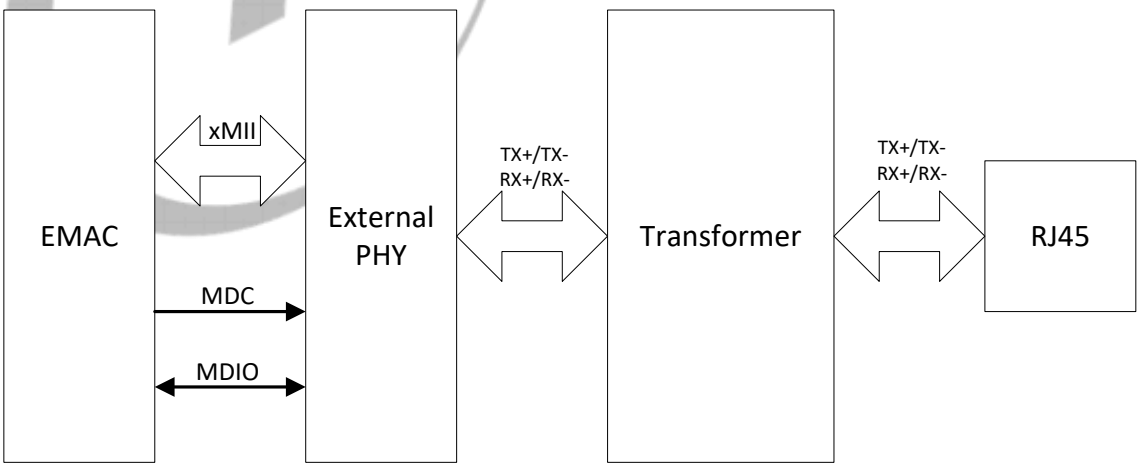
The following table describes the clock of EMAC.

Table 9-3 EMAC Clock Characteristics

Module Clock	Source	Description
EMAC_25M Clock	CCU	EMAC 25MHz clock source, refer to section 3.4 Clock Controller Unit (CCU) for detailed information.

9.3.3 Typical Application

Figure 9-2 EMAC Typical Application

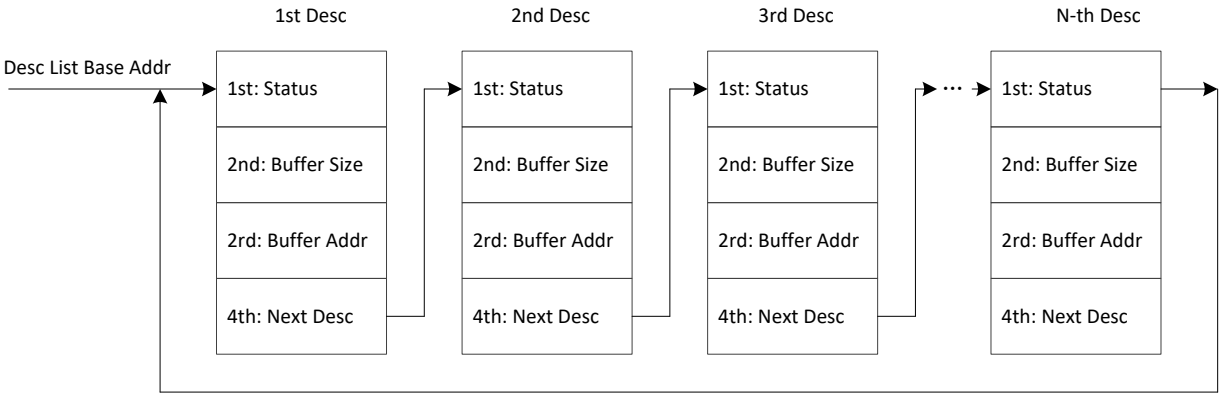


9.3.4 EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer

TX and RX frames. The following figure shows descriptor list structure. The address of each descriptor must be 32-bit aligned.

Figure 9-3 EMAC RX/TX Descriptor List



9.3.5 Transmit Descriptor

9.3.5.1 1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved.
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.

Bits	Description
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

9.3.5.2 2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

9.3.5.3 3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

9.3.5.4 4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

9.3.6 Receive Descriptor

9.3.6.1 1st Word of Receive Descriptor

Bits	Description
31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame don't pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame don't pass SA filter.
12	Reserved.
11	RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR When set, there is a late collision during reception in half-duplex mode.
5	Reserved.
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.
2	Reserved.
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

9.3.6.2 2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When set and a frame have been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

9.3.6.3 3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

9.3.6.4 4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

9.4 Register List

Module Name	Base Address	Comments
EMAC	0x04500000	EMAC Controller

Register Name	Offset	Description
EMAC		
EMAC_BASIC_CTL0	0x000	EMAC Basic Control Register0
EMAC_BASIC_CTL1	0x004	EMAC Basic Control Register1
EMAC_INT_STA	0x008	EMAC Interrupt Status Register
EMAC_INT_EN	0x00C	EMAC Interrupt Enable Register
EMAC_TX_CTL0	0x010	EMAC Transmit Control Register0
EMAC_TX_CTL1	0x014	EMAC Transmit Control Register1
EMAC_TX_FLOW_CTL	0x01C	EMAC Transmit Flow Control Register
EMAC_TX_DMA_DESC_LIST	0x020	EMAC Transmit DMA Descriptor List Address Register
EMAC_RX_CTL0	0x024	EMAC Receive Control Register0
EMAC_RX_CTL1	0x028	EMAC Receive Control Register1
EMAC_RX_DMA_DESC_LIST	0x034	EMAC Receive DMA Descriptor List Address Register

Register Name	Offset	Description
EMAC_RX_FRM_FLT	0x038	EMAC Receive Frame Filter Register
EMAC_RX_HASH0	0x040	EMAC Receive Hash Table Register0
EMAC_RX_HASH1	0x044	EMAC Receive Hash Table Register1
EMAC_MII_CMD	0x048	EMAC MII Command Register
EMAC_MII_DATA	0x04C	EMAC MII Data Register
EMAC_ADDR_HIGH0	0x050	EMAC MAC Address High Register0
EMAC_ADDR_LOW0	0x054	EMAC MAC Address Low Register0
EMAC_ADDR_HIGHN	0x050+0x8*N(N=1~7)	EMAC MAC Address High Register N
EMAC_ADDR_LOWN	0x054+0x8*N(N=1~7)	EMAC MAC Address Low Register N
EMAC_TX_DMA_STA	0x0B0	EMAC Transmit DMA Status Register
EMAC_TX_DMA_CUR_DESC	0x0B4	EMAC Transmit DMA Current Descriptor Register
EMAC_TX_DMA_CUR_BUF	0x0B8	EMAC Transmit DMA Current Buffer Address Register
EMAC_RX_DMA_STA	0x0C0	EMAC Receive DMA Status Register
EMAC_RX_DMA_CUR_DESC	0x0C4	EMAC Receive DMA Current Descriptor Register
EMAC_RX_DMA_CUR_BUF	0x0C8	EMAC Receive DMA Current Buffer Address Register

9.5 Register Description

9.5.1 0x0000 EMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMAC_BASIC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

9.5.2 0x0004 EMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: EMAC_BASIC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA priority 0: Same priority 1: RX priority over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset **Note: All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.**

9.5.3 0x0008 EMAC Interrupt Status Register (Default Value: 0x4000_0000)

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear .When this bit asserts, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserts, the RX DMA FSM is stopped.

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear .When this asserts, the RX DMA cannot acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when writing to DMA_RX_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear. When this bit asserts, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Frame Transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending Write '1' to clear.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this bit asserts, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to DMA_TX_START bit.

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear

9.5.4 0x000C EMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: EMAC_INT_EN
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/

Offset: 0x000C			Register Name: EMAC_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

9.5.5 0x0010 EMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: EMAC_TX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disable, transmit will continue until current transmit finish.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

9.5.6 0x0014 EMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	WAC	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission. 1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH The threshold value of TX DMA FIFO. When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/WAC	0x0	FLUSH_TX_FIFO This bit is set to flush the data in the TX FIFO, and cleared internally.

9.5.7 0x001C EMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

9.5.8 0x0020 EMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

9.5.9 0x0024 EMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

9.5.10 0x0028 EMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: EMAC_RX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	WAC	0x0	RX_DMA_START When set, the RX DMA will go to work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable,base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT

Offset: 0x0028			Register Name: EMAC_RX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 Only valid when RX_MD == 0, full frames with a length less than the threshold are transferred automatically.
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when receive descriptors/buffers is unavailable 1: Disable

9.5.11 0x0034 EMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: EMAC_RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

9.5.12 0x0038 EMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: EMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive All
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
7	/	/	/

Offset: 0x0038			Register Name: EMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass Frames whose SA field matches SA MAC address registers 1: Pass Frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it pass the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

9.5.13 0x0040 EMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: EMAC_RX_HASH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

9.5.14 0x0044 EMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: EMAC_RX_HASH1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

9.5.15 0x0048 EMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved MDC Clock is divided from AHB clock
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/WAC	0x0	MII_BUSY 0: Write no valid, read 0 indicate finish in read or write operation 1: Write start read or write operation and cleared internally, read 1 indicate busy.

9.5.16 0x004C EMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

9.5.17 0x0050 EMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: EMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16 bits of the 1st MAC address.

9.5.18 0x0054 EMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: EMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

9.5.19 0x0050+0x8*N (N=1~7) EMAC MAC Address High RegisterN (Default Value: 0x0000_FFFF)

Offset: 0x0050+0x8*N (N=1~7)			Register Name: EMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: used to compare with the destination address of the received frame 1: used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of in MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH The upper 16bits of the MAC address.

9.5.20 0x0054+0x8*N (N=1~7) EMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x8*N (N=1~7)			Register Name: EMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32bits of MAC address N (N: 1~7).

9.5.21 0x00B0 EMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	Read/Write	Default/Hex	Description
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, When reset or disable TX DMA 001: RUN_FETCH_DESC, Fetching TX DMA descriptor 010: RUN_WAIT_STA, Waiting for the status of TX frame 011: RUN_TRANS_DATA, Passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, Closing TX descriptor 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow

9.5.22 0x00B4 EMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: EMAC_TX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current transmit descriptor.

9.5.23 0x00B8 EMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: EMAC_TX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current transmit DMA buffer.

9.5.24 0x00C0 EMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: EMAC_RX_DMA_STA
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, When reset or disable RX DMA 001: RUN_FETCH_DESC, Fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, Waiting for frame. 100: SUSPEND, RX descriptor unavailable; 101: RUN_CLOSE_DESC, Closing RX descriptor. 110: Reserved 111: RUN_TRANS_DATA, Passing frame from host memory to RX DMA FIFO;

9.5.25 0x00C4 EMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: EMAC_RX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive descriptor

9.5.26 0x00C8 EMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: EMAC_RX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	The address of current receive DMA buffer

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10 Interfaces

10.1 The Two Wire Interface (TWI)

10.1.1 Overview

The Two Wire Interface (TWI) provides an interface between a CPU and any TWI-bus-compatible device that connects via the TWI bus. The TWI is designed to be compatible with the standard I2C bus protocol. The communication of the TWI is carried out by a byte-wise mode based on interrupt polled handshaking. Each device on the TWI bus is recognized by a unique address and can operate as either transmitter or receiver, a device connected to the TWI bus can be considered as master or slave when performing data transfers. Note that a master device is a device that initiates a data transfer on the bus and generates the clock signals to permit the transfer. During this transfer, any device addressed by this master is considered a slave.

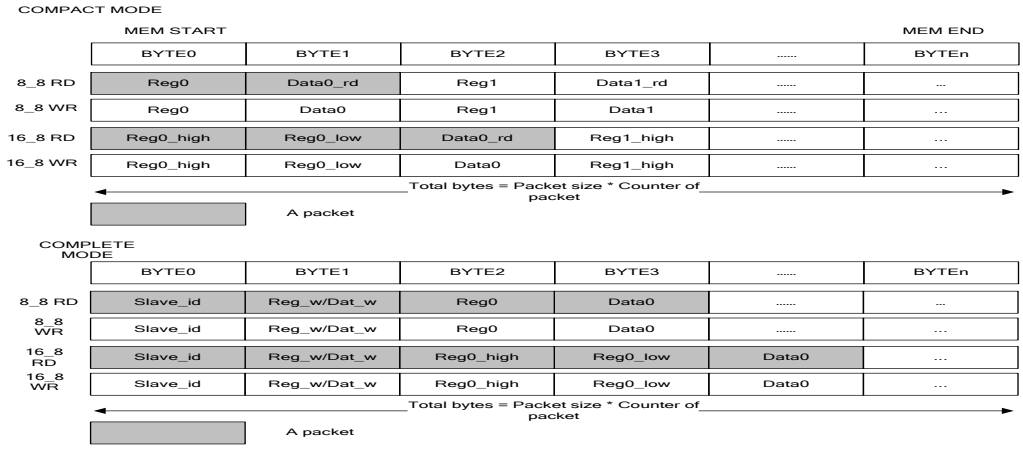
The TWI has the following features:

- Supports 5 TWIs
- Software programmability for slave or master
- Supports 7-bit and 10-bit device addressing modes
- Supports standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s)
- Master mode features:
  - Supports the bus arbitration in the case of multiple master devices
  - Supports clock synchronization and bit and byte waiting
  - Supports packet transmission and DMA
- Slave mode features:
  - Interrupt on address detection

10.1.2 Block Diagram

The following figure shows the block diagram of TWI.

Figure 10-1 TWI Block Diagram



TWI contains the following sub-blocks:

Table 10-1 TWI Sub-blocks

Term	Definition
RESET	Module reset signal
INT	Module output interrupt signal
CFG_REG	Module configuration register in TWI
PE	Packet encoding/decoding
CCU	Module clock controller unit

10.1.3 Functional Description

10.1.3.1 External Signals

The TWI controller has 5 TWI modules called TWI0, TWI1, TWI2, TWI3, and TWI4.The following table describes the external signals of the TWI. The TWIn-SCK and TWIn-SDA are bidirectional I/O, when the TWI is configured as a master device, the TWIn-SCK is an output pin; when the TWI is configurable as a slave device, the TWIn-SCK is an input pin. When using TWI, the corresponding PADs are selected as TWI function via section 10.6 GPIO.

Table 10-2 TWI External Signals

Signal	Description	Type
TWI0		
TWI0_SCK	TWI Clock Signal	I/O
TWI0_SDA	TWI Serial Data	I/O
TWI1		
TWI1_SCK	TWI Clock Signal	I/O
TWI1_SDA	TWI Serial Data	I/O

Signal	Description	Type
TWI2		
TWI2_SCK	TWI Clock Signal	I/O
TWI2_SDA	TWI Serial Data	I/O
TWI3		
TWI3_SCK	TWI Clock Signal	I/O
TWI3_SDA	TWI Serial Data	I/O
TWI4		
TWI4_SCK	TWI Clock Signal	I/O
TWI4_SDA	TWI Serial Data	I/O

10.1.3.2 Clock Sources

Each TWI controller has an input clock source. The following table describes the clock sources for TWI. After selecting a proper clock, users must open the gating of TWI and release the corresponding reset bit.

For more details on the clock setting, configuration, and gating information, see section 3.4 Clock Controller Unit (CCU).

Table 10-3 TWI Clock Sources

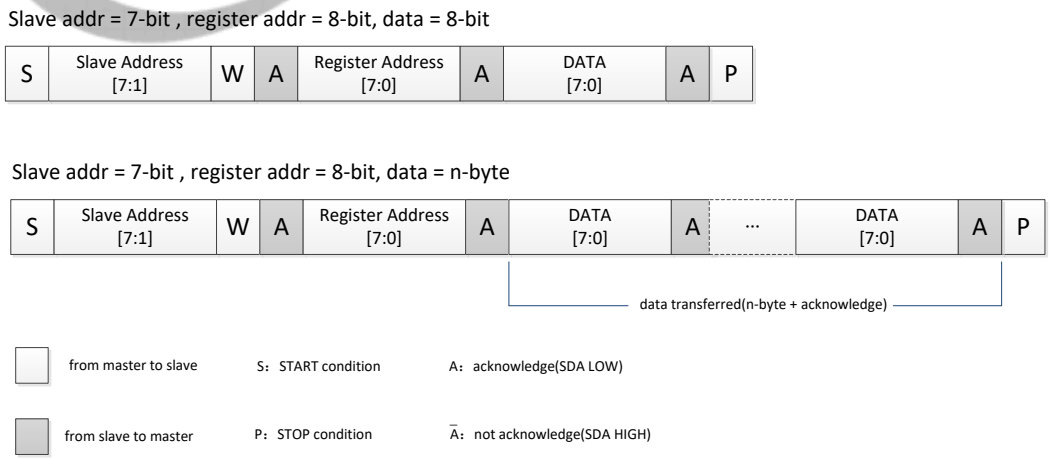
Clock Sources	Description
APB1 Bus	TWI clock source. Refer to section 3.4 Clock Controller Unit (CCU) for details on APB1.

10.1.3.3 Write/Read Timing in Standard and Extended Addressing Mode

This section is the 7-bit/10-bit addressing mode of the entire TWI protocol to read and write device registers. It can be achieved by directly using the TWI engine or using the TWI driver to control the TWI engine.

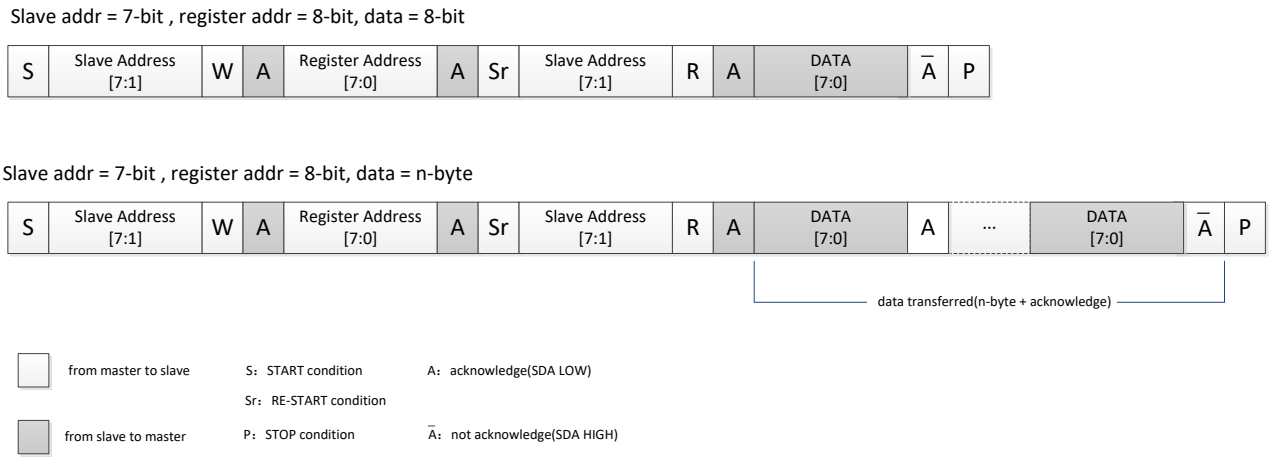
The following describes the write timing in 7-bit standard addressing mode.

Figure 10-2 Write Timing in 7-bit Standard Addressing Mode



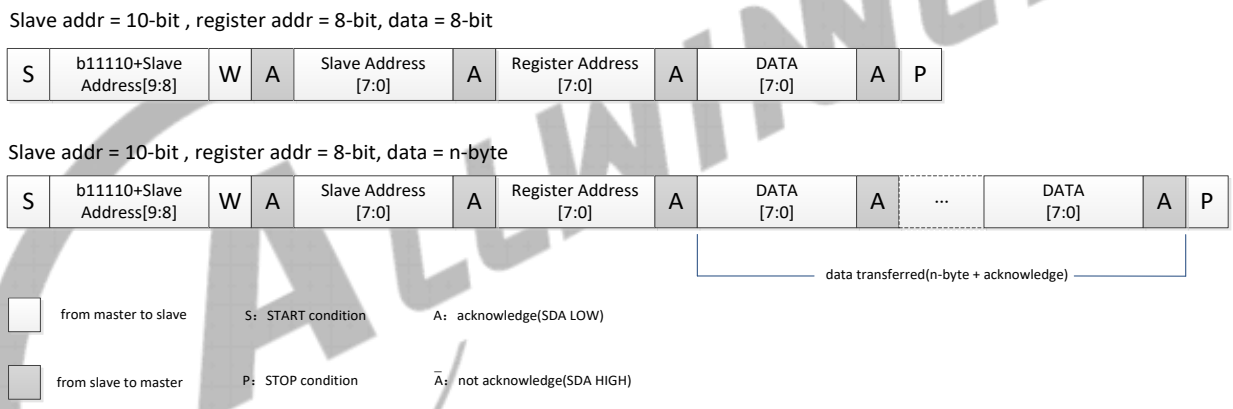
The following figure describes the read timing in 7-bit standard address mode.

Figure 10-3 Read Timing in 7-bit Standard Addressing Mode



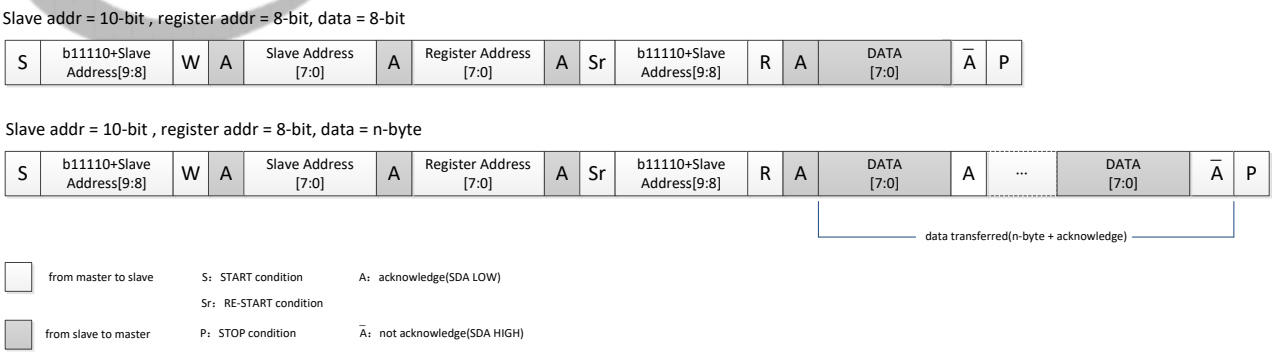
The following figure describes the write timing in 10-bit extended address mode.

Figure 10-4 Write Timing in 10-bit Extended Addressing Mode



The following figure describes the read timing in 10-bit extended address mode.

Figure 10-5 Read Timing in 10-bit Extended Addressing Mode



10.1.3.4 Write/Read Packet Transmission of TWI Driver

The TWI driver is only supported for master mode. When the TWI works in master mode, the TWI driver drives the TWI engine for one or more packet transmission instead of the CPU host. Packet transmission is defined in the following figures. The register address bytes and the written data bytes are buffered in SEND_FIFO, the read data bytes are buffered in RECV_FIFO.

Figure 10-6 TWI Driver Write Packet Transmission

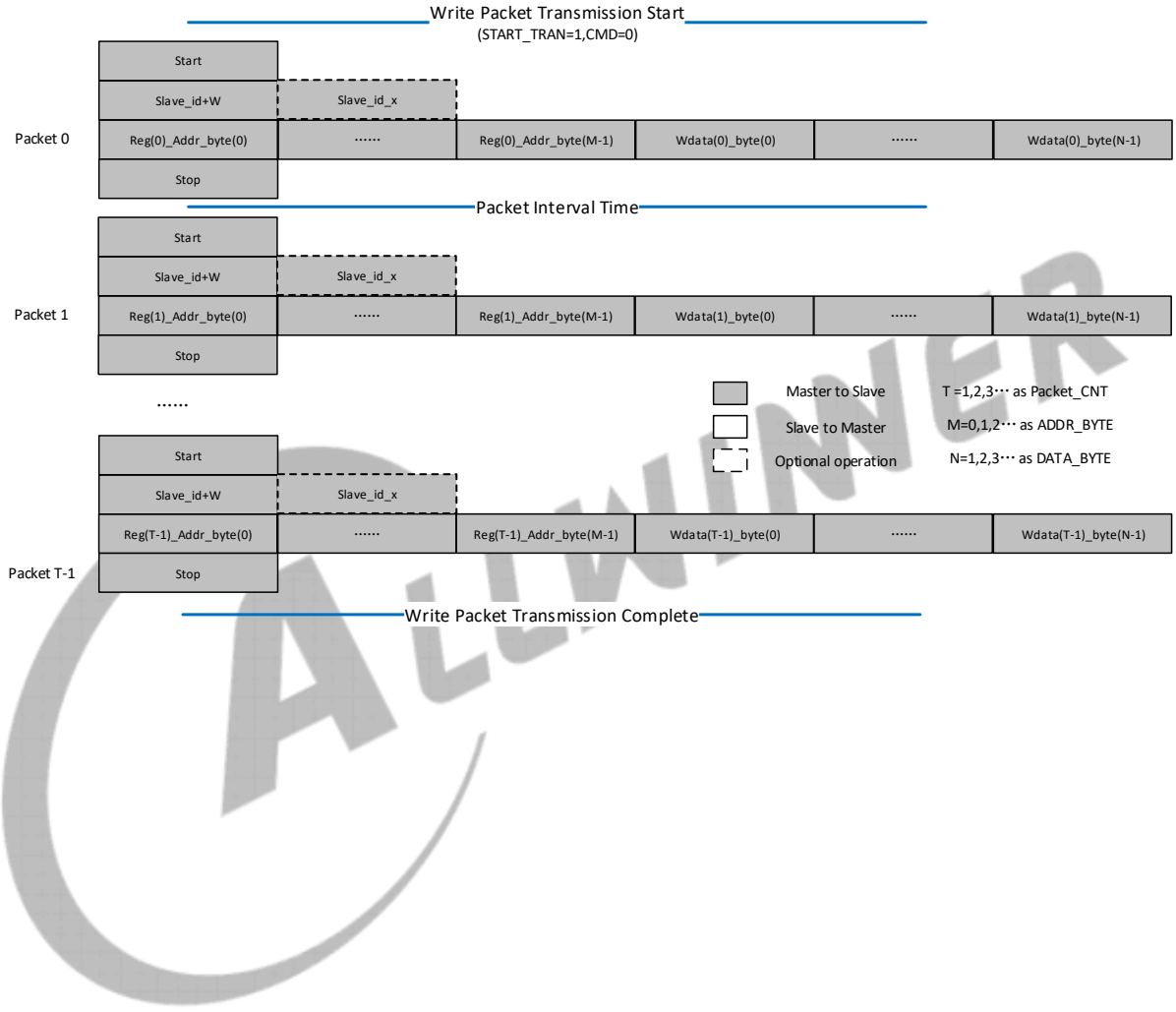
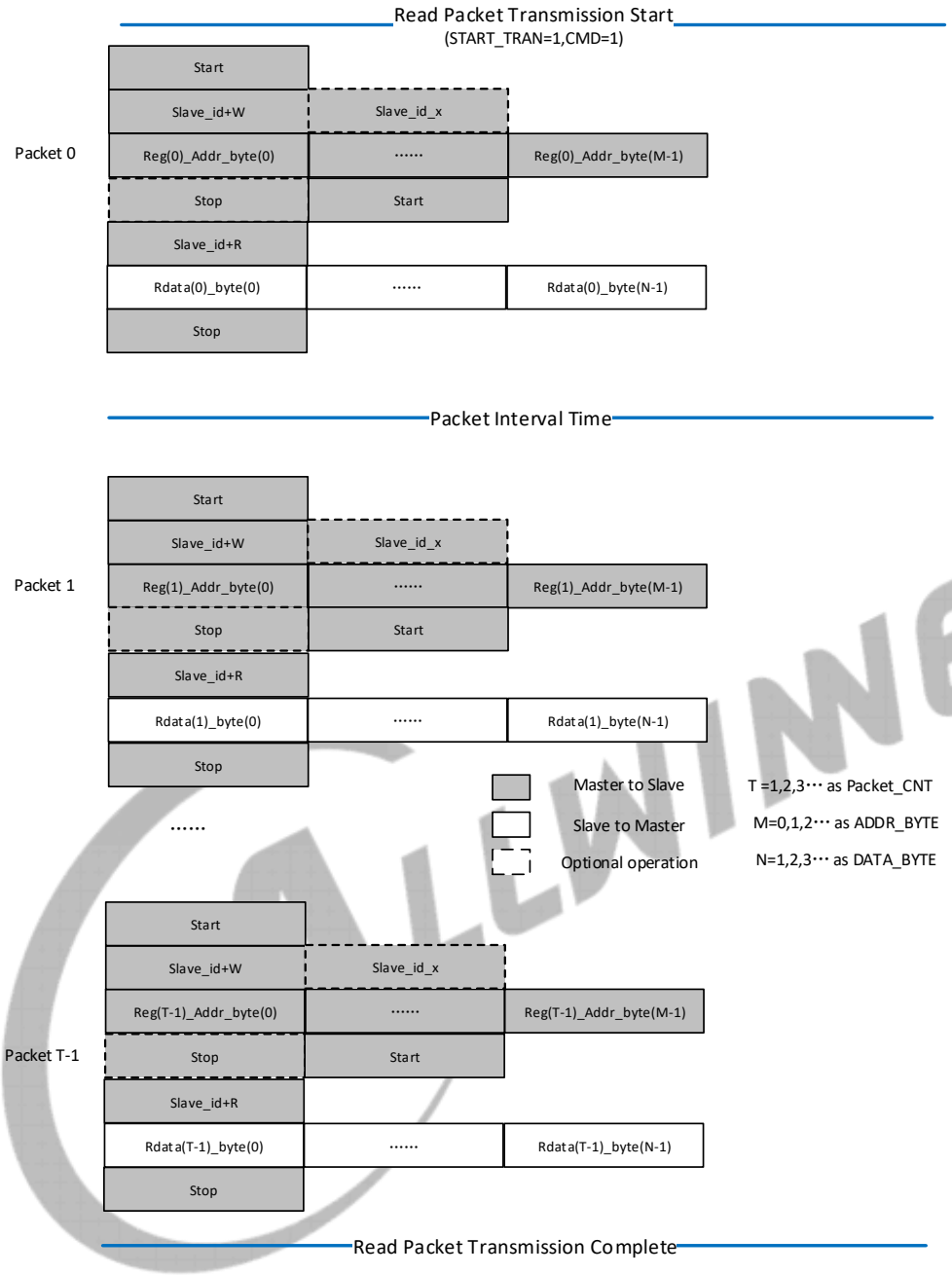


Figure 10-7 TWI Driver Read Packet Transmission



10.1.3.5 Master and Slave Mode of TWI Engine

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit, and Slave Receive. In general, CPU host controls TWI engine by writing commands and data to its registers. TWI engine transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the TWI_CNTR (Offset: 0x000C) to high (before it must be low). The TWI Engine will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each

interrupt, the micro-processor needs to check the TWI_STAT (Offset: 0x0010) for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI Engine also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write TWI_DATA (Offset: 0x0008) data register, and set the TWI_CNTR (Offset: 0x000C). After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

10.1.3.6 Generation of Repeated Start

After the data transfer, if the master still requires the bus, it can signal another Start followed by another slave address without signaling a Stop.

10.1.3.7 Programming State Diagram

The following figure shows the TWI programming state diagram. For the value between two states, see the TWI_STAT (Offset: 0x0010) register in section 10.1.6.5.

M_SEND_S: master sends START signal;

M_SEND_ADDR: master sends slave address;

M_SEND_XADD: master sends slave extended address;

M_SEND_SR: master repeated start;

M_SEND_DATA: master sends data;

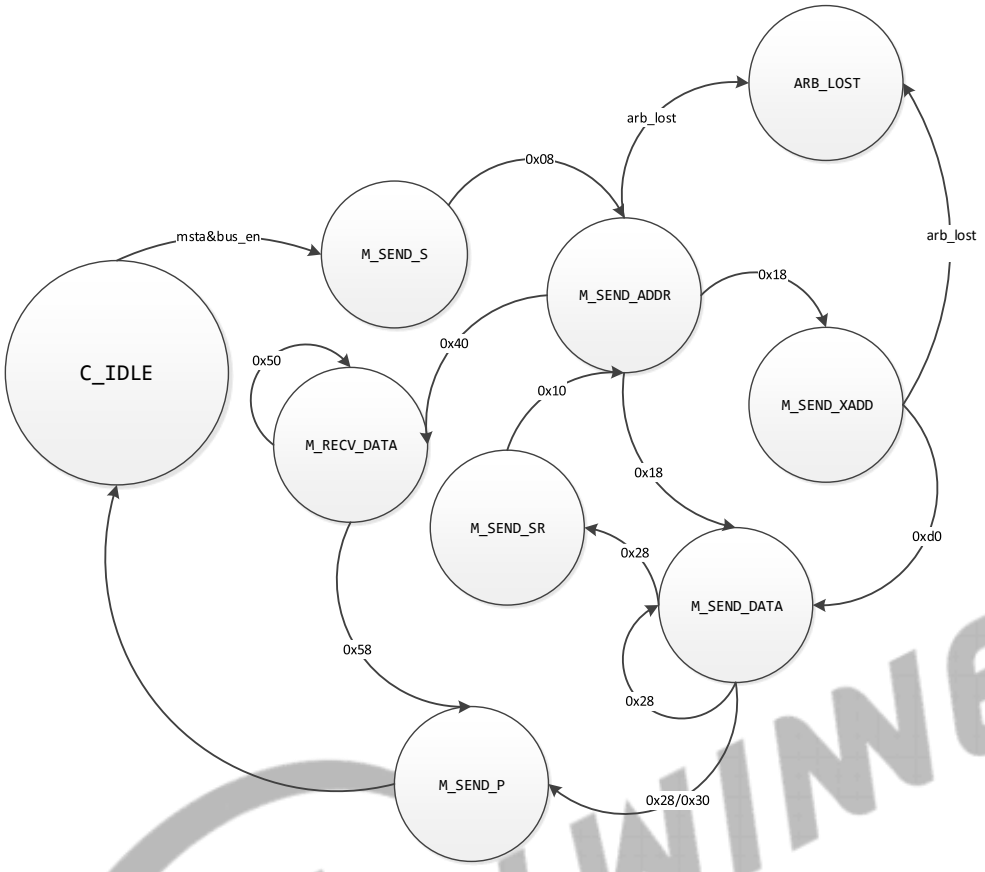
M_SEND_P: master sends STOP signal;

M_RECV_DATA: master receives data;

ARB_LOST: Arbitration lost;

C_IDLE: Idle.

Figure 10-8 TWI Programming State Diagram



10.1.4 Programming Guidelines

The TWI controller operates in an 8-bit data format. The data on the TWI_SDA line is always 8 bits long. At first, the TWI controller sends a start condition. When in the addressing formats of 7-bit, the TWI sends out an 8-bit message which includes 7 MSB slave address and 1 LSB read/write flag. The least significant of the salve address indicates the direction of transmission. When the TWI works in 10-bit slave address mode, the operation will be divided into two steps, for details on the operation, refer to register description in Section 10.1.6.1 and 10.1.6.2.

The following takes the TWI module in the CPUX domain as an example.

10.1.4.1 Initialization for TWI Engine

To initialize the TWI engine, perform the following steps:

1. Configure corresponding GPIO multiplex function as TWI mode.
2. For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 0 to close TWIn clock.
3. For TWIn, set TWI_BGR_REG[TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.
4. For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 1 to open TWIn clock.
5. Configure TWI_CCR[CLK_M] and TWI_CCR[CLK_N] to get the needed rate (The clock source of TWI is from APB1).

6. Configure TWI_CNTR[BUS_EN] and TWI_CNTR[A_ACK], when using interrupt mode, set TWI_CNTR[INT_EN] to 1, and register the system interrupt through PLIC module. In slave mode, configure TWI_ADDR and TWI_XADDR registers to finish TWI initialization configuration.

10.1.4.2 Writing Data Operation for TWI Engine

To write data to the device, perform the following steps:

1. Clear TWI_EFR register, and configure TWI_CNTR[M_STA] to 1 to transmit the START signal.
2. After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).
3. The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).
4. Interrupt is triggered after data address transmission completes, write data to be transmitted to TWI_DATA (For consecutive write data operation, every byte transmission completion triggers interrupt, during interrupt write the next byte data to TWI_DATA).
5. After transmission completes, write TWI_CNTR[M_STP] to 1 to transmit the STOP signal and end this write-operation.

10.1.4.3 Reading Data Operation for TWI Engine

To read data from the device, perform the following steps:

1. Clear TWI_EFR register, and set TWI_CNTR[A_ACK] to 1, and configure TWI_CNTR[M_STA] to 1 to transmit the START signal.
2. After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first-byte ID, secondly write the second-byte ID in the next interrupt).
3. The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).
4. The Interrupt is triggered after data address transmission completes, write TWI_CNTR[M_STA] to 1 to transmit new START signal, and after interrupt triggers, write device ID to TWI_DATA to start read-operation.
5. After device address transmission completes, each receive completion will trigger an interrupt, in turn, read TWI_DATA to get data, when receiving the previous interrupt of the last byte data, clear [A_ACK] to stop acknowledge signal of the last byte.
6. Write TWI_CNTR[M_STP] to 1 to transmit the STOP signal and end this read-operation.

10.1.4.4 Initialization for TWI Driver

To initialize the TWI driver, perform the following steps:

1. Configure corresponding GPIO multiplex function as TWI mode.
2. For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 0 to close TWIn clock.
3. For TWIn, set TWI_BGR_REG[TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.
4. For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 1 to open TWIn clock.
5. Set TWI_DRV_CTRL[TWI_DRV_EN] to 1 to enable the TWI driver.
6. Configure TWI_DRV_BUS_CTRL[CLK_M] and TWI_DRV_BUS_CTRL[CLK_N] to get the needed rate (The clock source of TWI is from APB1).
7. Set TWI_DRV_CTRL[RESTART_MODE] to 0 and [READ_TRAN_MODE] to 1, set TWI_DRV_INT_CTRL[TRAN_COM_INT_EN] to 1.
8. When using DMA for data transmission, set TWI_DRV_DMA_CFG[DMA_RX_EN] and TWI_DRV_DMA_CFG[DMA_TX_EN] to 1, and configure TWI_DRV_DMA_CFG[RX_TRIG] and TWI_DRV_DMA_CFG[TX_TRIG] to set the thresholds of RXFIFO and TXFIFO.

10.1.4.5 Writing Packet Transmission for TWI Driver

To write package to the device, perform the following steps:

1. Configure TWI_DRV_SLV[SLV_ID] to set the device ID, and configure TWI_DRV_SLV[CMD] to 0 to set the write operation.
2. Configure TWI_DRV_FMT[ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT[DATA_BYTE] according to the written data count in a packet.
3. Configure TWI_DRV_CFG[PACKET_CNT] to set the written packet number.
4. Configure DMA channel, including TWI TXFIFO, device register address, and the written data.
5. Set [START_TRAN] to 1 to start TWI Driver transmission.
6. When TWI driver transmission completes, the interrupt is triggered, it indicates that the write packet transmission ends.

10.1.4.6 Reading Packet Transmission for TWI Driver

To read package from the device, perform the following steps:

1. Configure TWI_DRV_SLV[SLV_ID] to set the device ID, and configure TWI_DRV_SLV[CMD] to 1 to set the read operation.
2. Configure TWI_DRV_FMT[ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT[DATA_BYTE] according to the read data count in a packet.
3. Configure TWI_DRV_CFG[PACKET_CNT] to set the read packet number.

4. Configure DMA channel, including TWI TXFIFO, TWI RXFIFO, device register address and the read data.
5. Set [START_TRAN] to 1 to start TWI Driver transmission.
6. When TWI driver transmission completes, the interrupt is triggered, it indicates that the read packet transmission ends.

10.1.5 Register List

Module Name	Base Address	Comments
TWI0	0x0250 2000	
TWI1	0x0250 2400	TWI1 register is the same with TWI0.
TWI2	0x0250_2800	TWI2 register is the same with TWI0.
TWI3	0x0250_2c00	TWI3 register is the same with TWI0.
TWI4	0x0250_3000	TWI4 register is the same with TWI0.

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address register
TWI_XADDR	0x0004	TWI Extend address register
TWI_DATA	0x0008	TWI Data register
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock register
TWI_SRST	0x0018	TWI Soft reset register
TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register
TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

10.1.6 Register Description

10.1.6.1 0x0000 TWI Slave Address Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address For 7-bit addressing, the bit[7:1] indicates: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 For 10-bit addressing, the bit[7:1] indicates: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with b'11110, the TWI recognizes b'11110 as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (For example, SLAX9 and SLAX8 for the extended address of the device), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

10.1.6.2 0x0004 TWI Extend Address Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

10.1.6.3 0x0008 TWI Data Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

10.1.6.4 0x000C TWI Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus SDA/SCL is ignored and the TWI controller will not respond to any address on the bus. 1: The TWI will respond to call to its slave address – and to the general call address if the GCE bit in the ADDR register is set. **Note: In master operation mode, this bit should be set to '1'.**
5	R/WAC	0x0	M_STA Master Mode Start When the M_STA is set to '1', the TWI controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W1C	0x0	M_STP Master Mode Stop If the M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode), then transmit the START condition. The M_STP bit is cleared automatically. Writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag The INT_FLAG is automatically set to '1' when any of the 28 (out of the possible 29) states is entered (see 'STAT Register' below). The state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when INT_FLAG is set to '1'. If the TWI is operating in slave mode, the data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the GCE bit in the ADDR register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1	/	/	/
0	R/W	0x0	CLK_COUNT_MODE 0: scl clock high period count on oscl 1: scl clock high period count on iscl

10.1.6.5 0x0010 TWI Status Register (Default Value: 0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Offset: 0x0010			Register Name: TWI_STAT
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0xF8	STA Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in the address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in the address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in the address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: The Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

10.1.6.6 0x0014 TWI Clock Register (Default Value: 0x0000_0080)

Offset: 0x0014			Register Name: TWI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x1	CLK_DUTY Setting duty cycle of clock as master 0: 50% 1: 40%
6:3	R/W	0x0	CLK_M The TWI SCL output frequency, in master mode, is F1/10: F1 = F0/(CLK_M + 1) Fscl = F1/10 = Fin/(2^CLK_N * (CLK_M + 1)*10) Specially, Fscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin/2^CLK_N The TWI SCL output frequency, in master mode, is F1/10: F1 = F0/(CLK_M + 1) Fscl = F1/10 = Fin/(2^CLK_N * (CLK_M + 1)*10) Specially, Fscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce. For Example: Fin = 24 MHz (APB clock input) For 400 kHz full speed 2-wire, CLK_N = 1, CLK_M = 2 F0 = 24 MHz/2^1 = 12 MHz, F1 = F0/(10*(2+1)) = 0.4 MHz For 100 kHz standard speed 2-wire, CLK_N = 1, CLK_M = 11 F0 = 24 MHz/2^1 = 12 MHz, F1 = F0/(10*(11+1)) = 0.1 MHz

10.1.6.7 0x0018 TWI Soft Reset Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

10.1.6.8 0x001C TWI Enhance Feature Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00: No data byte can be written after the read command 01: Only 1-byte data can be written after the read command 10: 2-bytes data can be written after the read command 11: 3-bytes data can be written after the read command

10.1.6.9 0x0020 TWI Line Control Register (Default Value: 0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When the line control mode is enabled (bit[2] is set), this bit decides the output level of TWI_SCL. 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When the line control mode is enabled (bit[0] is set), this bit decides the output level of TWI_SDA. 0: Output low level 1: Output high level

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

10.1.6.10 0x0200 TWI_DRV Control Register (Default Value: 0x00F8_1000)

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	START_TRAN Start transmission 0: Transmission idle 1: Start transmission Automatically cleared to '0' when finished. If the slave is not responding for the expected status over the time defined by TIMEOUT, the current transmission will stop. All setting formats and data will be loaded from registers and FIFO when the transmission starts.
30	/	/	/
29	R/W	0x0	RESTART_MODE Restart mode 0: RESTART 1: STOP+START Define the TWI_DRV action after sending the register address.
28	R/W	0x0	READ_TRAN_MODE Read transition mode 0: Send slave_id+W 1: Not send slave_id+W Setting this bit to 1 if reading from a slave in which the register width is equal to 0.
27:24	R	0x0	TRAN_RESULT Transition result 000: OK 001: FAIL Other: Reserved

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
23:16	R	0xf8	TWI_STA TWI status 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending the 9th SCL clock Other: Reserved
15:8	R/W	0x10	TIMEOUT_N Timeout number When sending the 9th clock, assert fail signal when the slave device does not respond after N*FSCL cycles. And the software must do a reset to the TWI_DRV module and send a stop condition to slave.
7:2	/	/	/
1	R/W	0x0	SOFT_RESET Software reset 0: Normal 1: Reset
0	R/W	0x0	TWI_DRV_EN TWI driver enable 0: Module disable 1: Module enable (only use in TWI Master Mode)

10.1.6.11 0x0204 TWI_DRV Transmission Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0204			Register Name: TWI_DRV_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL FSCL cycles.
15:0	R/W	0x1	PACKET_CNT The FIFO data is transmitted as PACKET_CNT packets in current format.

10.1.6.12 0x0208 TWI_DRV Slave ID Register (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID For 7-bit addressing, the bit[7:1] indicates: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 For 10-bit addressing, the bit[7:1] indicates: 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD R/W operation to slave device 0: Write 1: Read
7:0	R/W	0x0	SLV_ID_X SLAX[7:0] The low 8 bits for slave device ID with 10-bit addressing.

10.1.6.13 0x020C TWI_DRV Packet Format Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE How many bytes be sent as slave device reg address 0~255
15:0	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~65535

10.1.6.14 0x0210 TWI_DRV Bus Control Register (Default Value: 0x0000_80C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
15	R/W	0x1	CLK_DUTY Setting duty cycle of clock as Master 0: 50% 1: 40%
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL frequency is FSCL=F1/10=(F0/(CLK_M+1))/10 Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output enable
0	R/W	0x0	SDA_MOE SDA manual output enable

10.1.6.15 0x0214 TWI_DRV Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
19	R/W	0x0	RX_REQ_INT_EN If set, an interrupt is sent when RX_REQ_PD sets.
18	R/W	0x0	TX_REQ_INT_EN If set, an interrupt is sent when TX_REQ_PD sets.
17	R/W	0x0	TRAN_ERR_INT_EN If set, an interrupt is sent when TRAN_ERR_PD sets.
16	R/W	0x0	TRAN_COM_INT_EN If set, an interrupt is sent when TRAN_COM_PD sets.
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG.

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO.
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failure pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completion pending

10.1.6.16 0x0218 TWI_DRV DMA Configure Register (Default Value: 0x0010_0010)

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DMA_RX_EN DMA RX Enable
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG RX trigger When DMA_RX_EN is set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG, or the read transmission is completed, the data of RECV_FIFO does not reach RX_TRIG but as long as the RECV_FIFO is not empty.
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN DMA TX Enable
7:6	/	/	/
5:0	R/W	0x10	TX_TRIG TX trigger When DMA_TX_EN is set, send DMA TX Req when the space of SEND_FIFO (FIFO Level – data volume) reaches TX_TRIG.

10.1.6.17 0x021C TWI_DRV FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV_FIFO pointer, and this bit is cleared automatically.
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV_FIFO

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer, and this bit is cleared automatically.
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

10.1.6.18 0x0300 TWI_DRV Send Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TWI_DRV_SEND_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Address of a 32x8 SEND_FIFO, which stores reg address and data sending to the slave device.

10.1.6.19 0x0304 TWI_DRV Receive Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RECV_DATA_FIFO Address of a 32x8 RECV_FIFO, which stores data received from the slave device.

10.2 UART

10.2.1 Overview

The universal asynchronous receiver transmitter (UART) provides an asynchronous serial communication with external devices, modem (data carrier equipment, DCE). It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals.

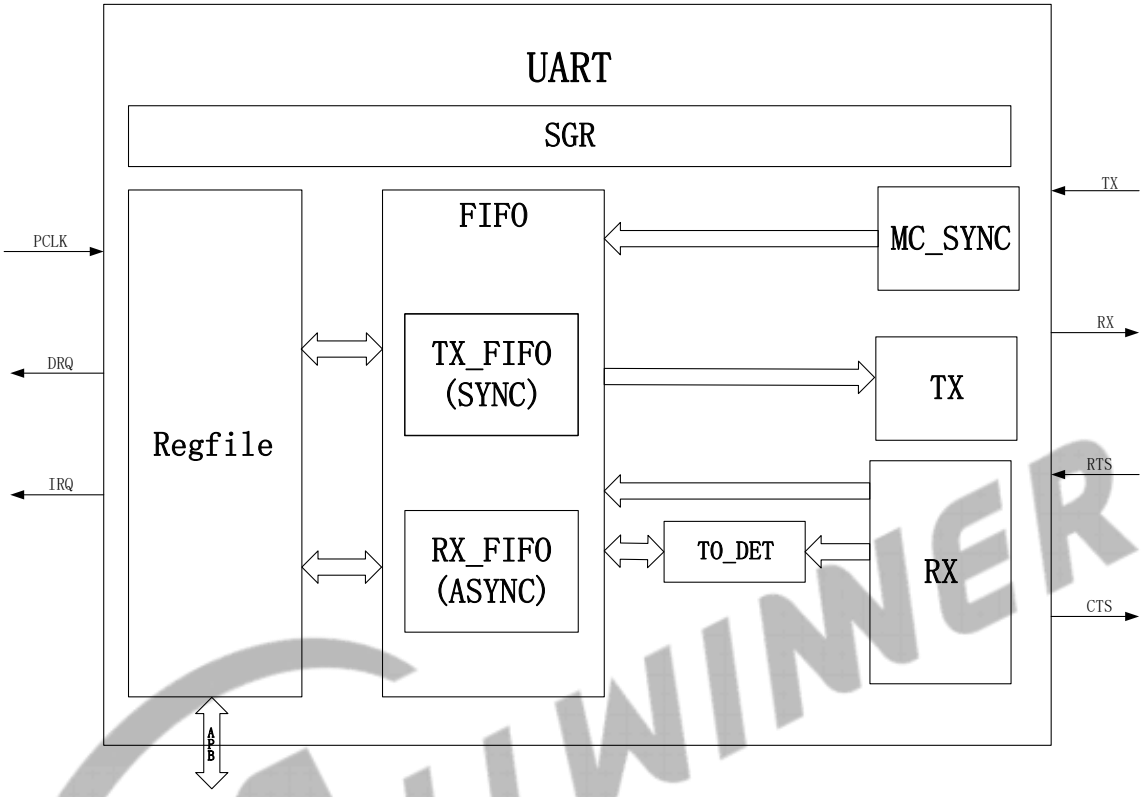
The UART has the following features:

- Compatible with industry-standard 16450/16550 UARTs
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes (for UART0)
  - Each of them is 128 bytes (for UART1, UART2, and UART3)
- The working reference clock is from the APB bus clock
  - Speed up to 4 Mbit/s with 64 MHz APB clock
  - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- Supports programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports auto-flow by using CTS & RTS (Only for UART1/2/3)
- Support IrDA 1.0 SIR
- Support RS-485/8-bit mode
- Supports 5-8 data bits and 1/1.5/2 stop bits

10.2.2 Block Diagram

The following figure shows a block diagram of the UART.

Figure 10-9 UART Block Diagram



10.2.3 Functional Description

10.2.3.1 External Signals

The following table describes the external signals of UART.

Table 10-4 UART External Signals

Signal	Description	Type
UART0		
UART0_TX	Serial Data Output	O
UART0_RX	Serial Data Input	I
UART1		
UART1_TX	Serial Data Output	O
UART1_RX	Serial Data Input	I
UART2		
UART2_TX	Serial Data Output	O
UART2_RX	Serial Data Input	I
UART2_CTS	Clear to Send	I
UART2_RTS	Request to Send	O

Signal	Description	Type
UART3		
UART3_TX	Serial Data Output	O
UART3_RX	Serial Data Input	I
UART3_CTS	Clear to Send	I
UART3_RTS	Request to Send	O

10.2.3.2 Clock Sources

The following table describes the clock sources of UART.

Table 10-5 UART Clock Sources

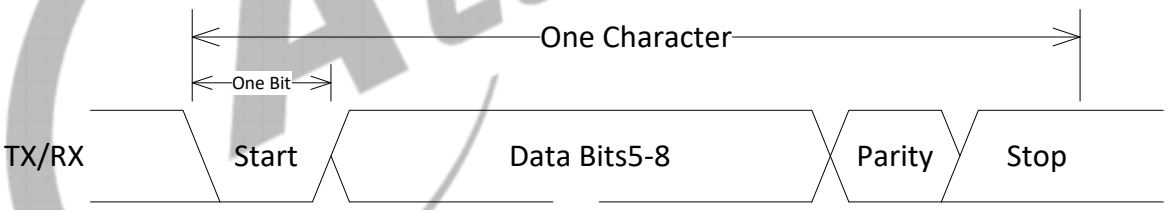
Clock Sources	Description
APB1 Bus	UART clock source. Refer to section 3.4 Clock Controller Unit (CCU) for details on APB1.

10.2.3.3 Typical Applications and Timing Diagram

UART Serial Data Format

The following figure shows the UART serial data format. The start bit, data bit, parity bit, and stop bit can be configured.

Figure 10-10 UART Serial Data Format



Using UART for RTS/CTS Autoflow Control

The following figure shows the typical application diagram for RTS/CTS autoflow control. Figure 9-12 shows the data format of the RTS/CTS autoflow control.

Figure 10-11 Application Diagram for RTS/CTS Autoflow Control

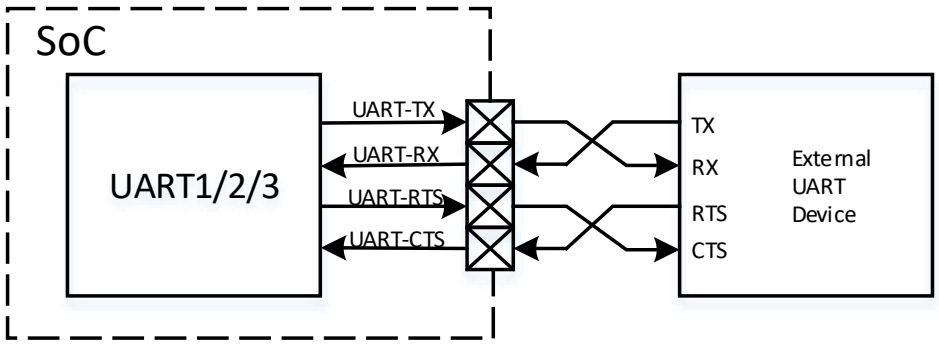
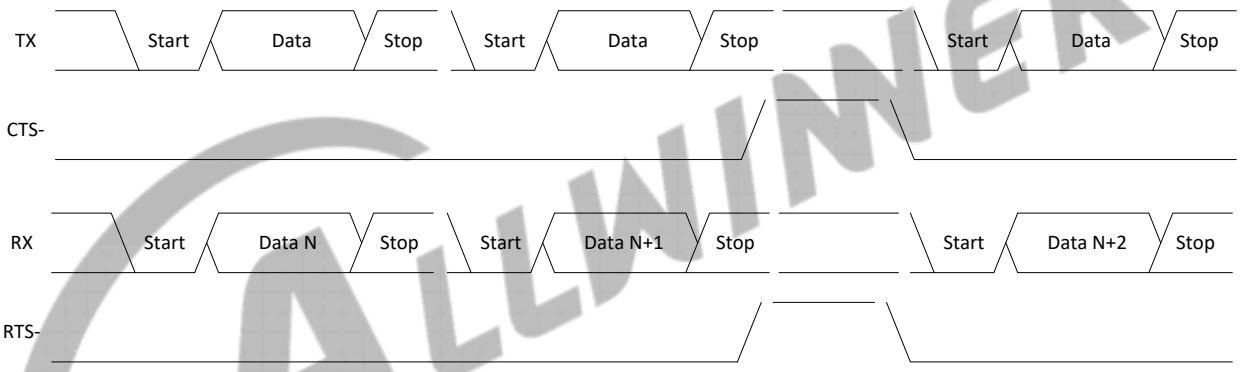


Figure 10-12 RTS/CTS Autoflow Control Data Format



Using UART for Serial IrDA

The following figure shows the application diagram for the IrDA transceiver. Figure 9-14 shows the data format of the serial IrDA.

Figure 10-13 Application Diagram for IrDA Transceiver

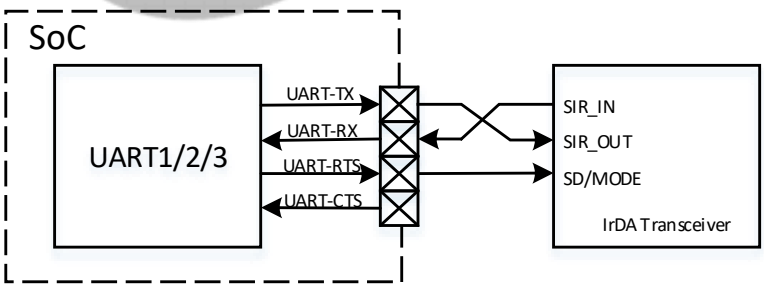
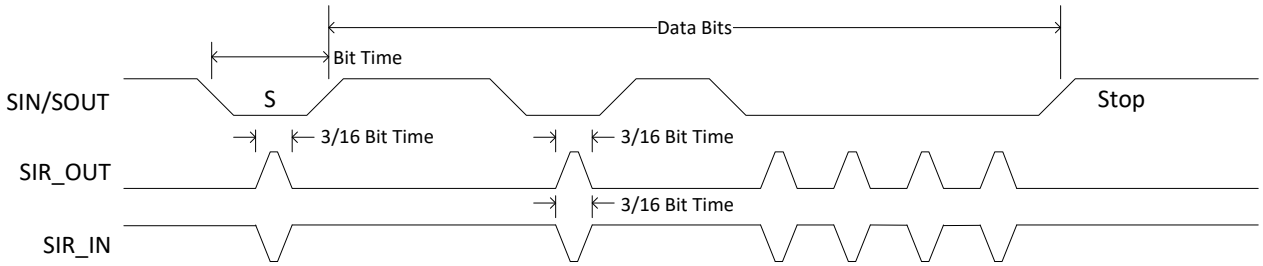


Figure 10-14 Serial IrDA Data Format



Using UART for RS-485

The following figure shows the application diagram for the RS-485 transceiver. Figure 9-16 shows the data format of the RS-485.

Figure 10-15 Application Diagram for RS-485 Transceiver

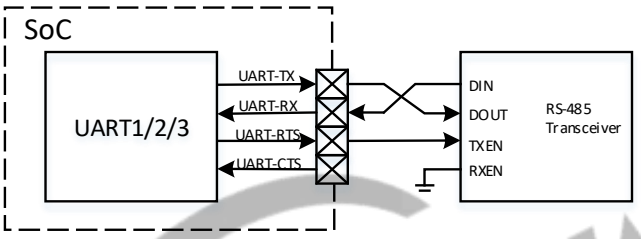
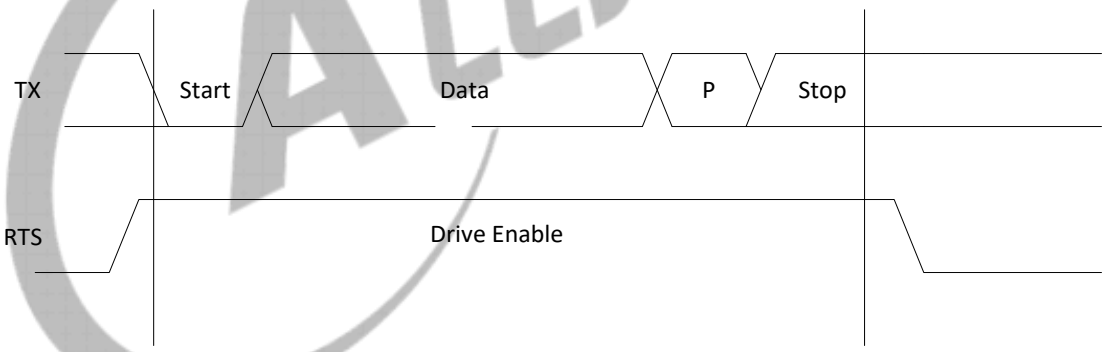


Figure 10-16 RS-485 Data Format



10.2.3.4 UART Operating Mode

Data Frame Format

The UART_LCR (Offset: 0x000C) register can set the basic parameter of a data frame: data width (5 to 8 bits), stop bit number (1/1.5/2), parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit, and stop signal. The LSB is transmitted first.

- Start signal (start bit): It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART transmits data, the level needs to hold high.
- Data signal (data bit): The data bit width can be configured as 5-bit, 6-bit, 7-bit, and 8-bit through different applications.
- Parity bit: It is a 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the UART_LCR (Offset: 0x000C) register.
- Stop Signal (stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit, 1.5-bit, and 2-bit by the UART_LCR (Offset: 0x000C) register. The high level of the TXD signal indicates the end of a data frame.

Baud and Error Rates

The baud rate is calculated as follows: Baud rate = SCLK/(16 * divisor).

The SCLK is usually APB2 or APS2 and can be set in section 3.4 Clock Controller Unit (CCU)

10.2.4 Programming Guidelines

The following takes the UART module in the CPUX domain as an example.

10.2.4.1 Initialization

1. System Initialization
   - Configure APB1_CFG_REG (Offset: 0x0524) in the CCU module to set the APB1 bus clock (The clock is 24MHz by default).
   - Set UART_BGR_REG (Offset: 0x090C)[UARTx_GATING] to 1 to enable the module clock, and set UART_BGR_REG (Offset: 0x090C) [UARTx_RST] to 1 to de-assert the module.
2. UART Controller Initialization
   - IO configuration: Configure GPIO multiplex as UART function, and set UART pins to internal pull-up mode (For detail, see the description in section 10.6 GPIO).
   - Baud-rate configuration:
     - Set UART baud-rate (refer to section 10.2.3.4 UART Operating Mode);
     - Write UART_FCR (Offset: 0x0008) [FIFOE] to 1 to enable TX/RX FIFO;
     - Write UART_HALT (Offset: 0x00A4) [HALT_TX] to 1 to disable TX transfer;
     - Set UART_LCR (Offset: 0x000C) [DLAB] to 1, remain default configuration for other bits; set 0x00 offset address to the UART_DLL (Offset: 0x0000) register, set 0x04 offset address to the UART_DLH (Offset: 0x0004) register;

- Write the high 8-bit of divisor to the UART_DLH (Offset: 0x0004) register, and write the low 8-bit of divisor to the UART_DLL (Offset: 0x0000) register;
- Set UART_LCR (Offset: 0x000C) [DLAB] to 0, remain default configuration for other bits; set 0x00 offset address to the UART_RBR (Offset: 0x0000)/UART_THR (Offset: 0x0000) register, set 0x04 offset address to the UART_IER (Offset: 0x0004) register;
- Set UART_HALT (0x00A4) [HALT_TX] to 0 to enable TX transfer.

3. Controller Parameter Configuration
   - Set data width, stop bits, and even/odd parity type by writing the UART_LCR (Offset: 0x000C) register.
   - Reset, enable FIFO and set FIFO trigger condition by writing the UART_FCR (Offset: 0x0008) register.
   - Set the flow control parameter by writing the UART_MCR (Offset: 0x0010) register.
4. Interrupt Configuration
   - Configure UART interrupt vector number to request UART interrupt.
   - In DMA mode, write UART_IER (Offset: 0x0004) to 0 to disable interrupt; write UART_HSK (Offset: 0x0088) [Handshake configuration] to 0xE5 to set DMA handshake mode; write UART_FCR (Offset: 0x0008) [DMAM] to 1 to set DMA transmission/reception mode; set DMA parameter and request DMA interrupt according to DMA configuration process.
   - In Interrupt mode, configure UART_IER (Offset: 0x0004) to enable the corresponding interrupt according to requirements: such as transmit (TX) interrupt, receive (RX) interrupt, receive line status interrupt, RS48 interrupt, etc. (Here TX/RX interrupt is usually used).

10.2.4.2 Transferring/Receiving Data in Query Mode

Data transfer

1. Write data to UART_THR (Offset: 0x0000) to start data transfer.
2. Check TX_FIFO status by reading UART_USR (Offset: 0x007C) [TFNF]. If the bit is 1, data can continue to be written; if the bit is 0, wait for data transfer, and data cannot continue to write until FIFO is not full.

Data receive

1. Check RX_FIFO status by reading UART_USR (Offset: 0x007C) [RFNE].
2. Read data from UART_RBR (Offset: 0x0000) if RX_FIFO is not empty.
3. If UART_USR (Offset: 0x007C) [RFNE] is 0, data is received completely.

10.2.4.3 Transferring/Receiving Data in Interrupt Mode

Data transfer

1. Set UART_IER (Offset: 0x0004) [ETBEI] to 1 to enable the UART transmission interrupt.

2. Write the data to be transmitted to UART_THR (Offset: 0x0000).
3. When the data of TX_FIFO meets trigger condition (such as FIFO/2, FIFO/4), the UART transfer interrupt is generated.
4. Check UART_USR (Offset: 0x007C) [TFE] and determine whether TX_FIFO is empty. If UART_USR (Offset: 0x007C) [TFE] is 1, it indicates that the data in TX_FIFO is transmitted completely.
5. Clear UART_IER (Offset: 0x0004) [ETBEI] to 0 to disable transfer interrupt.

Data receive

1. Set UART_IER (Offset: 0x0004) [ERBFI] to 1 to enable the UART reception interrupt.
2. When the received data from RX_FIFO meets trigger condition (such as FIFO/2, FIFO/4), the UART receive interrupt is generated.
3. Read data from UART_RBR (Offset: 0x0000).
4. Check RX_FIFO status by reading UART_USR (Offset: 0x007C) [RFNE] and determine whether to read data. If the bit is 1, continue to read data from UART_RBR (Offset: 0x0000) until UART_USR (Offset: 0x007C) [RFNE] is cleared to 0, which indicates data is received completely.

10.2.4.4 Transferring/Receiving Data in DMA Mode

Data transfer

1. Configure the UART DMA interrupt according to the initialization process.
2. Configure DMA data channel, including the transfer source address, the transfer destination address, the number of data to be transferred, and the transfer type, and so on. (For details, see section 3.10 Direct Memory Access Controller (DMAC)).
3. Enable the DMA transfer function of the UART by setting the register of the DMA module.
4. Determine whether UART data is transferred completely based on the DMA status. If all data is transferred completely, disable the DMA transfer function of the UART.

Data receive

1. Configure DMA data channel, including the transfer source address, the transfer destination address, the number of data to be transferred, and the transfer type, and so on. (For details, see section 3.10 Direct Memory Access Controller (DMAC)).
2. Enable the DMA receive function of the UART by setting the register of the DMA module.
3. Determine whether UART data is received completely based on the DMA status. If all data is received completely, disable the DMA receive function of the UART.

10.2.5 Register List

Module Name	Base Address
UART0	0x02500000

Module Name	Base Address
UART1	0x02500400
UART2	0x02500800
UART3	0x02500C00

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_DMA_REQ_EN	0x008C	UART DMA Request Enable Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_FCC	0x00F0	UART FIFO Clock Control Register

10.2.6 Register Description

10.2.6.1 0x0000 UART Receiver Buffer Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in UART_LCR is set. If in FIFO mode and FIFOs are enabled (The UART_FCR[0] is set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register can not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data are lost and an overrun error occurs.

10.2.6.2 0x0000 UART Transmit Holding Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data is transmitted on the serial output port (SOUT) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the UART_THR when the THRE bit (UART_LSR[5]) is set. If in FIFO mode and FIFOs are enabled (UART_FCR[0] = 1) and THRE is set, the 16 number of characters data may be written to the UART_THR before the FIFO is full. When the FIFO is full, any written data results in the written data being lost.

10.2.6.3 0x0000 UART Divisor Latch Low Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (UART_LCR[7]) is set and the UART is not busy (UART_USR[0] is 0). The output baud rate is equal to the serial clock (SCLK) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq)/(16 * divisor). Note that when the Divisor Latch Registers (UART_DLL and UART_DLH) are set to 0, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

10.2.6.4 0x0004 UART Divisor Latch High Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (UART_LCR[7]) is set and the UART is not busy (UART_USR[0] is 0). The output baud rate is equal to the serial clock (SCLK) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq)/(16 * divisor). Note that when the Divisor Latch Registers (UART_DLL and UART_DLH) is set to 0, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

10.2.6.5 0x0004 UART Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Offset: 0x0004			Register Name: UART_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third-highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second-highest priority interrupt. 0: Disable 1: Enable

10.2.6.6 0x0008 UART Interrupt Identity Register (Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types. 0000: modem status 0001: no interrupt pending 0010: THR empty 0011: RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout The bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE mode disabled) or XMIT FIFO at or below threshold (Program THRE mode enabled)	Reading the IIR register (if the source of interrupt); or, writing into THR (FIFOs or THRE mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if the autoflow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

10.2.6.7 0x0008 UART FIFO Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO when the Received Data Available Interrupt is generated. In the autoflow control mode, it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full

Offset: 0x0008			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
5:4	W	0x0	TFT TX Empty Trigger This is used to select the empty threshold level when the THRE Interrupts are generated and the mode is active. It also determines when the dma_tx_req_n signal is asserted in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, when the PTE in UART_HALT is high and TX FIFO is enabled, the TX DMA request will be set when the TFL in UART_TFL is less than or equal to FIFO Trigger Level (otherwise it will be cleared). When the PTE is high and TX FIFO is disabled, the TX DMA request will be set only if the THR in UART_THR is empty. If the PTE is low, the TX DMA request will be set only if the TX FIFO (TX FIFO enabled) or THR (TX FIFO disabled) is empty. When the DMA_PTE_RX in UART_HALT is high and RX FIFO is enabled, the RX DRQ will be set only if the RFL in UART_RFL is equal to or more than FIFO Trigger Level, otherwise, it will be cleared. 1: Mode 1 In this mode, TX FIFO should be enabled. If the PTE in UART_HALT is high, the TX DMA request will be set when the TFL in UART_TFL is less than or equal to FIFO Trigger Level; If the PTE is low, the TX DMA request will be set when TX FIFO is empty. Once the request is set, it is cleared only when TX FIFO is full. If the RFL in UART_RFL is equal to or more than FIFO Trigger Level or there is a character timeout, the RX DRQ will be set; Once the RX DRQ is set, it is cleared only when RX FIFO (RX FIFO enabled) or RBR (RX FIFO disabled) is empty.
2	W	0x0	XFIFOR XMIT FIFO Reset The bit resets the control part of the transfer FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-cleared'. It is not necessary to clear this bit.

Offset: 0x0008			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
1	W	0x0	RFIFOR RCVR FIFO Reset The bit resets the control part of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-cleared'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs The bit enables/disables the transmitting (XMIT) and receiving (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller part of FIFOs is reset.

10.2.6.8 0x000C UART Line Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writable only when UART is not busy (UART_USR[0] is 0) and always readable. This bit is used to enable the reading and writing of the Divisor Latch register (UART_DLL and UART_DLH) to set the baud rate of the UART. This bit must be cleared after the initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (UART_RBR)/TX Holding Register (UART_THR) and Interrupt Enable Register (UART_IER) 1: Select Divisor Latch LS Register (UART_DLL) and Divisor Latch MS Register (UART_DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to 0, the serial output is forced to the spacing (logic 0) state. When not in Loopback mode, as determined by UART_MCR[4], the SOUT line is forced low until the Break bit is cleared. If SIR_MODE is enabled and active (UART_MCR[6] is set to 1), the sir_out_n line is continuously pulsed. When in Loopback mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
5:4	R/W	0x0	EPS Even Parity Select It is writable only when UART is not busy (UART_USR[0] is 0). This is used to select the even and odd parity when the PEN is enabled (the UART_LCR[3] is set to 1). Setting the UART_LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11: 9th bit = 0, indicates that this is a data byte. 10: 9th bit = 1, indicates that this is an address byte. **Note: When using this function, the PEN(UART_LCR[3]) must set to 1.**
3	R/W	0x0	PEN Parity Enable It is writable only when UART is not busy (UART_USR[0] is 0) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial characters respectively. 0: Parity disabled 1: Parity enabled
2	R/W	0x0	STOP Number of stop bits It is writable only when UART is not busy (UART_USR[0] is 0) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to 0, one stop bit is transmitted in the serial data. If set to 1 and the data bits are set to 5 (UART_LCR[1:0] is 0), one and a half stop bit is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x0	DLS Data Length Select It is writable only when UART is not busy (UART_USR[0] is 0) and always readable. This is used to select the count of bits in a transmitted or received frame. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

10.2.6.9 0x0010 UART Modem Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 00: UART Mode 01: IrDA SIR Mode 10: RS485 Mode 11: Reserved
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the AFCE bit is set, the AutoFlow Control is enabled. 0: Auto Flow Control mode disabled 1: Auto Flow Control mode enabled

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, UART_MCR[6] is set to 0), the data on the SOUT line is held high, while serial data output is looped back to the sin line, internally. In this mode, all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, UART_MCR[6] is set to 1), the data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The RTS (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (UART_MCR[5] is set to 0), the rts_n signal is set low by programming UART_MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (UART_MCR[5] is set to 1) and FIFOs enable (UART_FCR[0] is set to 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when UART_MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (UART_MCR[4] is set to 1), the rts_n output is held inactive high while the value of this location is internally looped back to an input.

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The DTR output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (UART_MCR[4] is set to 1), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

10.2.6.10 0x0014 UART Line Status Register (Default Value: 0x0000_0060)

Offset:0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to “1” when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by reading from the UART_LSR register, there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register (UART_THR) and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" when the TX Holding Register (UART_THR) is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.

Offset:0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set when the serial input, sir_in, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set when the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the UART_LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the UART_LSR is read.
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (UART_LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (UART_LSR[4]). 0: no framing error 1: framing error Reading the UART_LSR clears the FE bit.

Offset:0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (UART_LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (UART_LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (UART_LSR[4]). 0: no parity error 1: parity error Reading the UART_LSR clears the PE bit.
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the UART_RBR. When this happens, the data in the UART_RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the UART_LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the UART_RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the UART_RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode. **Note: Not use when the RXDMA master is enabled (RXDMA_CTRl[0] is set to 1).**

10.2.6.11 0x0018 UART Modem Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by setting the modem or data. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of the dsr_n. When the Data Set Ready input (dsr_n) is asserted, it is an indication that the modem or data set is ready to establish communication with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (UART_MCR[4] is set to 1), the DSR is the same as the DTR (UART_MCR[0]).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (UART_MCR[4] = 1), the CTS is the same as the RTS (UART_MCR[1]).

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the UART_MSR was read. 0: no change on dcd_n since the last read of UART_MSR 1: change on dcd_n since the last read of UART_MSR Reading the UART_MSR clears the DDCD bit. **Note: If the DDCD bit is not set and the DCD_N signal is asserted (low) and a reset occurs, then the DDCD bit is set when the reset is removed if the DCD_N signal remains asserted.**
2	RC	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change in the input RI_N (from an active-low to an inactive-high state) has occurred since the last time the UART_MSR was read. 0: no change on RI_N since the last read of UART_MSR 1: change on RI_N since the last read of UART_MSR Reading the UART_MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the UART_MSR was read. 0: no change on dsr_n since the last read of UART_MSR 1: change on dsr_n since the last read of UART_MSR Reading the UART_MSR clears the DDSR bit. In Loopback Mode (UART_MCR[4] = 1), the DDSR reflects changes on the DTR (UART_MCR[0]). **Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs, then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.**
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the UART_MSR was read. 0: no change on ctsdsr_n since the last read of UART_MSR 1: change on ctsdsr_n since the last read of UART_MSR Reading the UART_MSR clears the DCTS bit. In Loopback Mode (UART_MCR[4] = 1), the DCTS reflects changes on the RTS (UART_MCR[1]). **Note: If the DCTS bit is not set and the CTS_N signal is asserted (low) and a reset occurs, then the DCTS bit is set when the reset is removed if the CTS_N signal remains asserted.**

10.2.6.12 0x001C UART Scratch Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: UART_SCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

10.2.6.13 0x007C UART Status Register (Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF RX FIFO Full This is used to indicate that the RX FIFO is completely full. 0: RX FIFO not full 1: RX FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE RX FIFO Not Empty This is used to indicate that the RX FIFO contains one or more entries. 0: RX FIFO is empty 1: RX FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE TX FIFO Empty This is used to indicate that the TX FIFO is completely empty. 0: TX FIFO is not empty 1: TX FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF TX FIFO Not Full This is used to indicate that the TX FIFO is not full. 0: TX FIFO is full 1: TX FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

10.2.6.14 0x0080 UART Transmit FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	TFL TX FIFO Level The bit indicates the number of data entries in the TX FIFO.

10.2.6.15 0x0084 UART Receive FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	RFL RX FIFO Level The bit indicates the number of data entries in the RX FIFO. **Note: Not use when the RXDMA master is enabled (UART_RXDMA_CTRL[0] is set to 1).**

10.2.6.16 0x0088 UART DMA Handshake Configuration Register (Default Value: 0x0000_00A5)

Offset: 0x0088			Register Name: UART_HSK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

10.2.6.17 0x008C UART DMA Request Enable Register (Default Value: 0x0000_0003)

Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DMA Timeout Enable 0: Disable 1: Enable
1	R/W	0x1	DMA TX REQ Enable 0: Disable 1: Enable

Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	DMA RX REQ Enable 0: Disable 1: Enable

10.2.6.18 0x00A4 UART Halt TX Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	PTE The sending of TX_REQ In DMA1 mode (FIFO on), if the PTE is set to 1 when the TFL in UART_TFL is less than or equal to the trigger value, the controller sends the DMA request. If the PTE is set to 0, when FIFO is empty, the controller sends the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if the PTE is set to 1 and FIFO is on, when the TFL in UART_TFL is less than or equal to the trigger value, the controller sends DMA request. If the PTE is set to 1 and FIFO off, when the THR in UART_THR is empty, the controller sends DMA request. If the PTE is set to 0, when FIFO(FIFO Enable) or THR(FIFO Enable) is empty, the controller sends DMA request. Otherwise, the DMA request is cleared.
6	R/W	0x0	DMA_PTE_RX The Transmission of RX_DRQ In DMA1 mode, when RFL is more than or equal to the trigger value, or a receive timeout has occurred, the controller sends DRQ. In DMA0 mode, when DMA_PTE_RX = 1 and FIFO is on, if RFL is more than or equal to trig, the controller sends DRQ, else DRQ is cleared. In other cases, once the received data is valid, the controller sends DRQ.
5	R/W	0x0	SIR_RX_INVERT SIR RX Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR TX Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/WAC	0x0	CHANGE_UPDATE After the user uses UART_HALT[1] to change the baud rate or LCR configuration, write 1 to update the configuration and wait this bit to self-clear to 0 to finish update process. Writing 0 to this bit has no effect. 1: Update trigger, self-clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baud rate register (UART_DLH and UART_DLL) when the UART is busy. 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0: Halt TX disabled 1: Halt TX enabled **Note: If FIFOs are not enabled, the setting has no effect on operation.**

10.2.6.19 0x00B0 UART DBG DLL Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: UART_DBG_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	DEBUG DLL

10.2.6.20 0x00B4 UART DBG DLH Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: UART_DBG_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	DEBUG DLH

10.2.6.21 0x00F0 UART FIFO Clock Control Register (Default Value: 0x0000_0003)

Offset: 0x00F0			Register Name: UART_FCC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R	0x0	FIFO Depth Indicates the depth of TX/RX FIFO
7:3	/	/	/
2	R/W	0x0	RXFIFO Clock Mode 0: Sync mode, writing/reading clocks use apb clock 1: Sync mode, writing clock uses apb clock, reading clock uses ahb clock
1	R/W	0x1	TX FIFO Clock Enable 0: Clock disable 1: Clock enable
0	R/W	0x1	RX FIFO Clock Enable 0: Clock disable 1: Clock enable

10.3 Serial Peripheral Interface (SPI)

10.3.1 Overview

The Serial Peripheral Interface (SPI) is a full-duplex, synchronous, four-wire serial communication interface between a CPU and SPI-compliant external devices. The SPI controller contains a 64 x 8 bits receiver buffer (RXFIFO) and a 64 x 8 bits transmit buffer (TXFIFO). It can work in master mode and slave mode.

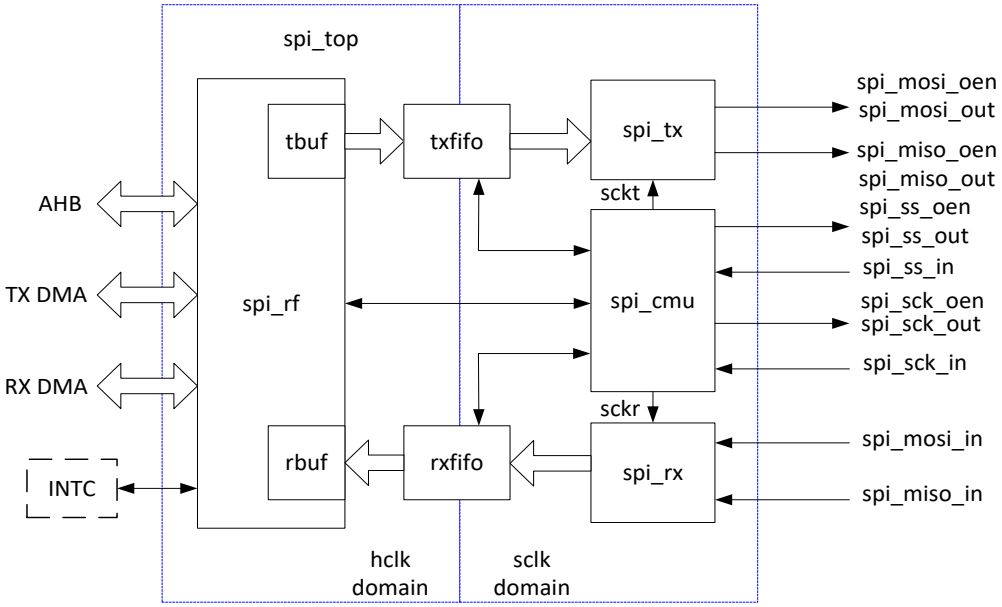
The SPI has the following features:

- Four SPI interfaces for V851S: SPI0, SPI1, SPI2, and SPI3
- Three SPI interfaces for V851SE: SPI0, SPI2, and SPI3
- Supports multiple SPI mode
  - Standard SPI (3-Wire/4-Wire SPI)
  - Dual-Output/Dual-Input SPI/ Dual I/O SPI
  - Quad-Output/Quad-Input SPI
  - Supports programmable serial data frame length: 0bit to 32bits
- Support the maximum IO rate of the mass production: 100 MHz
- Support TX/RX DMA slave interface
- Transmit and receive data FIFOs with 8-bit wide and 64-entry
- Supports data sample mode
  - mode0, mode1, mode2 and mode3
- Supports Controll singnal configutation
  - Four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

10.3.2 Block Diagram

The following figure shows a block diagram of the SPI.

Figure 10-17 SPI Block Diagram



SPI contains the following sub-blocks:

Table 10-6 SPI Sub-blocks

Sub-block	Description
spi_rf	Responsible for implementing the internal register, interrupt, and DMA Request.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	Responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.
spi_tx	Responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	Responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.

10.3.3 Functional Description

10.3.3.1 External Signals

The following table describes the external signals of SPI. The MOSI and MISO are bidirectional I/O, when SPI is as a master device, the CLK and CS are the output pin; when SPI is as a slave device, the CLK and CS are the input pin. When using SPI, the corresponding PADs are selected as SPI function via section 9.7 “GPIO”.

Table 10-7 SPI External Signals

Signal	Description	Type
SPI0-CS0	SPI0 Chip Select Signal0 (low active)	I/O
SPI0-CS1	SPI0 Chip Select Signal1 (low active)	I/O
SPI0-CLK	SPI0 Clock Signal Provides serial interface timing	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI0-HOLD	SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI2-CS0	SPI2 Chip Select Signal0 (low active)	I/O
SPI2-CS1	SPI2 Chip Select Signal1 (low active)	I/O
SPI2-CLK	SPI2 Clock Signal Provides serial interface timing.	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI3-CS0	SPI3 Chip Select Signal0 (low active)	I/O
SPI3-CLK	SPI3 Clock Signal Provides serial interface timing.	I/O
SPI3-MOSI	SPI3 Master Data Out, Slave Data In	I/O
SPI3-MISO	SPI3 Master Data In, Slave Data Out	I/O

10.3.3.2 Clock Sources

The SPI controller gets 5 different clock sources, users can select one of them to make SPI clock source. The following table describes the clock sources for SPI. For more details on the clock setting, configuration, and gating information, see section 3.4 Clock Controller Unit (CCU)

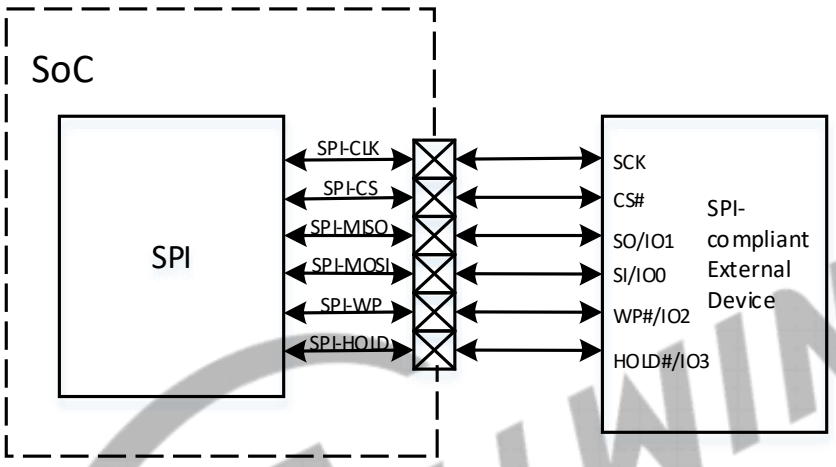
Table 10-8 SPI Clock Sources

Clock Sources	Description
OSC24M	24 MHz Crystal
PLL_PERI	Peripheral Clock

10.3.3.3 Typical Application

The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 10-18 SPI Application Block Diagram



10.3.3.4 SPI Transmit Format

The SPI supports 4 different formats for data transfer. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR (Offset: 0x0008). The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

The CPOL (SPI_TCR[1]) defines the polarity of the clock signal (SPI_SCLK). The SPI_SCLK is a high level when CPOL is '1' and it is a low level when CPOL is '0'. The CPHA (SPI_TCR[0]) decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used to setup data when CPHA is '1', and sample data when CPHA is '0'. The following table lists the four modes.

Table 10-9 SPI Transmit Format

Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
Mode0	0	0	Sample on the rising edge	Setup on the falling edge
Mode1	0	1	Setup on the rising edge	Sample on the falling edge
Mode2	1	0	Sample on the falling edge	Setup on the rising edge
Mode3	1	1	Setup on the falling edge	Sample on the rising edge

The following figures describe four waveform for SPI_SCLK.

Figure 10-19 SPI Phase 0 Timing Diagram

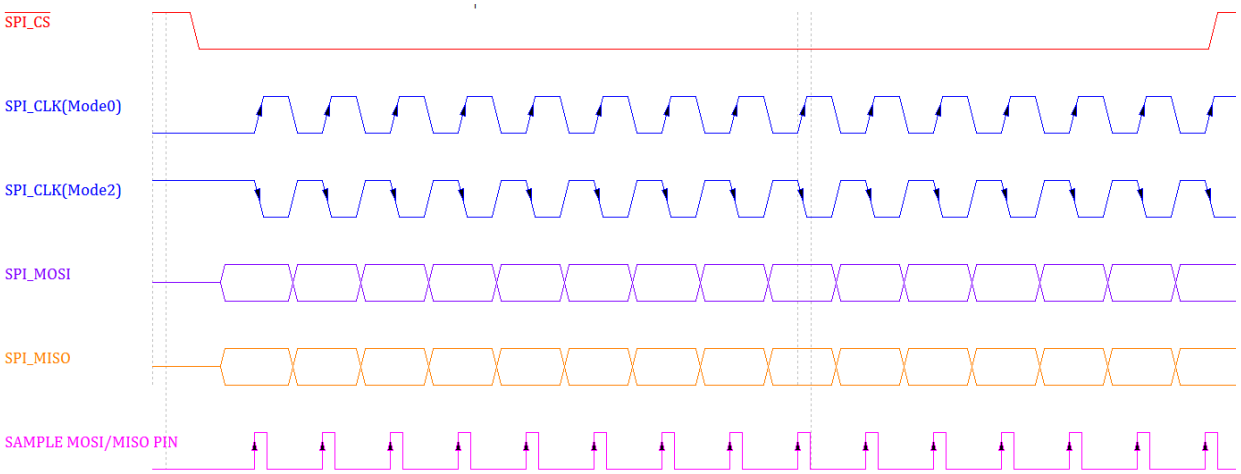
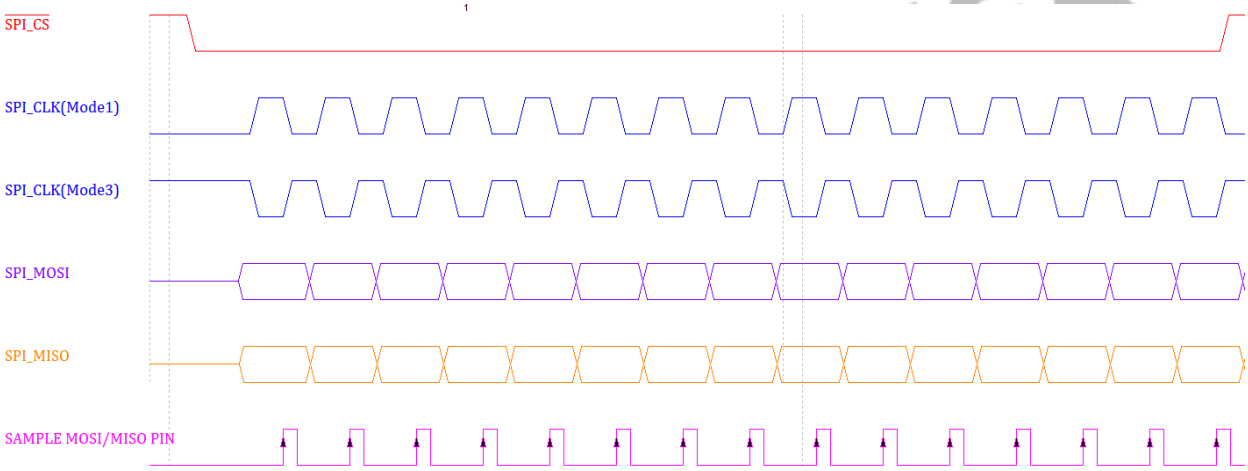


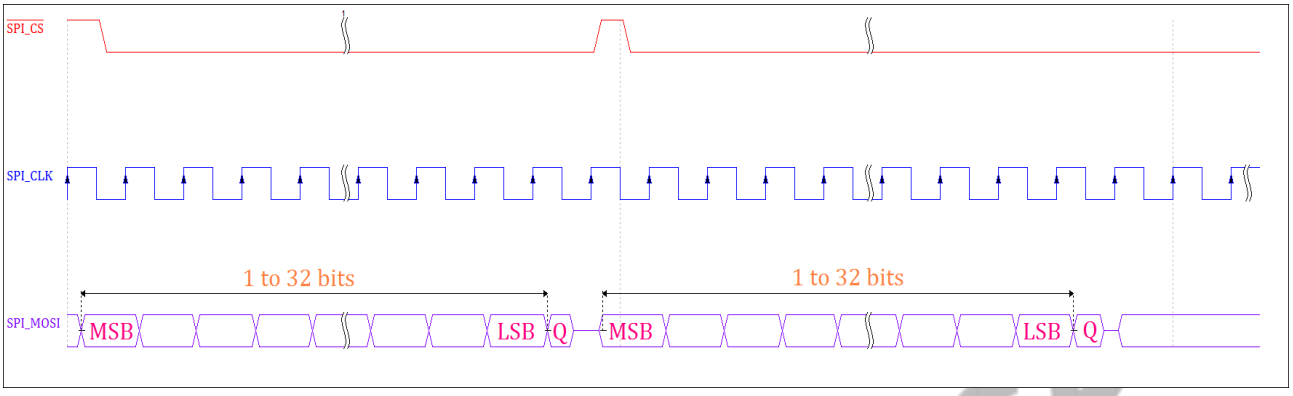
Figure 10-20 SPI Phase 1 Timing Diagram



10.3.3.5 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATCR[1:0]) is equal to 0x2. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes the 3-wire mode.

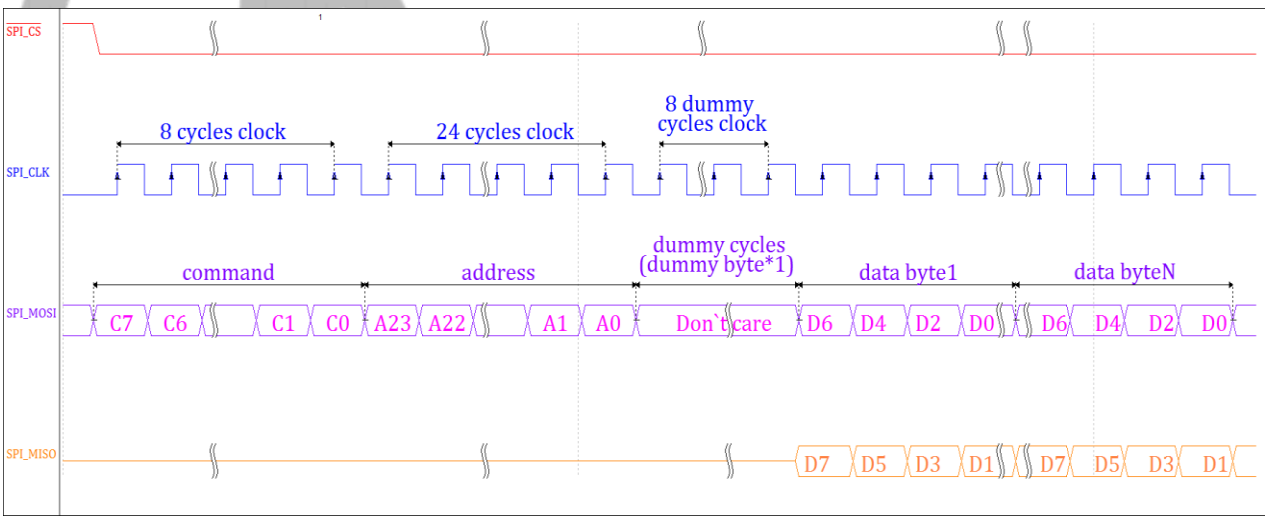
Figure 10-21 SPI 3-Wire Mode



10.3.3.6 SPI Dual-Input/Dual-Output and Dual I/O Mode

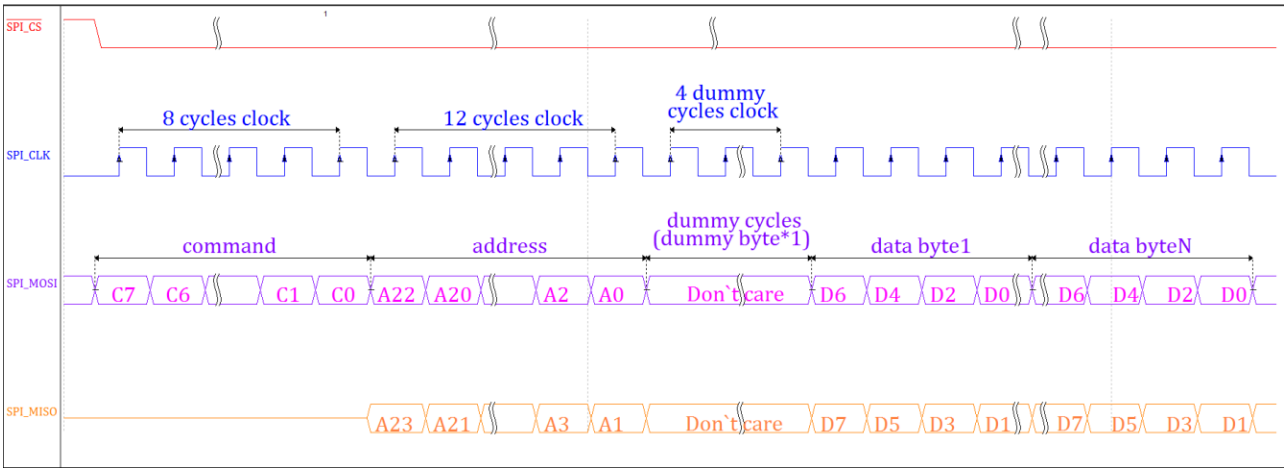
The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC (Offset: 0x0038) [28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI.

Figure 10-22 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 10-23 SPI Dual I/O Mode

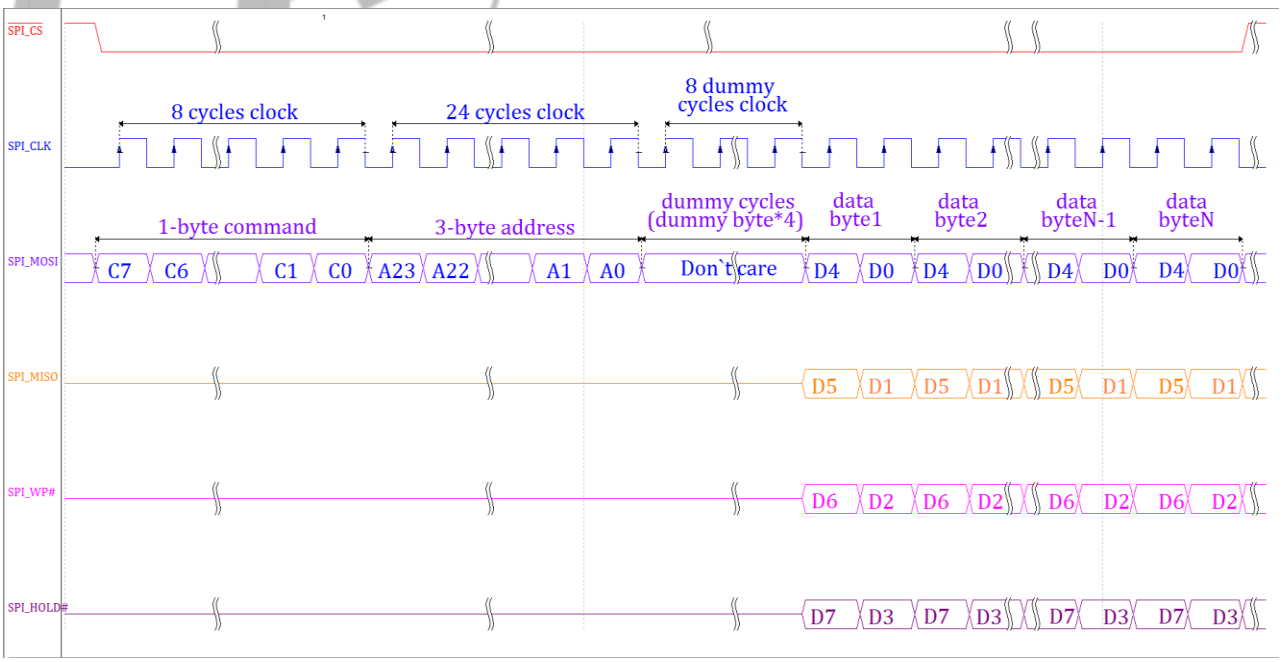


In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

10.3.3.7 SPI Quad-Input/Quad-Output Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC (Offset: 0x0038) [29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#) and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Figure 10-24 SPI Quad-Input/Quad-Output Mode



In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

10.3.3.8 SPI Error Conditions

If any error conditions occur, the hardware will set the corresponding status bits in the SPI Interrupt Status Register (Offset: 0x0014) and stop the transfer. For the SPI controller, the following error scenarios can happen.

- TX_FIFO Underrun

The TX_FIFO underrun happens when the CPU/DMA reads data from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- TX_FIFO Overflow

The TX_FIFO overflow happens when the CPU/DMA writes data into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Underrun

The RX_FIFO underrun happens when the CPU/DMA reads data from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_UDF bit. To start a new transaction, the software has to reset the fifo by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Overflow

The RX_FIFO overflow happens when the CPU/DMA writes data into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

10.3.4 Programming Guidelines

10.3.4.1 Writing/Reading Data Process

The SPI transfers serial data between the processor and the external device. The CPU mode and DMA mode are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX channel and RX channel. The

TX channel has the path from TX FIFO to the external device. The RX channel has the path from the external device to RX FIFO.

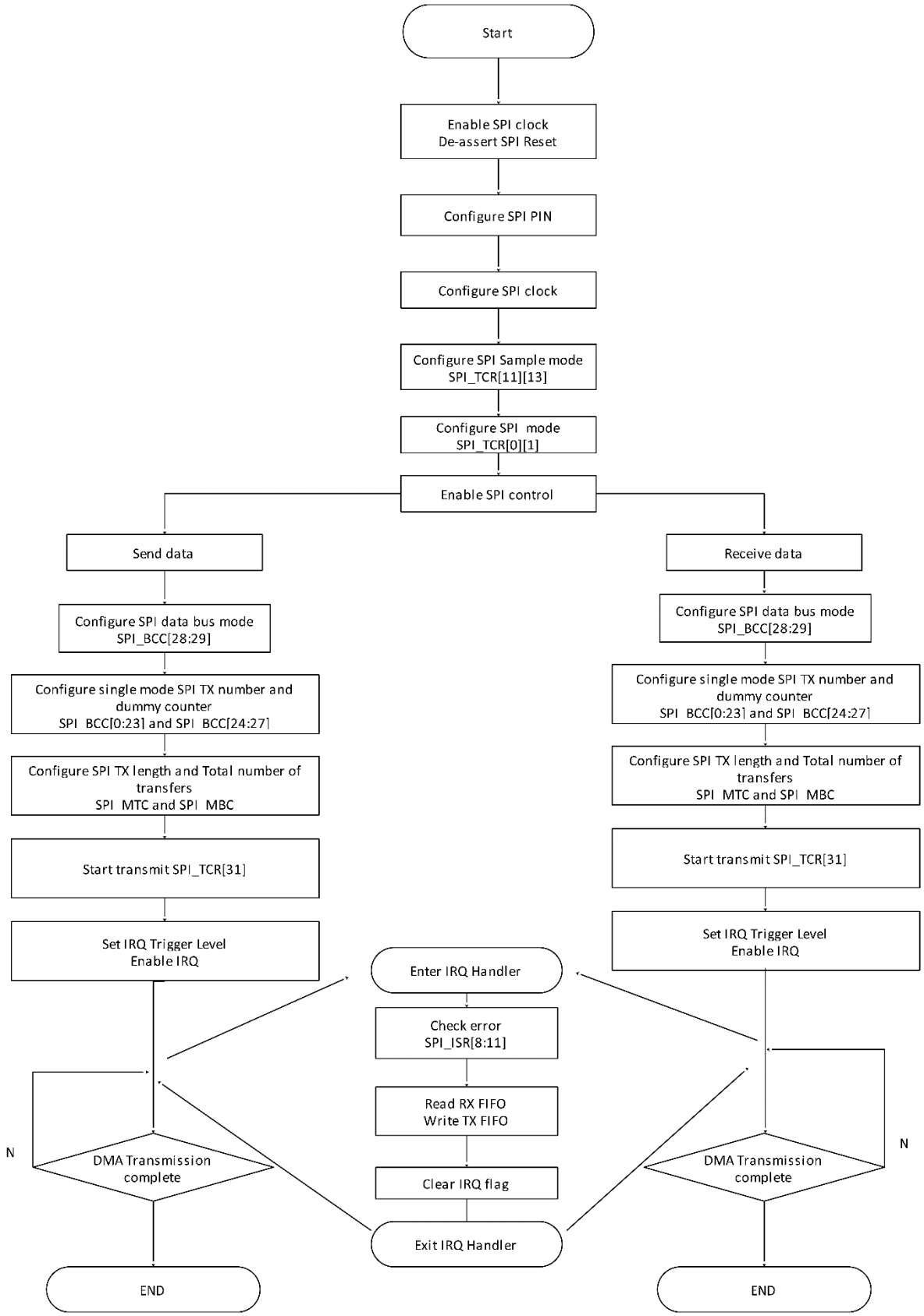
Write Data: The CPU or DMA must write data on the SPI_TXD (Offset: 0x0200), the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, the CPU or DMA must access the SPI_RXD (Offset: 0x0300) and the data are automatically sent to the SPI_RXD (Offset: 0x0300).

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor after each transmission is complete.

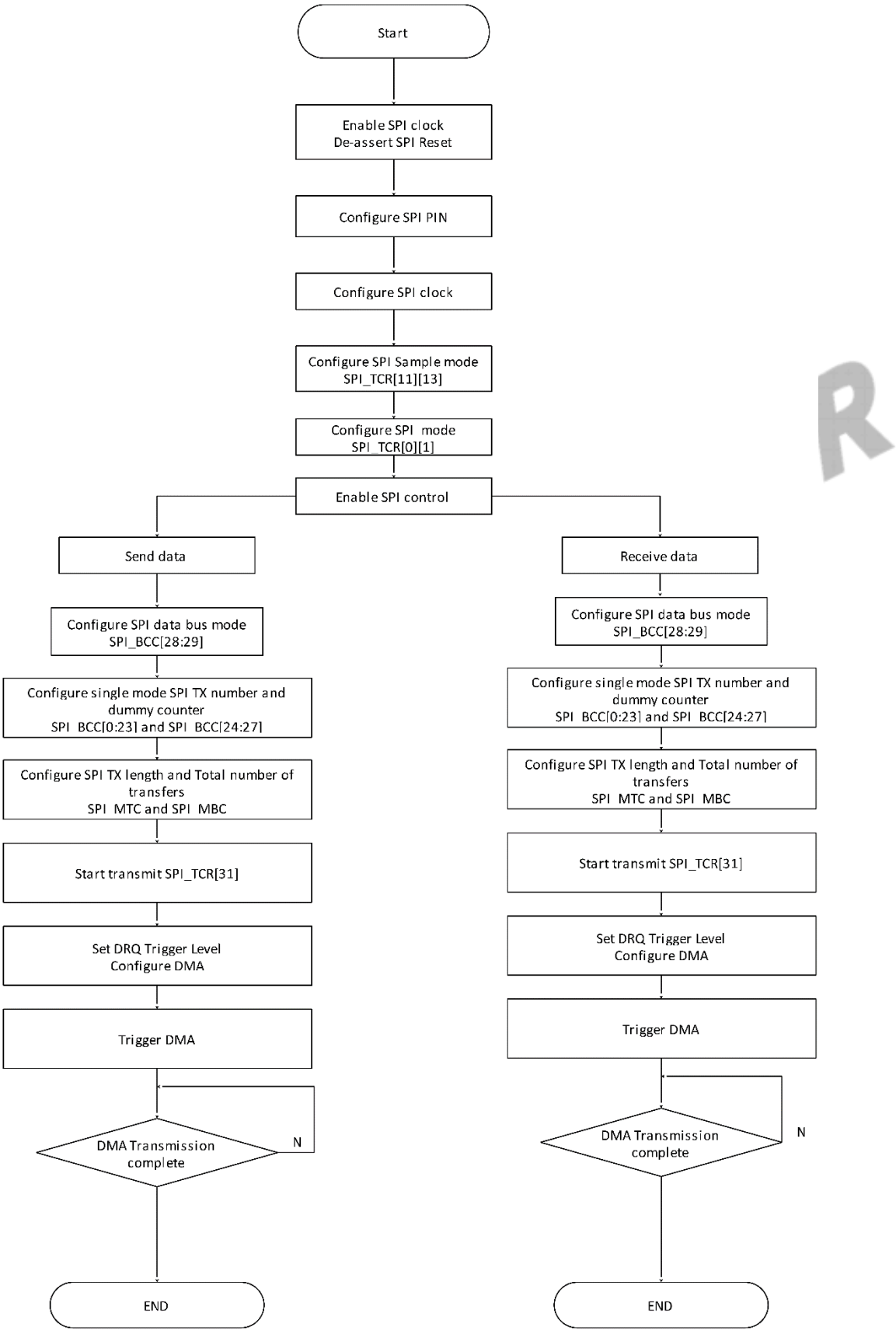
CPU Mode

Figure 10-25 SPI Write/Read Data in CPU Mode



DMA Mode

Figure 10-26 SPI Write/Read Data in DMA Mode



10.3.4.2 Calibrate Delay Chain

The SPI has one delay chain which is used to generate delay to make proper timing between the internal SPI clock signal and data signals. Delay chain is made up of 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

1. Enable SPI. To calibrate the delay chain by the operation registers in SPI, the SPI must be enabled through AHB reset and AHB clock gating control registers.
2. Configure a proper clock for SPI. The calibration delay chain is based on the clock for SPI from CCU.
3. Set proper initial delay value. Write 0xA0 to the SPI Sample Delay Control Register (Offset: 0x0028) to set initial delay value 0x20 to delay chain. Then write 0x0 to the SPI Sample Delay Control Register (Offset: 0x0028) to clear this value.
4. Write 0x8000 to the SPI Sample Delay Control Register (Offset: 0x0028) to start to calibrate the delay chain.
5. Wait until the flag (bit14 in the SPI Sample Delay Control Register) of calibration done is set. The number of delay cells is shown at the bit[13:8] of the SPI Sample Delay Control Register (Offset: 0x0028). The delay time generated by these delay cells is equal to the cycle of the SPI clock nearly. This value is the result of calibration.
6. Calculate the delay time of one delay cell according to the cycle of the SPI clock and the result of calibration.

10.3.5 Register List

Module Name	Base Address	Comments
SPI0	0x0402 5000	SPI controller
SPI1 (Only for V851S)	0x0402 6000	SPI controller
SPI2	0x0402 7000	SPI controller
SPI3	0x0402 8000	SPI controller

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control Register
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter Register
SPI_MTC	0x0034	SPI Master Transmit Counter Register

Register Name	Offset	Description
SPI_BCC	0x0038	SPI Master Burst Control Register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0044	SPI Bit-Aligned Clock Configuration Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

10.3.6 Register Description

10.3.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset:0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes. Writing '0' to this bit has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control the transmit state machine to stop smart burst sending when RX FIFO is full. 0: Normal operation, ignore RXFIFO status 1: Stop transmit data when RXFIFO full Cannot be written when XCH=1.
6:3	/	/	/
2	R/W	0x0	MODE_SELEC Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing Cannot be written when XCH=1.
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave mode 1: Master mode Cannot be written when XCH=1.

Offset:0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable After transforming from bit_mode to byte_mode, it must enable the SPI module again.

10.3.6.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode, it is used to start SPI burst. 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will auto-clear after finishing the bursts transfer specified by SPI_MBC. Writing “1” to SRST (SPI_GCR[31]) will also clear this bit. Writing ‘0’ to this bit has no effect. Cannot be written when XCH=1.
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to ‘1’ to make the internal read sample point with a delay of half-cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. 0: normal operation, do not delay the internal read sample point 1: delay the internal read sample point Cannot be written when XCH=1.
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to "1" to make the data that should be sent with a delay of half-cycle for SPI_CLK in dual IO mode of SPI mode0. Cannot be written when XCH=1.

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay sample mode 1: Normal sample mode In normal sample mode, the SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, the SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode. Cannot be written when XCH=1.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Cannot be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half-cycle for SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. 0: Normal operation, do not delay the internal read sample point 1: Delay the internal read sample point Cannot be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select rapid mode for high speed write. 0: Normal write mode 1: Rapid write mode Cannot be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Cannot be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode, it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in the BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during the dummy burst period. The burst number is specified by TC. Cannot be written when XCH=1.

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x1	SS_LEVEL When control SS signal manually (SS_OWNER (SPI_TCR[6])==1), set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high Cannot be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, the controller sends the SS signal automatically with data together. When this bit is set to 1, the software must manually write SS_LEVEL (SPI_TCR[7]) to 1 or 0 to control the level of the SS signal. 0: SPI controller 1: Software Cannot be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Cannot be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output waveform for the SPI_SSx signal. Only valid when SS_OWNER (SPI_TCR[6])= 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Cannot be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Cannot be written when XCH=1.

10.3.6.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip select signal (SSx) from the valid state to the invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

10.3.6.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SPI_SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by SPI_MBC have been exchanged. In other conditions, when setting, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer completed

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when the TXFIFO is overflowed. Writing 1 to this bit clears it. 0: TXFIFO is not overflowed 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO is underrun. Writing 1 to this bit clears it. 0: RXFIFO is not underrun 1: RXFIFO is underrun
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is not overflowed 1: RXFIFO is overflowed
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set when the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words 1: TXFIFO is empty

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit will be immediately set to 1 if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. The TX_WL is the water level of TXFIFO.
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is will be immediately set to 1 if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. The RX_WL is the water level of RXFIFO.

10.3.6.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, writing to ‘0’ has no effect.

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable In normal mode, the TXFIFO can only be read by the SPI controller, writing '1' to this bit will switch the read and write function of the TXFIFO to AHB bus. This bit is used to test the TXFIFO, do not set in normal operation, and do not set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TXFIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TXFIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, writing '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, the RXFIFO can only be written by the SPI controller, writing '1' to this bit will switch the read and write function of RXFIFO to AHB bus. This bit is used to test the RXFIFO, do not set in normal operation, and do not set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

10.3.6.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64: 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

10.3.6.7 0x0020 SPI Wait Clock Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/

Offset: 0x0020			Register Name: SPI_WCR
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). These bits control the number of wait states to be inserted before starting dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying the next word data transfer. 0: No wait states inserted n: n SPI_SCLK wait states inserted Cannot be written when XCH=1.
15:0	R/W	0x0	WCC Wait Clock Counter (In master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying the next word data transfer. 0: No wait states inserted n: n SPI_SCLK wait states inserted Cannot be written when XCH=1.

10.3.6.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, the sample delay chain calibration is started. Cannot be written when XCH=1.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL. Cannot be written when XCH=1.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to the current card clock. The delay time generated by these delay cells is equal to the cycle of the card clock nearly. Generally, it is necessary to do drive delay calibration when the card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set. Cannot be written when XCH=1.

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, it indicates that enable sample delay specified at SAMP_DL_SW. Cannot be written when XCH=1.
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between the clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of the card clock, and the input timing requirement of the device. Cannot be written when XCH=1.

10.3.6.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. The total transfer data include the TXD, RXD, and dummy burst. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

10.3.6.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Offset: 0x0034			Register Name: SPI_MTC
Bit	**Read/Write**	**Default/Hex**	**Description**
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy bursts. For saving bus bandwidth, the dummy bursts (all zero bits or all one bits) are sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

10.3.6.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad Mode Enable The quad mode includes Quad-Input and Quad-Output. 0: Quad mode disable 1: Quad mode enable Cannot be written when XCH=1.
28	R/W	0x0	DRM Master Dual Mode RX Enable It is only valid when Quad_Mode_EN=0. 0: RX uses the single-bit mode 1: RX uses the dual-bit mode Cannot be written when XCH=1.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receiving in dual SPI mode. The data does not care by the device. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in the single mode before automatically sending dummy bursts. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

10.3.6.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bit frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer Writing “1” to this bit will start to transfer serial bit frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto-clear after the bursts transfer completely. Writing ‘0’ to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Delay Sample Mode 1: Standard Sample Mode In Standard Sample Mode, the SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, the SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/

Offset: 0x0040			Register Name: SPI_BATCR
Bit	**Read/Write**	**Default/Hex**	**Description**
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed It is only valid when Work Mode Select==0x10/0x11.
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when Work Mode Select==0x10/0x11.
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame (burst) of RX 000000: 0 bit 000001: 1 bit … 100000: 32 bits Other values: reserved It is only valid when Work Mode Select==0x10/0x11, and cannot be written when TCE (bit31) is 1.
15:14	/	/	/
13:8	R/W	0x00	TX_FRM_LEN Configure the length of serial data frame (burst) of TX 000000: 0 bit 000001: 1 bit … 100000: 32 bits Other values: reserved It is only valid when Work Mode Select==0x10/0x11, and cannot be written when TCE (bit31) is 1.
7	R/W	0x1	SS_LEVEL When control the SS signal manually, set this bit to ‘1’ or ‘0’ to control the level of SS signal. 0: Set SS to low 1: Set SS to high It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE (bit31) is 1.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, the controller sends the SS signal automatically with data together. When this bit is set to 1, the software must manually write SS_LEVEL to 1 or 0 to control the level of the SS signal. 0: SPI controller 1: Software It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE (bit31) is 1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE (bit31) is 1.
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when Work Mode Select= =0x10/0x11, and only work in Mode0, cannot be written when TCE (bit31) is 1.
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in standard SPI, dual-output/dual input SPI, dual IO SPI, and quad-output/quad-input SPI 01: Reserved 10: Data frame is bit aligned in 3-wire SPI 11: Data frame is bit aligned in standard SPI

10.3.6.13 0x0044 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)). This register is only valid when Work Mode Select==0x10/0x11.

10.3.6.14 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

10.3.6.15 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

10.3.6.16 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	SPI_ACT_M SPI NDMA Active Mode 00: dma_active is low 01: dma_active is high 10: dma_active is controlled by dma_request (DRQ) 11: dma_active is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to dma_active high

10.3.6.17 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in the byte, half-word, or word unit by AHB. In the byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In the half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In the word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note: This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TXFIFO through the AHB bus.**

10.3.6.18 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in the byte, half-word, or word unit by AHB. In the byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In the half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In the word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **Note: This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RXFIFO through the AHB bus.**

10.4 SPI_DBI (Only for V851S)

10.4.1 Overview

The V851S provides a 3/4 line SPI display bus interface (SPI_DBI) for video data transmission. It supports DBI mode or SPI mode. The DBI mode is compatible with multiple video data formats at the same time. The SPI mode is used for low-cost display schemes.

The SPI mode has the following features:

- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Supports interrupts and DMA
- Supports mode0, mode1, mode2, and mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1 bit to 32 bits
- Supports standard SPI, dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI
- Supports maximum IO rate of the mass production: 40 MHz

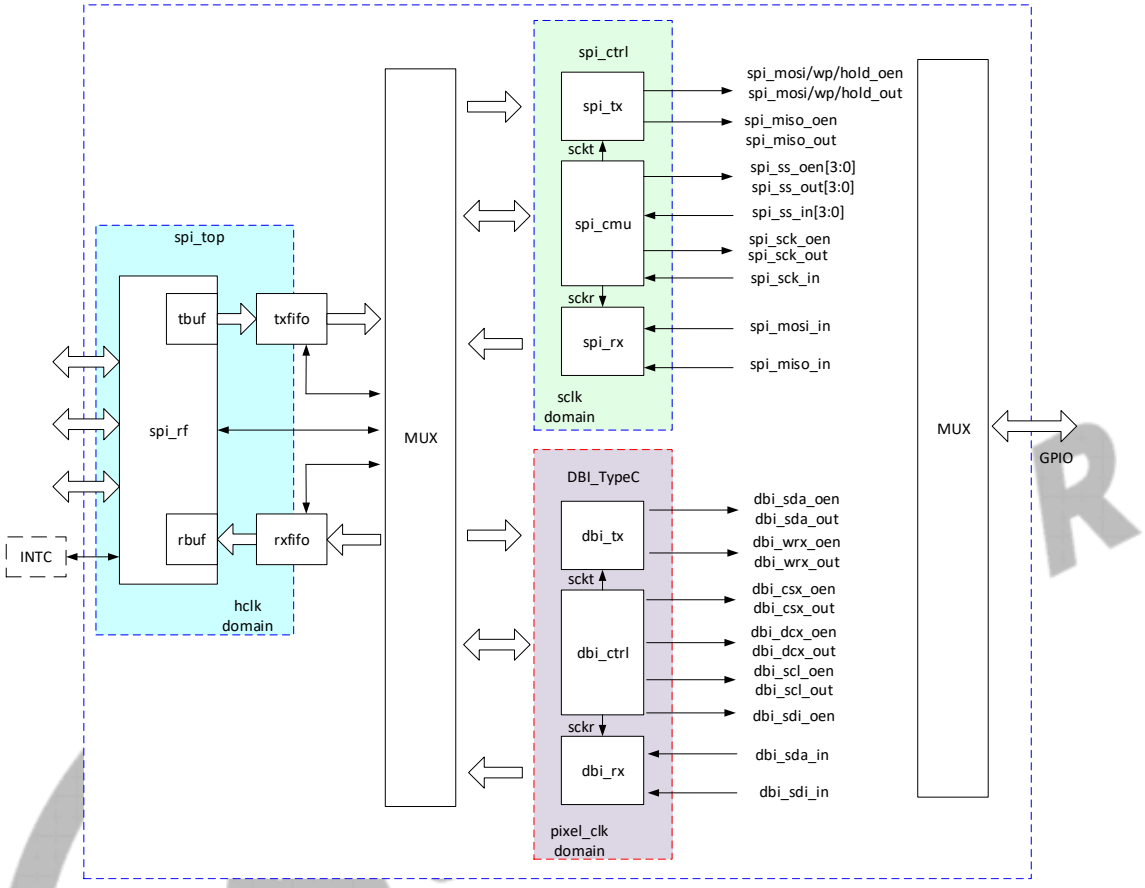
The DBI mode has the following features:

- Supports DBI Type C 3 Line/4 Line Interface Mode
- Supports 2 Data Lane Interface Mode
- Supports data source from CPU or DMA
- Supports RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Supports Tearing effect
- Supports software flexible control video frame rate

10.4.2 Block Diagram

The following figure shows a block diagram of the SPI_DBI.

Figure 10-27 SPI_DBI Block Diagram



SPI_DBI contains the following sub-blocks:

Table 10-10 SPI_DBI Sub-blocks

Sub-block	Description
spi_rf	Responsible for implementing the internal register, interrupt, and DMA Request.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	Responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.
spi_tx	Responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.

Sub-block	Description
spi_rx	Responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.
dbi_ctrl	Responsible for implementing DBI bus clock, chip select, data command select, RGB format reshape.
dbi_tx	Responsible for implementing DBI data transfer, the interface of the internal TXFIFO, and status register.
dbi_rx	Responsible for implementing DBI data receive, the interface of the internal RXFIFO, and status register.

10.4.3 Functional Description

10.4.3.1 External Signals

The following tables describe the external signals of SPI_DBI. When using SPI_DBI, the corresponding PADs are selected as SPI_DBI function via section 10.6 GPIO.

Table 10-11 GPIO multiplexing of SPI1 and DBI

DBI	SPI1
DBI-CSX	SPI1-CS0
DBI-SCLK	SPI1-CLK
DBI-SDO	SPI1-MOSI
DBI-SDI/ DBI-TE/ DBI-DCX	SPI1-MISO
DBI-DCX/DBI-WRX	SPI1-HOLD
DBI-TE	SPI1-WP
/	SPI1-CS1

Table 10-12 SPI_DBI External Signals

External Signal	Description	Type
DBI Mode		
DBI-CSX	Chip select signal, low active	I/O
DBI-SCLK	Serial clock signal	I/O
DBI-SDO	Data output signal	I/O
DBI-SDI	Data input signal, the data is sampled on the rising edge and the falling edge	I/O
DBI-TE	Tearing effect input, it is used to capture the external TE signal edge.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
SPI Mode		

External Signal	Description	Type
SPI1-CS0	SPI1 chip select signal0, low active When the device is not selected, data will not be accepted via the SI pin, and the SO pin will stop transmission.	I/O
SPI1-CS1	SPI1 chip select signal1, low active When the device is not selected, data will not be accepted via the SI pin, and the SO pin will stop transmission.	I/O
SPI1-CLK	SPI1 clock signal This pin is used to provide a clock to the device and is used to control the flow of data to and from the device.	I/O
SPI1-MOSI	SPI1 master data out, slave data in	I/O
SPI1-MISO	SPI1 master data in, slave data out	I/O
SPI1-WP	Write protection and active low It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-HOLD	When the device is selected and a serial sequence is underway, the HOLD pin is can be used to temporarily pause the serial communication with the master device without deselecting or resetting the device serial sequence. While the HOLD pin is asserted, the SO pin is at high impedance, and all transitions on the SCK pin and data on the SI pin are ignored. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O

10.4.3.2 Clock Sources

The SPI_DBI controller gets 3 different clock sources, users can select one of them to make SPI_DBI clock source. The following table describes the clock sources for SPI_DBI. For more details on the clock setting, configuration, and gating information, see section 3.4 Clock Controller Unit (CCU).

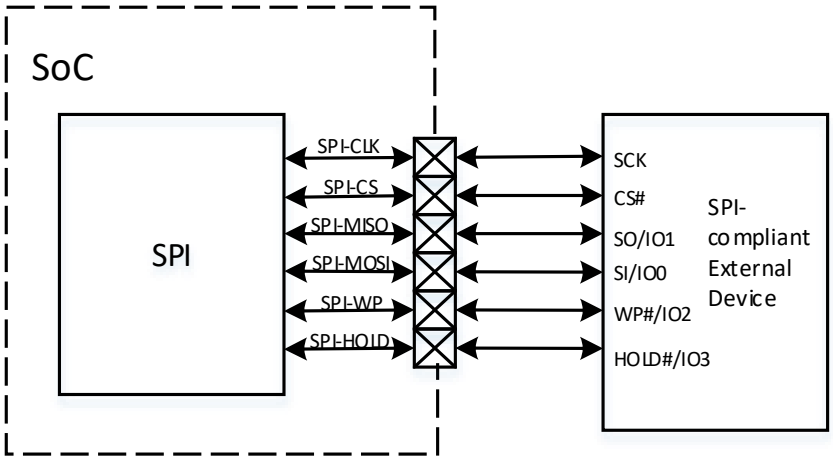
Table 10-13 SPI_DBI Clock Sources

Clock Sources	Description
HOSC	24 MHz Crystal
PLL_PERI(1X)	Peripheral Clock, default value is 600 MHz
PLL_PERI(2X)	Peripheral Clock, default value is 1200 MHz

10.4.3.3 Typical Application

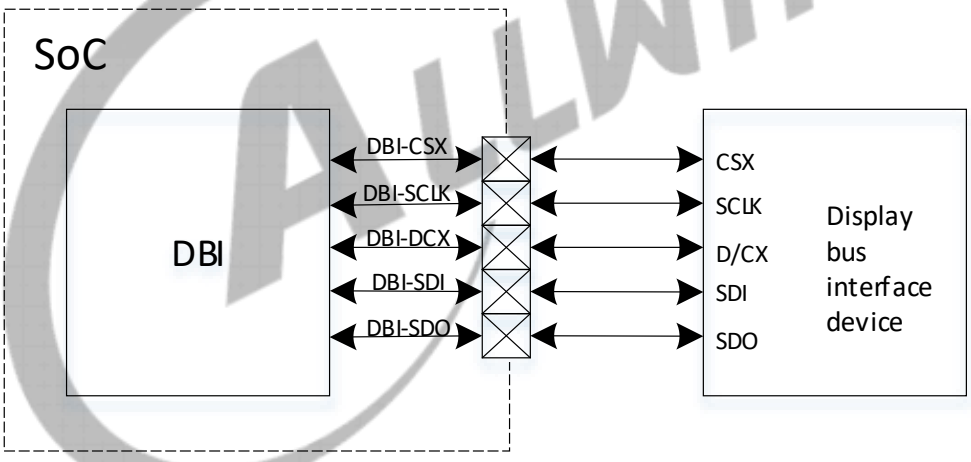
The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 10-28 SPI Application Block Diagram



The following figure shows the application block diagram when the DBI master device is connected to a display bus interface device.

Figure 10-29 DBI Application Block Diagram



10.4.3.4 SPI Transmission Format

The SPI supports 4 different formats for data transmission. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

The CPOL (SPI_TCR[1]) defines the polarity of the clock signal (SPI_SCLK). The SPI_SCLK is a high level when CPOL is '1' and it is a low level when CPOL is '0'. The CPHA (SPI_TCR[0]) decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used to setup data when CPHA is '1', and sample data when CPHA is '0'. The following table lists the four modes.

Table 10-14 SPI Transmit Format

SPI Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
mode0	0	0	Sample on the rising edge	Setup on the falling edge
mode1	0	1	Setup on the rising edge	Sample on the falling edge
mode2	1	0	Sample on the falling edge	Setup on the rising edge
mode3	1	1	Setup on the falling edge	Sample on the rising edge

The following figures describe four waveforms for SPI_SCLK.

Figure 10-30 SPI Phase 0 Timing Diagram

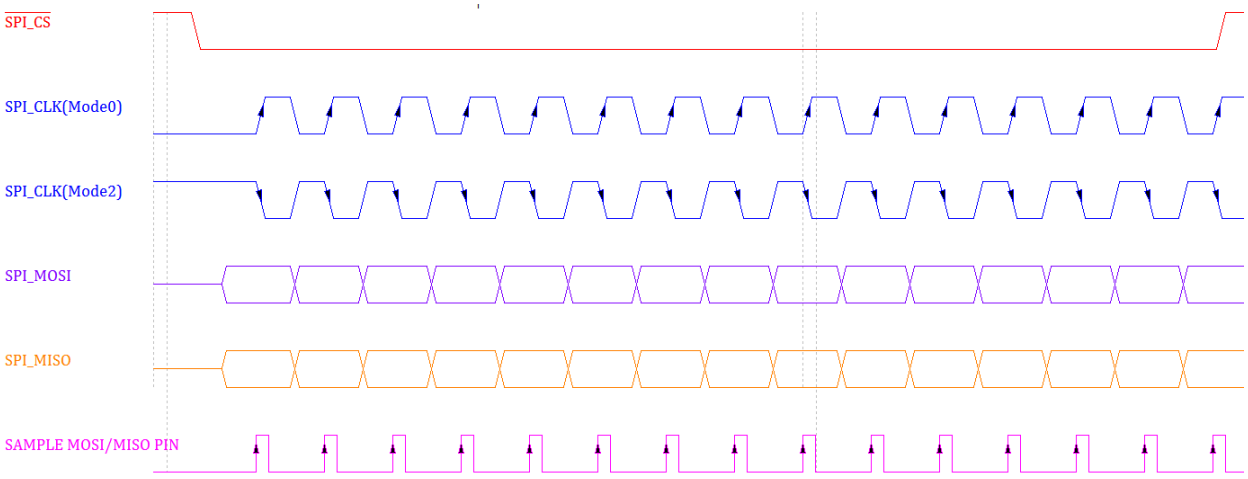
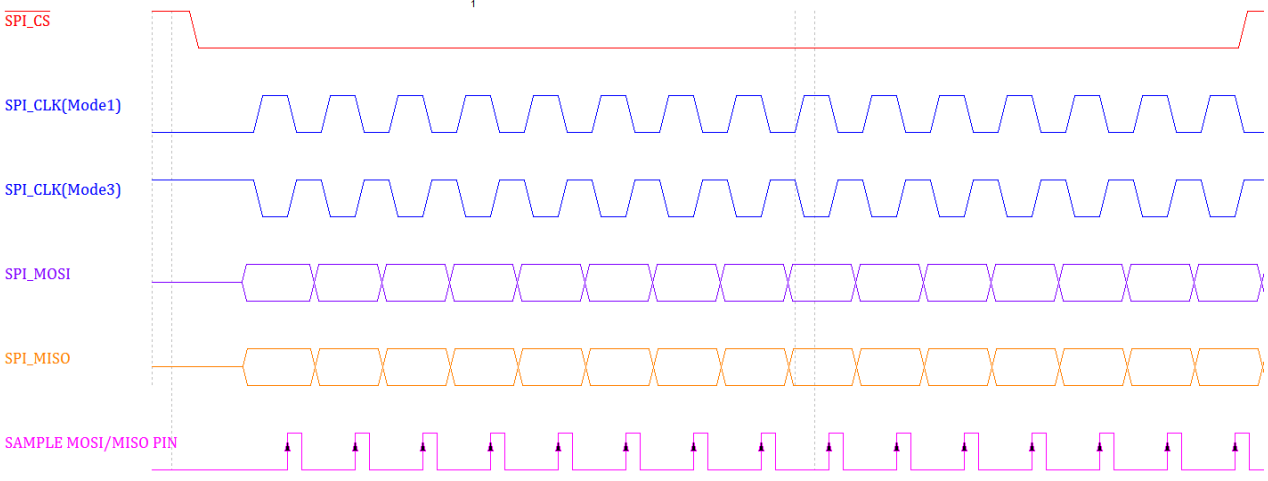


Figure 10-31 SPI Phase 1 Timing Diagram



10.4.3.5 SPI Master and Slave Mode

The SPI controller can be configured to a master or slave device. The master mode is selected by setting the MODE bit (SPI_GCR[1]); the slave mode is selected by clearing the MODE bit.

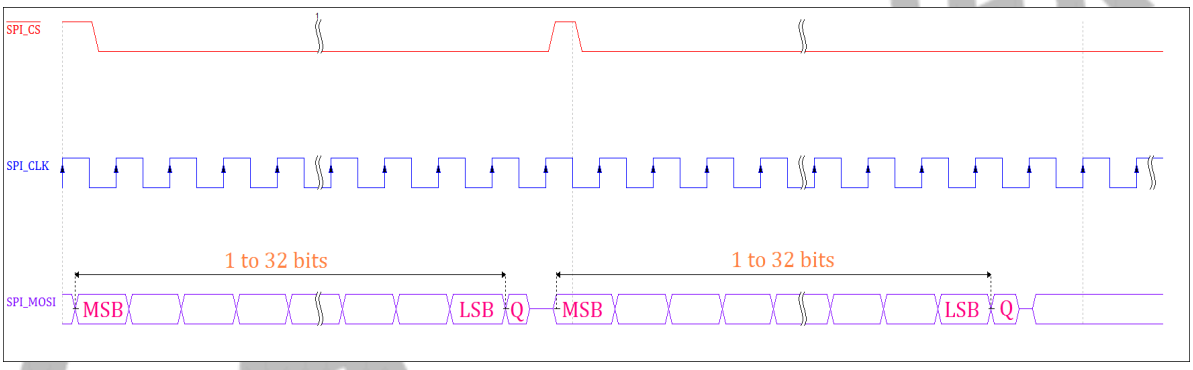
In master mode, the SPI_CLK is generated and transmitted to the external device, and the data from the TX FIFO is transmitted on the MOSI pin, the data from the slave is received on the MISO pin and sent to RX FIFO. The Chip Select (SPI_SS) is an active low signal, and it must be set low before the data are transmitted or received. The SPI_SS can be selected the auto control mode or the software manual control mode. When using auto control, the SS_OWNER (SPI_TCR[6]) must be cleared (default value is 0); when using manual control, the SS_OWNER must be set. And the level of SPI_SS is controlled by SS_LEVEL (SPI_TCR[7]).

In slave mode, after the software selects the MODE bit (SPI_GCR [1]) to '0', it waits for master initiate a transaction. When the master asserts SPI_SS, and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on the MISO pin, and the data from the MOSI pin is received in RX FIFO.

10.4.3.6 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATC[1:0]) is equal to 0x2. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes the 3-wire mode.

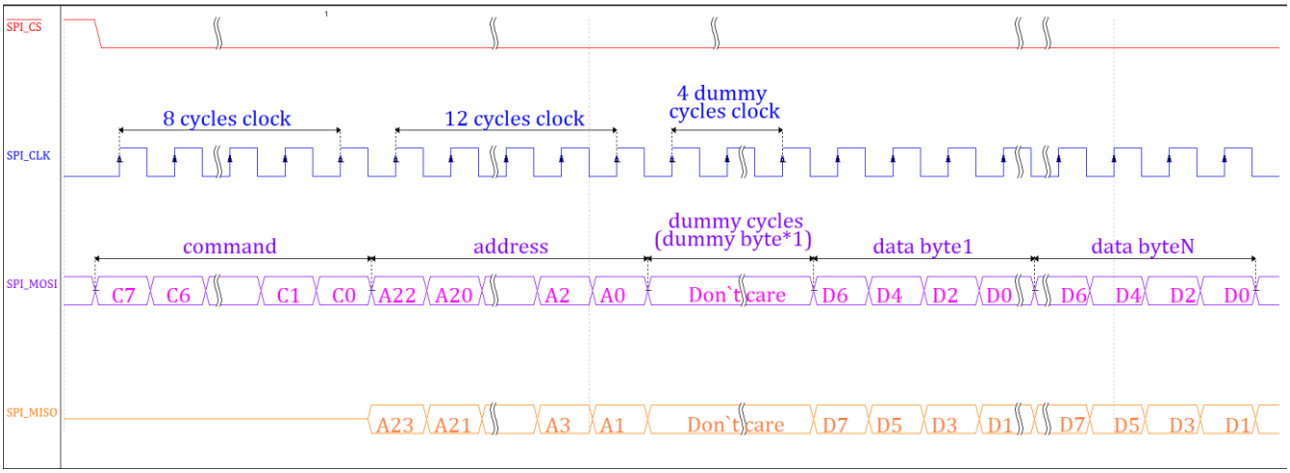
Figure 10-32 SPI 3-Wire Mode



10.4.3.7 SPI Dual-Input/Dual-Output and Dual I/O Mode

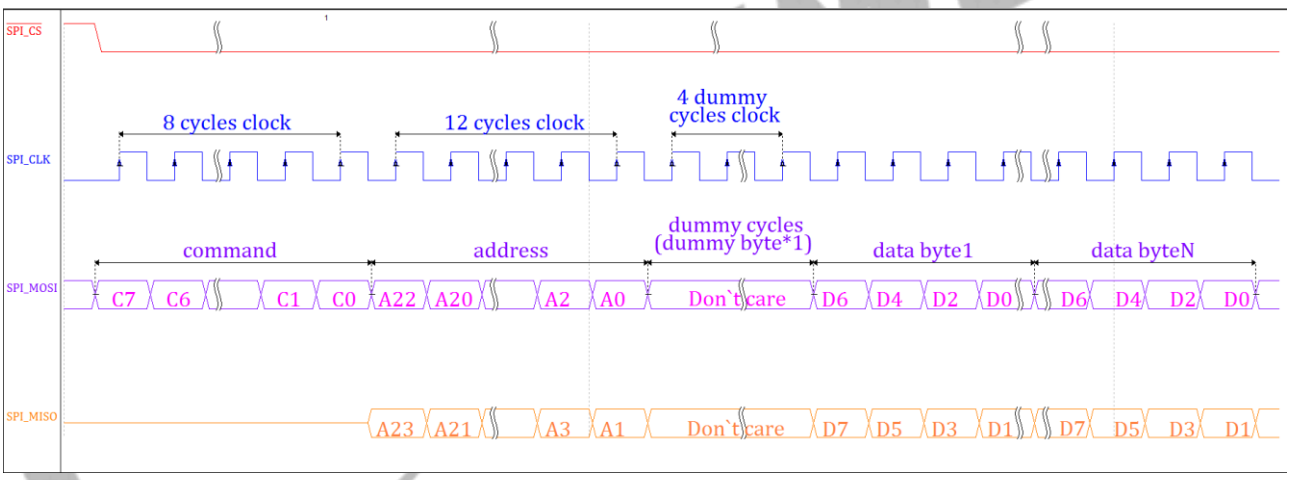
The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC[28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode SPI devices, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI

Figure 10-33 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 10-34 SPI Dual I/O Mode

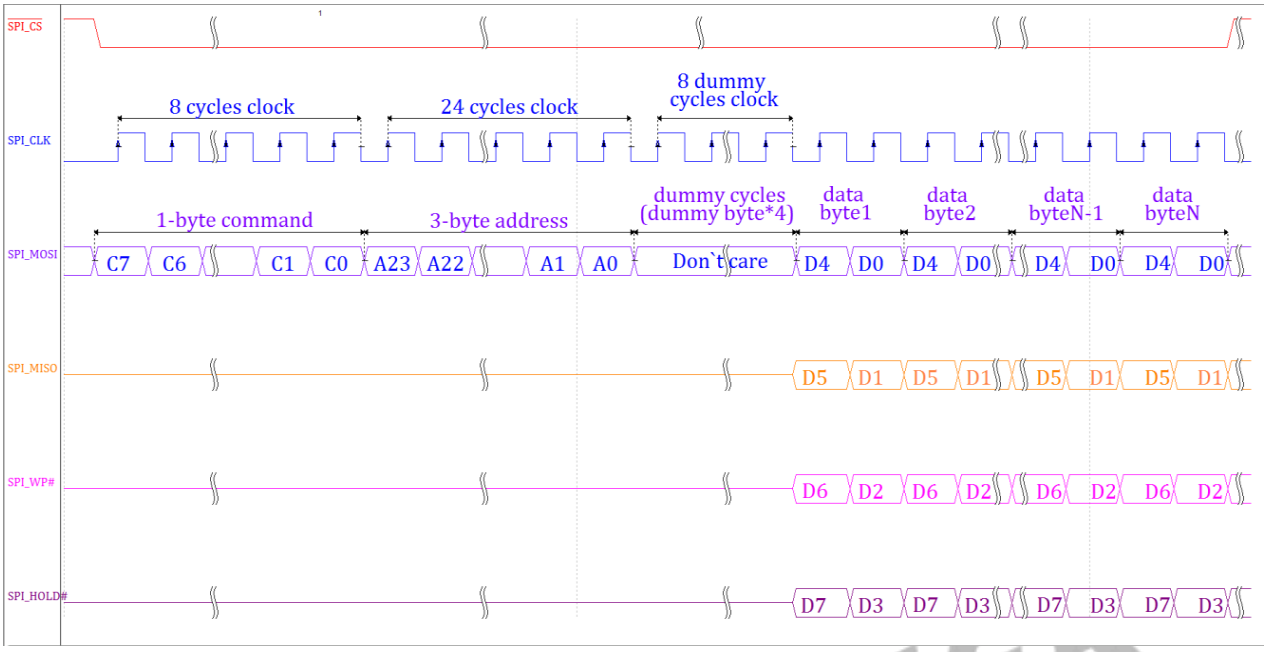


In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

10.4.3.8 SPI Quad-Input/Quad-Output Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC[29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#) and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Figure 10-35 SPI Quad-Input/Quad-Output Mode



In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

10.4.3.9 Transmission/Reception Bursts in Master Mode

In SPI master mode, the transmission and reception bursts (byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmission bursts are written in MWTC (bit[23:0]) of the SPI Master Transmit Counter Register. The transmission bursts in single mode before automatically sending dummy bursts are written in STC (bit[23:0]) of the SPI Master Transmit Counter Register. For dummy data, the SPI controller can automatically send before receiving by writing DBC (bit[27:24]) in the SPI Master Transmit Counter Register. If users do not use the SPI controller to send dummy data automatically, then the dummy bursts are used as the transmission counters to write together in MWTC (bit[23:0]) of the SPI Master Transmit Counter Register. In master mode, the total burst numbers are written in MBC (bit[23:0]) of the SPI Master Transmit Counter Register. When all transmission and reception bursts are transferred, the SPI controller will send a completed interrupt, at the same time, the SPI controller will clear DBC, MWTC, and MBC.

10.4.3.10 SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz–100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in the master mode. The SPI clock is selected from different clock sources, the SPI must configure different work mode. There are three work modes: normal sample mode, delay half-cycle sample mode, delay one-cycle sample mode. Delay half-cycle sample mode is the default mode of the SPI controller. When the SPI runs at 40 MHz or below 40 MHz, the SPI can work at normal sample mode or delay half-cycle sample mode. When the SPI runs over 80 MHz, setting the SDC bit in the SPI Transfer Control Register to '1' makes the internal read sample point with a half-cycle delay of SPI_CLK, which is used in high

speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. The following tables show the different configurations of the SPI sample mode.

Table 10-15 SPI Old Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24 MHz
delay half cycle sample	0	0	<=40 MHz
delay one cycle sample	0	1	>=80 MHz

CAUTION

The remaining spectrum is not recommended. Because when the output delay of SPI flash (refer to the datasheet of the manufactures for the specific delay time) is the same with the half-cycle time of SPI working clock, the variable edge of the output data for the device bumps into the clock sampling edge of the controller, so setting 1 cycle of sampling delay would cause stability problem.

Table 10-16 SPI New Sample Mode

SPI Sample Mode	SDM (bit13)	SDC (bit11)	SDC1 (bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

10.4.3.11 DBI 3-Line Interface Writing and Reading Timing

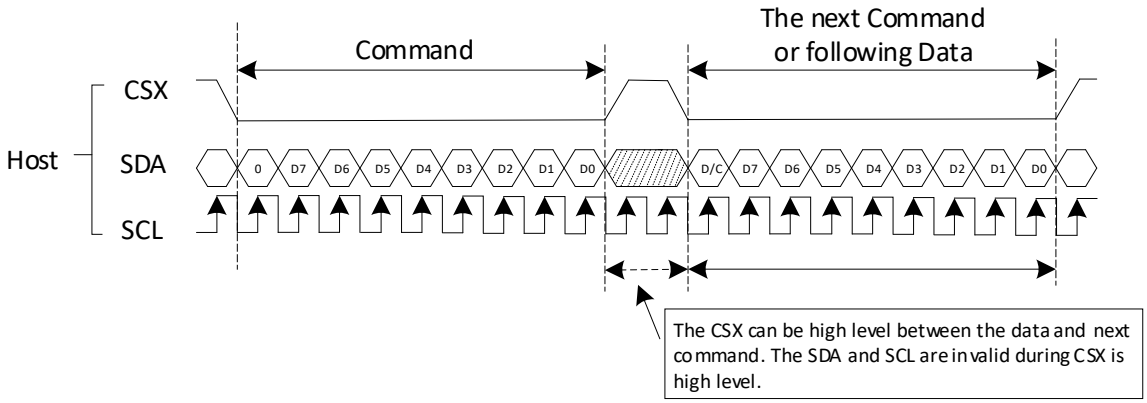
The 3-line DBI Interface I contains CSX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 3-line DBI Interface II contains CSX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

Since the 3-line display bus mode has no Data/Command data line indicating whether Data or Command is currently being transmitted, an extra bit is added to the data-stream before MSB to indicate whether Data or Command is currently being transmitted. (0: Command, 1: Data)

The following figure shows the writing operation format of 3-line DBI Interface I and Interface II.

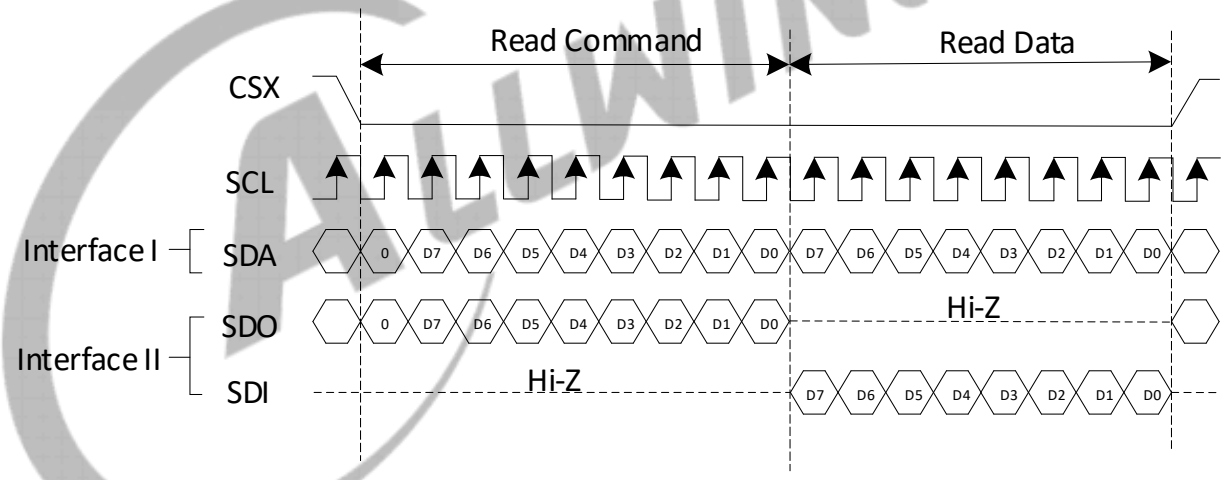
Figure 10-36 DBI 3-Line Display Bus Serial Interface Writing Operation Format



The 3-line DBI Interface I uses the SDA port as bidirectional data input and output port. There are only three cases of data reading volume, 8bits/24bits/32bits, and the first data sampled is high.

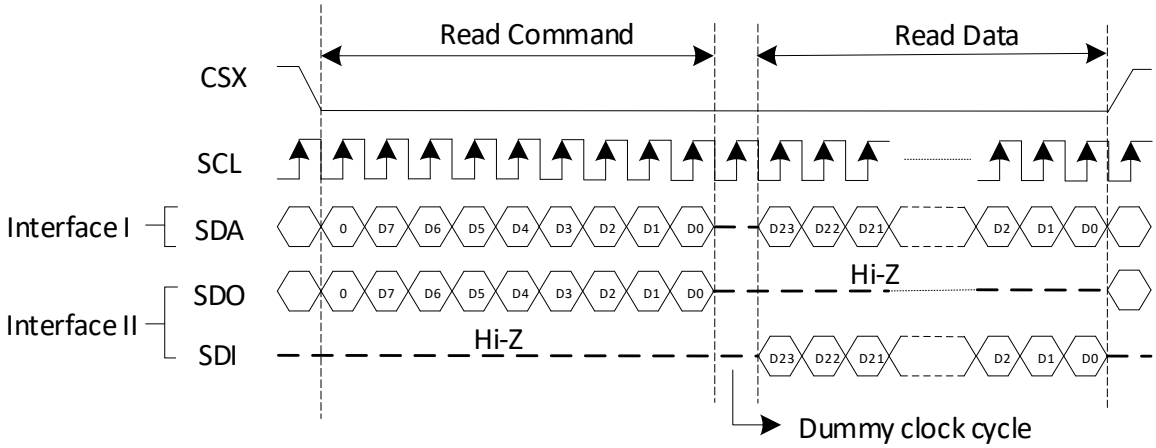
The following figure shows the 8 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read immediately with on dummy period.

Figure 10-37 DBI 3-Line Display Bus Serial Interface 8-bit Reading Operation Format



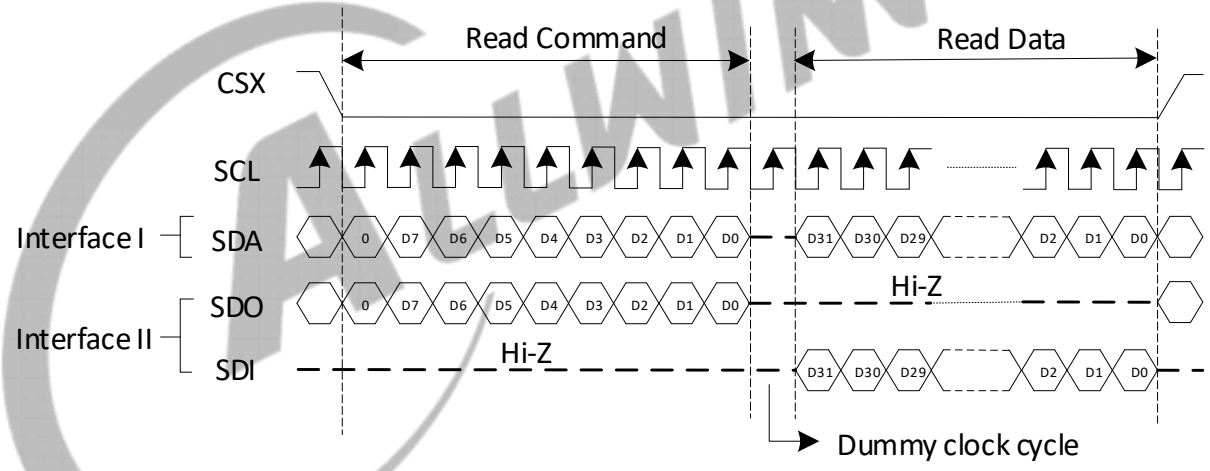
The following figure shows the 24 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read after waiting for the dummy clock cycle.

Figure 10-38 DBI 3-Line Display Bus Serial Interface 24-bit Reading Operation Format



The following figure shows the 32 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read after waiting for the dummy clock cycle.

Figure 10-39 DBI 3-Line Display Bus Serial Interface 32-bit Reading Operation Format



10.4.3.12 DBI 4-Line Interface Writing and Reading Timing

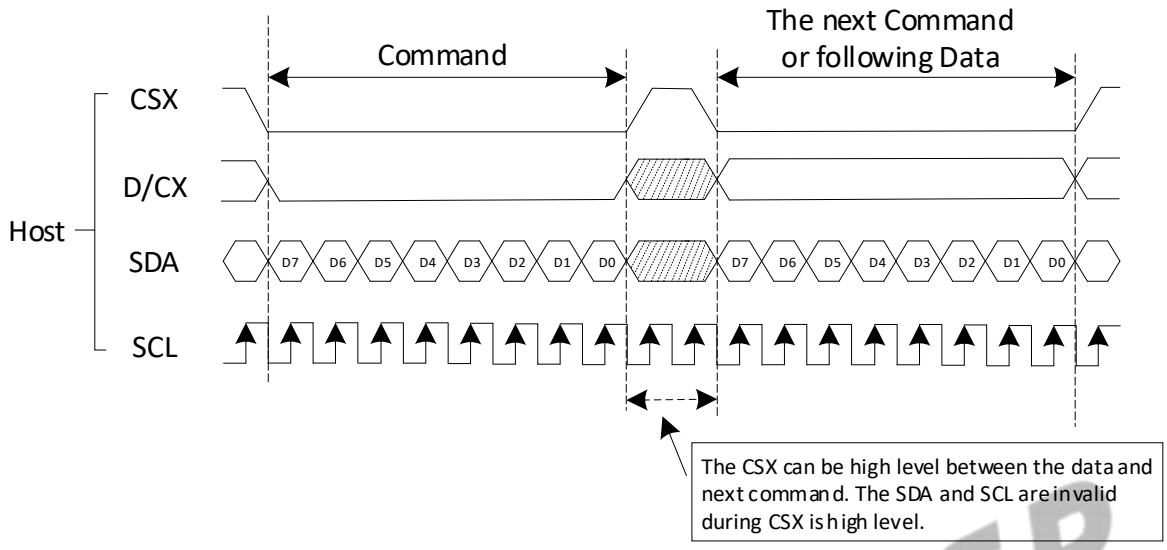
The 4-line DBI Interface I contains CSX, D/CX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 4-line DBI Interface II contains CSX, D/CX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

Since the 4-line display bus mode has a Data/Command data line indicating whether Data or Command is currently being transmitted (0: Command, 1: Data). So there is no need to add an extra bit to data-stream before MSB like the 3-line DBI.

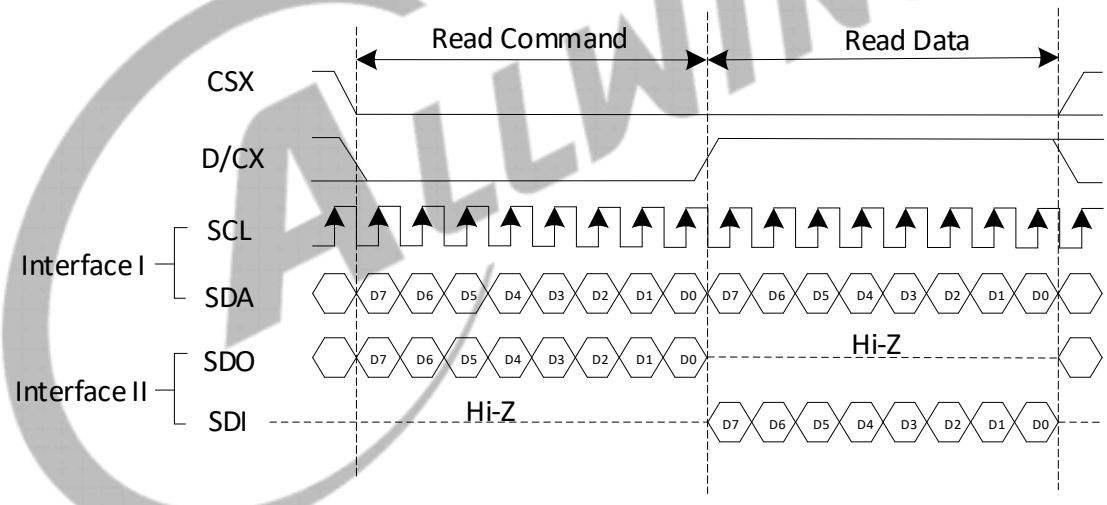
The following figure shows the writing operation format of 4-line DBI Interface I and Interface II.

Figure 10-40 DBI 4-Line Display Bus Serial Interface Writing Operation Format



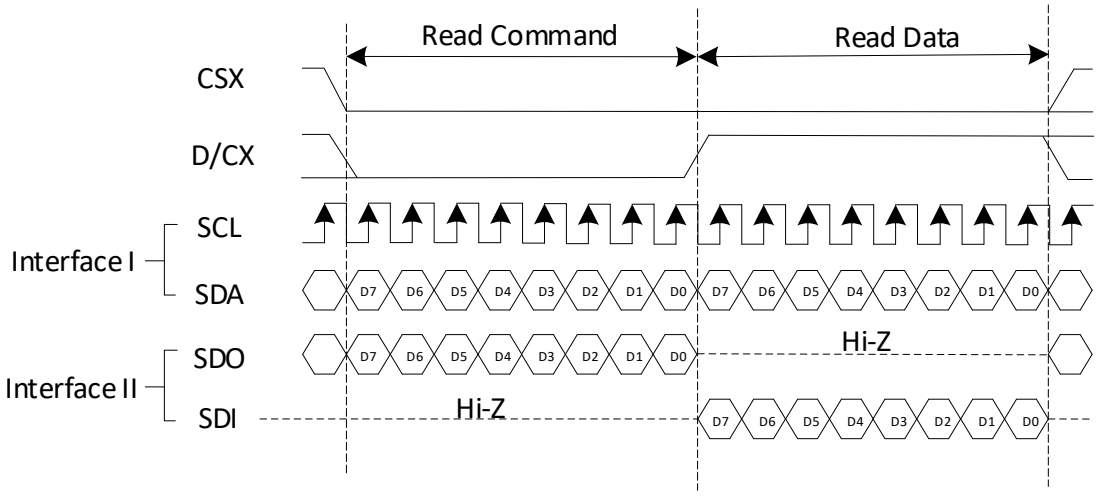
The following figure shows the 8 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 10-41 DBI 4-Line Display Bus Serial Interface 8-bit Reading Operation Format



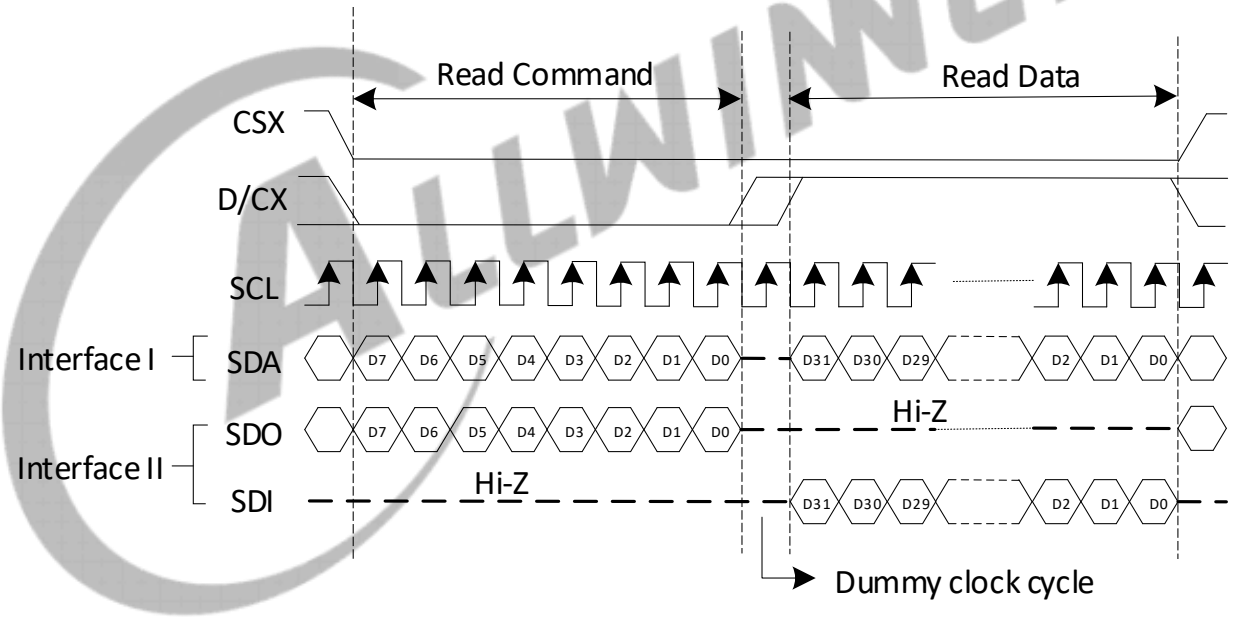
The following figure shows the 24 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 10-42 DBI 4-Line Display Bus Serial Interface 24-bit Reading Operation Format



The following figure shows the 32 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 10-43 DBI 4-Line Display Bus Serial Interface 32-bit Reading Operation Format



10.4.3.13 DBI 3-Line Interface Transmit Video Format

Figure 10-44 RGB111 3-Line Interface Transmit Video Format

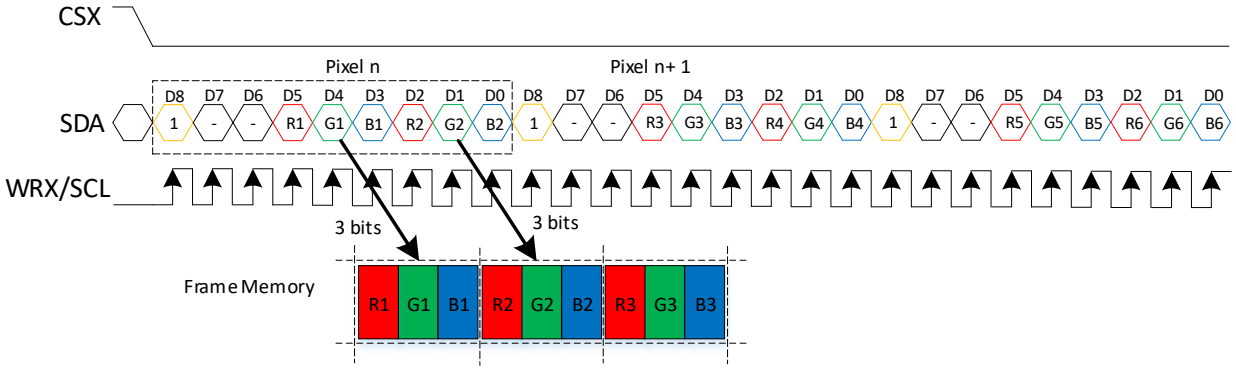
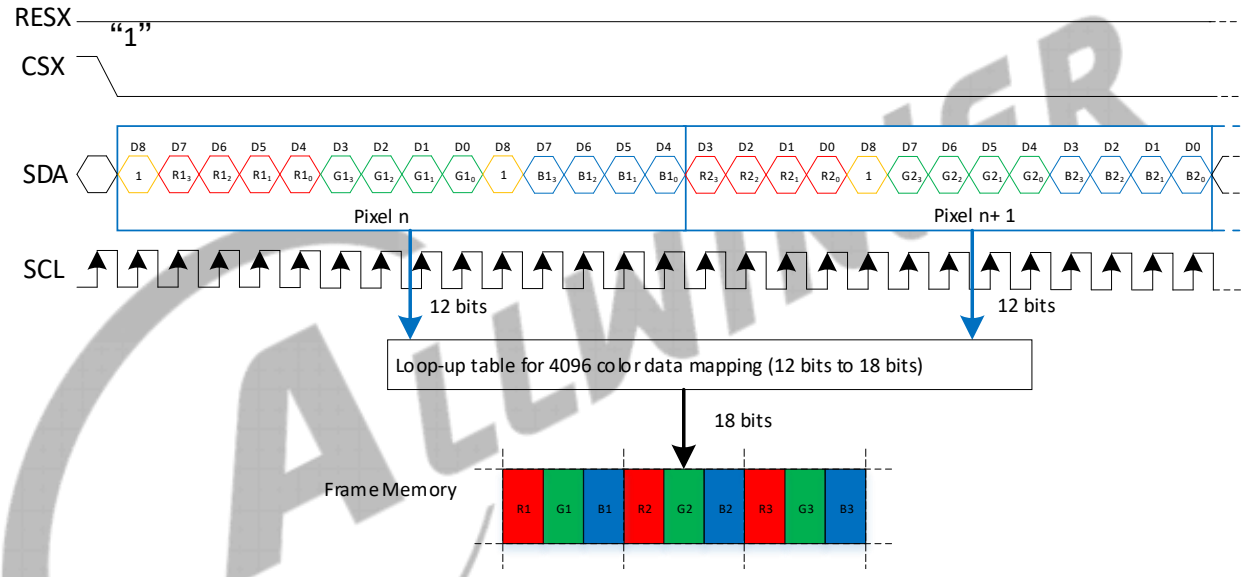
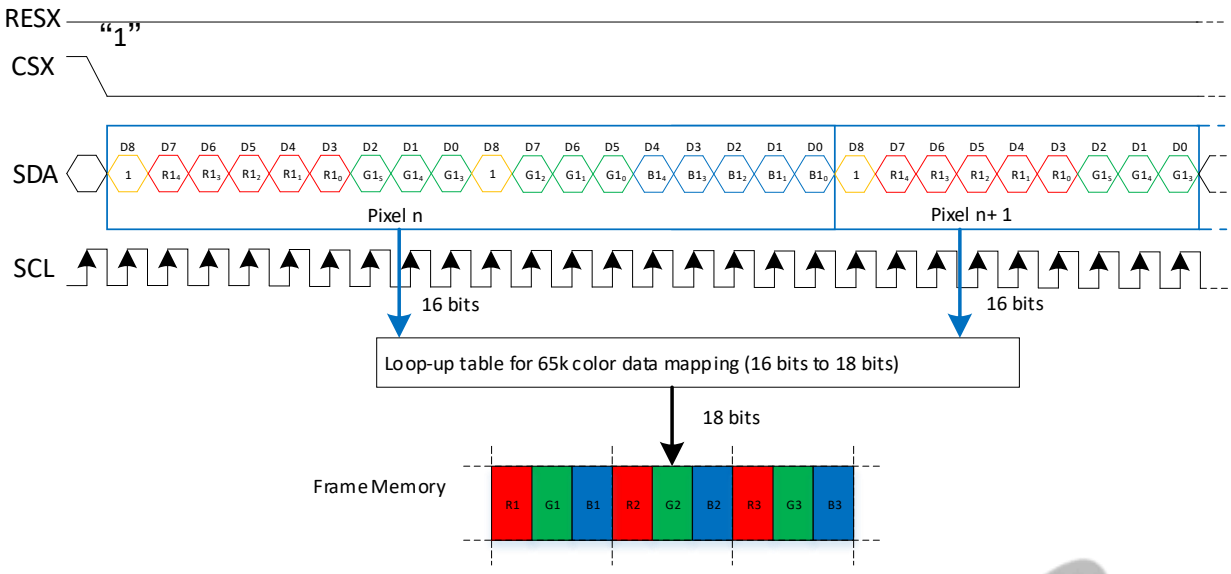


Figure 10-45 RGB444 3-Line Interface Transmit Video Format



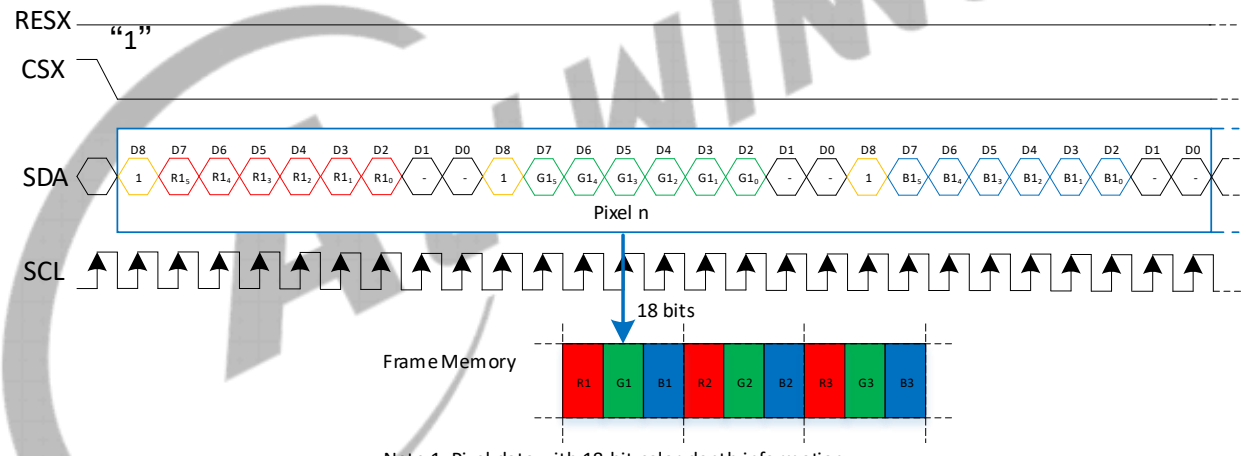
Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-46 RGB565 3-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-47 RGB666 3-Line Interface Transmit Video Format



Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

10.4.3.14 DBI 4-Line Interface Transmit Video Format

Figure 10-48 RGB111 4-Line Interface Transmit Video Format

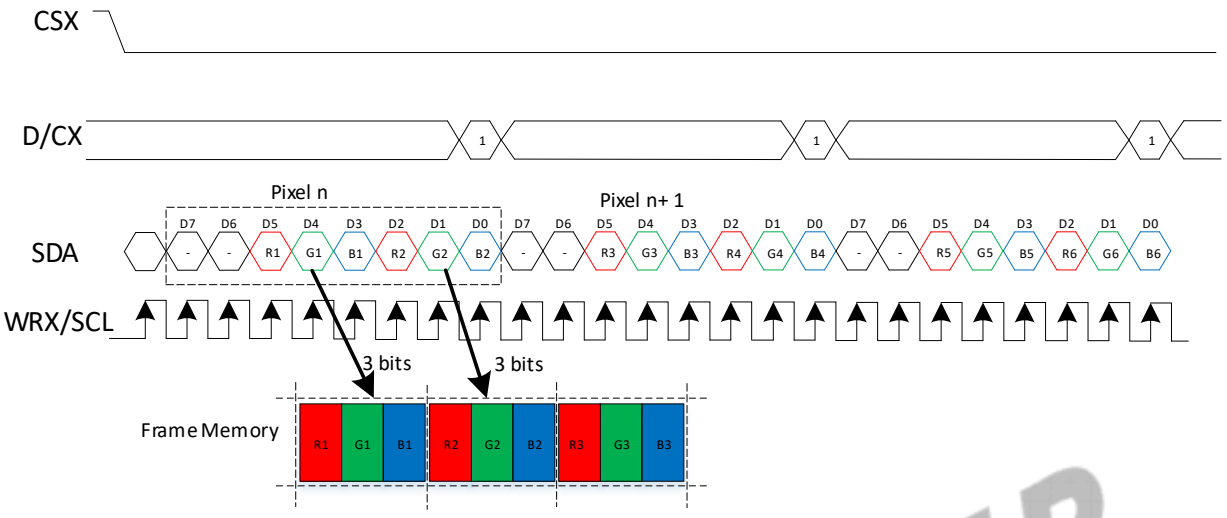
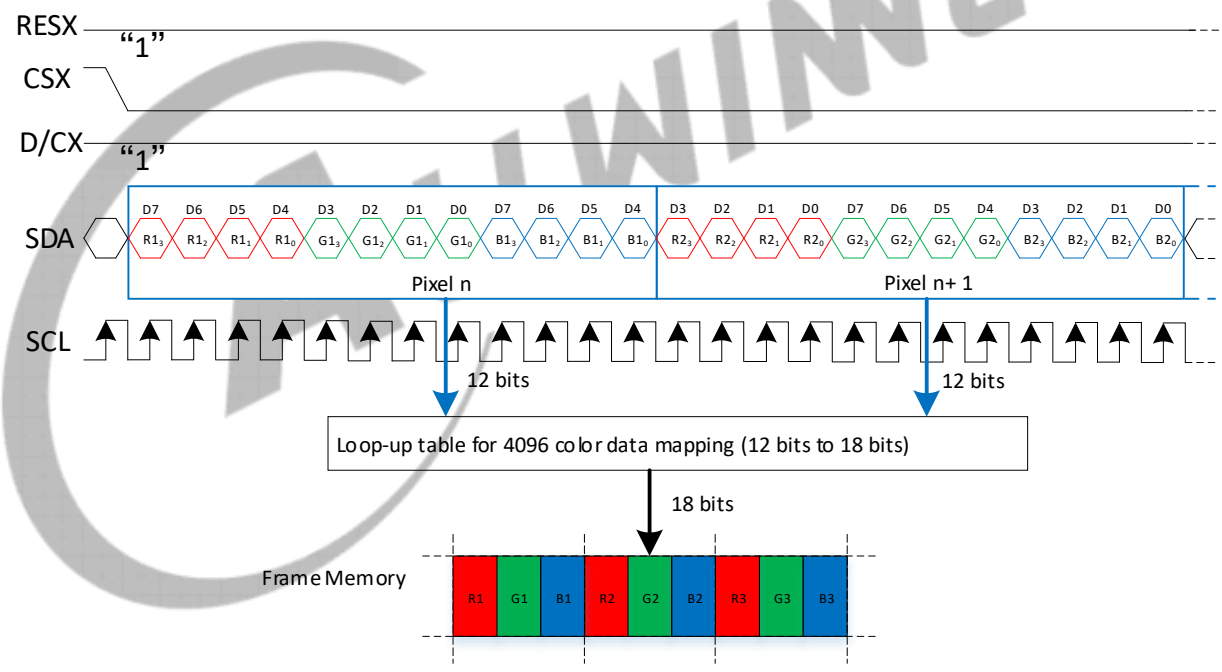
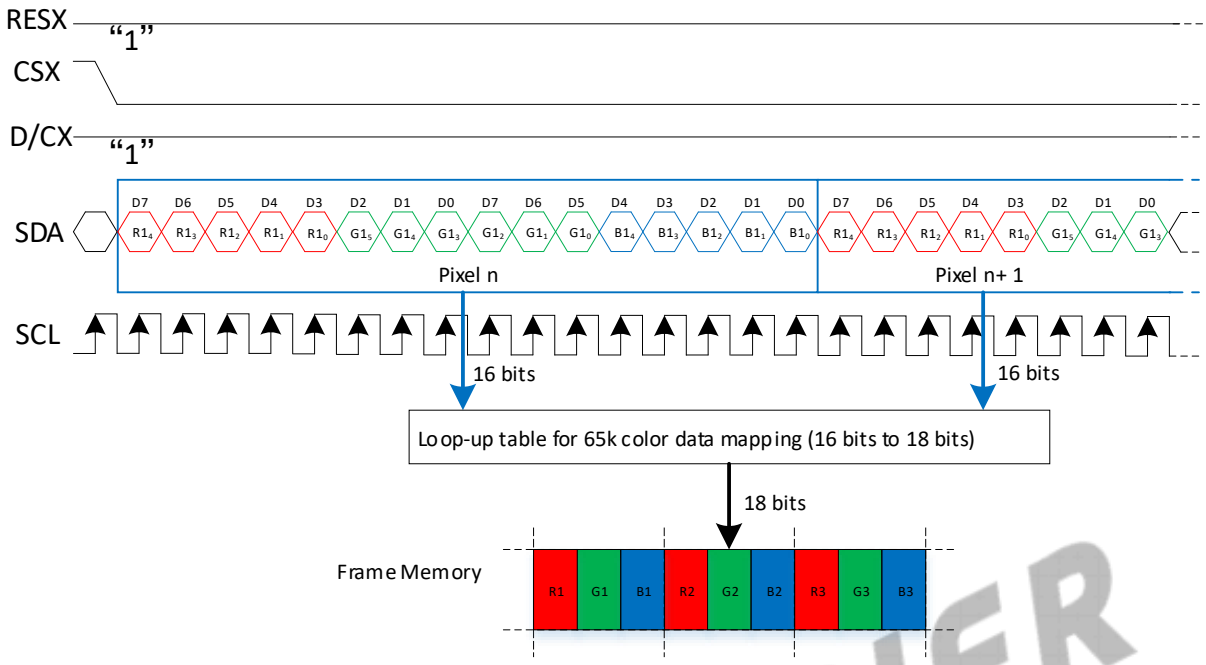


Figure 10-49 RGB444 4-Line Interface Transmit Video Format



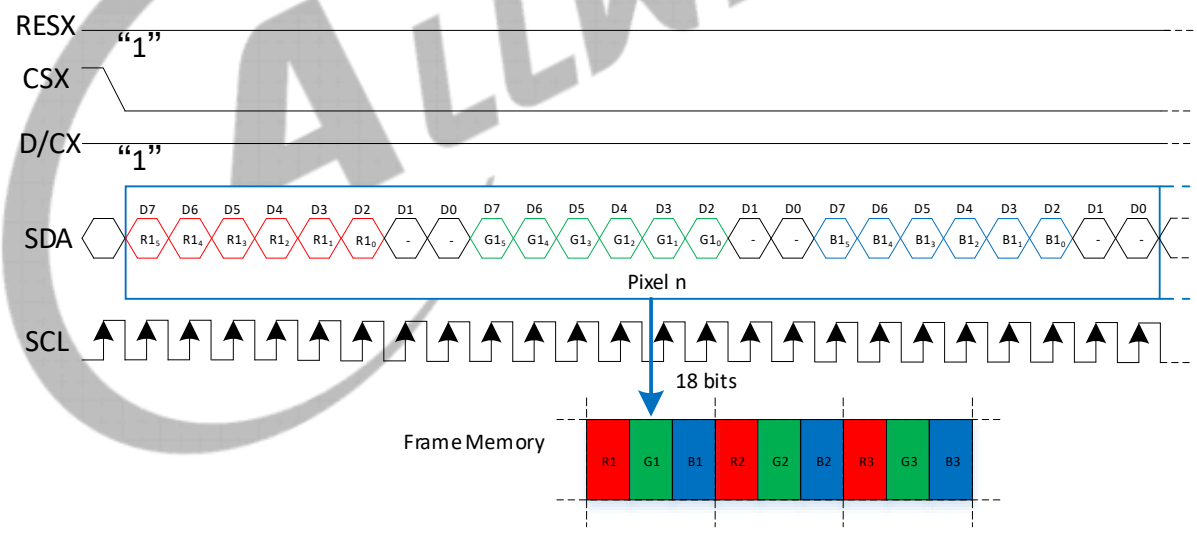
Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-50 RGB565 4-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-51 RGB666 4-Line Interface Transmit Video Format

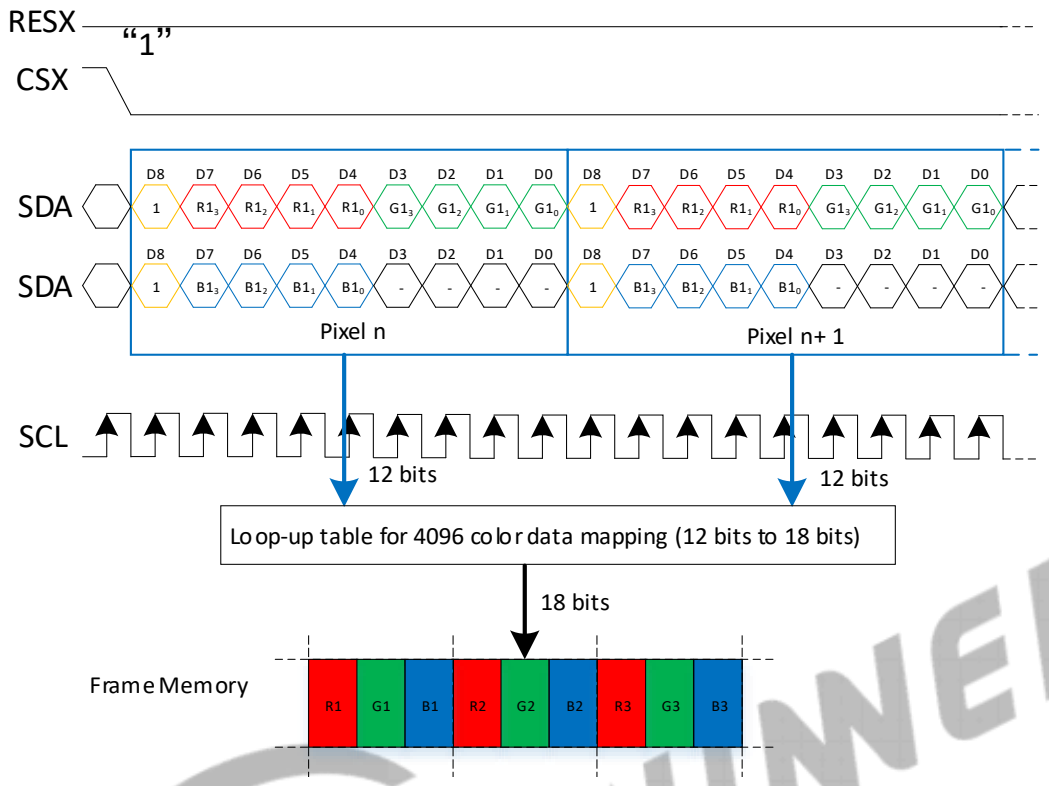


Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

10.4.3.15 DBI 2 Data Lane Interface Transmit Video Format

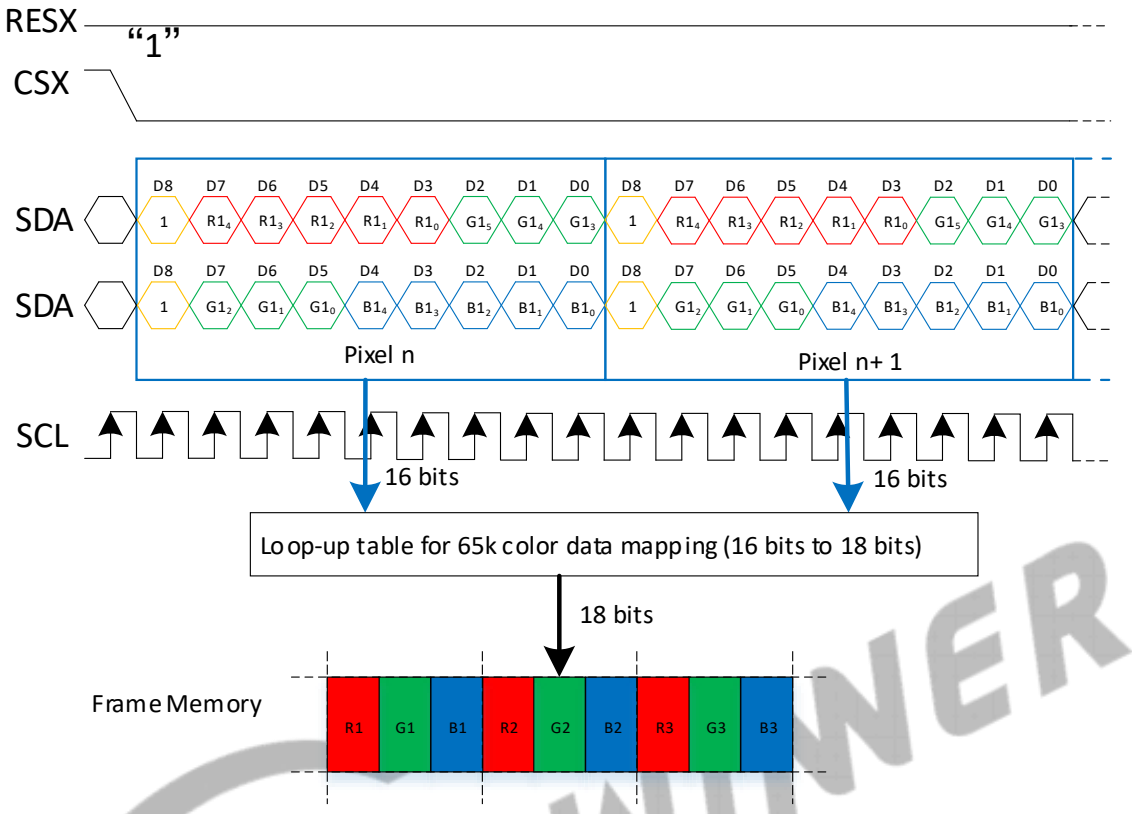
For RGB444:

Figure 10-52 RGB444 2 Data Lane Interface Transmit Video Format



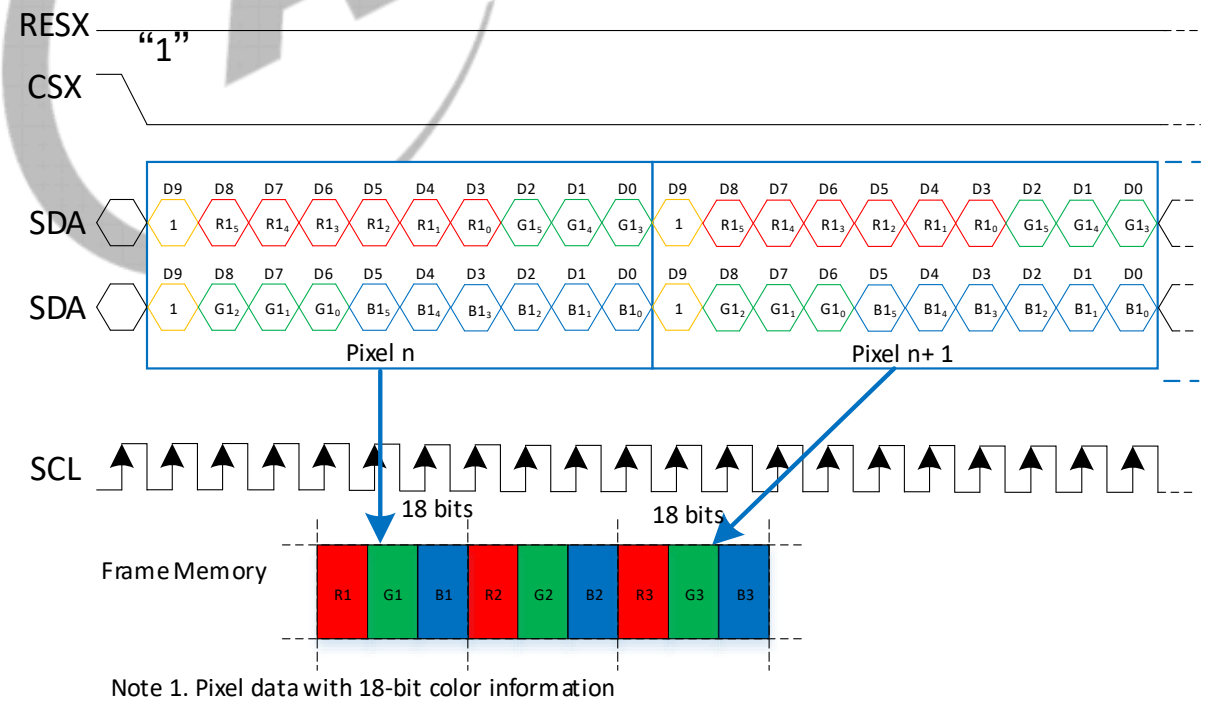
Note 1. Pixel data with 12-bit color information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-53 RGB565 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 16-bit color information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-54 RGB666 2 Data Lane Interface Transmit Video Format 0



Note 1. Pixel data with 18-bit color information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 10-55 RGB666 2 Data Lane Interface Transmit Video Format 1 (ilitek)

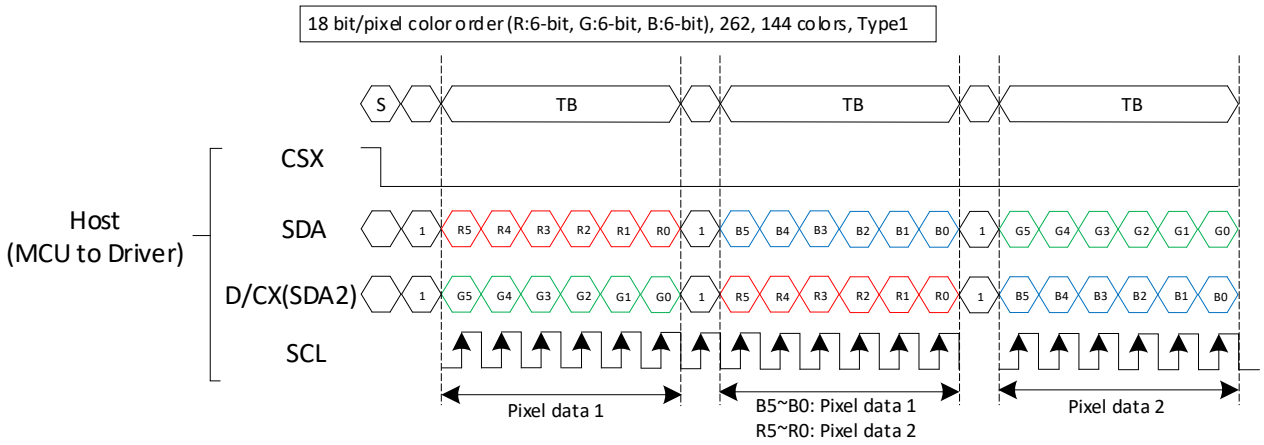


Figure 10-56 RGB666 2 Data Lane Interface Transmit Video Format 2 (New vision)

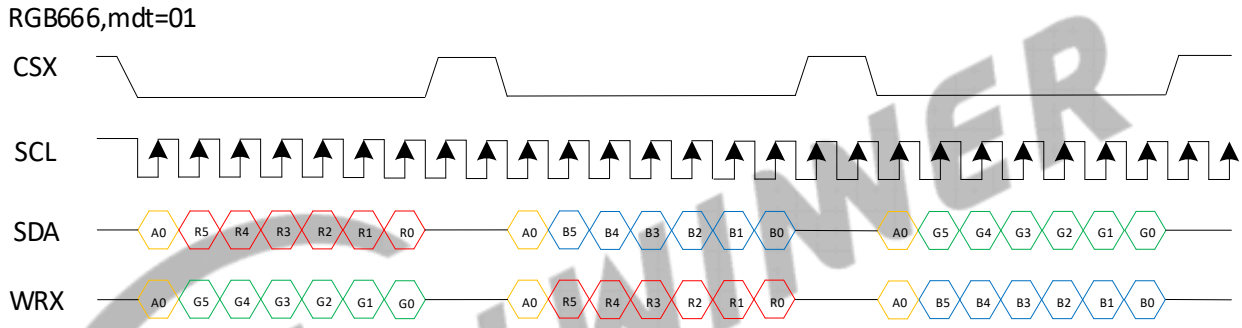
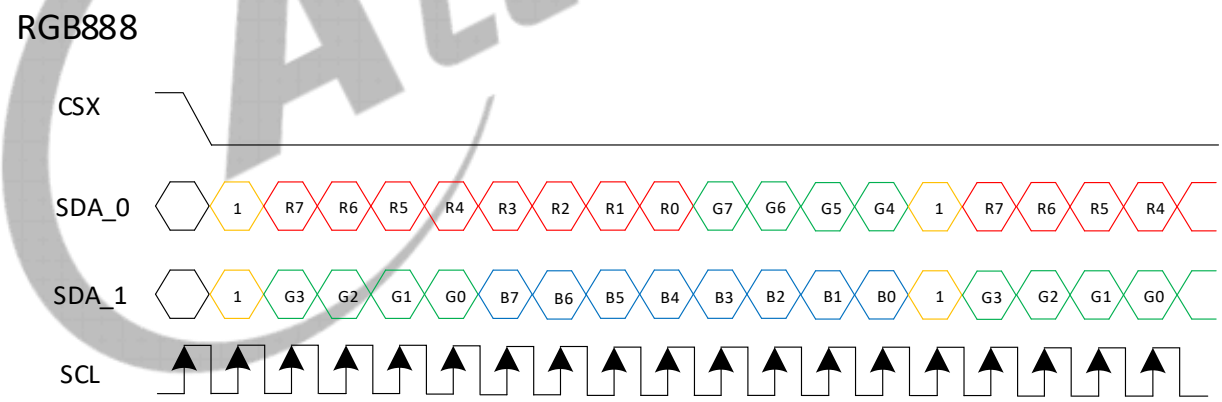


Figure 10-57 RGB888 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 24-bit color information
Note 2. The most significant bits are: R7, G7 and B7
Note 3. The least significant bits are: R0, G0 and B0

10.4.4 Programming Guidelines

10.4.4.1 Writing/Reading Data Process Using SPI Mode

The SPI transfers serial data between the processor and the external device. CPU and DMA are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX channel and RX channel. The TX channel

has the path from TX FIFO to the external device. The RX channel has the path from the external device to RX FIFO.

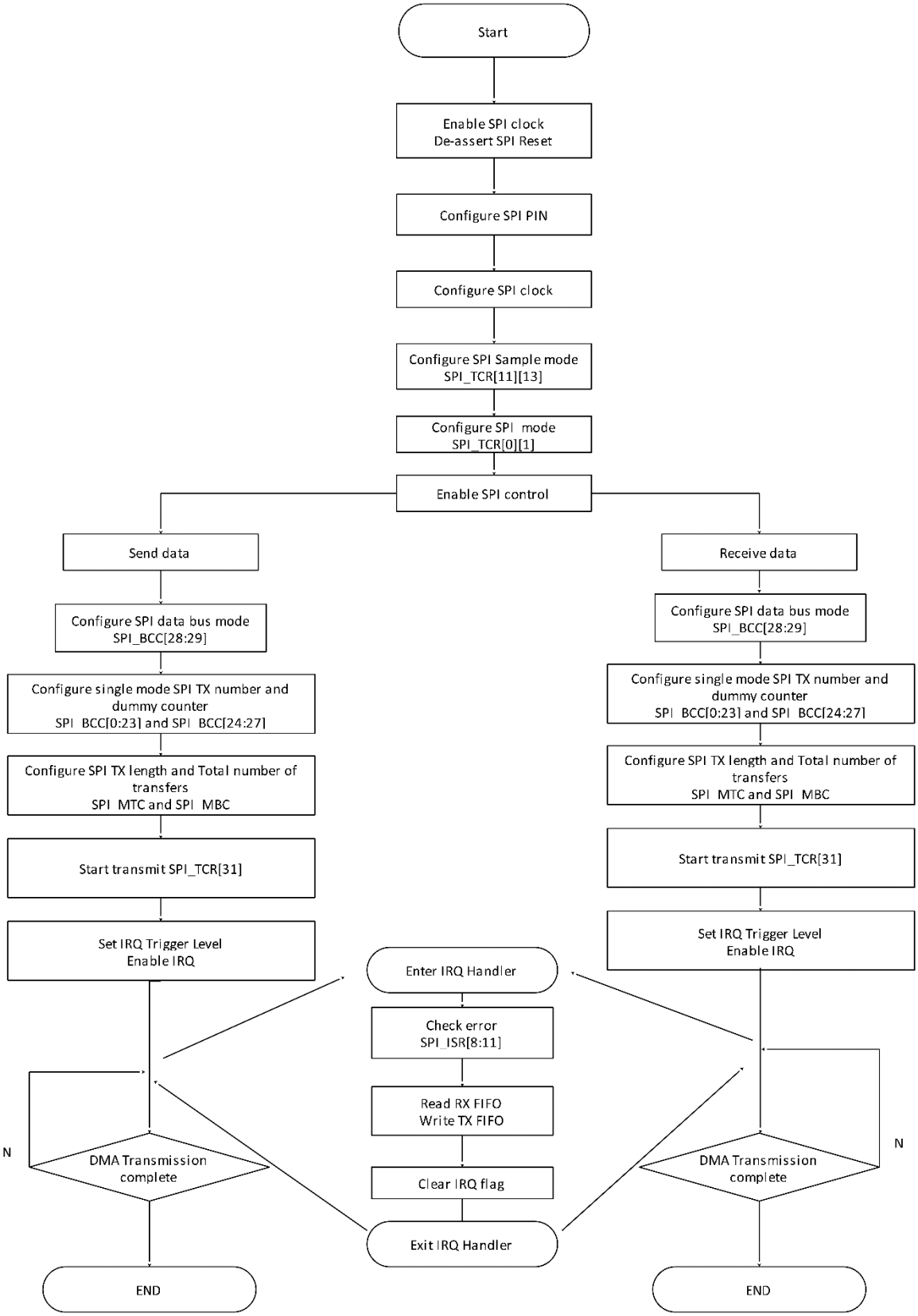
Write Data: CPU or DMA must write data on the SPI_TXD register, the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor at the end of each transfer.

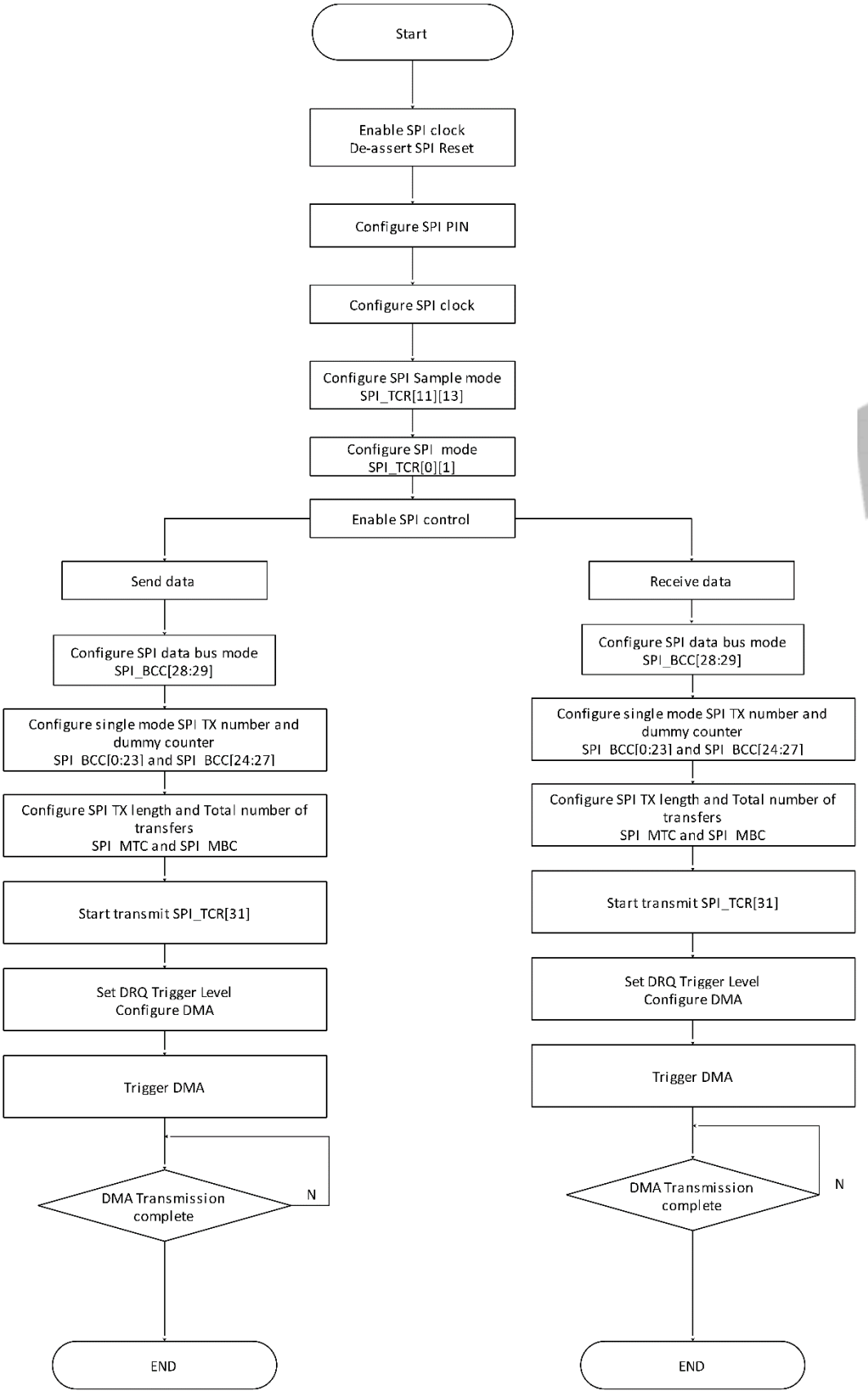
CPU Mode

Figure 10-58 SPI Write/Read Data in CPU Mode



DMA Mode

Figure 10-59 SPI Write/Read Data in DMA Mode



10.4.4.2 Calibrate Delay Chain Using SPI Mode

The SPI has one delay chain which is used to generate delay to make proper timing between the internal SPI clock signal and data signals. Delay chain is made up of 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

7. Enable SPI. To calibrate the delay chain by operation registers in SPI, the SPI must be enabled through AHB reset and AHB clock gating control registers.
8. Configure a proper clock for SPI. The calibration delay chain is based on the clock for SPI from CCU.
9. Set proper initial delay value. Write 0xA0 to the SPI Sample Delay Control Register to set initial delay value 0x20 to delay chain. Then write 0x0 to the SPI Sample Delay Control Register to clear this value.
10. Write 0x8000 to the SPI Sample Delay Control Register to start to calibrate the delay chain.
11. Wait until the flag (Bit14 in the SPI Sample Delay Control Register) of calibration done is set. The number of delay cells is shown at Bit[13:8] in SPI Sample Delay Control Register. The delay time generated by these delay cells is equal to the cycle of SPI's clock nearly. This value is the result of calibration.
12. Calculate the delay time of one delay cell according to the cycle of the SPI clock and the result of calibration.

10.4.4.3 Transmitting Write Command Using DBI Mode

13. Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.
14. Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.
15. Configure the DBI_CTL_0 (0x0100).
    c) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.
    d) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.
    e) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.
    f) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.
    g) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.
    h) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.
    i) The remaining values of the DBI_CTL_0 register remain the default value.
16. Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.
17. DMA Path: Configure the SPI_FCR register (0x0018).
    j) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

k) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

18. Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.
19. Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

10.4.4.4 Transmitting Parameter Using DBI Mode

20. Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.
21. Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.
22. Configure the DBI_CTL_0 register (0x0100).

    l) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

    m) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

    n) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

    o) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

    p) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

    q) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

    r) The remaining values of the DBI_CTL_0 register remain the default value.

23. Set DBI_CTL_1[DCX_DATA] (bit22) to 1 to send the parameter.
24. DMA Path: Configure the SPI_FCR register (0x0018).

    s) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

    t) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

    CPU Path: Write the command to be sent to the 0x200 address.

25. Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.
26. Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

10.4.4.5 Transmitting Video Using DBI Mode

Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

If the data is from the CPU path, the controller writes the command to be sent to the 0x0200 address by the AHB bus.

If the data is from the DMA path, configure DBI_CTL_1[DBI_FIFO_DRQ_EN] (bit15) to 1 and DBI_CTL_1[TX_TRIG_LEVEL] (bit[14:8]) to 64, which indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 64.

Software Trigger Mode

The software enables DBI_en_trigger when the edge interrupt of TE is detected.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt and stops transmitting data.

Wait for the edge interrupt of TE, the software needs to enable DBI_en_trigger, in circulation.

The operation process is as follows.

27. Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.
28. Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 1 to select the software trigger mode.
29. Configure the DBI_CTL_0 register (0x0100).
    u) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.
    v) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.
    w) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.
    x) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.
    y) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111//444/565/666/888.
    z) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.
    aa) The remaining values of the DBI_CTL_0 register remain the default value.
30. Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.
31. Configure DBI_Video_Size (0x110) according to the sent image size.
32. Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.
33. Detect the TE interrupt of the DBI_INT (0x0120) register.
34. Configure DBI_CTL_1[DBI_soft_trigger] to 1.

Timer Trigger Mode

The software configures timer_en to enable timer counting, and when the counter reaches the specified value, the DBI_EN automatically can be enabled to start transmitting data.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt, and stops transmitting data.

The timer starts counting again. When the counter reaches the specified value, the controller automatically enables DBI_EN, and in circulation until the software turns off the timer_en.

The operation process is as follows.

35. Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.
36. Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 2 to select the timer trigger mode.
37. Configure the DBI_CTL_0 register (0x0100).
    bb) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.
    cc) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.
    dd) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.
    ee) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.
    ff) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.
    gg) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.
    hh) The remaining values of the DBI_CTL_0 register remain the default value.
38. Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.
39. Configure DBI_Video_Size (0x110) to transmit the image size.
40. Configure the related parameter of DBI_Timer (0x10C).

TE Trigger Mode

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN automatically can be enabled to start transmitting data.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt, and stops transmitting data.

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN automatically can be enabled to start transmitting data until the software shuts down TE_EN or the screen no longer sends TE signals.

The operation process is as follows.

41. Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.
42. Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 3 to select the TE Configure the DBI_CTL_0 register (0x0100).
43. Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.
    ii) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

jj) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

kk) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

ll) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

mm) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

nn) The remaining values of the DBI_CTL_0 register remain the default value.

44. Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.
45. Configure DBI_Video_Size (0x0110) to transmit the image size.
46. Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

10.4.4.6 Transmitting Read Command and Read Data Using DBI Mode

47. Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.
48. Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0.
49. Configure the DBI_CTL_0 register (0x0100).

oo) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the reading command.

pp) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

qq) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

rr) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0.

ss) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

tt) The remaining values of the DBI_CTL_0 register remain the default value.

50. Configure the DBI_CTL_1 register (0x0104).

uu) Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

vv) Configure DBI_CTL_1[Read_MSB_First] (bit20) to select whether the first bit of the read data is the highest or lowest bit of data.

ww) Configure DBI_CTL_1[Read Data Number of Bytes] to set the byte number to be read.

xx) Configure DBI_CTL_1[Read Command Dummy Cycles] to set the dummy cycle between the read command and the read data, when the dummy cycle is complete, the data starts to be sampled.

51. DMA Path: Configure the SPI_FCR register (0x0018).

yy) Set SPI_FCR[RF_DRQ_EN] (bit8) to 1 to enable RXFIFO DMA.

zz) Set SPI_FCR[RX_TRIG_LEVEL] (bit[7:0]) to 32, which indicates the controller requests receiving data from DMA if the data of the RX FIFO is greater than 64.

CPU Path: Read data in RX FIFO from the 0x0300 address.

52. Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting command.

53. Wait until DBI_INT[RD_DONE_INT] is 1. It indicates that the data is read completely.

10.4.5 Register List

Module Name	Base Address	Comments
SPI_DBI	0x0402 6000	SPI_DBI controller

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter register
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0044	SPI Bit-Aligned CLOCK Configuration Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
DBI_CTL_0	0x0100	DBI Control Register 0
DBI_CTL_1	0x0104	DBI Control Register 1
DBI_CTL_2	0x0108	DBI Control Register 2
DBI_TIMER	0x010C	DBI Timer Control Register
DBI_VIDEO_SIZE	0x0110	DBI Video Size Register
DBI_INT	0x0120	DBI Interrupt Register
DBI_DEBUG_0	0x0124	DBI DEBUG Register 0
DBI_DEBUG_1	0x0128	DBI DEBUG Register 1
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register

10.4.6 Register Description

10.4.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset:0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes. Writing '0' to this bit has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 0: Normal operation, ignore RXFIFO status 1: Stop transmit data when RXFIFO full Cannot be written when XCH=1.
6:5	/	/	/
4	R/W	0x0	DBI EN DBI Module Enable Control 0: Disable 1: Enable
3	R/W	0x0	SPI_DBI_MODE_SEL DBI Working Mode Select 0: SPI MODE 1: DBI MODE
2	R/W	0x0	MODE_SELEC Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing Cannot be written when XCH=1.
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave mode 1: Master mode Cannot be written when XCH=1.
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable After transforming from bit_mode to byte_mode, it must enable the SPI module again.

10.4.6.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode, it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will auto-clear after finishing the bursts transfer specified by BC. Writing “1” to SRST will also clear this bit. Writing ‘0’ to this bit has no effect. Cannot be written when XCH=1.
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to ‘1’ to make the internal read sample point with a delay of half-cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. 0: Normal operation, do not delay the internal read sample point 1: Delay the internal read sample point Cannot be written when XCH=1.
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to "1" to make the data that should be sent with a delay of half-cycle of SPI_CLK in dual IO mode for SPI mode 0. Cannot be written when XCH=1.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay sample mode 1: Normal sample mode In normal sample mode, the SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, the SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode. Cannot be written when XCH=1.

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first. The upper bits are transmitted first. 1: LSB first. The lower bits are transmitted first. Cannot be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half-cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. 0: Normal operation, do not delay the internal read sample point 1: Delay the internal read sample point Cannot be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select rapid mode for high speed write. 0: Normal write mode 1: Rapid write mode Cannot be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Cannot be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode, it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in the BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during the dummy burst period. The burst number is specified by TC. Cannot be written when XCH=1.
7	R/W	0x1	SS_LEVEL SPI Chip Select Level When control SS signal manually (SS_OWNER (SPI_TCR[6])==1), set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high Cannot be written when XCH=1.

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, the controller sends the SS signal automatically with data together. When this bit is set to 1, the software must manually write SS_LEVEL (SPI_TCR[7]) to 1 or 0 to control the level of the SS signal. 0: SPI controller 1: Software Cannot be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Cannot be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output waveform for the SPI_SSx signal. Only valid when SS_OWNER (SPI_TCR[6])= 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Cannot be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Cannot be written when XCH=1.

10.4.6.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip select signal (SSx) from the valid state to the invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

10.4.6.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from the valid state to the invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC have been exchanged. In other conditions, when set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer completed
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when the TXFIFO is overflowed. Writing 1 to this bit clears it. 0: TXFIFO is not overflowed 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO is underrun. Writing 1 to this bit clears it. 0: RXFIFO is not underrun 1: RXFIFO is underrun
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO is overflowed. Writing 1 to this bit clears it. 0: RXFIFO is not overflowed 1: RXFIFO is overflowed
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set when the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit will be immediately set to 1 if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. The TX_WL is the water level of TXFIFO.
3	/	/	/

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit will be immediately set to 1 if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. The RX_WL is the water level of RXFIFO.

10.4.6.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TXFIFO and auto clear to ‘0’ when completing the reset operation, writing ‘0’ to this bit has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable In normal mode, the TXFIFO can only be read by the SPI controller, writing ‘1’ to this bit will switch the read and write function of TXFIFO to AHB bus. This bit is used to test the TXFIFO, do not set in normal operation, and do not set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing the reset operation, writing '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, the RXFIFO can only be written by the SPI controller, writing '1' to this bit will switch the read and write function of RXFIFO to AHB bus. This bit is used to test the RXFIFO, do not set in normal operation, and do not set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RXFIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RXFIFO Ready Request Trigger Level

10.4.6.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TXFIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TXFIFO Write Buffer Counter These bits indicate the number of words in TXFIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TXFIFO Counter These bits indicate the number of words in TXFIFO 0: 0 byte in TXFIFO 1: 1 byte in TXFIFO … 64: 64 bytes in TXFIFO other: Reserved

Offset: 0x001C			Register Name: SPI_FSR
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R	0x0	RB_WR RXFIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RXFIFO Read Buffer Counter These bits indicate the number of words in RXFIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RXFIFO Counter These bits indicate the number of words in RXFIFO 0: 0 byte in RXFIFO 1: 1 byte in RXFIFO … 64: 64 bytes in RXFIFO other: Reserved

10.4.6.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). These bits control the number of wait states to be inserted before starting dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying the next word data transfer. 0: No wait states inserted n: n SPI_SCLK wait states inserted Cannot be written when XCH=1.
15:0	R/W	0x0	WCC Wait Clock Counter (In master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying the next word data transfer. 0: No wait states inserted n: n SPI_SCLK wait states inserted Cannot be written when XCH=1.

10.4.6.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, it indicates that start sample delay chain calibration. Cannot be written when XCH=1.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it indicates that the sample delay chain calibration is done and the result of calibration is shown in SAMP_DL. Cannot be written when XCH=1.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to the current card clock. The delay time generated by these delay cells is equal to the cycle of the card clock nearly. Generally, it is necessary to do drive delay calibration when the card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set. Cannot be written when XCH=1.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, it indicates that enable sample delay specified at SAMP_DL_SW. Cannot be written when XCH=1.
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between the clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of the card clock, and the input timing requirement of the device. Cannot be written when XCH=1.

10.4.6.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number which includes the TXD, RXD, and dummy burst. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

10.4.6.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy bursts. For saving bus bandwidth, the dummy bursts (all zero bits or all one bits) are sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

10.4.6.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN The Quad mode includes Quad-Input and Quad-Output. 0: Quad mode disable 1: Quad mode enable Cannot be written when XCH=1.

Offset: 0x0038			Register Name: SPI_BCC
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	DRM Master Dual Mode RX Enable It is only valid when Quad_Mode_EN=0. 0: RX uses the single-bit mode 1: RX uses the dual mode Cannot be written when XCH=1.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receiving in dual SPI mode. The data does not care by the device. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in the single mode before automatically sending dummy bursts. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1

10.4.6.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer Writing “1” to this bit will start to transfer serial bits frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto-clear after the bursts transfer completely. Writing ‘0’ to this bit has no effect.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0x0	MSMS Master Sample Standard 0: Delay Sample Mode 1: Standard Sample Mode In Standard Sample Mode, the SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, the SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed It is only valid when Work Mode Select==0x10/0x11.
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when Work Mode Select==0x10/0x11.
23:22	/	/	/
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame (burst) of RX 000000: 0 bit 000001: 1 bit … 100000: 32 bits Other values: reserved It is only valid when Work Mode Select==0x10/0x11, and cannot be written when TCE (SPI_BATC[31])=1.
15:14	/	/	/

Offset: 0x0040			Register Name: SPI_BATCR
Bit	**Read/Write**	**Default/Hex**	**Description**
13:8	R/W	0x00	TX_FEM_LEN Configure the length of serial data frame (burst) of TX 000000: 0 bit 000001: 1 bit … 100000: 32 bits Other values: reserved It is only valid when Work Mode Select==0x10/0x11, and cannot be written when TCE=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, the controller sends the SS signal automatically with data together. When this bit is set to 1, the software must manually write SS_LEVEL (SPI_BATC[7]) to 1 or 0 to control the level of the SS signal. 0: SPI controller 1: Software It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE=1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE=1.
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, cannot be written when TCE=1.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	WMS Work Mode Select 00: Data frame is byte aligned in standard SPI, dual-output/dual input SPI, dual IO SPI, and quad-output/quad-input SPI 01: Reserved 10: Data frame is bit aligned in 3-wire SPI 11: Data frame is bit aligned in standard SPI

10.4.6.13 0x0044 SPI Bit-Aligned Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)). This register is only valid when Work Mode Select==0x10/0x11.

10.4.6.14 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

10.4.6.15 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

10.4.6.16 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: dma_active is low 01: dma_active is high 10: dma_active is controlled by dma_request (DRQ) 11: dma_active is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	SPI_DMA_WAIT Delay Cycles The counts of hold cycles from DMA last signal high to dma_active high

10.4.6.17 0x0100 DBI Control Register 0 (Default Value: 0x0010_0000)

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMDT Command Type 0: Write Command 1: Read Command
30:20	R/W	0x1	WCDC Write Command Dummy Cycles Controls dummy cycles between two write commands Range 1~255 Default Condition: there is a dbi_clk cycle between each command or parameter.
19	R/W	0x0	DAT_SEQ Output Data Sequence 0: MSB First 1: LSB First

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	**Read/Write**	**Default/Hex**	**Description**
18:16	R/W	0x0	RGB_SEQ Output RGB Sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR 110, 111: Reserved
15	R/W	0x0	TRAN_MOD Transmit Mode 0: Command/Parameter 1: Video
14:12	R/W	0x0	DAT_FMT Output Data Format 000: RGB111 001: RGB444 010: RGB565 011: RGB666 100: RGB888 (only for 2 Data Lane Interface) 101~111: Reserved
11	/	/	/
10:8	R/W	0x0	DBI_INTF DBI Interface 000: 3 Line Interface I 001: 3 Line Interface II 010: 4 Line Interface I 011: 4 Line Interface II 100: 2 Data Lane Interface

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	**Read/Write**	**Default/Hex**	**Description**
7:4	R/W	0x0	RGB_FMT RGB_Source_Format When video_source_type is RGB32 (DBI_CTL_0[bit0] = 0) 0000: RGB 0001: RBG 0010: GRB 0011: GBR 0100: BRG 0101: BGR Others: Reserved When video_source_type is RGB16 (DBI_CTL_0[bit0] = 1) 0000: RGB 0001~0100: Reserved 0101: BGR 0110: GRBG_0 {G[5:3]R[4:0]B[4:0]G[2:0]} 0111: GBRG_0 {G[5:3]B[4:0]R[4:0]G[2:0]} 1000: GRBG_1 {G[2:0]R[4:0]B[4:0]G[5:3]} 1001: GBRG_1 {G[2:0]B[4:0]R[4:0]G[5:3]} Others: Reserved
3	R/W	0x0	DUM_VAL Dummy Cycle Value Output Value During Dummy Cycle
2	R/W	0x0	RGB_BO RGB Bit Order 0: Remain the sequence of RGB data 1: Swap the higher bit and the lower bit for each component of DRAM RGB
1	R/W	0x0	ELEMENT_A_POS Element A Position Only for RGB32 Data Format 0: A component is in the bit[31:24] of data source 1: A component is in the bit[7:0] of data source
0	R/W	0x0	VI_SRC_TYPE Video Source Type 0: RGB32 1: RGB16

10.4.6.18 0x0104 DBI Control Register 1 (Default Value: 0x0000_0001)

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	DBI_SOFT_TRG DBI soft trigger It is only available for software trigger mode. Writing '1' to this bit will start DBI TX module and auto clear to '0' when completing start operation, writing '0' to this bit has no effect.
30:29	R/W	0x0	DBI EN MODE SEL DBI Enable Mode Select 00: Always on DBI mode 01: Software trigger mode 10: Timer trigger mode 11: TE trigger mode
28	/	/	/
27:26	R/W	0x0	RGB666_FMT 2 Data Lane RGB666 Format 00: Normal Format 01: Special Format for ILITEK 10: Special Format for New Vision
25	R/W	0x0	DBI_RXCLK_INV DBI rx clock inverse 0: Sample data by using the positive edge of the output clock 1: Sample data by using the negative edge of the output clock
24	R/W	0x0	DBI_CLKO_MOD DBI output clock mode 0: DBI clock always on (DCX Setup/hold equals one clock cycle) 1: DBI clock auto gating (DCX Setup/hold equals to a half clock cycle)
23	R/W	0x0	DBI_CLKO_INV DBI clock output inverse When the bit24 (DBI output clock mode) is 0. 0: The falling edge releases the CSX signal, and the falling edge releases data 1: The rising edge releases the CSX signal, and the rising edge releases data When the bit24 (DBI output clock mode) is 1. 0: The rising edge releases the CSX signal, and the falling edge releases data 1: The falling edge releases the CSX signal, and the rising edge releases data

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	**Read/Write**	**Default/Hex**	**Description**
22	R/W	0x0	DCX_DATA DCX Data Value 0: DCX Value equal to 0 1: DCX Value equal to 1
21	R/W	0x0	RGB 16 Data Source Select RGB 16 Data Source Select 0: Pixel1 is stored in the higher bit of address, and Pixel0 is stored in the lower bit of address 1: Pixel0 is stored in the higher bit of address, and Pixel1 is stored in the lower bit of address
20	R/W	0x0	RDAT_LSB Bit Order of Read Data 0: A reading data is the higher bit 1: A reading data is the lower bit
19:16	/	/	/
15:8	R/W	0x0	RCDC Read Command Dummy Cycles The dummy cycle between the read command and read data Reading 1-byte (8 bits) data has not dummy cycle.
7:0	R/W	0x1	RDBN Read Data Number of Bytes Sample Bytes data based on configuration.

10.4.6.19 0x0108 DBI Control Register 2 (Default Value: 0x0000_4000)

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
15	R/W	0x0	DBI_FIFO_DRQ_EN DBI FIFO DMA Request Enable 0: Disable 1: Enable
14:8	R/W	0x40	DBI_TRIG_LEVEL DBI FIFO Empty Request Trigger Level
7	/	/	/
6	R/W	0x0	DBI_SDI_OUT_SEL DBI SDI PIN Output Select The signal is used with the DBI SDI PIN Function Sel bit. 0: Output WRX (When DBI DCX PIN Function Sel = 0, the SDI pin outputs data) 1: Output DCX

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	DBI_DCX_SEL DBI DCX PIN Function Select 0: DBI DCX Function 1: WRX (2 Data Lane Interface)
4:3	R/W	0x0	DBI_SDI_SEL DBI SDI PIN Function Select 00: DBI_SDI (Interface II) 01: DBI_TE 10: DBI_DCX 11: Reserved
2	R/W	0x0	TE_DBC_SEL TE debounce function select 0: debounce 1: no-debounce
1	R/W	0x0	TE_TRIG_SEL TE edge trigger select 0: TE rising edge 1: TE falling edge
0	R/W	0x0	TE_EN TE enable 0: TE Disable 1: TE Enable

10.4.6.20 0x010C DBI Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: DBI_Timer
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DBI_TM_EN DBI Timer Enable 0: Enable 1: Disable
30:0	R/W	0x0	DBI Timer Value It sets the time interval between sending data twice, which is frame blanking. It is used to set the time at which the interrupt of the DBI Timer is triggered. When the Timer_EN is 1, the timer starts to count (the clock of the counting is SCLK), and the counter reaches the target value to trigger the Timer_INT of DBI, the data will start to send in series. Note: Do not count when sending the series data.

10.4.6.21 0x0110 DBI Video Size Register (Default Value: 0x01E0_0140)

Offset: 0x0110			Register Name: DBI_Video_Size
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x1E0	V_SIZE It is used to generate the Frame int.
15:11	/	/	/
10:0	R/W	0x140	H_SIZE It is used to generate the Line int.

10.4.6.22 0x0120 DBI Interrupt Register (Default Value: 0x0000_4000)

Offset: 0x0120			Register Name: DBI_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W1C	0x1	DBI_FIFO_EMPTY_INT DBI FIFO Empty Interrupt Status 0: DBI_FIFO is not empty 1: DBI_FIFO is empty
13	R/W1C	0x0	DBI_FIFO_FULL_INT DBI FIFO Full Interrupt Status 0: DBI_FIFO is not full 1: DBI_FIFO is full
12	R/W1C	0x0	TIMER_INT It indicates that the timer has been count sclk cycles to the value of DBI_Timer Register[30:0]. Writing 1 to this bit clears it. 0: Timer has not been achieved the objective 1: Timer has been achieved the objective
11	R/W1C	0x0	RD_DONE_INT It indicates that the number of byte setting in DBI_Control Register 1[19:8] has been read. Writing 1 to this bit clears it. 0: All data has not been read 1: All data has been read
10	R/W1C	0x0	TE_INT It indicates that the TE signal has been changed. Writing 1 to this bit clears it. 0: TE signal has not been changed 1: TE signal has been changed
9	R/W1C	0x0	FRAM_DONE_INT It indicates that a frame video data has been sent. Writing 1 to this bit clears it. 0: A frame video has not been sent 1: A frame video has been sent

Offset: 0x0120			Register Name: DBI_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W1C	0x0	LINE_DONE_INT It indicates that a line of video data has been sent. Writing 1 to this bit clears it. 0: A line of video data has not been sent 1: A line of video data has been sent
7	/	/	/
6	R/W	0x0	DBI_FIFO_EMPTY_INT_EN DBI FIFO Empty Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DBI_FIFO_FULL_INT_EN DBI FIFO Full Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TIMER_INT_EN Timer Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RD_DONE_INT_EN Read Done Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	TE_INT_EN TE Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	FRAM_DONE_INT_EN Frame Done Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	LINE_DONE_INT_EN Line Done Interrupt Enable 0: Disable 1: Enable

10.4.6.23 0x0124 DBI Debug Register 0 (Default Value: 0x007F_0000)

Offset: 0x0124			Register Name: DBI_Debug_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/

Offset: 0x0124			Register Name: DBI_Debug_0
Bit	**Read/Write**	**Default/Hex**	**Description**
22:16	R	0x7F	DBI_FIFO_AVAIL DBI_FIFO ROOM VALID 0~127 Words
15:13	/	/	/
12	R	0x0	TE_VAL TE input value 0: TE not Trigger 1: TE Trigger
11:8	R	0x0	DBI_RXCS FSM for DBI Receive RX_BS0 ~ RX_BS6 , Gray - Code
7:4	R	0x0	SH_CS FSM for shifter 0~11 : SH0~SH11
3:2	/	/	DBI_TXCS FSM for DBI Transmit 00: IDLE 01: SHIF 10: DUMY 11: READ
1:0	R	0x0	MEM_CS FSM for DBI Memory 00: IDLE_FRM 01: FRM_POS 10: FRM_RDY

10.4.6.24 0x0128 DBI Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: DBI_Debug_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R	0x0	LCNT Line counter The number of pixel lines that are currently sent
15:12	/	/	/
11:0	R	0x0	CCNT Component counter The number of RGB components that are currently sent The field is equal to pixel_cnt *3.

10.4.6.25 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in the byte, half-word, or word unit by AHB. In the byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In the half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In the word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. Note: This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.

10.4.6.26 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in the byte, half-word, or word unit by AHB. In the byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In the half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In the word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. Note: This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.

10.5 USB2.0 DRD

10.5.1 Overview

The USB2.0 dual-role device (USB2.0 DRD) supports both device and host functions which can also be configured as a Host-only or Device-only controller. It complies with the USB2.0 Specification.

For saving CPU bandwidth, the DMA interface of the DRD module can also support the external DMA controller to do the data transfer between the memory and the DRD FIFO. The DRD core also supports USB power saving functions.

The USB2.0 DRD has the following features:

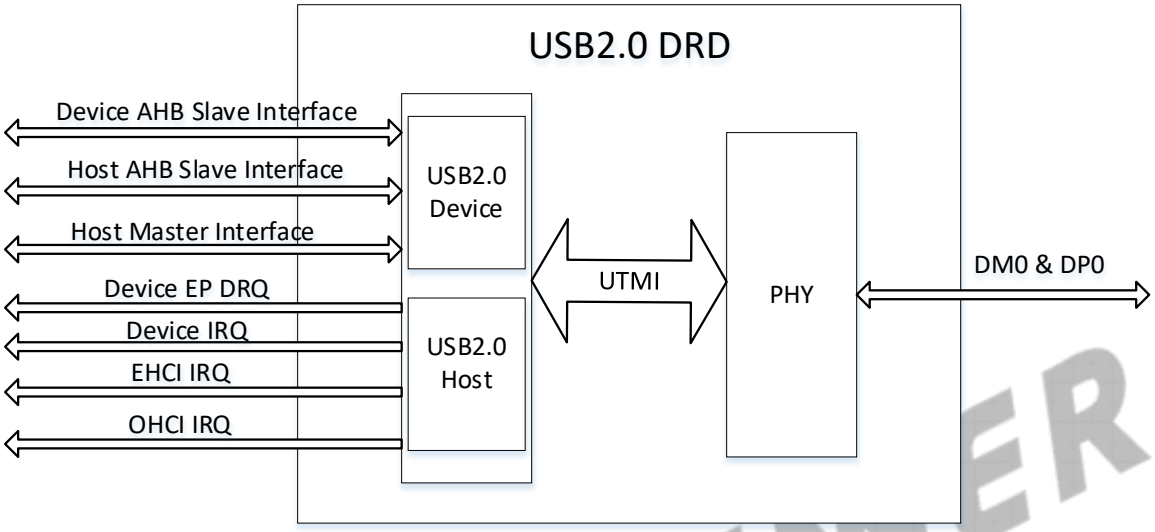
- Complies with USB2.0 Specification
- Supports USB Host function
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root port shared between EHCI and OHCI
- Supports USB Device function
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
  - Supports bi-directional endpoint0 (EP0) for Control transfer
  - Up to 10 user-configurable endpoints (EP1+, EP1-, EP2+, EP2-, EP3+, EP3-, EP4+, EP4-, EP5+, EP5-) for Bulk transfer, Isochronous transfer and Interrupt transfer
  - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
  - Supports interface to an external Normal DMA controller for every EP
- Supports an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral modes
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Device and host controller share a 8K SRAM and a physical PHY

- Supports USB standby

10.5.2 Block Diagram

The following figure shows the block diagram of USB2.0 DRD Controller.

Figure 10-60 USB2.0 DRD Controller Block Diagram



10.5.3 Functional Description

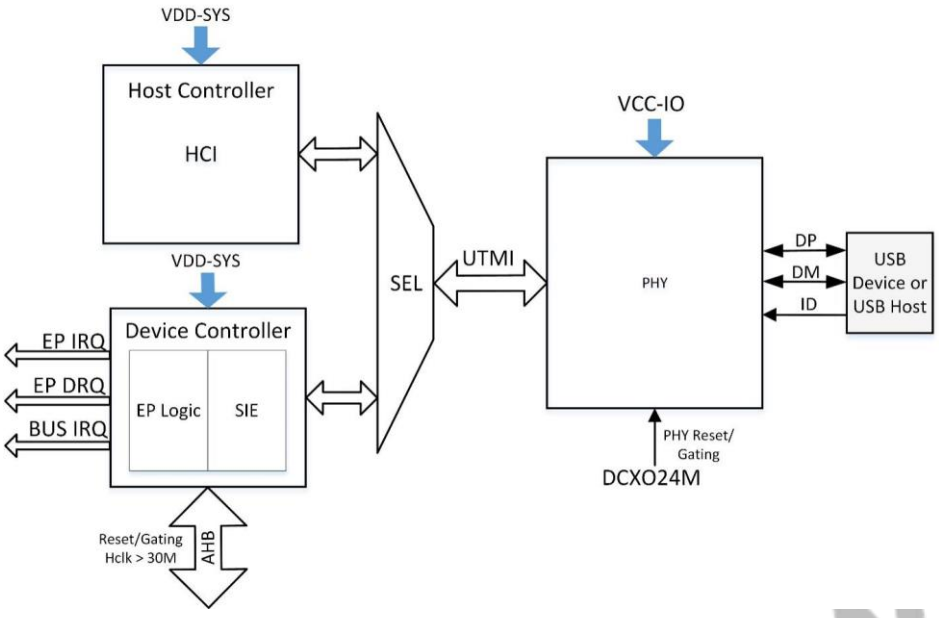
10.5.3.1 External Signals

Table 10-17 USB2.0 DRD External Signals

Signal	Description	Type
USB0-DP	USB2.0 DRD differential signal positive	AI/O
USB0-DM	USB2.0 DRD differential signal negative	AI/O
V33-USB	3.3V USB Analog Power Supply	P

10.5.3.2 Controller and PHY Connection Diagram

Figure 10-61USB2.0 DRD Controller and PHY Connection Diagram



10.5.4 USB_DRD_DEVICE Register List

Module Name	Base Address	Comments
USB_DRD_DEVICE	0x04100000	USB Device Controller

Register Name	Offset	Description
USB_EPFIFOn	0x0000+N*4 (N=0,1,2,3,4,5)	USB FIFO Entry for Endpoint N
USB_GCS	0x0040	USB Global Control and Status Register
USB_EPINTF	0x0044	USB Endpoint Interrupt Flag Register
USB_EPINTE	0x0048	USB Endpoint Interrupt Enable Register
USB_BUSINTF	0x004C	USB Bus Interrupt Flag Register
USB_BUSINTE	0x0050	USB Bus Interrupt Enable Register
USB_FNUM	0x0054	USB Frame Number Register
USB_TESTC	0x007C	USB Test Control Register
USB_CSR0	0x0080	USB EP0 Control and Status Register
USB_TXCSR	0x0080	USB EP1~5 Tx Control and Status Register
USB_RXCSR	0x0084	USB EP1~5 Rx Control and Status Register
USB_COUNT0	0x0088	USB EP0 Rx Counter Register
USB_RXCOUNT	0x0088	USB EP1~5 Rx Counter Register
USB_ATTR0	0x008C	USB EP0 Attribute Register
USB_EPATTR	0x008C	USB EP1~5 Attribute Register
USB_TXFIFO	0x0090	USB EP1~5 TxFIFO Setting Register
USB_RXFIFO	0x0094	USB EP1~5 RxFIFO Setting Register

Register Name	Offset	Description
USB_FADDR	0x0098	USB Function Address Register
USB_ISCR	0x0400	USB Interface Status and Control Register
USB_PHY_CTL	0x0404	USB PHY Control Register
USB_PHY_TEST	0x0414	USB PHY Test Register
USB_PHY_TUNE	0x0418	USB PHY Tune Register
USB_PHY_SEL	0x0420	USB PHY Select Register
USB_PHY_STA	0x0424	USB PHY Status Register
USB_DMA_INTE	0x0500	USB DMA Interrupt Enable Register
USB_DMA_INTS	0x0504	USB DMA Interrupt Status Register
USB_DMA_CHAN_CFG	0x0540+N*0x10(N=0~7)	USB DMA Channel Configuration Register
USB_DMA_SDRAM_ADD	0x0544+N*0x10(N=0~7)	USB DMA SDRAM Start Address Register
USB_DMA_BC	0x0548+N*0x10(N=0~7)	USB DMA Byte Counter Register
USB_DMA_RESIDUAL_BC	0x0548+N*0x10(N=0~7)	USB DMA RESIDUAL Byte Counter Register

10.5.5 USB_DRD_DEVICE Register Description

10.5.5.1 0x0000+N*0x04(N=0~5) USB FIFO Entry for Endpoint N (Default Value:0x0000_0000)

Offset: 0x0000+N*0x04(N=0~5)			Register Name: USB_EPFIFOn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	EPnFIFO FIFO Entry for Endpoint n

10.5.5.2 0x0040 USB Global Control and Status Register (Default Value:0x0000_0020)

Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_EDMA 1'b0: DMA_REQ signal for all IN Endpoints will be de-asserted when MAXP bytes have been written to and endpoint. This is late mode. 1'b1: DMA_REQ signal for all IN Endpoints will be de-asserted when MAXP-8 bytes have been written to an endpoint. This is early mode.

Offset: 0x0040			Register Name: USB_GCS
Bit	**Read/Write**	**Default/Hex**	**Description**
30	R/W	0x0	RX_EDMA 1'b0: DMA_REQ signal for all OUT Endpoints will be de-asserted when MAXP bytes have been read to an endpoint. This is late mode. 1'b1: DMA_REQ signal for all OUT Endpoints will be de-asserted when MAXP-8 bytes have been read to and endpoint. This is early mode.
29	/	/	/
28:25	R/W	0x0	BUS_DRQ_SEL USB DMA Request Signal Source Select 4'b0000: Select TX Endpoint 1 DRQ 4'b0001: Select RX Endpoint 1 DRQ 4'b0010: Select TX Endpoint 2 DRQ 4'b0011: Select RX Endpoint 2 DRQ 4'b0100: Select TX Endpoint 3 DRQ 4'b0101: Select RX Endpoint 3 DRQ 4'b0110: Select TX Endpoint 4 DRQ 4'b0111: Select RX Endpoint 4 DRQ
24	R/W	0x0	FIFO_BUS_SEL 0: CPU bus for FIFO Access, 1: DMA bus for FIFO operation.
23:20	/	/	/
19:16	R/W	0x0	EPIND Endpoint Index Index is a 4-bit register that determines which endpoint control/status registers are accessed. Before accessing an endpoint's control/status registers at 0x0080~0x00BF, the endpoint number should be written to the Index register to ensure that correct control/status registers in the memory map. **Note: The valid value for Index register is 0-4.**
15	R	0x0	BDev B-Device 0 => 'A' device; 1 => 'B' device; Only valid while a session is in progress. **Note: If the core is in Force_Host mode (i.e. a session has been started with USB_TMCTL.7=1), this bit will indicate the state of the HOSTDISCON input signal from the PHY.**
14:13	/	/	/

<table>
<tr><th colspan="3">Offset: 0x0040</th><th>Register Name: USB_GCS</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>12:11</td><td>R</td><td>0x0</td><td>VBus
These bits encode the current VBus level as follows:
<table>
<tr><td>D4</td><td>D3</td><td>Meaning</td></tr>
<tr><td>0</td><td>0</td><td>Below SessionEnd</td></tr>
<tr><td>0</td><td>1</td><td>Above SessionEnd, below AValid</td></tr>
<tr><td>1</td><td>0</td><td>Above AValid, below VBusValid</td></tr>
<tr><td>1</td><td>1</td><td>Above VBusValid</td></tr>
</table></td></tr>
<tr><td>10</td><td>R</td><td>0x0</td><td>HostMode
Host Mode
This bit is set when the USB/DRD is acting as a Host.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8</td><td>R/W</td><td>0x0</td><td>Session
When operating as an ‘A’ device, this bit is set or cleared by the CPU to start or end a session.
When operating as an ‘B’ device, this bit is set/cleared by the USB/DRD when a session starts/ends. It is also set by the CPU to initiate the Session Request Protocol.
When the USB/DRD is in Suspend mode, the bit may be cleared by the CPU to perform a software disconnect.
Note: Clearing this bit when the core is not suspending will result in undefined behavior.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>IsoUpdateEn
Isochronous Update Enable
When set by the CPU, the USB/DRD will wait for an SOF token from the Tx packet ready before sending the packet. If an IN token is received before an SOF token, then a zero length data packet will be send.
Note: This bit only affects endpoints performing Isochronous transfer.</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>SoftConn
Soft Connect
The USB D+/D- line is enabled when this bit is set by CPU and tri-stated when this bit is cleared by CPU.
Note: Only valid in Peripheral Mode (but not means ‘B’ Device).</td></tr>
<tr><td>5</td><td>R/W</td><td>0x1</td><td>HSEN
High-speed Mode Enable
When set by CPU , the USB/DRD will negotiate for High-speed mode when the device is reset by host. If not set, the device will only operate in Full-speed mode.</td></tr>
</table>

Offset: 0x0040			Register Name: USB_GCS
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R	0x0	HSFLAG High-speed Mode Flag When set, this read-only bit indicates High-speed mode successfully negotiated during USB reset. And this bit becomes valid when USB Reset completes (as indicated by USB reset interrupt).
3	R	0x0	Reset This bit is set when Reset Signaling is present on the bus.
2	R/W	0x0	Resume Set by the CPU to generate Resume signaling when the function is in Suspend mode. The CPU should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling.
1	R	0x0	SuspendM Suspend Mode This bit is set on entry into Suspend mode.
0	R/W	0x0	SuspendMEn Enable SuspendM Set by the CPU to enable the SUSPENDM output of UTMI+ bus.

10.5.5.3 0x0044 USB Endpoint Interrupt Flag Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: USB_EPINTF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	R	0x0	EP4Rx Rx Endpoint 4 interrupt flag
19	R	0x0	EP3Rx Rx Endpoint 3 interrupt flag
18	R	0x0	EP2Rx Rx Endpoint 2 interrupt flag
17	R	0x0	EP1Rx Rx Endpoint 1 interrupt flag
16:5	/	/	/
4	R	0x0	EP4Tx Tx Endpoint 4 interrupt flag
3	R	0x0	EP3Tx Tx Endpoint 3 interrupt flag
2	R	0x0	EP2Tx Tx Endpoint 2 interrupt flag
1	R	0x0	EP1Tx Tx Endpoint 1 interrupt flag

Offset: 0x0044			Register Name: USB_EPINTF
Bit	Read/Write	Default/Hex	Description
0	R	0x0	EP0 Endpoint 0 interrupt flag

10.5.5.4 0x0048 USB Endpoint Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: USB_EPINTE
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	EP4Rx Rx Endpoint 4 interrupt enable
19	R/W	0x0	EP3Rx Rx Endpoint 3 interrupt enable
18	R/W	0x0	EP2Rx Rx Endpoint 2 interrupt enable
17	R/W	0x0	EP1Rx Rx Endpoint 1 interrupt enable
16:5	/	/	/
4	R/W	0x0	EP4Tx Tx Endpoint 4 interrupt enable
3	R/W	0x0	EP3Tx Tx Endpoint 3 interrupt enable
2	R/W	0x0	EP2Tx Tx Endpoint 2 interrupt enable
1	R/W	0x0	EP1Tx Tx Endpoint 1 interrupt enable
0	R/W	0x0	EP0 Endpoint 0 interrupt enable

10.5.5.5 0x004C USB Bus Interrupt Flag Register (Default Value:0x0000_0000)

Offset: 0x004C			Register Name: USB_BUSINTF
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0x0	VBusError Set when VBus drops below the VBus Valid threshold during a session. **Note: Only valid when USB/DRD is 'A' device.**
6	R	0x0	SessionRequest Set when Session Request signaling has been detected. **Note: Only valid when USB/DRD is 'A' device.**

Offset: 0x004C			Register Name: USB_BUSINTF
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R	0x0	Disconnect Set in Host mode when a device disconnect is detected. Set in Peripheral mode when a session ends. **Note: Valid at all transaction speeds.**
4	R	0x0	Connect Set in host mode when a device connection is detected. **Note: Only valid in Host mode. Valid at all transaction speeds.**
3	R	0x0	SOF Set when a new frame starts.
2	R	0x0	ResetBabble Reset Set in Peripheral mode when Reset signaling is detected on the bus. Babble Set in Host mode when babble is detected. **Note: Only active after first SOF has been sent.**
1	R	0x0	Resume Set when Resume signaling is detected on the bus while the USB/DRD is in Suspend mode.
0	R	0x0	Suspend Set when Suspend signaling is detected on the bus. **Note: Only valid in Peripheral mode.**

10.5.5.6 0x0050 USB Bus Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: USB_BUSINTE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	VBusError VBusError interrupt enable
6	R/W	0x0	Session Request Session Request interrupt enable
5	R/W	0x0	Disconnect Disconnect interrupt enable
4	R/W	0x0	Connect Connect interrupt enable
3	R/W	0x0	SOF SOF interrupt enable

Offset: 0x0050			Register Name: USB_BUSINTE
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	ResetBabble Reset Reset interrupt enable Babble Babble interrupt enable
1	R/W	0x0	Resume Resume interrupt enable
0	R/W	0x0	Suspend Suspend interrupt enable

10.5.5.7 0x0054 USB Frame Number Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: USB_FNUM
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	FRNUM Frame Number Hold the last received frame number.

10.5.5.8 0x007C USB Test Control Register (Default Value:0x0000_0000)

Offset: 0x007C			Register Name: USB_TESTC
Bit	Read/Write	Default/Hex	Description
31:24	/	0	/
23:16	R	/	FSM USB Operation Finite State Machine for Debug
15:11	/	/	/
10	R/W	0x0	EXTRXACT Extend Rx Active Signal for safe
9	R/W	0x0	RESUME_SE0 Resume from SE0 Enable
8	R/W	0x0	TM1 Test Mode Enable for Simulation.

<table>
<tr><th colspan="3">Offset: 0x007C</th><th>Register Name: USB_TESTC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Force_Host
The CPU sets this bit to instruct the core to enter Host mode when the Session bit (Bit 0 of USB_DEVCTL) is set, regardless of whether it is connected to any peripheral. The state of the CID input, HostDisconnect and Linestate signals are ignored. The core will then remain in Host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set.
While in this mode, the status if the HOSTDISCON signal from the PHY may be read from bit 7 of the USB_DEVCTL (in 0x0060) register.
The operating speed is determined from the Force_HS and Force_FS bits as follows:
<table>
<tr><td>Force_HS</td><td>Force_FS</td><td>Operating Speed</td></tr>
<tr><td>0</td><td>0</td><td>Low Speed</td></tr>
<tr><td>0</td><td>1</td><td>Full Speed</td></tr>
<tr><td>1</td><td>0</td><td>High Speed</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>6</td><td>W</td><td>0x0</td><td>FIFO_Access
The CPU sets this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO. It is cleared automatically.
Note: Writing ‘0’ to this bit will be ignored.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Force_FS
The CPU sets this bit either in conjunction with bit 7 above or to force the USB/DRD into Full-speed mode when it receive a USB reset.</td></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Force_HS
The CPU sets this bit either in conjunction with bit 7 above or to force the USB/DRD into High-speed mode when it receive a USB reset.</td></tr>
<tr><td>3</td><td>R/W</td><td>0x0</td><td>Test_Packet
(High-speed mode) The CPU sets this bit to enter Test_Packet test mode. In the mode, the USB/DRD repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the Universal Serial Bus Specification Revision 2.0, Section 7.1.20.
Note: The text packet has a fixed 0format and must be loaded into the Endpoint 0 FIFO before the test mode is entered.</td></tr>
<tr><td>2</td><td>R/W</td><td>0x0</td><td>Test_K
(High-speed mode) The CPU sets this bit to enter the Test_K test mode. In this mode, the USB/DRD transmits a continuous K on the bus.</td></tr>
</table>

Offset: 0x007C			Register Name: USB_TESTC
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	Test_J (High-speed mode) The CPU sets this bit to enter the Test_J est mode. In this mode, the USB/DRD transmits a continuous J on the bus.
0	R/W	0x0	Test_SE0_NAK (High-speed mode) The CPU sets this bit to enter the Test_SE0_NAK test mode. In this mode, the USB/DRD remains in High-speed mode but responds to any valid IN token with a NAK.

10.5.5.9 0x0080 USB EP0 Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: USB_CSR0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	W	0x0	FlushFIFO The CPU writes a '1' to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset, and the TxPktRdy/RxPktRdy bit (below) is cleared. **Note:** **(1) Writing '0' to this bit is ignored.** **(2) Flush FIFO should only be used when TxPktRdy/RxPktRdy is set, at other times, it may cause data to be corrupted.**
23	W	0x0	ServicedSetupEnd The CPU writes a '1' to this bit to clear the SetupEnd bit. It is cleared automatically.
22	W	0x0	ServicedRxPktRdy The CPU writes a 1 to this bit to clear the RxPktRdy bit. It is cleared automatically.
21	W	0x0	SendStall The CPU writes a '1' to this bit to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically. **Note: The FIFO should be flushed before SendStall is set.**
20	R	0x0	SetupEnd This bit will be set when a control transaction ends before the DataEnd bit has been set. An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing a '1' to the ServicedSetupEnd bit.

Offset: 0x0080			Register Name: USB_CSR0
Bit	**Read/Write**	**Default/Hex**	**Description**
19	W	0x0	DataEnd The CPU sets this bit: When setting TxPktRdy for the last data packet. When clearing RxPktRdy after unloading the last data packet. When setting TxPktRdy for a zero length data packet. It is cleared automatically.
18	R/W	0x0	SentStall This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.
17	R/W	0x0	TxPktRdy The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
16	R	0x0	RxPktRdy This bit is set when a data packet has been received. An interrupt is generated (if enabled) when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.
15:0	/	/	/

10.5.5.10 0x0080 USB EP1~5 Tx Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: USB_TXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	AutoSet If CPU sets this bit, TxPktRdy will be automatically set when data of maximum packet size (value in the USB_TXMAXP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. **Note: Should not be set for high-bandwidth Isochronous/Interrupt endpoints.**
30	R/W	0x0	ISO The CPU sets this bit to enable the Tx endpoint for Isochronous transfers, and clears it to enable the Tx endpoint for Bulk or Interrupt transfers. **Note: This is only has any effect in Peripheral mode. In Host mode, it always returns zero.**
29	R/W	0x0	Mode The CPU sets this bit to enable the endpoint direction as Tx, and clears the bit to enable it as Rx. **Note: This bit only has any affect where the same endpoint FIFO is used for Tx and Rx transactions.**

Offset: 0x0080			Register Name: USB_TXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	DMAReqEnab The CPU sets this bit to enable the DMA request for the Tx endpoint.
27	R/W	0x0	FrcDataTog The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
26	R/W	0x0	DMAReqMode The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. **Note: This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is cleared.**
25:24	/	/	/
23	R/W	0x0	IncompTx When the endpoint is being used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts. **Note: In anything other than a high-bandwidth transfer, this bit will always return 0. And writing '1' to this bit is ignored.**
22	W	0x0	ClrDataTog The CPU writes a 1 to this bit to reset the endpoint data toggle to 0. It is cleared automatically. **Note: Writing '0' to this bit is ignored.**
21	R/W	0x0	SentStall This bit is set when a STALL handshake is transmitted. The FIFO is flushed and the TxPktRdy bit is cleared. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
20	R/W	0x0	SendStall The CPU writes a 1 to this to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition. **Note:** **(1) The FIFO should be flushed before SendStall is set.** **(2)This bit has no effect where the endpoint is being used for Isochronous transfers.**

Offset: 0x0080			Register Name: USB_TXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
19	W	0x0	FlushFIFO The CPU writes a 1 to this bit to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. **Note:** **(1) Writing '0' to this bit is ignored.** **(2) Flush FIFO should only be used when TxPktRdy is set, at other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.**
18	R/W	0x0	UnderRun The USB sets this bit if an IN token is received when the TxPktRdy bit not set. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
17	R/W	0x0	FIFONotEmpty The USB sets this bit when there is at least 1 packet in the Tx FIFO. **Note: Writing '1' to this bit is ignored.**
16	R/W	0x0	TxPktRdy The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared prior to loading a second packet to a double buffered FIFO. **Note: Writing '0' to this bit is ignored.**

Offset: 0x0080			Register Name: USB_TXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	R/W	0x0	PacketCount In the case of Bulk endpoints with the packet splitting option enabled, the Packet Count can be up to 32 and defines the maximum number of USB packets of specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. If the packet splitting option is not enabled, Packet Count is not implemented. For Isochronous/Interrupt endpoints operating in High-speed mode and with the High-bandwidth option enabled, Packet Count may only either 2 or 3 (corresponding to bit 11 or bit 12 set, respectively) and it specifies the maximum number of such transactions that can be take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB/DRD will automatically split any data packet written to the FIFO into up to 2 or 3 USB packet, each containing the specified payload (or less). For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bit 11 and 12 are ignored. **Note: Value for this bits is (Packet Count - 1), but not Packet Count.**
10:0	R/W	0x0	MaximumPayload These bits define the maximum payload (in bytes) transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. **Note:** **(1) The value written to Maximum Payload (multiplied by Packet Count in the case of high-bandwidth Isochronous/Interrupt transfer) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint, a mismatch could cause unexpected result.** **(2) The total amount of data represented by the value written to this register (Maximum payload × Packet Count) must not exceed the FIFO size for Tx endpoint, and should not exceed half the FIFO size if double-buffering is required.**

10.5.5.11 0x0084 USB EP1~5 Rx Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: USB_RXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	AutoClear If CPU sets this bit then the RxPktRdy will be automatically cleared when data of maximum packet size (value in the USB_TXMAXP) is unloaded from the Rx FIFO. If a packet of less than the maximum packet size is unloaded, then RxPktRdy will have to be cleared manually. **Note: Should not be set for high-bandwidth Isochronous endpoints.**
30	R/W	0x0	ISO The CPU sets this bit to enable the Rx endpoint for Isochronous transfers, and clears it to enable the Rx endpoint for Bulk or Interrupt transfers.
29	R/W	0x0	DMAReqEnab The CPU sets this bit to enable the DMA request for the Rx endpoint.
28	R/W	0x0	DisNyet_PIDError DisNyet *Bulk/Interrupt Transactions:* The CPU sets this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the FIFO becomes full. **Note: This bit only has any affect in High-speed mode, in which mode it should be set for all Interrupt endpoints.** PIDError ISO Transactions: The core sets this bit to indicate a PID error in the received packet.
27	R/W	0x0	DMAReqMode The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. **Note: This bit must not be cleared in the same cycle as the above RxPktRdy(or DMAReqEnab) bit is cleared.**
26:25	/	/	/
24	R/W	0x0	IncompRx This bit will be set in a high-bandwidth Isochronous/Interrupt transfer if the packet received is incomplete. It will be cleared when RxPktRdy is cleared. **Note:** **(1) Writing '1' to this bit is forbidden.** **(2) In anything other than a high-bandwidth transfer, this bit will always return 0.**

Offset: 0x0084			Register Name: USB_RXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
23	W	0x0	ClrDataTog The CPU writes a '1' to this bit to reset the endpoint data toggle to 0. It is cleared automatically. **Note: Writing '0' to this bit is ignored.**
22	R/W	0x0	SentStall This bit is set when a STALL handshake is transmitted. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
21	R/W	0x0	SendStall The CPU writes a '1' to this to issue a STALL handshake. The CPU clears this bit to terminate the stall condition. **Note:** **(1) The FIFO should be flushed before SendStall is set.** **(2)This bit has no effect where the endpoint is being used for Isochronous transfers.**
20	W	0x0	FlushFIFO The CPU writes a '1' to this bit to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. **Note:** **(1) Writing '0' to this bit is ignored.** **(2) Flush FIFO should only be used when RxPktRdy is set, at other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.**
19	R	0x0	DataError This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. It is cleared when RxPktRdy is cleared. **Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns zero.**
18	R/W	0x0	OverRun The USB sets this bit if an OUT token can not be loaded into the Rx FIFO. The CPU should clear this bit. **Note:** **(1) Writing '1' to this bit is ignored.** **(2) This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns zero.**
17	R	0x0	FIFOFull The USB sets this bit when no more packets can be loaded into the Rx FIFO.

Offset: 0x0084			Register Name: USB_RXCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W	0x0	RxPktRdy This bit is set when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set. **Note: Writing '1' to this bit is ignored.**
15:11	R/W	0x0	PacketCount In the case of Bulk endpoints with the packet combining option enabled, the Packet Count can be up to 32 and defines the maximum number of USB packets of specified payload which are to be combined into a single data packet within the FIFO. For Isochronous/Interrupt endpoints operating in High-speed mode and with the High-bandwidth option enabled, Packet Count may only either 2 or 3 (corresponding to bit 11 or bit 12 set, respectively) and it specifies the maximum number of such transactions that can be take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB/DRD will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bit 11 and 12 are ignored. **Note: Value for this bits is (Packet Count - 1), but not Packet Count.**
10:0	R/W	0x0	MaximumPayload These bits define the maximum payload (in bytes) transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. **Note:** **(1) The value written to Maximum Payload (multiplied by Packet Count in the case of high-bandwidth Isochronous/Interrupt transfer) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint, a mismatch could cause unexpected result.** **(2) The total amount of data represented by the value written to this register (Maximum payload × Packet Count) must not exceed the FIFO size for OUT endpoint, and should not exceed half the FIFO size if double-buffering is required.**

10.5.5.12 0x0088 USB EP0 Rx Counter Register (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: USB_COUNT0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RxCount0 Endpoint 0 Rx Count These bits indicate the number of received data bytes in the Endpoint 0 FIFO. **Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (of USB_CSR0) is set.**

10.5.5.13 0x0090 USB EP1~5 TxFIFO Setting Register (Default Value:0x0000_0000)

Offset: 0x0090			Register Name: USB_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	AD AD[12:0] Start address of the endpoint FIFO is in units of 8 bytes, and it equals (AD[12:0]*8).
15:5	/	/	/
4	R/W	0x0	DPB Defines whether double-packet buffering supported. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.
3:0	R/W	0x0	SZ SZ[3:0] Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission) is $2^{(SZ[3:0]+3)}$ bytes, and the valid values for SZ[3:0] are 0x0–0x09. If DPB=0, the FIFO will also this size; if DPB=1, the FIFO will be twice this size.

10.5.5.14 0x0094 USB EP1~5 RxFIFO Setting Register (Default Value:0x0000_0000)

Offset: 0x0094			Register Name: USB_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	AD AD[12:0] Start address of the endpoint FIFO is in units of 8 bytes, and it equals (AD[12:0]*8).

Offset: 0x0094			Register Name: USB_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
15:5	/	/	/
4	R/W	0x0	DPB Defines whether double-packet buffering supported. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.
3:0	R/W	0x0	SZ SZ[3:0] Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission) is $2^{(SZ[3:0]+3)}$ bytes, and the valid values for SZ[3:0] are 0x0–0x09. If DPB=0, the FIFO will also this size; if DPB=1, the FIFO will be twice this size.

10.5.5.15 0x0098 USB Function Address Register (Default Value:0x0000_0000)

Offset: 0x0098			Register Name: USB_FADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	RW	0x0	FADDR The function address in peripheral mode. This field is reset to zero after a USB bus reset, and should be updated by software after Set_Address Command during USB enumeration.

10.5.5.16 0x0400 USB Interface Status and Control Register (Default Value:0x0000_0000)

Offset: 0x0400			Register Name: USB_ISCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	0	/
30	R	-	VBUSLS USB VBUS Valid Status detected from Line State
29	R	-	VBUSEX USB VBUS Valid Status detected from external VBUS input
28	R	-	IDEX USB ID Status detected from external ID input
27:26	R	-	LS USB Line Status [27]—DM [26]—DP
25	R	-	VBUS USB VBUS Status merged from both internal and external

Offset: 0x0400			Register Name: USB_ISCR
Bit	**Read/Write**	**Default/Hex**	**Description**
24	R	-	ID USB ID Status merged from both internal and external
23:18	/	0x0	/
17	R/W	0x0	IDPullupEn ID pull up enable 0: disable 1: enable ID pull up
16	R/W	0x0	DataPullupEn DP/DM pull up enable 0: DP/DM pull up diable 1: DP/DM pull up enable
15:14	R/W	0x0	ForceID Force ID 0x: use external ID Status 10: force ID to LOW 11: force ID to HIGH
13:12	R/W	0x0	ForceVBUS Force VBUS Valid 0x: use external VBUS Valid Status from VBUS Input or Line State 10: Force VBUS Valid to LOW 11: Force VBUS Valid to HIGH
11:10	R/W	0x0	VBUSSEL External VBUS Valid Source Select 0x: External VBUS Valid detected from VBUS Input 10: External VBUS Valid detected from DP/DM Input 11: External VBUS Valid detected from either VBUS or DP/DM input
9:8	/	0x0	/
7	R/W	0x0	WakeupEn USB Wakeup Enable 0: Disable 1: Enable
6	R/W	0x0	VBUSCDS VBUS Input Change Detect Status This bit is set by hardware after VBUS input changed when VBUS change detect is enable. Writing ‘1’ will clear this bit.
5	R/W	0x0	IDCDS ID Input Change Detect Status This bit is set by hardware after ID input changed when ID change detect is enable. Writing ‘1’ will clear this bit.

Offset: 0x0400			Register Name: USB_ISCR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	DATACDS DP/DM Input Change Detect Status This bit is set by hardware after DP/DM input changed when DP/DM change detect is enable. Writing '1' will clear this bit.
3	R/W	0x0	WakeupIE USB Wakeup IRQ Enable 1: Enable USB Wakeup IRQ 0: Disable USB Wakeup IRQ If this bit is set to zero, an USB wakeup event (VBUS/ID/DP/DM change) will generate an USB wakeup request to wakeup the system, but not generate an USB wakeup IRQ to CPU.
2	R/W	0x0	VBUSCDE VBUS Input Change Detect enable 0: Disable; 1: Enable
1	RW	0x0	IDCDE ID Input Change Detect enable 0: Disable; 1: Enable
0	R/W	0x0	DATACDE DP/DM Input Change Detect enable 0: Disable; 1: Enable

10.5.5.17 0x0410 USB PHY Control Register (Default Value:0x0000_0008)

Offset: 0x0410			Register Name: USB_PHY_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	BIST_EN_A
15:8	R/W	0x0	VC_ADDR
7	R/W	0x0	VC_DI
6:4	/	/	/
3	R/W	0x1	SIDDQ 1: Write 1 to disable PHY. 0: Write 0 to enable PHY.
2	/	/	/
1	R/W	0x0	VC_EN 0: Write 0 to disable PHY VC bus 1: Write 1 to enable PHY VC bus. **Note: only 1 VC bus of all the USB controllers could be enabled at the same time**
0	R/W	0x0	VC_CLK

10.5.5.18 0x0414 USB PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0414			Register Name: USB_PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

10.5.5.19 0x0418 USB PHY Tune Register (Default Value:0x0234_38E4)

Offset: 0x0418			Register Name: USB_PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:23	R/W	0x04	COMPDISTUNE
22:20	R/W	0x03	SQRXTUNE
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x04	DRDTUNE
15:12	R/W	0x03	TXFSLSTUNE
11:8	R/W	0x08	TXVREFTUNE
7:6	R/W	0x03	TXHSXVTUNE
5:4	R/W	0x02	TXRISETUNE
3:2	R/W	0x01	TXRESTUNE
1:0	R/W	0x0	TXPREEMPAMPTUNE

10.5.5.20 0x420 USB PHY Select Register (Default Value:0x0000_0001)

Offset: 0x420			Register Name: USB_PHY_SEL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	Reserved
0	R/W	0x1	OTG_SEL 1: Phy is connected to OTG SIE 0: Phy is connected to HCI SIE

10.5.5.21 0x424 USB PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x424			Register Name: USB_PHY_STA
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x0	BIST_ERROR

Offset: 0x424			Register Name: USB_PHY_STA
Bit	Read/Write	Default/Hex	Description
16	R	0x0	BIST_DONE
15:1	/	/	/
0	R	0x0	VC_DO

10.5.5.22 0x0500 USB DMA Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: USB_DMA_INTE
Bit	Read/Write	Default/Hex	Description
31:8	/	/	Reserved
7	R/W	0x0	USB_DMA7_PKG_INT_EN DMA7 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
6	R/W	0x0	USB_DMA6_PKG_INT_EN DMA6 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
5	R/W	0x0	USB_DMA5_PKG_INT_EN DMA5 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
4	R/W	0x0	USB_DMA4_PKG_INT_EN DMA4 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
3	R/W	0x0	USB_DMA3_PKG_INT_EN DMA3 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
2	R/W	0x0	USB_DMA2_PKG_INT_EN DMA2 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
1	R/W	0x0	USB_DMA1_PKG_INT_EN DMA1 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
0	R/W	0x0	USB_DMA0_PKG_INT_EN DMA0 Package End Transfer Interrupt Enable 0: Disable 1: Enable.

10.5.5.23 0x0504 USB DMA Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0504			Register Name: USB_DMA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	Reserved
7	R/W	0x0	USB_DMA7_PKG_INT_STA DMA7 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending
6	R/W	0x0	USB_DMA6_PKG_INT_STA DMA6 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending
5	R/W	0x0	USB_DMA5_PKG_INT_STA DMA5 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending
4	R/W	0x0	USB_DMA4_PKG_INT_STA DMA4 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending
3	R/W	0x0	USB_DMA3_PKG_INT_STA DMA3 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending
2	R/W	0x0	USB_DMA2_PKG_INT_STA DMA2 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending
1	R/W	0x0	USB_DMA1_PKG_INT_STA DMA1 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending

Offset: 0x0504			Register Name: USB_DMA_INTS
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	USB_DMA0_PKG_INT_STA DMA0 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending

10.5.5.24 0x0540+N*0x10(N=0~7) USB DMA Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0540+N*0x10(N=0~7)			Register Name: USB_DMA_CHAN_CFG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA_EN DMA Channel Enable If set to 1, DMA will start the data transfer between the source and the destination. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to this bit will stop the corresponding DMA channel and reset its state machine.
30:27	/	/	/
26:16	R/W	0x0	DMA_BST_LEN DMA Burst Length The value setting on this field should be equated to the usb max packet length of the corresponding endpoint.
15:5	/	/	/
4	R/W	0x0	DMA_DIR DMA Transfer Direction 0: SDRAM to USB FIFO 1: USB FIFO to SDRAM
3:0	R/W	0x0	DMA_FOR_EP DMA Channel for Endpoint The Endpoint number setting on this field selects the dma channel for the corresponding endpoint.

10.5.5.25 0x0544+N*0x10(N=0~7) USB DMA SDRAM Start Address Register (Default Value:0x0000_0000)

Offset: 0x0544+N*0x10(N=0~7)			Register Name: USB_DMA_SDRAM_ADD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMA_SDRAM_STR_ADDR DMA SDRAM Start Address The SDRAM start address for the DMA channel transfer between the SDRAM and USB FIFO.

10.5.5.26 0x0548+N*0x10(N=0~7) USB DMA Byte Counter Register (Default Value:0x0000_0000)

Offset: 0x0548+N*0x10(N=0~7)			Register Name: USB_DMA_BC
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	DMA_BC DMA Byte Counter

10.5.5.27 0x0548+N*0x10(N=0~7) USB DMA RESIDUAL Byte Counter Register (Default Value:0x0000_0000)

Offset: 0x0548+N*0x10(N=0~7)			Register Name: USB_DMA_RESIDUAL_BC
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	DMA_RESIDUAL_BC DMA Residual Byte Counter This field contains the residual byte count in current transfer.

10.5.6 USB_DRD_HOST Register List

Module Name	Base Address	Comments
USB_DRD_HOST	0x04101000	USB Host Controller

Register Name	Offset	Description
E_CAPLENGTH	0x0000	EHCI Identification Register
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000C	EHCI Companion Port Route Description
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_PERIODICLISTBASE	0x0024	EHCI Periodic Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Current Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status and Control Register
O_HcRevision	0x0400	OHCI Revision Register
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register

Register Name	Offset	Description
O_HcHCCA	0x0418	OHCI HCCA Register
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Register
O_HcControlHeadED	0x0420	OHCI Control Head ED Register
O_HcControlCurrentED	0x0424	OHCI Control Current ED Register
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Register
O_HcBulkCurrentED	0x042c	OHCI Bulk Current ED Register
O_HcDoneHead	0x0430	OHCI Done Head Register
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
O_HcRhDescriptorA	0x0448	OHCI Root Hub DescriptorA Register
O_HcRhDesriptorB	0x044C	OHCI Root Hub DescriptorB Register
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register
USB_CTRL	0x0800	HCI Interface Register
HCI_CTRL3	0x0808	HCI Control 3 Register
PHY_CTRL	0x0810	PHY Control Register
PHY_STA	0x0824	PHY Status Register
USB_SPDCR	0x0828	HCI SIE Port Disable Control Register

10.5.7 USB_DRD_HOST Register Description

10.5.7.1 0x0000 EHCI Identification Register (Default Value:0x10)

Offset:0x0000			Register Name: E_CAPLENGTH
Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

10.5.7.2 0x0002 EHCI Host Interface Version Number Register (Default Value:0x0100)

Offset: 0x0002			Register Name: E_HCIVERSION
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0100	HCIVERSION This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

10.5.7.3 0x0004 EHCI Host Control Structural Parameter Register (Default Value:0x0000_1101)

<table>
<tr><th colspan="3">Offset: 0x0004</th><th>Register Name: E_HCSPARAMS</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>31:24</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>23:20</td><td>R</td><td>0x0</td><td>Debug Port Number
This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port.
This field will always be ‘0’.</td></tr>
<tr><td>19:16</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>15:12</td><td>R</td><td>0x1</td><td>Number of Companion Controller (N_CC)
This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s).
This field will always be ‘0’.</td></tr>
<tr><td>11:8</td><td>R</td><td>0x1</td><td>Number of Port per Companion Controller(N_PCC)
This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software.
This field will always fix with ‘0’.</td></tr>
<tr><td>7</td><td>R</td><td>0x0</td><td>Port Routing Rules
This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation:
<table>
<tr><th>Value</th><th>Meaning</th></tr>
<tr><td>0</td><td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td></tr>
<tr><td>1</td><td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td></tr>
</table>
This field will always be ‘0’.</td></tr>
<tr><td>6:4</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>3:0</td><td>R</td><td>0x1</td><td>N_PORTS
This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f.
This field is always 1.</td></tr>
</table>

10.5.7.4 0x0008 EHCI Host Control Capability Parameter Register (Default Value:0x0000_a026)

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R	0xa0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R	0x2	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	0x1	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R	0x1	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

10.5.7.5 0x000C EHCI Companion Port Route Description (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: E_HCSPPORTROUTE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

10.5.7.6 0x0010 EHCI USB Command Register (Default Value:0x0008_0B00)

<table>
<tr><th colspan="3">Offset: 0x0010</th><th>Register Name: USBCMD</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>31:24</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x08</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table><tr><td>Value</td><td>Minimum Interrupt Interval</td></tr><tr><td>0x00</td><td>Reserved</td></tr><tr><td>0x01</td><td>1 micro-frame</td></tr><tr><td>0x02</td><td>2 micro-frame</td></tr><tr><td>0x04</td><td>4 micro-frame</td></tr><tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr><tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr><tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr><tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr></table>Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11</td><td>R</td><td>0x1</td><td>Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS (Offset: 0x0008) register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9:8</td><td>R</td><td>0x3</td><td>Asynchronous Schedule Park Mode Count(OPTIONAL)
Asynchronous Park Capability bit in the HCCPARAMS (Offset: 0x0008) is a one, then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.
Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0010</th><th>Register Name: USBCMD</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Light Host Controller Reset(OPTIONAL)
This control bit is not required.
If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships).
A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-
Ware must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:
<table>
<tr><th>Bit Value</th><th>Meaning</th></tr>
<tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr>
<tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr>
</table>
The default value of this field is ‘0b’.</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0010</th><th>Register Name: USBCMD</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>0x0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index
Register should be used for the Frame List Current index. Values mean:
<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr><tr><td>01b</td><td>512 elements(2048byts)</td></tr><tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
</table>

Offset: 0x0010			Register Name: USBCMD
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0x0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

10.5.7.7 0x0014EHCI USB Status Register (Default Value:0x0000_1000)

Offset: 0x0014			Register Name: E_USBSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

Offset: 0x0014			Register Name: E_USBSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
15	R	0x0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a '0' then the status of the Asynchronous Schedule is disabled. If this bit is a '1', then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0x0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a '0' then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0x0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.

Offset: 0x0014			Register Name: E_USBSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/WC	0x0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition (e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

10.5.7.8 0x0018 EHCI USB Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: E_USBINTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.

Offset: 0x0018			Register Name: E_USBINTR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

10.5.7.9 0x001C EHCI Frame Index Register (Default Value:0x0000_0000)

Offset: 0x001C			Register Name: E_FRINDEX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	**/**

Offset: 0x001C			Register Name: E_FRINDEX
Bit	**Read/Write**	**Default/Hex**	**Description**
13:0	R/W	0x0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times (frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

NOTE

If This register must be written as a DWord. Byte writes produce undefined results.

10.5.7.10 0x0024 EHCI Periodic Frame List Base Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: E_PERIODICLISTBASE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

NOTE

Writes must be Dword Writes.

10.5.7.11 0x0028 EHCI Current Asynchronous List Address Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: E_ASYNCLISTADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	R/W	0x0	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

10.5.7.12 0x0050 EHCI Configure Flag Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: E_CONFIGFLAG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 — Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 — Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

NOTE

This register is not use in the normal implementation.

10.5.7.13 0x0054 EHCI Port Status and Control Register (Default Value:0x0000_2000)

<table>
<tr><th colspan="3">Offset: 0x0054</th><th>Register Name: E_PORTSC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>31:22</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>21</td><td>R/W</td><td>0x0</td><td>Wake on Disconnect Enable(WKDSCNNT_E)
Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>20</td><td>R/W</td><td>0x0</td><td>Wake on Connect Enable(WKCNNT_E)
Writing this bit to a one enable the port to be sensitive to device connects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0x0</td><td>Port Test Control
The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow:
<table>
<tr><td>Bits</td><td>Test Mode</td></tr>
<tr><td>0000b</td><td>The port is NOT operating in a test mode.</td></tr>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-1111b</td><td>Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.</td></tr>
<tr><td>15:14</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>13</td><td>R/W</td><td>0x1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>/</td><td>/</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0054</th><th>Register Name: E_PORTSC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>11:10</td><td>R</td><td>0x0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
</table>

Offset: 0x0054			Register Name: E_PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	Port Reset 1=Port is in Reset. 0=Port is not in Reset. Default value = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one, it must also write a zero to the Port Enable bit. Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one. This field is zero if Port Power is zero.

<table>
<tr><th colspan="3">Offset: 0x0054</th><th>Register Name: E_PORTSC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table><tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr><tr><td>0x</td><td>Disable</td></tr><tr><td>10</td><td>Enable</td></tr><tr><td>11</td><td>Suspend</td></tr></table>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
① Software sets the Force Port Resume bit to a zero (from a one).
② Software sets the Port Reset bit to a one (from a zero).
If host software sets this bit to a one when the port is not enabled (i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
</table>

Offset: 0x0054			Register Name: E_PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0x0	Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.

Offset: 0x0054			Register Name: E_PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/WC	0x0	Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0x0	Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (Bit 1) to be set. This field is zero if Port Power zero.

NOTE

This register is only reset by hardware or in response to a host controller reset.

10.5.7.14 0x0400 OHCI Revision Register (Default Value:0x10)

Offset: 0x0400				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	/	/	/	/
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

10.5.7.15 0x0404 OHCI Control Register (Default Value:0x0000_0000)

Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus (Offset: 0x040C) is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
8	R/W	R	0x0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus (Offset: 0x040C). If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System

<table>
<tr><th colspan="4">Offset: 0x0404</th><th>Register Name: O_HcControl</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td></td><td></td><td></td><td></td><td>Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB
00b USBReset
01b USBResume
10b USBOperational
11b USBSuspend
A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus (Offset: 0x040C).
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.
HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.</td></tr>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>BulkListEnable
This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED (Offset: 0x42C)is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED (Offset: 0x42C) before re-enabling processing of the list.</td></tr>
<tr><td>4</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlListEnable
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED (Offset: 0x424) is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED (Offset: 0x424) before re-enabling processing of the list.</td></tr>
<tr><td>3</td><td>R/W</td><td>R</td><td>0x0</td><td>IsochronousEnable
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame,</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0404</th><th colspan="2">Register Name: O_HcControl</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td></td><td></td><td></td><td></td><td>HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.
Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).</td></tr>
<tr><td>2</td><td>R/W</td><td>R</td><td>0x0</td><td>PeriodicListEnable
This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlBulkServiceRatio
This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
<table>
<tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr>
<tr><td>0</td><td>1:1</td></tr>
<tr><td>1</td><td>2:1</td></tr>
<tr><td>2</td><td>3:1</td></tr>
<tr><td>3</td><td>4:1</td></tr>
</table>
The default value is 0x0.</td></tr>
</table>

10.5.7.16 0x0408 OHCI Command Status Register (Default Value:0x0000_0000)

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:18	/	/	0x0	Reserved

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus (Offset: 0x040C) has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus (Offset: 0x040C). After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
0	R/W	R/E	0x0	**HostControllerReset** This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl (Offset: 0x404), and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

10.5.7.17 0x040C OHCI Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of HcRhStatus (Offset: 0x450) or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of HcFmNumber (Offset: 0x43C,bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber (Offset:0x43C) has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.

Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus (Offset: 0x408) to be Incremented.

10.5.7.18 0x0410 OHCI Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

10.5.7.19 0x0414 OHCI Interrupt Disable Register (Default Value:0x0000_0000)

Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Resume Detected;

<table>
<tr><th colspan="4">Offset: 0x0414</th><th colspan="2">Register Name: O_HcInterruptDisable</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>2</td><td>R/W</td><td>R</td><td>0x0</td><td>StartofFrame Interrupt Disable
0 Ignore;
1 Disable interrupt generation due to Start of Flame;</td></tr>
<tr><td>1</td><td>R/W</td><td>R</td><td>0x0</td><td>WritebackDoneHead Interrupt Disable
0 Ignore;
1 Disable interrupt generation due to Write back Done Head;</td></tr>
<tr><td>0</td><td>R/w</td><td>R</td><td>0x0</td><td>SchedulingOverrun Interrupt Disable
0 Ignore;
1 Disable interrupt generation due to Scheduling Overrun;</td></tr>
</table>

10.5.7.20 0x0418 OHCI HCCA Register (Default Value:0x0000_0000)

Offset: 0x0418				Register Name: O_HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

10.5.7.21 0x041C OHCI Period Current ED Register (Default Value:0x0000_0000)

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED[31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
3:0	R	R	0x0	PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.7.22 0x0420 OHCI Control Head ED Register (Default Value:0x0000_0000)

Offset: 0x0420				Register Name: O_HcControlHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.7.23 0x0424 OHCI Control Current ED Register (Default Value:0x0000_0000)

Offset: 0x0424				Register Name: HcControlCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus (Offset: 0x0408). If set, it copies the content of HcControlHeadED (Offset: 0x0420) to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl (Offset: 0x0404) is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.7.24 0x0428 OHCI Bulk Head ED Register (Default Value:0x0000_0000)

Offset: 0x0428				Register Name: O_HcBulkHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.7.25 0x042C OHCI Bulk Current ED Register (Default Value:0x0000_0000)

Offset: 0x042C				Register Name: O_HcBulkCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl (Offset: 0x0404). If set, it copies the content of HcBulkHeadED (Offset: 0x0428) to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl (Offset: 0x0404) is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.7.26 0x0430 OHCI Done Head Register (Default Value:0x0000_0000)

Offset: 0x0430				Register Name: O_HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus (Offset: 0x040C).
3:0	R	R	0x0	HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.5.7.27 0x0434 OHCI Frame Interval Register (Default Value:0x0000_2EDF)

Offset: 0x0434				Register Name: O_HcFmInterval
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus (Offset: 0x408) as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

10.5.7.28 0x0438 OHCI Frame Remaining Register (Default Value:0x0000_0000)

Offset: 0x0438				Register Name: O_HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval (Offset: 0x0434) whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval (Offset: 0x0434) at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of HcFmInterval (Offset: 0x0434) and uses the updated value from the next SOF.

10.5.7.29 0x043C OHCI Frame Number Register (Default Value:0x0000_0000)

Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/
15:0	R	R/W	0x0	FrameNumber This is incremented when HcFmRemaining (Offset: 0x0438) is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus (Offset: 0x040C).

10.5.7.30 0x0440 OHCI Periodic Start Register (Default Value:0x0000_0000)

Offset: 0x0440				Register Name: O_HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval (Offset: 0x0434). A typical value will be 0x2A3F (0x3e67??). When HcFmRemaining (Offset: 0x0438) reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

10.5.7.31 0x0444 OHCI LS Threshold Register (Default Value:0x0000_0628)

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	/

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

10.5.7.32 0x0448 OHCI Root Hub DescriptorA Register (Default Value:0x0200_1201)

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	0x1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 Over-current status is reported collectively for all downstream ports. 1 No overcurrent protection supported.
11	R/W	R	0x0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 Over-current status is reported collectively for all downstream ports. 1 Over-current status is reported on per-port basis.
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.

<table>
<tr><th colspan="3">Offset: 0x0448</th><th colspan="2">Register Name: O_HcRhDescriptorA</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>9</td><td>R/W</td><td>R</td><td>0x1</td><td>PowerSwitchingMode
This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared.<table><tr><td>0</td><td>All ports are powered at the same time.</td></tr><tr><td>1</td><td>Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port
switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).</td></tr></table></td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>NoPowerSwithcing
These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.<table><tr><td>0</td><td>Ports are power switched.</td></tr><tr><td>1</td><td>Ports are always powered on when the HC is powered on.</td></tr></table></td></tr>
<tr><td>7:0</td><td>R</td><td>R</td><td>0x01</td><td>NumberDownstreamPorts
These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.</td></tr>
</table>

10.5.7.33 0x044C OHCI Root Hub DescriptorB Register (Default Value:0x0000_0000)

Offset: 0x044C				Register Name: O_HcRhDescriptorB
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. … Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. … Bit15 Device attached to Port #15.

10.5.7.34 0x0450 OHCI Root Hub Status Register (Default Value:0x0000_0000)

Offset: 0x0450				Register Name: O_HcRhStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	(write)ClearRemoteWakeupEnable Write a ‘1’ clears DeviceRemoteWakeupEnable. Write a ‘0’ has no effect.
30:18	/	/	/	/
17	R/W	R	0x0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a ‘1’.Writing a ‘0’ has no effect.

<table>
<tr><th colspan="4">Offset: 0x0450</th><th>Register Name: O_HcRhStatus</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>16</td><td>R/W</td><td>R</td><td>0x0</td><td>(read)LocalPowerStartusChange
The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’.
(write)SetGlobalPower
In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.</td></tr>
<tr><td>15</td><td>R/W</td><td>R</td><td>0x0</td><td>(read)DeviceRemoteWakeupEnable
This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt.
<table><tr><td>0</td><td>ConnectStatusChange is not a remote wakeup event.</td></tr><tr><td>1</td><td>ConnectStatusChange is a remote wakeup event.</td></tr></table>
(write)SetRemoteWakeupEnable
Writing a ‘1’ sets DeviceRemoveWakeupEnable. Writing a ‘0’ has no effect.</td></tr>
<tr><td>14:2</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>1</td><td>R</td><td>R/W</td><td>0x0</td><td>OverCurrentIndicator
This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal.
If per-port overcurrent protection is implemented this bit is always ‘0’</td></tr>
<tr><td>0</td><td>R/W</td><td>R</td><td>0x0</td><td>(Read)LocalPowerStatus
When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as ‘0’.
(Write)ClearGlobalPower
When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.</td></tr>
</table>

10.5.7.35 0x0454 OHCI Root Hub Port Status Register (Default Value:0x0000_0100)

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortEnableStatus 1 change in PortEnableStatus

<table>
<tr><th colspan="3">Offset: 0x0454</th><th colspan="2">Register Name: O_HcRhPortStatus</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>16</td><td>R/W</td><td>R/W</td><td>0x0</td><td>ConnectStatusChange
This bit is set whenever a connect or disconnect event occurs. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If
CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.
<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.
<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0454</th><th colspan="2">Register Name: O_HcRhPortStatus</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls
this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>(write)SetPortPower
The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect.
Note: This bit is always reads '1b' if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if
CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>(write)SetPortReset
The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0454</th><th colspan="2">Register Name: O_HcRhPortStatus</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when
PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
</table>

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
1	R/W	R/W	0x0	(read)PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 port is disabled 1 port is enabled (write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0 No device connected 1 Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. **Note: This bit is always read '1' when the attached device is nonremovalble (DviceRemoveable[NumberDownstreamPort]).**

10.5.7.36 0x0800 HCI Interface Register (Default Value:0x0000_0000)

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB Standby Clock Sel 0: normal mode USB clock as usual 1: standby mode USB clock switch to RC 16M clock
30:29	/	/	Reserved.

Offset: 0x0800			Register Name: USB_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R	0x1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0x0	OHCI count select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time
24	R/W	0x0	Simulation mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect
23:21	/	/	/
20	R/W	0x0	EHCI HS force Set 1 to this field force the EHCI enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19	/	/	/
18	R/W	0x0	1: within 2us of the resume-K to SE0 transition 0: random time value of the resume-K to SE0 transition
17:13	/	/	/
12	R/W	0x0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0x0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0x0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: do not use INCR8,use other enabled INCRX or unspecified length burst INCR
9	R/W	0x0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: do not use INCR4,use other enabled INCRX or unspecified length burst INCR

Offset: 0x0800			Register Name: USB_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	AHB Master interface INCRX align enable 1: start INCRx burst only on burst x-align address 0: Start burst on any double word boundary **Note: This bit must enable if any bit of 11:9 is enabled.**
7:4	/	/	/
3	R/W	0x0	RC Clock Gating 0x0: clock gated 0x1: clock ungated
2	R/W	0x0	RC Generation Enable 0x0: disable 0x1: enable
1	/	/	/
0	R/W	0x0	ULPI bypass enable。 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

10.5.7.37 0x0808 HCI Control 3 Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: HCI_CTRL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	Reserved.
16	R/W1C	0x1	Linestate Change Detect 0: Linestate change not dected. 1: Linestate change dected. Write '1' to clear.
15:4	/	/	Reserved.
3	R/W	0x0	Remote Wakeup Enable 1: Enable 0: Disable
2	/	/	Reserved.
1	R/W	0x0	Linestate Change Interrupt Enable 1: Enable 0: Disable
0	R/W	0x0	Linestate Change Detect Enable 1: Enable 0: Disable

10.5.7.38 0x0810 PHY Control Register (Default Value: 0x0000_0008)

Offset: 0x0810			Register Name: PHY_CTRL(Default Value: 0x0000_0008)
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	BIST_EN_A
15:8	R/W	0x0	VC_ADDR
7	R/W	0x0	VC_DI
6:4	/	/	/
3	R/W	0x1	SIDDQ 1: Write 1 to disable PHY. 0: Write 0 to enable PHY.
2	/	/	/
1	R/W	0x0	VC_EN 0: Write 0 to disable PHY VC bus 1: Write 1 to enable PHY VC bus. **Note: Only 1 VC bus of all the USB controllers could be enabled at the same time.**
0	R/W	0x0	VC_CLK

10.5.7.39 0x0824 PHY Status Register(USB1) (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: PHY_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x0	BIST_ERROR
16	R	0x0	BIST_DONE
15:1	/	/	/
0	R	0x0	VC_DO

10.5.7.40 0x0828 HCI SIE Port Disable Control Register (Default Value:0x0000_0003)

Offset: 0x0828			Register Name: USB_SPDCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:5	/	/	/
4	R/W	0x0	Resume_Sel When set k-se0 transition 2us, setting this bit to 1, which is cooperated with SS_UTMI_BACKWARD_ENB_I.
3:2	/	/	/

Offset: 0x0828			Register Name: USB_SPDCR
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x3	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 Frames

10.6 GPIO

10.6.1 Overview

The general purpose input/output (GPIO) is one of the blocks controlling the chip multiplexing pins. V851S supports 6 groups of GPIO pins and V851SE supports 5 groups of GPIO pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

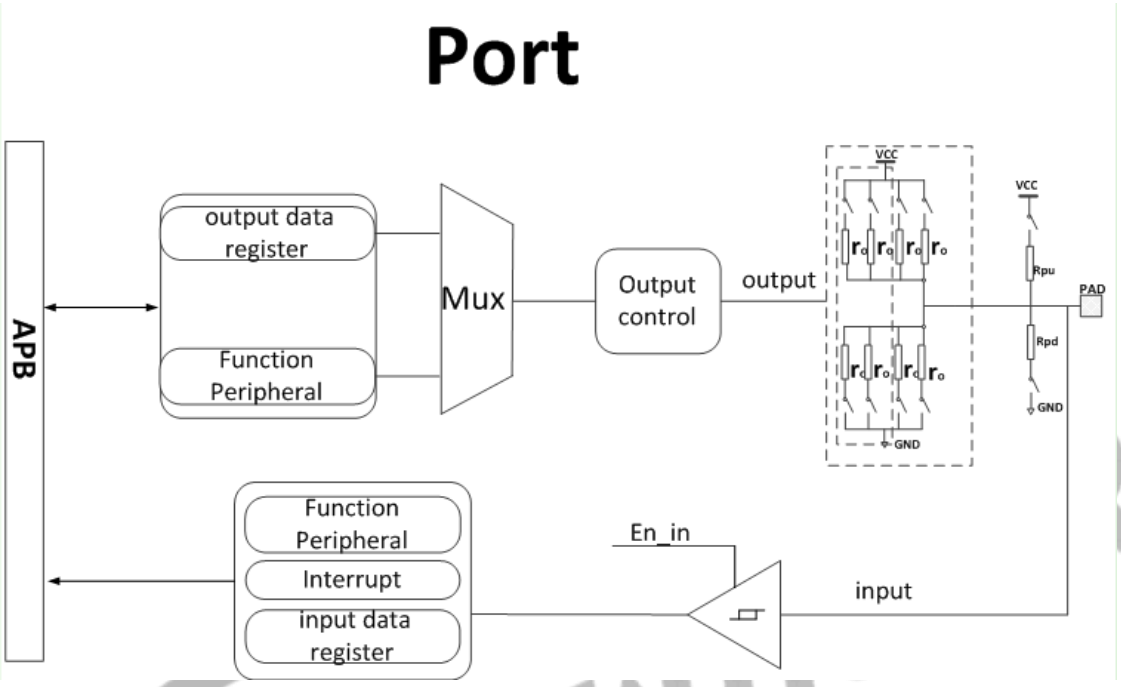
The port controller has the following features:

- 6 ports (PA, PC, PD, PE, PF, PH) for V851S
- 5 ports (PA, PC, PE, PF, PH) for V851SE
- Software control for each signal pin
- Each GPIO peripheral can produce an interrupt
- Pull_up/Pull_down/no_Pull register control
- Controls the direction of every signal
- 4 drive strengths in each operating mode
- Up to 58 interrupts for V851S
- Up to 46 interrupts for V851SE
- Configurable interrupt edges

10.6.2 Block Diagram

The following figure shows the block diagram of the GPIO.

Figure 10-62 GPIO Block Diagram



The GPIO consists of the digital part (GPIO, external interface) and IO analog part (output buffer, dual pull down, pad). The digital part can select the output interface by the MUX switch; the analog part can configure pull up/down and buffer strength.

When executing GPIO read state, the GPIO reads the current level of the pin into the internal register bus. When not executing GPIO read state, the external pin and the internal register bus are off-status, which is high-impedance.

10.6.3 Functional Description

10.6.3.1 Multi-function Port

The V851S includes 58 multi-functional input/output port pins. There are 6 ports as listed below.

Table 10-18 V851S Multi-function Port

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Typical Power Supply
PA	12	Schmitt	CMOS	CSI/ CLK-FANOUT/PWM/UART/TWI/PA-EINT	1.8V
PC	6	Schmitt	CMOS	BOOT-SEL /SDC/SPI/PWM/TWI/PC-EINT	3.3V/1.8V
PD	12	Schmitt	CMOS	LCD/SPI/DSI/DMIC/RMII/TWI/PWM/UART/PD-EINT	3.3V
PE	14	Schmitt	CMOS	CSI/I2S/PWM/RMII/SDC/TWI/UART/WIEGAND/PE-EINT	3.3V/1.8V
PF	7	Schmitt	CMOS	SDC/SPI/JTAG/UART/PF-EINT	3.3V
PH	7	Schmitt	CMOS	CSI/ CLK-FANOUT/DMIC/JTAG/PWM/TWI/UART/RMII/ WIEGAND/PH-EINT	3.3V

The V851SE includes 46 multi-functional input/output port pins. There are 5 ports as listed below.

Table 10-19 V851SE Multi-function Port

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Typical Power Supply
PA	12	Schmitt	CMOS	CSI/ CLK-FANOUT/PWM/UART/TWI/PA-EINT	1.8V
PC	6	Schmitt	CMOS	BOOT-SEL/SDC/SPI/PWM/TWI/PC-EINT	3.3V/1.8V
PE	14	Schmitt	CMOS	CSI/I2S/PWM/SDC/TWI/UART/WIEGAND/PE-EINT	3.3V/1.8V
PF	7	Schmitt	CMOS	SDC/SPI/JTAG/UART/PF-EINT	3.3V
PH	7	Schmitt	CMOS	CSI/ CLK-FANOUT/DMIC/JTAG/PWM/TWI/UART/ WIEGAND/PH-EINT	3.3V

10.6.3.2 GPIO Multiplex Function

V851S

The following tables show the multiplex function pins of the V851S.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

Table 10-20 V851S PA Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PA0	MIPIA_CSI_CK0P							PA_EINT0
PA1	MIPIA_CSI_CK0N							PA_EINT1
PA2	MIPIA_CSI_D1N							PA_EINT2
PA3	MIPIA_CSI_D1P							PA_EINT3
PA4	MIPIA_CSI_D0P							PA_EINT4
PA5	MIPIA_CSI_D0N							PA_EINT5
PA6	MIPIB-CSI-D0N/MIPIA-CSI-D2N		TWI1_SCK	PWM0				PA_EINT6
PA7	MIPIB-CSI-D0P/MIPIA-CSI-D2P		TWI1_SDA	PWM1				PA_EINT7
PA8	MIPIB-CSI-D1N/MIPIA-CSI-D3N	TWI4_SCK	TWI3_SCK	PWM2	UART2_TX			PA_EINT8
PA9	MIPIB-CSI-D1P/MIPIA-CSI-D3P	TWI4_SDA	TWI3_SDA	PWM3	UART2_RX			PA_EINT9
PA10	MIPIB_CSI_CK0N		MIPI_CSI_MCLK0	TWI0_SCK	CLK_FANOUT0			PA_EINT10
PA11	MIPIB_CSI_CK0P		MIPI_CSI_MCLK1	TWI0_SDA	CLK_FANOUT1			PA_EINT11

Table 10-21 V851S PC Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PC0		SDC2_CLK	SPI0_CLK					PC_EINT0
PC1		SDC2_CMD	SPI0_CS0					PC_EINT1
PC2		SDC2_D2	SPI0_MOSI	BOOT_SEL0				PC_EINT2
PC3		SDC2_D1	SPI0_MISO	BOOT_SEL1				PC_EINT3
PC4		SDC2_D0	SPI0_WP	PWM4	TWI1_SCK			PC_EINT4
PC5		SDC2_D3	SPI0_HOLD	PWM5	TWI1_SDA			PC_EINT5

Table 10-22 V851S PD Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PD1	LCD_D3	PWM0	RMII_RXD1	DSI_D0N	SPI1_CS0/DBI_CSX			PD_EINT1
PD2	LCD_D4	PWM1	RMII_RXD0	DSI_D0P	SPI1_CLK/DBI_SCLK			PD_EINT2
PD3	LCD_D5	PWM2	RMII_CRS_DV	DSI_D1N	SPI1_MOSI/DBI_SDO			PD_EINT3
PD4	LCD_D6	PWM3	RMII_RXER	DSI_D1P	SPI1_MISO/ DBI_SDI/ DBI_TE/DBI_DCX			PD_EINT4
PD5	LCD_D7	PWM4	RMII_TXD1	DSI_CKN	SPI1_HOLD/DBI_DCX/ DBI_WRX			PD_EINT5
PD6	LCD_D10	PWM5	RMII_TXD0	DSI_CKP	SPI1_WP/DBI_TE			PD_EINT6
PD7	LCD_D11	PWM6	RMII_TXCK		SPI1_CS1			PD_EINT7
PD8	LCD_D12	PWM7	RMII_TXEN					PD_EINT8
PD18	LCD_CLK		EPHY_25M	SPI2_CLK	TWI3_SCK	UART2_TX		PD_EINT18
PD19	LCD_DE	PWM9	TCON_TRIG	SPI2_MOSI	TWI3_SDA	UART2_RX		PD_EINT19
PD20	LCD_HSYNC	PWM10	MDC	SPI2_MISO	TWI2_SCK	UART2_RTS		PD_EINT20
PD21	LCD_VSYNC		MDIO	SPI2_CS0	TWI2_SDA	UART2_CTS		PD_EINT21

Table 10-23 V851S PE Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PE0	NCSI_PCLK	RMII_RXD1	I2S1_MCLK	PWM0	SDC1_CLK	UART3_TX	TWI3_SCK	PE_EINT0
PE1	NCSI_MCLK	RMII_TXCK	I2S1_BCLK	PWM1	SDC1_CMD	UART3_RX	TWI3_SDA	PE_EINT1
PE2	NCSI_HSYNC	MII_CRS_DV	I2S1_LRCK	PWM2	SDC1_D0	UART3_CTS	TWI1_SCK	PE_EINT2
PE3	NCSI_VSYNC	RMII_RXD0	I2S1_DIN0	PWM3	SDC1_D1	UART3_RTS	TWI1_SDA	PE_EINT3
PE4	NCSI_D0	RMII_TXD0	I2S1_DOUT0	PWM4	SDC1_D2	TWI3_SCK	TWI0_SCK	PE_EINT4
PE5	NCSI_D1	RMII_TXD1		PWM5	SDC1_D3	TWI3_SDA	TWI0_SDA	PE_EINT5
PE6	NCSI_D2	RMII_TXEN		PWM6	UART1_TX		TWI4_SCK	PE_EINT6
PE7	NCSI_D3	RMII_RXER		PWM7	UART1_RX	I2S1_DOUT0	TWI4_SDA	PE_EINT7
PE8	NCSI_D4	MDC		PWM8	WIEGAND_D0	I2S1_DIN0	TWI1_SCK	PE_EINT8
PE9	NCSI_D5	MDIO		PWM9	WIEGAND_D1	I2S1_LRCK	TWI1_SDA	PE_EINT9
PE10	NCSI_D6	EPHY_25M		PWM10	UART2_RTS	I2S1_BCLK	WIEGAND_D0	PE_EINT10
PE11	NCSI_D7			CSI_SM_VS	UART2_CTS	I2S1_MCLK	WIEGAND_D1	PE_EINT11
PE12	NCSI_D8			MIPI_CSI_MCLK0	UART2_TX	UART3_TX		PE_EINT12
PE13	NCSI_D9			MIPI_CSI_MCLK1	UART2_RX	UART3_RX		PE_EINT13

Table 10-24 V851S PF Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PF0	SDC0_D1	JTAG_MS	SPI0_CLK	SPI2_CLK	R_JTAG_MS	CPU_BIST0		PF_EINT0
PF1	SDC0_D0	JTAG_DI	SPI0_MOSI	SPI2_MOSI	R_JTAG_DI	CPU_BIST1		PF_EINT1
PF2	SDC0_CLK	UART0_TX	SPI0_MISO	SPI2_MISO				PF_EINT2
PF3	SDC0_CMD	JTAG_DO	SPI0_CS0	SPI2_CS0	R_JTAG_DO			PF_EINT3
PF4	SDC0_D3	UART0_RX	SPI0_CS1	SPI2_CS1				PF_EINT4
PF5	SDC0_D2	JTAG_CK			R_JTAG_CK			PF_EINT5
PF6	DBG_CLK							PF_EINT6

Table 10-25 V851S PH Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PH0	PWM0							PH_EINT0
PH9	PWM9		TWI3_SCK	UART0_TX		DMIC_DATA0		PH_EINT9
PH10	PWM10		TWI3_SDA	UART0_RX		DMIC_CLK		PH_EINT10
PH11	JTAG_MS		R_JTAG_MS	TWI2_SCK	SPI3_CLK	CLK_FANOUT0	PWM4	PH_EINT11
PH12	JTAG_CK		R_JTAG_CK	TWI2_SDA	SPI3_MOSI	CLK_FANOUT1	PWM5	PH_EINT12
PH13	JTAG_DO	MDC	R_JTAG_DO	TWI3_SCK	SPI3_MISO	WIEGAND_D0	PWM6	PH_EINT13
PH14	JTAG_DI	MDIO	R_JTAG_DI	TWI3_SDA	SPI3_CS0	WIEGAND_D1	PWM7	PH_EINT14

The following tables show the multiplex function pins of the V851SE.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function9 to Function13 are reserved.

Table 10-26 V851SE PA Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PA0	MIPIA_CSI_CK0P							PA_EINT0
PA1	MIPIA_CSI_CK0N							PA_EINT1
PA2	MIPIA_CSI_D1N							PA_EINT2
PA3	MIPIA_CSI_D1P							PA_EINT3
PA4	MIPIA_CSI_D0P							PA_EINT4
PA5	MIPIA_CSI_D0N							PA_EINT5
PA6	MIPIB-CSI-D0N/MIPIA-CSI-D2N		TWI1_SCK	PWM0				PA_EINT6
PA7	MIPIB-CSI-D0P/MIPIA-CSI-D2P		TWI1_SDA	PWM1				PA_EINT7
PA8	MIPIB-CSI-D1N/MIPIA-CSI-D3N	TWI4_SCK	TWI3_SCK	PWM2	UART2_TX			PA_EINT8
PA9	MIPIB-CSI-D1P/MIPIA-CSI-D3P	TWI4_SDA	TWI3_SDA	PWM3	UART2_RX			PA_EINT9
PA10	MIPIB_CSI_CK0N		MIPI_CSI_MCLK0	TWI0_SCK	CLK_FANOUT0			PA_EINT10
PA11	MIPIB_CSI_CK0P		MIPI_CSI_MCLK1	TWI0_SDA	CLK_FANOUT1			PA_EINT11

Table 10-27 V851SE PC Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PC0		SDC2_CLK	SPI0_CLK					PC_EINT0
PC1		SDC2_CMD	SPI0_CS0					PC_EINT1
PC2		SDC2_D2	SPI0_MOSI	BOOT_SEL0				PC_EINT2
PC3		SDC2_D1	SPI0_MISO	BOOT_SEL1				PC_EINT3
PC4		SDC2_D0	SPI0_WP	PWM4	TWI1_SCK			PC_EINT4
PC5		SDC2_D3	SPI0_HOLD	PWM5	TWI1_SDA			PC_EINT5

Table 10-28 V851SE PE Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PE0	NCSI_PCLK		I2S1_MCLK	PWM0	SDC1_CLK	UART3_TX	TWI3_SCK	PE_EINT0
PE1	NCSI_MCLK		I2S1_BCLK	PWM1	SDC1_CMD	UART3_RX	TWI3_SDA	PE_EINT1
PE2	NCSI_HSYNC		I2S1_LRCK	PWM2	SDC1_D0	UART3_CTS	TWI1_SCK	PE_EINT2
PE3	NCSI_VSYNC		I2S1_DIN0	PWM3	SDC1_D1	UART3_RTS	TWI1_SDA	PE_EINT3
PE4	NCSI_D0		I2S1_DOUT0	PWM4	SDC1_D2	TWI3_SCK	TWI0_SCK	PE_EINT4
PE5	NCSI_D1			PWM5	SDC1_D3	TWI3_SDA	TWI0_SDA	PE_EINT5
PE6	NCSI_D2			PWM6	UART1_TX		TWI4_SCK	PE_EINT6
PE7	NCSI_D3			PWM7	UART1_RX	I2S1_DOUT0	TWI4_SDA	PE_EINT7
PE8	NCSI_D4			PWM8	WIEGAND_D0	I2S1_DIN0	TWI1_SCK	PE_EINT8
PE9	NCSI_D5			PWM9	WIEGAND_D1	I2S1_LRCK	TWI1_SDA	PE_EINT9
PE10	NCSI_D6			PWM10	UART2_RTS	I2S1_BCLK	WIEGAND_D0	PE_EINT10
PE11	NCSI_D7			CSI_SM_VS	UART2_CTS	I2S1_MCLK	WIEGAND_D1	PE_EINT11
PE12	NCSI_D8			MIPI_CSI_MCLK0	UART2_TX	UART3_TX		PE_EINT12
PE13	NCSI_D9			MIPI_CSI_MCLK1	UART2_RX	UART3_RX		PE_EINT13

Table 10-29 V851SE PF Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PF0	SDC0_D1	JTAG_MS	SPI0_CLK	SPI2_CLK	R_JTAG_MS	CPU_BIST0		PF_EINT0
PF1	SDC0_D0	JTAG_DI	SPI0_MOSI	SPI2_MOSI	R_JTAG_DI	CPU_BIST1		PF_EINT1
PF2	SDC0_CLK	UART0_TX	SPI0_MISO	SPI2_MISO				PF_EINT2
PF3	SDC0_CMD	JTAG_DO	SPI0_CS0	SPI2_CS0	R_JTAG_DO			PF_EINT3
PF4	SDC0_D3	UART0_RX	SPI0_CS1	SPI2_CS1				PF_EINT4
PF5	SDC0_D2	JTAG_CK			R_JTAG_CK			PF_EINT5
PF6	DBG_CLK							PF_EINT6

Table 10-30 V851SE PH Multiplex Function

GPIO Port	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 14
PH0	PWM0							PH_EINT0
PH9	PWM9		TWI3_SCK	UART0_TX		DMIC_DATA0		PH_EINT9
PH10	PWM10		TWI3_SDA	UART0_RX		DMIC_CLK		PH_EINT10
PH11	JTAG_MS		R_JTAG_MS	TWI2_SCK	SPI3_CLK	CLK_FANOUT0	PWM4	PH_EINT11
PH12	JTAG_CK		R_JTAG_CK	TWI2_SDA	SPI3_MOSI	CLK_FANOUT1	PWM5	PH_EINT12
PH13	JTAG_DO		R_JTAG_DO	TWI3_SCK	SPI3_MISO	WIEGAND_D0	PWM6	PH_EINT13
PH14	JTAG_DI		R_JTAG_DI	TWI3_SDA	SPI3_CS0	WIEGAND_D1	PWM7	PH_EINT14

10.6.3.3 Port Function

The Port Controller supports 6 GPIOs, every GPIO can configure as Input, Output, Function Peripheral, IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 10-31 Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/: non-configure, configuration is invalid

Y: configure

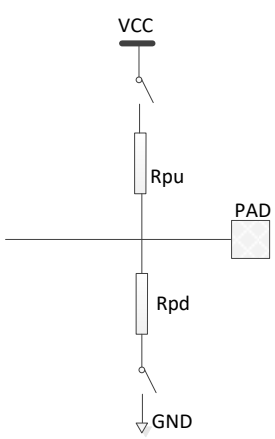
X: Select configuration according to the actual situation

N: Forbid to configure

10.6.3.4 Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

Figure 10-63 Pull up/down Logic



High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, the software configures the switch on Rpu and Rpd as off, and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by resistance, the resistance has a current-limiting function. When pulling up, the switch on Rpu is conducted by software configuration, the IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is conducted by software configuration, the IO is pulled down to GND by Rpd.

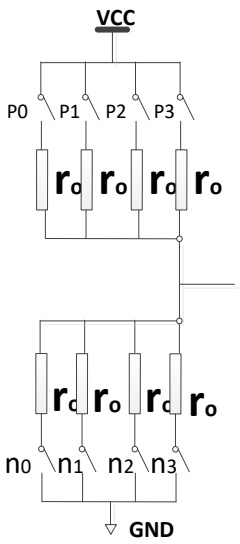
The pull-up/down of each IO is weak pull-up/down.

The setting of pull-down, pull-up, high-impedance is decided by the external circuit.

10.6.3.5 Buffer Strength

Each IO can be set as different buffer strength. The IO buffer diagram is as follows.

Figure 10-64 IO Buffer Strength Diagram



When output high level, the n0, n1, n2, n3 of NMOS is off, the p0, p1, p2, p3 of PMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the p0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the p0, p1, and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, the p0, p1, p2, and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0, p1, p2, p3 of PMOS is off, the n0, n1, n2, n3 of NMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the n0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the n0, n1, and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When the buffer strength is 3, the n0, n1, n2, and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between the output driver circuit and the port is unconnected, the driver configuration is invalid.

10.6.3.6 Interrupt

Each group IO has an independent interrupt number. The IO within-group uses one interrupt number when one IO generates interrupt, the GPIO pins sent interrupt request to interrupt module. External Interrupt Status Register is used to query which IO generates interrupt.

The interrupt trigger of GPIO supports the following trigger types.

- Positive Edge: When a low level changes to a high level, the interrupt will generate. No matter how long a high level keeps, the interrupt generates only once.
- Negative Edge: When a high level changes to a low level, the interrupt will generate. No matter how long a low level keeps, the interrupt generates only once.
- High Level: Just keep a high level and the interrupt will always generate.
- Low Level: Just keep a low level and the interrupt will always generate.
- Double Edge: Positive and negative edge.

External Interrupt Configure Register is used to configure the trigger type.

The GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using a lower sample clock, to reach the debounce effect because the dither frequency of the signal is higher than the sample frequency.

Set the sample clock source by PIO_INT_CLK_SELECT and the prescale factor by DEB_CLK_PRE_SCALE.

10.6.4 Register List

Module Name	Base Address
GPIO	0x02000000

Register Name	Offset	Description
PA_CFG0	0x0000	PA Configure Register 0
PA_CFG1	0x0004	PA Configure Register 1
PA_DAT	0x0010	PA Data Register
PA_DRV0	0x0014	PA Multi_Driving Register 0
PA_DRV1	0x0018	PA Multi_Driving Register 1
PA_PUL0	0x0024	PA Pull Register 0
PC_CFG0	0x0060	PC Configure Register 0
PC_DAT	0x0070	PC Data Register
PC_DRV0	0x0074	PC Multi_Driving Register 0
PC_PUL	0x0084	PC Pull Register
PD_CFG0	0x0090	PD Configure Register 0

Register Name	Offset	Description
PD_CFG1	0x0094	PD Configure Register 1
PD_CFG2	0x0098	PD Configure Register 2
PD_DAT	0x00A0	PD Data Register
PD_DRV0	0x00A4	PD Multi_Driving Register 0
PD_DRV1	0x00A8	PD Multi_Driving Register 1
PD_DRV2	0x00AC	PD Multi_Driving Register 2
PD_PUL0	0x00B4	PD Pull Register 0
PD_PUL1	0x00B8	PD Pull Register 1
PE_CFG0	0x00C0	PE Configure Register 0
PE_CFG1	0x00C4	PE Configure Register 1
PE_DAT	0x00D0	PE Data Register
PE_DRV0	0x00D4	PE Multi_Driving Register 0
PE_DRV1	0x00D8	PE Multi_Driving Register 1
PE_PUL0	0x00E4	PE Pull Register 0
PF_CFG	0x00F0	PF Configure Register
PF_DAT	0x0100	PF Data Register
PF_DRV	0x0104	PF Multi_Driving Register
PF_PUL	0x0114	PF Pull Register
PH_CFG0	0x0150	PH Configure Register 0
PH_CFG1	0x0154	PH Configure Register 1
PH_DAT	0x0160	PH Data Register
PH_DRV0	0x0164	PH Multi_Driving Register 0
PH_DRV1	0x0168	PH Multi_Driving Register 1
PH_PUL	0x0174	PH Pull Register
PA_INT_CFG0	0x0200	PA External Interrupt Configure Register 0
PA_INT_CFG1	0x0204	PA External Interrupt Configure Register 1
PA_INT_CTL	0x0210	PA External Interrupt Control Register
PA_INT_STA	0x0214	PA External Interrupt Status Register
PA_INT_DEB	0x0218	PA External Debounce Configure Register
PC_INT_CFG0	0x0240	PC External Interrupt Configure Register 0
PC_INT_CTL	0x0250	PC External Interrupt Control Register
PC_INT_STA	0x0254	PC External Interrupt Status Register
PC_INT_DEB	0x0258	PC External Debounce Configure Register
PD_INT_CFG0	0x0260	PD External Interrupt Configure Register 0
PD_INT_CFG1	0x0264	PD External Interrupt Configure Register 1
PD_INT_CFG2	0x0268	PD External Interrupt Configure Register 2
PD_INT_CTL	0x0270	PD External Interrupt Control Register
PD_INT_STA	0x0274	PD External Interrupt Status Register
PD_INT_DEB	0x0278	PD External Debounce Configure Register
PE_INT_CFG0	0x0280	PE External Interrupt Configure Register 0
PE_INT_CFG1	0x0284	PE External Interrupt Configure Register 1
PE_INT_CTL	0x0290	PE External Interrupt Control Register

Register Name	Offset	Description
PE_INT_STA	0x0294	PE External Interrupt Status Register
PE_INT_DEB	0x0298	PE External Debounce Configure Register
PF_INT_CFG	0x02A0	PF External Interrupt Configure Register
PF_INT_CTL	0x02B0	PF External Interrupt Control Register
PF_INT_STA	0x02B4	PF External Interrupt Status Register
PF_INT_DEB	0x02B8	PF External Debounce Configure Register
PH_INT_CFG0	0x02E0	PH External Interrupt Configure Register 0
PH_INT_CFG1	0x02E4	PH External Interrupt Configure Register 1
PH_INT_CTL	0x02F0	PH External Interrupt Control Register
PH_INT_STA	0x02F4	PH External Interrupt Status Register
PH_INT_DEB	0x02F8	PH External Debounce Configure Register
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_MS_CTL	0x0344	PIO Group Withstand Voltage Mode Select Control Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register
PIO_POW_VAL_SET_CTL	0x0350	PIO Group Power Voltage Select Control Register

10.6.5 V851S GPIO Register Description

10.6.5.1 0x0000 PA Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	PA7_SELECT PA7 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D0P/MIPIA-CSI-D2P 0011: Reserved 0100: TWI1_SDA 0101: PWM1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT7 1111: IO Disable

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	0xF	PA6_SELECT PA6 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D0N/MIPIA-CSI-D2N 0011: Reserved 0100: TWI1_SCK 0101: PWM0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT6 1111: IO Disable
23:20	R/W	0xF	PA5_SELECT PA5 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT5 1111: IO Disable
19:16	R/W	0xF	PA4_SELECT PA4 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D0P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT4 1111: IO Disable
15:12	R/W	0xF	PA3_SELECT PA3 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D1P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT3 1111: IO Disable

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0xF	PA2_SELECT PA2 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D1N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT2 1111: IO Disable
7:4	R/W	0xF	PA1_SELECT PA1 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_CK0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT1 1111: IO Disable
3:0	R/W	0xF	PA0_SELECT PA0 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_CK0P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT0 1111: IO Disable

10.6.5.2 0x0004 PA Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0004			Register Name: PA_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

Offset: 0x0004			Register Name: PA_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0xF	PA11_SELECT PA11 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_CK0P 0011: Reserved 0100: MIPI_CSI_MCLK1 0101: TWI0_SDA 0110: CLK_FANOUT1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT11 1111: IO Disable
11:8	R/W	0xF	PA10_SELECT PA10 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_CK0N 0011: Reserved 0100: MIPI_CSI_MCLK0 0101: TWI0_SCK 0110: CLK_FANOUT0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT10 1111: IO Disable
7:4	R/W	0xF	PA9_SELECT PA9 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D1P/MIPIA-CSI-D3P 0011: TWI4_SDA 0100: TWI3_SDA 0101: PWM3 0110: UART2_RX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT9 1111: IO Disable
3:0	R/W	0xF	PA8_SELECT PA8 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D1N/MIPIA-CSI-D3N 0011: TWI4_SCK 0100: TWI3_SCK 0101: PWM2 0110: UART2_TX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT8 1111: IO Disable

10.6.5.3 0x0010 PA Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PA_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	0	PA_DAT PA Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.4 0x0014 PA Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0014			Register Name: PA_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	PA7_DRV PA7 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PA6_DRV PA6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PA5_DRV PA5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PA4_DRV PA4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PA3_DRV PA3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/

Offset: 0x0014			Register Name: PA_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x1	PA2_DRV PA2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PA1_DRV PA1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PA0_DRV PA0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.5 0x0018 PA Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0018			Register Name: PA_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PA11_DRV PA11 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PA10_DRV PA10 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PA9_DRV PA9 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PA8_DRV PA8 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.6 0x0024 PA Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PA_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x0	PA11_PULL PA11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PA10_PULL PA10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PA9_PULL PA9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PA8_PULL PA8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PA7_PULL PA7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PA6_PULL PA6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PA5_PULL PA5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PA4_PULL PA4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PA3_PULL PA3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0024			Register Name: PA_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
5:4	R/W	0x0	PA2_PULL PA2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PA1_PULL PA1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PA0_PULL PA0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.5.7 0x0060 PC Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0060			Register Name: PC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0xF	PC5_SELECT PC5 Select. 0000: Input 0001: Output 0010: Reserved 0011: SDC2_D3 0100: SPI0_HOLD 0101: PWM5 0110: TWI1_SDA 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC_EINT5 1111: IO Disable
19:16	R/W	0xF	PC4_SELECT PC4 Select. 0000: Input 0001: Output 0010: Reserved 0011: SDC2_D0 0100: SPI0_WP 0101: PWM4 0110: TWI1_SCK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC_EINT4 1111: IO Disable

Offset: 0x0060			Register Name: PC_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
15:12	R/W	0xF	PC3_SELECT	
			PC3 Select.	
			0000: Input	0001: Output
			0010: Reserved	0011: SDC2_D1
			0100: SPI0_MISO	0101: BOOT_SEL1
			0110: Reserved	0111: Reserved
			1000: Reserved	1001: Reserved
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PC_EINT3	1111: IO Disable
11:8	R/W	0xF	PC2_SELECT	
			PC2 Select.	
			0000: Input	0001: Output
			0010: Reserved	0011: SDC2_D2
			0100: SPI0_MOSI	0101: BOOT_SEL0
			0110: Reserved	0111: Reserved
			1000: Reserved	1001: Reserved
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PC_EINT2	1111: IO Disable
7:4	R/W	0xF	PC1_SELECT	
			PC1 Select.	
			0000: Input	0001: Output
			0010: Reserved	0011: SDC2_CMD
			0100: SPI0_CS0	0101: Reserved
			0110: Reserved	0111: Reserved
			1000: Reserved	1001: Reserved
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PC_EINT1	1111: IO Disable
3:0	R/W	0xF	PC0_SELECT	
			PC0 Select.	
			0000: Input	0001: Output
			0010: Reserved	0011: SDC2_CLK
			0100: SPI0_CLK	0101: Reserved
			0110: Reserved	0111: Reserved
			1000: Reserved	1001: Reserved
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PC_EINT0	1111: IO Disable

10.6.5.8 0x0070 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0	PC_DAT PC Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.9 0x0074 PC Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0074			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x1	PC5_DRV PC5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC4_DRV PC4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC3_DRV PC3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC2_DRV PC2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC1_DRV PC1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/

Offset: 0x0074			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x1	PC0_DRV PC0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.10 0x0084 PC Pull Register (Default Value: 0x0000_0050)

Offset: 0x0084			Register Name: PC_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PC5_PULL PC5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PC4_PULL PC4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x1	PC2_PULL PC2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.5.11 0x0090 PD Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0090			Register Name: PD_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	PD7_SELECT PD7 Select. 0000: Input 0001: Output 0010: LCD_D11 0011: PWM6 0100: RMII_TXCK 0101: Reserved 0110: SPI1_CS1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT7 1111: IO Disable
27:24	R/W	0xF	PD6_SELECT PD6 Select. 0000: Input 0001: Output 0010: LCD_D10 0011: PWM5 0100: Reserved 0101: DSI_CKP 0110: SPI1_WP/DBI_TE 0111: RMII_RXD0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT6 1111: IO Disable
23:20	R/W	0xF	PD5_SELECT PD5 Select. 0000: Input 0001: Output 0010: LCD_D7 0011: PWM4 0100: Reserved 0101: DSI_CKN 0110: SPI1_HOLD/DBI_DCX/DBI_WRX 0111: RMII_RXD1 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT5 1111: IO Disable

Offset: 0x0090			Register Name: PD_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0xF	PD4_SELECT PD4 Select. 0000: Input 0001: Output 0010: LCD_D6 0011: PWM3 0100: Reserved 0101: DSI_D1P 0110: SPI1_MISO/DBI_SDI/DBI_TE/DBI_DCX0111: RMII_CRS_DV 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT4 1111: IO Disable
15:12	R/W	0xF	PD3_SELECT PD3 Select. 0000: Input 0001: Output 0010: LCD_D5 0011: PWM2 0100: Reserved 0101: DSI_D1N 0110: SPI1_MOSI/DBI_SDO 0111: RMII_RXER 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT3 1111: IO Disable
11:8	R/W	0xF	PD2_SELECT PD2 Select. 0000: Input 0001: Output 0010: LCD_D4 0011: PWM1 0100: Reserved 0101: DSI_D0P 0110: SPI1_CLK/DBI_SCLK 0111: RMII_TXD1 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT2 1111: IO Disable
7:4	R/W	0xF	PD1_SELECT PD1 Select. 0000: Input 0001: Output 0010: LCD_D3 0011: PWM0 0100: Reserved 0101: DSI_D0N 0110: SPI1_CS0/DBI_CSX 0111: RMII_TXD0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT1 1111: IO Disable
3:0	/	/	/

10.6.5.12 0x0094 PD Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0094			Register Name: PD_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xF	PD8_SELECT PD8 Select. 0000: Input 0001: Output 0010: LCD_D12 0011: PWM7 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT8 1111: IO Disable

10.6.5.13 0x0098 PD Configure Register 2 (Default Value: 0x0FFF_FFFF)

Offset: 0x0098			Register Name: PD_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0xF	PD21_SELECT PD21 Select. 0000: Input 0001: Output 0010: LCD_VSYNC 0011: Reserved 0100: MDIO 0101: SPI2_CS0 0110: TWI2_SDA 0111: UART2_CTS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT21 1111: IO Disable
19:16	R/W	0xF	PD20_SELECT PD20 Select. 0000: Input 0001: Output 0010: LCD_HSYNC 0011: PWM10 0100: MDC 0101: SPI2_MISO 0110: TWI2_SCK 0111: UART2_RTS 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT20 1111: IO Disable

Offset: 0x0098			Register Name: PD_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0xF	PD19_SELECT PD19 Select. 0000: Input 0001: Output 0010: LCD_DE 0011: PWM9 0100: TCON_TRIG 0101: SPI2_MOSI 0110: TWI3_SDA 0111: UART2_RX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT19 1111: IO Disable
11:8	R/W	0xF	PD18_SELECT PD18 Select. 0000: Input 0001: Output 0010: LCD_CLK 0011: Reserved 0100: EPHY_25M 0101: SPI2_CLK 0110: TWI3_SCK 0111: UART2_TX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD_EINT18 1111: IO Disable
7:0	/	/	/

10.6.5.14 0x00A0 PD Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PD_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:0	R/W	0	PD_DAT PD Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.15 0x00A4 PD Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00A4			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

Offset: 0x00A4			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
29:28	R/W	0x1	PD7_DRV PD7 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD6_DRV PD6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD5_DRV PD5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD4_DRV PD4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD3_DRV PD3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD2_DRV PD2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD1_DRV PD1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:0	/	/	/

10.6.5.16 0x00A8 PD Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00A8			Register Name: PD_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

Offset: 0x00A8			Register Name: PD_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x1	PD8_DRV PD8 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.17 0x00AC PD Multi_Driving Register 2 (Default Value: 0x0111_1111)

Offset: 0x00AC			Register Name: PD_DRV2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x1	PD21_DRV PD21 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD20_DRV PD20 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD19_DRV PD19 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD18_DRV PD18 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:0	/	/	/

10.6.5.18 0x00B4 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: PD_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	PD8_PULL PD8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x00B4			Register Name: PD_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	R/W	0x0	PD7_PULL PD7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	/	/	/

10.6.5.19 0x00B8 PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PD_PUL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PD21_PULL PD21 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x00B8			Register Name: PD_PUL1
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	PD20_PULL PD20 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:0	/	/	/

10.6.5.20 0x00C0 PE Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C0			Register Name: PE_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	PE7_SELECT PE7 Select. 0000: Input 0001: Output 0010: NCSI_D3 0011: RMII_RXER 0100: Reserved 0101: PWM7 0110: UART1_RX 0111: I2S1_DOUT0 1000: TWI4_SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT7 1111: IO Disable
27:24	R/W	0xF	PE6_SELECT PE6 Select. 0000: Input 0001: Output 0010: NCSI_D2 0011: RMII_TXEN 0100: Reserved 0101: PWM6 0110: UART1_TX 0111: Reserved 1000: TWI4_SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT6 1111: IO Disable

Offset: 0x00C0			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
23:20	R/W	0xF	PE5_SELECT PE5 Select. 0000: Input 0010: NCSI_D1 0011: RMII_TXD1 0100: Reserved 0110: SDC1_D3 1000: TWI0_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT5	0001: Output 0101: PWM5 0111: TWI3_SDA 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PE4_SELECT PE4 Select. 0000: Input 0010: NCSI_D0 0011: RMII_TXD0 0100: I2S1_DOUT0 0110: SDC1_D2 1000: TWI0_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT4	 0001: Output 0101: PWM4 0111: TWI3_SCK 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PE3_SELECT PE3 Select. 0000: Input 0010: NCSI_VSYNC 0011: RMII_RXD0 0100: I2S1_DIN0 0110: SDC1_D1 1000: TWI1_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT3	 0001: Output 0101: PWM3 0111: UART3_RTS 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00C0			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
11:8	R/W	0xF	PE2_SELECT PE2 Select. 0000: Input 0010: NCSI_HSYNC 0100: I2S1_LRCK 0110: SDC1_D0 1000: TWI1_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT2	 0001: Output 0011: RMII_CRS_DV 0101: PWM2 0111: UART3_CTS 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PE1_SELECT PE1 Select. 0000: Input 0010: NCSI_MCLK 0011: RMII_TXCK 0100: I2S1_BCLK 0110: SDC1_CMD 1000: TWI3_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT1	 0001: Output 0101: PWM1 0111: UART3_RX 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PE0_SELECT PE0 Select. 0000: Input 0010: NCSI_PCLK 0011: RMII_RXD1 0100: I2S1_MCLK 0110: SDC1_CLK 1000: TWI3_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT0	 0001: Output 0101: PWM0 0111: UART3_TX 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

10.6.5.21 0x00C4 PE Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C4			Register Name: PE_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x00C4			Register Name: PE_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0xF	PE13_SELECT PE13 Select. 0000: Input 0001: Output 0010: NCSI_D9 0011: Reserved 0100: Reserved 0101: MIPI_CSI_MCLK1 0110: UART2_RX 0111: UART3_RX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT13 1111: IO Disable
19:16	R/W	0xF	PE12_SELECT PE12 Select. 0000: Input 0001: Output 0010: NCSI_D8 0011: Reserved 0100: Reserved 0101: MIPI_CSI_MCLK0 0110: UART2_TX 0111: UART3_TX 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT12 1111: IO Disable
15:12	R/W	0xF	PE11_SELECT PE11 Select. 0000: Input 0001: Output 0010: NCSI_D7 0011: Reserved 0100: Reserved 0101: CSI_SM_VS 0110: UART2_CTS 0111: I2S1_MCLK 1000: WIEGAND_D1 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT11 1111: IO Disable
11:8	R/W	0xF	PE10_SELECT PE10 Select. 0000: Input 0001: Output 0010: NCSI_D6 0011: EPHY_25M 0100: Reserved 0101: PWM10 0110: UART2_RTS 0111: I2S1_BCLK 1000: WIEGAND_D0 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT10 1111: IO Disable

Offset: 0x00C4			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PE9_SELECT PE9 Select. 0000: Input 0001: Output 0010: NCSI_D5 0011: MDIO 0100: Reserved 0101: PWM9 0110: WIEGAND_D1 0111: I2S1_LRCK 1000: TWI1_SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT9 1111: IO Disable
3:0	R/W	0xF	PE8_SELECT PE8 Select. 0000: Input 0001: Output 0010: NCSI_D4 0011: MDC 0100: Reserved 0101: PWM8 0110: WIEGAND_D0 0111: I2S1_DIN0 1000: TWI1_SCK 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT8 1111: IO Disable

10.6.5.22 0x00D0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0	PE_DAT PE Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.23 0x00D4 PE Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00D4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/

Offset: 0x00D4			Register Name: PE_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
29:28	R/W	0x1	PE7_DRV PE7 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE6_DRV PE6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE5_DRV PE5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE4_DRV PE4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE3_DRV PE3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE2_DRV PE2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE1_DRV PE1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE0_DRV PE0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.24 0x00D8 PE Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00D8			Register Name: PE_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x1	PE13_DRV PE13 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE12_DRV PE12 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE11_DRV PE11 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE10_DRV PE10 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE9_DRV PE9 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE8_DRV PE8 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.25 0x00E4 PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PE_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

Offset: 0x00E4			Register Name: PE_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
27:26	R/W	0x0	PE13_PULL PE13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x00E4			Register Name: PE_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x0	PE3_PULL PE3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.5.26 0x00F0 PF Configure Register (Default Value: 0x0FFF_FFFF)

Offset: 0x00F0			Register Name: PF_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0xF	PF6_SELECT PF6 Select. 0000: Input 0001: Output 0010: DBG_CLK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT6 1111: IO Disable
23:20	R/W	0xF	PF5_SELECT PF5 Select. 0000: Input 0001: Output 0010: SDC0_D2 0011: JTAG_CK 0100: Reserved 0101: Reserved 0110: R_JTAG_CK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT5 1111: IO Disable

Offset: 0x00F0			Register Name: PF_CFG	
Bit	**Read/Write**	**Default/Hex**	**Description**	
19:16	R/W	0xF	PF4_SELECT PF4 Select. 0000: Input 0010: SDC0_D3 0100: SPI0_CS1 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT4	 0001: Output 0011: UART0_RX 0101: SPI2_CS1 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PF3_SELECT PF3 Select. 0000: Input 0010: SDC0_CMD 0100: SPI0_CS0 0110: R_JTAG_DO 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT3	 0001: Output 0011: JTAG_DO 0101: SPI2_CS0 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PF2_SELECT PF2 Select. 0000: Input 0010: SDC0_CLK 0100: SPI0_MISO 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT2	 0001: Output 0011: UART0_TX 0101: SPI2_MISO 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PF1_SELECT PF1 Select. 0000: Input 0010: SDC0_D0 0100: SPI0_MOSI 0110: R_JTAG_DI 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT1	 0001: Output 0011: JTAG_DI 0101: SPI2_MOSI 0111: CPU_BIST1 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00F0			Register Name: PF_CFG
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PF0_SELECT PF0 Select. 0000: Input 0001: Output 0010: SDC0_D1 0011: JTAG_MS 0100: SPI0_CLK 0101: SPI2_CLK 0110: R_JTAG_MS 0111: CPU_BIST0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT0 1111: IO Disable

10.6.5.27 0x0100 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R/W	0	PF_DAT PF Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.28 0x0104 PF Multi_Driving Register (Default Value: 0x0111_1111)

Offset: 0x0104			Register Name: PF_DRV
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PF6_DRV PF6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PF5_DRV PF5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/

Offset: 0x0104			Register Name: PF_DRV
Bit	**Read/Write**	**Default/Hex**	**Description**
17:16	R/W	0x1	PF4_DRV PF4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PF3_DRV PF3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PF2_DRV PF2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PF1_DRV PF1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PF0_DRV PF0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.29 0x0114 PF Pull Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PF_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0114			Register Name: PF_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x0	PF3_PULL PF3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.5.30 0x0150 PH Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0150			Register Name: PH_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xF	PH0_SELECT PH0 Select. 0000: Input 0001: Output 0010: PWM0 0011: Reserved 0100: SPI1_CLK 0101: UART3_TX 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT0 1111: IO Disable

10.6.5.31 0x0154 PH Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0154			Register Name: PH_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

Offset: 0x0154			Register Name: PH_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
27:24	R/W	0xF	PH14_SELECT PH14 Select. 0000: Input 0010: JTAG_DI 0100: R_JTAG_DI 0110: SPI3_CS0 1000: PWM7 1010: Reserved 1100: Reserved 1110: PH_EINT14	 0001: Output 0011: MDIO 0101: TWI3_SDA 0111: WIEGAND_D1 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
23:20	R/W	0xF	PH13_SELECT PH13 Select. 0000: Input 0010: JTAG_DO 0100: R_JTAG_DO 0110: SPI3_MISO 1000: PWM6 1010: Reserved 1100: Reserved 1110: PH_EINT13	 0001: Output 0011: MDC 0101: TWI3_SCK 0111: WIEGAND_D0 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PH12_SELECT PH12 Select. 0000: Input 0010: JTAG_CK 0100: R_JTAG_CK 0110: SPI3_MOSI 1000: PWM5 1010: Reserved 1100: Reserved 1110: PH_EINT12	 0001: Output 0011: Reserved 0101: TWI2_SDA 0111: CLK_FANOUT1 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PH11_SELECT PH11 Select. 0000: Input 0010: JTAG_MS 0100: R_JTAG_MS 0110: SPI3_CLK 1000: PWM4 1010: Reserved 1100: Reserved 1110: PH_EINT11	 0001: Output 0011: Reserved 0101: TWI2_SCK 0111: CLK_FANOUT0 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x0154			Register Name: PH_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0xF	PH10_SELECT PH10 Select. 0000: Input 0001: Output 0010: PWM10 0011: Reserved 0100: TWI3_SDA 0101: UART0_RX 0110: Reserved 0111: DMIC_CLK 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT10 1111: IO Disable
7:4	R/W	0xF	PH9_SELECT PH9 Select. 0000: Input 0001: Output 0010: PWM9 0011: Reserved 0100: TWI3_SCK 0101: UART0_TX 0110: Reserved 0111: DMIC_DATA0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT9 1111: IO Disable
3:0	/	/	/

10.6.5.32 0x0160 PH Data Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0	PH_DAT PH Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.5.33 0x0164 PH Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0164			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

Offset: 0x0164			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x1	PH0_DRV PH0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.5.34 0x0168 PH Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0168			Register Name: PH_DRV1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PH14_DRV PH14 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH13_DRV PH13 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH12_DRV PH12 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH11_DRV PH11 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH10_DRV PH10 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH9_DRV PH9 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:0	/	/	/

10.6.5.35 0x0174 PH Pull Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PH_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	PH14_PULL PH14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:2	/	/	/
1:0	R/W	0x0	PH0_PULL PH0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.5.36 0x0200 PA External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PA_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0200			Register Name: PA_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.37 0x0204 PA External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PA_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
/	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0204			Register Name: PA_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0204			Register Name: PA_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.38 0x0210 PA External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PA_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable

Offset: 0x0210			Register Name: PA_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.5.39 0x0214 PA External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PA_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0214			Register Name: PA_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0214			Register Name: PA_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.40 0x0218 PA External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PA_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK32KHz 1: HOSC 24MHz

10.6.5.41 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.42 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.5.43 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0254			Register Name: PC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.44 0x0258 PC External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.5.45 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: PD_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0260			Register Name: PD_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	/	/	/

10.6.5.46 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: PD_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0264			Register Name: PD_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0264			Register Name: PD_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.47 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT22_CFG External INT22 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	EINT19_CFG External INT19 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.48 0x0270 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	EINT21_CTL External INT21 Enable. 0: Disable 1: Enable

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
20	R/W	0x0	EINT20_CTL External INT20 Enable. 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable. 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable. 0: Disable 1: Enable
17:9	/	/	/
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	/	/	/

10.6.5.49 0x0274 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
17:9	/	/	/
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	/	/	/

10.6.5.50 0x0278 PD External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: PD_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/

Offset: 0x0278			Register Name: PD_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.5.51 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.52 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.53 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.5.54 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0294			Register Name: PE_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0294			Register Name: PE_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.55 0x0298 PE External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.5.56 0x02A0 PF External Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_INT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x02A0			Register Name: PF_INT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.57 0x02B0 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable

Offset: 0x02B0			Register Name: PF_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.5.58 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x02B4			Register Name: PF_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.59 0x02B8 PF External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.5.60 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.5.61 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	/	/	/

10.6.5.62 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8:1	/	/	/
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.5.63 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8:1	/	/	/
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.5.64 0x02F8 PH External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.5.65 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	VCCIO_PWR_MOD_SEL. VCC_IO POWER MODE Select. 0: 3.3V 1: 1.8V
11:6	/	/	/
5	R/W	0x0	PF_PWR_MOD_SEL PF_POWER MODE Select. 0: 3.3V 1: 1.8V If PF Port Power Source select VCC_IO, this bit is invalid
4	R/W	0x0	PE_PWR_MOD_SEL PE_POWER MODE Select. 0: 3.3V 1: 1.8V If PE Port Power Source select VCC_IO, this bit is invalid
3	R/W	0x0	PD_PWR_MOD_SEL PD_POWER MODE Select. 0: 3.3V 1: 1.8V If PD Port Power Source select VCC_IO, this bit is invalid
2	R/W	0x0	PC_PWR_MOD_SEL PC_POWER MODE Select. 0: 3.3V 1: 1.8V If PC Port Power Source select VCC_IO, this bit is invalid
1	/	/	/
0	R/W	0x0	PA_PWR_MOD_SEL PA_POWER MODE Select. 0: 3.3V 1: 1.8V If PA Port Power Source select VCC_IO, this bit is invalid

10.6.5.66 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL VCC_IO Withstand Voltage Mode Select Control. 0: Enable 1: Disable
11:6	/	/	/
5	R/W	0x0	VCC_PF_WS_VOL_MOD_SEL VCC_PF Withstand Voltage Mode Select Control. 0: Enable 1: Disable
4	R/W	0x0	VCC_PE_WS_VOL_MOD_SEL VCC_PE Withstand Voltage Mode Select Control. 0: Enable 1: Disable
3	R/W	0x0	VCC_PD_WS_VOL_MOD_SEL VCC_PD Withstand Voltage Mode Select Control. 0: Enable 1: Disable
2	R/W	0x0	VCC_PC_WS_VOL_MOD_SEL VCC_PC Withstand Voltage Mode Select Control. 0: Enable 1: Disable
1	/	/	/
0	R/W	0x0	VCC_PA_WS_VOL_MOD_SEL VCC_PA Withstand Voltage Mode Select Control. 0: Enable 1: Disable

10.6.5.67 0x0348 PIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	VCCIO_PWR_VAL VCC_IO Power Value.
15:6	/	/	/
5	R	0x0	PF_PWR_VAL PF_Port Power Value. If PF_Port Power Source select VCC_IO, this bit is invalid

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R	0x0	PE_PWR_VAL PE_Port Power Value. If PE_Port Power Source select VCC_IO, this bit is invalid
3	R	0x0	PD_PWR_VAL PD_Port Power Value. If PD_Port Power Source select VCC_IO, this bit is invalid
2	R	0x0	PC_PWR_VAL PC_Port Power Value. If PC_Port Power Source select VCC_IO, this bit is invalid
1	/	/	/
0	R	0x0	PA_PWR_VAL PA_Port Power Value. If PA_Port Power Source select VCC_IO, this bit is invalid

10.6.5.68 0x0350 PIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: PIO_POW_VAL_SET_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control. 0: 1.8V 1: 3.3V When configuring this register to switch PF port power, you need to configure bit [5] of PIO_POW_MOD_SEL (Offset: 0x0340) to '1', configure bit [5] of PIO_POW_MS_CTL (Offset: 0x0344) to '0' and set the voltage mode of GPIO group to compatible mode.

10.6.6 V851SE GPIO Register Description

10.6.6.1 0x0000 PA Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	PA7_SELECT PA7 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D0P/MIPIA-CSI-D2P 0011: Reserved 0100: TWI1_SDA 0101: PWM1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT7 1111: IO Disable
27:24	R/W	0xF	PA6_SELECT PA6 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D0N/MIPIA-CSI-D2N 0011: Reserved 0100: TWI1_SCK 0101: PWM0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT6 1111: IO Disable
23:20	R/W	0xF	PA5_SELECT PA5 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT5 1111: IO Disable

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0xF	PA4_SELECT PA4 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D0P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT4 1111: IO Disable
15:12	R/W	0xF	PA3_SELECT PA3 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D1P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT3 1111: IO Disable
11:8	R/W	0xF	PA2_SELECT PA2 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_D1N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT2 1111: IO Disable
7:4	R/W	0xF	PA1_SELECT PA1 Select. 0000: Input 0001: Output 0010: MIPIA_CSI_CK0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT1 1111: IO Disable

Offset: 0x0000			Register Name: PA_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
3:0	R/W	0xF	PA0_SELECT PA0 Select. 0000: Input 0010: MIPIA_CSI_CK0P 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PA_EINT0	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

10.6.6.2 0x0004 PA Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0004			Register Name: PA_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:16	/	/	/	
15:12	R/W	0xF	PA11_SELECT PA11 Select. 0000: Input 0010: MIPIB_CSI_CK0P 0100: MIPI_CSI_MCLK1 0110: CLK_FANOUT1 1000: Reserved 1010: Reserved 1100: Reserved 1110: PA_EINT11	 0001: Output 0011: Reserved 0101: TWI0_SDA 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PA10_SELECT PA10 Select. 0000: Input 0010: MIPIB_CSI_CK0N 0100: MIPI_CSI_MCLK0 0110: CLK_FANOUT0 1000: Reserved 1010: Reserved 1100: Reserved 1110: PA_EINT10	 0001: Output 0011: Reserved 0101: TWI0_SCK 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x0004			Register Name: PA_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
7:4	R/W	0xF	PA9_SELECT PA9 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D1P/MIPIA-CSI-D3P 0011: TWI4_SDA 0100: TWI3_SDA 0101: PWM3 0110: UART2_RX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT9 1111: IO Disable
3:0	R/W	0xF	PA8_SELECT PA8 Select. 0000: Input 0001: Output 0010: MIPIB_CSI_D1N/MIPIA-CSI-D3N 0011: TWI4_SCK 0100: TWI3_SCK 0101: PWM2 0110: UART2_TX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PA_EINT8 1111: IO Disable

10.6.6.3 0x0010 PA Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PA_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	0	PA_DAT PA Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.6.4 0x0014 PA Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0014			Register Name: PA_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	PA7_DRV PA7 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PA6_DRV PA6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PA5_DRV PA5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PA4_DRV PA4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PA3_DRV PA3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PA2_DRV PA2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PA1_DRV PA1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PA0_DRV PA0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.5 0x0018 PA Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0018			Register Name: PA_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PA11_DRV PA11 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PA10_DRV PA10 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PA9_DRV PA9 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PA8_DRV PA8 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.6 0x0024 PA Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PA_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x0	PA11_PULL PA11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PA10_PULL PA10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PA9_PULL PA9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0024			Register Name: PA_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
17:16	R/W	0x0	PA8_PULL PA8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PA7_PULL PA7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PA6_PULL PA6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PA5_PULL PA5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PA4_PULL PA4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PA3_PULL PA3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PA2_PULL PA2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PA1_PULL PA1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PA0_PULL PA0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.6.7 0x0060 PC Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0060			Register Name: PC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x0060			Register Name: PC_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
23:20	R/W	0xF	PC5_SELECT PC5 Select. 0000: Input 0010: Reserved 0100: SPI0_HOLD 0110: TWI1_SDA 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC_EINT5	 0001: Output 0011: SDC2_D3 0101: PWM5 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PC4_SELECT PC4 Select. 0000: Input 0010: Reserved 0100: SPI0_WP 0110: TWI1_SCK 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC_EINT4	 0001: Output 0011: SDC2_D0 0101: PWM4 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PC3_SELECT PC3 Select. 0000: Input 0010: Reserved 0100: SPI0_MISO 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC_EINT3	 0001: Output 0011: SDC2_D1 0101: BOOT_SEL1 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PC2_SELECT PC2 Select. 0000: Input 0010: Reserved 0100: SPI0_MOSI 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC_EINT2	 0001: Output 0011: SDC2_D2 0101: BOOT_SEL0 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x0060			Register Name: PC_CFG0	
Bit	Read/Write	Default/Hex	Description	
7:4	R/W	0xF	PC1_SELECT PC1 Select. 0000: Input 0010: Reserved 0100: SPI0_CS0 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC_EINT1	 0001: Output 0011: SDC2_CMD 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PC0_SELECT PC0 Select. 0000: Input 0010: Reserved 0100: SPI0_CLK 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC_EINT0	 0001: Output 0011: SDC2_CLK 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

10.6.6.8 0x0070 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PC_DAT
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0	PC_DAT PC Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.6.9 0x0074 PC Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0074			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/

Offset: 0x0074			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
21:20	R/W	0x1	PC5_DRV PC5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC4_DRV PC4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC3_DRV PC3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC2_DRV PC2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC1_DRV PC1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PC0_DRV PC0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.10 0x0084 PC Pull Register (Default Value: 0x0000_0050)

Offset: 0x0084			Register Name: PC_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PC5_PULL PC5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0084			Register Name: PC_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x0	PC4_PULL PC4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x1	PC2_PULL PC2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.6.11 0x00C0 PE Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C0			Register Name: PE_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	PE7_SELECT PE7 Select. 0000: Input 0001: Output 0010: NCSI_D3 0011: Reserved 0100: Reserved 0101: PWM7 0110: UART1_RX 0111: I2S1_DOUT0 1000: TWI4_SDA 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE_EINT7 1111: IO Disable

Offset: 0x00C0			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
27:24	R/W	0xF	PE6_SELECT PE6 Select. 0000: Input 0010: NCSI_D2 0011: Reserved 0100: Reserved 0110: UART1_TX 1000: TWI4_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT6	0001: Output 0101: PWM6 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
23:20	R/W	0xF	PE5_SELECT PE5 Select. 0000: Input 0010: NCSI_D1 0011: Reserved 0100: Reserved 0110: SDC1_D3 1000: TWI0_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT5	 0001: Output 0101: PWM5 0111: TWI3_SDA 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PE4_SELECT PE4 Select. 0000: Input 0010: NCSI_D0 0011: Reserved 0100: I2S1_DOUT0 0110: SDC1_D2 1000: TWI0_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT4	 0001: Output 0101: PWM4 0111: TWI3_SCK 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00C0			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
15:12	R/W	0xF	PE3_SELECT PE3 Select. 0000: Input 0010: NCSI_VSYNC 0011: Reserved 0100: I2S1_DIN0 0110: SDC1_D1 1000: TWI1_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT3	0001: Output 0101: PWM3 0111: UART3_RTS 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PE2_SELECT PE2 Select. 0000: Input 0010: NCSI_HSYNC 0100: I2S1_LRCK 0110: SDC1_D0 1000: TWI1_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT2	 0001: Output 0011: Reserved 0101: PWM2 0111: UART3_CTS 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PE1_SELECT PE1 Select. 0000: Input 0010: NCSI_MCLK 0011: Reserved 0100: I2S1_BCLK 0110: SDC1_CMD 1000: TWI3_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT1	 0001: Output 0101: PWM1 0111: UART3_RX 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00C0			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
3:0	R/W	0xF	PE0_SELECT PE0 Select. 0000: Input 0010: NCSI_PCLK 0011: Reserved 0100: I2S1_MCLK 0110: SDC1_CLK 1000: TWI3_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT0	 0001: Output 0101: PWM0 0111: UART3_TX 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

10.6.6.12 0x00C4 PE Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C4			Register Name: PE_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:24	/	/	/	
23:20	R/W	0xF	PE13_SELECT PE13 Select. 0000: Input 0010: NCSI_D9 0100: Reserved 0110: UART2_RX 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE_EINT13	 0001: Output 0011: Reserved 0101: MIPI_CSI_MCLK1 0111: UART3_RX 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PE12_SELECT PE12 Select. 0000: Input 0010: NCSI_D8 0100: Reserved 0110: UART2_TX 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE_EINT12	 0001: Output 0011: Reserved 0101: MIPI_CSI_MCLK0 0111: UART3_TX 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00C4			Register Name: PE_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
15:12	R/W	0xF	PE11_SELECT PE11 Select. 0000: Input 0010: NCSI_D7 0100: Reserved 0110: UART2_CTS 1000: WIEGAND_D1 1010: Reserved 1100: Reserved 1110: PE_EINT11	 0001: Output 0011: Reserved 0101: CSI_SM_VS 0111: I2S1_MCLK 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PE10_SELECT PE10 Select. 0000: Input 0010: NCSI_D6 0100: Reserved 0110: UART2_RTS 1000: WIEGAND_D0 1010: Reserved 1100: Reserved 1110: PE_EINT10	 0001: Output 0011: EPHY_25M 0101: PWM10 0111: I2S1_BCLK 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PE9_SELECT PE9 Select. 0000: Input 0010: NCSI_D5 0100: Reserved 0110: WIEGAND_D1 1000: TWI1_SDA 1010: Reserved 1100: Reserved 1110: PE_EINT9	 0001: Output 0011: MDIO 0101: PWM9 0111: I2S1_LRCK 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PE8_SELECT PE8 Select. 0000: Input 0010: NCSI_D4 0100: Reserved 0110: WIEGAND_D0 1000: TWI1_SCK 1010: Reserved 1100: Reserved 1110: PE_EINT8	 0001: Output 0011: MDC 0101: PWM8 0111: I2S1_DIN0 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

10.6.6.13 0x00D0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PE_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R/W	0	PE_DAT PE Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.6.14 0x00D4 PE Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00D4			Register Name: PE_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	PE7_DRV PE7 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE6_DRV PE6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE5_DRV PE5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE4_DRV PE4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE3_DRV PE3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/

Offset: 0x00D4			Register Name: PE_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
9:8	R/W	0x1	PE2_DRV PE2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE1_DRV PE1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE0_DRV PE0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.15 0x00D8 PE Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00D8			Register Name: PE_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x1	PE13_DRV PE13 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE12_DRV PE12 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE11_DRV PE11 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE10_DRV PE10 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/

Offset: 0x00D8			Register Name: PE_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
5:4	R/W	0x1	PE9_DRV PE9 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE8_DRV PE8 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.16 0x00E4 PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PE_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:26	R/W	0x0	PE13_PULL PE13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x00E4			Register Name: PE_PUL0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	R/W	0x0	PE7_PULL PE7 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.6.17 0x00F0 PF Configure Register (Default Value: 0x0FFF_FFFF)

Offset: 0x00F0			Register Name: PF_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

Offset: 0x00F0			Register Name: PF_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	0xF	PF6_SELECT PF6 Select. 0000: Input 0001: Output 0010: DBG_CLK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT6 1111: IO Disable
23:20	R/W	0xF	PF5_SELECT PF5 Select. 0000: Input 0001: Output 0010: SDC0_D2 0011: JTAG_CK 0100: Reserved 0101: Reserved 0110: R_JTAG_CK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT5 1111: IO Disable
19:16	R/W	0xF	PF4_SELECT PF4 Select. 0000: Input 0001: Output 0010: SDC0_D3 0011: UART0_RX 0100: SPI0_CS1 0101: SPI2_CS1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT4 1111: IO Disable
15:12	R/W	0xF	PF3_SELECT PF3 Select. 0000: Input 0001: Output 0010: SDC0_CMD 0011: JTAG_DO 0100: SPI0_CS0 0101: SPI2_CS0 0110: R_JTAG_DO 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF_EINT3 1111: IO Disable

Offset: 0x00F0			Register Name: PF_CFG	
Bit	Read/Write	Default/Hex	Description	
11:8	R/W	0xF	PF2_SELECT PF2 Select. 0000: Input 0010: SDC0_CLK 0100: SPI0_MISO 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT2	 0001: Output 0011: UART0_TX 0101: SPI2_MISO 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PF1_SELECT PF1 Select. 0000: Input 0010: SDC0_D0 0100: SPI0_MOSI 0110: R_JTAG_DI 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT1	 0001: Output 0011: JTAG_DI 0101: SPI2_MOSI 0111: CPU_BIST1 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PF0_SELECT PF0 Select. 0000: Input 0010: SDC0_D1 0100: SPI0_CLK 0110: R_JTAG_MS 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF_EINT0	 0001: Output 0011: JTAG_MS 0101: SPI2_CLK 0111: CPU_BIST0 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

10.6.6.18 0x0100 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Offset: 0x0100			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
6:0	R/W	0	PF_DAT PF Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.6.19 0x0104 PF Multi_Driving Register (Default Value: 0x0111_1111)

Offset: 0x0104			Register Name: PF_DRV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x1	PF6_DRV PF6 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PF5_DRV PF5 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PF4_DRV PF4 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PF3_DRV PF3 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PF2_DRV PF2 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/

Offset: 0x0104			Register Name: PF_DRV
Bit	**Read/Write**	**Default/Hex**	**Description**
5:4	R/W	0x1	PF1_DRV PF1 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PF0_DRV PF0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.20 0x0114 PF Pull Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PF_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0114			Register Name: PF_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x0	PF0_PULL PF0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.6.21 0x0150 PH Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0150			Register Name: PH_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xF	PH0_SELECT PH0 Select. 0000: Input 0001: Output 0010: PWM0 0011: Reserved 0100: SPI1_CLK 0101: UART3_TX 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT0 1111: IO Disable

10.6.6.22 0x0154 PH Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0154			Register Name: PH_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0xF	PH14_SELECT PH14 Select. 0000: Input 0001: Output 0010: JTAG_DI 0011: MDIO 0100: R_JTAG_DI 0101: TWI3_SDA 0110: SPI3_CS0 0111: WIEGAND_D1 1000: PWM7 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT14 1111: IO Disable

Offset: 0x0154			Register Name: PH_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
23:20	R/W	0xF	PH13_SELECT PH13 Select. 0000: Input 0010: JTAG_DO 0100: R_JTAG_DO 0110: SPI3_MISO 1000: PWM6 1010: Reserved 1100: Reserved 1110: PH_EINT13	 0001: Output 0011: MDC 0101: TWI3_SCK 0111: WIEGAND_D0 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PH12_SELECT PH12 Select. 0000: Input 0010: JTAG_CK 0100: R_JTAG_CK 0110: SPI3_MOSI 1000: PWM5 1010: Reserved 1100: Reserved 1110: PH_EINT12	 0001: Output 0011: Reserved 0101: TWI2_SDA 0111: CLK_FANOUT1 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PH11_SELECT PH11 Select. 0000: Input 0010: JTAG_MS 0100: R_JTAG_MS 0110: SPI3_CLK 1000: PWM4 1010: Reserved 1100: Reserved 1110: PH_EINT11	 0001: Output 0011: Reserved 0101: TWI2_SCK 0111: CLK_FANOUT0 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PH10_SELECT PH10 Select. 0000: Input 0010: PWM10 0100: TWI3_SDA 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PH_EINT10	 0001: Output 0011: Reserved 0101: UART0_RX 0111: DMIC_CLK 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x0154			Register Name: PH_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
7:4	R/W	0xF	PH9_SELECT PH9 Select. 0000: Input 0001: Output 0010: PWM9 0011: Reserved 0100: TWI3_SCK 0101: UART0_TX 0110: Reserved 0111: DMIC_DATA0 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT9 1111: IO Disable
3:0	/	/	/

10.6.6.23 0x0160 PH Data Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0	PH_DAT PH Data. If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.6.6.24 0x0164 PH Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0164			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	PH0_DRV PH0 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3

10.6.6.25 0x0168 PH Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0168			Register Name: PH_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/

Offset: 0x0168			Register Name: PH_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
25:24	R/W	0x1	PH14_DRV PH14 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH13_DRV PH13 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH12_DRV PH12 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH11_DRV PH11 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH10_DRV PH10 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH9_DRV PH9 Multi_Driving Select. 00: Level0 01: Level1 10: Level2 11: Level3
3:0	/	/	/

10.6.6.26 0x0174 PH Pull Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PH_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	PH14_PULL PH14 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0174			Register Name: PH_PUL
Bit	**Read/Write**	**Default/Hex**	**Description**
27:26	R/W	0x0	PH13_PULL PH13 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:2	/	/	/
1:0	R/W	0x0	PH0_PULL PH0 Pull_up or down Select. 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

10.6.6.27 0x0200 PA External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PA_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0200			Register Name: PA_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0200			Register Name: PA_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.28 0x0204 PA External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PA_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
/	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0204			Register Name: PA_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.29 0x0210 PA External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PA_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable

Offset: 0x0210			Register Name: PA_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.6.30 0x0214 PA External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PA_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0214			Register Name: PA_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.6.31 0x0218 PA External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PA_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK32KHz 1: HOSC 24MHz

10.6.6.32 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.33 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.6.34 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.6.35 0x0258 PC External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.6.36 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.37 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.38 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable. 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable. 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.6.39 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0294			Register Name: PE_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.6.40 0x0298 PE External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.6.41 0x02A0 PF External Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_INT_CFG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x02A0			Register Name: PF_INT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0x0	EINT5_CFG External INT5 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x02A0			Register Name: PF_INT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.42 0x02B0 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable. 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable. 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable. 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable. 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable. 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable. 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.6.43 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.6.44 0x02B8 PF External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.6.45 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	EINT0_CFG External INT0 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

10.6.6.46 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
23:20	R/W	0x0	EINT13_CFG External INT13 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode. 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	/	/	/

10.6.6.47 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable. 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable. 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable. 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable. 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable. 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable. 0: Disable 1: Enable
8:1	/	/	/
0	R/W	0x0	EINT0_CTL External INT0 Enable. 0: Disable 1: Enable

10.6.6.48 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
8:1	/	/	/
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.6.6.49 0x02F8 PH External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Offset: 0x02F8			Register Name: PH_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n. The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select. 0: CLK 32KHz 1: HOSC 24MHz

10.6.6.50 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCCIO_PWR_MOD_SEL. VCC_IO POWER MODE Select. 0: 3.3V 1: 1.8V
11:6	/	/	/
5	R/W	0x0	PF_PWR_MOD_SEL PF_POWER MODE Select. 0: 3.3V 1: 1.8V If PF Port Power Source select VCC_IO, this bit is invalid
4	R/W	0x0	PE_PWR_MOD_SEL PE_POWER MODE Select. 0: 3.3V 1: 1.8V If PE Port Power Source select VCC_IO, this bit is invalid
3	R/W	0x0	PD_PWR_MOD_SEL PD_POWER MODE Select. 0: 3.3V 1: 1.8V If PD Port Power Source select VCC_IO, this bit is invalid

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	PC_PWR_MOD_SEL PC_POWER MODE Select. 0: 3.3V 1: 1.8V If PC Port Power Source select VCC_IO, this bit is invalid
1	/	/	/
0	R/W	0x0	PA_PWR_MOD_SEL PA_POWER MODE Select. 0: 3.3V 1: 1.8V If PA Port Power Source select VCC_IO, this bit is invalid

10.6.6.51 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL VCC_IO Withstand Voltage Mode Select Control. 0: Enable 1: Disable
11:6	/	/	/
5	R/W	0x0	VCC_PF_WS_VOL_MOD_SEL VCC_PF Withstand Voltage Mode Select Control. 0: Enable 1: Disable
4	R/W	0x0	VCC_PE_WS_VOL_MOD_SEL VCC_PE Withstand Voltage Mode Select Control. 0: Enable 1: Disable
3	R/W	0x0	VCC_PD_WS_VOL_MOD_SEL VCC_PD Withstand Voltage Mode Select Control. 0: Enable 1: Disable
2	R/W	0x0	VCC_PC_WS_VOL_MOD_SEL VCC_PC Withstand Voltage Mode Select Control. 0: Enable 1: Disable
1	/	/	/

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	VCC_PA_WS_VOL_MOD_SEL VCC_PA Withstand Voltage Mode Select Control. 0: Enable 1: Disable

10.6.6.52 0x0348 PIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: PIO_POW_VAL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	VCCIO_PWR_VAL VCC_IO Power Value.
15:6	/	/	/
5	R	0x0	PF_PWR_VAL PF_Port Power Value. If PF_Port Power Source select VCC_IO, this bit is invalid
4	R	0x0	PE_PWR_VAL PE_Port Power Value. If PE_Port Power Source select VCC_IO, this bit is invalid
3	R	0x0	PD_PWR_VAL PD_Port Power Value. If PD_Port Power Source select VCC_IO, this bit is invalid
2	R	0x0	PC_PWR_VAL PC_Port Power Value. If PC_Port Power Source select VCC_IO, this bit is invalid
1	/	/	/
0	R	0x0	PA_PWR_VAL PA_Port Power Value. If PA_Port Power Source select VCC_IO, this bit is invalid

10.6.6.53 0x0350 PIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: PIO_POW_VAL_SET_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

Offset: 0x0350			Register Name: PIO_POW_VAL_SET_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control. 0: 1.8V 1: 3.3V When configuring this register to switch PF port power, you need to configure bit [5] of PIO_POW_MOD_SEL (Offset: 0x0340) to '1', configure bit [5] of PIO_POW_MS_CTL (Offset: 0x0344) to '0' and set the voltage mode of GPIO group to compatible mode.

10.7 GPADC

10.7.1 Overview

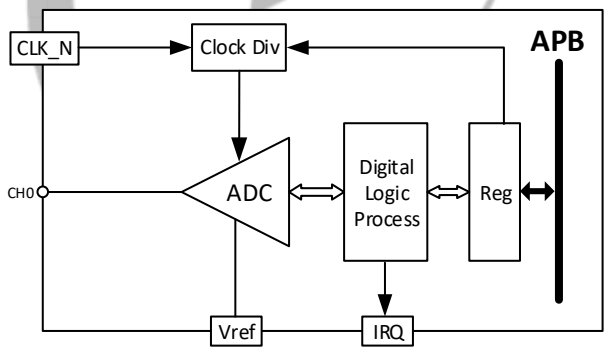
The General Purpose ADC (GPADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection. This ADC is a 1-channel successive approximation register (SAR) A/D converter.

- 12-bit resolution and 8-bit effective SAR type A/D converter
- 1-channel multiplexer
- 64 FIFO depth of data register
- Power Supply Voltage: 1.8 V, Analog Input Range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Supports data compare and interrupt
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

10.7.2 Block Diagram

The following figure shows a block diagram of the GPADC.

Figure 10-65 GPADC Block Diagram



10.7.3 Functional Descriptions

10.7.3.1 External Signals

The following table describes the external signals of GPADC.

Table 10-32GPADC External Signals

Signal	Description	Type
GPADC0	ADC Input Channel0	AI

10.7.3.2 Clock Sources

The following table describes the clock source for GPADC. Users can see section 3.4 Clock Controller Unit (CCU) for clock setting, configuration, and gating information.

Table 10-33 GPADC Clock Sources

Clock Sources	Description
OSC24M	24 MHz

10.7.3.3 GPADC Work Mode

- Single conversion mode

The GPADC completes one conversion in a specified channel, the converted data is updated at the data register of the corresponding channel.

- Continuous conversion mode

The GPADC has continuous conversion in a specified channel until the software stops, the converted data is updated at the data register of the corresponding channel.

- Burst conversion mode

The GPADC samples and converts in a specified channel, and sequentially stores the results in FIFO.

10.7.3.4 Clock and Timing Requirements

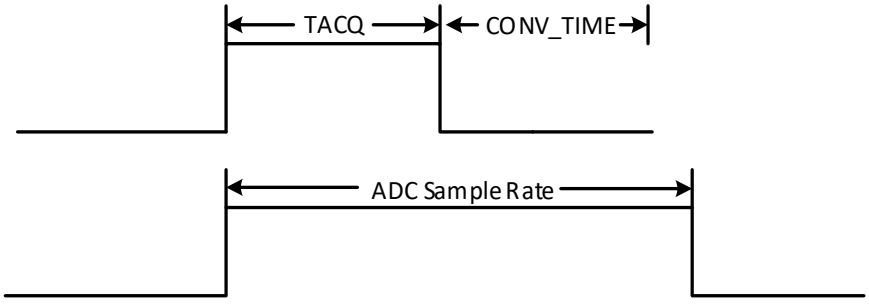
CLK_IN = 24 MHz.

CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us).

TACQ>10RC (R is output impedance of ADC sample circuit, C = 6.4 pF)

ADC Sample Frequency > TACQ+CONV_TIME.

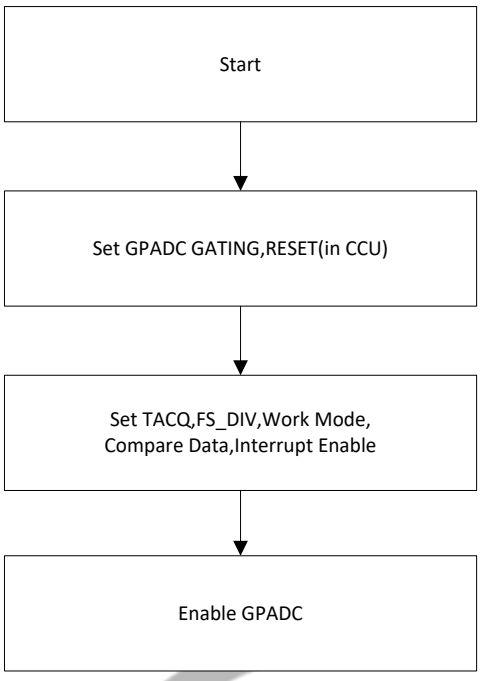
Figure 10-66 GPADC Clock and Timing Requirement



10.7.4 Programming Guidelines

The GPADC initial process is as follows.

Figure 10-67 GPADC Initial Process



Take channel 0 as an example:

Query Mode

1. Write 0x1 to the bit[16] of GPADC_BGR_REG (Offset: 0x09EC) to dessert reset.
2. Write 0x1 to the bit[0] of GPADC_BGR_REG (Offset: 0x09EC) to enable the GPADC clock.
3. Write 0x2F to the bit[15:0] of GP_SR_CON (Offset: 0x0000) to set the acquiring time of ADC.
4. Write 0x1DF to the bit[31:16] of GP_SR_CON (Offset: 0x0000) to set the ADC sample frequency divider.
5. Write 0x2 to the bit[19:18] of GP_CTRL (Offset: 0x0004) to set the continuous conversion mode.
6. Write 0x1 to the bit[0] of GP_CS_EN (Offset: 0x0008) to enable the analog input channel.
7. Write 0x1 to the bit[16] of GP_CTRL (Offset: 0x0004) to enable the ADC function.
8. Read the bit[0] of GP_DATA_INTS (Offset: 0x0038), if the bit is 1, then data conversion is complete.
9. Read the bit[11:0] of GP_CH0_DATA (Offset: 0x0080), and calculate voltage value based on GPADC formula.

Interrupt Mode

1. Write 0x1 to the bit[16] of GPADC_BGR_REG (Offset: 0x09EC) to dessert reset.
2. Write 0x1 to the bit[0] of GPADC_BGR_REG (Offset: 0x09EC) to enable the GPADC clock.
3. Write 0x2F to the bit[15:0] of GP_SR_CON (Offset: 0x0000) to set the acquiring time of ADC.

4. Write 0x1DF to the bit[31:16] of GP_SR_CON (Offset: 0x0000) to set the ADC sample frequency divider.
5. Write 0x2 to the bit[19:18] of GP_CTRL (Offset: 0x0004)to set the continuous conversion mode.
6. Write 0x1 to the bit[0] of GP_CS_EN (Offset: 0x0008) to enable the analog input channel.
7. Write 0x1 to the bit[0] of GP_DATA_INTC (Offset: 0x0028) to enable the GPADC data interrupt.
8. Set interrupt based on PLIC module.
9. Put interrupt handler address into interrupt vector table.
10. Write 0x1 to the bit16 of GP_CTRL (Offset: 0x0004) to enable the ADC function.
11. Read the bit[11:0] of GP_CH0_DATA (Offset: 0x0080) from the interrupt handler, calculate voltage value based on GPADC formula.

10.7.5 Register List

Module Name	Base Address
GPADC	0x02009000

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Config Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Config Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Config Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Config Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_OPA_EN	0x00F0	GPADC OPAMP Enable Register
GP_OPA_TUNE0	0x00F4	GPADC OPAMP Tune0 Register
IO_CON	0x0100	IO Configure Register
GP_GPIO_IO_CON	0x0110	GPADC GPADC IO Configure Register
GP_GPIO_DATA	0x0120	GPADC GPIO Data Register
GP_GPIO_IRQ_CON	0x0130	GPADC GPIO Interrupt Configure Register
GP_GPIO_IRQ_EN	0x0138	GPADC GPIO Interrupt Enable Register
GP_GPIO_IRQ	0x013C	GPADC GPIO Interrupt Select Register
GP_GPIO_PULL	0x0140	GPADC GPIO Pull Register

Register Name	Offset	Description
GP_GPIO_MDR	0x0150	GPADC GPIO Multi-driver Register

10.7.6 Register Description

10.7.6.1 0x0000 GPADC Sample Rate Config Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 16	R/W	0x1DF(50K)	FS_DIV. ADC Sample Frequency Divider CLK_IN/(n+1)
15:0	R/W	0x2F(2uS)	TACQ. ADC acquire time (n+1)/CLK_IN

10.7.6.2 0x0004 GPADC Control Register (Default Value: 0x0080_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/ W	0x0	ADC_FIRST_DLY. ADC First Convert Delay setting, ADC conversion of each channel is delayed by N samples
23	R/W	0x1	ADC_AUTOCALI_EN ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS.(Adjust the bandwidth of the ADC amplifier) ADC OP Bias
19:18	R/W	0x0	GPADC Work Mode 00: Single conversion mode 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN. ADC Calibration 1: start Calibration, it is clear to 0 after calibration
16	R/W	0x0	ADC_EN. (Before enabling this bity, configure the parameters such as ADC working mode and channels) ADC Function Enable 0: Disable 1: Enable **Note: when the single conversion mode is selected, this bit be automatically cleared to 0 after the conversion is finished.**

Offset: 0x0004			Register Name: GP_CTRL
Bit	Read/Write	Default/Hex	Description
15:0	/	/	/

10.7.6.3 0x0008 GPADC Compare and Select Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GP _CS_EN
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable 0: Disable 1: Enable
15:1	/	/	/
0	R/W	0x0	ADC_CH0_SELECT. Analog input channel 0 Select 0: Disable 1: Enable

10.7.6.4 0x000C GPADC FIFO Interrupt Control Register (Default Value: 0x0000_1F00)

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	FIFO_DATA_DRQ_EN. ADC FIFO Date DRQ Enable 0: Disable 1: Enable
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN. ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN. ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL. Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/WAC	0x0	FIFO_FLUSH. ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'
3:0	/	/	/

10.7.6.5 0x0010 GPADC FIFO Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING. ADC FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
16	R/W1C	0x0	FIFO_DATA_PENDING. ADC FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt
15:14	/	/	/
13:8	R	0x0	RXA_CNT. ADC FIFO available Sample Word Counter
7:0	/	/	/

10.7.6.6 0x0014 GPADC FIFO Data Register (Default Value: 0x0000_0xxx)

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	UDF	GP_FIFO_DATA GPADC Data in FIFO

10.7.6.7 0x0018 GPADC Calibration Data Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GP_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x000	GP_CDATA GPADC Calibration Data

10.7.6.8 0x0020 GPADC Low Interrupt Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CH0_LOW_IRQ_EN 0: Disable 1: Enable

10.7.6.9 0x0024 GPADC HIGH Interrupt Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CH0_HIG_IRQ_EN 0: Disable 1: Enable

10.7.6.10 0x0028 GPADC DATA Interrupt Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CH0_DATA_IRQ_EN 0: Disable 1: Enable

10.7.6.11 0x0030 GPADC Low Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	CH0_LOW_PENGDING 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

10.7.6.12 0x0034 GPADC High Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	CH0_HIG_PENGDING 0: NO Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

10.7.6.13 0x0038 GPADC Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	CH0_DATA_PENGDING 0: NO Pending IRQ 1: Channel 0 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

10.7.6.14 0x0040 GPADC CH0 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0040			Register Name: GP_CH0_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

10.7.6.15 0x0080 GPADC CH0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GP_CH0_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

10.7.6.16 0x00F0 GPADC OPAMP Enable Register Description (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: GP_OPA_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GP_CH0_OPA_SEL 0: ADC input bypass operation amplifier 1: ADC input from operation amplifier
15:1	/	/	/
0	R/W	0x0	GP_CH0_OPA_EN 0: Disable 1:enable operation amplifier for GPADC Channel 0

10.7.6.17 0x00F4 GPADC OPAMP Tune0 Register Description (Default Value 0x0000_8888)

Offset: 0x00F4			Register Name: GP_OPA_TUNE0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x8	GP_CH0_OPA_TUNE Indicates the magnification of operation amplifier for GPADC Channel 0 0: 1 times 1: 2 times …… 15: 16 times

10.7.6.18 0x0100 IO Configure Register Description (Default Value 0x0000_0000)

Offset: 0x0100			Register Name: IO_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CH0_IO_CON Channel 0 GPADC or GPIO IO Configure 0: Used IO as GPADC Pin 1: Used IO as GPIO Pin

10.7.6.19 0x0110 GPADC GPIO IO Configure Register Description (Default Value 0x0000_0000)

Offset: 0x0110			Register Name: GP_GPIO_IO_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

Offset: 0x0110			Register Name: GP_GPIO_IO_CON
Bit	Read/Write	Default/Hex	Description
1:0	R/W	0x0	CH0_GPIO_IO_CON Channel 0 GPIO IO Configure 00: Disable 01: Input 10: Output 11: Interrupt

10.7.6.20 0x0120 GPADC GPIO Data Register Description (Default Value 0x0000_0000)

Offset: 0x0120			Register Name: GP_GPIO_DATA
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CH0_GPIO_DATA Channel 0 GPIO DATA Show the value of input or output data

10.7.6.21 0x0130 GPADC GPIO Interrupt Configure0 Register Description (Default Value 0x0000_0000)

Offset: 0x0130			Register Name: GP_GPIO_IRQ_CON0
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/GPIO
3:0	R/W	0x0	CH0_GP_GPIO_IRQ_CON Channel 0 GPADC GPIO Interrupt Configure. 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.6.22 0x0138 GPADC GPIO Interrupt Enable Register Description (Default Value 0x0000_0000)

Offset: 0x0138			Register Name: GP_GPIO_IRQ_EN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CH0_GPIO_IRQ_EN Channel 0 GPIO Interrupt Enable 0: Disable 1: Enable

10.7.6.23 0x013C GPADC GPIO Interrupt Pending Register Description (Default Value 0x0000_0000)

Offset: 0x013C			Register Name: GP_GPIO_IRQ_PENDING
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	CH0_GPIO_IRQ_PENDING Channel 0 GPIO Interrupt Pending 0: NO interrupt pending 1: GPIO has at least one interrupt pending

10.7.6.24 0x0140 GPADC GPIO Pull Register Description (Default Value 0x0000_0000)

Offset: 0x0140			Register Name: GP_GPIO_PULL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CH0_GPIO_PULL Channel 0 GPIO Pull Register 00: Both pull up and pull down are disabled 01: Pull up enable 10: Pull down enable 00: Reserved

10.7.6.25 0x0150 GPADC GPIO Multi-drive Register Description (Default Value 0x0000_0000)

Offset: 0x0150			Register Name: GP_GPIO_MDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CH0_GPIO_SEL Channel 0 GPIO Selectors 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.8 PWM

10.8.1 Overview

The Pulse Width Modulation (PWM) module can output the configurable PWM waveforms and measure the external input waveforms.

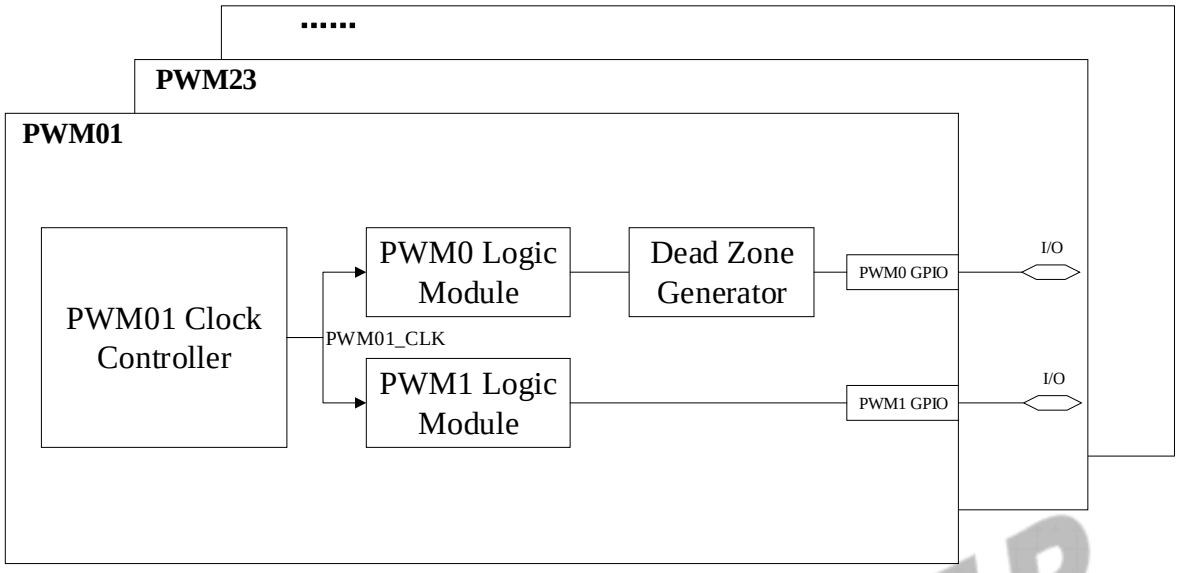
The PWM has the following features:

- Supports 11 independent PWM channels (PWM0 to PWM10)
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range: 0 to 24 MHz or 100 MHz
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Supports 5 complementary pairs output
  - PWM01 pair (PWM0 + PWM1), PWM23 pair (PWM2 + PWM3), PWM45 pair (PWM4 + PWM5), PWM67 pair (PWM6 + PWM7), PWM89 pair (PWM8+PWM9)
  - Supports dead-zone generator, and the dead-zone time is configurable
- Supports 4 group of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Supports 11 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

10.8.2 Block Diagram

The PWM includes multi PWM channels. Each channel can generate different PWM waveform by the independent counter and duty-ratio configuration register. Each PWM pair shares one group of clock and dead-zone generator to generate PWM waveform.

Figure 10-68 PWM Block Diagram



Each PWM pair consists of 1 clock module, 2 timer logic module, and 1 programmable dead-zone generator.

10.8.3 Functional Description

10.8.3.1 External Signals

The following table describes the external signals of the PWM.

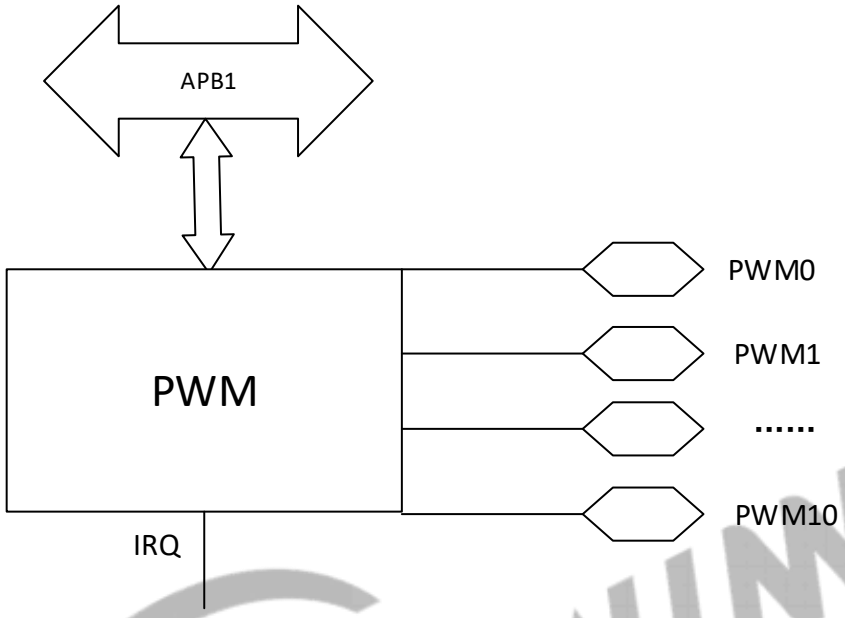
Table 10-34 PWM External Signals

Signal	Description	Type
PWM0	Pulse Width Module Channel0	I/O
PWM1	Pulse Width Module Channel1	I/O
PWM2	Pulse Width Module Channel2	I/O
PWM3	Pulse Width Module Channel3	I/O
PWM4	Pulse Width Module Channel4	I/O
PWM5	Pulse Width Module Channel5	I/O
PWM6	Pulse Width Module Channel6	I/O
PWM7	Pulse Width Module Channel7	I/O
PWM8	Pulse Width Module Channel8	I/O
PWM9	Pulse Width Module Channel9	I/O
PWM10	Pulse Width Module Channel10	I/O

10.8.3.2 Typical Application

The PWM module configure the registers through APB1, output the PWM waveform and generate the interrupt. The typical application is as follows:

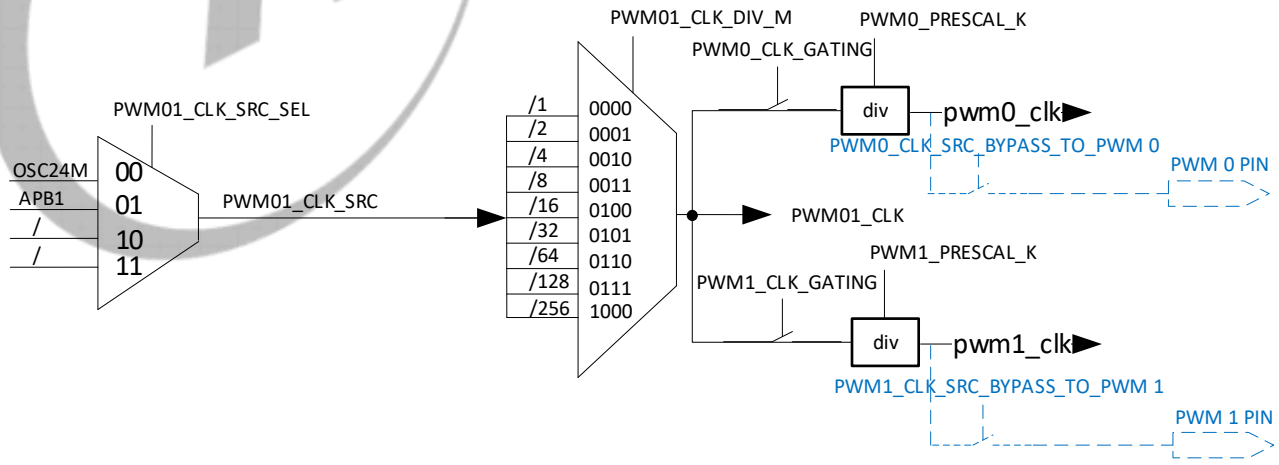
Figure 10-69 PWM Typical Application



10.8.3.3 Clock Controller

Using PWM01 as an example. The other PWM pairs are the same as PWM01.

Figure 10-70 PWM01 Clock Controller Diagram



The clock controller of each PWM pair includes clock source select (PWM01_CLK_SRC), 1~256 scaler (PWM01_CLK_DIV_M). Each PWM channel has the secondary frequency division (PWM_PRESCAL_K), clock source bypass (PWMx_CLK_BYPASS) and clock switch (PWMx_CLK_GATING).

The clock sources have HOSC and APB0. The HOSC comes from the external high-frequency oscillator; the APB0 is APB0 bus clock.

The bypass function of the clock source is that the clock source directly accesses PWM output, the PWM output waveform is the waveform of the clock controller output. The BYPASS gridlines in the above figure indicate the bypass function of the clock source, see Figure 10-71 for the details about implement. At last, the output clock of the clock controller is sent to the PWM logic module.

10.8.3.4 PWM Output

Taking PWM01 as an example, the following figure indicates the PWM01 output logic diagram. The logic diagrams of other PWM pairs are the same as PWM01.

The timer logic module of PWM consists of one 16-bit up-counter (PCNTR) and three 16-bit parameters (PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE, PWM_COUNTER_START). The PWM_ENTIRE_CYCLE is used to control the PWM cycle, the PWM_ACT_CYCLE is used to control the duty-cycle, the PWM_COUNTER_START is used to control the output phase (multi-channel synchronization work requirements).

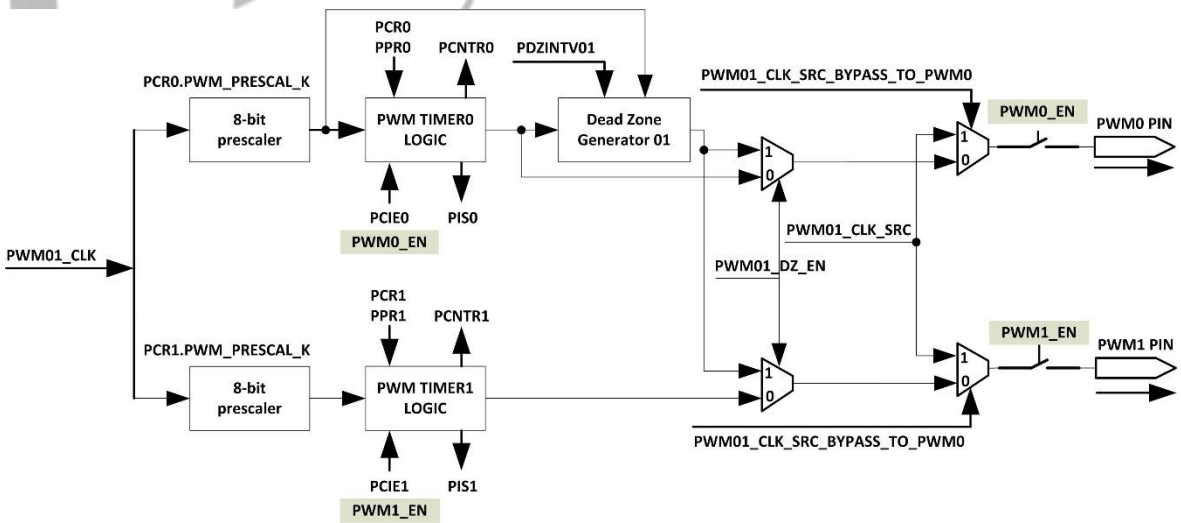
The PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE support the cache load, after PWM output is enabled, the register values of the PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE can be changed anytime, the changed value caches into the cache register. When the PCNTR counter outputs a period of PWM waveform, the value of the cache register can be updated for the PCNTR control. The purpose of the cache load is to avoid the unstable PWM output waveform with the burred feature when updating the values of the PWM_ENTIRE_CYCLE and PWM_ACT_CYCLE.

The PWM supports cycle and pulse waveform output.

Cycle mode: The PWM outputs the setting PWM waveform continually, that is, the output waveform is a continuous PWM square wave.

Pulse mode: After setting the PWM_PUL_NUM parameter, the PWM outputs (PWM_PULNUM+1) periods of PWM waveform, that is, the waveform with several pulses are output.

Figure 10-71 PWM01 Output Logic Module Diagram



10.8.3.5 Up-Counter and Comparator

The period, duty-cycle, and phase of PWM output waveform are decided by the PCNTR, PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE, and PWM_COUNTER_START. The rules are as follows.

- PCNTR= (PCNTR==PWM_ENTIRE_CYCLE)?0 : PCNTR + 1
- PCNTR starts to count by PWM_COUNTER_START, the counter of a PWM period is (PWM_ENTIRE_CYCLE+1).
- PCNTR > (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output "active state"
- PCNTR <= (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output "~ (active state)"

Active state of PWM0 channel is high level (PCR0. PWM_ACT_STA = 1)

When PCNTR0 > (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1 (high level).

When PCNTR0 <= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0 (low level).

The formula of the output period and the duty-cycle for PWM are as follows.

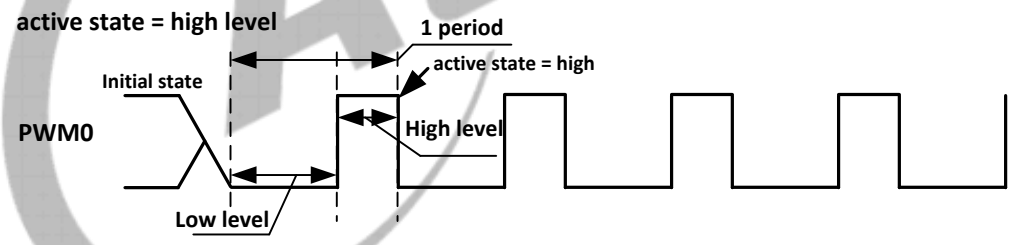
Tperiod = (PWM01_CLK / PWM0_PRESCALE_K)-1 * (PPR0.PWM_ENTIRE_CYCLE + 1)

Thigh-level = (PWM01_CLK / PWM0_PRESCALE_K)-1 * PPR0.PWM_ACT_CYCLE

Tlow-level = (PWM01_CLK / PWM0_PRESCALE_K)-1 * (PPR0.PWM_ENTIRE_CYCLE + 1 - PPR0.PWM_ACT_CYCLE)

Duty-cycle = (high level time) / (1 period time) = Thigh-level / Tperiod

Figure 10-72 PWM0 High Level Active State



Active state of PWM0 channel is low level (PCR0. PWM_ACT_STA = 0)

When PCNTR0 > (PPR0.PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0.

When PCNTR0 <= (PPR0.PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1.

The formula of the output period and the duty-cycle for PWM are as follows.

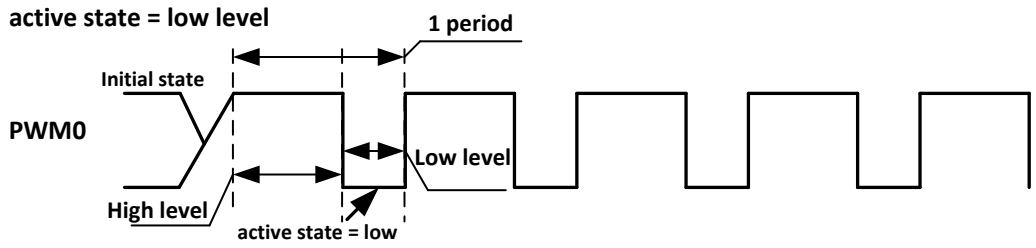
T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE + 1)

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE + 1 - PPR0.PWM_ACT_CYCLE)

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

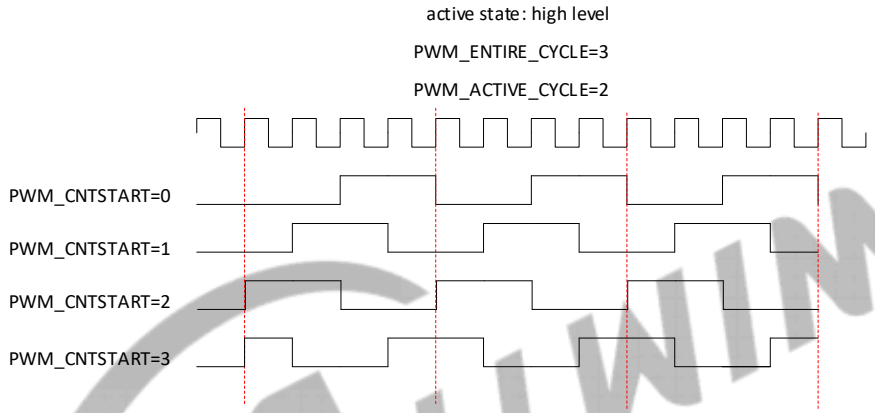
Duty-cycle = (low level time) / (1 period time) = $T_{low\text{-}level}$ /T_{period}

Figure 10-73 PWM0 Low Level Active State



The counter of PCNTR starts from 0 by default, it can output the pulse control of the waveform by setting PWM_COUNTER_START. The figure is as follows.

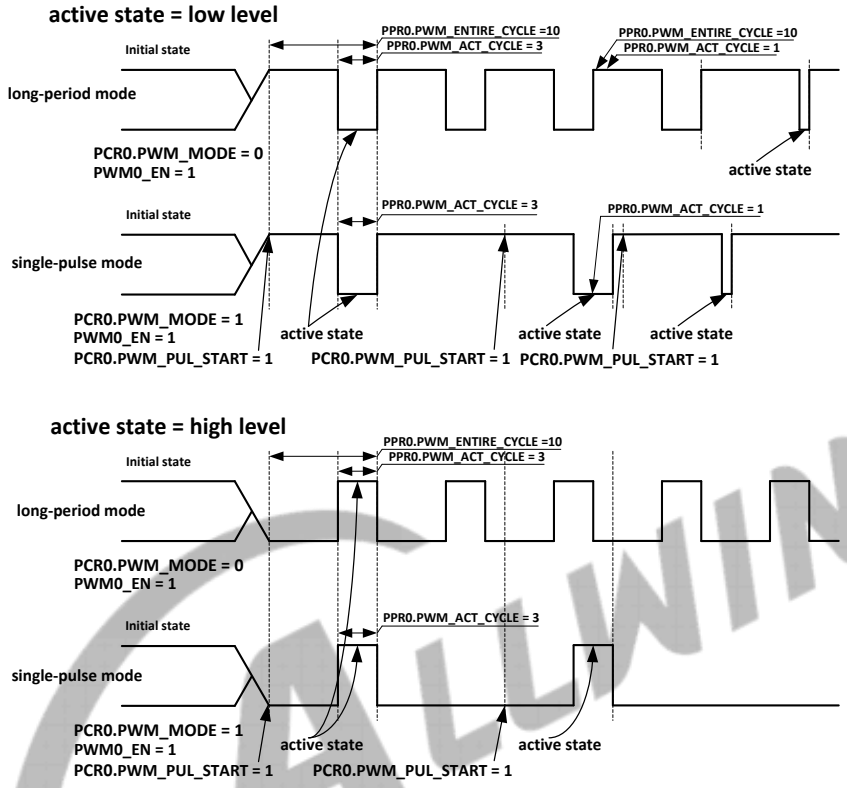
Figure 10-74 Phase of PWM0 High Level Active State



10.8.3.6 Pulse Mode and Cycle Mode

The PWM output supports pulse mode and cycle mode. PWM in pulse mode outputs one pulse waveform, but PWM in cycle mode outputs continuous waveform. The following figure shows the PWM output waveform in pulse mode and cycle mode.

Figure 10-75 PWM0 Output Waveform in Pulse Mode and Cycle Mode



Each channel of the PWM module supports the PWM output of pulse mode and cycle mode, the active state of the PWM output waveform can be programmed to control.

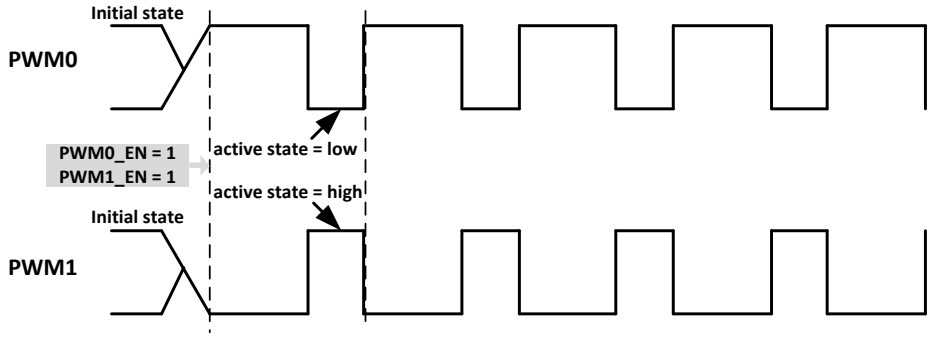
When PCR0[PWM_MODE] is 0, the PWM0 outputs in cycle mode. When PCR0[PWM_MODE] is 1, the PWM0 outputs in pulse mode.

Specifically, in pulse mode, after the PWM0 channel enabled, PCR0[PWM_PUL_START] needs to be set to 1 when the PWM0 needs to output pulse waveform, after completed the output, PCR0[PWM_PUL_START] can be cleared to 0 by hardware. The next setting 1 can be operated after PCR0[PWM_PUL_START] is cleared.

10.8.3.7 Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time. the following figure shows the complementary pair output of PWM01.

Figure 10-76 PWM01 Complementary Pair Output



The complementary pair output needs to satisfy the following conditions:

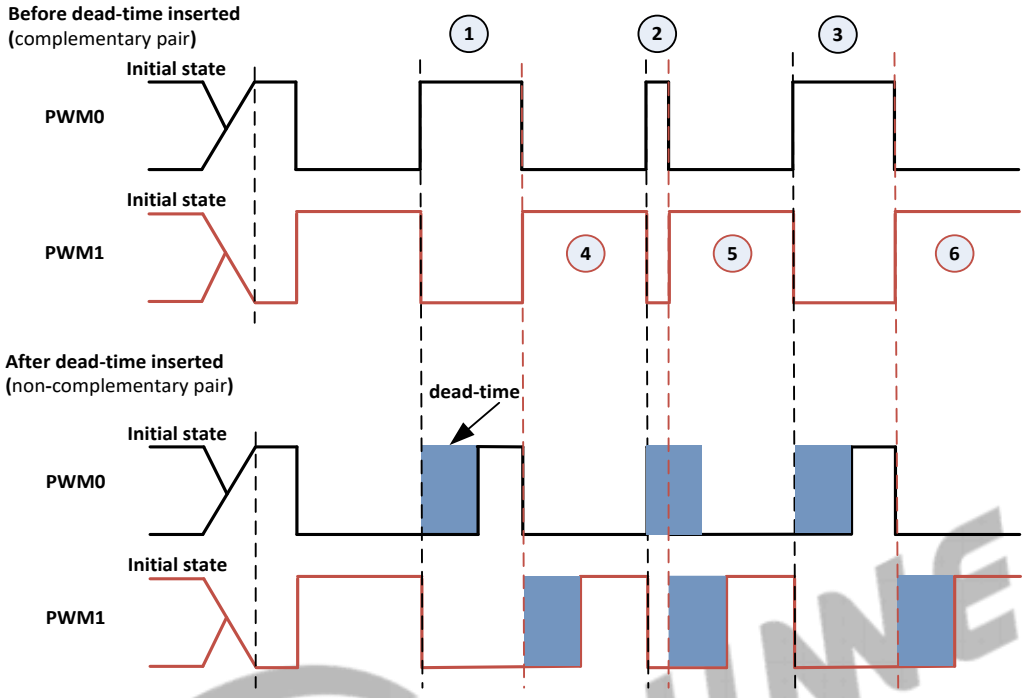
- PWM0 and PWM1 have the same clock divider, frequency, duty-cycle, and phase
- PWM0 and PWM1 have an opposite active state
- Enable the clock gating of PWM0 and PWM1 at the same time
- Enable the waveform output of PWM0 and PWM1 at the same time

10.8.3.8 Dead-time Generator

Every PWM pair has a programmable dead-time generator. When the dead-time function of the PWM pair enabled, the PWM01 output waveform is decided by PWM timer logic and DeadZone Generator.

The following figure shows the output waveform.

Figure 10-77 Dead-time Output Waveform



The PWM waveform before the insertion of dead-time indicates a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.

The PWM waveform after the insertion of dead-time indicates a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01. The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.

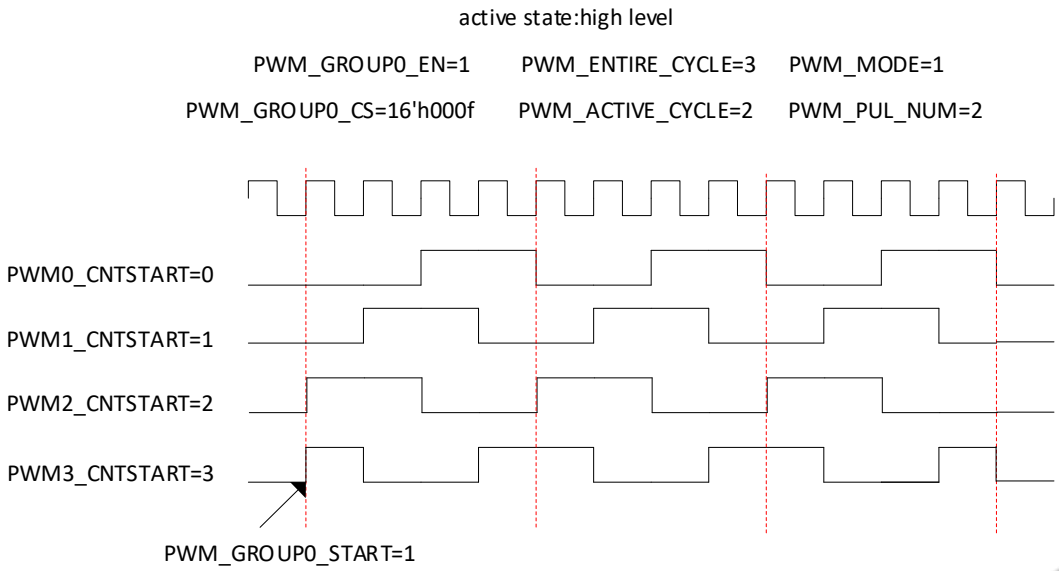
For the complementary pair of Dead Zone Generator 01, the principle of inserting dead-time is that to insert dead-time as soon as the rising edge came. If the high level time for mark② in the above figure is less than dead-time, then dead-time will override the high level. The setting of dead-time needs to consider the period and the duty-cycle of the output waveform. The dead-time formula is defined as follows:

Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)-1 * PDZINTV01

10.8.3.9 PWM Group Mode

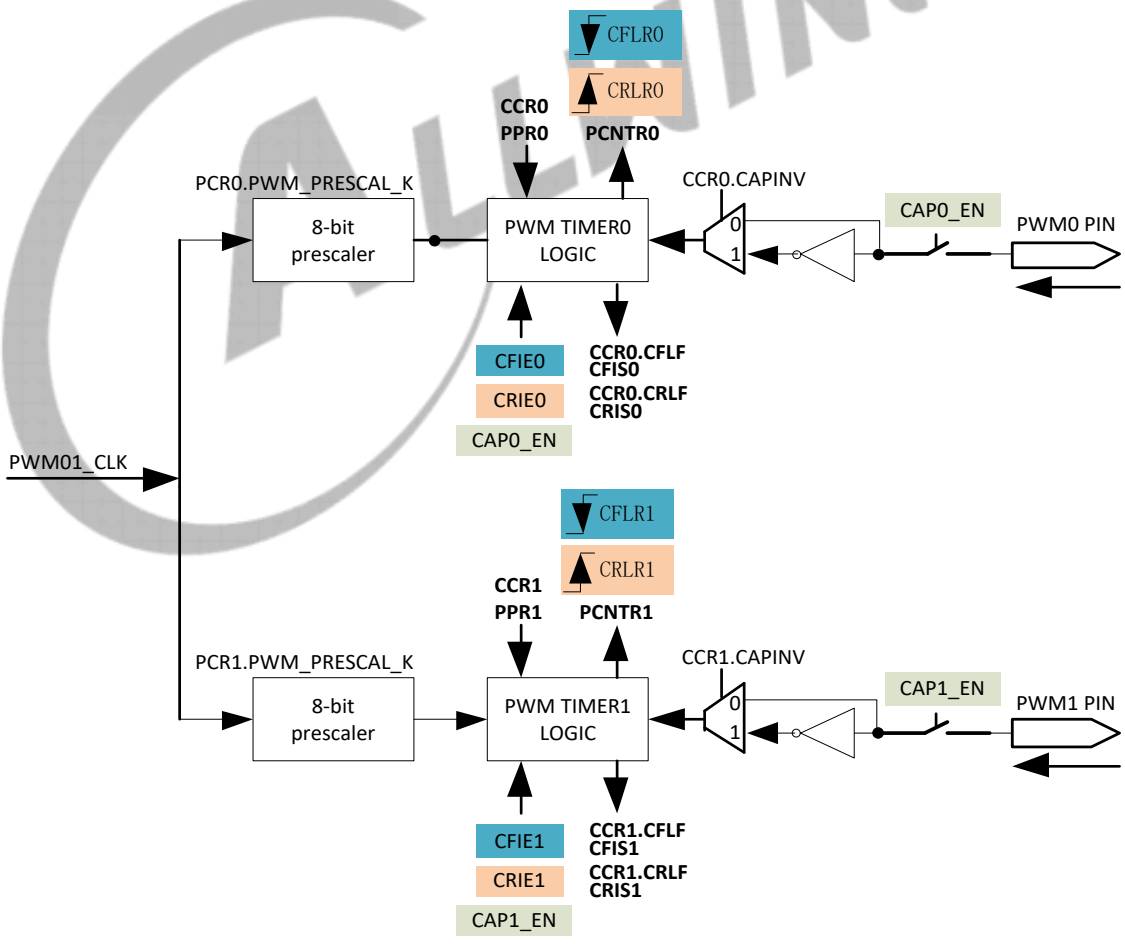
Taking PWM Group0 as an example. The same group of PWM channel is selected to work by PGR0.CS; the same PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE are set by the same clock configuration; the different PWM_COUNTER_START can output PWM group signals with the same duty-cycle and the different phase.

Figure 10-78 Group 0–3 PWM Signal Output



10.8.3.10 Capture Input

Figure 10-79 PWM01 Capture Logic Module Diagram



Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture the rising edge and the falling edge of the external clock. Using the PWM0 channel as an example, the PWM0

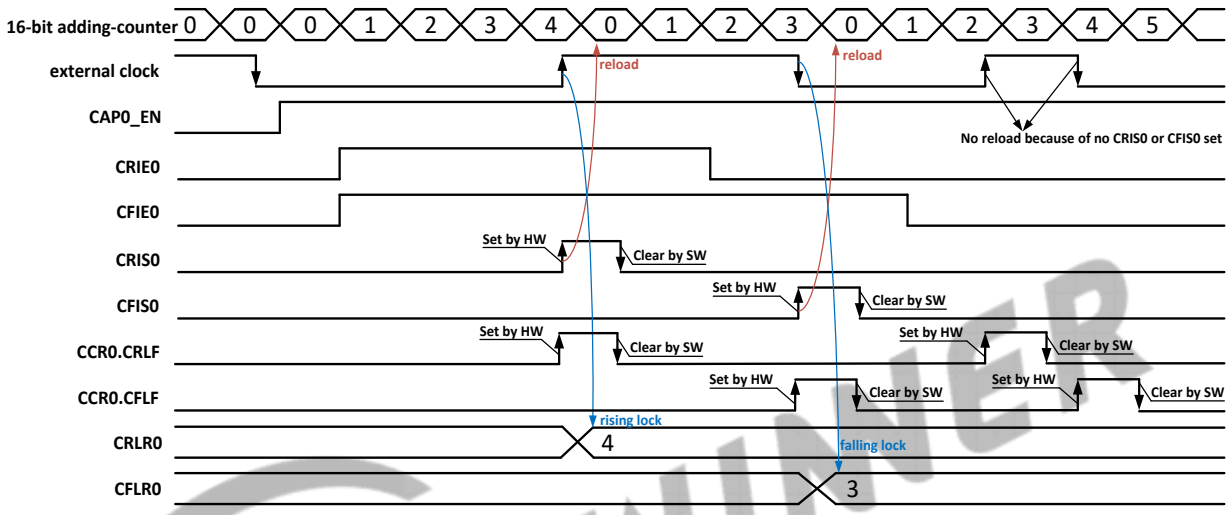
channel has one CFLR0 and one CRLR0 for capturing up-counter value on the falling edge and rising edge, respectively. You can calculate the period of the external clock by CFLR0 and CRLR0.

Thigh-level = (PWM01_CLK / PWM0_PRESCALE_K)-1 * CRLR0

Tlow-level = (PWM01_CLK / PWM0_PRESCALE_K)-1 * CFLR0

Tperiod = Thigh-level + Tlow-level

Figure 10-80 PWM0 Channel Capture Timing



When the capture input function of the PWM0 channel is enabled, the PCNTR of the PWM0 channel starts to work.

When the timer logic module of PWM0 captures a rising edge, the current value of the up-counter is locked to CRLR0 and CCR0[CRLF] is set to 1. If CRIE0 is 1, then CRIS0 is set to 1, the PWM0 channel sends interrupt requests, and the up-counter is loaded to 0 and continues to count. If CRIE0 is 0, the timer logic module of PWM0 captures a rising edge, CRIS0 cannot be set to 1, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of PCNTR is locked to CFLR0 and CCR0[CFLF] is set to 1. If CFIE0 is 1, then CFIS0 is set to 1, the PWM0 channel sends interrupt requests, and the up-counter is loaded to 0 and continues to count. If CFIE0 is 0, the timer logic module of PWM0 captures a falling edge, CFIS0 cannot be set to 1, the up-counter is not loaded to 0.

10.8.3.11 Interrupt

The PWM supports an interrupt generation when configuring the PWM channel to PWM output or capturing input.

For PWM output function, when the controller outputs one period of PWM waveform in cycle mode, the PIS of the corresponding PWM channel is set to 1; when the controller outputs (PWM_PULNUM+1) periods of PWM waveform in pulse mode, the PIS of the corresponding PWM channel is set to 1.

NOTE

The PIS bit is set to 1 automatically by hardware and cleared by software.

For capturing input function, when the timer logic module of the capture channel0 captures rising edge, and CRIE0 is 1, then CRIS0 is set to 1; when the timer logic module of the capture channel0 captures falling edge, and CFIE0 is 1, then CFIS0 is set to 1.

10.8.4 Programming Guidelines

The following working mode takes PWM01 as an example, other PWM pairs and PWM01 are consistent.

10.8.4.1 Configuring Clock

1. PWM gating: When using PWM, write 1 to PCGR[PWMx_CLK_GATING].
2. PWM clock source select: Set PCCR01[PWM01_CLK_SRC] to select HOSC or APB0 clock.
3. PWM clock divider: Set PCCR01[PWM01_CLK_DIV_M] to select different frequency division coefficient (1/2/4/8/16/32/64/128/256).
4. PWM clock bypass: Set PCGR[PWM_CLK_SRC_BYPASS_TO_PWM] to 1, output the PWM clock after the secondary frequency division to the corresponding PWM output pin.
5. PWM internal clock configuration: Set PCR[PWM_PRESCAL_K] to select any frequency division coefficient from 1 to 256.

NOTE

For the channel of complementary output and group mode, firstly, set the same clock configurations (clock source selects APB0, clock division configures the same division factor); secondly, open clock gating at the same time; thirdly, configure PWM parameters; finally, enable PWM output at the same time to ensure each channel sync.

We suggest that the two channels of the same PWM pair cannot subject to two groups because of they have the same first level clock division and gating. If must allocate based on this way, the first level of clock division of the channel used by all groups needs to set to the same coefficient and open gating at the same time. And the total module needs to be reset when the group mode regroups.

10.8.4.2 Configuring PWM

1. PWM mode: Set PCR[PWM_MODE] to select cycle mode or pulse mode, if pulse mode, PCR[PWM_PUL_NUM] needs to be configured.
2. PWM active level: Set PCR[PWM_ACT_STA] to select a low level or high level.

3. PWM duty-cycle: Configure PPR[PWM_ENTIRE_CYCLE] and PPR[PWM_ACT_CYCLE] after clock gating is opened.
4. PWM starting/stoping phase: Configure PCNTR[PWM_COUNTER_START] after the clock gating is enabled and before the PWM is enabled. You can verify whether the configuration was successful by reading back PCNTR[PWM_COUNTER_STATUS].
5. Enable PWM: Configure PER to select the corresponding PWM enable bit; when selecting pulse mode, PCR[PWM_PUL_START] needs to be enabled.

10.8.4.3 Configuring Deadzone

1. Set initial value: set [PDZINTV01].
2. Enable Deadzone: set [PWM01_DZ_CN].

10.8.4.4 Configuring Capture Input

1. Enable capture: Configure CER to enable the corresponding channel.
2. Capture mode: Configure CCR[CRLF] and CCR[CFLF] to select rising edge capture or falling edge capture, configure CCR[CAPINV] to select whether the input signal does reverse processing.

10.8.5 Register List

Module Name	Base Address
PWM	0x02000C00

Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register
PCCR23	0x0024	PWM23 Clock Configuration Register
PCCR45	0x0028	PWM45 Clock Configuration Register
PCCR67	0x002C	PWM67 Clock Configuration Register
PCCR89	0x0030	PWM89 Clock Configuration Register
PCCRa	0x0034	PWMa Clock Configuration Register
PCGR	0x0040	PWM Clock Gating Register
PDZCR01	0x0060	PWM01 Dead Zone Control Register
PDZCR23	0x0064	PWM23 Dead Zone Control Register
PDZCR45	0x0068	PWM45 Dead Zone Control Register
PDZCR67	0x006C	PWM67 Dead Zone Control Register
PDZCR89	0x0070	PWM89 Dead Zone Control Register

Register Name	Offset	Description
PER	0x0080	PWM Enable Register
PGR0	0x0090	PWM Group0 Register
PGR1	0x0094	PWM Group1 Register
PGR2	0x0098	PWM Group2 Register
PGR3	0x009c	PWM Group3 Register
CER	0x00c0	Capture Enable Register
PCR	0x0100+0x0000+N*0x0020(N= 0~10)	PWM Control Register
PPR	0x0100+0x0004+N*0x0020(N= 0~10)	PWM Period Register
PCNTR	0x0100+0x0008+N*0x0020(N= 0~10)	PWM Counter Register
PPCNTR	0x0100+0x000C+N*0x0020(N= 0~10)	PWM Pulse Counter Register
CCR	0x0100+0x0010+N*0x0020(N= 0~10)	Capture Control Register
CRLR	0x0100+0x0014+N*0x0020(N= 0~10)	Capture Rise Lock Register
CFLR	0x0100+0x0018+N*0x0020(N= 0~10)	Capture Fall Lock Register

10.8.6 Register Description

10.8.6.1 0x0000 PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	PGIE3 PWM group 3 Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PGIE2 PWM group 2 Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PGIE1 PWM group 1 Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	PGIE0 PWM group 0 Interrupt Enable 0: Disable 1: Enable
15:11	/	/	/
10	R/W	0x0	PCIE10 PWM channel 10 Interrupt Enable. 0: PWM channel 10 Interrupt Disable; 1: PWM channel 10 Interrupt Enable.

Offset:0x0000			Register Name: PIER
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	PCIE9 PWM channel 9 Interrupt Enable. 0: PWM channel 9 Interrupt Disable; 1: PWM channel 9 Interrupt Enable.
8	R/W	0x0	PCIE8 PWM channel 8 Interrupt Enable. 0: PWM channel 8 Interrupt Disable; 1: PWM channel 8 Interrupt Enable.
7	R/W	0x0	PCIE7 PWM channel 7 Interrupt Enable 0: PWM channel 7 Interrupt Disable; 1: PWM channel 7 Interrupt Enable.
6	R/W	0x0	PCIE6 PWM channel 6 Interrupt Enable. 0: PWM channel 6 Interrupt Disable; 1: PWM channel 6 Interrupt Enable.
5	R/W	0x0	PCIE5 PWM channel 5 Interrupt Enable 0: PWM channel 5 Interrupt Disable; 1: PWM channel 5 Interrupt Enable.
4	R/W	0x0	PCIE4 PWM channel 4 Interrupt Enable 0: PWM channel 4 Interrupt Disable; 1: PWM channel 4 Interrupt Enable.
3	R/W	0x0	PCIE3 PWM channel 3 Interrupt Enable 0: PWM channel 3 Interrupt Disable; 1: PWM channel 3 Interrupt Enable.
2	R/W	0x0	PCIE2 PWM channel 2 Interrupt Enable 0: PWM channel 2 Interrupt Disable; 1: PWM channel 2 Interrupt Enable.
1	R/W	0x0	PCIE1 PWM channel 1 Interrupt Enable 0: PWM channel 1 Interrupt Disable; 1: PWM channel 1 Interrupt Enable.
0	R/W	0x0	PCIE0 PWM channel 0 Interrupt Enable 0: PWM channel 0 Interrupt Disable; 1: PWM channel 0 Interrupt Enable.

10.8.6.2 0x0004 PWM IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: PISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W1C	0x0	PGIS3 PWM group 3 Interrupt Status
18	R/W1C	0x0	PGIS2 PWM group 3 Interrupt Status
17	R/W1C	0x0	PGIS1 PWM group 1 Interrupt Status
16	R/W1C	0x0	PGIS0 PWM group 0 Interrupt Status
15:11	/	/	/
10	R/W1C	0x0	PIS10 PWM channel 10 Interrupt Status. When PWM channel 10 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 10 interrupt is not pending. Reads 1: PWM channel 10 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 10 interrupt status.
9	R/W1C	0x0	PIS9 PWM channel 9 Interrupt Status. When PWM channel 9 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 9 interrupt is not pending. Reads 1: PWM channel 9 interrupt is pending. Writes 0: no effect. Writes 1: Clear PWM channel 9 interrupt status.
8	R/W1C	0x0	PIS8 PWM channel 8 Interrupt Status. When PWM channel 8 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 8 interrupt is not pending. Reads 1: PWM channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 8 interrupt status.

Offset:0x0004			Register Name: PISR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W1C	0x0	PIS7 PWM channel 7 Interrupt Status. When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. Reads 1: PWM channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6 PWM channel 6 Interrupt Status. When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. Reads 1: PWM channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5 PWM channel 5 Interrupt Status. When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. Reads 1: PWM channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4 PWM channel 4 Interrupt Status. When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. Reads 1: PWM channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3 PWM channel 3 Interrupt Status. When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. Reads 1: PWM channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 3 interrupt status.

Offset:0x0004			Register Name: PISR
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W1C	0x0	PIS2 PWM channel 2 Interrupt Status. When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. Reads 1: PWM channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1 PWM channel 1 Interrupt Status. When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. Reads 1: PWM channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0 PWM channel 0 Interrupt Status. When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. Reads 1: PWM channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 0 interrupt status.

10.8.6.3 0x0010 Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: CIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	CFIE10 If this enable bit is set 1, when capture channel 10 captures falling edge, it generates a capture channel 10 pending. 0: Capture channel 10 fall lock Interrupt disable; 1: Capture channel 10 fall lock Interrupt enable.
20	R/W	0x0	CRIE10 If this enable bit is set 1, when capture channel 10 captures rising edge, it generates a capture channel 10 pending. 0: Capture channel 10 rise lock Interrupt disable; 1: Capture channel 10 rise lock Interrupt enable.

Offset:0x0010			Register Name: CIER
Bit	**Read/Write**	**Default/Hex**	**Description**
19	R/W	0x0	CFIE9 If this enable bit is set 1, when capture channel 9 captures falling edge, it generates a capture channel 9 pending. 0: Capture channel 9 fall lock Interrupt disable; 1: Capture channel 9 fall lock Interrupt enable.
18	R/W	0x0	CRIE9 If this enable bit is set 1, when capture channel 9 captures rising edge, it generates a capture channel 9 pending. 0: Capture channel 9 rise lock Interrupt disable; 1: Capture channel 9 rise lock Interrupt enable.
17	R/W	0x0	CFIE8 If this enable bit is set 1, when capture channel 8 captures falling edge, it generates a capture channel 8 pending. 0: Capture channel 8 fall lock Interrupt disable; 1: Capture channel 8 fall lock Interrupt enable.
16	R/W	0x0	CRIE8 If this enable bit is set 1, when capture channel 8 captures rising edge, it generates a capture channel 8 pending. 0: Capture channel 8 rise lock Interrupt disable; 1: Capture channel 8 rise lock Interrupt enable.
15	R/W	0x0	CFIE7 If this enable bit is set 1, when capture channel 7 captures falling edge, it generates a capture channel 7 pending. 0: Capture channel 7 fall lock Interrupt disable; 1: Capture channel 7 fall lock Interrupt enable.
14	R/W	0x0	CRIE7 If this enable bit is set 1, when capture channel 7 captures rising edge, it generates a capture channel 7 pending. 0: Capture channel 7 rise lock Interrupt disable; 1: Capture channel 7 rise lock Interrupt enable.
13	R/W	0x0	CFIE6 If this enable bit is set 1, when capture channel 6 captures falling edge, it generates a capture channel 6 pending. 0: Capture channel 6 fall lock Interrupt disable; 1: Capture channel 6 fall lock Interrupt enable.
12	R/W	0x0	CRIE6 If this enable bit is set 1, when capture channel 6 captures rising edge, it generates a capture channel 6 pending. 0: Capture channel 6 rise lock Interrupt disable; 1: Capture channel 6 rise lock Interrupt enable.

Offset:0x0010			Register Name: CIER
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W	0x0	CFIE5 If this enable bit is set 1, when capture channel 5 captures falling edge, it generates a capture channel 5 pending. 0: Capture channel 5 fall lock Interrupt disable; 1: Capture channel 5 fall lock Interrupt enable.
10	R/W	0x0	CRIE5 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
9	R/W	0x0	CFIE4 If this enable bit is set 1, when capture channel 4 captures falling edge, it generates a capture channel 4 pending. 0: Capture channel 4 fall lock Interrupt disable; 1: Capture channel 4 fall lock Interrupt enable.
8	R/W	0x0	CRIE4 If this enable bit is set 1, when capture channel 4 captures rising edge, it generates a capture channel 4 pending. 0: Capture channel 4 rise lock Interrupt disable; 1: Capture channel 4 rise lock Interrupt enable.
7	R/W	0x0	CFIE3 If this enable bit is set 1, when capture channel 3 captures falling edge, it generates a capture channel 3 pending. 0: Capture channel 3 fall lock Interrupt disable; 1: Capture channel 3 fall lock Interrupt enable.
6	R/W	0x0	CRIE3 If this enable bit is set 1, when capture channel 3 captures rising edge, it generates a capture channel 3 pending. 0: Capture channel 3 rise lock Interrupt disable; 1: Capture channel 3 rise lock Interrupt enable.
5	R/W	0x0	CFIE2 If this enable bit is set 1, when capture channel 2 captures falling edge, it generates a capture channel 2 pending. 0: Capture channel 2 fall lock Interrupt disable; 1: Capture channel 2 fall lock Interrupt enable.
4	R/W	0x0	CRIE2 If this enable bit is set 1, when capture channel 2 captures rising edge, it generates a capture channel 2 pending. 0: Capture channel 2 rise lock Interrupt disable; 1: Capture channel 2 rise lock Interrupt enable.

Offset:0x0010			Register Name: CIER
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	CFIE1 If this enable bit is set 1, when capture channel 1 captures falling edge, it generates a capture channel 1 pending. 0: Capture channel 1 fall lock Interrupt disable; 1: Capture channel 1 fall lock Interrupt enable.
2	R/W	0x0	CRIE1 If this enable bit is set 1, when capture channel 1 captures rising edge, it generates a capture channel 1 pending. 0: Capture channel 1 rise lock Interrupt disable; 1: Capture channel 1 rise lock Interrupt enable.
1	R/W	0x0	CFIE0 If this enable bit is set 1, when capture channel 0 captures falling edge, it generates a capture channel 0 pending. 0: Capture channel 0 fall lock Interrupt disable; 1: Capture channel 0 fall lock Interrupt enable.
0	R/W	0x0	CRIE0 If this enable bit is set 1, when capture channel 0 captures rising edge, it generates a capture channel 0 pending. 0: Capture channel 0 rise lock Interrupt disable; 1: Capture channel 0 rise lock Interrupt enable.

10.8.6.4 0x0014 Capture IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W1C	0x0	CFIS10 Capture channel 10 falling lock interrupt status. When capture channel 10 captures falling edge, if capture channel 10 fall lock interrupt (CFIE10) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 10 interrupt is not pending. Reads 1: Capture channel 10 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 10 interrupt status.

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
20	R/W1C	0x0	CRIS10 Capture channel 10 rising lock interrupt status. When capture channel 10 captures rising edge, if capture channel 10 rise lock interrupt (CRIE10) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 10 interrupt is not pending. Reads 1: Capture channel 10 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 10 interrupt status.
19	R/W1C	0x0	CFIS9 Capture channel 9 falling lock interrupt status. When capture channel 9 captures falling edge, if capture channel 9 fall lock interrupt (CFIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. Reads 1: Capture channel 9 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 9 interrupt status.
18	R/W1C	0x0	CRIS9 Capture channel 9 rising lock interrupt status. When capture channel 9 captures rising edge, if capture channel 9 rise lock interrupt (CRIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. Reads 1: Capture channel 9 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 9 interrupt status.
17	R/W1C	0x0	CFIS8 Capture channel 8 falling lock interrupt status. When capture channel 8 captures falling edge, if capture channel 8 fall lock interrupt (CFIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. Reads 1: Capture channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 8 interrupt status.

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
16	R/W1C	0x0	CRIS8 Capture channel 8 rising lock interrupt status. When capture channel 8 captures rising edge, if capture channel 8 rise lock interrupt (CRIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. Reads 1: Capture channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 8 interrupt status.
15	R/W1C	0x0	CFIS7 Capture channel 7 falling lock interrupt status. When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (CFIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. Reads 1: Capture channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capture channel 7 rising lock interrupt status. When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (CRIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. Reads 1: Capture channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6 Capture channel 6 falling lock interrupt status. When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (CFIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. Reads 1: Capture channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 6 interrupt status.

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W1C	0x0	CRIS6 Capture channel 6 rising lock interrupt status. When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (CRIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. Reads 1: Capture channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capture channel 5 falling lock interrupt status. When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (CFIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. Reads 1: Capture channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 5 interrupt status.
10	R/W1C	0x0	CRIS5 Capture channel 5 rising lock interrupt status. When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (CRIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. Reads 1: Capture channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 5 interrupt status.
9	R/W1C	0x0	CFIS4 Capture channel 4 falling lock interrupt status. When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (CFIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. Reads 1: Capture channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 4 interrupt status.

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W1C	0x0	CRIS4 Capture channel 4 rising lock interrupt status. When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (CRIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. Reads 1: Capture channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (CFIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (CRIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (CFIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 2 interrupt status.

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
4	R/W1C	0x0	CRIS2. Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (CRIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (CFIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (CRIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (CFIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 0 interrupt status.

Offset:0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (CRIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 0 interrupt status.

10.8.6.5 0x0020 PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PCCR01
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM01_CLK_SRC Select PWM01 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM01_CLK_DIV_M PWM01 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.8.6.6 0x0024 PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PCCR23
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/

Offset: 0x0024			Register Name: PCCR23
Bit	**Read/Write**	**Default/Hex**	**Description**
8:7	R/W	0x00	PWM23_CLK_SRC_SEL Select PWM23 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM23_CLK_DIV_M PWM23 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.8.6.7 0x0028 PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PCCR45
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x00	PWM45_CLK_SRC_SEL Select PWM45 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM45_CLK_DIV_M PWM45 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.8.6.8 0x002C PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PCCR67
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x00	PWM67_CLK_SRC_SEL Select PWM67 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM67_CLK_DIV_M PWM67 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.8.6.9 0x0030 PWM89 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PCCR89
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x00	PWM89_CLK_SRC_SEL Select PWM89 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/

Offset: 0x0030			Register Name: PCCR89
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0000	PWM89_CLK_DIV_M PWM89 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.8.6.10 0x0034 PWMa Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PCCR89
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x00	PWMa_CLK_SRC_SEL Select PWMa clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWMa_CLK_DIV_M PWMa clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

10.8.6.11 0x0040 PWM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PCGR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	PWM10_CLK_BYPASS Bypass clock source (after pre-scale) to PWM10 output 0: not bypass 1: bypass
25	R/W	0x0	PWM9_CLK_BYPASS Bypass clock source (after pre-scale) to PWM9 output 0: not bypass 1: bypass
24	R/W	0x0	PWM8_CLK_BYPASS Bypass clock source (after pre-scale) to PWM8 output 0: not bypass 1: bypass
23	R/W	0x0	PWM7_CLK_BYPASS Bypass clock source (after pre-scale) to PWM7 output 0: not bypass 1: bypass
22	R/W	0x0	PWM6_CLK_BYPASS Bypass clock source (after pre-scale) to PWM6 output 0: not bypass 1: bypass
21	R/W	0x0	PWM5_CLK_BYPASS Bypass clock source (after pre-scale) to PWM5 output 0: not bypass 1: bypass
20	R/W	0x0	PWM4_CLK_BYPASS Bypass clock source (after pre-scale) to PWM4 output 0: not bypass 1: bypass
19	R/W	0x0	PWM3_CLK_BYPASS Bypass clock source (after pre-scale) to PWM3 output 0: not bypass 1: bypass
18	R/W	0x0	PWM2_CLK_BYPASS Bypass clock source (after pre-scale) to PWM2 output 0: not bypass 1: bypass

Offset: 0x0040			Register Name: PCGR
Bit	**Read/Write**	**Default/Hex**	**Description**
17	R/W	0x0	PWM1_CLK_BYPASS Bypass clock source (after pre-scale) to PWM1 output 0: not bypass 1: bypass
16	R/W	0x0	PWM0_CLK_BYPASS Bypass clock source (after pre-scale) to PWM0 output 0: not bypass 1: bypass
15:11	/	/	/
10	R/W	0x0	PWM10_CLK_GATING Gating clock for PWM10 0: Mask 1: Pass
9	R/W	0x0	PWM9_CLK_GATING Gating clock for PWM9 0: Mask 1: Pass
8	R/W	0x0	PWM8_CLK_GATING Gating clock for PWM8 0: Mask 1: Pass
7	R/W	0x0	PWM7_CLK_GATING Gating clock for PWM7 0: Mask 1: Pass
6	R/W	0x0	PWM6_CLK_GATING Gating clock for PWM6 0: Mask 1: Pass
5	R/W	0x0	PWM5_CLK_GATING Gating clock for PWM5 0: Mask 1: Pass
4	R/W	0x0	PWM4_CLK_GATING Gating clock for PWM4 0: Mask 1: Pass
3	R/W	0x0	PWM3_CLK_GATING Gating clock for PWM3 0: Mask 1: Pass

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	PWM2_CLK_GATING Gating clock for PWM2 0: Mask 1: Pass
1	R/W	0x0	PWM1_CLK_GATING Gating clock for PWM1 0: Mask 1: Pass
0	R/W	0x0	PWM0_CLK_GATING Gating clock for PWM0 0: Mask 1: Pass

10.8.6.12 0x0060 PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: PDZCR01
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01 PWM01 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable.

10.8.6.13 0x0064 PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: PDZCR23
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN PWM23 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable.

10.8.6.14 0x0068 PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: PDZCR45
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM45_DZ_INTV PWM45 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN PWM45 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable.

10.8.6.15 0x006C PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: PDZCR67
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM67_DZ_INTV PWM67 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN PWM67 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable.

10.8.6.16 0x0070 PWM89 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PDZCR89
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM89_DZ_INTV PWM89Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM89_DZ_EN PWM89 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable.

10.8.6.17 0x0080 PWM Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	PWM10_EN PWM Channel 10 Enable 0: PWM disable 1: PWM enable.
9	R/W	0x0	PWM9_EN PWM Channel 9 Enable 0: PWM disable 1: PWM enable.
8	R/W	0x0	PWM8_EN PWM Channel 8 Enable 0: PWM disable 1: PWM enable.
7	R/W	0x0	PWM7_EN PWM Channel 7 Enable 0: PWM disable 1: PWM enable.
6	R/W	0x0	PWM6_EN PWM Channel 6 Enable 0: PWM disable 1: PWM enable.
5	R/W	0x0	PWM5_EN PWM Channel 5 Enable 0: PWM disable 1: PWM enable.
4	R/W	0x0	PWM4_EN PWM Channel 4 Enable 0: PWM disable 1: PWM enable.
3	R/W	0x0	PWM3_EN PWM Channel 3 Enable 0: PWM disable 1: PWM enable.
2	R/W	0x0	PWM2_EN PWM Channel 2 Enable 0: PWM disable 1: PWM enable.

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	PWM1_EN PWM Channel 1 Enable 0: PWM disable 1: PWM enable.
0	R/W	0x0	PWM0_EN PWM Channel 0 Enable 0: PWM disable 1: PWM enable.

10.8.6.18 0x0090 PWM Group0 Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: PGR0
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG0_START PWM channels selected in PWMG0_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG0_EN PWM Group0 Enable.
15:0	R/W	0x0	PWMG0_CS If bit[i] is set, PWM i is selected as one channel of PWM Group0.

10.8.6.19 0x0094 PWM Group1 Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: PGR1
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG1_START PWM channels selected in PWMG1_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG1_EN PWM Group1 Enable.
15:0	R/W	0x0	PWMG1_CS If bit[i] is set, PWM i is selected as one channel of PWM Group1.

10.8.6.20 0x0098 PWM Group2 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: PGR2
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG2_START PWM channels selected in PWMG2_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG2_EN PWM Group2 Enable.
15:0	R/W	0x0	PWMG2_CS If bit[i] is set, PWM i is selected as one channel of PWM Group2.

10.8.6.21 0x009C PWM Group3 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PGR3
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG3_START PWM channels selected in PWMG3_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG3_EN PWM Group3 Enable.
15:0	R/W	0x0	PWMG3_CS If bit[i] is set, PWM i is selected as one channel of PWM Group3.

10.8.6.22 0x00C0 Capture Enable Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CAP10_EN When enable capture function, the 16-bit up-counter starts working and capture channel10 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

Offset: 0x00C0			Register Name: CER
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	CAP9_EN When enable capture function, the 16-bit up-counter starts working and capture channel9 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
8	R/W	0x0	CAP8_EN When enable capture function, the 16-bit up-counter starts working and capture channel8 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
7	R/W	0x0	CAP7_EN When enable capture function, the 16-bit up-counter starts working and capture channel7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
6	R/W	0x0	CAP6_EN When enable capture function, the 16-bit up-counter starts working and capture channel6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
5	R/W	0x0	CAP5_EN When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
4	R/W	0x0	CAP4_EN When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
3	R/W	0x0	CAP3_EN When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

Offset: 0x00C0			Register Name: CER
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	CAP2_EN When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
1	R/W	0x0	CAP1_EN When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
0	R/W	0x0	CAP0_EN. When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

10.8.6.23 0x0100+N*0x0020(N= 0~10) PWM Control Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0000+N*0x0020(N= 0~10)			Register Name: PCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_PUL_NUM In pulse mode, PWM output pulse for PWM_CYCLE_NUM+1 times and then stop.
15:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM period register ready 0: PWM period register is ready to write 1: PWM period register is busy.
10	R/WAC	0x0	PWM_PUL_START PWM pulse output start 0: No effect 1: output pulse for PWM_CYCLE_NUM+1 After finishing configuration for outputting pulse, set this bit once and then PWM would output waveform. After the waveform is finished, the bit will be cleared automatically.

Offset: 0x0100+0x0000+N*0x0020(N= 0~10)			Register Name: PCR
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	PWM_MODE PWM output mode select 0: cycle mode 1: pulse mode.
8	R/W	0x0	PWM_ACT_STA PWM active state 0: Low Level 1: High Level.
7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1) K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256.

10.8.6.24 0x0104+N*0x0020(N= 0~10) PWM Period Register (Default Value: 0x0000_0000)

Offset:0x0100+0x0004+N*0x0020(N= 0~10)			Register Name: PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock 0 = 1 cycle 1 = 2 cycles ..... N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK .
15:0	R/W	0x0	PWM_ACT_CYCLE Number of the active cycles in the PWM clock 0 = 0 cycle 1 = 1 cycles ..... N = N cycles

10.8.6.25 0x0108+N*0x0020(N= 0~10) PWM Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0008+N*0x0020(N= 0~10)			Register Name: PCNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_COUNTER_START PWM counter value is set for phase control.
15:0	R	0x0	PWM_COUNTER_STATUS On PWM output or capture input, reading this register could get the current value of the PWM 16bit up-counter.

10.8.6.26 0x010C+N*0x0020(N= 0~10) PWM Pulse Counter Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x000C+N*0x0020(N= 0~10)			Register Name: PPCNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	PWM_PUL_COUNTER_STATUS On PWM output , reading this register could get the current value of the PWM pulse counter.

10.8.6.27 0x0110+N*0x0020(N= 0~10) Capture Control Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0010+N*0x0020(N= 0~10)			Register Name: CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	CRLF When capture channel captures rising edge, the 16-bit up-counter's current value is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
3	R/W1C	0x0	CFLF When capture channel captures falling edge, the 16-bit up-counter's current value is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
2	R/W	0x0	CRTE Rising edge capture trigger enable
1	R/W	0x0	CFTE Falling edge capture trigger enable

Offset: 0x0100+0x0010+N*0x0020(N= 0~10)			Register Name: CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	CAPINV Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: not inverse 1: inverse

10.8.6.28 0x0114+N*0x0020(N= 0~10) Capture Rise Lock Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0014+N*0x0020(N= 0~10)			Register Name: CRLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	CRLR When capture channel captures rising edge, the 16-bit up-counter’s current value is latched to this register.

10.8.6.29 0x0118+N*0x0020(N= 0~10) Capture Fall Lock Register (Default Value: 0x0000_0000)

Offset: 0x0100+0x0018+N*0x0020(N= 0~10)			Register Name: CFLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	CFLR When capture channel captures falling edge, the 16-bit up-counter’s current value is latched to this register.

10.9 Wiegand Protocol

10.9.1 Overview

The Wiegand Protocol is a communication protocol developed by Motorola, which is commonly used in the card readers and IC cards of access control systems. The WIEGAND_CTRL is a data reading control module for external Wiegand devices. CPU can configure this module through the APB bus to receive the signals of DATA0 and DATA1 sent by external Wiegand devices.

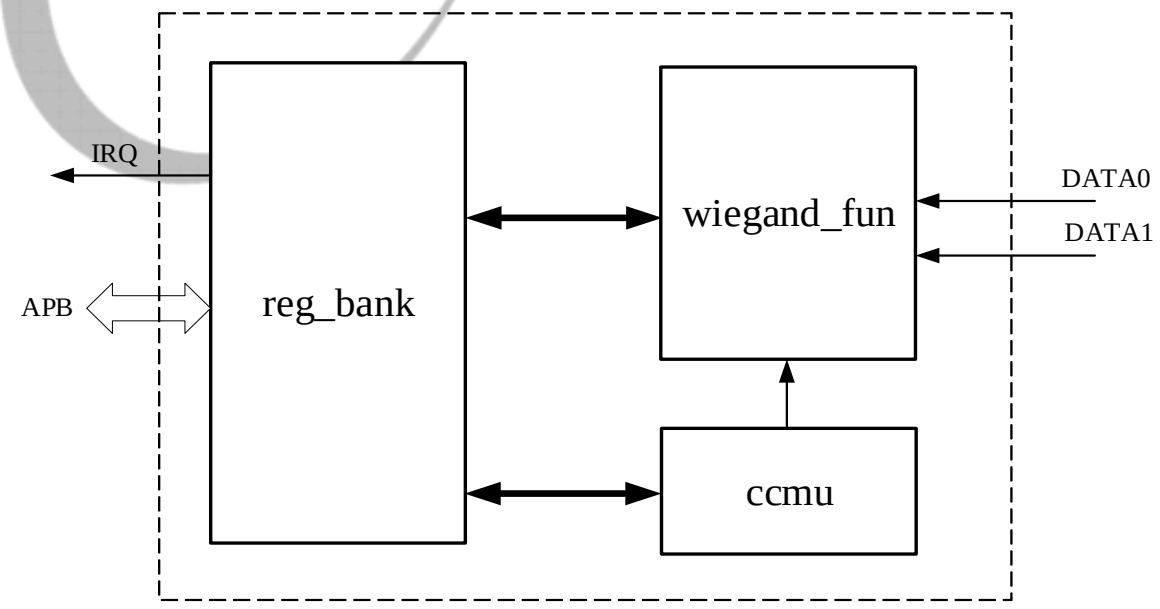
The features of The Wiegand Protocol are as follows:

- Support 26-bit & 34-bit Wiegand protocol formats.
- Support the configurable duration and period of Wiegand data waveforms.
- Support CPU to access the configuration register and data transmission through the APB bus.
- Support receive completion interrupt, parity error reporting interrupt and receive timeout interrupt.
- Support observing the number and contents of received data during the timeout interrupt.
- Support configuring the highest and lowest parity bit polarity.
- Support configuring the polarity of DATA0 and DATA1.
- Support adjusting the frequency dividing coefficients of internal counting reference clock.

10.9.2 Block Diagram

As shown in Figure 10-81, the WIEGAND_CTRL module is composed of the register file REG_BANK, the Wiegand protocol function module WIEGAND_FUN, the clock module ccmu and some interfaces.

Figure 10-81 Block Diagram of WIEGAND_CTRL Module



10.9.3 Functional Description

10.9.3.1 External Signals

The following table describes the external signals of WIEGAND_CTRL.

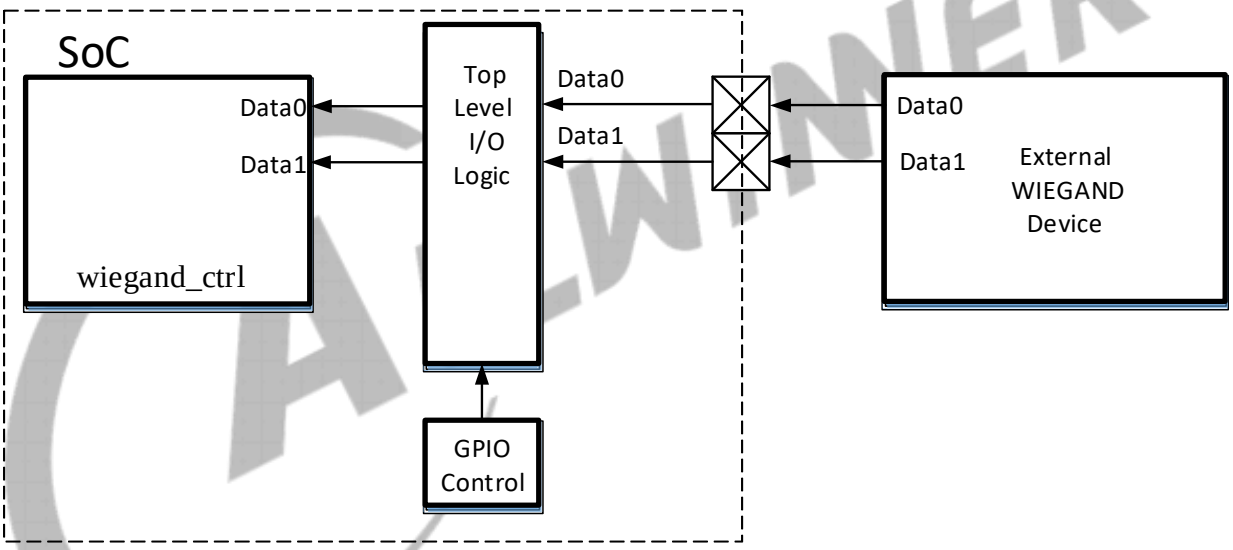
Table 10-35 External Signals of WIEGAND_CTRL

Wiegand Interface Signal	Description	Type	Width
DATA0	Input Signal Line 0 of Wiegand Protocol	I	1
DATA1	Input Signal Line 1 of Wiegand Protocol	I	1

10.9.3.2 Typical Application

As shown in Figure 10-82, the GPIO controller must be correctly configured to connect the WIEGAND_CTRL module to external devices.

Figure 10-82 Application Diagram of WIEGAND_CTRL Module



26-bit Wiegand Protocol

As shown in Table 10-36, the bits 1 to 8 are group codes (HID codes of electronic card), which have 8 binary data and 256 states.

The bits 9 to 24 are identification codes (PID codes of electronic card), which have 16 binary data and 65536 states.

Bit 0 is the even party bit of bits 1 to 12; bit 25 is the odd parity bit of bits 13 to 24.

HID code is the abbreviation of Hidden ID Code; PID code is the abbreviation of Public ID Code.

Table 10-36 Data Format of Wiegand (26-bit)

Bits	Meaning
Bit 0	Even party bit of bits 1 to 12

Bits	Meaning
Bits 1-8	Group Code (PID code of electronic card)
Bits 9-24	Identification Code (PID code of electronic card)
Bit 25	Odd parity bit of bits 13 to 24

The Wiegand transmitter outputs 26-bit data through DATA0 and DATA1, which are kept at a high level of +5V when there is no data. If the output is 0, the DATA0 will be at a low level for some time; if the output is 1, the DATA1 will be at a low level for some time. To prevent the data reading conflicts, the minimum interval between the Wiegand outputs of two electronic cards is 0.25 seconds. For example, in the bus or subway, if multiple cards are stacked together, any of them may not be successfully swiped.

To ensure that card numbers are correct and not mixed up, they are verified by means of odd parity or even parity.

Odd Parity: During the bit transmission, an additional bit is taken as a check bit. If the number of "1" in the total data is even, the check bit is "1", otherwise the check bit is "0". The received data will be checked according to the requirements of odd parity. If the number of "1" is odd, it indicates the transmission is correct, otherwise the transmission is wrong.

Even Parity: During the bit transmission, an additional bit is taken as a check bit. If the number of "1" in the total data is odd, the check bit is "1", otherwise the check bit is "0". The received data will be checked according to the requirements of even parity. If the number of "1" is even, it indicates the transmission is correct, otherwise the transmission is wrong.

34-bit Wiegand Protocol

As shown in Table 10-37, the bits 1 to 16 are group codes (HID code of electronic card), which have 8 binary data and 256 states.

The bits 17 to 32 are identification codes (PID code of electronic card), which have 16 binary data and 65536 states.

Bit 0 is the even party bit of bits 1 to 16; bit 33 is the odd parity bit of bits 17 to 32.

HID code is the abbreviation of Hidden ID Code; PID code is the abbreviation of Public ID Code.

Table 10-37 Data Format of Wiegand (34-bit)

Bits	Meaning
Bit 0	Even party bit of bits 1 to 16
Bits 1-16	Group Code (PID code of electronic card)
Bits 17-32	Identification Code (PID code of electronic card)
Bit 33	Odd parity bit of bits 17 to 32

Configurable Parity Check Polarity and Input Port Polarity

This module supports configurable parity check polarity and input port polarity for better compatibility. As stipulated by the 26-bit & 34-bit Wiegand Protocol, high bit is odd check bit while low bit is even check bit. This

module supports configuring the parity type of high and low parity bits. Please see the Section 6.10 for more details.

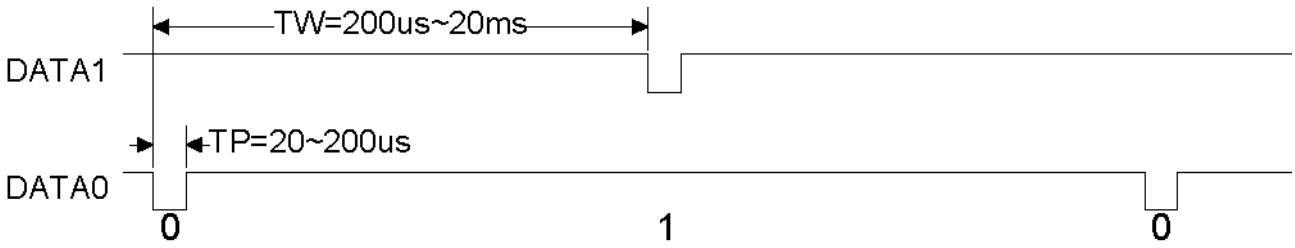
The input signal polarity can be configured by the WIEGAND_DBP register to cope with the situation that the signals of DATA0 and DATA1 are reversely connected.

10.9.3.3 Functions

Wiegand protocol, also known as Wiegand code, only needs two cables during data transmission. One is DATA0, and the other is DATA1. The protocol stipulates that the two cables are at a high level when there is no data. As shown in Figure 10-83, the DATA0 at a low level represents 0, and the DATA1 at a low level represents 1. (Low level signal is less than 1V, and high level signal is more than 4V) The pulse width ranges are 20us-200us, and the intervals of two pulses are 200us-20ms.

TP is the duration of low level, and TW is the period of low level. Both of them are flexible in a range, among which different devices may have their TP and TW parameter configuration. Therefore, to achieve more reasonable signal detection, this module provides register port for parameter configuration in accordance with peripheral values of TP and TW. Please see the section 10.9.6 Register Description for more details.

Figure 10-83 Data Signal Oscillogram



10.9.3.4 Cautions and Notes

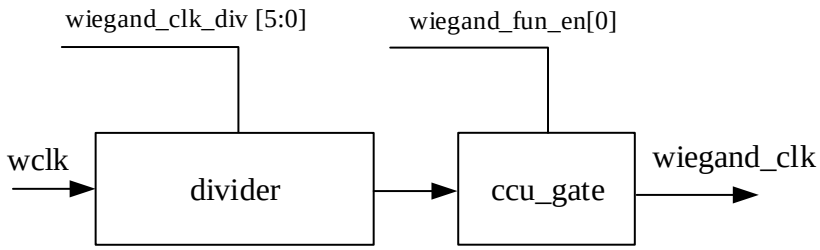
SCLK Clock Frequency Division Configuration

The bit [5:0] of WIEGAND_CLK_DIV register is used for configuring the frequency dividing coefficients. The equation of the frequency-divided WIEGAND_CLK is WIEGAND_CLK= (WCLK) / (WIEGAND_CLK_DIV [5:0]). The output of a frequency divider is controlled by clock gating, and the control signal sources from the data that is written from the APB interface to WIEGAND_FUN_EN register. When CPU configures WIEGAND_FUN_EN register as 1 through the APB bus, the clock gating of frequency divider will be turned on and output the frequency-divided WIEGAND_CLK. The logic diagram of clock gating is shown in Figure 10-84, in which CCU_GATE is the clock logic unit of CCMU library.

This clock divider supports the two frequency divisions at least. If the value of WIEGAND_CLK_DIV is 0 or 1, it equals 2, namely, two frequency divisions. This clock divider supports 48 frequency divisions at most. If the value of WIEGAND_CLK_DIV is larger than 48, it equals 48 frequency divisions. This is because that when the frequency dividing coefficient equals 48, the WCLK before frequency division is 24MHz, and the WIEGAND_CLK after frequency division is 0.5MHz with a period of 2us. As stipulated by Wiegand protocol, the minimum pulse width of Wiegand data is 20us. Therefore, the larger frequency dividing coefficients (more than 48 frequency

divisions) will lead to clock frequencies not enough to collect Wiegand data. Therefore, the value of WIEGAND_CLK_DIV register ranges from 0 to 48.

Figure 10-84 Diagram of WCLK Clock Module



Error Flag of Parity Check

When receiving complete data, the module will conduct internal parity check and read the original parity information received this time by using the WIEGAND_RXC register. If a check error is found when the module checks the received data and parity bit, the corresponding bit of the WIEGAND_CBSR register will be set to 1. The high parity bit and low parity bit respectively corresponds to the CBS_H and CBS_L of WIEGAND_CBSR register.

Timeout Interrupt

As the Wiegand protocol stipulates that the interval of two adjacent data waveforms is 200us-30ms, a timeout interrupt will be triggered if the next waveform beyond this interval isn't detected. This interrupt flag corresponds to the TRIS bit of WIEGAND_ISR register. The threshold of triggering this interrupt is set by the WIEGAND_TW register. When this interrupt is triggered, the module can check the number of receive completion bits and the data value by reading the WIEGAND_TDNR and the WIEGAND_TDR. The interrupt flag can be cleared by writing 1.

Range Setting of TP and TW

The following table is the data in case of WCLK=24MHz.

Table 10-38 Range Setting of WIEGAND_TP Register and WIEGAND_TW Register under different frequency dividing coefficients

Frequency Dividing Coefficients	WIEGAND_CLK	Period	TP Min Value （20us）	TP Max Value (200us)	TW Min Value （200us）	TW Max Value (20ms)
0	12MHz	0.083us	240	2400	2400	240000
1	12MHz	0.083us	240	2400	2400	240000
2	12MHz	0.083us	240	2400	2400	240000
…	…	…	…	…	…	…
24	1MHz	1us	20	200	200	20000
…	…	…	…	…	…	…
48	0.5MHz	2us	10	100	100	10000

10.9.4 Programming Guidelines

10.9.4.1 Initialization Process

1. Reset release, and turn on the clock gating.
2. Configure the IO interface of DATA0 and DATA1 as the input port.
3. Configure the WIEGAND_WMR register to set the format of Wiegand Protocol as 26-bit or 34-bit.
4. Configure the WIEGAND_CLK_DIV register to set the frequency dividing coefficients of internal divided clock. As the frequency of input oscillator clock is 24MHz, it is recommended to set WIEGAND_CLK_DIV as 24 frequency division to get the 1MHz divided clock.
5. Configure WIEGAND_TP register to set the detection time of TP in microseconds (us). The detection counter clock is the 1MHz divided clock. The value of WIEGAND_TP should be smaller than the actual duration of its data pulse.
6. Configure the WIEGAND_TW register to set the detection time of TW in microseconds (us). The detection counter clock is the 1MHz divided clock. The value of WIEGAND_TW should be smaller than the actual period of its data pulse.
7. Configure the WIEGAND_ICR register to set the interrupt enable.
8. Configure the WIEGAND_CBP register to set the detection polarity of parity bit.
9. Configure the WIEGAND_DBP register to set the data polarity of DATA0 and DATA1.
10. After completing the above configurations, configure the WIEGAND_FUN_EN register to enable the WIEGAND_CTRL module.

10.9.4.2 Data Reading Process

1. When the initialization process finishes, the WIEGAND_CTRL module will continuously monitor the varying level of DATA0 and DATA1. When receiving the specified number of bits (26bit or 34bit), the module will trigger the signal of receive completion interrupt and start the parity check.
2. WIEGAND_ISR register is an interrupt flag register. CPU decides the next operations based on the IRQ interrupt signals and the different interrupt flags of WIEGAND_ISR register.
3. WIEGAND_RXD register read data while WIEGAND_RXC register read parity bits. When the format of Wiegand protocol is 26bit, the least significant bit of WIEGAND_RXD register is 24 (not included two check bits). When the format of Wiegand protocol is 34bit, the least significant bit of WIEGAND_RXD register is 32 (not included two check bits).
4. Write 1 to clear the specified bits of WIEGAND_ISR register.

10.9.5 Register List

Module Name	Base Address
WIEGAND_CTRL	0x02020000

Register Name	Offset	Description
WIEGAND_WMR	0x0004	WIEGAND Work Mode Register
WIEGAND_TP	0x0008	WIEGAND TP Control Register
WIEGAND_TW	0x000C	WIEGAND TW Control Register
WIEGAND_CLK_DIV	0x0010	WIEGAND Clock Divide Register
WIEGAND_FUN_EN	0x0014	WIEGAND Function Enable Register
WIEGAND_ICR	0x001C	WIEGAND Interrupt Control Register
WIEGAND_ISR	0x0020	WIEGAND Interrupt Status Register
WIEGAND_CBSR	0x0024	WIEGAND Check Bit Status Register
WIEGAND_CBP	0x0028	WIEGAND Check Bit Polar Register
WIEGAND_DBP	0x002C	WIEGAND Data Bit Polar Register
WIEGAND_DSR	0x0034	WIEGAND Data Status Register
WIEGAND_TDNR	0x0038	WIEGAND Timeout Data Number Register
WIEGAND_TDR	0x003C	WIEGAND Timeout Data Register
WIEGAND_RXD	0x0100	WIEGAND RX DATA Register
WIEGAND_RXC	0x0200	WIEGAND RX CHECK Register

10.9.6 Register Description

10.9.6.1 0x0004 WIEGAND Work Mode Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: WIEGAND_WMR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	WM Work Mode 0: wiegand-26bit 1: wiegand-34bit

10.9.6.2 0x0008 WIEGAND TP Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: WIEGAND_TP
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TPV TP Value Before setting the TP Value, work out its time unit according to the WIEGAND_CLK_DIV. The equation is as below: Unit(TPV) = 1/(WCLK/WIEGAND_CLK_DIV) For example, if the WCLK is 24MHz, and the WIEGAND_CLK_DIV is set to 24. Then, the divided clock frequency will be 1MHz, and the unit of the WIEGAND_TP will be 1/1MHz=1us.

10.9.6.3 0x000C WIEGAND TW Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: WIEGAND_TW
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TWV TW Value Before setting the TW Value, work out its time unit according to the WIEGAND_CLK_DIV. The equation is as below: Unit(TWV) = 1/(WCLK/WIEGAND_CLK_DIV) For example, if the WCLK is 24MHz, and the WIEGAND_CLK_DIV is set to 24, the divided clock frequency will be 1MHz, and the unit of the WIEGAND_TW will be 1/1MHz=1us.

10.9.6.4 0x0010 WIEGAND Clock Divide Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: WIEGAND_CLK_DIV
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/

Offset: 0x0010			Register Name: WIEGAND_CLK_DIV
Bit	**Read/Write**	**Default/Hex**	**Description**
5:0	R/W	0x0	RCD Rate of WCLK divider The actual clock equals the WCLK frequency divided by the value of the WIEGAND_CLK_DIV. For example, if the WCLK is 24MHz, and the register is set to 24, the frequency of divided clock will be 1MHz. **Note:** **(1) The divider does not support one divided-frequency. That means if the value of RCD is set to 0 or 1, it equals 2.** **(2) The upper limit of RCD is 48. That means the frequency divider only supports 2-48 divided frequencies.**

10.9.6.5 0x0014 WIEGAND Function Enable Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: WIEGAND_FUN_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	FUN_EN Function Enable This is used to enable/disable the function module. 0: Disable, the function module will be reset. 1: Enable

10.9.6.6 0x001C WIEGAND Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: WIEGAND_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	TRIE Timeout Report Interrupt Enable This is used to enable/disable the generation of TRIE Interrupt. 0: Disable 1: Enable
0	R/W	0x0	RIE Receive Interrupt Enable This is used to enable/disable the generation of RIE Interrupt. 0: Disable 1: Enable

10.9.6.7 0x0020 WIEGAND Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: WIEGAND_ISR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/.
1	R/W1C	0x0	TRIS Timeout Report Interrupt Status Reads 0: Timeout Report Interrupt is not pending. 1: Timeout Report Interrupt is pending. Writes 0: No Effect. 1: Clear Timeout Report Interrupt status.
0	R/W1C	0x0	RIS Receive Interrupt Status Reads 0: Receive Interrupt is not pending. 1: Receive Interrupt is pending. Writes 0: No Effect. 1: Clear Receive Interrupt status.

10.9.6.8 0x0024 WIEGAND Check Bit Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: WIEGAND_CBSR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/.
1	R	0x0	CBS_H Check the Bit Status of Identification Code This is used to indicate whether the Check Bit Status of Identification Code is right or wrong. 0: Right 1: Wrong
0	R	0x0	CBS_L Check the Bit Status of Group Code This is used to indicate whether the Check Bit Status of Group Code is right or wrong. 0: Right 1: Wrong

10.9.6.9 0x0028 WIEGAND Check Bit Polar Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: WIEGAND_CBP
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/.

Offset: 0x0028			Register Name: WIEGAND_CBP
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	CBP_H Check the Bit Polar of High Check Bit This is used to set the check polar of high bit 0: even check 1: odd check
0	R/W	0x0	CBP_L Check the Bit Polar of Low Check Bit This is used to set the check polar of low bit 0: even check 1: odd check

10.9.6.10 0x002C WIEGAND Data Bit Polar Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: WIEGAND_DBP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/.
0	R/W	0x0	DBP Data Bit Polar This is used to set whether the Data 0 and DATA1 is inversed or not. 0: normal 1: inverse

10.9.6.11 0x0034 WIEGAND Data Status Register (Default Value: 0x0000_0003)

Offset: 0x0034			Register Name: WIEGAND_DSR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/.
1	R	0x1	DS1 DATA1 Status This is used to read the value of DATA1 directly.
0	R	0x1	DS0 DATA0 Status This is used to read the value of DATA0 directly.

10.9.6.12 0x0038 WIEGAND Timeout DATA Number Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: WIEGAND_TDNR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.

Offset: 0x0038			Register Name: WIEGAND_TDNR
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	TDN Timeout Data Number In case of timeout error, TDN indicates the bit number that already received by the serial-to-parallel buffer.

10.9.6.13 0x003C WIEGAND Timeout DATA Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: WIEGAND_TDR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TD Timeout Data In case of timeout error, TD indicates the bit data that already received by the serial-to-parallel buffer. **Note that only bit[31:0] of the serial-to-parallel buffer can be read by the TD.**

10.9.6.14 0x0100 WIEGAND RX DATA Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: WIEGAND_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RD Rx Data The data received from Wiegand interface

10.9.6.15 0x0200 WIEGAND RX Check Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: WIEGAND_RXC
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x0	RCB_H Rx Check bit of Identification Code The high Check bit received from Wiegand interface
0	R	0x0	RCB_L Rx Check bit of Group Code The low Check bit received from Wiegand interface

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11 Security System

11.1 Crypto Engine

11.1.1 Overview

The Crypto Engine (CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RBG algorithms. There are two software interfaces for secure and non-secure world each. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world, and has an internal DMA controller to transfer data between CE and memory. It supports parallel running for symmetric, HASH, asymmetric algorithms.

The CE has the following features:

- Supports symmetrical algorithm for encryption and decryption: AES, XTS-AES, DES, 3DES, SM4
  - Supports ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC, GCM mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports 256/512-bit key for XTS-AES
  - Supports ECB, CBC, CTR, CBC-MAC mode for DES
- Hash Algorithms
  - Support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, SM3
  - Support HMAC-SHA1, HMAC-SHA256
  - Support multi-package[1] mode for these ones
  - Support hardware padding
- Radom bit generate Algorithms
  - Support PRNG, 15 bits seed width, and output with multiple of 5 words
  - Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words
  - Support Instantiate/Reseed/Generate/Uninstantiate 4 process
  - Support prediction resistance requests
  - Support 8 separate suits of Internal State

[1] If not last package, input should be aligned with computation block, namely 512bits or 1024bit

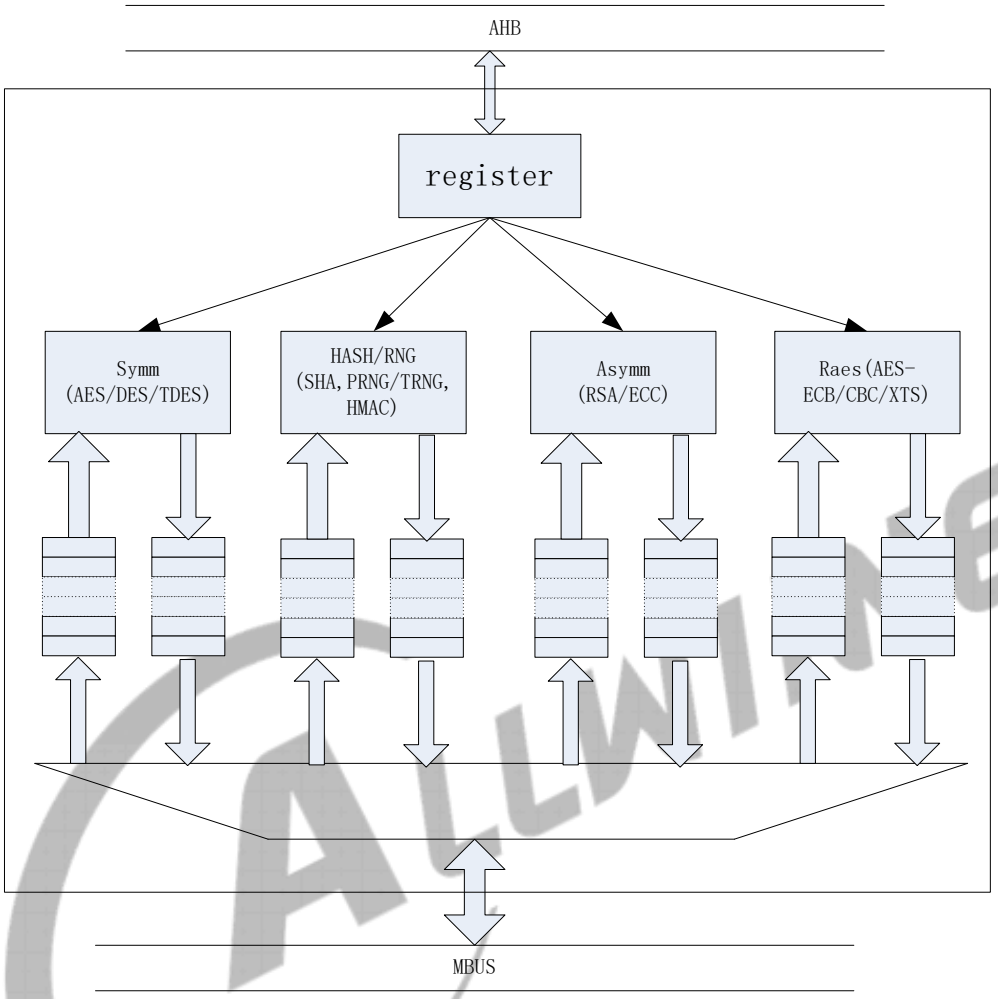
- Maxim 2^32 BYTE length of Entropy input, Nonce, Personalization, Additional input. And length is multiple of word

- Public Key Algorithms
  - Support RSA Public Key Algorithms, include 512/1024/2048/3072/4096 bit width
  - Support ECC Public Key Algorithms, include 160/224/256/384/521 bit width
  - Support SM2 Algorithms
- Security Strategy and System Feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time.
  - Support task chain mode for each request. Task or task chain are executed at request order.
  - 8 scatter group(sg) are supported for both input and output data
  - Support secure and non-secure interfaces respectively, each world issues task request through its own interface, don't know each other's existence.
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other.
  - Supports word-aligned address for all configurations

11.1.2 Block Diagram

The following figure shows a block diagram of CE.

Figure 11-1 CE Block Diagram

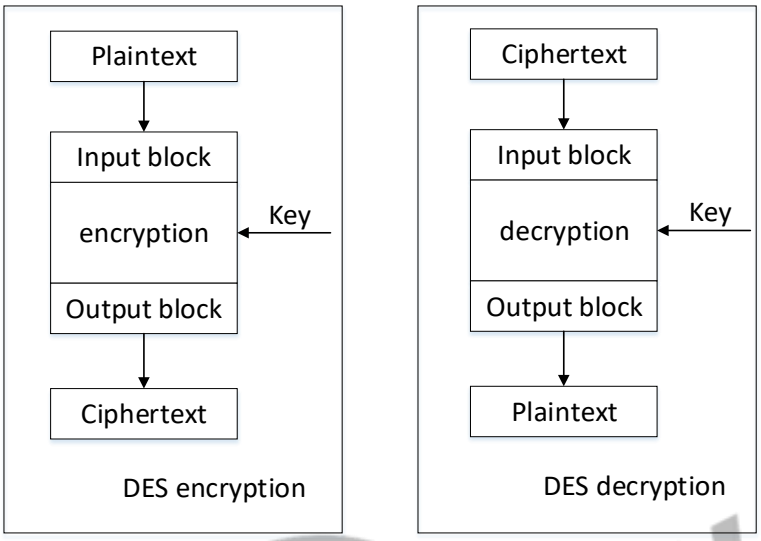


11.1.3 Functional Description

11.1.3.1 DES Algorithm

The following figure shows the DES encryption and decryption operation.

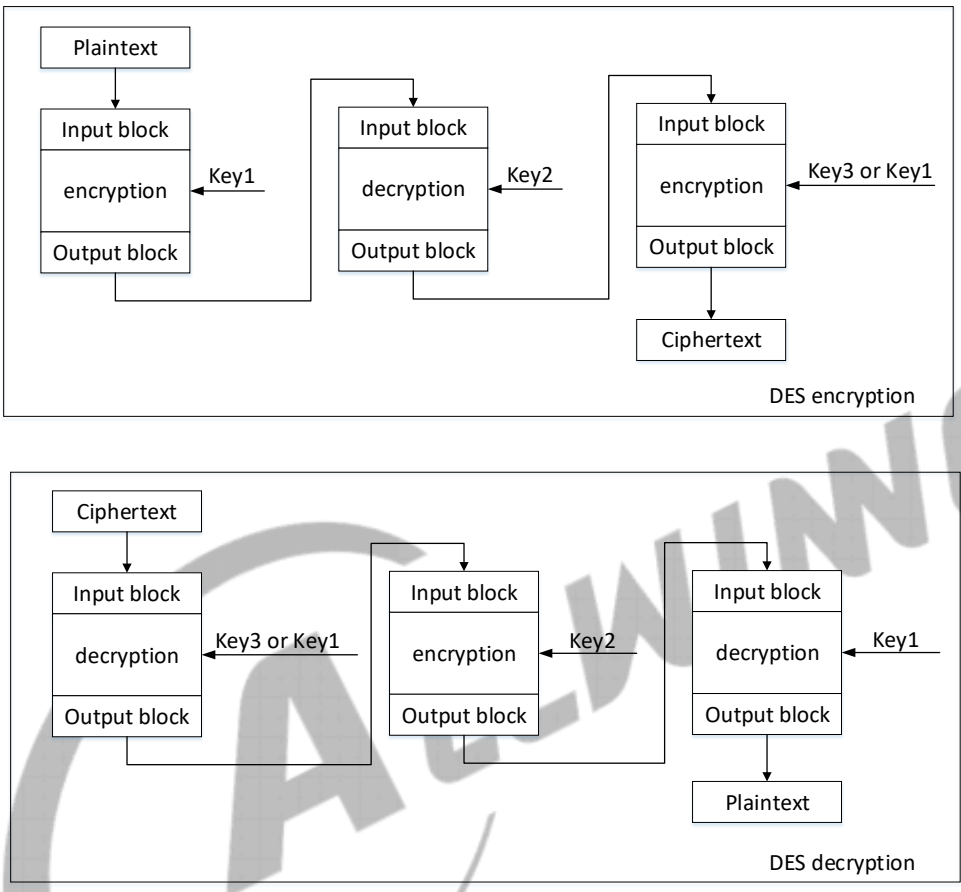
Figure 11-2 DES Encryption and Decryption



11.1.3.2 3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation. The following figure shows the 3DES encryption and decryption operation of a 3-key operation and a 2-key operation.

Figure 11-3 3DES Encryption and Decryption of a 3-key Operation and a 2-key Operation

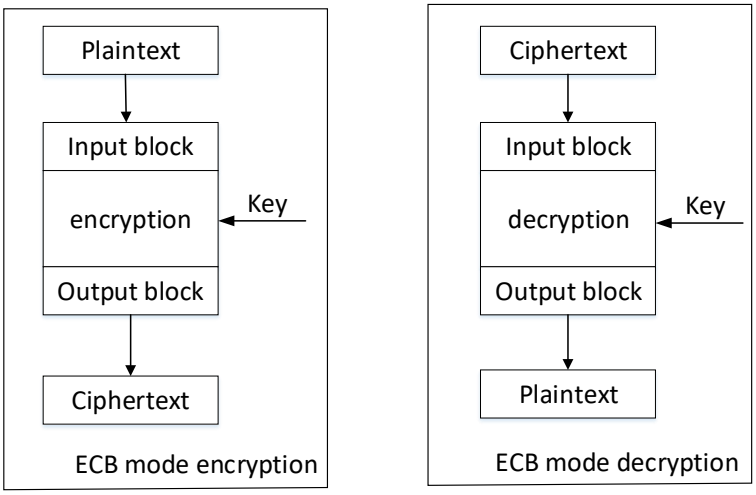


11.1.3.3 ECB Mode

The ECB mode is a confidentiality mode that features, for a given key, the assignment of a fixed ciphertext block to each plaintext block, analogous to the assignment of code words in a codebook.

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent, so the plaintext encryption and ciphertext decryption can be performed concurrently.

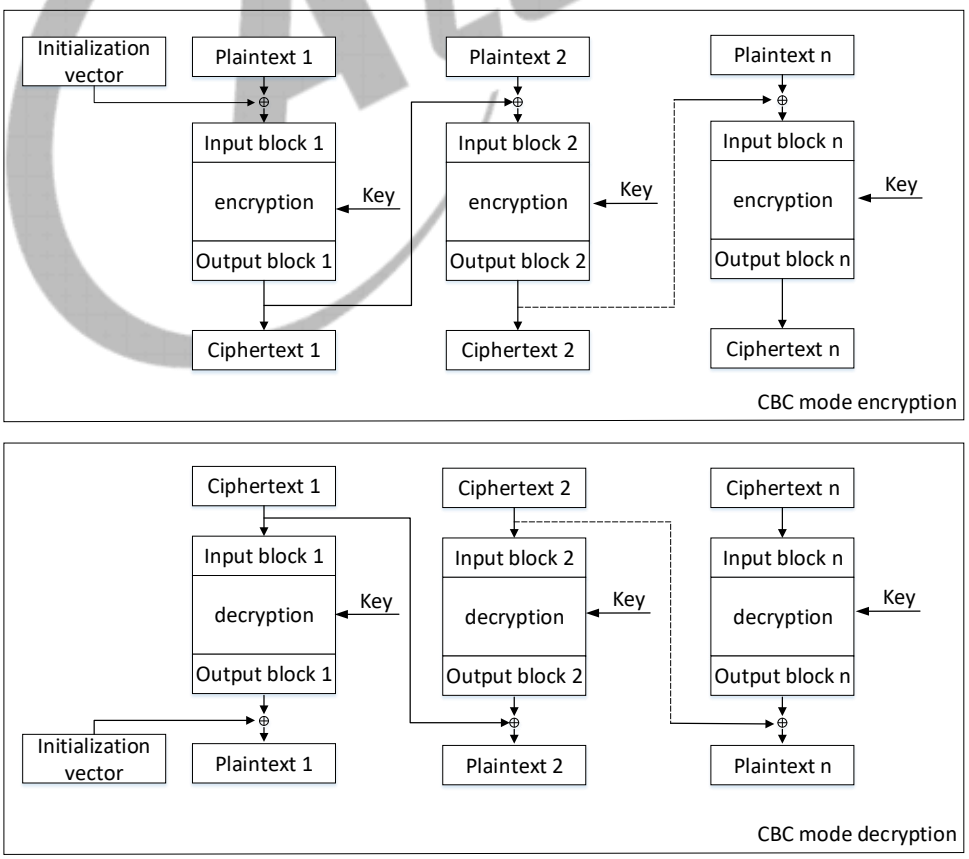
Figure 11-4 ECB Mode Encryption and Decryption



11.1.3.4 CBC Mode

The CBC mode is a confidentiality mode whose encryption process features the combining of the plaintext blocks with the previous ciphertext blocks. The CBC mode requires an initialization vector (IV) to combine with the first plaintext block. The encryption process of each plaintext block is related to the block processing result of the previous ciphertext blocks, so encryption operations cannot be concurrently performed in CBC mode. The decryption operation is independent of output plain text of the previous block, so decryption operations can be performed concurrently.

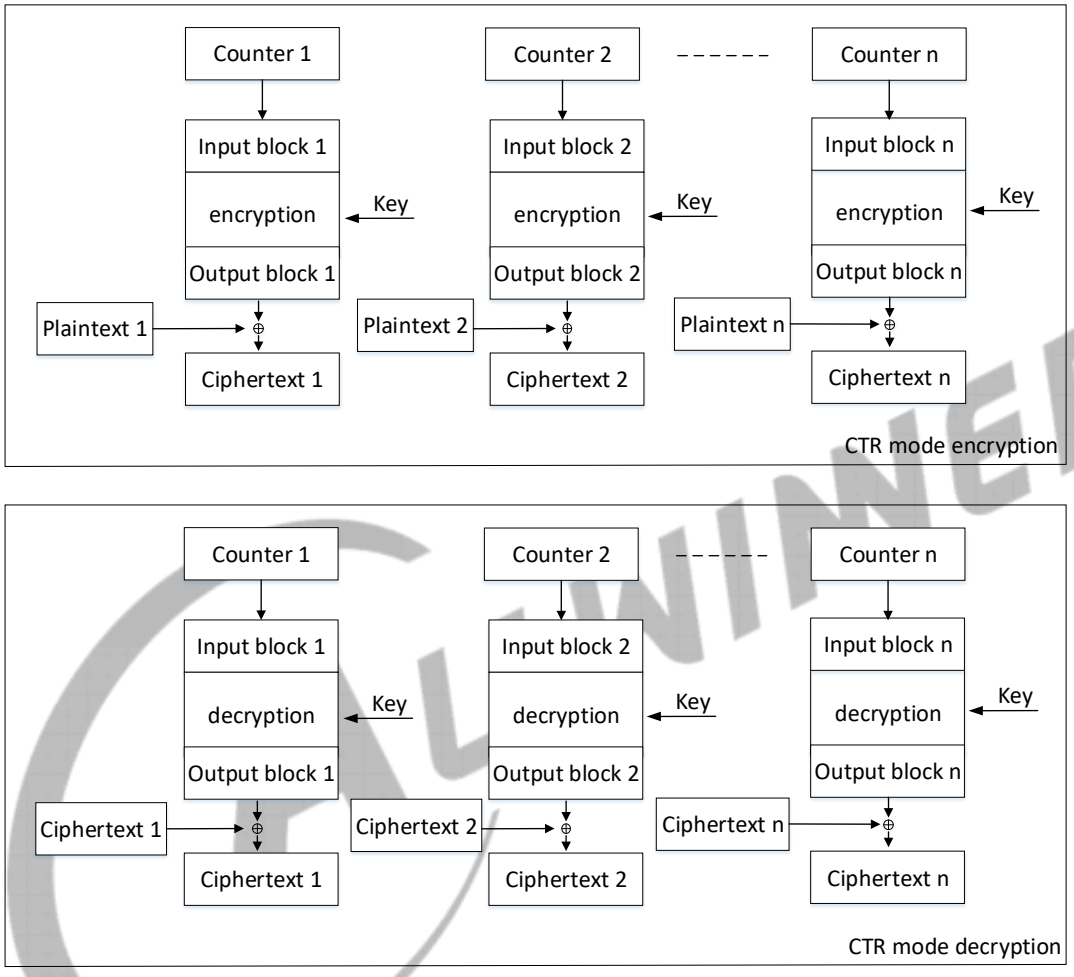
Figure 11-5 CBC Mode Encryption and Decryption



11.1.3.5 CTR Mode

The CTR mode is a confidentiality mode that features the application of the forward cipher to a set of input blocks, called counters, to produce a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. All of the counters must be distinct.

Figure 11-6 CTR Mode Encryption and Decryption

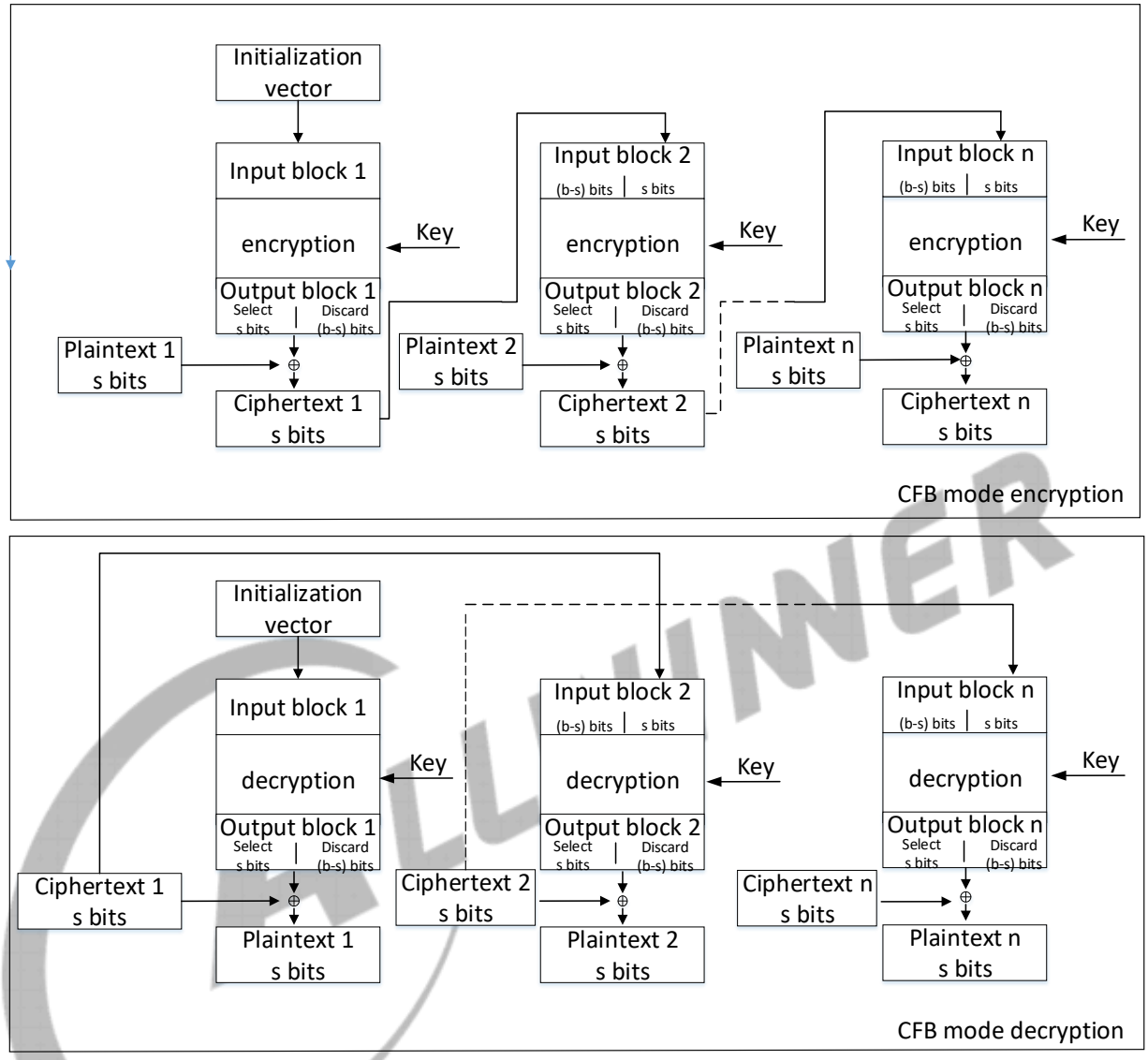


11.1.3.6 CFB Mode

The CFB mode is a confidentiality mode that features the feedback of successive ciphertext segments into the input blocks of the forward cipher to generate output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The CFB mode requires an IV as the initial input block, and the forward cipher operation is applied to the IV to produce the first output block. The first ciphertext segment is produced by exclusive-ORing the first plaintext segment with the s most significant bits of the first output block. The value of s is 1 bit, 8 bits, 64 bits, or 128 bits.

The following figure shows the s-bit CFB mode of the AES algorithms.

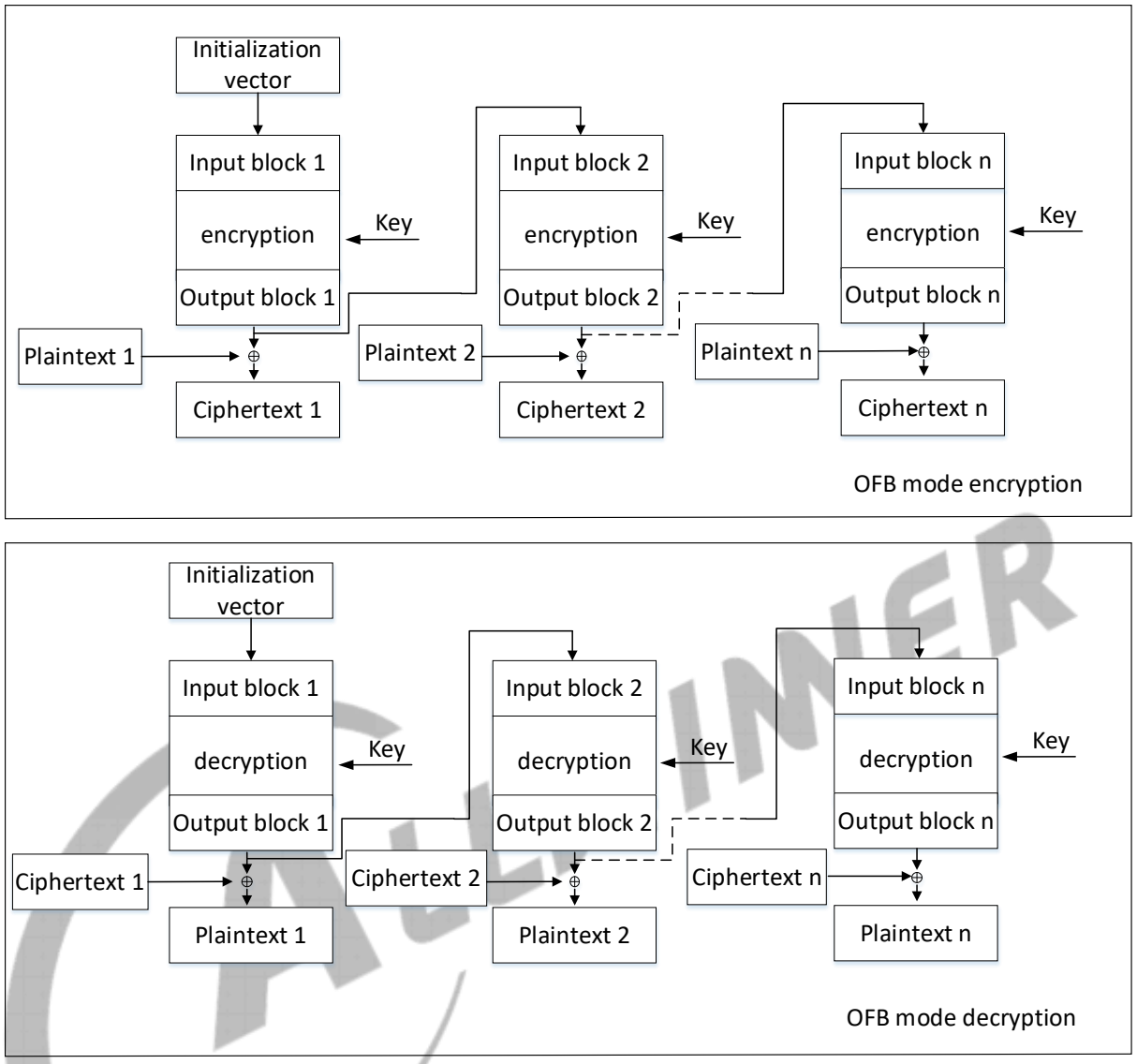
Figure 11-7 CFB Mode Encryption and Decryption



11.1.3.7 OFB Mode

The OFB mode is a confidentiality mode that features the iteration of the forward cipher on an IV to generate a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. If a same key is used, different IVs must be used to ensure operation security.

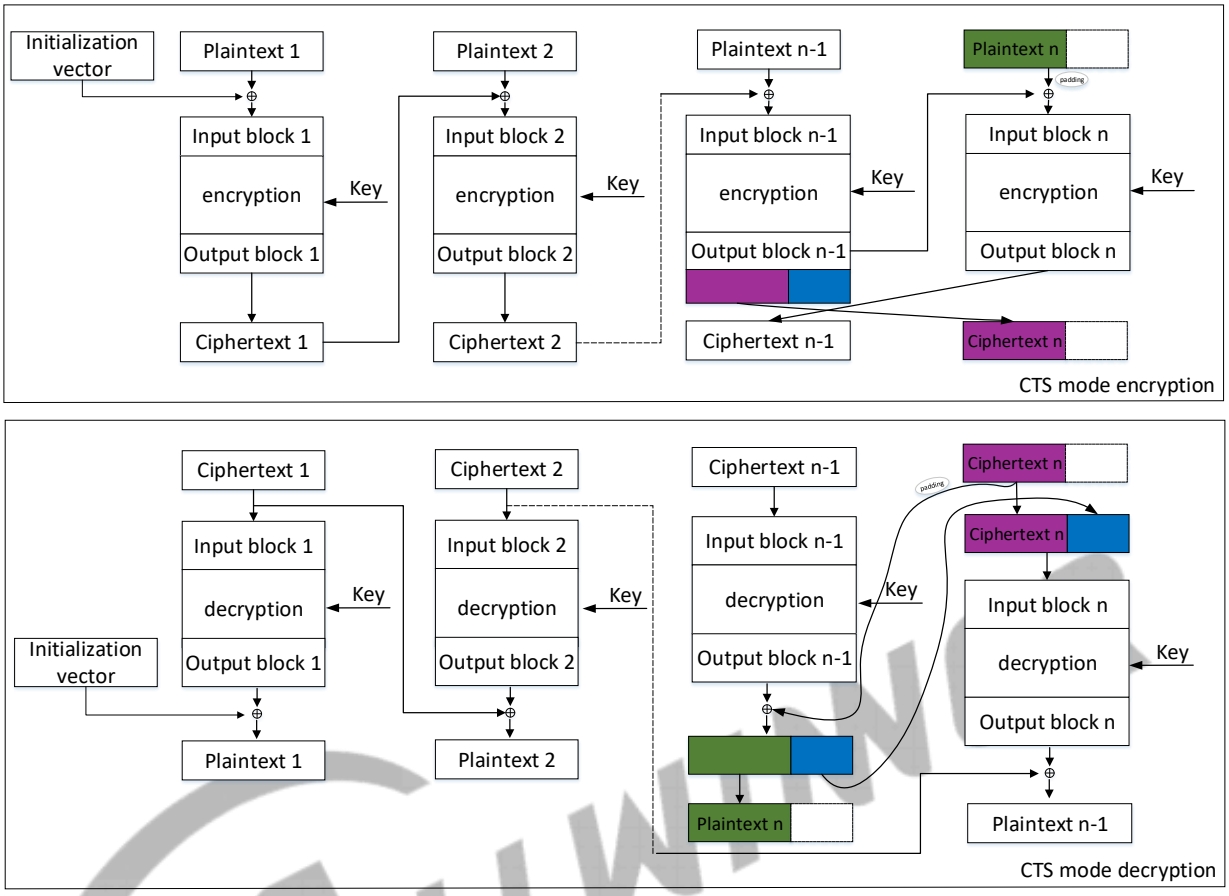
Figure 11-8 OFB Mode Encryption and Decryption



11.1.3.8 CTS Mode

The CTS mode is a confidentiality mode that accepts any plaintext input whose bit length is greater than or equal to the block size but not necessarily a multiple of the block size. Below are the diagrams for CTS encryption and decryption.

Figure 11-9 CTS Mode Encryption and Decryption



11.1.3.9 HASH Algorithm

The hash algorithms support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC-SHA1, and HMAC-SHA256. All algorithms are iterative, one-way hash functions that can process a message to produce a condensed representation called a message digest. When a message is received, the message digest can be used to verify whether the data has changed, that is, to verify its integrity.

The hash algorithm of the CE supports block-aligned total length of the input data (padded by software), that is, a multiple of 64 bytes. The message length after padding by software is used as the configured data length for the hash algorithm.

11.1.3.10 RSA Algorithm

The RSA is a public key encryption/decryption algorithm implemented through the modular exponentiation operation.

The ciphertext is obtained as follows: C = ME mod N. The plaintext is obtained as follows: M = CD mod N.

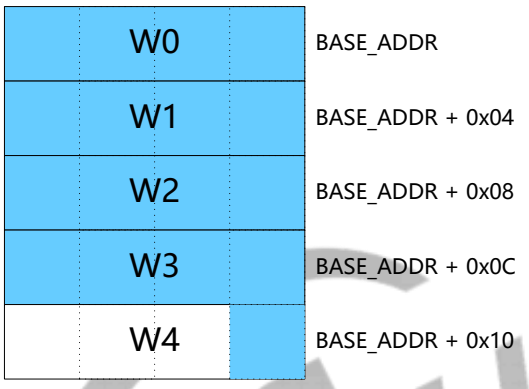
M indicates the plaintext, C indicates the ciphertext, (N, E) indicates the public key, and (N, D) indicates the private key.

11.1.3.11 Storing Message

In the application, a message may not be stored contiguously in the memory, but divided into multiple segments. Or a piece of continuously stored messages can be artificially split into multiple pieces as needs. Then each segment corresponds to a set of the source address and source length in the descriptor. Multiple segments correspond to groups 0-7 source address/source length in sequence.

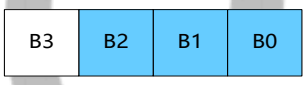
Each task supports up to 8 message segments, and the data volume of each message segment supports up to 4 GWord (AES-CTS is 1 GByte). The total amount of all segments in a task (that is a package) supports up to 4 GWord (AES-CTS is 1 GByte). If a message is divided into multiple packages, all others are required to be whole words; when the last package of AES-CTS is less than one word, 0 needs to be padded, and those less than one word are counted as one word. The following figure shows the address order structure.

Figure 11-10 Word Address of Message



Byte order: low byte first, high byte last. When the data is less than one word, the low byte is filled first. The following figure shows the byte order structure (blue means it is filled by the message).

Figure 11-11 Byte Order



Bit order: high bit first, low bit last. When the data is less than one Byte, the high bit is filled first. The following figure shows the bit order structure.

Figure 11-12 Bit Order

11.1.3.12 Storing Key

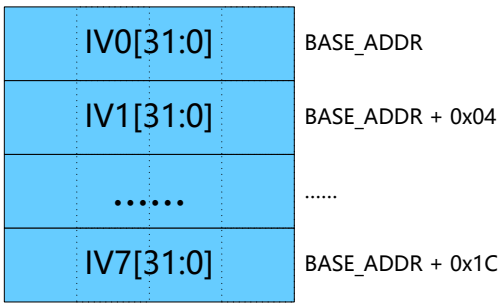
The length of KEY must be an integer multiple of word, refer to section 11.1.3.14 Algorithm Length Properties.

11.1.3.13 Storing IV

For different algorithms, the length of IV is different. But they are integer multiples of word. To keep the byte order of IV and HASH digest output consistent, the byte order of IV is different from that of the message. For the multi-packet operation, the first address of the digest output result of the previous HASH can be directly configured to the first address of the next IV, and the software does not need to do any processing on the digest.

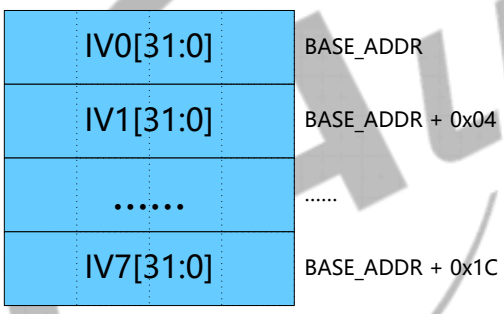
The following figure shows the storage method of 32-bit IV value.

Figure 11-13 The Storage Method of 32-bit IV



The following figure shows the storage method of 64-bit IV value.

Figure 11-14 The Storage Method of 64-bit IV



11.1.3.14 Algorithm Length Properties

The algorithm length has different requirements for different algorithms.

Table 11-1 Symmetric Algorithm Configuration Properties

Algorithm	Length Setting				Alignment	Software Padding
	Source Size	Destination Size	KEY	IV		
AES (except CTS)	< 4 GWord	< 4 GWord	AES-128: 4 Word AES-192: 6 Word AES 256: 8 Word	4 Word	Word-aligned	need
AES-CTS	< 1 GByte	< 1 GByte	AES-128: 4 word AES-192: 6 word AES 256: 8 word	4 Word	Word-aligned	need

Algorithm	Length Setting				Alignment	Software Padding
	Source Size	Destination Size	KEY	IV		
DES	< 4 GWord	< 4 GWord	2 Word	2 Word	Word-aligned	need
TDES	< 4 GWord	< 4 GWord	6 Word	2 Word	Word-aligned	need

Table 11-2 Hash Algorithm Configuration Properties

Algorithm	Length Setting				Alignment	Software Padding
	Source Size	Destination Size	KEY	IV		
MD5	< 4 GWord	4 Word	Fixed to 0	4 Word	Word-aligned	need
SHA-1	< 4 GWord	5 Word	Fixed to 0	5 Word	Word-aligned	need
SHA-224	< 4 GWord	8 Word	Fixed to 0	8 Word	Word-aligned	need
SHA-256	< 4 GWord	8 Word	Fixed to 0	8 Word	Word-aligned	need
SHA-384	< 4 GWord	16 Word	Fixed to 0	16 Word	Word-aligned	need
SHA-512	< 4 GWord	16 Word	Fixed to 0	16 Word	Word-aligned	need
HMAC-SHA1	< 4 GWord	5 Word	16 Word	5 Word	Word-aligned	need
HMAC-SHA256	< 4 GWord	8 Word	16 Word	8 Word	Word-aligned	need

Table 11-3 RNG Configuration Properties

Algorithm	Length Setting				Alignment	Software Padding
	Source Size	Destination Size	KEY	IV		
TRNG	< 4 GWord	< 4 GWord	Fixed to 0	4 Word	Word-aligned	need
PRNG	< 4 GWord	< 4 GWord	6 Word	4 Word	Word-aligned	need

Table 11-4 Asymmetric Algorithm Configuration Properties

Algorithm	Length Setting				Alignment	Software Padding
	Source Size	Destination Size	KEY	IV		
RSA512	16 Word	16 Word	16 Word	Not use IV	Word-aligned	need
RSA1024	32 Word	32 Word	32 Word	Not use IV	Word-aligned	need

Algorithm	Length Setting				Alignment	Software Padding
	Source Size	Destination Size	KEY	IV		
RSA2048	64 Word	64 Word	64 Word	Not use IV	Word-aligned	need

11.1.3.15 Error Detection

The CE module includes error detection for task configuration, data computing error, and authentication invalid. When the algorithm type in task descriptor is read into the CE module, the CE will check whether this type is supported through checking algorithm type field in common control. If the type value is out of scope, the CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting a task descriptor, the input size and output size configuration will be checked to avoid size error. If the size configuration is wrong, the CE will issue interrupt signal and set error state.

11.1.3.16 Clock Requirement

Clock Name	Description	Requirement
AHB_CLK	AHB bus clock	24 MHz ~ 200 MHz
M_CLK	MBUS clock	24 MHz ~ 400 MHz
CE_CLK	CE work clock	24 MHz ~ 400 MHz
OSL_CLK	TRNG sample clock	<3 MHz

11.1.4 Operation Guides

11.1.4.1 Task Descriptor of Hash Algorithms and RBG Algorithms

The task descriptor is data written by software to a contiguous space in memory. The data describes the various properties of a task, such as algorithm type, mode, subcommand, key address, data source address, the data size read from data source, abstract destination address, the written destination data size, and the information of other tasks. First, we configure the task descriptor by software; then we operates the registers of CE to start this task. After the task starts, CE will read task descriptor based on the address of the task descriptor configured in register, and perform the task one time based on the described properties.

In applications, the “NEXT TASK ADDR” field can be configured as the starting address of the next task descriptor, to concatenate multi task descriptors into a task chain. After starting the first task, CE will perform every task in order until the “NEXT TASK ADDR” field is invalid (that is 0).

The HASH/RBG algorithms and Symmetrical/Asymmetrical algorithms use the different descriptor structure, separately.

Figure 11-15 Task Chaining of Hash Algorithms and Random Bit Generator Algorithms

The detail structures are as follows.

No.	Descriptor	Name	Width	Description
0	CTRL	CHN	[1:0]	Channel ID
		IVE	[8]	IV mode enable, active high
		LPKG	[12]	Last package flag, active high
		DLAV	[13]	Data length valid For last package, the bit needs be configured. For non last package, the bit needs not be configured. (Please configure it as 0 in PRNG/TRNG/DRBG.) 1: DLA means the WORD address where data total length (by bits) is saved. 0: DLA means the value of message total length (by bits).
		IE	[16]	Interrupt enable for current task, active high
1	CMD	HASH SEL	[3:0]	Hash algorithms select 0: MD5 1: SHA1 2: SHA224 3: SHA256 4: SHA384 5: SHA512 6: SM3 Other: Reserved
		HME	[4]	HMAC mode enable, active high
		RGB SEL	[11:8]	RGB algorithms select 0: No RGB use 1: PRNG 2: TRNG Other: Reserved
		SUB CMD	[31:16]	Sub-command in a specific algorithms When using PRNG, sub_cmd[15] means PRNG seed reload； sub_cmd[14:0] means PRNG linearly shifted seed
2	DLA	DLA	[31:0]	Data length OR its address. For last package, the field needs be configured. For non last package, the field needs not be configured. (Not used in PRNG/TRNG) When DLAV=1, here is the WORD address where data total length (by bits) is saved. When DLAV=0, here is the value of message total length (by bits)

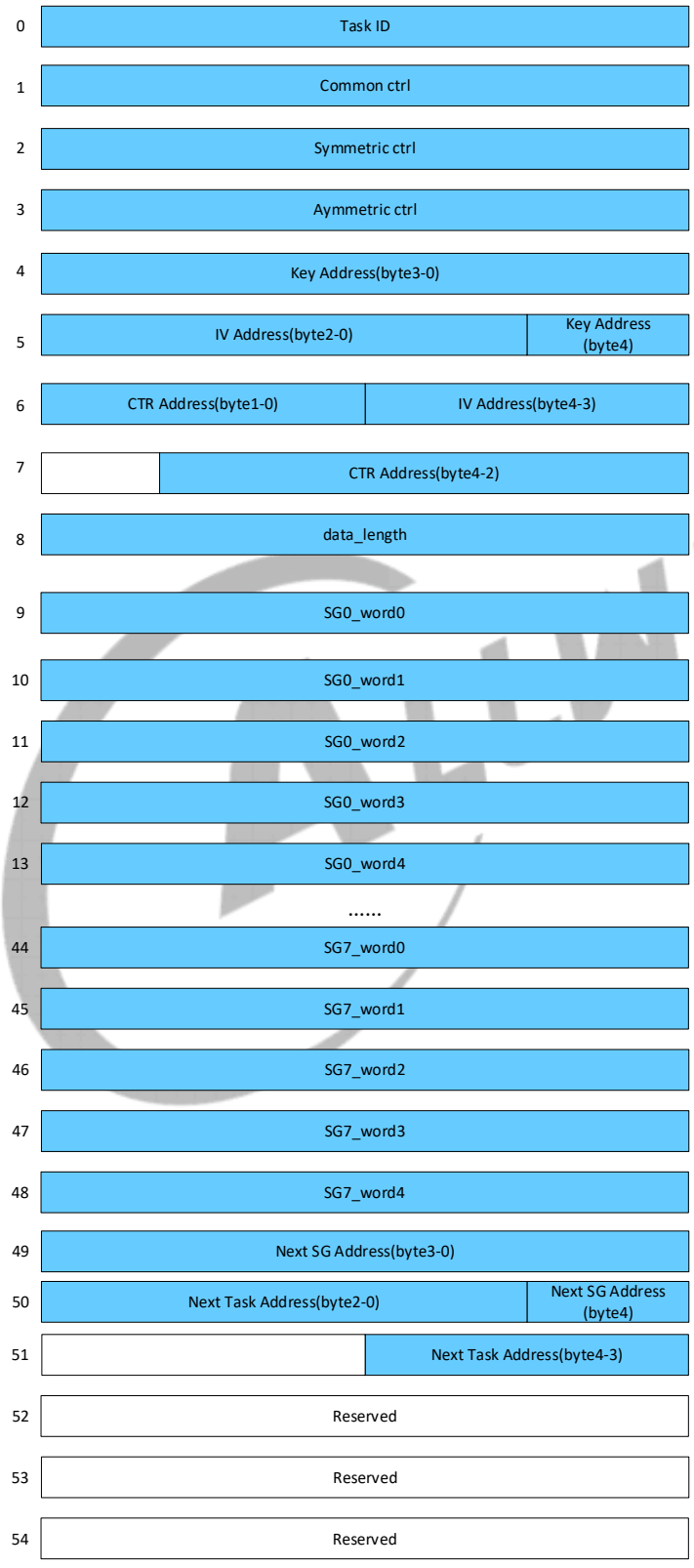
No.	Descriptor	Name	Width	Description
3	DLA	DLA	[7:0]	When DLAV=1, here is the byte address bit[39:32] where data total length (by bits) is saved.
	KA	KA	[31:8]	KEY Address: The byte address bit[23:0].where HMAC KEY or PRNG KEY is saved.
4	KA	KA	[15:0]	KEY Address: The byte address bit[39:24].where HMAC KEY or PRNG KEY is saved.
	IVA	IVA	[31:16]	IV Address: The byte address bit[15:0] where IV is saved.
5	IVA	IVA	[23:0]	IV Address: The byte address bit[39:16] where IV is saved.
	Reversed	Reversed	[31:24]	/
6+5*x	SGx_W0	SGx_WORD0	[31:0]	Source Data Address x: The byte address bit[31:0] where Source Datax is saved.
7+5*x	SGx_W1	SGx_WORD1	[7:0]	Source Data Address x: The byte address bit[39:32] where Source Datax is saved.
			[31:8]	Output Data Address x: The byte address bit[23:0]where Output Datax to be saved.
8+5*x	SGx_W2	SGx_WORD2	[15:0]	Output Data Address x: The byte address bit[39:24]where Output Datax to be saved.
	Reversed	Reversed	[31:16]	/
9+5*x	SGx_W3	SGx_WORD3	[31:0]	Source Data length x: The Length (by bytes) of Source Datax.
10+5*x	SGx_W4	SGx_WORD4	[31:0]	Output Data length x: The Length (by bytes) of output Datax.
46	NSA	NSA	[31:0]	Next SG Address: The byte address bit[31:0].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 32'h0.
47	NSA	NSA	[7:0]	Next SG Address: The byte address bit[39:32].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 8'h0.

No.	Descriptor	Name	Width	Description
	NTA	NTA	[31:8]	Next task Address: The byte address bit[23:0] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 24'h0.
48	NTA	NTA	[7:0]	Next task Address: The byte address bit[39:24] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 16'h0.
	Reversed	Reversed	[31:8]	/
49	Reversed	Reversed	/	/
50	Reversed	Reversed	/	/
51	Reversed	Reversed	/	/

11.1.4.2 Other Algorithms Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination sg address and size, etc. The task descriptor is as follows.

Figure 11-16 CE Block Diagram



Channel id supports 0-3 for each world.

- Common ctrl:

Bit	Read/Write	Default	Description
31	R/W	0	interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:25	/	/	/
24:17	R/W	0	cbc_mac_len the outcome bit length of CBC-MAC when in CBC-MAC mode. The part also be used as gcm/ocb mode tag_len.
16:9	/	/	/
8	R/W	0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0	Algorithm type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x3：SM4 others: reserved 0x20: RSA 0x21: ECC 0x22: SM2 others: reserved 0x30: RAES Others: reserved

- Symmetric ctrl

Bit	Read/Write	Default	Description
31:30	/	/	/
29:28	R/W	0	SCK_SEL 0: use sck0/maskkey0 1: use sck1/maskkey1 2: use sck2/maskkey2 3: reserved

Bit	Read/Write	Default	Description
27	R/W	0	ESCK_EN 0: the process ESCK to SCK not need 1: the process ESCK to SCK need *Anyway, when firstly starting the keyladder as after reset,it will be the process ESCK to SCK whether the bit is 1 or not.When once again ,the process ESCK to SCK will see the bit.
26	R/W	0	no_modk 0: have module key derivation function 1: no module key derivation function
25:24	R/W	0	Key ladder stage 0: no key ladder 1: 3-stage key ladder 2: 5-stage key ladder 3: reserved
23:20	R/W	0	KEY Select key select for AES/SM4/TDES（TDES only configured as 0/8-15） 0: Select input CE_KEYx (Normal Mode) 1: Select {SSK} 2: Select {HUK} 3: Select {RSSK}, used for decrypt HDCP key, EK, BSSK 4-7: Reserved 8-15: Select internal Key n (n from 0 to 7)
19:18	R/W	0	cfb_width For AES-CFB width 0: CFB1 1: CFB8 2: CFB64 3: CFB128
17	/	/	/
16	R/W	0	AES CTS last package flag When set to ‘1’, it means this is the last package for AES-CTS mode(the size of the last package >128bit). The part also be used as gcm/ocb mode gcm_last/ocb_last .
15:14	/	/	/
13	R/W	0	xts_last 0: not last block for XTS 1: last block for XTS
12	R/W	0	xts_first 0: not first block for XTS 1: first block for XTS

Bit	Read/Write	Default	Description
11:8	R/W	0	AES/DES/3DES/RAES modes. DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC/XTS. operation mode for symmetric 0: Electronic Code Book (ECB) mode 1: Cipher Block Chaining (CBC) mode 2: Counter (CTR) mode 3: CipherText Stealing (CTS) mode 4: Output feedback (OFB)mode 5: Cipher feedback (CFB)mode 6: CBC-MAC mode 7:OCB mode 8:GCM mode 9: XTS mode Other: reserved
7:6	/	/	/
5:4	R/W	0	gcm_iv_mode[1:0] gcm_iv_mode[0]:value 1 show the last req for iv calculate gcm_iv_mode[1]: 0 :no GHASH calculate mode 1: GHASH calculate mode gcm_iv_mode[1:0]: 00: IDLE state ,this calculate do not have the process from iv to J0. 01: by iv padding generating J0. On the mode ,iv padding is 96 bits, so iv_length will be 96bits. 10: by GHASH calculate for iv generating J0, and this is not the last req for iv calculate. 11: by GHASH calculate for iv generating J0, and this is the last req for iv calculate
3:2	R/W	0	CTR Width Counter Width for CTR Mode 0: 16-bits Counter 1: 32-bits Counter, gcm mode always use this setting without software 2: 64-bits Counter 3: 128-bits Counter
1:0	R/W	0	AES Key Size 0: 128-bits 1: 192-bits 2: 256-bits 3: Reserved

- Asymmetric ctrl

Bit	Read/Write	Default	Description
31:21	/	/	/
20:16	R/W	0	PKC algorithm mode. For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved For SM2： 00000: encryption 00001: decryption 00010: sign 00011: sign verify 00100: key exchange
15:8	/	/	/
7:0	R/W	0	Asymmetric algorithms operation width field. It indicates how much width this request apply, as words.

key addr field is address for each algorithm's key, also for extension feature micro codes address.(By byte)

iv addr field is tweak value address for XTS.

ctr addr is address for next block's IV. (By byte)

src/dst sgX addr field indicate 40bits address for source and destination data. (By byte)

src/dst sgX size field indicates size for each sg respectively(by byte)

For SG, the detail as flow:

byte3	byte2	byte1	byte0	
SRC_ADDR0 [B3]	SRC_ADDR0 [B2]	SRC_ADDR0 [B1]	SRC_ADDR0 [B0]	SG_WORD0
DST_ADDR0 [B2]	DST_ADDR0 [B1]	DST_ADDR0 [B0]	SRC_ADDR0 [B4]	SG_WORD1
		DST_ADDR0 [B4]	DST_ADDR0 [B3]	SG_WORD2
SRC_SIZE0 [B3]	SRC_SIZE0 [B2]	SRC_SIZE0 [B1]	SRC_SIZE0 [B0]	SG_WORD3
DST_SIZE0 [B3]	DST_SIZE0 [B2]	DST_SIZE0 [B1]	DST_SIZE0 [B0]	SG_WORD4

1 group SG has 8 sg, each sg has 5 words, the ADDR is 40 bits and byte-addr; the SIZE is 32bits nad byte-unit. We will support unlimited SG number,but the 1860 just use for test. This can has many group SG in a task, using the next_sg_addr to create the new SG information in the task.

Next sg field should be set to 0 when no next group sg, else set to next sg's descriptor.

next task field should be set to 0 when no next task, else set to next task's descriptor.

11.1.4.3 Security Operations

CE has two sets of complete registers, the base address of one register is CE_NS, is called non-secure world; the base address of the other register is CS_S, is called secure world. The configurations of two registers are independent each other. The task started by configuring the non-secure world register is called non-secure task; otherwise, called secure task. The difference between secure world and non-secure world has mainly two aspects.

- Non-secure CPU only can access the registers of non-secure world; secure CPU can access the registers of non-secure world and the registers of secure world;
- Non-secure task cannot access any secure domain in system, such as KEYSRAM and SID. But secure task can.

For example, if the EK stored in KEYSRAM needs to do a MD5 operation, the task requires CE to read the EK of KEYSRAM during execution, so it can only access secure-world registers by secure CPU to configure and start the task.

11.1.4.4 Task Parallel

Algorithms are divided into 4 types: symmetric, HASH/RBG, asymmetric, and RAES. These four algorithms can run in parallel. Among these 4 types, the task request and complete time are not sure. If one type uses the outcome of another type, software should make sure to start one type after another type is finished.

Each type has a task queue with 8 elements for requests. Tasks in each queue are handled in sequence. If software makes several requests with the same type, these tasks will be executed in request sequence. If software makes several requests with different types, these tasks will be executed in parallel.

CE supports 4 virtual channels with ID 0-3 in each world. Because parallel tasks would finish out of order, software should make different type request with different channel id, which results in generating different interrupt status bit.

11.1.4.5 PKC Microcode

PKC module supports RSA, ECC, SM2 algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC/SM2 encryption, decryption, sign, verify are implemented with these microcode.

Asymmetric algorithms RSA/ECC/SM2 are implemented as microcode in PKC module. The encryption, decryption, sign, verify operations of asymmetric algorithms are composed with certain fixed microcode with hardware.

11.1.4.6 PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.

For RSA, parameters should be at the order of key, modulus, plaintext.

For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.

For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.

For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.

For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.

For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.

For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

11.1.4.7 Error Check

After CE reads the task descriptor, CE can monitor error during algorithm operation. When the error is monitored, CE will do the following operations:

The task will pause immediately

Generates interrupt

The corresponding channel of the task status register is Fail

The corresponding channel bit of error status register can be read error number

The error number has the following types.

Code	Name	Description	Algorithms Type
0x01	algorithm not support	The algorithm type is not supported.	All
0x11	KEYSRAM access error	In AES decryption task, RSSK is used as plaintext, the DST address is not in KEYSRAM space.	AES decryption
0x21	key ladder configuration error	/	KL
0x31	data length error	Input size or output size configuration size error.	All

11.1.5 Register List

Module Name	Base Address	Comments
CE_NS	0x03040000	Non-Security CE
CE_S	0x03040800	Security CE

Register Name	Offset	Description
CE_NS		
CE_TDA0_NS	0x0000	Non-Security CE Task Descriptor Address0 Register
CE_TDA1_NS	0x0004	Non-Security CE Task Descriptor Address1 Register
CE_ICR_NS	0x0008	Non-Security CE Interrupt Control Register
CE_ISR_NS	0x000C	Non-Security CE Interrupt Status Register
CE_TLR_NS	0x0010	Non-Security CE Task Load Register
CE_TSR_NS	0x0014	Non-Security CE Task Status Register
CE_ESR_NS	0x0018	Non-Security CE Error Status Register
CE_DRL_NS	0x001C	Non-Security CE DRBG Request limit Register
CE_S		
CE_TDA0_S	0x0000	Security CE Task Descriptor Address0 Register
CE_TDA1_S	0x0004	Security CE Task Descriptor Address1 Register
CE_ICR_S	0x0008	Security CE Interrupt Control Register
CE_ISR_S	0x000C	Security CE Interrupt Status Register
CE_TLR_S	0x0010	Security CE Task Load Register
CE_TSR_S	0x0014	Security CE Task Status Register
CE_ESR_S	0x0018	Security CE Error Status Register
CE_DRL_S	0x001C	Security CE DRBG Request limit Register
CE_SCSA0_S	0x0020	Security CE Symmetric algorithm DMA Current Source Address0 Register
CE_SCSA1_S	0x0024	Security CE Symmetric algorithm DMA Current Source Address1 Register
CE_SCDA0_S	0x0028	Security CE Symmetric algorithm DMA Current Destination Address0 Register

Register Name	Offset	Description
CE_SCDA1_S	0x002C	Security CE Symmetric algorithm DMA Current Destination Address1 Register
CE_HCSA0_S	0x0030	Security CE HASH algorithm DMA Current Source Address0 Register
CE_HCSA1_S	0x0034	Security CE HASH algorithm DMA Current Source Address1 Register
CE_HCDA0_S	0x0038	Security CE HASH algorithm DMA Current Destination Address0 Register
CE_HCDA1_S	0x003C	Security CE HASH algorithm DMA Current Destination Address1 Register
CE_ACSA0_S	0x0040	Security CE Asymmetric algorithm DMA Current Source Address0 Register
CE_ACSA1_S	0x0044	Security CE Asymmetric algorithm DMA Current Source Address1 Register
CE_ACDA0_S	0x0048	Security CE Asymmetric algorithm DMA Current Destination Address0 Register
CE_ACDA1_S	0x004C	Security CE Asymmetric algorithm DMA Current Destination Address1 Register
CE_XCSA0_S	0x0050	Security CE XTS algorithm DMA Current Source Address0 Register
CE_XCSA1_S	0x0054	Security CE XTS algorithm DMA Current Source Address1 Register
CE_XCDA0_S	0x0058	Security CE XTS algorithm DMA Current Destination Address0 Register
CE_XCDA1_S	0x005C	Security CE XTS algorithm DMA Current Destination Address1 Register

11.1.6 Register Description

11.1.6.1 0x0000 Non-Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_NS
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_Address0 Task Descriptor Address0 is bit[31:0] (byte address)

11.1.6.2 0x0004 Non-Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_Address1 Task Descriptor Address is bit[39:32] (byte address)

11.1.6.3 0x0008 Non-Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_NS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

Offset: 0x0008			Register Name: CE_ICR_NS
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

11.1.6.4 0x000C Non-Security CE Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR_NS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status: Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status: Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status: Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status: Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

11.1.6.5 0x0010 Non-Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_NS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	TASK_LOAD_RAES Task Load For Channel RAES type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
2	R/W	0x0	TASK_LOAD_ASYM Task Load For Channel ASYM type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
1	R/W	0x0	TASK_LOAD_HR Task Load For Channel HASH/RBG type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
0	R/W	0x0	TASK_LOAD_SYMM Task Load For Channel SYMM type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect

11.1.6.6 0x0014 Non-Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR_NS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

Offset: 0x0014			Register Name: CE_TSR_NS
Bit	Read/Write	Default/Hex	Description
7:6	R	0x0	TASK_CHAN_XTS indicate which channel in run for XTS. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
5:4	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
3:2	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
1:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

11.1.6.7 0x0018 Non-Security CE Error Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	**Read/Write**	**Default/Hex**	**Description**
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved

11.1.6.8 0x001C Non-Security CE DRBG Request Limit Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: CE_DRL_NS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAX_NUM_REQ Maxim number of requests between reseeds in DRBG. **Note: This register can only be configured when there is no DRBG task to be completed.**

11.1.6.9 0x0000 Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_ADDR0 Task Descriptor Address is bit[31:0] (byte address)

11.1.6.10 0x0004 Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_ADDR1 Task Descriptor Address is bit[39:32] (byte address)

11.1.6.11 0x0008 Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_S
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

11.1.6.12 0x000C Security CE Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR_S
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

11.1.6.13 0x0010 Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_S
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	TASK_LOAD_RAES Task Load For Channel RAES type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect

Offset: 0x0010			Register Name: CE_TLR_S
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	TASK_LOAD_ASYM Task Load For Channel ASYM type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
1	R/W	0x0	TASK_LOAD_HR Task Load For Channel HASH/RBG type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect
0	R/W	0x0	TASK_LOAD_SYMM Task Load For Channel SYMM type Read as 1: CE is busy to load another task, or the task queue is full. Write this bit is not allowed now. Read as 0: CE is ready to load another task Write 1: Load task and start to run. Write 0: No effect

11.1.6.14 0x0014 Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR_S
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	TASK_CHAN_XTS indicate which channel in run for XTS. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
5:4	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

Offset: 0x0014			Register Name: CE_TSR_S
Bit	Read/Write	Default/Hex	Description
3:2	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
1:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

11.1.6.15 0x0018 Security CE Error Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved

Offset: 0x0018			Register Name: CE_ESR_S
Bit	Read/Write	Default/Hex	Description
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x31data length error 0x42 DRBG internal state invalid 0x44 DRBG Entropy or Nonce missing 0x46 DRBG do not support Prediction Resistance in current Instantiate other: reserved

11.1.6.16 0x001C Security CE DRBG Request Limit Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: CE_DRL_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	MAX_NUM_REQ Maxim number of requests between reseeds in DRBG. **Note: This register can only be configured after all tasks have been completerd.**

11.1.6.17 0x0020 Security CE Symmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CE_SCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_SRC_ADDR0 Symmetric algorithm current source address DMA reads. Bit[31:0], byte address.

11.1.6.18 0x0024 Security CE Symmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_SRC_ADDR1 Symmetric algorithm current source address DMA reads. Bit[39:32], byte address.

11.1.6.19 0x0028 Security CE Symmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_DST_ADDR0 Symmetric algorithm current destination address DMA writes. Bit[31:0], byte address.

11.1.6.20 0x002C Security CE Symmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_SCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_DST_ADDR1 Symmetric algorithm current destination address DMA writes. Bit[39:32], byte address.

11.1.6.21 0x0030 Security CE HASH algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CE_HCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_SRC_ADDR0 HASH algorithm current source address DMA reads. Bit[31:0], byte address.

11.1.6.22 0x0034 Security CE HASH algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_HCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Offset: 0x0034			Register Name: CE_HCSA1_S
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	HASH_CUR_SRC_ADDR1 HASH algorithm current source address DMA reads. Bit[39:32], byte address.

11.1.6.23 0x0038 Security CE HASH algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_HCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_DST_ADDR0 HASH algorithm current destination address DMA writes. Bit[31:0], byte address.

11.1.6.24 0x003C Security CE HASH algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CE_HCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_DST_ADDR1 HASH algorithm current destination address DMA writes. Bit[39:32], byte address.

11.1.6.25 0x0040 Security CE Asymmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CE_ACSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_SRC_ADDR0 Asymmetric algorithm current source address DMA reads. Bit[31:0], byte address.

11.1.6.26 0x0044 Security CE Asymmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_ACSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

Offset: 0x0044			Register Name: CE_ACSA1_S
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	ASYMM_CUR_SRC_ADDR1 Asymmetric algorithm current source address DMA reads. Bit[39:32], byte address.

11.1.6.27 0x0048 Security CE Asymmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_ACDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_DST_ADDR0 Asymmetric algorithm current destination address DMA writes. Bit[31:0], byte address.

11.1.6.28 0x004C Security CE Asymmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CE_ACDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_DST_ADDR1 Asymmetric algorithm current destination address DMA writes. Bit[39:32], byte address.

11.1.6.29 0x0050 Security CE XTS algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CE_XCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	XTS_CUR_CUR_ADDR0 XTS algorithm current source address DMA reads.

11.1.6.30 0x0054 Security CE XTS algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	XTS_CUR_CUR_ADDR1 XTS algorithm current source address DMA reads.

11.1.6.31 0x0058 Security CE XTS algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA0_S
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	XTS_CUR_DST_ADDR0 XTS algorithm current destination address DMA writes. Bit[31:0], byte address.

11.1.6.32 0x005C Security CE XTS algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: CE_XCDA1_S
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	XTS_CUR_DST_ADDR1 XTS algorithm current destination address DMA writes. Bit[39:32], byte address.

11.2 Security ID

The Security ID (SID) is used to program and read keys which include chip ID, thermal sensor, HASH code, and so on.

The SID module has the following features:

- 2 Kbits electrical fuse (eFuse)
- Backup eFuse information by using SID_SRAM
- A fuse only can program one time
- The module register is non-secure forever, the eFuse has secure zone and non-secure zone

CAUTION

Before performing the burning operation, ensure that the power supply of the eFuse power pin is stable. After the burning operation is completed, cancel the power supply of the eFuse power pin.

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12 Carrier, Storage and Baking Information

12.1 Carrier

12.1.1 Matrix Tray Information

The following table shows the V851S/V851SE matrix tray carrier information.

Table 12-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	260 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

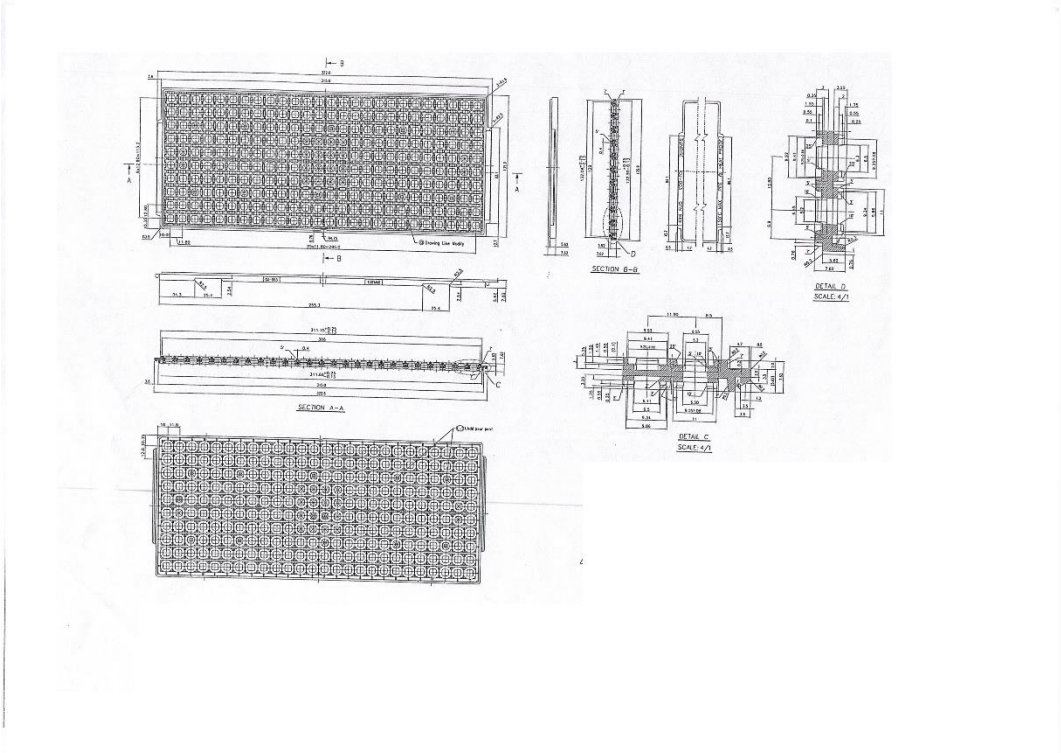
The following table shows the V851S/V851SE packing quantity.

Table 12-2 V851S/V851SE Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V851S/V851SE	9x9	260	10	2600	6	15600

The following figure shows the tray dimension drawing of V851S/V851SE.

Figure 12-1 V851S/V851SE Tray Dimension Drawing



12.2 Storage

The reliability will be affected if any condition specified in the section 12.2.2 and the section 12.2.3 is exceeded.

12.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand the exposure after it is removed from its shipment bag. A low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8 4 defines all MSL.

NOTE

V851S/V851SE device samples are classified as MSL3.

Table 12-3 MSL Summary

MSL	Out-of-bag Floor Life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

12.2.2 Bagged Storage Conditions

The following table defines the shelf life of the V851S/V851SE device samples.

Table 12-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20–26°C
Storage humidity	40%–60%RH
Shelf life	12 months

12.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of V851S/V851SE is as follows.

Table 12-5 Out-of-bag Duration

Storage temperature	20–26°C
Storage humidity	40%–60%RH
Moisture sensitive level (MSL)	3
Floor life	168 hours

For the storage rules not mentioned in this document, refer to the latest ***IPC/JEDEC J-STD-020C***.

12.2.4 Baking

It is not necessary to bake V851S/V851SE if the conditions specified in the section 12.2.2 and the section 12.2.3 have not been exceeded. It is necessary to bake V851S/V851SE if any condition specified in section 12.2.2 and section 12.2.3 has been exceeded.

It is necessary to bake V851S/V851SE if the storage humidity condition has been exceeded. If the device sample is removed from its shipment bag for more than 2 days, it shall be baked to guarantee the production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 time due to a risk of the deformation.

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Figure 13-2 Measuring the Reflow Soldering Process 1162

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Table 13-1 Lead-free Reflow Profile Conditions 1161

13 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is lead-free, it is suitable for the pure lead-free technology of lead-free solder paste. If customers need to use the lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 13-1 Lead-free Reflow Profile

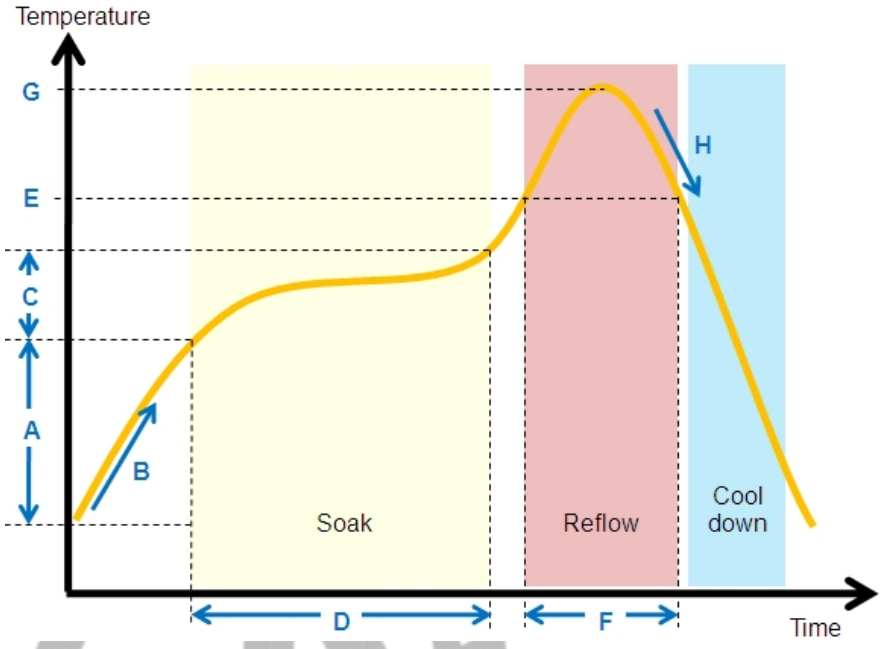


Table 13-1 Lead-free Reflow Profile Conditions

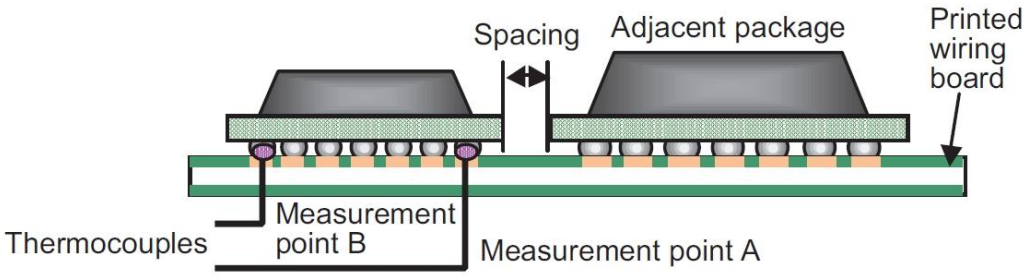
	QTI Typical SMT Reflow Profile Conditions (for Reference Only)	
	Step	**Reflow Condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C/sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80–110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 sec
G	Peak temperature	240–250°C
H	Cool down temperature rate	≤4°C/sec

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using the high-temperature solder wire or the high-

temperature tape. Fix the packaged device at the pad by using the high-temperature tape or other methods, and cover over the thermocouple probe as shown in the following figure

Figure 13-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

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14.1 FT Test 1164

14.2 QA Test 1164

14.3 QC Test 1164

14 FT/QA/QC Test

14.1 FT Test

FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.

14.2 QA Test

QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

14.3 QC Test

QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

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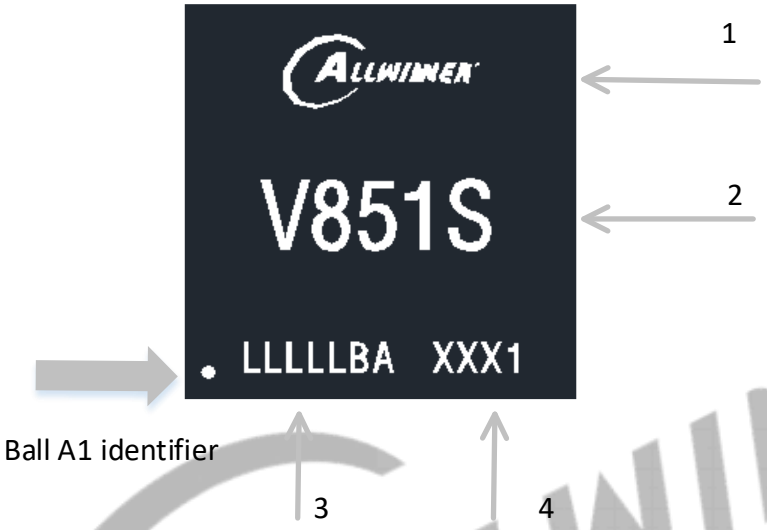
15 Part Marking

15.1 V851S

The following figure shows the V851S marking.

Figure 15-1 V851S Marking



The following figure describes the V851S marking definitions.

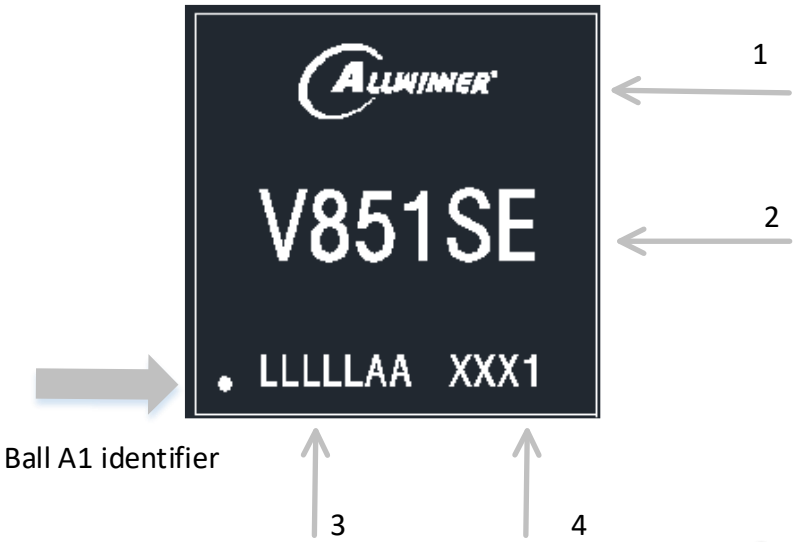
Table 15-1 V851S Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V851S	Product name	Fixed
3	LLLLLBA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

15.2 V851SE

The following figure shows the V851SE marking.

Figure 15-2 V851SE Marking



The following figure describes the V851SE marking definitions.

Table 15-2 V851SE Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V851SE	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

Appendix: Glossary

The following table contains acronyms and abbreviations used in this document.

ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
AWB	Automatic White Balance
BROM	Boot ROM
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FEL	Fireware Exchange Launch
FIFO	First In First Out
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor

JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OSD	On-Screen Display
OTP	One Time Programmable
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Sychronous Dynamic Random Access Memory
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TWI	Two Wire Interface

UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

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