4.2.6 Register Description

4.2.6.1 0x0000 I2S|PCM Control Register (Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S|PCM_CTL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START Only if RX_SYNC_EN set 1, RX_SYNC_EN_START can take effect. Audio Codec / I2S0 / I2S1 / I2S2/I2S3/ DMIC /OWA RX Synchronize Enable Start. 0: Disable 1: Enable
20	R/W	0x0	RX_SYNC_EN I2S RX Synchronize Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x1	BCLK_OUT Bit Clock Direction Select 0: Input 1: Output
17	R/W	0x1	LRCK_OUT LR Clock Direction Select 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	DOUT3_EN Data3 Output Enable 0: Disable, Hi-Z State 1: Enable
10	R/W	0x0	DOUT2_EN Data2 Output Enable 0: Disable, Hi-Z State 1: Enable
9	R/W	0x0	DOUT1_EN Data1 Output Enable 0: Disable, Hi-Z State 1: Enable
8	R/W	0x0	DOUT0_EN Data0 Output Enable 0: Disable, Hi-Z State

Offset: 0x0000			Register Name: I2S|PCM_CTL
Bit	Read/Write	Default/Hex	Description
			1: Enable
7	/	/	/
6	R/W	0x0	DOUT_MUTE_EN Data Output Mute Enable 0: Normal Transfer 1: Force DOUT to Output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 0: PCM Mode offset 0: Long Frame offset 1: Short Frame 1: Left Mode offset 0: LJ Mode offset 1: I2S Mode 2: Right-Justified Mode 3: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When Set '1' , Connecting the DOUT with the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

4.2.6.2 0x0004 I2S|PCM Format Register 0 (Default Value: 0x0000_0033)

Offset: 0x0004			Register Name: I2S|PCM_FMT0
Bit	Read/Write	Default/Hex	Description
31	/	/	/

Offset: 0x0004			Register Name: I2S|PCM_FMT0
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	LRCK_WIDTH (Only Apply in PCM Mode) LRCK Width 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When Apply in I2S / Left-Justified / Right-Justified Mode: 0: Left Channel When LRCK is Low 1: Left Channel When LRCK is High When Apply in PCM Mode: 0: PCM LRCK Asserted at the Negative Edge 1: PCM LRCK Asserted at the Positive Edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM Mode: Number of BCLKs within (Left + Right) channel width. I2S / Left-Justified / Right-Justified Mode: Number of BCLKs within each individual channel width (Left or Right). N+1 For example: N = 7: 8 BCLKs width ... N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY BCLK Polarity Select 0: Normal Mode, DOUT Drive Data at Negative Edge 1: Invert Mode, DOUT Drive Data at Positive Edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit

Offset: 0x0004			Register Name: I2S|PCM_FMT0
Bit	Read/Write	Default/Hex	Description
			111: 32-bit
3	R/W	0x0	EDGE_TRANSFER Edge Transfer 0: DOUT Drive Data and DIN Sample Data at the Different BCLK Edge 1: DOUT Drive Data and DIN Sample Data at the Same BCLK Edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN Sample Data at Positive Edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN Sample Data at Negative Edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN Sample Data at Positive Edge.
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

4.2.6.3 0x0008 I2S|PCM Format Register 1 (Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S|PCM_FMT1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	RX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX_MLS MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width]

Offset: 0x0008			Register Name: I2S|PCM_FMT1
Bit	Read/Write	Default/Hex	Description
			00: Zeros or Audio Gain Padding at LSB Position 01: Sign Extension at MSB Position 10: Reserved 11: Transfer 0 after each Sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits U-law 11: 8-bits A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bits U-law 11: 8-bits A-law

4.2.6.4 0x000C I2S|PCM Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S|PCM_ISTA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Underrun Pending Interrupt Write '1' to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: TXFIFO Overrun Pending Interrupt Write '1' to clear this interrupt.
4	R	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No Pending IRQ 1: TXFIFO Empty Pending Interrupt When Data in TXFIFO are Less than TX Trigger Level
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No Pending Interrupt

Offset: 0x000C			Register Name: I2S|PCM_ISTA
Bit	Read/Write	Default/Hex	Description
			1: RXFIFO Underrun Pending Interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No Pending IRQ 1: RXFIFO Overrun Pending IRQ Write '1' to clear this interrupt.
0	R	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ When Data in RXFIFO are More than RX Trigger Level

4.2.6.5 0x0010 I2S|PCM RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S|PCM_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

4.2.6.6 0x0014 I2S|PCM FIFO Control Register (Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S|PCM_FCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable Only if TXEN set 1, HUB_EN can take effect. Audio Codec / I2S0/ I2S1/ I2S2/ OWA TXFIFO Hub Enable. 0: Disable 1: Enable
30:26	/	/	/
25	R/WAC	0x0	FTX Flush TX FIFO Write '1' to flush TXFIFO, self-clear to '0'.
24	R/WAC	0x0	FRX Flush RX FIFO

Offset: 0x0014			Register Name: I2S|PCM_FCTL
Bit	Read/Write	Default/Hex	Description
			Write '1' to flush RXFIFO, self-clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid Data at the MSB of TXFIFO Register 1: Valid Data at the LSB of TXFIFO Register Example for 20-bits Transmitted Audio Sample: Mode 0: TXFIFO [31:0] = {APB_WDATA [31:12], 12'h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO Register 01: Expanding Received Sample Sign Bit at MSB of RXFIFO Register 10: Truncating Received Samples at High Half-word of RXFIFO Register and Low Half-word of RXFIFO Register is Filled by '0' 11: Truncating Received Samples at Low Half-word of RXFIFO Register and High Half-word of RXFIFO Register is Expanded by Its Sign Bit Example for 20-bits Received Audio Sample: Mode 0: APB_RDATA [31:0] = {RXFIFO [31:12], 12'h0} Mode 1: APB_RDATA [31:0] = {12{RXFIFO [31]}, RXFIFO [31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO [31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

4.2.6.7 0x0018 I2S|PCM FIFO Status Register (Default Value: 0x1080_0080)

Offset: 0x0018			Register Name: I2S|PCM_FSTA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No Room for New Sample in TXFIFO 1: More than One Room for New Sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No Available Data in RXFIFO 1: More than One Sample in RXFIFO (>= 1 Word)
7	R	0x1	PLACE_HOLDER NO Meaning
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

4.2.6.8 0x001C I2S|PCM DMA and Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S|PCM_INT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to '1', an interrupt happens when writing new audio data if TXFIFO is full.

Offset: 0x001C			Register Name: I2S|PCM_INT
Bit	Read/Write	Default/Hex	Description
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When set to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

4.2.6.9 0x0020 I2S|PCM TXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S|PCM_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

4.2.6.10 0x0024 I2S|PCM Clock Divide Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S|PCM_CLKD
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCLKO_EN

Offset: 0x0024			Register Name: I2S|PCM_CLKD
Bit	Read/Write	Default/Hex	Description
			MCLK Out Enable 0: Disable MCLK Output 1: Enable MCLK Output Notes: Whether in Slave or Master mode, when this bit is set to '1', MCLK should be output.
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

4.2.6.11 0x0028 I2S|PCM TX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S|PCM_TXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

4.2.6.12 0x002C I2S|PCM RX Sample Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S|PCM_RXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

4.2.6.13 0x0030 I2S|PCM Channel Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S|PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ TX Slot Value in Half Cycle of BCLK 0: Normal Mode for the Last Half Cycle of BCLK in the Slot 1: Turn to Hi-Z State for the Last Half Cycle of BCLK in the Slot
8	R/W	0x0	TX_STATE The state of transmission line When there is No Transmission

Offset: 0x0030			Register Name: I2S|PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
			0: Transfer Level 0 When Not Transferring Slot 1: Turn to Hi-Z State (TDM) When Not Transferring Slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot Number Which between CPU/DMA and RXFIFO 0: 1 Channel or Slot ... 7: 8 Channels or Slots 8: 9 Channels or Slots ... 15:16 Channels or Slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot Number Which between CPU/DMA and TXFIFO 0: 1 Channel or Slot ... 7: 8 Channels or Slots 8: 9 Channels or Slots ... 15:16 Channels or Slots

4.2.6.14 0x0034 I2S|PCM TX0 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S|PCM_TX0CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX0_OFFSET TX0 offset Tune, TX0 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX0_CHSEL TX0 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX0_CHEN TX0 Channel (Slot) Enable, bit [15:0] Refer to Slot

Offset: 0x0034			Register Name: I2S|PCM_TX0CHSEL
Bit	Read/Write	Default/Hex	Description
			[15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.15 0x0038 I2S|PCM TX1 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: I2S|PCM_TX1CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX1_OFFSET TX1 offset Tune, TX1 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX1_CHSEL TX1 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX1_CHEN TX1 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.16 0x003C I2S|PCM TX2 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: I2S|PCM_TX2CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX2_OFFSET TX2 offset Tune, TX2 Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX2_CHSEL TX2 Channel (Slot) Number Select for each Output

Offset: 0x003C			Register Name: I2S|PCM_TX2CHSEL
Bit	Read/Write	Default/Hex	Description
			0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX2_CHEN TX2 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.17 0x0040 I2S|PCM TX3 Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: I2S|PCM_TX3CHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	TX3_OFFSET TX3 offset Tune, TX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX3_CHSEL TX3 Channel (Slot) Number Select for each Output 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	R/W	0x0	TX3_CHEN TX3 Channel (Slot) Enable, bit [15:0] Refer to Slot [15:0]. When One or More Slot(s) is(are) Disabled, the Affected Slot(s) is(are) Set to Disable State. 0: Disable 1: Enable

4.2.6.18 0x0044 I2S|PCM TX0 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0044	Register Name: I2S|PCM_TX0CHMAP0

Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH15_MAP TX0 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX0_CH14_MAP TX0 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX0_CH13_MAP TX0 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX0_CH12_MAP TX0 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX0_CH11_MAP TX0 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX0_CH10_MAP TX0 Channel 10 Mapping 0: 1st Sample

Offset: 0x0044			Register Name: I2S|PCM_TX0CHMAP0
Bit	Read/Write	Default/Hex	Description
			... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX0_CH9_MAP TX0 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX0_CH8_MAP TX0 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.19 0x0048 I2S|PCM TX0 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S|PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX0_CH7_MAP TX0 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX0_CH6_MAP TX0 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ...

Offset: 0x0048			Register Name: I2S|PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
			15: 16th Sample
23:20	R/W	0x0	TX0_CH5_MAP TX0 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX0_CH4_MAP TX0 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX0_CH3_MAP TX0 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX0_CH2_MAP TX0 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX0_CH1_MAP TX0 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Offset: 0x0048			Register Name: I2S|PCM_TX0CHMAP1
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	TX0_CH0_MAP TX0 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.20 0x004C I2S|PCM TX1 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: I2S|PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX1_CH15_MAP TX1 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX1_CH14_MAP TX1 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX1_CH13_MAP TX1 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX1_CH12_MAP TX1 Channel 12 Mapping 0: 1st Sample ...

Offset: 0x004C			Register Name: I2S|PCM_TX1CHMAP0
Bit	Read/Write	Default/Hex	Description
			7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX1_CH11_MAP TX1 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX1_CH10_MAP TX1 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX1_CH9_MAP TX1 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX1_CH8_MAP TX1 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.21 0x0050 I2S|PCM TX1 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: I2S|PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description

Offset: 0x0050			Register Name: I2S|PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX1_CH7_MAP TX1 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX1_CH6_MAP TX1 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX1_CH5_MAP TX1 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX1_CH4_MAP TX1 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX1_CH3_MAP TX1 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX1_CH2_MAP

Offset: 0x0050			Register Name: I2S|PCM_TX1CHMAP1
Bit	Read/Write	Default/Hex	Description
			TX1 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX1_CH1_MAP TX1 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX1_CH0_MAP TX1 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.22 0x0054 I2S|PCM TX2 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S|PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX2_CH15_MAP TX2 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX2_CH14_MAP TX2 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample

Offset: 0x0054			Register Name: I2S|PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
			8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX2_CH13_MAP TX2 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX2_CH12_MAP TX2 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX2_CH11_MAP TX2 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
11:8	R/W	0x0	TX2_CH10_MAP TX2 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX2_CH9_MAP TX2 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample

Offset: 0x0054			Register Name: I2S|PCM_TX2CHMAP0
Bit	Read/Write	Default/Hex	Description
			... 15: 16th Sample
3:0	R/W	0x0	TX2_CH8_MAP TX2 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.23 0x0058 I2S|PCM TX2 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: I2S|PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX2_CH7_MAP TX2 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX2_CH6_MAP TX2 Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX2_CH5_MAP TX2 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX2_CH4_MAP TX2 Channel 4 Mapping

Offset: 0x0058			Register Name: I2S|PCM_TX2CHMAP1
Bit	Read/Write	Default/Hex	Description
			0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX2_CH3_MAP TX2 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX2_CH2_MAP TX2 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX2_CH1_MAP TX2 Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX2_CH0_MAP TX2 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.24 0x005C I2S|PCM TX3 Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: I2S|PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX3_CH15_MAP TX3 Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX3_CH14_MAP TX3 Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th sample
23:20	R/W	0x0	TX3_CH13_MAP TX3 Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX3_CH12_MAP TX3 Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX3_CH11_MAP TX3 Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ...

Offset: 0x005C			Register Name: I2S|PCM_TX3CHMAP0
Bit	Read/Write	Default/Hex	Description
			15: 16th sample
11:8	R/W	0x0	TX3_CH10_MAP TX3 Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX3_CH9_MAP TX3 Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX3_CH8_MAP TX3 Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.25 0x0060 I2S|PCM TX3 Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: I2S|PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TX3_CH7_MAP TX3 Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
27:24	R/W	0x0	TX3_CH6_MAP TX3 Channel 6 Mapping 0: 1st Sample

Offset: 0x0060			Register Name: I2S|PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
			... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:20	R/W	0x0	TX3_CH5_MAP TX3 Channel 5 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
19:16	R/W	0x0	TX3_CH4_MAP TX3 Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:12	R/W	0x0	TX3_CH3_MAP TX3 Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
11:8	R/W	0x0	TX3_CH2_MAP TX3 Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:4	R/W	0x0	TX3_CH1_MAP TX3 Channel 1 Mapping 0: 1st Sample ...

Offset: 0x0060			Register Name: I2S|PCM_TX3CHMAP1
Bit	Read/Write	Default/Hex	Description
			7: 8th Sample 8: 9th Sample ... 15: 16th Sample
3:0	R/W	0x0	TX3_CH0_MAP TX3 Channel 0 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.26 0x0064 I2S|PCM RX Channel Select Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S|PCM_RXCHSEL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX offset Tune, RX Data offset to LRCK 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0: 1 Channel / Slot ... 7: 8 Channels / Slots 8: 9 Channels / Slots ... 15: 16 Channels / Slots
15:0	/	/	/

4.2.6.27 0x0068 I2S|PCM RX Channel Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S|PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH15_SELECT Rx channel 15 select 00: SDI0

Offset: 0x0068			Register Name: I2S|PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
			01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH14_SELECT Rx channel 14 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH13_SELECT Rx channel 13 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Offset: 0x0068			Register Name: I2S|PCM_RXCHMAP0
Bit	Read/Write	Default/Hex	Description
7:6	/	/	/
5:4	R/W	0x0	RX_CH12_SELECT Rx channel 12 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.28 0x006C I2S|PCM RX Channel Mapping Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S|PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH11_SELECT Rx channel 11 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH10_SELECT Rx channel 10 select 00: SDI0 01: SDI1 10: SDI2

Offset: 0x006C			Register Name: I2S|PCM_RXCHMAP1
Bit	Read/Write	Default/Hex	Description
			11: SDI3
19:16	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH9_SELECT Rx channel 9 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH8_SELECT Rx channel 8 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.29 0x0070 I2S|PCM RX Channel Mapping Register2(Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: I2S|PCM_RXCHMAP2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH7_SELECT Rx channel 7 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
23:22	/	/	/
21:20	R/W	0x0	RX_CH6_SELECT Rx channel 6 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH5_SELECT Rx channel 5 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11: 8	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping

Offset: 0x0070			Register Name: I2S|PCM_RXCHMAP2
Bit	Read/Write	Default/Hex	Description
			0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH4_SELECT Rx channel 4 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.30 0x0074 I2S|PCM RX Channel Mapping Register3(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: I2S|PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	RX_CH3_SELECT Rx channel 4 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
27:24	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample

Offset: 0x0074			Register Name: I2S|PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21:20	R/W	0x0	RX_CH2_SELECT Rx channel 2 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
19:16	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
15:14	/	/	/
13:12	R/W	0x0	RX_CH1_SELECT Rx channel 1 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
11:8	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0: 1st Sample ... 7: 8th Sample 8: 9th Sample ... 15: 16th Sample
7:6	/	/	/
5:4	R/W	0x0	RX_CH0_SELECT Rx channel 0 select 00: SDI0 01: SDI1 10: SDI2 11: SDI3
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0: 1st Sample ...

Offset: 0x0074			Register Name: I2S|PCM_RXCHMAP3
Bit	Read/Write	Default/Hex	Description
			7: 8th Sample 8: 9th Sample ... 15: 16th Sample

4.2.6.31 0x0080 I2S|PCM ASRC MCLK Configure Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: MCLKCFG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	ASRC_MCLK_GATE ASRC Clock Gate Enable 0: Gated 1: Not gated
15:4	/	/	/
3:0	R/W	0x0	ASRC_MCLK_FREQ_DIV_COE Frequency Division Coefficient 4'd0 = Res (no output), 4'd1 = 1x, 4'd2 = 1/2x, 4'd3 = 1/4x, 4'd4 = 1/6x, 4'd5 = 1/8x, 4'd6 = 1/12x, 4'd7 = 1/16x, 4'd8 = 1/24x, 4'd9 = 1/32x, 4'd10 = 1/48, 4'd11 = 1/64x, 4'd12 = 1/96x, 4'd13 = 1/128x, 4'd14 = 1/176x, 4'd15 = 1/192x, others = Res

4.2.6.32 0x0084 I2S|PCM ASRC Out Sample Configure Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: F_{SOUT}CFG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

Offset: 0x0084			Register Name: F_{SOUT}CFG
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	FSOUT_GATE Fsout Clock Gate Enable Control 0: Gated 1: Not gated
19:16	R/W	0x0	FSOUT_CLK_SRC_SEL Fsout Clock Source Select 00: I2S0_ASRC_CLK 01: ACLK 10: ACLKM 11: BCLK Others: Reserved
15:8	/	/	/
7:4	R/W	0x0	FSOUT_CLK_FREQ_DIV_COE1 Fsout Frequency Division Coefficient 1 The First Division Factor It has two levels of frequency division, the first level is bit [7:4], the second level is bit [3:0], and the frequency division factors are multiplied by the two division factors, the division relationship of the two divisions are the same. 4'd0 = Res (no output), 4'd1 = 1x, 4'd2 = 1/2x, 4'd3 = 1/4x, 4'd4 = 1/6x, 4'd5 = 1/8x, 4'd6 = 1/12x, 4'd7 = 1/16x, 4'd8 = 1/24x, 4'd9 = 1/32x, 4'd10 = 1/48, 4'd11 = 1/64x, 4'd12 = 1/96x, 4'd13 = 1/128x, 4'd14 = 1/176x, 4'd15 = 1/192x
3:0	R/W	0x0	FSOUT_CLK_FREQ_DIV_COE2 Fsout Frequency Division Coefficient 2 The Second Division Factor 4'd0 = Res (no output), 4'd1 = 1x,

Offset: 0x0084			Register Name: F_{SOUT}CFG
Bit	Read/Write	Default/Hex	Description
			4'd2 = 1/2x, 4'd3 = 1/4x, 4'd4 = 1/6x, 4'd5 = 1/8x, 4'd6 = 1/12x, 4'd7 = 1/16x, 4'd8 = 1/24x, 4'd9 = 1/32x, 4'd10 = 1/48, 4'd11 = 1/64x, 4'd12 = 1/96x, 4'd13 = 1/128x, 4'd14 = 1/176x, 4'd15 = 1/192x

4.2.6.33 0x0088 I2S|PCM IN Sample Pulse Extend Configure Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: FsinEXTCFG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EXTEND_EN Extend Enable 0: Disabled 1: Enabled Enable the bit when using ASRC.
15:0	R/W	0x0	EXTEND_VALUE Extend value The Cycle Number of Pulse Extend The cycle is BCLK clock and is 1 at least.

4.2.6.34 0x008C I2S|PCM ASRC Enable Configure Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: ASRCEN
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ASRC_EN ASRC Function Enable 0: Disabled 1: Enabled

4.2.6.35 0x0090 I2S|PCM ASRC Manual Configure Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: ASRCMANCFG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ASRC_RATIO_MANUAL_EN Manual Configuration of ASRC Ratio Enable 0: Disabled 1: Enabled
30:26	/	/	/
25:0	R/W	0x0	ASRC_RATIO_VALUE_MANUAL_CFG ASRC Ratio Value Manual Configuration The ratio value is an unsigned 26-bit number and uses 4.22 data format, which means there are 4 bits to the left of the decimal point and 22 bits to the right of the decimal point.

4.2.6.36 0x0094 I2S|PCM ASRC Ratio State Configure Register (Default Value: 0x0040_0000)

Offset: 0x0094			Register Name: ASRCRATIOSTAT
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R	0x0	ASRC_BUF_OVERFLOW_STA ASRC Receive Data Buffer Overflow State It can control the mute with lock. 0: No overflow 1: Overflow
28	R	0x0	ADAPT_COMPUT_LOCK Adaptive Ratio Computational Lock 0: Unlocked 1: Locked
27:26	/	/	/
25:0	R	0x400000	ADAPT_COMPUT_VALUE Adaptive Ratio Computational Value

4.2.6.37 0x0098 I2S|PCM ASRC FIFO State Configure Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: ASRCFIFOSTAT
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0x0	ASRC_RX_FIFO_FULL_LEVAL ASRC RXFIFO Full Level The manually-configured FIFO fill level for the ratio

Offset: 0x0098			Register Name: ASRCFIFOSTAT
Bit	Read/Write	Default/Hex	Description
			value of the received data.

4.2.6.38 0x009C I2S|PCM ASRC MBIST Test Configure Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: ASRCMBISTCFG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	ASRC_RAM_BIST_EN ASRC RAM BIST Enable Enable the RAM BIST.
7:1	/	/	/
0	R/W	0x0	ASRC_ROM_BIST_EN ASRC ROM BIST Enable Enable the ROM BIST.

4.2.6.39 0x00A0 I2S|PCM ASRC MBIST Test State Configure Register (Default Value: 0x0000_0002)

Offset: 0x00A0			Register Name: ASRCMBISTSTA
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R	0x0	ROM_BIST_ERROR_XOR ROM Bist Error Xor
17	R	0x0	ROM_BIST_ERROR_SUM ROM Bist Error Sum
16	R	0x0	ROM_BUSY_STATUS ROM Busy Status 1: ROM busy 0: ROM IDLE
15:8	/	/	/
7	R	0x0	RAM_BIST_ERR_STATUS RAM Bist Error Status 1: Error 0: No Effect
6:4	R	0x0	RAM_BIST_ERROR_PATTERN. RAM Bist Error Pattern.
3:2	R	0x0	RAM_BIST_ERROR_CYCLE RAM Bist Error Cycle.
1	R	0x1	RAM_STOP_STATUS RAM Stop Status 1: Stop

Offset: 0x00A0			Register Name: ASRCMBISTSTA
Bit	Read/Write	Default/Hex	Description
			0: Running
0	R	0x0	RAM_BUSY_STATUS RAM Busy Status 1: RAM busy 0: RAM IDLE.

4.3 DMIC

4.3.1 Overview

The DMIC controller supports one 8-channel digital microphone interface and can output 128 fs or 64 fs (fs = ADC sample rate).

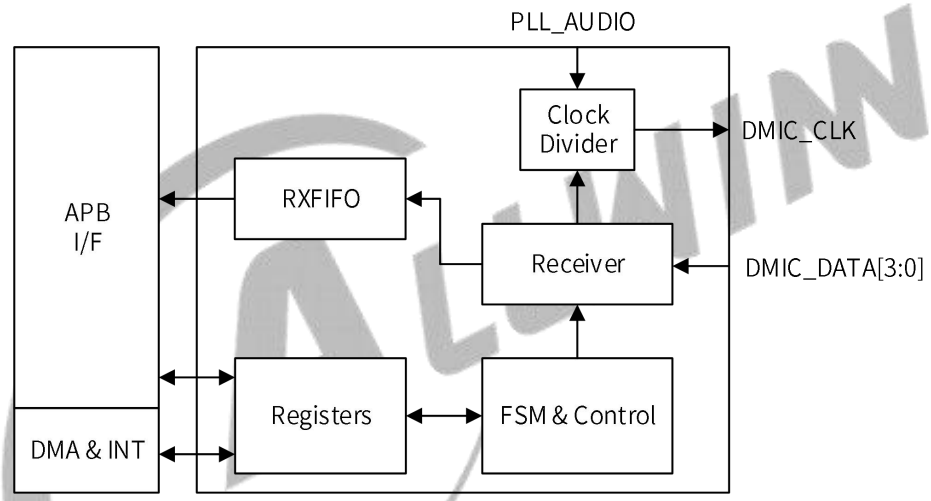
The DMIC controller includes the following features:

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

4.3.2 Block Diagram

The following figure shows a block diagram of the DMIC.

Figure 4-24 DMIC Block Diagram



4.3.3 Functional Description

4.3.3.1 External Signals

The following table describes the external signals of DMIC.

Table 4-5 DMIC External Signals

Signal Name	Description	Type
DMIC-DATA[3:0]	Digital Microphone Data Input	I
DMIC-CLK	Digital Microphone Clock Output	O

4.3.3.2 Clock Sources

The following table describes the clock source for DMIC. For clock setting, configurations, and gating information, refer to section 2.11 Power Reset Clock Management (PRCM).

Table 4-6 DMIC Clock Sources

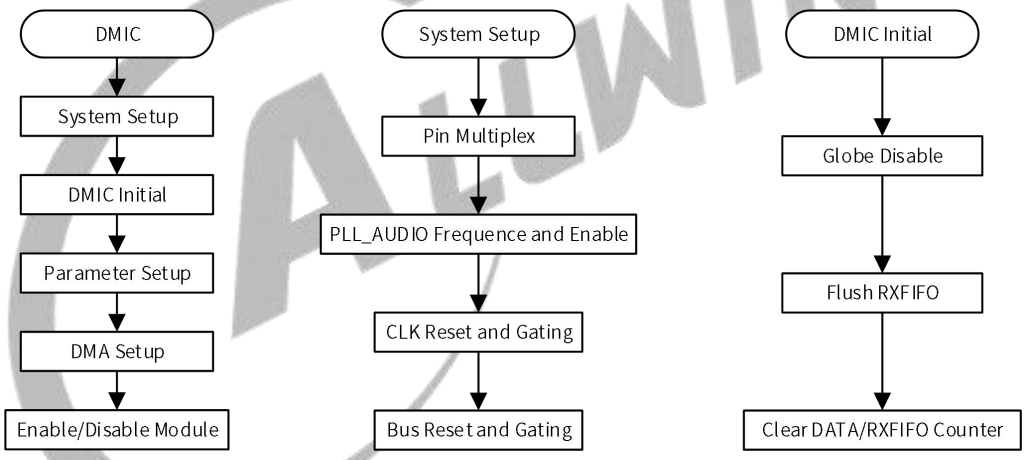
Clock Source	Description	Module
PLL_AUODIO(4x)	By default, PLL_AUDIO(4X) is 98.2856 MHz.	CCU
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz, and PLL_AUDIO1(DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1(DIV5)		

4.3.3.3 Operation Mode

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, channel setup, DMA setup, and Enable/Disable module.

The following figure shows the flow chart of the whole operation, the system setup, and the DMIC initialization.

Figure 4-25 DMIC Operation Mode



Step 1 System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO because the DMIC port is a multiplex pin. For functions of the multiplex pins, refer to section 8.5 GPIO.

Perform the following steps for the clock source. Firstly, disable the PLL_AUDIO through PLL_AUDIOx Control Register[PLL_ENABLE]. Secondly, set up the frequency of the PLL_AUDIO in PLL_AUDIOx Control Register. Then enable PLL_AUDIO. After that, enable the DMIC gating through DMIC_CLK_REG when you checkout that the LOCK bit of PLL_AUDIOx Control Register becomes 1. At last, reset and enable the DMIC bus gating by DMIC_BGR_REG.

After the system setup, the register of DMIC can be setup. Firstly, initialize the DMIC. You should close the globe enable bit (DMIC_EN[8]), data channel enable bit (DMIC_EN[7:0]) by writing 0 to it. After that, flush the RXFIFO by writing 1 to DMIC_RXFIFO_CTR[31]. At last, you can clear the Data/RXFIFO counter by writing 1 to DMIC_RXFIFO_STA, DMIC_CNT.

Step 2 Parameter Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over-sample rate, the channel number, the RXFIFO output mode, the RXFIFO trigger level, and so on. The setup of the register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in section 2.6 DMA Controller (DMAC). In this module, you just enable the DRQ.

Step 3 Enable and Disable DMIC

To enable the function, you can enable the data channel enable bit (DMIC_EN[7:0]) by writing 1 to it. After that, enable DMIC by writing 1 to the Globe Enable bit (DMIC_EN[8]). Write 0 to DMIC_EN[8] to disable DMIC

4.3.4 Register List

Module Name	Base Address
DMIC	0x0711 1000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_DATA	0x0010	DMIC DATA Register
DMIC_INTC	0x0014	DMIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register
DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	DATA0 And DATA1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	DATA2 And DATA3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register
DMIC_REV	0x0050	DMIC Revision Register

4.3.5 Register Description

4.3.5.1 0x0000 DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	RX_SYNC_EN_START Audio Subsys RX Synchronize Enable Start Includes Audio Codec/I2S0/I2S1/I2S2/I2S3/DMIC/OWA. The bit takes effect only when RX_SYNC_EN is set to 1. 0: Disabled 1: Enabled
28	R/W	0x0	RX_SYNC_EN DMIC RX Synchronize Enable 0: Disabled 1: Enabled
27:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disabled 1: Enabled
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel Enable 0: Disabled 1: Enabled
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disabled 1: Enabled
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel Enable 0: Disabled 1: Enabled
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disabled 1: Enabled
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel Enable 0: Disabled 1: Enabled

Offset: 0x0000			Register Name: DMIC_EN
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disabled 1: Enabled
1	R/W	0x0	DATA0_CHR_EN DATA0 Right Channel Enable 0: Disabled 1: Enabled
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disabled 1: Enabled

4.3.5.2 0x0004 DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

4.3.5.3 0x0008 DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5 ms

Offset: 0x0008			Register Name: DMIC_CTR
Bit	Read/Write	Default/Hex	Description
			01: 10 ms 10: 20 ms 11: 30 ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disabled 1: Enabled
7	R/W	0x0	DATA3 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
6	R/W	0x0	DATA2 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
5	R/W	0x0	DATA1 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
4	R/W	0x0	DATA0 Left Data and Right Data Swap Enable 0: Disabled 1: Enabled
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Supports 8 kHz to 24 kHz) 1: 64 (Supports 16 kHz to 48 kHz)

4.3.5.4 0x0010 DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMIC_DATA

4.3.5.5 0x0014 DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disabled 1: Enabled

Offset: 0x0014			Register Name: DMIC_INTC
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disabled 1: Enabled
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disabled 1: Enabled

4.3.5.6 0x0018 DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DMIC_INTS
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing '1' to clear this interrupt or automatically clear if the interrupt condition fails.
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing '1' to clear this interrupt or automatically clear if the interrupt condition fails.

4.3.5.7 0x001C DMIC RXFIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing '1' to flush RXFIFO, self-clear to '0'
30:10	/	/	/
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register

Offset: 0x001C			Register Name: DMIC_RXFIFO_CTR
Bit	Read/Write	Default/Hex	Description
			For 24-bit received audio sample: Mode 0: RXDATA [31:0] = {RXFIFO_O [20:0], 11'h0} Mode 1: RXDATA [31:0] = {8{RXFIFO_O [20]}, RXFIFO_O [20:0], 3'h0} For 16-bit received audio sample: Mode 0: RXDATA [31:0] = {RXFIFO_O [20:5], 16'h0} Mode 1: RXDATA[31:0] = {16{RXFIFO_O[20]}, RXFIFO_O[20:5]}
8	R/W	0x0	Sample Resolution 0: 16-bit 1: 24- bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV [7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV [7:0]) WLEVEL represents the number of valid samples in the DMIC RXFIFO

4.3.5.8 0x0020 DMIC RXFIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R	0x1	Reserved
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

4.3.5.9 0x0024 DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC enable channel numbers are (N + 1).

4.3.5.10 0x0028 DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028	Register Name: DMIC_CH_MAP

Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping 0000: DATA0 Left Channel

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	Read/Write	Default/Hex	Description
			0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

4.3.5.11 0x002C DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C	Register Name: DMIC_CNT

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMIC_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is read by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After being updated by the initial value, the counter register should count on the base of this initial value. Note: It is used for Audio/Video Synchronization.

4.3.5.12 0x0030 DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xA0	DATA1L_VOL Data1 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL Data1 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA0L_VOL Data0 Left Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	Read/Write	Default/Hex	Description
			... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL Data0 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

4.3.5.13 0x0034 DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xA0	DATA3L_VOL Data3 Light Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA3R_VOL Data3 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	Read/Write	Default/Hex	Description
			0xA1: 0.75 dB ... 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA2L_VOL Data2 Light Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL Data2 Right Channel Volume Control (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB ... 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ... 0xFF: 71.25 dB

4.3.5.14 0x0038 High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	HPF_DATA3_CHR_EN High Pass Filter DATA3 Right Channel Enable 0: Disabled 1: Enabled
6	R/W	0x0	HPF_DATA3_CHL_EN High Pass Filter DATA3 Left Channel Enable 0: Disabled 1: Enabled
5	R/W	0x0	HPF_DATA2_CHR_EN High Pass Filter DATA2 Right Channel Enable

Offset: 0x0038			Register Name: HPF_EN_CTR
Bit	Read/Write	Default/Hex	Description
			0: Disabled 1: Enabled
4	R/W	0x0	HPF_DATA2_CHL_EN High Pass Filter DATA2 Left Channel Enable 0: Disabled 1: Enabled
3	R/W	0x0	HPF_DATA1_CHR_EN High Pass Filter DATA1 Right Channel Enable 0: Disabled 1: Enabled
2	R/W	0x0	HPF_DATA1_CHL_EN High Pass Filter DATA1 Left Channel Enable 0: Disabled 1: Enabled
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disabled 1: Enabled
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disabled 1: Enabled

4.3.5.15 0x003C High Pass Filter Coefficient Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			Register Name: HPF_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00FFAA45	HPF_COE High Pass Filter Coefficient

4.3.5.16 0x0040 High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			Register Name: HPF_GAIN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00FFD522	HPF_GAIN High Pass Filter Gain

4.4 One Wire Audio (OWA)

4.4.1 Overview

The One Wire Audio (OWA) provides a serial bus interface for audio data. This interface is widely used for consumer audio.

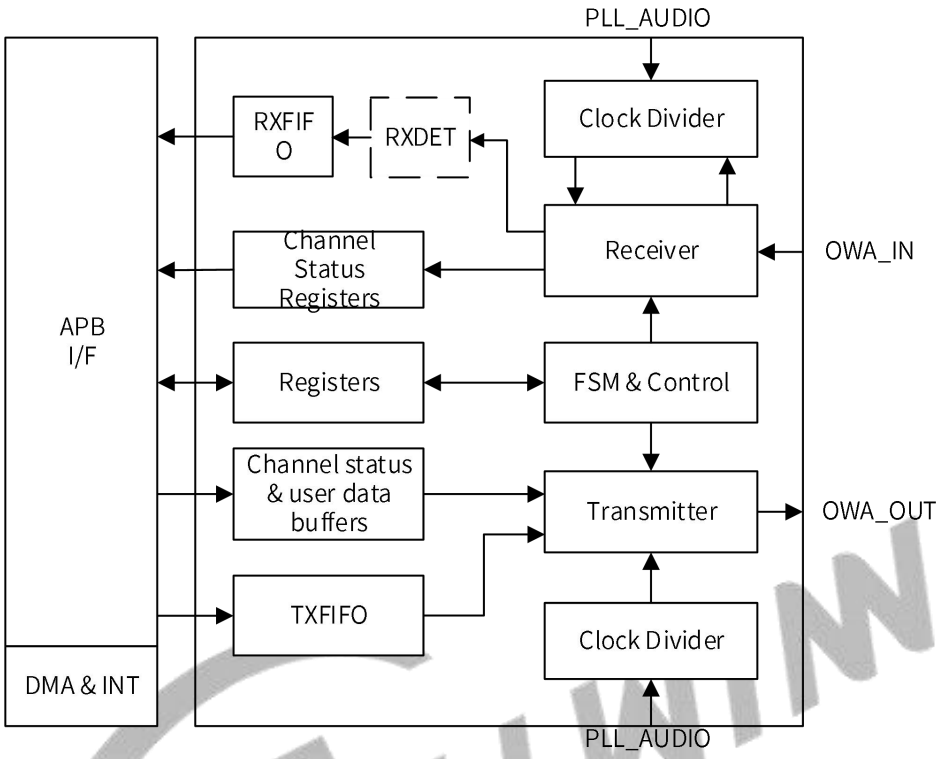
The OWA includes the following features:

- One OWA TX and One OWA RX
- Compliance with S/PDIF interface
- IEC-60958 and IEC-61937 transmitter and receiver functionality
- IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- TXFIFO and RXFIFO
  - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer
  - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Multiple function clock
  - Separate clock for OWA TX and OWA RX
  - The clock of TX function includes 24.576 MHz and 22.5792 MHz
  - The clock of RX function includes 24.576*8 MHz
- Supports hardware parity on TX/RX
  - Hardware parity generation on the transmitter
  - Hardware parity checking on the receiver
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter

4.4.2 Block Diagram

The following figure shows the OWA block diagram.

Figure 4-26 OWA Block Diagram



OWA contains the following sub-blocks:

Table 4-7 OWA Sub-blocks

Sub-block	Description
Registers	Analyze the configuration parameter, DMA requests, and IRQ feedbacks.
Receiver	Parses the frame header and receives the data.
Transmitter	Sends the data
FSM	Finite state machine
Clock Divider	Clock divider circuit

4.4.3 Functional Description

4.4.3.1 External Signals

The OWA is a Biphasic-Mark Encoding Digital Audio Transfer protocol. In this protocol, the CLK signal and data signal are transferred in the same line. The following table describes the external signals of OWA. OWA-OUT is the output pin for the output CLK and DATA, and OWA-IN is the input pin for the input CLK and DATA.

Table 4-8 OWA External Signals

Signal Name	Description	Type
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O

4.4.3.2 Clock Sources

The OWA has separate clock for OWA_TX and OWA_RX. The following tables describe the clock sources for OWA_TX and OWA_RX. For clock setting, configurations and gating information, refer to section 2.11 Power Reset Clock Management (PRCM).

Table 4-9 OWA_TX Clock Sources

Clock Sources	Description	Module
PLL_AUODIO(4x)	By default, PLL_AUDIO(4X) is 98.2856 MHz.	CCU
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz, and PLL_AUDIO1(DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1(DIV5)		

Table 4-10 OWA_RX Clock Sources

Clock Sources	Description	Module
PERI0_300M	By default, PERI0_300M is 300 MHz.	CCU
PLL_AUDIO1(DIV2)	By default, PLL_AUDIO1 is 3072 MHz, PLL_AUDIO1(DIV2) is 1536 MHz, and PLL_AUDIO1(DIV5) is 614.4 MHz (24.576 MHz*25).	PRCM
PLL_AUDIO1(DIV5)		

4.4.3.3 Biphase-Mark Code (BMC)

In the OWA format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal—the data pin. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin. The following figure and table show how data is encoded to the BMC format.

The frequency of the clock is twice the data bit rate, as shown in the following figure. Also, the clock is always programmed to 128 x fs, where fs is the sample rate. The device receiving in the OWA format can recover the clock and frame information from the BMC signal.

Figure 4-27 OWA Biphase-Mark Code

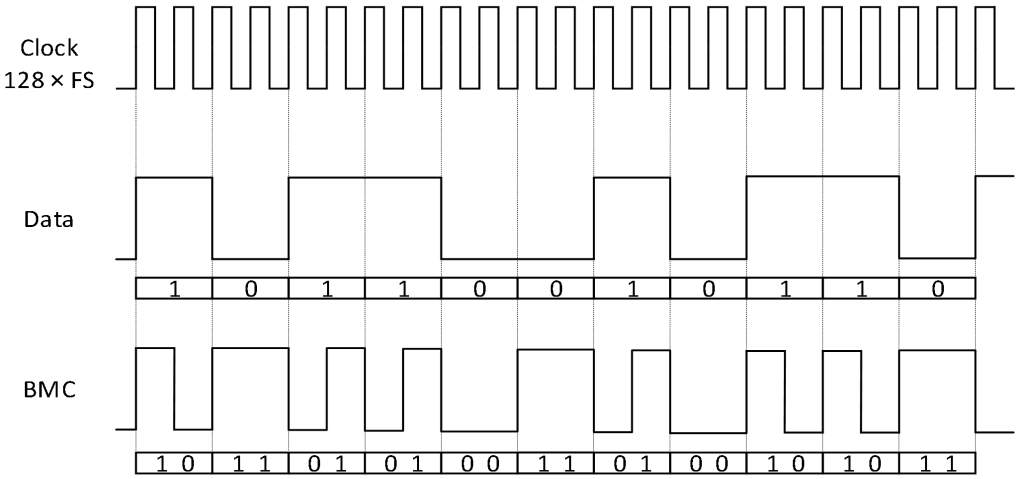


Table 4-11 Biphase-Mark Encoder

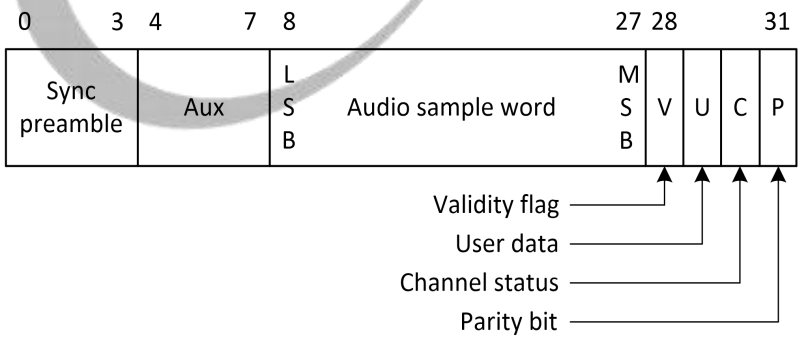
Data	Previous State	BMC
0	0	11
0	1	00
1	0	10
1	1	01

4.4.3.4 IEC60958 Transmit Format

The OWA supports digital audio data transfer and receive. It also supports full-duplex synchronous work mode. The software can set the work mode by the OWA Control Register.

Every audio sample transmitted in a sub-frame consists of 32-bit, numbered from 0 to 31. The following figure shows a sub-frame.

Figure 4-28 OWA Sub-Frame Format



Bits 0-3 carry one of the four permitted preambles to signify the type of audio sample in the current sub-frame. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0 or 1 logical states in a row.

Bits 4-27 carry the audio sample word in linear 2s-complement representation. The most-significant bit (MSB) is carried by bit 27. When a 24-bit coding range is used, the

least-significant bit (LSB) is in bit 4. When a 20-bit coding range is used, bit [8:27] carry the audio sample word with the LSB in bit 8. Bit [4:7] may be used for other applications and are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field may carry any other information.

Bit 28 carries the validity bit (V) associated with the main data field in the sub-frame.

Bit 29 carries the user data channel (U) associated with the main data field in the sub-frame.

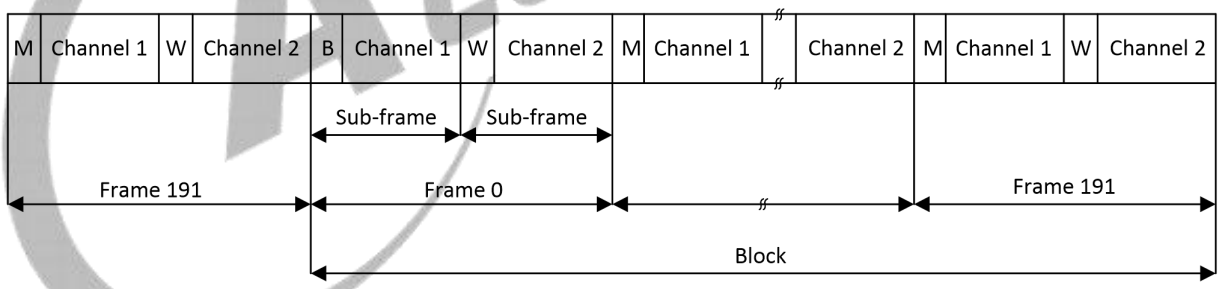
Bit 30 carries the channel status information (C) associated with the main data field in the sub-frame. The channel status indicates if the data in the sub-frame is a digital audio or some other type of data.

Bit 31 carries a parity bit (P) such that bit 4-31 carry an even number of 1s and an even number of 0s (even parity). As shown in the following table, the preambles (bit 0-3) are also defined with even parity.

Table 4-12 Preamble Codes

Preamble Code	Previous Logical State	Logical State	Description
B (or Z)	0	1110 1000	Start of a block and sub-frame 1
M (or X)	0	1110 0010	Sub-frame 1
W (or Y)	0	1110 0100	Sub-frame 2

Figure 4-29 OWA Frame/Block Format



4.4.3.5 IEC61937 Transmit Format

IEC 61937 applies to the digital audio interface by using the IEC 60958 series for the conveying of non-linear PCM encoded audio bitstreams. The non-linear PCM encoded audio bitstream is transferred by using the basic 16-bit data area of the IEC 60958 subframes, i.e. in time-slots 12 to 27. Because the non-linear PCM encoded audio bitstream to be transported is at a lower data rate than that supported by the IEC 60958 interface, the audio bitstream is broken into a sequence of discrete data-bursts, and stuffing between the data-bursts is necessary.

IEC 60958 Data Burst

The method of placing the data into the IEC 60958 bitstream is to format the data to be transmitted into data-bursts and to send each data-burst in a continuous sequence of IEC 60958 frames.

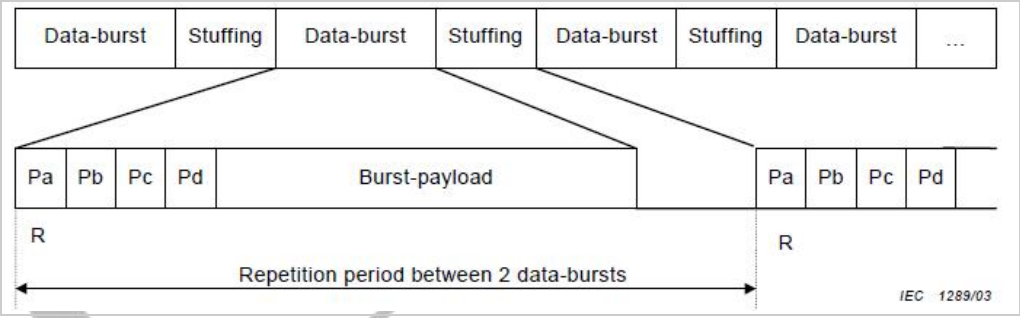
Table 4-13 Bit Allocation of Data-Burst in IEC 60958 Subframes

Subframe	Bit of subframes				
	MSB b27	b26	b25 ..... b14	b13	LSB b12
Frame 0; subframe B or M	0	1		14	15
Frame 0; subframe W	16	17		30	31
Frame 1; subframe B or M	32	33		46	47
Frame 1; subframe W	48	49		62	63
Frame 2; subframe B or M	64	65		78	79
----------			----------		
Last subframe B or M of data-burst	n-32	n-31		n-18	n-17
Last subframe W of data-burst	n-16	n-15		n-2	n-1

Data Burst Format

Each data-burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc and Pd) followed by the burst-payload which contains data of an encoded audio frame.

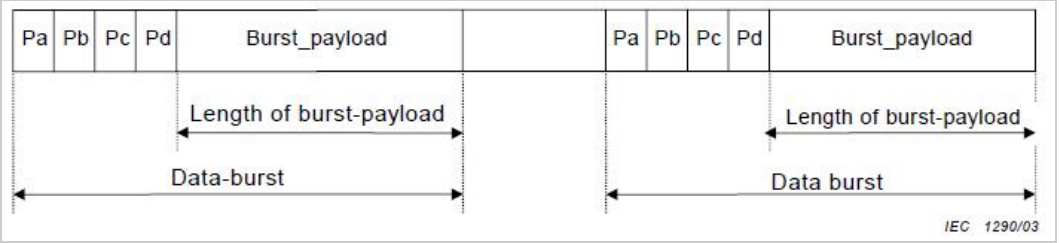
Figure 4-30 Data-Burst Format



- Burst-preamble

The burst-preamble consists of four mandatory fields. Pa and Pb represent a synchronization word. Pc gives information about the type of data, and some information/control for the receiver. Pd gives the length of the burst-payload, and is limited to 65535 bits in the case of Pd represent bits' length, or is limited to 65535 bytes in the case of Pd represent bytes' length.

Figure 4-31 Data-burst Preamble



The four preamble words are contained in two sequential IEC 60958 frames. The frame beginning the data-burst contains preamble word Pa in subframe 1, and Pb in subframe 2. The next frame contains Pc in subframe 1 and Pd in subframe 2. When placed into an IEC 60958 subframe, the MSB of a 16-bit burst-preamble word is placed into time-slot 27 and the LSB is placed into time-slot 12.

Figure 4-32 Data-burst Preamble words

Preamble word	Length of field	Contents	Value MSB..LSB
Pa	16-bit	Sync word 1	F872h
Pb	16-bit	Sync word 2	4E1Fh
Pc	16-bit	Burst-info	Table 5
Pd	16-bit	Length-code	Number of bits or number of bytes according to data-type

- Burst-information

The 16-bit burst-information contains information about the data which will be found in the data-burst.

Figure 4-33 Fields of Burst-information

Bits of Pc	Value	Contents	Remark
0 – 6		Data-type	See IEC 61937-2
7	0	Error-flag indicating a valid burst-payload	
	1	Error-flag indicating that the burst-payload may contain errors	
8 – 12		Data-type-dependent info	
13 – 15	0	Bitstream-number	
NOTE The repetition period of pause data-bursts depends on the application in which IEC 60958 is used to convey encoded audio bitstreams.			

The 7-bit data-type is defined in bits 0-6 of the burst-preamble Pc, the bit 6 is the MSB. This data-type field indicates the format of the burst-payload, which will be conveyed in the data-burst. Typical properties of a data-type are the reference point and repetition period of the burst, which is the number of sampling periods of the audio between the reference point of the current data-burst and the reference point of the next data-burst. The reference point is inherently defined for each data-type.

The error-flag bit is available to indicate if the contents of the data-burst contain data errors. If a data-burst is thought to be error-free, or if the data source does not know if the data contains errors, then the value of this bit is set to a '0'. If the data source does know that a particular data-burst contains some errors this bit may be set to a '1'. The usage of this bit by receiver is optional.

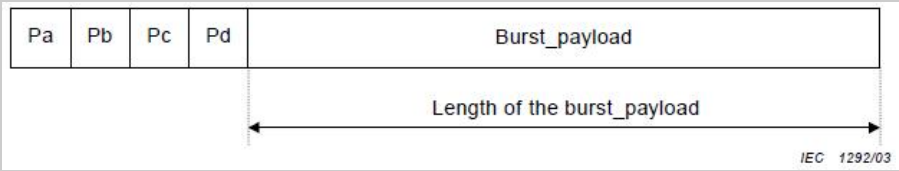
The meaning of the 5-bit data-type-dependent info depends on the value of the data-type.

The 3-bit bitstream-number indicates to which bitstream the data-burst belongs. Eight codes (0-7) are available so that up to eight independent bitstreams may be multiplexed in one bitstream in a time multiplex. Each independent bitstream shall use a unique bit-streamnumber.

- Length-code

The length-code indicates the number of bits or bytes according to data-type within the databurst, from 0 to 65535. The size of the Pa, Pb, Pc and Pd is not counted in the value of the length-code. In other words, the length-code indicates the number of bits of the burst-payload in bits, plus the conditional length of Pe and Pf, or the number of bytes of the burst-payload in bytes, plus the conditional length of Pe and Pf if exists.

Figure 4-34 Length of the Burst-Payload Specified by Pd



4.4.3.6 Audio Sample Ratio Detection

The sampling rate is calculated according to the data pulse back-stepping method. In the first phase lock of the CDR, find 1 Frame period, count by using the high-speed sampling clock, and read the counting value of the pulse, then the sampling rate can be calculated.

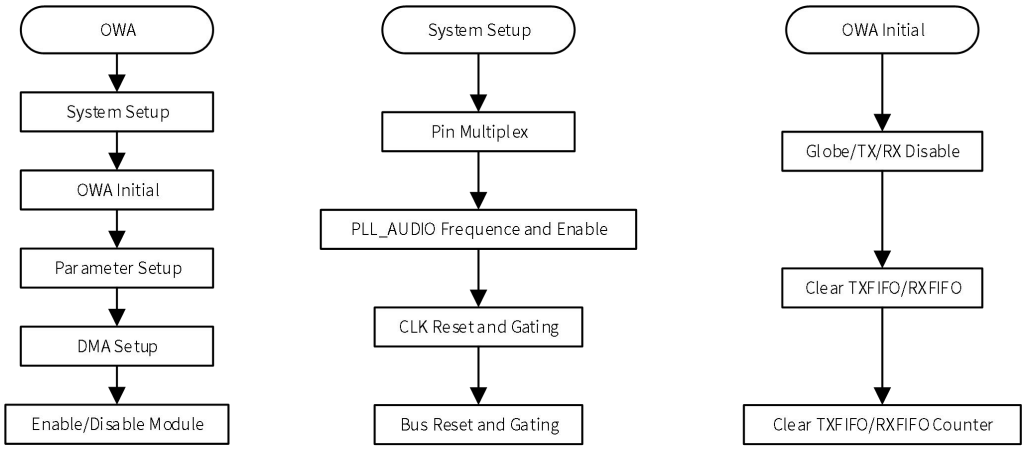
Table 4-14 The Corresponding Relation between Different System Clock and Sample Ratio

	Sample Clock Cycles		
TX Sample Rate(kHz)	196.608 MHz-SysClk	200 MHz-SysClk	300 MHz-SysClk
22.05	8916(±5)	9070(±5)	13605(±5)
24	8192(±5)	8333(±5)	12500(±5)
32	6144(±5)	6250(±5)	9375(±5)
44.1	4458(±5)	4535(±5)	6802(±5)
48	4096(±5)	4166(±5)	6250(±5)
96	2048(±5)	2083(±5)	3125(±5)
176.4	1114(±5)	1133(±5)	1700(±5)
192	1024(±5)	1041(±5)	1562(±5)

4.4.3.7 Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, channel setup, DMA setup and enable/disable module. The following sections describe these five steps.

Figure 4-35 OWA Operation Flow



Step 1 System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO because the OWA port is a multiplex pin. You can find the function in section 8.5 GPIO.

The clock source for the OWA should be followed. Firstly, reset the audio PLL in PLL_AUDIOx Control Register. Secondly, set up the frequency of the Audio PLL in the PLL_AUDIOx Control Register. After that, enable the OWA gating. Lastly, enable the OWA bus gating.

After the system setup, the register of OWA can be set up. Firstly, reset the OWA by writing 1 to OWA_CTL[0] and clear the TX/RX FIFO by writing 1 to OWA_FCTL[17:16]. After that, enable the globe enable bit by writing 1 to OWA_CTL[1] and clear the interrupt and TX/RX counter by setting OWA_ISTA and OWA_TX_CNT/OWA_RX_CNT.

Step 2 Parameter Setup and DMA Setup

You can set up the audio type, clock divider ratio, the sample format, and the trigger level, and so on. The setup of the register can be found in the specification.

The OWA supports two methods to transfer the data. The most common way is DMA; the configuration of DMA can be found in section 3.9 “DMAC”. In this module, you just enable the DRQ in OWA_INT[7].

Step 3 Enable and Disable OWA

To enable the function, you can enable TX/RX by writing OWA_TX_CFIG[31]/OWA_RX_CFIG[0]. After that, enable OWA by writing 1 to OWA_CTL[1]. Writing 0 to OWA_CTL[1] to disable process.

4.4.4 Programming Guidelines

4.4.4.1 Configuring RX CDR

The RX_CDR_MANUAL bit (bit [5]) of OWA_RX_CFIG register decides whether manual mode or automatic mode is used for clock recovery.

- Automatic Mode (default mode)

Configure RX_CDR_MANUAL bit as 1'b0 to choose automatic mode.

- Manual Mode

The manual mode could be chosen by configuring RX_CDR_MANUA bit as 1'b1. In this mode, you can select RX CDR from preamble X (11100010) or preamble X (00011101) by configuring the RX_CDR_PREAMBLE bit (bit [2]) of OWA_RX_CFIG register. The operation steps are as follows:

Step 1 Configure the INSERT_INT_EN bit (bit [16]) of OWA_EXP_ISTA register to enable insert interrupt.

Step 2 Insert TX device and wait for a while.

Step 3 Keep reading the INSERT_INT bit (bit [0]) of OWA_EXP_ISTA register until INSERT_INT = 1.

Step 4 Keep reading the RX_LOCK_FLAG bit (bit [4]) of OWA_RX_CFIG register for a software-setting period.

- If the value of RX_LOCK_FLAG bit turns to 1, it is unnecessary to configure the RX_CDR_PREAMBLE bit (bit [2]) of OWA_RX_CFIG register.
- If the value of RX_LOCK_FLAG bit doesn't turn to 1, configure the RX_CDR_PREAMBLE bit (bit [2]) of OWA_RX_CFIG register to the opposite value.

4.4.5 Register List

Module Name	Base Address
OWA	0x0711 6000

-

Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control Register
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_RX_CFIG	0x0008	OWA RX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_RXFIFO	0x0010	OWA RXFIFO Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_RX_CNT	0x0028	OWA RX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1
OWA_RXCHSTA0	0x0034	OWA RX Channel Status Register0
OWA_RXCHSTA1	0x0038	OWA RX Channel Status Register1

Register Name	Offset	Description
OWA_INSERT_REDET_CTL	0x003C	OWA Insert Redetect Control Register
OWA_EXP_CTL	0x0040	OWA Expand Control Register
OWA_EXP_ISTA	0x0044	OWA Expand Interrupt Status Register
OWA_EXP_INFO_0	0x0048	OWA Expand Information Register0
OWA_EXP_INFO_1	0x004C	OWA Expand Information Register1
OWA_EXP_DBG_0	0x0050	OWA Expand Debug Register0
OWA_EXP_DBG_1	0x0054	OWA Expand Debug Register1

4.4.6 Register Description

4.4.6.1 0x0000 OWA General Control Register (Default Value: 0x0000_0080)

Offset: 0x0000			Register Name: OWA_CTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/WAC	0x0	RST_RX Reset RX 0: Normal 1: Reset Self-clear to '0'.
11:10	/	/	/
9:5	R/W	0x4	MCLKDIV MCLK Clock Divide Ratio MCLK Divide Ratio from PLL_AUDIO 00000: Divide by 128 00001: Divide by 2 00010: Divide by 4 00011: Divide by 6 00100: Divide by 8 00101: Divide by 10 00110: Divide by 12 00111: Divide by 14 01000: Divide by 16 01001: Divide by 18 01010: Divide by 20 01011: Divide by 22 01100: Divide by 24 ..... 11111: Divide by 62
4	/	/	/
3	R/W	0x0	MCLKEN MCLK Enable

Offset: 0x0000			Register Name: OWA_CTL
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
2	R/W	0x0	LOOP Loopback Test 0: Normal Mode 1: Loopback Test When the bit is set to '1', the DOUT and DIN need be connected.
1	R/W	0x0	GEN Global Enable Disabling this bit overrides the operations of enabling and flushing all FIFOs by any other blocks or channels. 0: Disabled 1: Enabled
0	R/W	0x0	RST_TX Reset TX 0: Normal 1: Reset Self-clear to 0.

4.4.6.2 0x0004 OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_SINGLE_MODE TX Single Channel Mode 0: Disabled 1: Enabled
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select when TX FIFO Underrun 0: Sending 0 1: Sending the last audio Note: This bit is only valid in PCM mode.
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio (Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	Read/Write	Default/Hex	Description
			TX Clock Divide Ratio Clock divide ratio = TX_TATIO + 1 Fs = PLL_AUDIO/[(TX_TATIO + 1)*64*2]
3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A and B set to 0 1: Channel status A and B generated from TX_CHSTA
0	R/W	0x0	TXEN TX Enable 0: Disabled 1: Enabled

4.4.6.3 0x0008 OWA RX Configure Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	RX_CDR_MANUAL RX CDR mode 0: Automatic (in this mode, RX_CDR_PREAMBLE does not need to be configured) 1: Manual (in this mode, if the header code is not able to be received accurately, RX_CDR_PREAMBLE needs to be configured)
4	R	0x0	RX_LOCK_FLAG RX Lock Flag 0: Unlocked 1: Locked
3	R/W	0x0	RX_CHST_SRC RX Channel State Source Select 0: RX_CH_STA register holds status from Channel A 1: RX_CH_STA register holds status from Channel B
2	R/W	0x0	RX_CDR_PREAMBLE RX channel CDR Preamble Type 0: support CDR from preamble X (11100010)

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	Read/Write	Default/Hex	Description
			1: support CDR from preamble X (00011101)
1	R/W	0x0	CHST_CP Channel Status Capture 0: Idle or Capture End 1: Capture Channel Status Start The field must be set to 1 at each operation (such as recording). When set to '1', the system starts to capture the channel status. When finished, the bit will automatically turn to '0'.
0	R/W	0x0	RXEN 0: Disabled 1: Enabled

4.4.6.4 0x000C OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	RX_LOCK_INT RX Lock Interrupt 0: No Pending IRQ 1: RX Lock Pending Interrupt (RX_LOCK_FLAG turns from 0 to 1) Write '1' to clear this interrupt.
17	R/W1C	0x0	RX_UNLOCK_INT RX Unlock Pending Interrupt 0: No Pending IRQ 1: RX Unlock Pending Interrupt (RX_LOCK_FLAG turns from 0 to 1) Write 1 to clear this interrupt.
16	R/W1C	0x0	RX_PARERRI_INT RX Parity Error Pending Interrupt 0: No Pending IRQ 1: RX Parity Error Pending Interrupt Write "1" to clear this interrupt.
15:7	/	/	/
6	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: FIFO Underrun Pending Interrupt

Offset: 0x000C			Register Name: OWA_ISTA
Bit	Read/Write	Default/Hex	Description
			Writing “1” to clear this interrupt.
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Writing “1” to clear this interrupt.
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Writing “1” to clear this interrupt or automatically clear if the interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: RXFIFO Overrun Pending Write ‘1’ to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if the interrupt condition fails.

4.4.6.5 0x0010 OWA RXFIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: OWA_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA The host can get one sample by reading this register, A channel data is first, and then the B channel data.

4.4.6.6 0x0014 OWA FIFO Control Register (Default Value: 0x0004_0200)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable The bit takes effect only when the TXEN is set to 1.

Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
			Audio codec/I2S0/I2S1/I2S2/I2S3/OWA TXFIFO Hub Enable. 0: Disabled 1: Enabled
30	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self-clear to '0'.
29	R/W1C	0x0	FRX Write '1' to flush RXFIFO, self-clear to '0'.
28:22	/	/	/
21	R/W	0x0	RX_SYNC_EN_START The bit takes effect only when the RX_SYNC_EN is set to 1. Audio Codec/I2S0/I2S1/I2S2/I2S3/DMIC/OWA RX Synchronize Enable Start. 0: Disabled 1: Enabled
20	R/W	0x0	RX_SYNC_EN OWA RX Synchronize Enable 0: Disabled 1: Enabled
19:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition. Trigger Level = TXTL
11	/	/	/
10:4	R/W	0x20	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode0, 1) 0: Valid data at the MSB of TXFIFO Register 1: Valid data at the LSB of TXFIFO Register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO [23:0] = {APB_WDATA [31:12], 4'h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode(Mode 0,1,2,3)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	Read/Write	Default/Hex	Description
			00: Expanding '0' at LSB of RXFIFO Register 01: Expanding received sample sign bit at MSB of RXFIFO Register 10: Truncating received samples at high half-word of RXFIFO Register and low half-word of RXFIFO Register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO Register and high half-word of RXFIFO Register is expanded by its sigh bit Mode 0: APB_RDATA [31:0] = {RXFIFO [23:0], 8'h0} Mode 1: APB_RDATA [31:0] = {8'RXFIFO [23], RXFIFO [23:0]} Mode 2: APB_RDATA [31:0] = {RXFIFO [23:8], 16'h0} Mode 3: APB_RDATA[31:0] = {16'RXFIFO[23], RXFIFO[23:8]}

4.4.6.7 0x0018 OWA FIFO Status Register (Default Value: 0x8080_0000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	Read/Write	Default/Hex	Description
31	R	0x1	TXE TXFIFO Empty (indicate the TXFIFO is not full) 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
30:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
14:7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

4.4.6.8 0x001C OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description

Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	RX_LOCKI_EN RX LOCK Interrupt Enable 0: Disabled 1: Enabled
17	R/W	0x0	RX_UNLOCKI_EN RX UNLOCK Interrupt Enable 0: Disabled 1: Enabled
16	R/W	0x0	RX_PARERRI_EN RX PARITY ERORR Interrupt Enable 0: Disabled 1: Enabled
15:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disabled 1: Enabled
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disabled 1: Enabled
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disabled 1: Enabled
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disabled 1: Enabled
3	/	/	/
2	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable When set to '1', RXFIFO DMA Request is asserted if data is available in RXFIFO. 0: Disabled 1: Enabled
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disabled 1: Enabled

Offset: 0x001C			Register Name: OWA_INT
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disabled 1: Enabled

4.4.6.9 0x0020 OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. A channel data is first, and then the B channel data.

4.4.6.10 0x0024 OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After updated by the initial value, the counter register should count on the base of this initial value.

4.4.6.11 0x0028 OWA RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: OWA_RX_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX counter register can be set to any initial value at any time. After being updated by the initial value, the

Offset: 0x0028			Register Name: OWA_RX_CNT
Bit	Read/Write	Default/Hex	Description
			counter register should count on the base of this value.

4.4.6.12 0x002C OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1 kHz 0001: Not indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	Read/Write	Default/Hex	Description
			Mode 00: Default Mode 01 to 11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 μs/15 μs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100 to 111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001 to 111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application This bit must be fixed to “0”.

4.4.6.13 0x0030 OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz 0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = “0”: 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

4.4.6.14 0x0034 OWA RX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not Matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1 kHz 0001: Not Indicated 0010: 48 kHz 0011: 32 kHz 0100: 22.05 kHz 0101: Reserved 0110: 24 kHz 0111: Reserved 1000: Reserved 1001: 768 kHz 1010: 96 kHz 1011: Reserved 1100: 176.4 kHz 1101: Reserved 1110: 192 kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the Kind of Equipment that Generates the digital audio interface Signal.
7:6	R/W	0x0	MODE Mode 00: Default mode 01 to 11: Reserved
5:3	R/W	0x0	EMP Emphasis

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	Read/Write	Default/Hex	Description
			Additional Format Information For bit 1 = '0', Linear PCM Audio mode: 000: 2 Audio channels without pre-emphasis 001: 2 Audio channels with 50 μs/15 μs pre-emphasis 010: Reserved (For 2 Audio channels with pre-emphasis) 011: Reserved (For 2 Audio channels with pre-emphasis) 100 to 111: Reserved For bit 1 = '1', Other than Linear PCM applications: 000: Default state 001 to 111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No Copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application

4.4.6.15 0x0038 OWA RX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition is not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192 kHz 0010: 12 kHz 0011: 176.4 kHz

Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	Read/Write	Default/Hex	Description
			0100: Reserved 0101: 96 kHz 0110: 8 kHz 0111: 88.2 kHz 1000: 16 kHz 1001: 24 kHz 1010: 11.025 kHz 1011: 22.05 kHz 1100: 32 kHz 1101: 48 kHz 1110: Reserved 1111: 44.1 kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = '0': 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = '1': 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum Audio sample word length is 20 bits 1: Maximum Audio sample word length is 24 bits

4.4.6.16 0x003C OWA Insert Redetect Control Register (Default Value:0x0000_0180)

Offset: 0x003C			Register Name: S|PDIF_INSERT_REDET_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x1	INSERT_REDET_MONITOR_ENABLE

Offset: 0x003C			Register Name: S|PDIF_INSERT_REDET_CTL
Bit	Read/Write	Default/Hex	Description
			Insert Re-detect Monitor Enable 0: disable 1: enable
7:0	R/W	0x80	INSERT_REDET_MONITOR_ENABLE Insert Re-detect Monitor Length The unit is one 32KHz cycle.

4.4.6.17 0x0040 OWA Expand Control Register (Default Value: 0x0000_000F)

Offset: 0x0040			Register Name: OWA_EXP_CTL
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	BURST_DATAOUT_SELECT Burst data output select 0: Burst preamble and payload 1: Burst payload
29:16	R/W	0x0	REPEAT_PERIOD_OF_FR_NUM The number for the repetition period of the burst frame Configure this field according to RX data. A mismatch between the configuration data and the received data will result in an error interrupt.
15	R/W	0x0	UNIT_SELECT Unit Select Configure this field according to RX data type 0: In units of 16-bit 1: In units of 2-byte
14	R/W	0x0	OWA_RX_MODE_MAN OWA RX Protocol Select 0: IEC60958 1: IEC61937
13	R/W	0x0	OWA_RX_MODE OWA RX Mode Select 0: Manual Ctrl. Configure by OWA RX_MODE_MAN 1: Auto Ctrl. Configure by the channel status values resolved by hardware
12	R/W	0x0	AUDIO_DATA_BITORDER_EN Audio Data Bitorder Enable 0: The audio data received by RX is stored directly into FIFO 1: The audio data received by RX is reversed high and

Offset: 0x0040			Register Name: OWA_EXP_CTL
Bit	Read/Write	Default/Hex	Description
			low bits, then stored into FIFO
11	R/W	0x0	DATA_LENGTH_BITORDER_EN Data Length Bitorder Enable 0: The received PD data is as the length of the valid audio data 1: The received PD data is reversed high and low bits, then as the length of the valid audio data
10	R/W	0x0	DATA_TYPE_BITORDER_EN Data Type Bitorder Enable 0: The received PC data is as the data length of the valid audio 1: The received PC data is reversed high and low bits, then as the length of the valid audio data
9	R/W	0x0	SYNCW_BITORDER_EN 0: Pa/Pb is the sync code of audio data 1: Pa/Pb reversed high and low bits is the sync code of audio data
8	R/W	0x0	INSERT_DETECTION_ENABLE Insert Detection Enable 0: Disable 1: Enable
7:0	R/W	0x0F	INSERT_DETECTION_NUM Insert Detection Number Configure how many jumping edges are detected to generate an insertion interrupt

4.4.6.18 0x0044 OWA Expand Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	PD_CHANGE_INT_EN PD_LENGTH_CHANGE Interrupt Enable 0: Disable 1: Enable
23	R/W	0x0	PC_PAUSE_STOP_INT PC_PAUSE_BURSTS_STOP Interrupt Enable 0: Disable 1: Enable
22	R/W	0x0	PC_BITSTRM_CHANGE_INT_EN PC_BITSTREAM_CHANGE Interrupt Enable

Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
21	R/W	0x0	PC_ERR_FLAG_INT PC_ERROR_FLAG Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	PC_DTYPE_CHANGE_INT_EN PC_DATATYPE_CHANGE Interrupt Enable 0: Disable 1: Enable
19	R/W	0x0	RPDB_ERR_INT_EN RPDB_ERROR Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PCPD_CAP_INT_EN PCPD_CAP Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PAPB_CAP_INT_EN PAPB_CAP Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	INSERT_INT_EN INSERT Interrupt Enable 0: Disable 1: Enable
15:9	/	/	/
8	R/W1C	0x0	PD_CHANGE_INT PD CHANGE INT 0: No Pending IRQ 1: PD Data length information is change. (except Pause/Null data burst type) Write '1' to clear this interrupt.
7	R/W1C	0x0	PC_PAUSE_STOP_INT Audio bitstream is interrupted. When stopped, the interface becomes idle. 0: No Pending IRQ 1: PC Pause burst Stop, frame sequence discontinued. Transmitters may optionally use the STOP value to indicate that the transmission of the current encoded

Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
			Write '1' to clear this interrupt.
6	R/W1C	0x0	PC_BITSTRM_CHANGE_INT PC BITSTRM CHANGE INT 0: No Pending IRQ 1: PC Bitstream Number is change. Bitstream Number indicates which bitstream the data burst belongs. (except Pause/Null data bursts type) Write '1' to clear this interrupt.
5	R/W1C	0x0	PC_ERR_FLAG_INT PC ERR FLAG INT 0: No Pending IRQ 1: PC Error-flag is available to indicate if the contents of the data-burst contain data errors (except Pause/Null data bursts type). The using of this bit by receivers is optional. Write '1' to clear this interrupt.
4	R/W1C	0x0	PC_DTYPE_CHANGE_INT PC DTYPE CHANGE INT 0: No Pending IRQ 1: PC Datatype (except Pause/Null data type) information is change Write '1' to clear this interrupt.
3	R/W1C	0x0	RPDB_ERR_INT RPDB ERR INT 0: No Pending IRQ 1: Hardware counts the repetition period of the burst frame is different from register configuration number Write '1' to clear this interrupt.
2	R/W1C	0x0	PCPD_CAP_INT PCPD CAP INT 0: No Pending IRQ 1: IEC61937 mode captures PC and PD Write '1' to clear this interrupt.
1	R/W1C	0x0	PAPB_CAP_INT PAPB CAP INT 0: No Pending IRQ 1: IEC61937 mode captures PA and PB Write '1' to clear this interrupt.
0	R/W1C	0x0	INSERT_INT INSERT INT 0: No Pending IRQ

Offset: 0x0044			Register Name: OWA_EXP_ISTA
Bit	Read/Write	Default/Hex	Description
			1: OWA RX detects device insertion Write '1' to clear this interrupt.

4.4.6.19 0x0048 OWA Expand Information Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: OWA_EXP_INFO_0
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PC_DATA PC Data information
15:0	R	0x0	PD_DATA PD Data information

4.4.6.20 0x004C OWA Expand Information Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: OWA_EXP_INFO_1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	REPET_PERIOD_OF_FR_VALUE Repetition period of the burst frame value Check whether the repetition period of the burst frame calculated by hardware is consistent with the configuration value.
15:0	R	0x0	SR_VALUE Sample Rate Value Read this value after RX_LOCK.

4.4.6.21 0x0050 OWA Expand Debug Register 0 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: OWA_EXP_DBG_0
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	IEC61937_DATA_CAP_FSM IEC61937 Data Captures State Machine 000: IDLE 001: SYNC_PA 010: SYNC_PB 011: DTYPE_PC 100: DLEN_PD 101: RX_ACTIVE

Offset: 0x0050			Register Name: OWA_EXP_DBG_0
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0	DATA_CAP_NUM Remains Data Counter Value See the value of the sampled valid data in real time.

4.4.6.22 0x0054 OWA Expand Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: OWA_EXP_DBG_1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	REPET_PERIOD_OF_FR_CNT Repetition period of the burst frame counter See the value of repetition period counter in real time.
15:0	R	0x0	SR_CNT Sample Rate Counter See the value of audio sample ratio in real time.

Contents

5 Video and Graphics

5.1 Display Engine (DE)

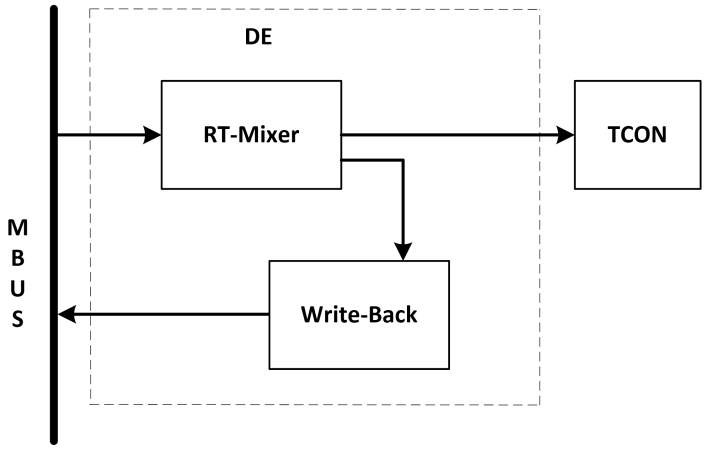
The Display Engine (DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 5-1.

The DE has the following features:

- Output size up to 4096 x 2048
- Supports seven alpha blending channels for main display and two display outputs
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports AFBC buffer decoder
- Supports vertical keystone correction
- Input format
  - Semi-planar of YUV422/YUV420/YUV411/P010/P210
  - Planar of YUV422/YUV420/ YUV411
  - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Output format: 8-bit or 10-bit YUV444/YUV422/YUV420/RGB444
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- 10-bit processing path for HDR video
- SmartColor5.0 for excellent display experience
  - Adaptive de-noising for compression noise or mosquito noise with yuv420/422 input
  - Adaptive super resolution scaler
  - Adaptive local dynamic contrast enhancement
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement (blue-stretch, green-stretch, and fresh tone correction) and
  - Skin tone protection
  - Hue gain, saturation gain, and value gain controller
  - Fully programmable color matrix
  - Dynamic gamma

- Supports write back for high efficient dual display and miracast
- Supports register configuration queue for register update function

Figure 5-1 DE Block Diagram



5.2 De-interlacer (DI)

The De-interlacer (DI) converts the interlaced input video frame to progressive video frame.

The DI has the following features:

- Only off-line processing mode
- Video resolution from 32x32 to 2048x1280 pixel
- Input data format: 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined
- Output data format
  - 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined for DIT
  - YV12/planar YUV422 for TNR
- Weave/pixel-motion-adaptive de-interlace method
- Temporal noise reduction
- Film mode detection with video-on-film detection
- Performance
  - Module clock 120MHz for 1080P@60Hz YUV420 with all functions enable
  - Module clock 150MHz for 1080P@60Hz YUV422 with all functions enable

5.3 Graphic 2D (G2D)

The Graphic 2D (G2D) engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- layer size up to 2048x2048 pixels
- Input format and output format contain the following:
  - YUV422 (semi-planar and planar format)
  - YUV420 (semi-planar and planar format)
  - P010, P210, P410, and Y8
  - ARGB8888, XRGB8888, RGB888, ARGB4444, ARGB1555, ARGB2101010, and RGB565
- Multiple rotation types
  - Horizontal flip and vertical flip
  - 0, 90, 180, or 270 degrees' rotation in clockwise direction

5.4 Video Engine

5.4.1 Video Decoding

The Video Decoding consists of Video Control Firmware(VCF) running on ARM processor and embedded hardware Video Engine(VE). VCF gets the bitstream from topper software, parses bitstream, invokes the Video Engine, and generates the decoding image sequence. The decoder image sequence is transmitted by the video output controller to the display device under the control of the topper software.

The Video Decoding has the following features:

- Supports ITU-T H.265 Main/Main10, level 6.1
  - Maximum video resolution:8192x4320
  - Maximum decoding rate: 3840x2160@60fps, 10bit
- Supports VP9 Profile0/ Profile2, level 6.1
  - Maximum video resolution: 8192 x 4320
  - Maximum decoding rate: 3840x2160@60fps, 10bit
- Supports ITU-T H.264 Base/Main/High Profile@Level 4.2
  - Maximum video resolution: 3840 x 2160
  - Maximum decoding rate: 3840x2160@30fps, 8bit
- Supports ITU-T H.263 Base Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports VP8
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG4 Simple/ Advanced Simple Profile@Level 5
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG2 Main Profile, High Level
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports MPEG1 Main Profile, High Level
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps

- Supports XVID
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports Sorenson Spark
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports AVS/AVS+ Jizhun Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 1920x1080@60fps
- Supports JPEG JFIF file format, Not Support Non-interleaved Scan
  - Maximum video resolution: 16384 x 16384
  - Maximum decoding rate: 1920x1080@60fps

5.4.2 Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPEG). The VE supports H.264 encoding, and JPEG supports JPEG/MJPEG encoding.

5.4.2.1 VE

The VE is a CODEC that supports H.264 protocol based on ASIC. It is custom-made for the IPC usage and features high compressing rate, low CPU usage, short delay and low power consumption.

The VE has the following features:

- Supports ITU-T H.264 High profile /Main Profile/Baseline profile @Level 4.2 encoding
- Supports the output picture format: semi-planar YCbCr4:2:0
- Motion compensation with 1/2 or 1/4-pixel precision
- Four prediction unit (PU) types of 16x16, 16x8, 8x16 and 8x8 for inter-prediction
- Three PU types of 16x16, 8x8 and 4x4 for intra-prediction
- Transform 4x4 and transform 8x8
- CABAC and CAVLC entropy encoding
- In-loop deblocking filter
- Multi-slice encoding
- Supports normal functions: Macro-block rate control, 3D denoising, intra-refresh, inter-only-in-P-frame
- Supports special functions: dynamic search window range

- Supports region of interest(ROI) encoding with custom QP map
- Supports three-bit rate control modes: constant bit rate(CBR), variable bit rate(VBR), and FIXEDQP
- Supports lossless compression for reference frame.
- Supports OSD front-end overlaying
- Supports the output bit rate ranging from 256 kbit/s to 100 Mbit/s

5.4.2.2 JPEG

The JPEG is a high-performance JPEG encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPEG has the following features:

- ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - YCbCr4:2:2
  - YCbCr4:4:4
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlaying
- Supports the color-to-gray function

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6 Video Output Interfaces

6.1 eDP1.3

6.1.1 Overview

The Embedded Display Port (eDP) is a standard protocol in the digital display field. It is completely compatible with DP and consists of main link, auxiliary channel, and hot plugging.

The eDP includes the following features:

- Up to 2.5K@60fps
- 1-lane, 2-lane, or 4-lane transmission, up to 2.7 Gbps/lane
- Video formats: RGB, YCbCr4:4:4, and YCbCr4:2:2
- Color depth: 8-bit and 10-bit per channel
- Supports I2S interface
  - Supports mono sound, stereo sound, and 7.1 surround sound
  - Maximum sampling rate: 192 kHz
- Full link training
- Hot plug detection
- AUX channel
  - Maximum working frequency: 1MHz
  - Adopts Manchester-II encoding
- Clock spread spectrum
- Programmable voltage swing and pre-emphasis
- Embedded ESD

6.1.2 Functional Descriptions

6.1.2.1 External Signals

The following table describes the external I/O signals of the eDP module.

Table 6-1 eDP External Signals

Signal Name	Description	Type
EDP-AUXN	AUX channel Negative Input/Output	A I/O
EDP-AUXP	AUX channel Positive Input/Output	A I/O

Signal Name	Description	Type
EDP-HPD	Hot Plug Detection Signal	AI
EDP-REXT	eDP External Reference Resistor	AO
EDP-TX0N	eDP Negative Output of Data Channel0	AO
EDP-TX0P	eDP Positive Output of Data Channel0	AO
EDP-TX1N	eDP Negative Output of Data Channel1	AO
EDP-TX1P	eDP Positive Output of Data Channel1	AO
EDP-TX2N	eDP Negative Output of Data Channel2	AO
EDP-TX2P	eDP Positive Output of Data Channel2	AO
EDP-TX3N	eDP Negative Output of Data Channel3	AO
EDP-TX3P	eDP Positive Output of Data Channel3	AO
VCC18-EDP	1.8V Analog Supply	P
VDD09-EDP	0.9V Digital Supply	P

6.1.2.2 PLL Configuration

Allwinner eDP TX IP contains a core PLL to generate core clock and high speed half-rate bit clock required for normal operation from the reference clock. If the additional pixel PLL is included, it can generate the pixel clock for controller from the reference clock.

- Core PLL VCO Clock

The frequency of core PLL VCO clock is controlled by pre-div divider (corepll_prediv [5:0], 0x0180[13:8]) and feedback divider (corepll_fbdiv [11:0], 0x0180[19:16]and 0x0180[31:24]). The pre-PLL VCO frequency is calculated as:

fcorevco = fref / corepll_prediv [5:0] * corepll_fbdiv [11:0]

For fractional operation, the fractional divider (corepll_frac [23:0], 0x0184 [7:0], 0x0184 [15:8] and 0x0184 [23:16]) should be turned on by setting the fractional divider control register (corepll_frac_pd [1:0], 0x0180[5:4]) to 2'b00. The core PLL VCO frequency is calculated as:

fcorevco = fref / corepll_prediv [5:0] * (corepll_fbdiv [11:0] +corepll_frac [23:0]/224)

- Bit Clock

The frequency of bit clock should be half of the channel data rate and is controlled by post-div divider (corepll_postdiv [1:0], 0x0188[3:2]). The frequency of bit clock is calculated as:

fbitclk = fcorevco / corepll_postdiv [1:0]

- Core Clock

The frequency of core clock is calculated as:

fcoreclk = fbitclk / 10

- Pixel PLL VCO Clock

The frequency of pixel PLL VCO clock is controlled by pre-div divider (pixelpll_prediv [5:0], 0x00A1 [5:0]) and feedback divider (pixelpll_fbdiv [11:0], 0x0190 [19:16] and 0x0190 [31:24]). The pixel PLL VCO frequency is calculated as:

fpixelvco = fref / pixelpll_prediv [5:0] * pixelpll_fbdiv [11:0]

For fractional operation, the fractional divider (pixelpll_frac [23:0], 0x019C [7:0], 0x019C [15:8] and 0x019C [23:16]) should be turned on by setting the fractional divider control register (pixelpll_frac_pd [1:0], 0x0190[5:4]) to 2'b00. The pixel PLL VCO frequency is calculated as:

fpixelvco = fref / pixelpll_prediv [5:0] * (pixelpll_fbdiv [11:0] +pixelpll_frac [23:0]/2^{24})

- Pixel Clock

The frequency of pixel clock is controlled by pixel clock divider a (pixelpll_pclkdiva [4:0], 0x0194 [4:0]), divider b (pixelpll_pclkdivb [1:0], 0x0194[9:8]) and divider c (pixelpll_pclkdivc [4:0], 0x0194 [20:16]). When pixelpll_pclkdiva [4:0] is set to be 5'h01, the frequency of pixel clock is calculated as:

fpclk = fpixelvco / (2*pixelpll_pclkdivb [1:0] *pixelpll_pclkdivc [4:0])

When pixelpll_pclkdiva [4:0] is not set to be 5'b01, the frequency of pixel clock is calculated as:

fpclk = fpixelvco / (2*pixelpll_pclkdiva [4:0] * pixelpll_pclkdivc [4:0])

NOTE

- The VCO running frequency should be kept in the range from 1 GHz to 3 GHz for core PLL and pixel PLL.
- PLL should be power down before configuration.

Table below gives the recommended core PLL configuration with 24MHz reference clock for typical link rates.

Table 6-2 Recommended Core PLL Configuration with 24MHz Reference Clock

Link Rate	1.62G	2.7G
core PLL VCO	1.62GHz	2.7GHz
bit clock	0.81GHz	1.35GHz
core clock	81MHz	135MHz
24MHz reference clock		
corepll_prediv[5:0]	6'h02	6'h02
corepll_fbdiv[11:0]	12'h087	12'h0e1
corepll_postdiv[1:0]	2'b01	2'b01
corepll_frac_pd[1:0]	2'b11	2'b11
corepll_frac[23:0]	24'b0	24'b0

Table below gives the recommended pixel PLL configuration with 24MHz reference clock for typical video formats.

Table 6-3 Recommended Pixel PLL Configuration with 24MHz Reference Clock

Video Format	720P/60	1080P/60	2160P/30
pixel PLL VCO	2.376GHz	2.376GHz	2.376GHz
pixel clock	74.25MHz	148.5MHz	297MHz
24MHz reference clock			
pixelpll_prediv[5:0]	6'h01	6'h01	6'h01
pixelpll_fbdiv[11:0]	12'h063	12'h063	12'h063
pixelpll_pclkdiva[4:0]	5'h01	5'h01	5'h01
pixelpll_pclkdivb[1:0]	2'b01	2'b01	2'b01
pixelpll_pclkdivc[4:0]	5'h08	5'h04	5'h02
pixelpll_frac_pd[1:0]	2'b11	2'b11	2'b11
pixelpll_frac[23:0]	24'b0	24'b0	24'b0

6.1.2.3 Termination Configuration

In order to improve the signal quality, the termination resistance should match the impedance of PCB trace to minimize reflection. The differential characteristic impedance of differential pair trance on PCB is typical 100Ω. Thus the differential termination resistance of the receiver is preferred to be 100Ω around.

The termination resistance could be manually set by writing the differential termination resistance control registers (rtm [5:0], 0x01C4[5:0]/0x01C4[13:8]/0x01C4[21:16]/0x01C4[29:24]) with reference value for 4 data channels and AUX channel, respectively. The reference value for TT corner is calculated as:

RT = 4000 / rtm [5:0]

For example, if rtm [5:0] is set to 6'h28 and the decimal value is 40, the differential termination resistance will be 100Ω for TT corner. If rtm [5:0] is set to 6'h00, the termination resistance will be turned off. However, the termination resistance value varies along with the process variation.

Allwinner eDP TX IP also employs a resistance calibration mechanism to eliminate the process variation. The resistance calibration compares the termination resistor with the off-chip reference resistor, and adjusts its value to the target value set by calibration control register (rcal_sel [1:0], 0x01C0[26:25]) with insignificant error. The calibration result will be stored in calibration result register (rcal_val [5:0], 0x01C0[5:0]). After calibration, the transmitter termination resistance will be configured according to the calibration result.

The configuration method for termination resistance is controlled by the calibration bypass register (rcal_byp, 0x01C0[15]). If the termination resistance is desired to be set with the manual method, the resistance calibration should be bypassed.

The termination resistance calibration is configured as follow:

Step 1 configure the resistance calibration clock divider (0x01C0[14:8] and 0x01C0[23:16]) to set the clock frequency to be 100KHz around. For example, if the system clock is 100MHz, write 15'd1000 to the divider register.

Step 2 configure the resistance calibration target value (0x01C0[26:25]). For example, if 100Ω differential termination resistance is desired, write 2'b00 to register 0x01C0[26:25].

Step 3 configure the calibration bypass register (0x01C0[15]) to start the resistance calibration by writing 1'b1 to 0x01C0[15] firstly and then writing 1'b0 to register 0x01C0[15]. A falling edge of 0x01C0[15] will trigger the startup of the automatic resistance calibration. After calibration is done, the termination resistance of data channels and AUX channel will be configured according to the calibration result.

6.1.2.4 Transmitter Configuration

The transmitter in each data channel adopts 3-tap FFE (Feed Forward Equalizer) to compensate the channel loss, including the pre-cursor tap, main cursor tap and post-cursor tap. The pre-cursor tap and the post-cursor tap serve as the pre-emphasis.

The output levels of above 3 taps are all programmable and controlled by the driver current bias (Ibias). Ibias can be adjusted by current bias control register (isel [3:0], 0x01A8[3:0] 0x01A8[7:4] 0x01A4[27:24] and 0x01A4[31:28]) and is calculated as:

Ibias = 160uA + 40uA * isel [3:0]

There are also independent registers to adjust the levels of 3 taps, respectively.

The main cursor tap could be adjusted by registers output voltage level control registers (mainsel [4:0], 0x01AC[12:8]/0x01AC[4:0]/0x01A8[28:24]/0x01A8[20:16]) for 4 TMDS channels, respectively, and the output current level is calculated as:

Imain = Ibias * mainsel [4:0]

The pre-cursor tap could be adjusted by pre-cursor pre-emphasis level control registers (presel [2:0], 0x01B0[6:4]/0x01B0[2:0]/0x01B0[14:12]/0x01B0[10:8]) for 4 TMDS data channels, respectively, and the output current level is calculated as:

Ipre = Ibias * presel [2:0]

The post-cursor tap could be adjusted by post-cursor pre-emphasis level control registers (postsel [3:0], 0x01AC [23:20]/0x01AC [19:16]/0x01AC [31:28]/0x01AC [27:24]) for 4 TMDS channels, respectively, and the output current level is calculated as:

Ipost = Ibias * postsel [3:0]

The pre-cursor pre-emphasis level is calculated as:

Lpre = 20 * log [(Imain + Ipre) / (Imain – Ipre)]

The post-cursor pre-emphasis level is calculated as:

Lpost = 20 * log [(Imain + Ipost) / (Imain – Ipost)]

The combinations of different levels of 3 taps result in different transmitter eye and output voltage levels for different data pattern. The pre-emphasis levels should be carefully adjusted according to the actual condition to minimize the ISI introduced by the TX end. The following table gives the recommended transmitter configuration for different data rates.

Table 6-4 Recommended Transmitter Configuration for Different Data Rates

Register	Level	1.62Gbps	2.7Gbps
isel[3:0]	Voltage Swing Level 0	4'b0000	4'b0000
	Voltage Swing Level 1	4'b0010	4'b0010
	Voltage Swing Level 2	4'b0100	4'b0100
	Voltage Swing Level 3	4'b0110	4'b0110
mainsel[4:0]		5'b11111	5'b11111
postsel[3:0]	Pre-emphasis Level 0	4'b0000	4'b0000
	Pre-emphasis Level 1	4'b0001	4'b0001
	Pre-emphasis Level 2	4'b0010	4'b0010
	Pre-emphasis Level 3	4'b0011	4'b0011
presel[2:0]		3'b000	3'b000

6.1.2.5 SSC Configuration

Allwinner eDP TX IP contains SSC function for data channel to deal with possible EMI problem. The features the SSC modulation are listed as follow:

- Support down spread and center spread modulation.
- Support 3-bit programmable modulation depth from 500ppm to 32000ppm.
- Support default triangular wave and programmable wave modulation.
- Support adjustable modulation frequency.

The SSC modulation is configured as follows:

Step 1 Configure the modulation mode control register (0x0180[20]) to select down spread or center spread.

Step 2 Configure the modulation frequency control register (0x0188[27:24]) to select SSC modulation frequency.

Step 3 Configure the modulation amplitude control register (0x0188[30:28]) to select SSC modulation amplitude.

Step 4 Configure the fractional PLL enable register (0x0180[5:4]) to 2'b00.

Step 5 Configure the SSC modulation enable register (0x0180[21]) to 1'b0.

The SSC modulation frequency is calculated as:

$f_{ssc} = f_{ref}$ /corepll_prediv[5:0]/128/decimal value of 0x0188[27:24]

The default setting results in down spread SSC modulation with 31.25KHz frequency and 4000ppm amplitude with 24MHz reference clock.

6.1.3 Register List

Module Name	Base Address
EDP	0x0572_0000

Register Name	Offset	Description
EDP_HPD_SCALE	0x0018	EDP HPD Scale Register
EDP_RST	0x001C	EDP Reset Register
EDP_HPD_EVENT	0x0080	HPD Event Status Register
EDP_HPD_INT	0x0084	Enable Hpd Plug Interrupt Register
EDP_HPD_PLUG	0x0088	HPD Plug Event Register
EDP_HPD_EN	0x008C	HPD Plug EN Register
EDP_CAPACITY	0x0100	Capacity Register
EDP_ANA_PLL_FBDIV	0x0180	CORE Pll Fbdiv Register
EDP_ANA_PLL_FRAC	0x0184	Core Pll Frac Register
EDP_ANA_PLL_POSDIV	0x0188	Core Pll Postdiv Register
EDP_ANA_PIXELPLL_FBDIV	0x0190	Pixel Pll Feedback Divide Register
EDP_ANA_PIXELPLL_DIV	0x0194	Pixel Pll Divider Register
EDP_ANA_PIXELPLL_FRAC	0x019C	Pixel Pll Frac Register
EDP_TX32_ISEL_DRV	0x01A4	Lane 32 Current Bias Control Register
EDP_TX_MAINSEL	0x01A8	Output Voltage Control Register
EDP_TX_POSTSEL	0x01AC	Post-cursor Pre-Emphasis Register
EDP_TX_PRESEL	0x01B0	Pre-cursor Pre-Emphasis Register
EDP_TX_RCAL_SEL	0x01C0	The Resistance Calibration Register
EDP_VIDEO_STREAM_EN	0x0200	Video_Stream Enable Register
EDP_SYNC_POLARITY	0x020C	Polarity of Hsync and Vsync Register
EDP_HACTIVE_BLANK	0x0210	H acitve and Blank Register
EDP_VACTIVE_BLANK	0x0214	V acitve and Blank Register
EDP_HWIDTH_FRONT_PORCH	0x0218	Hs Width and H Front Porch Register
EDP_VWIDTH_FRONT_PORCH	0x021C	Vs Width and V Front Porch Register
EDP_FRAME_UNIT	0x0220	Transfer Unit Register
EDP_SYNC_START	0x0224	Vstart and Hstart Register
EDP_MSA_MISC0	0x0228	MSA Miscellaneous0 Field Register
EDP_MSA_MISC1	0x022C	MSA Miscellaneous1 Field Register
EDP_HBLAN_LINK_CYC	0x0230	Hblank Link CYC Register
EDP_AUDIO	0x0300	Audio Register

Register Name	Offset	Description
EDP_PHY_AUX	0x0400	Phy Aux Register
EDP_AUX_TIMEOUT	0x0404	Aux Timeout Register
EDP_AUX_DATA1	0x0408	Aux Data1 Register
EDP_AUX_DATA2	0x040C	Aux Data2 Register
EDP_AUX_DATA3	0x0410	Aux Data3 Register
EDP_AUX_DATA4	0x0414	Aux Data4 Register
EDP_AUX_START	0x0418	Aux Write/Read Request Start register
EDP_AUDIO_VBLANK_EN	0x0500	Audio Vblank Transmit Register
EDP_AUDIO_HBLANK_EN	0x0504	Audio Hblank Transmit Register
EDP_BIST_CFG	0x2010	EDP Bist Control Register
EDP_RES1000_CFG	0x2014	EDP Res 1000 Config Register

6.1.4 Register description

6.1.4.1 0x0018 EDP HPD Scale Register (default value 32’h0800_0000)

Offset: 0x0018			Register Name: EDP_HPD_SCALE
Bit	Read/Write	Default/Hex	Description
31:4	R/W	0	/
3	R/W	0	REG_HPD_SCALE Scaling HPD Counter for Fast Simulation 0: Normal 1: Scaling
2:0	/	/	/

6.1.4.2 0x001C EDP Reset Register (default value 32’h0000_0000)

Offset: 0x001C			Register Name: EDP_RST
Bit	Read/Write	Default/Hex	Description
31:4	R/W	0	/
3	R/W	0	REG_RESET_AUDIO 0: Normal 1: Reset
2	/	/	/
1	R/W	0	REG_RESET_PHY Reset PHY Logic 0: Normal 1: Reset
0	/	/	/

6.1.4.3 0x0080 EDP HPD Event Register (default value 32’ h0000_0000)

Offset: 0x0080			Register Name: EDP_HPD_EVENT
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0	STA_AUX_REPLY_EVENT
0	R	0	STA_HPD_EVENT HPD event, can be cleared by STA_HPD_PLUG

6.1.4.4 0x0084 EDP HPD Interrupt Register (default value 32’ h0000_0000)

Offset: 0x0084			Register Name: EDP_HPD_INT
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0	Enable_aux_reply_event
0	R/W	0	ENABLE_HPD_PLUG_EVENT 1’b1 : Enable HPD plug interrupt

6.1.4.5 0x0088 EDP HPD Plug Register (default value 32’ h0000_0000)

Offset: 0x0088			Register Name: EDP_HPD_PLUG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0	HDP disconnection event, and this bit can be cleared by writing 1’b1.
1	R/W	0	STA_HPD_PLUG HPD Plug event, can be clear by write 1’b1
0	/	/	/

6.1.4.6 0x008C EDP HPD Enable Register (default value 32’ h0000_0000)

Offset: 0x008C			Register Name: EDP_HPD_EN
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0	HPD_PLUG_EN 1’b1:enable HPD plug event to assert the interrupt output
0	/	/	/

6.1.4.7 0x0100 EDP Capacity Register (default value 32’ h8001_0000)

Offset: 0x0100			Register Name: EDP_CAPACITY
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:26	R/W	0	EDP_PHY_RATE Rate Set for PHY. 3’b000: PHY rate setting by reg0x0100[5:4] 3’b001:2.16G 3’b010:2.43G
25:12	/	/	/
11:8	R/W	0	Transmit Enable Enable transmitter on the per lane. Bit8: lane 0 Bit9: lane 1 Bit10: lane 2 Bit11: lane 3
7:6	R/W	0	PHY_LANES number of lanes active: 2’b00:1 lane 2’b01:2 lanes 2’b10:4 lanes
5:4	R/W	0	PHY_RATE rate set for the PHY. 2’b00: RBR 1.62 G 2’b01: HBR 2.7G 2’b10/2’b11:reserved
3:0	R/W	0	TPS_SEL selects the training pattern. 0000: No training pattern. Normal stream data is transmitted instead. 0001: TPS1 0010: TPS2 0011: TPS3 0100: TPS4 0110: PRBS7 Others: Reserved

6.1.4.8 0x0180 EDP Analog Core PLL1 Register (default value 32’ h5830_0130)

Offset: 0x0180			Register Name: EDP_ANA_PLL_FBDIV
Bit	Read/Write	Default/Hex	Description
31:24	R/W	8’h58	REG_COREPLL_FBDIV [7:0]

Offset: 0x0180			Register Name: EDP_ANA_PLL_FBDIV
Bit	Read/Write	Default/Hex	Description
			CORE PLL feedback divide value
23:22	/	/	/
21	R/W	1	REG_DISABLE_SSCG 1'b0: Enable SSC 1'b1: Disable SSC
20	R/W	1	REG_DOWNSPREAD 1'b0: Center spread 1'b1: Down spread
19:16	R/W	0	EG_COREPLL_FBDIV [11:8] CORE PLl Feedback Divide Value
15:14	/	/	/
13:8	R/W	1	DA_COREPLL_PREDIV [5:0] CORE PLL Reference Divide Value
7:6	/	/	/
5:4	R/W	2'b11	DA_COREPLL_FRAC_PD [1:0] Fractional Divider Control Register
3:1	/	/	/
0	R/W	0	REG_COREPLL_PD 1: power down pixel PLL

6.1.4.9 0x0184 EDP Analog Core PLL2 Register (default value 32' h2200_0000)

Offset: 0x0184			Register Name: EDP_ANA_PLL_FRAC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	REG_COREPLL_FRAC [7:0] The fractional part of CORE PLL feedback divide value
15:8	R/W	0	REG_COREPLL_FRAC [15:8] The fractional part of CORE PLL feedback divide value
7:0	R/W	0	REG_COREPLL_FRAC [23:16] The fractional part of CORE PLL feedback divide value

6.1.4.10 0x0188 EDP Analog Core Pll3 Register (default value 32' h4700_0090)

Offset: 0x0188			Register Name: EDP_ANA_PLL_POSDIV
Bit	Read/Write	Default/Hex	Description
31	/	/	/

Offset: 0x0188			Register Name: EDP_ANA_PLL_POSDIV
Bit	Read/Write	Default/Hex	Description
30:28	R/W	2'b10	REG_SPREAD [2:0] SSC Modulation Amplitude Control 3'b000: 0 ppm 3'b001: 500 ppm 3'b010: 1000 ppm 3'b011: 2000 ppm 3'b100: 4000 ppm 3'b101: 8000 ppm 3'b110: 16000 ppm 3'b111: 32000 ppm
27:24	R/W	4'b0111	REG_DIVVAL [3:0] SSC modulation frequency control
3:2	R/W	0	DA_COREPLL_POSTDIV [1:0] CORE PLL reference divide value 2'b00: divide by 1 2'b01: divide by 2 2'b10: divide by 4 2'b11: divide by 8
1:0	/	/	/

6.1.4.11 0x018C EDP Analog AUX CLOCK Register (default value 0x0100_0000)

Offset: 0x018C			Register Name: EDP_ANA_AUX_CLOCK
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0	da_corepll_clk_div_16m AUX CLK sources from aux_16m which is divided by bitclock. Because it is an integer division, the configured value makes aux_16M close to 16 MHz. aux_16m=bitclock/8/da_corepll_clk_div_16m

6.1.4.12 0x0190 EDP Analog Pixel Pll1 Register (default value 32' h5000_0430)

Offset: 0x0190			Register Name: EDP_ANA_PIXELPLL_FBDIV
Bit	Read/Write	Default/Hex	Description
31:24	R/W	8'h50	DA_PIXELPLL_FBDIV [7:0] PIXEL PLL feedback divide value
23:20	/	/	/
19:16	R/W	0	DA_PIXELPLL_FBDIV [11:8] PIXEL PLL feedback divide value

Offset: 0x0190			Register Name: EDP_ANA_PIXELPLL_FBDIV
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:8	R/W	4	DA_PIXELPLL_PREDIV [5:0] PIXEL PLL reference divide value
5:4	R/W	2'b11	DA_PIXELPLL_FRAC_PD [1:0] Fractional divider control register
0	R/W	0	REG_PIXELPLL_PD 1: power down pixel PLL

6.1.4.13 0x0194 EDP Analog Pixel Pll2 Register (default value 32' h0101_0001)

Offset: 0x0194			Register Name: EDP_ANA_PIXELPLL_DIV
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	1	PIXEL PLL divider c [4:0] divide by 1-31
15:10	/	/	/
9:8	R/W	0	PIXEL PLL divider b [1:0] 2'b00: divide by 1 2'b01: divide by 2 2'b10: divide by 3 2'b11: divide by 5
7:5	/	/	/
4:0	R/W	1	PIXEL PLL divider a [4:0] divide by 1-31

6.1.4.14 0x019C EDP Analog Pixel Pll3 Register (default value 32' h0000_0000)

Offset: 0x019C			Register Name: EDP_ANA_PIXELPLL_FRAC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	da_pixelpll_frac [7:0] The fractional part of PIXEL PLL feedback divide value
15:8	R/W	0	da_pixelpll_frac [15:8] The fractional part of PIXEL PLL feedback divide value
7:0	R/W	0	da_pixelpll_frac [23:16] The fractional part of PIXEL PLL feedback divide value

6.1.4.15 0x01A4 EDP Current Bias Control Register (default value 32’ h5500_0F0F)

Offset: 0x01A4			Register Name: EDP_TX32_ISEL_DRV
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x5	da_tx_isel_drv_d3[3:0] Current bias control register of lane3. Ibias = 160uA + 40uA * isel[3:0]
27:24	R/W	0x5	da_tx_isel_drv_d2[3:0] Current bias control register of lane2. Ibias = 160uA + 40uA * isel[3:0]

6.1.4.16 0x01A8 EDP TX Voltage Register (default value 32’ h1010_0055)

Offset: 0x01A8			Register Name: EDP_TX_MAINSEL
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	da_tx_mainsel_d2[4:0] Output voltage level control registers of lane2. Imain = Ibias * mainsel[4:0]
20:16	R/W	0x10	da_tx_mainsel_d3[4:0] Output voltage level control registers of lane3. Imain = Ibias * mainsel[4:0]
7:4	R/W	0x5	da_tx_isel_drv_d1[3:0] Current bias control register of lane1. Ibias = 160uA + 40uA * isel[3:0]
3:0	R/W	0x5	da_tx_isel_drv_d0[3:0] Current bias control register of lane0. Ibias = 160uA + 40uA * isel[3:0]

6.1.4.17 0x01AC EDP TX Pre-emphasis1 Register (default value 32’ h0202_1010)

Offset: 0x01AC			Register Name:EDP_TX_POSTSEL
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x2	da_tx_postsel_d1[3:0] Post-cursor pre-emphasis level control registers of lane1. Ipost = Ibias * postsel[3:0]
27:24	R/W	0x2	da_tx_postsel_d0[3:0] Post-cursor pre-emphasis level control registers of lane0. Ipost = Ibias * postsel[3:0]
23:20	R/W	0x2	da_tx_postsel_d3[3:0]

Offset: 0x01AC			Register Name:EDP_TX_POSTSEL
Bit	Read/Write	Default/Hex	Description
			Post-cursor pre-emphasis level control registers of lane3. Ipost = Ibias * postsel[3:0]
19:16	R/W	0x2	da_tx_postsel_d2[3:0] Post-cursor pre-emphasis level control registers of lane2. Ipost = Ibias * postsel[3:0]
12:8	R/W	0x2	da_tx_mainsel_d0[4:0] Output voltage level control registers of lane0. Imain = Ibias * mainsel[4:0]
4:0	R/W	0x2	da_tx_mainsel_d1[4:0] Output voltage level control registers of lane1. Imain = Ibias * mainsel[4:0]

6.1.4.18 0x01B0 EDP TX Pre-emphasis2 Register (Default value 32’ hF000_0000)

Offset: 0x01B0			Register Name:EDP_TX_PRESEL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0	4’b1111: Current regulation, adjust the amplitude by the isel in 0x1A8 and 0x1AC. 4’b0000: Voltage regulation, adjust the amplitude by the mainsel in 0x1A8 and 0x1AC.
23:15	/	/	/
14:12	R/W	0	da_tx_presel_d1[2:0] Pre-cursor pre-emphasis level control registers of lane1. Ipre = Ibias * presel[2:0]
10:8	R/W	0	da_tx_presel_d0[2:0] Pre-cursor pre-emphasis level control registers of lane0. Ipre = Ibias * presel[2:0]
6:4	R/W	0	da_tx_presel_d3[2:0] Pre-cursor pre-emphasis level control registers of lane3. Ipre = Ibias * presel[2:0]
2:0	R/W	0	da_tx_presel_d2[2:0] Pre-cursor pre-emphasis level control registers of lan2. Ipre = Ibias * presel[2:0]

6.1.4.19 0x01C0 EDP Resistance Calibration Register (default value 32’ h020e_8100)

Offset: 0x01C0			Register Name: EDP_TX_RCAL_SEL
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:25	R/W	0x1	reg_bg_rcal_sel [1:0] The resistance calibration, adjust the termination resistor to approach the off-chip reference resistor.
23:16	R/W	0x0e	reg_rtcal_freqdiv [7:0] The resistance calibration clock divider.
15	R/W	0x1	reg_rtcal_bypass Control the configuration method for termination resistance.
14:8	R/W	0x1	reg_rtcal_freqdiv [14:8] The resistance calibration clock divider.
5:0	R/W	0x0	reg_bg_rcal_val [5:0] The resistance calibration result.

6.1.4.20 0x0200 EDP Video Stream Set Register (default value 32’ h0100_0000)

Offset: 0x0200			Register Name: EDP_VIDEO_STREAM_EN
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	1	reg_alt_screamble_reset alternate_scrambler_reset_capable, a setting of 0 indicates that this is an eDP device that can use the eDP alternate scrambler reset value of FFFEh
23:21	/	/	/
20:16	R/W	0	video_mapping the bit width of each color 5’d0: RGB 6bits 5’d1: RGB 8bits 5’d2: RGB 10bits 5’d3: RGB 12bits 5’d4: RGB 16bits 5’d5: YCbCR4:4:4 8bits 5’d6: YCbCr4:4:4 10bits 5’d7: YCbCr4:4:4 12bits 5’d8: YCbCr4:4:4 16bits 5’d9: YCbCR4:2:2 8bits 5’d10: YCbCr4:2:2 10bits

Offset: 0x0200			Register Name: EDP_VIDEO_STREAM_EN
Bit	Read/Write	Default/Hex	Description
			5'd11: YCbCr4:2:2 12bits 5'd12: YCbCr4:2:2 16bits
15:6	/	/	/
5	R/W	0	Video_stream_en 0:vide0 stream disable 1: video stream enable
4:0	/	/	/

6.1.4.21 0x020C EDP Sync Polarity Register (default value 32' h0000_0000)

Offset: 0x020C			Register Name: EDP_SYNC_POLARITY
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0	eg_tx_polarity [1:0] polarity of hsync and vsync. bit1: Hsync polarity bit0: Vsync polarity if the vsync/hsync of simulation video source is active low, then the corresponding bit in reg_tx_polarity should set 0; or active high

6.1.4.22 0x0210 EDP Horizontal Active Blank Register (default value 32' h0280_0280)

Offset: 0x0210			Register Name: EDP_HACTIVE_BLANK
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h0280	reg_tx_hactive [15:0] Active horizontal pixels per line
15:2	R/W	14'hA0	reg_tx_hblank [13:0]/htotal – hactive
1:0	/	/	/

6.1.4.23 0x0214 EDP Vertical Active Blank Register (default value 32' h002D_01E0)

Offset: 0x0214			Register Name: EDP_VACTIVE_BLANK
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h002D	reg_tx_vblank [15:0] vtotal – vactive
15:0	R/W	16'h01E0	reg_tx_vactive [15:0] Active vertical pixels per line

6.1.4.24 0x0218 EDP Horizontal Width Front Porch Register (default value 32’ h0060_0010)

Offset: 0x0218			Register Name: EDP_HWIDTH_FRONT_PORCH
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16’h0060	reg_tx_hswidth [15:0] Hsync width
15:0	R/W	16’h0010	reg_tx_h_front_porch [15:0] htotal – hactive – hstart

6.1.4.25 0x021C EDP Vertical Width Front Porch Register (default value 32’ h0020_000A)

Offset: 0x021C			Register Name: EDP_VWIDTH_FRONT_PORCH
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16’h0060	reg_tx_hswidth [15:0] Hsync width
15:0	R/W	16’h0010	reg_tx_h_front_porch [15:0] htotal – hactive – hstart

6.1.4.26 0x0220 EDP Frame Unit Register (default value 32’ h0280_C796)

Offset: 0x0220			Register Name:EDP_FRAME_UNIT
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0	reg_avg_per_tu_frac fractional portion of average valid symbol per Transfer Unit, calculate formula refer to DP spec. For example, pixel clock is 27M RGB888, @2.7Gbps 4lanes,then average valid symbol per Transfer Unit = 4.8, configure reg_avg_per_tu_frac to 8
15:14	/	/	/
13:7	R/W	7’h0f	reg_line_rd_thres An asynchronous FIFO needed to deal with video data from pixel clock domain to link clock domain, reg_line_rd_thres is related to read enable of FIFO. According to video format and main link rate, this value may changed as following description: reg_line_rd_thres = average valid symbol per TU<6?7'd32: hblank < 80? 7'd12:7'd16;

Offset: 0x0220			Register Name:EDP_FRAME_UNIT
Bit	Read/Write	Default/Hex	Description
6:0	R/W	7'h16	reg_avg_per_tu_int integer portion of average valid symbol per Transfer Unit, calculate formula refer to DP spec. For example, pixel clock is 27M RGB888, @2.7Gbps 4lanes, then average valid symbol per Transfer Unit = 4.8, configure reg_avg_per_tu_int to 4

6.1.4.27 0x0224 EDP Sync Start Register (default value 32' h0023_0090)

Offset: 0x0224			Register Name: EDP_SYNC_START
Bit	Read/Write	Default/Hex	Description
31:16	R/W	16'h0043	reg_tx_vstart [15:0] Vsync width + Vback porch width
15:0	R/W	16'h0090	reg_tx_hstart [15:0] Hsync width + Hback porch width

6.1.4.28 0x0228 EDP MSA MISC0 Register (default value 32' h0000_0000)

Offset: 0x0228			Register Name:EDP_MSA_MISC0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	reg_tx_msa_misc0[7:0] MSA Miscellaneous0 field bit0: 1'b0, IP Link clock and main video stream clock asynchronous. tips: the bit must set 1'b0. bit1-bit7: color encoding format, please refer to DP spec for example: 6'b0000000, 6'b 0010000, 6'b 0100000, 6'b 0110000, 6'b 1000000 (6,8, 10, 12, 16 bits/color respectively)
23:0	/	/	/

6.1.4.29 0x022C EDP MSA MISC1 Register (default value 32' h0000_0000)

Offset: 0x022C			Register Name:EDP_MSA_MISC1
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	reg_tx_msa_misc1[7:0]

Offset: 0x022C			Register Name:EDP_MSA_MISC1
Bit	Read/Write	Default/Hex	Description
			MSA Miscellaneous1 field please refer to DP spec
23:0	/	/	/

6.1.4.30 0x0230 EDP Horizontal Blank Link Cycle Register (default value 32’ h0000_005A)

Offset: 0x0230			Register Name: EDP_HBLAN_LINK_CYC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	16’h005A	hblank_link_cyc How many link clock cycles of hblank. hblank *link_clk/pixel_clk, For example, pixel clock is 27M hblank 138, @2.7Gbps 4lanes, hblank_link_cyc = 138*67.5/27. link_clk = symbol clock /4

6.1.4.31 0x0300 EDP Audio Register (default value 32’ h1200_1A02)

Offset: 0x0300			Register Name:EDP_AUDIO
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0	audio_mute 1’b1: Sets the AudioMute_Flag in VB-ID 1’b0: Clears the AudioMute_Flag in VB-ID.
14:12	R/W	1	audio_channel_num Number of audio channels. 3’b000:1 channel 3’b001:2 channel Others:8 channel
11:10	/	/	/
9:5	R/W	5’h10	audio_data_width Indicates the bit width of the data samples at input. 5’b10000: 16 bits 5’b10100: 20 bits 5’b11000: 24 bits
4:1	R/W	1	audio_data_en Indicates whether the input data is valid. Bit 1: indicates whether the channels 1,2 input data is valid.

Offset: 0x0300			Register Name:EDP_AUDIO
Bit	Read/Write	Default/Hex	Description
			Bit 2: indicates whether the channels 3,4 input data is valid. Bit 3: indicates whether the channels 5,6 input data is valid. Bit 4: indicates whether the channels 7,8 input data is valid. tips: must be consistent with audio_channel_num(0x0300[14:12])
0	R/W	0	Audio_interface_sel 1'b0: select I2S as input(default) 1'b1:select OWA as input

6.1.4.32 0x0400 EDP AUX Command Register (default value 32' h0000_0000)

Offset: 0x0400			Register Name:EDP_PHY_AUX
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0	cfg_phy_aux_enc_cmd [31:0] CMD(4bits)
27:8	R/W	0	addr(20bits)
7:4	/	/	/
3:0	R/W	0	len(4bits)

6.1.4.33 0x0404 EDP AUX Reply Register (default value)

Offset: 0x0404			Register Name: EDP_AUX_TIMEOUT
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	/	aux_timeout as described in spec, TX must wait for a Reply Time-out period of 400us before initiating the next AUX Request transaction. When timeout, this bit will set to 1
16	R	/	Aux_reply_received 1'b1: waiting for AUX_REPLY 1'b0: received AUX_REPLY
15:8	/	/	/
7:4	R	/	Aux_reply_cmd 4'b0000: ack 4'b0001:nack
3:0	/	/	/

6.1.4.34 0x0408 EDP AUX Data1 Register (default value 32’ h0000_0000)

Offset: 0x0408			Register Name:EDP_AUX_DATA1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	cfg_phy_aux_data [127:0], composed of 16’h0408, 16’h040C, 16/h0410, 16’h0414, totally 16bytes, including data(8bits*16), payload for write request or read request. tips: for a write request, filled attached data needs to be transmitted for a read reply, stored the replied data write request: cfg_phy_aux_data [31:0]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [7:0]: write to DPCD address+0 as the byte0 cfg_phy_aux_data [31:24]: write to DPCD address+3 as the byte3 read reply: cfg_phy_aux_data [31:0]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [7:0]: read from DPCD address+0 as the byte0 cfg_phy_aux_data [31:24] read from DPCD address+3 as the byte3

6.1.4.35 0x040C EDP AUX Data2 Register (default value 32’ h0000_0000)

Offset: 0x040C			Register Name:EDP_AUX_DATA2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	write request: cfg_phy_aux_data [63:32]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [39:32]: write to DPCD address+4 as the byte4 cfg_phy_aux_data [63:56]: write to DPCD address+7 as the byte7

Offset: 0x040C			Register Name:EDP_AUX_DATA2
Bit	Read/Write	Default/Hex	Description
			read reply: cfg_phy_aux_data [63:32]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [39:32]: read from DPCD address+4 as the byte4 cfg_phy_aux_data [63:56] read from DPCD address+7 as the byte7

6.1.4.36 0x0410 EDP AUX Data3 Register (default value 32’h0000_0000)

Offset: 0x0410			Register Name:EDP_AUX_DATA3
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	write request: cfg_phy_aux_data [95:64]: the data to be transfer by AUX requester, please refer to Native AUX syntax of DP spec. For example: cfg_phy_aux_data [71:64]: write to DPCD address+8 as the byte8 cfg_phy_aux_data [95:88]: write to DPCD address+11 as the byte11 read reply: cfg_phy_aux_data [95:64]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [71:64]: read from DPCD address+8 as the byte8 cfg_phy_aux_data [95:88] read from DPCD address+11 as the byte11

6.1.4.37 0x0414 EDP AUX Data4 Register (default value 32’h0000_0000)

Offset: 0x0414			Register Name:EDP_AUX_DATA4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	write request: cfg_phy_aux_data [127:96]: the data to be transfer by AUX requester, please refer to

Offset: 0x0414			Register Name:EDP_AUX_DATA4
Bit	Read/Write	Default/Hex	Description
			Native AUX syntax of DP spec. For example, cfg_phy_aux_data [103:96]: write to DPCD address+12 as the byte12 cfg_phy_aux_data [127:120]: write to DPCD address+15 as the byte15 read reply: cfg_phy_aux_data [127:96]: the data to be replied by sink device, please refer to Native AUX syntax of DP spec. For example, cfg_phy_aux_data [103:96]: read from DPCD address+12 as the byte12 cfg_phy_aux_data [127:120] read from DPCD address+15 as the byte15

6.1.4.38 0x0418 EDP AUX Start Register (default value 32’ h0000_0000)

Offset: 0x0418			Register Name:EDP_AUX_START
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	W/R	0	cfg_phy_aux_start the trigger signal to start a write/read request by AUX requester (Source to Device), write 0 or 1.

6.1.4.39 0x0500 EDP Audio Vertical Blank Enable Register (default value 32’ h0000_0000)

Offset: 0x0500			Register Name: EDP_AUDIO_VBLANK_EN
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	W/R	0	sdp_audio_stream_vertical_en 1’b1: Enable audio stream is transmitted during vertical blanking period.
0	W/R	0	sdp_audio_timestamp_vertical_en 1’b1: Enable send audio timestamp SDP once every video frame during vertical blanking period.

6.1.4.40 0x0504 EDP Audio Horizontal Blank Enable Register (default value 32’h0000_0000)

Offset: 0x0504			Register Name: EDP_AUDIO_HBLANK_EN
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	W/R	0	sdp_audio_stream_horizontal_en 1’b1: Enable audio stream is transmitted during horizontal blanking period.
0	W/R	0	sdp_audio_timestamp_horizontal_en 1’b1: Enable send audio timestamp SDP once every video frame during horizontal blanking period

6.1.4.41 0x2010 EDP Bist Configuration Register (default value 32’h0000_0000)

Offset: 0x2010			Register Name: EDP_BIST_CFG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0	Bist test pass flag
4	R	0	Bist test done flag
3:2	/	/	/
1	W/R	0	Bist test enable
0	W/R	0	Bist test select

6.1.4.42 0x2014 EDP RES1000 Configuration Register (default value 32’h0000_0033)

Offset: 0x2014			Register Name:EDP_RES1000_CFG
Bit	Read/Write	Default/Hex	Description
31:9	R/W	0x0	Reserved
8	R/W	0x0	reg_sel,1000ohms resistor manual control enable,0:disable 1,enable
7:6	R/W	0x0	Reserved
5:0	R/W	0x33	di_reg[5:0], 1000ohms resistor manual control bits

6.2 MIPI DSI

The Display Serial Interface is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.02 and a D-PHY module which is compliance with MIPI DPHY specification V1.1.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI V1.02
- Up to 1.5 Gbit/s for each lane
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports 4+4-lane MIPI DSI, up to 2560 x 1600@60fps
- Supports non-burst mode with sync pulse/sync event and burst mode
- Pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Continuous and non-continuous lane clock modes
- Generic commands support bidirectional communication in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Supports hardware checksum

6.3 TCON LCD

6.3.1 Overview

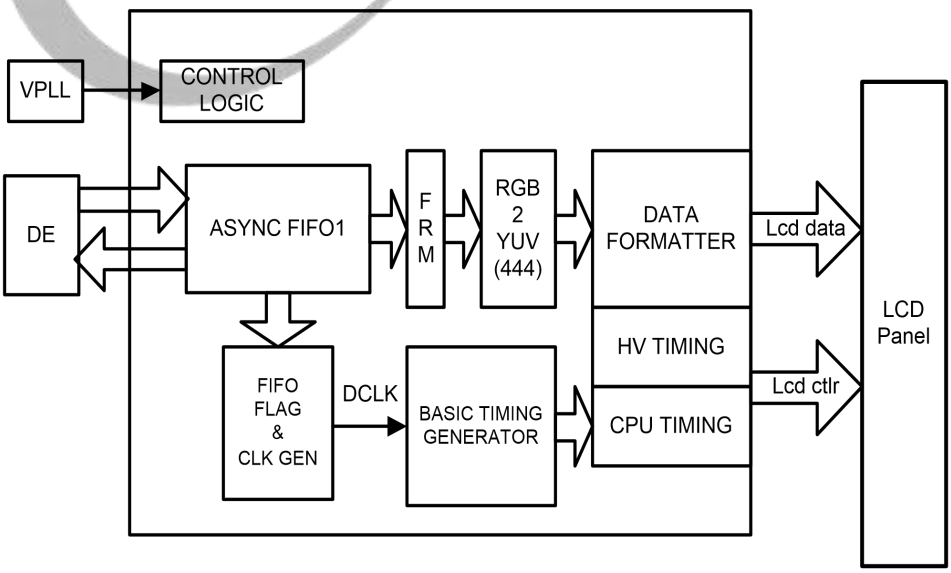
The Timing Controller_LCD (TCON_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- Two TCON LCD controllers: TONC_LCD0 and TCON_LCD1
- TCON_LCD0 supports the following
  - Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
  - Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps
  - Supports LVDS interface with dual link, up to 1920 x 1080@60fps
  - Supports LVDS interface with single link, up to 1366 x 768@60fps
  - Dither function for RGB888, RGB666, and RGB565
  - Supports i8080 interface, up to 800 x 480@60fps
  - Supports BT.656 interface for NTSC and PAL
  - Supports MIPI DSI interface with dual link, up to 2560x1600@60fps
  - Supports MIPI DSI interface with single link, up to 1920x1200@60fps
- TCON_LCD1 supports MIPI DSI interface with single link, up to 1920x1200@60fps

6.3.2 Block Diagram

Figure 6-1 TCON_LCD Block Diagram



6.3.3 Functional Description

6.3.3.1 External Signals

The following table describes the external I/O signals of LCD and LVDS.

Table 6-5 TCON_LCD External Signals

Signal Name	Description	Type
LCD0-D[23:0]	LCD Data Input/Output	I/O
LCD0-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD0-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD0-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD0-DE	LCD Data Output Enable	O
LCD0-TRIG	LCD0 Sync It is input from peripherals for sync	I
LCD1-TRIG	LCD1 Sync It is input from peripherals for sync	I
LVDS0-D[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	AO
LVDS0-D[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	AO
LVDS0-CKN	LVDS0 Negative Port of Clock	AO
LVDS0-CKP	LVDS0 Positive Port of Clock	AO
LVDS1-D[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	AO
LVDS1-D[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	AO
LVDS1-CKN	LVDS1 Negative Port of Clock	AO
LVDS1-CKP	LVDS1 Positive Port of Clock	AO

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

Table 6-6 The Correspondence between LCD and RGB

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0-D23	R4	R5	R7
LCD0-D22	R3	R4	R6
LCD0-D21	R2	R3	R5
LCD0-D20	R1	R2	R4
LCD0-D19	R0	R1	R3
LCD0-D18	-	R0	R2
LCD0-D17	-	-	R1
LCD0-D16	-	-	R0
LCD0-D15	G5	G5	G7

LCD I/O	Parallel RGB I/O		
	RGB565	RGB666	RGB888
LCD0-D14	G4	G4	G6
LCD0-D13	G3	G3	G5
LCD0-D12	G2	G2	G4
LCD0-D11	G1	G1	G3
LCD0-D10	G0	G0	G2
LCD0-D9	-	-	G1
LCD0-D8	-	-	G0
LCD0-D7	B4	B5	B7
LCD0-D6	B3	B4	B6
LCD0-D5	B2	B3	B5
LCD0-D4	B1	B2	B4
LCD0-D3	B0	B1	B3
LCD0-D2	-	B0	B2
LCD0-D1	-	-	B1
LCD0-D0	-	-	B0

The multiplex relationship among LCD, LVDS, and DSI is shown as follows.

Table 6-7 The Correspondence among LCD, LVDS, and DSI.

LCD I/O	LVDS I/O	DSI I/O
LCD0-D0	/	/
LCD0-D1	/	/
LCD0-D2	LVDS0-D0P	DSI0-D0P
LCD0-D3	LVDS0-D0N	DSI0-D0N
LCD0-D4	LVDS0-D1P	DSI0-D1P
LCD0-D5	LVDS0-D1N	DSI0-D1N
LCD0-D6	LVDS0-D2P	DSI0-CKP
LCD0-D7	LVDS0-D2N	DSI0-CKN
LCD0-D8	/	/
LCD0-D9	/	/
LCD0-D10	LVDS0-CKP	DSI0-D2P
LCD0-D11	LVDS0-CKN	DSI0-D2N
LCD0-D12	LVDS0-D3P	DSI0-D3P
LCD0-D13	LVDS0-D3N	DSI0-D3N
LCD0-D14	LVDS1-D0P	DSI1-D0P
LCD0-D15	LVDS1-D0N	DSI1-D0N
LCD0-D16	/	/
LCD0-D17	/	/
LCD0-D18	LVDS1-D1P	DSI1-D1P
LCD0-D19	LVDS1-D1N	DSI1-D1N
LCD0-D20	LVDS1-D2P	DSI1-CKP

LCD I/O	LVDS I/O	DSI I/O
LCD0-D21	LVDS1-D2N	DSI1-CKN
LCD0-D22	LVDS1-CKP	DSI1-D2P
LCD0-D23	LVDS1-CKN	DSI1-D2N
LCD0-CLK	LVDS1-D3P	DSI1-D3P
LCD0-DE	LVDS1-D3N	DSI1-D3N
LCD0-HSYNC	/	/
LCD0-VSYNC	/	/

6.3.3.2 Clock Sources

The following table describes the clock sources of TCON_LCD.

Table 6-8 TCON_LCD Clock Sources

Clock sources	Description	Module
PLL_VIDEO0(3x)	By default, PLL_VIDEO0(4x) is 1188 MHz, PLL_VIDEO0(3x) is 792MHz.	CCU
PLL_VIDEO0(4x)		
PLL_VIDEO1(3x)	By default, PLL_VIDEO1(4x) is 1188 MHz, PLL_VIDEO1(3x) is 792MHz.	
PLL_VIDEO1(4x)		
PLL_VIDEO2(4x)	By default, PLL_VIDEO2(4x) is 1188 MHz.	
PLL_VIDEO3(4x)	By default, PLL_VIDEO3(4x) is 1188 MHz.	
PLL_PERI0(2x)	By default, PLL_PERI0(2x) is 1.2 GHz.	

6.3.3.3 Control signal and data port mapping

		SYNC RGB				YUV		DC	CPU Cmd	CPU 18-bit	CPU 18-bit							CPU 16-bit	CPU 18-bit							LVDS		DSI	
External I/O	Internal pin	Para	Serial RGB			BT656	BT601	YUV422		256K	256K							64K	256K			64K		256K		Single Link		DSI 0	DSI1
			1st	2nd	3rd						1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd	LVDS0	LVDS1		
LCD0_VSYNC	IO0	VSYNC					VSYNCC	VSYNC	CS																				
LCD0_HSYNC	IO1	HSYNC					HSYNC		RD																				
LCD0_CLK	IO2	DCLK				PCLK	DCLK	DCLK	WR																		D3N		D3N
LCD0_DE	IO3	DE					DE	HSYNC	RS																		D3P		D3P
LCD0_D23	D23	R7							D23	R5	R5	B5	G5	R5		R5	B5	R4									CKN		D2N
LCD0_D22	D22	R6							D22	R4	R4	B4	G4	R4		R4	B4	R3									CKP		D2P
LCD0_D21	D21	R5							D21	R3	R3	B3	G3	R3		R3	B3	R2									D2N		CKN
LCD0_D20	D20	R4							D20	R2	R2	B2	G2	R2		R2	B2	R1									D2P		CKP
LCD0_D19	D19	R3							D19	R1	R1	B1	G1	R1		R1	B1	R0									D1N		D1N
LCD0_D18	D18	R2							D18	R0	R0	B0	G0	R0		R0	B0	G5									D1P		D1P
LCD0_D17	D17	R1							D17																		D0N		D0N
LCD0_D16	D16	R0							D16																		D0P		D0P
LCD0_D15	D15	G7							D15	G5								G4											
LCD0_D14	D14	G6							D14	G4								G3											
LCD0_D13	D13	G5							D13	G3																D3N		D3	
LCD0_D12	D12	G4	D71	D72	D73	D7	D7	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2	D3P		D3P	
LCD0_D11	D11	G3	D61	D62	D63	D6	D6	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1	CKN		D2	
LCD0_D10	D10	G2	D51	D52	D53	D5	D5	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0	CKP		D2P	
LCD0_D9	D9	G1							D9																				
LCD0_D8	D8	G0							D8																				
LCD0_D7	D7	B7	D41	D42	D43	D4	D4	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5	D2N		CK	
LCD0_D6	D6	B6	D31	D32	D33	D3	D3	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4	D2P		CK	
LCD0_D5	D5	B5	D21	D22	D23	D2	D2	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3	D1N		D1	
LCD0_D4	D4	B4	D11	D12	D13	D1	D1	D1	D4	B2								B1				G4	B1	G5	B2	D1P		D1P	
LCD0_D3	D3	B3	D01	D02	D03	D0	D0	D0	D3	B1								B0				G3	B0	G4	B1	D0N		D0	
LCD0_D2	D2	B2							D2	B0														G3	B0	D0P		D0P	
LCD0_D1	D1	B1							D1																				
LCD0_D0	D0	B0							D0																				

6.3.3.4 HV interface (Sync+DE mode)(Only for TCON_LCD0)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are defined as:

Table 6-9 HV Panel Signals

Signal Name	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
DE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

Figure 6-2 HV Interface Vertical Timing

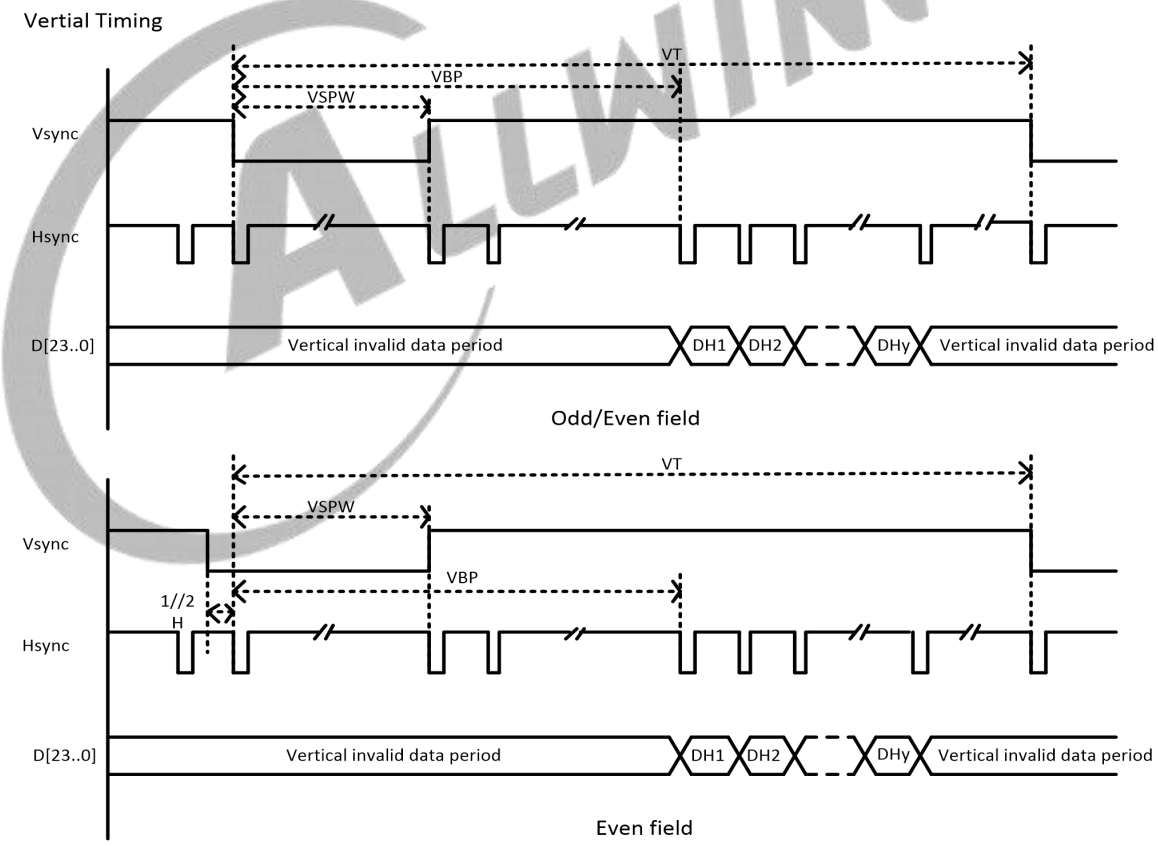
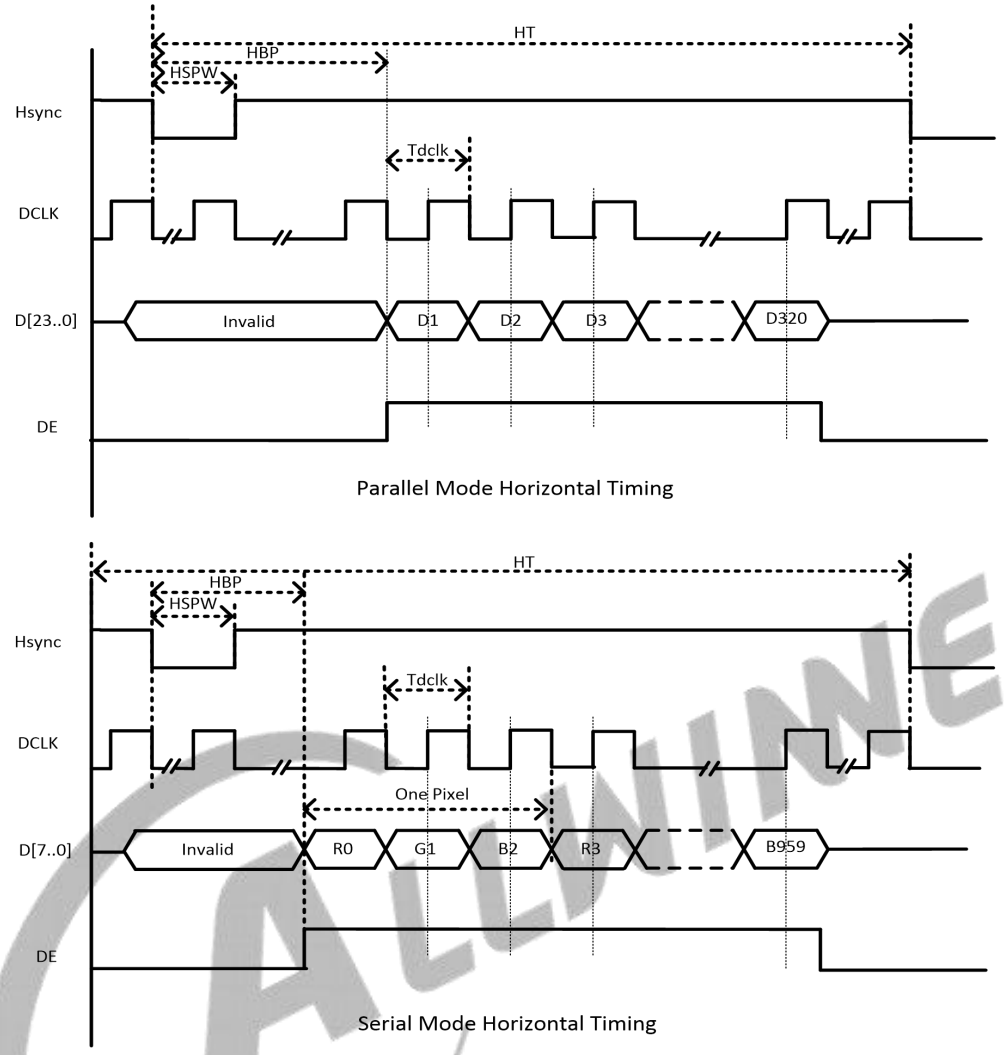
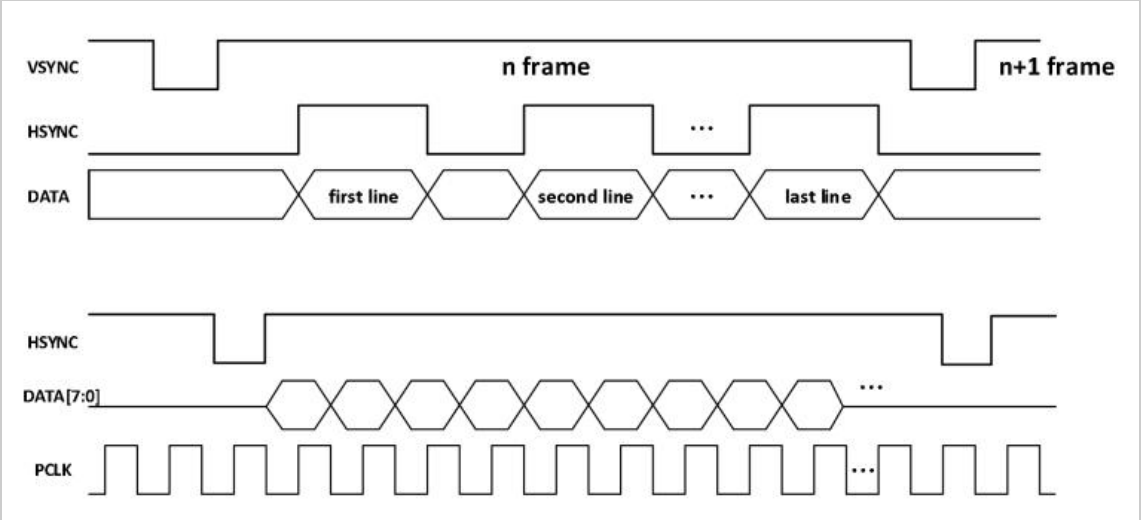


Figure 6-3 HV Interface Horizontal Timing



6.3.3.5 DC (Digital Camera) Interface (Only for TCON_LCD0)

Figure 6-46-5 DC Interface Timing



6.3.3.6 BT.656 Interface (Only for TCON_LCD0)

When the data in YUV format is transmitted in HV mode, TCON_LCD0 needs to use ITU-R BT.656 protocol. Compared with standard CSI interface, there are not synchronous signals, such as FIELD, VSYN, and HSYN, for BT.656 interface. The horizontal and vertical synchronization information of images are built in the BT.656 data stream. BT.656 data format only includes PCLK signal, DVLD signal (unnecessary), and data bus signal. The BT.656 protocol provides 8-bit width and interlaced data of YUV422 format. The encoding format for each line is as follows:

Line=End of Active Video (EAV) + horizontal blanking data (80H/10H) + Start of Active Video (SAV) + valid data (UYVY)

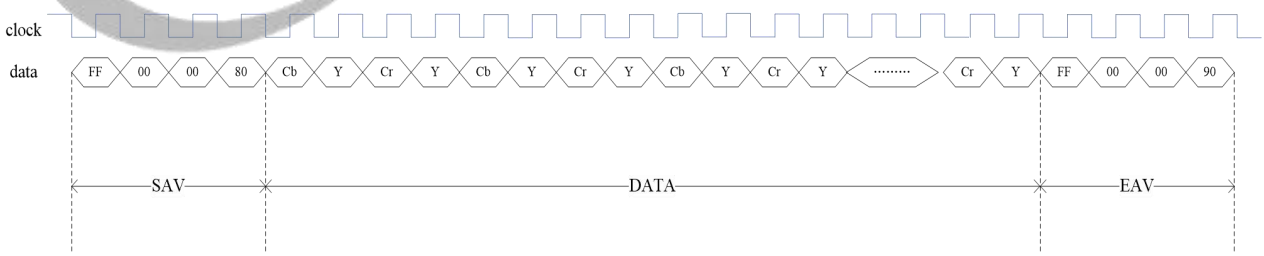
Both of EAV and SAV consist of a 4-bytes sequence in the following format: FF 00 00 XY. The first three bytes are fixed as hexadecimal 8'hFF 8'h00 8'h00. The fourth byte of XY is used to control the format. The assignment of the XY bit is shown in the following table.

Table 6-10 Analysis of XY Signal

BIT	7	6	5	4	3	2	1	0
XY	1'b1	F	V	H	P3	P2	P1	P0
F	0: during field 1 1: during field 2							
V	1: during field blanking 0: field active							
H	0: in SAV 1: in EAV							
P3-P0	protection bits. Single channel: P3=V^H，P2=F^H，P1=F^V，P0=F^V^H Multi-Channel: Channel ID							

During single-channel data transmission, P3-P0 is used for calibration. The transmission timing is shown in the following figure.

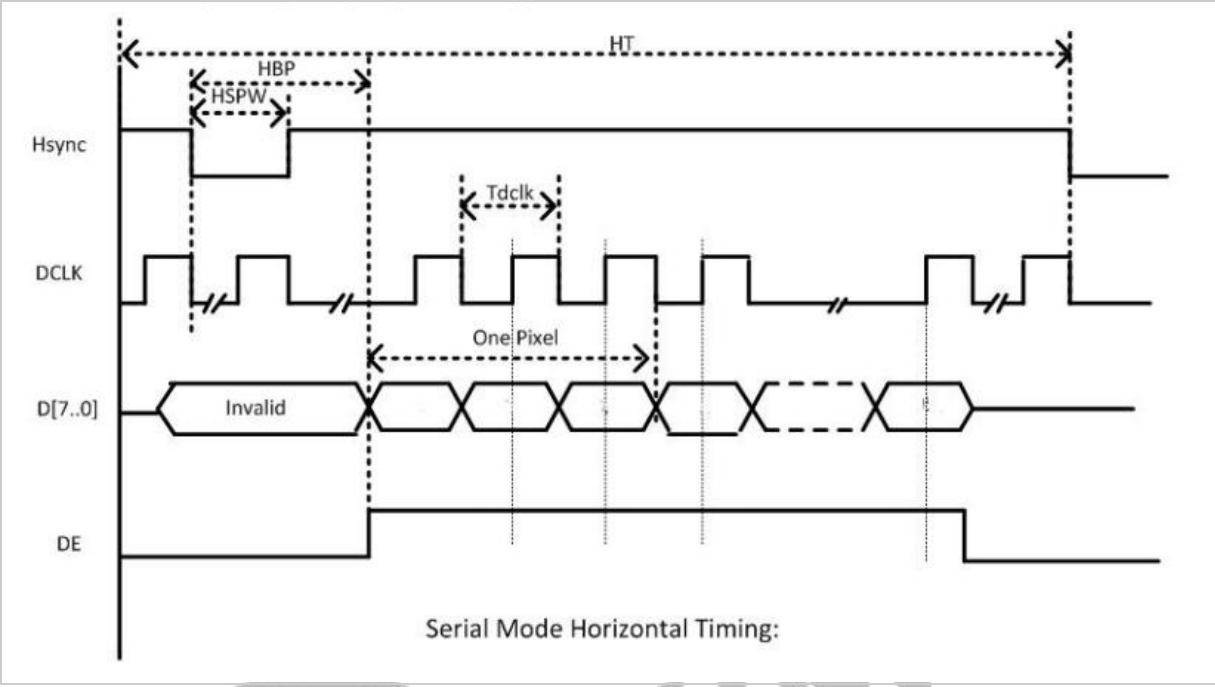
Figure 6-6 Singl-channel Transmission Timing



In programming, the final output format is finished in rgb2yuv, which means the 8-bit data format output by rgb2yuv is the format shown above. ctrl_data_out just inplement the pin-mapping of the data.

6.3.3.7 BT.601 Interface (Only for TCON_LCD0)

Figure 6-7 BT.601 Interface Timing



6.3.3.8 i8080 Interface (Only for TCON_LCD0)

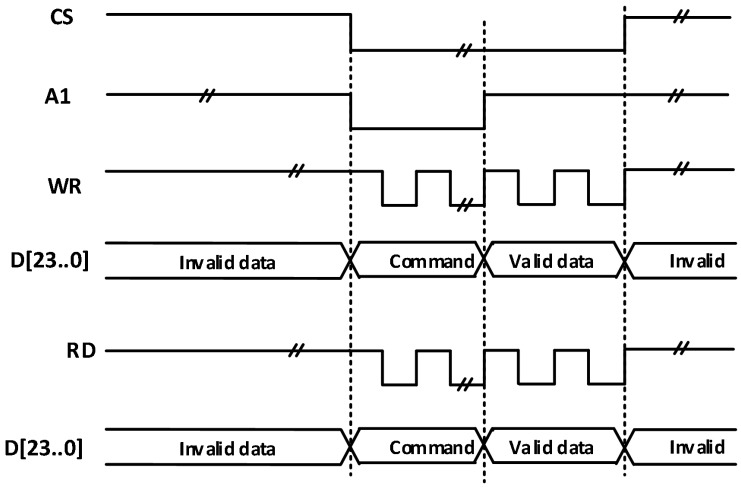
The i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. The CPU control signals are active low.

Table 6-11 CPU Panel Signals

Signal Name	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180o delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

Figure 6-8 i8080 Interface Timing



When CPU I/F is in IDLE state, it can generate WR/RD timing by setting “Lcd_CPUI/F”. The CS strobe is one DCLK width, and the WR/RD strobe is half DCLK width.

6.3.3.9 LVDS Interface (Only for TCON_LCD0)

Table 6-12 LVDS Panel Signals

Signal Name	Description	Type
CKP	The positive port of clock	O
CKN	The negative port of clock	O
D0P	The positive port of data channel 0	O
D0N	The negative port of data channel 0	O
D1P	The positive port of data channel 1	O
D1N	The negative port of data channel 1	O
D2P	The positive port of data channel 2	O
D2N	The negative port of data channel 2	O
D3P	The positive port of data channel 3	O
D3N	The negative port of data channel 3	O

NOTE

A523 adopts 7:1 LVDS interface.

The following figures show the timing of LVDS interface.

Figure 6-9 LVDS Single Link JEDIA Mode Interface Timing

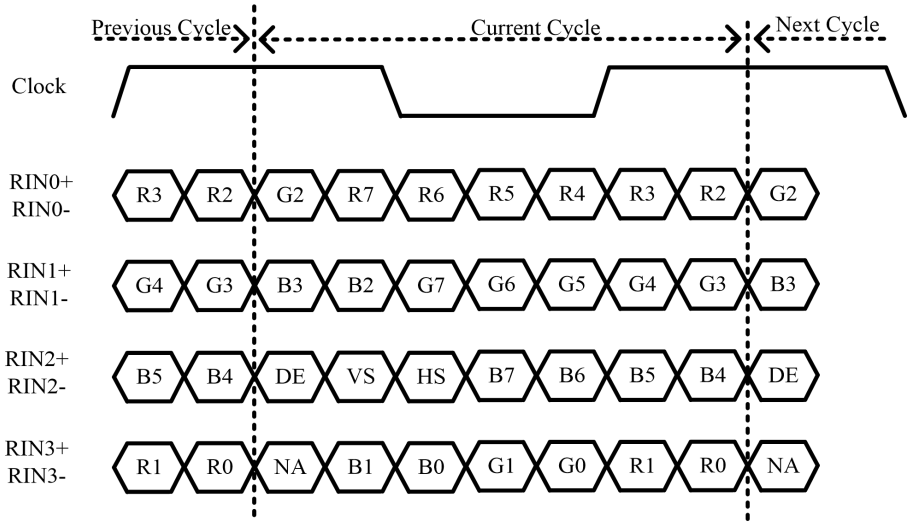
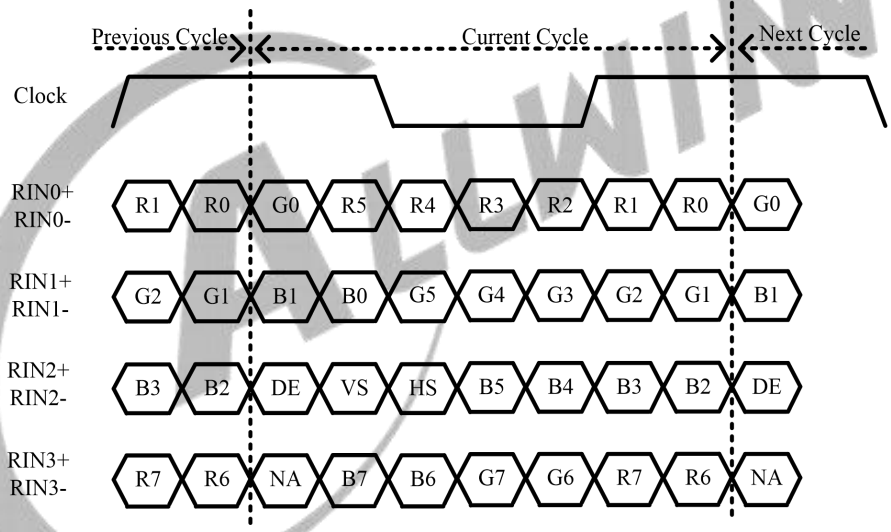
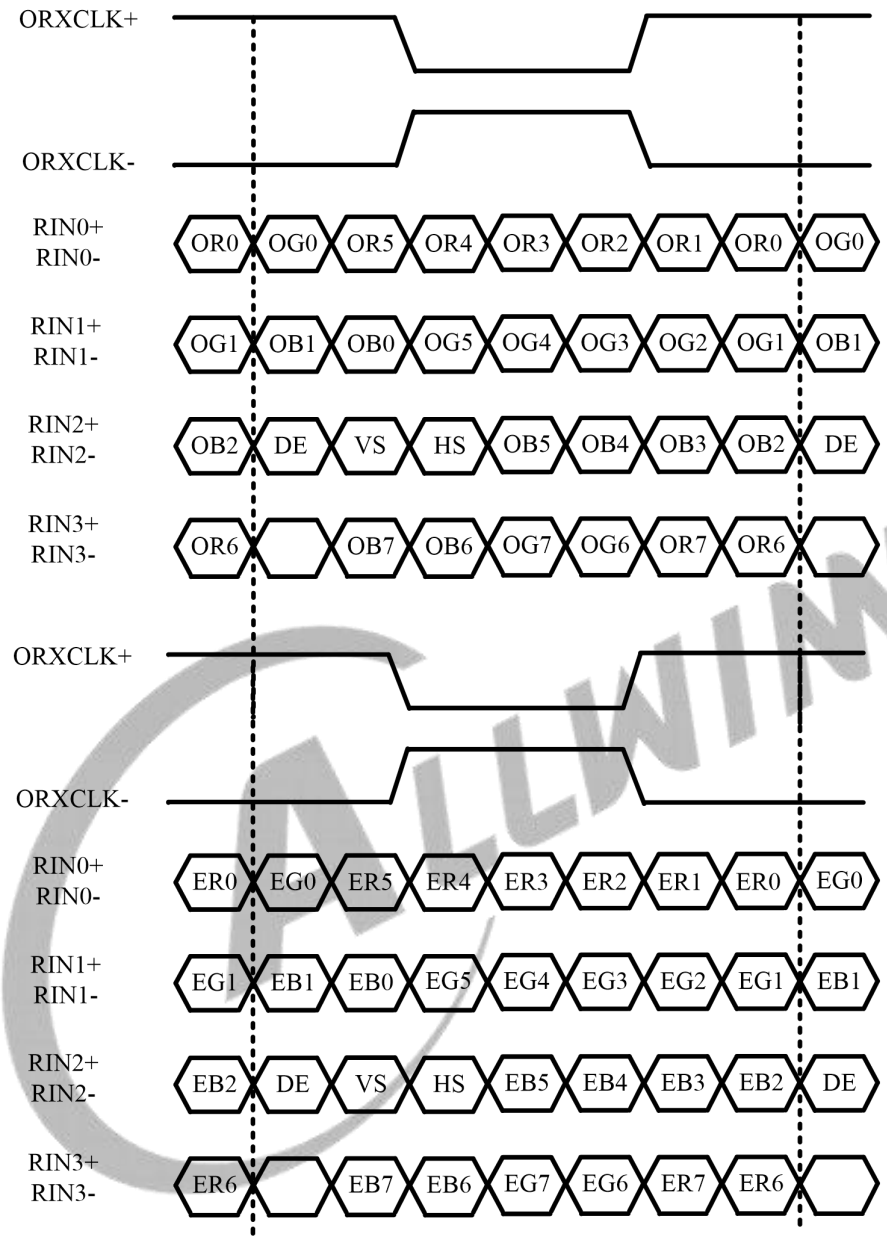


Figure 6-10 LVDS single link NS Mode interface timing



The following figure shows the timing of one mode of the dual-link LVDS, in which odd pixel channel and even pixel channel output to a single-monitor. Dual-link can be configured in the LVDS_DUAL_CHANEL_SRC_SEL bit (bit [30]) of LCD_LVDS_ANA0_REG register.

Figure 6-11 LVDS Dual Link NS Mode Interface Timing



6.3.3.10 CEU Module (Only for TCON_LCD0)

This module enhances color data from DE .

R′ = Rr*R + Rg*G + Rb*B + Rc

G′ = Gr*R + Gg*G + Gb*B + Gc

B′ = Br*R + Bg*G + Bb*B + Bc

Rr, Rg, Rb, Gr, Gg, Gb, Br, Bg, Bb s13 (-16, 16)

Rc, Gc, Bc	s19 (-16384, 16384)
R, G, B	u8 [0-255]

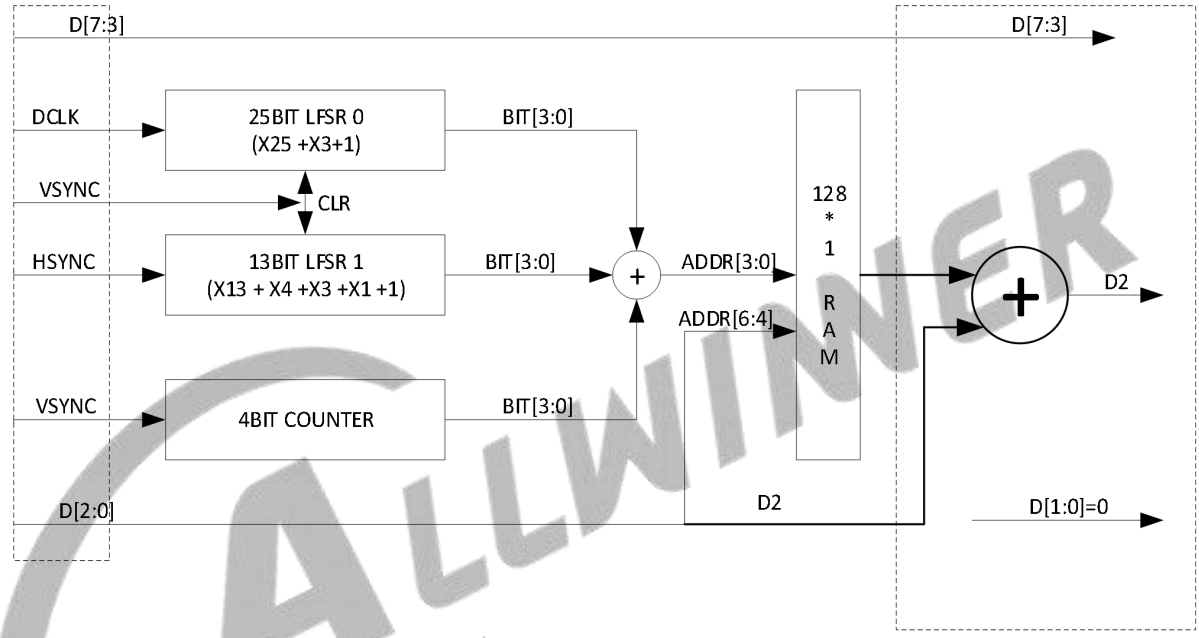
R′ has the range of [Rmin, Rmax]

G′ has the range of [Rmin, Rmax]

B′ has the range of [Rmin, Rmax]

6.3.3.11 FRM Module (Only for TCON_LCD0)

Figure 6-12 FRM Module

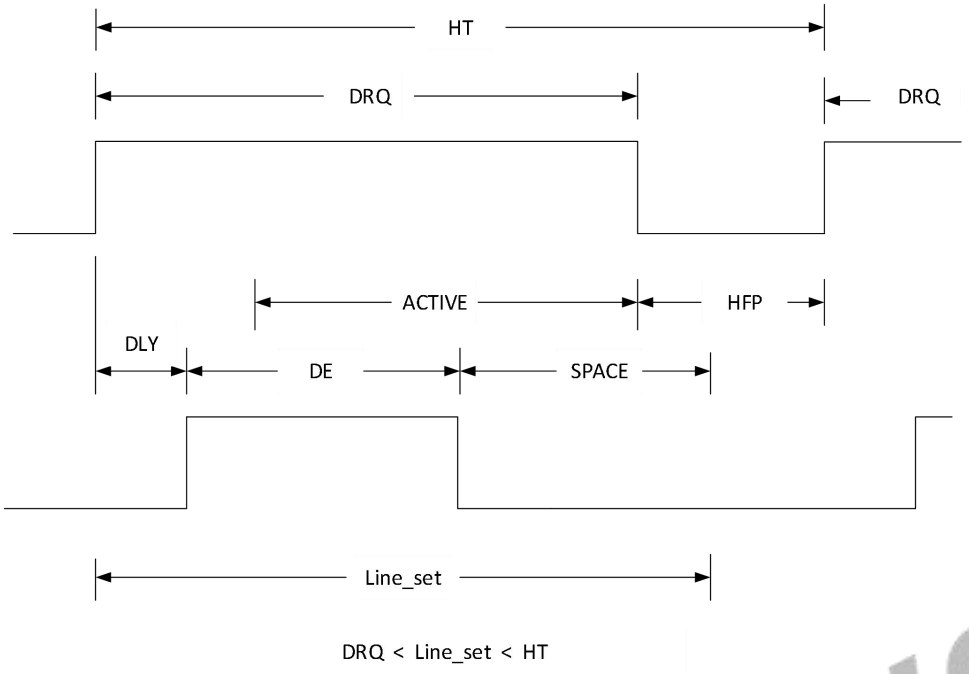


6.3.3.12 MIPI DSI Notes

The requirements on MIPI DSI mode are as follows.

- When using MIPI DSI as display interface, the data clk of TCON needs be started firstly.
- When it is used with DSI video mode, the setting of block space needs to meet the following relationship.

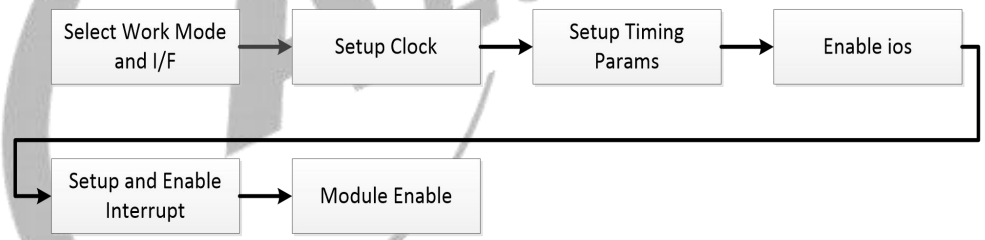
Figure 6-13 The Data Timing of MIPI DSI Video Mode



6.3.4 Programming Guidelines (Only for TCON_LCD0)

6.3.4.1 Enabling HV Mode

Figure 6-14 HV Mode Initial Process



Parallel RGB

Step 1 Select HV interface type

Configure LCD_CTL_REG[LCD_IF] (reg0x40) to 0 to select HV (Sync+DE) mode, and configure LCD_HV_IF_REG[HV_MODE] (reg0x58) to 0 to select 24bit/1cycle parallel mode.

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = 24bit/1cycle parallel mode;

Step 2 Clock configuration

NOTE

- In parallel RGB mode, the displayed pixel clock (pixel_CLK) is required to be consistent with the DCLK, the pixel_clk(pixel_clk=Ht*Vt*frame rate) is decided by external LCD.
- When using phase adjustment function, the LCD_IO_POL_REG.DCLK_SEL (reg0x88) selects dclk0–2 of different phase, and LCD_IO_POL_REG.IO2_INV can achieve 180°phase delay.

Configure corresponding frequency by setting PLL_VIDEO0/1 register, and configure TCON LCD0 Clock register.

Configure internal frequency division of TCON_LCD. Based on clock source of TCON and DCLK clock ratio, configure LCD_DCLK_REG[LCD_DCLK_DIV]. If using phase adjustment function, LCD_DCLK_REG[LCD_DCLK_EN] needs be set, usually is 0xf. When the dclk1 and dclk2 in LCD_DCLK_REG[LCD_DCLK_EN] are used, the value of LCD_DCLK_REG[LCD_DCLK_DIV] needs no less than 6.

lcd_dev[sel]->lcd_dclk.dclk_en = en;

lcd_dev[sel]->lcd_dclk.dclk_div = div;

Step 3 Set sequence parameters

The sequence parameters include x,ht,hbp,hspw,y,vt,vbp,vspw, and correspond to LCD_BASE_REG from reg0x48 to reg 0x54. Note that hbp includes hspw, and vbp includes vspw. And LCD_BASIC2_REG.VT needs be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic0.x = x-1;

lcd_dev[sel]->lcd_basic0.y = y-1;

lcd_dev[sel]->lcd_basic1.ht = ht-1;

lcd_dev[sel]->lcd_basic1.hbp = hbp-1;

lcd_dev[sel]->lcd_basic2.vt = vt*2;

lcd_dev[sel]->lcd_basic2.vbp = vbp-1;

lcd_dev[sel]->lcd_basic3.hspw = hspw-1;

lcd_dev[sel]->lcd_basic3.vspw = vspw-1;

Step 4 Open IO output

Set the corresponding data IO enable and control signal IO enable of LCD_IO_TRI_REG (reg0x8C) to 0 to start enable. Note that except the internal IO of TCON_LCD, the external GPIO mapping needs to be set to LCD mode.

When some control signals require polarity reversal, it can realize by setting LCD_IO_POL_REG.IO0-3_INV (reg0x88).

Step 5 Set and open interrupt function

The LCD_GINT0_REG (reg0x4) controls interrupt mode and flag, and the LCD_GINT1_REG (reg0x8) sets the interrupt line position of Line interrupt mode.

V interrupt:

lcd_dev[sel]->lcd_gint0.vb_en = 1;

Line interrupt:

lcd_dev[sel]->lcd_gint1.lcd_line_int_num = line;

lcd_dev[sel]->lcd_gint0.line_en = 1;

Step 6 Open module enable

Enable LCD_CTL_REG.LCD_EN (reg0x40) and LCD_GCTL_REG.LCD_EN (reg0x00).

lcd_dev[sel]->lcd_ctl.lcd_en = 1;

lcd_dev[sel]->lcd_gctl.lcd_en = 1;

The following table is an example of typical parameter configuration.

Table 6-13 HV Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB
	LCD_CTL_REG (0x0040)	32'h0000_0041	Select HV (Sync+DE) mode
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actule value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0010_0000	/
	LCD_GINT0_REG (0x004)	32'h2000_0000	/

Step	Register	Typical Value of Simulation	Description
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

Serial RGB

The serial RGB mode is consistent with parallel RGB mode, the main difference is the definition of clock and the sequence of serial data. The difference is as follows.

Step 1 Select HV interface type

Set LCD_CTL_REG.LCD_IF (reg0x40) to 0 to select HV(Sync+DE) mode; set LCD_HV_IF_REG.HV_MODE (reg0x58) to select 8bit/3cycle RGB serial mode (RGB888), 8bit/4cycle Dummy RGB mode (DRGB) or 8bit/4cycle RGB Dummy mode (RGBD).

lcd_dev[sel]->lcd_ctl.lcd_if = HV(Sync+DE);

lcd_dev[sel]->lcd_ctl.src_sel = src; //src = DE/color/grayscale/...

lcd_dev[sel]->lcd_hv_ctl.hv_mode = Serial mode;

Step 2,3 Set clock and sequence parameters

In serial RGB mode, DCLK is the transfer clock of each byte data. In the same resolution, pixel_clk of serial RGB is three times of its clock in parallel RGB, and ht,hbp,hspw own the same conversion relation. When display is split into odd field and even field, LCD_BASIC2_REG.VT needs not to be set to the twice of the actual value.

lcd_dev[sel]->lcd_basic2.vt = vt;

Set LCD_HV_IF_REG.RGB888_ODD_ORDER/LCD_HV_IF_REG.RGB888_ODD_EVEN to select RGB output sequence of the selected odd and even lines.

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_even = seq_even;

lcd_dev[lcd_sel]->lcd_hv_ctl.srgb_seq_odd = seq_odd;

6.3.4.2 Enabling DC Mode

The DC mode configuration process is similar to the parallel mode of HV mode.

6.3.4.3 Enabling BT.656 Mode

The BT.656 mode configuration process is similar to the parallel mode of HV mode. The following table is an example of typical parameter configuration.

Table 6-14 BT.656 Mode Configuration Example

Step	Register	Typical Value of Simulation	Description
1	LCD_HV_IF_REG (0x0058)	32'h0000_0000	Select parallel RGB

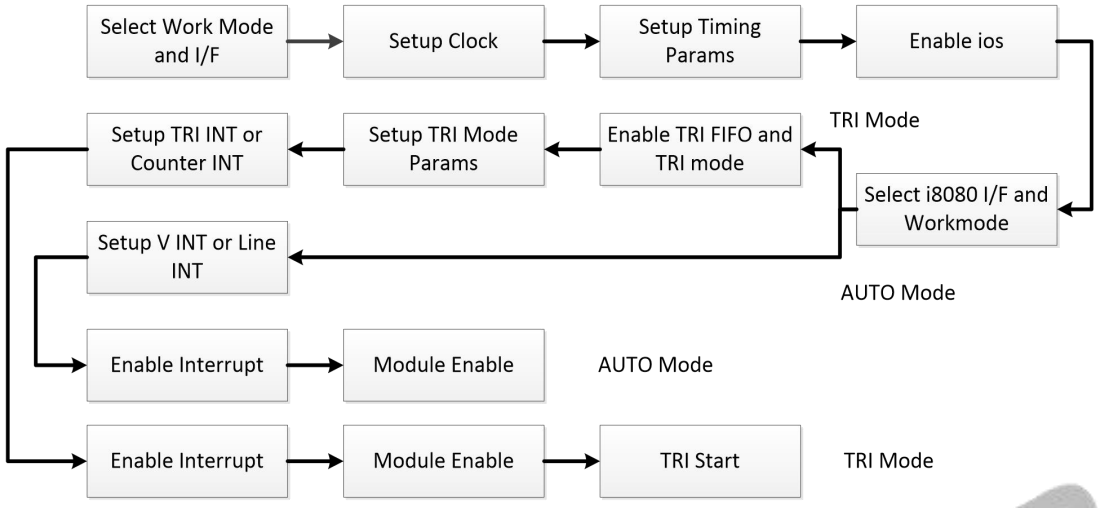
Step	Register	Typical Value of Simulation	Description
	LCD_CTL_REG (0x0040)	32'h0000_0041	Select HV (Sync+DE) mode
	/	/	Enable some functions such as 3DFIFO and FRM. (Optional)
2	LCD_DCLK_REG (0x0044)	32'hf000_0002	/
3	LCD_BASIC0_REG (0x0048)	32'h0063_000f	Set x and y.
	LCD_BASIC1_REG (0x004C)	32'h0095_0013	Set ht and hbp.
	LCD_BASIC2_REG (0x0050)	32'h0030_0001	Set vt and vbp.
	LCD_BASIC3_REG (0x0054)	32'h0009_0000	Set HSPW and VSPW to get the configured value. The actule value is equal to the configured value plus one.
4	LCD_IO_POL_REG (0x0088)	32'h0000_0000	/
	LCD_IO_TRI_REG (0x008C)	32'he000_0000	1: Disable 0: Enable
5	LCD_GINT1_REG (0x008)	32'h0010_0000	/
	LCD_GINT0_REG (0x004)	32'h2000_0000	/
6	LCD_CTL_REG (0x0040)	32'h8000_0041	Open module enable.
	LCD_GCTL_REG (0x0000)	32'h8000_0000	Enable vs and hs to count.

6.3.4.4 Enabling BT.601 Mode

The BT.601 mode configuration process is similar to the parallel mode of HV mode.

6.3.4.5 Enabling i8080 Mode

Figure 6-15 i8080 Mode Initial Process



Step 1 Select i8080 interface type.

Step 2 The step is the same as HV mode, but pulse adjustment function is invalid.

Step 3 The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode, or a handful of functions such as CMAP will not be able to apply.

Step 4 The step is the same as HV mode.

Step 5 Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------If For TRI mode----------

Step 6 Open TRI FIFO switch, and TRI mode function.

Step 7 Set parameters of TRI mode, including block size, block space and block number.

NOTE

- When output interface is parallel mode, then the setting value of block space parameter is not less than 20.
- When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.
- When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.
- When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

Step 8 Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.

Step 9 Open the total switch of interrupt.

Step 10 Open the total enable of interrupt.

Step 11 Operate “tri start” operation (the bit1 of LCD_CPU_IF_REG is set to "1").

----------**If For Auto mode**----------

Step 6 Set and open V interrupt or Line interrupt, the step is the same as HV mode.

Step 7 Open module total enable.

6.3.5 Register List

Module Name	Base Address
TCON_LCD0	0x0550 1000
TCON_LCD1	0x0550 2000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04(N=0-5)	LCD FRM Seed Register
LCD_FRM_TAB_REG	0x002C+N*0x04(N=0-3)	LCD FRM Table Register
LCD_3D_FIFO_REG	0x003C	LCD 3D Fifo Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0

Register Name	Offset	Description
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1
LCD_LVDS_IF_REG	0x0084	LCD LVDS Interface Register
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG0	0x0110+N*0x4(N=0-2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_MUL_REG1	0x0120+N*0x4(N=0-2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_MUL_REG2	0x0130+N*0x4(N=0-2)	LCD CEU Coefficient Register0
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10(N=0-2)	LCD CEU Coefficient Register1
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04(N=0-2)	LCD CEU Coefficient Register2
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
FSYNC_GEN_CTRL_REG	0x0228	LCD FSYNC Generate Control Register
FSYNC_GEN_DLY_REG	0x022C	LCD FSYNC Generate Delay Register
LCD_SYNC_CTL_REG	0x0230	LCD Sync Control Register
LCD_SYNC_POS_REG	0x0234	LCD Sync Position Register
LCD_SLAVE_STOP_POS_REG	0x0238	LCD Slave Stop Position Register

6.3.6 Register Description

6.3.6.1 0x0000 LCD Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN When it's disabled, the module will be reset to idle state. 0: Disable 1: Enable
30:0	/	/	/

6.3.6.2 0x0004 LCD Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004	Register Name: LCD_GINT0_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_VB_INT_EN Enable the Vb interrupt. 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN Enable the line interrupt. 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN Enable the trigger finish interrupt. 0: Disable 1: Enable
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN Enable the trigger counter interrupt. 0: Disable 1: Enable
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 match the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when CPU trigger mode finish. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when SYNC by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W0C	0x0	FSYNC_INT_INV Enable the FSYNC interrupt set signal inverse polarity.

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	Read/Write	Default/Hex	Description
			When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame. Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the FSYNC signal in every frame. Write 0 to clear it.

6.3.6.3 0x0008 LCD Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger (including inactive lines). Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:0	/	/	/

6.3.6.4 0x0010 LCD FRM Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_FRM_EN Enable the dither function. 0: Disable 1:Enable
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R The R component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
5	R/W	0x0	LCD_FRM_MODE_G The G component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
4	R/W	0x0	LCD_FRM_MODE_B

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	Read/Write	Default/Hex	Description
			The B component output bits in dither function. 0: 6bit FRM output 1: 5bit FRM output
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST Set the test mode of dither function. 00: FRM 01: Half 5/6bit, half FRM 10: Half 8bit, half FRM 11: Half 8bit, half 5/6bit

6.3.6.5 0x0014+N*0x04(N=0-5) LCD FRM Seed Register (Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04(N=0-5)			Register Name: LCD_FRM_SEED_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE Set the seed for LFSR used in dither function. N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Note: avoid set it to 0.

6.3.6.6 0x002C+N*0x04(N=0-3) LCD FRM Table Register (Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0-3)			Register Name: LCD_FRM_TAB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

6.3.6.7 0x003C LCD 3D FIFO Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	3D_FIFO_BIST_EN Enable the 3D FIFO bist test function. 0: Disable 1: Enable
30:24	/	/	/
23:20	R/W	0x0	3D_FIFO_OVERLAP The number of overlap when dual DSI mode = 3D_FIFO_OVERLAP, only valid when 3D_FIFO_SETTING set as 2.
19:15	/	/	/
14:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line = 3D_FIFO_HALF_LINE_SIZE+1, only valid when 3D_FIFO_SETTING set as 2.
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING Set the work mode of 3D FIFO. 0: Bypass 1: Used as normal FIFO 2: Used as 3D interlace FIFO 3: Reserved

6.3.6.8 0x0040 LCD Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_EN It executes at the beginning of the first blank line of LCD timing. 0: Disable 1: Enable
30:26	/	/	/
25:24	R/W	0x0	LCD_IF Set the interface type of LCD controller. 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved
23	R/W	0x0	LCD_RB_SWAP

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	Read/Write	Default/Hex	Description
			Enable the function to swap red data and blue data in FIFO1. 0: Default 1: Swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20	R/W	0x0	LCD_INTERLACE_EN This flag is valid only when LCD_EN == 1 0: Disable 1: Enable
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DLY The unit of delay is T_{line}. NOTE: valid only when LCD_EN == 1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL LCD Source Select 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reversed 111: Gridding Check

6.3.6.9 0x0044 LCD Data Clock Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable. 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0;

Offset: 0x0044			Register Name: LCD_DCLK_REG
Bit	Read/Write	Default/Hex	Description
			dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others: Reversed
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk /DCLKDIV Note: 1.If dclk1&dclk2 used, DCLKDIV >=6 2.If only dclk is used, DCLKDIV >=1

6.3.6.10 0x0048 LCD Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	WIDTH_X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	HEIGHT_Y Panel height is Y+1

6.3.6.11 0x004C LCD Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel:HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch (in dclk)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
			Thbp = (HBP +1) * Tdclk

6.3.6.12 0x0050 LCD Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

6.3.6.13 0x0054 LCD Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk Note: HT > (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

6.3.6.14 0x0058 LCD HV Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	HV_MODE Set the HV mode of LCD controller. 0000: 24bit/1cycle parallel mode 1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(CCIR656)
27:26	R/W	0x0	RGB888_ODD_ORDER

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	Read/Write	Default/Hex	Description
			Serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7...). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_EVEN_ORDER Serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8...). 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0x0	YUV_SM Serial YUV mode Output sequence 2-pixel-pair of every scan line. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0x0	YUV_EAV_SAV_F_LINE_DLY Set the delay line mode. 00: F toggle right after active video line 01: delay 2 line (CCIR PAL) 10: delay 3 line (CCIR NTSC) 11:reserved
19	R/W	0x0	CCIR_CSC_DIS Select '0' LCD convert source from RGB to YUV. 0: Enable 1: Disable Only valid when HV mode is "1100".
18:0	/	/	/

6.3.6.15 0x0060 LCD CPU Panel Interface Register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	CPU_MODE Set the CPU interface work mode. 0000: 18bit/256K mode 0010: 16bit mode0

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
			0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG The status of write operation. 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG The status of read operation. 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by VSYNC
16	R/W	0x0	FLUSH Direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
15:3	/	/	/
2	R/W	0x0	TRI_FIFO_EN Enable the trigger FIFO. 0: Disable 1: Enable
1	R/W1S	0x0	TRI_START Software must make sure write '1' only when this flag is '0'.

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	Read/Write	Default/Hex	Description
			Write '1' to start a frame flush, write'0' has no effect. This flag indicated frame flush is running.
0	R/W	0x0	TRI_EN Enable trigger mode. 0: Trigger mode disable 1: Trigger mode enable

6.3.6.16 0x0064 LCD CPU Panel Write Data Register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus.

6.3.6.17 0x0068 LCD CPU Panel Read Data Register0 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus.

6.3.6.18 0x006C LCD CPU Panel Read Data Register1 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus.

6.3.6.19 0x0084 LCD LVDS Interface Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	LCD_LVDS_EN Enable LVDS interface. 0: Disable 1: Enable
30	R/W	0x0	LCD_LVDS_LINK Select work in single link mode or dual link mode. 0: Single link 1: Dual link
29	R/W	0x0	LCD_LVDS_EVEN_ODD_DIR Set the order of even field and odd field. 0: normal 1: reverse
28	R/W	0x0	LCD_LVDS_DIR Set the LVDS direction. 0: Normal 1: Reverse
27	R/W	0x0	LCD_LVDS_MODE Set the LVDS data mode. 0: NS mode 1: JEIDA mode
26	R/W	0x0	LCD_LVDS_BITWIDTH Set the bit width of data. 0: 24bit 1: 18bit
25	R/W	0x0	LCD_LVDS_DEBUG_EN Enable LVDS debug function. 0: Disable 1: Enable
24	R/W	0x0	LCD_LVDS_DEBUG_MODE Set the output signal in debug mode. 0: Mode0 Random data 1: Mode1 Output CLK period=7/2 LVDS CLK period
23	R/W	0x0	LCD_LVDS_CORRECT_MODE Set the LVDS correct mode. 0: Mode0 1: Mode1
22:21	/	/	/
20	R/W	0x0	LCD_LVDS_CLK_SEL Select the clock source of LVDS. 0: Revered

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
			1: LCD CLK
19:5	/	/	/
4	R/W	0x0	LCD_LVDS_CLK_POL Set the clock polarity of LVDS. 0: Reverse 1: Normal
3:0	R/W	0x0	LCD_LVDS_DATA_POL Set the data polarity of LVDS. 0: Reverse 1: Normal

6.3.6.20 0x0088 LCD IO Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IO_OUTPUT_SEL When set as '1', d [23:0], IO0, Io1, IO3 sync to dclk. 0: Normal output 1: Register output
30	/	/	/
29:28	R/W	0x0	DCLK_SEL Set the phase offset of clock and data in hv mode. 00: Used DCLK0(normal phase offset) 01: Used DCLK1(1/3 phase offset) 10: Used DCLK2(2/3 phase offset) Others: Reserved
27	R/W	0x0	IO3_INV Enable invert function of IO3. 0: Not invert 1: Invert
26	R/W	0x0	IO2_INV Enable invert function of IO2. 0: Not invert 1: Invert
25	R/W	0x0	IO1_INV Enable invert function of IO1. 0: Not invert 1: Invert
24	R/W	0x0	IO0_INV Enable invert function of IO0. 0: Not invert

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
			1: Invert
23:0	R/W	0x0	Data_INV LCD output port D [23:0] polarity control, with independent bit control. 0: Normal polarity 1: Invert the specify output

6.3.6.21 0x008C LCD IO Control Register (Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN Set the endian of data bits. 0: Normal 1: Bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN Enable the output of IO3. 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN Enable the output of IO2. 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUR_TRI_EN Enable the output of IO1. 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN Enable the output of IO0. 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN LCD output port D [23:0] output enable, with independent bit control. 1: Disable 0: Enable

6.3.6.22 0x00FC LCD Debug Register (Default Value: 0x2000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	LCD_FIFO_UNDERFLOW The flag shows whether the FIFOs in underflow status. 0: Not underflow 1: Underflow
30	/	/	/
29	R	0x1	LCD_FIELD_POL The flag indicates the current field polarity. 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line.
15:0	/	/	/

6.3.6.23 0x0100 LCD CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CEU_EN Enable CEU function. 0: bypass 1: enable
30	R/W	0x0	BT656_F_MASK BT656 F Mask 0: disable 1: enable
29	R/W	0x0	BT656_F_MASK_VALUE BT656 F Mask Value 0/1
28:0	/	/	/

6.3.6.24 0x0110+N*0x04(N=0-2) LCD CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04(N=0-2)			Register Name: LCD_CEU_COEF_MUL_REG0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE

Offset: 0x0110+N*0x04(N=0-2)			Register Name: LCD_CEU_COEF_MUL_REG0
Bit	Read/Write	Default/Hex	Description
			Signed 13bit value, range of (-16,16). N=0: Rr N=1: Rg N=2: Rb

6.3.6.25 0x0120+N*0x04(N=0-2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x0120+N*0x04(N=0-2)			Register Name: LCD_CEU_COEF_MUL_REG1
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Gr N=1: Gg N=2: Gb

6.3.6.26 0x0130+N*0x04(N=0-2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0130+N*0x04(N=0-2)			Register Name: LCD_CEU_COEF_MUL_REG2
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16). N=0: Br N=1: Bg N=2: Bb

6.3.6.27 0x011C+N*0x10(N=0-2) LCD CEU Coefficient Register1 (Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0-2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19bit value, range of (-16384, 16384). N=0: Rc N=1: Gc N=2: Bc

6.3.6.28 0x0140+N*0x04(N=0-2) LCD CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0-2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255].
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8bit value, range of [0,255].

6.3.6.29 0x0160 LCD CPU Panel Trigger Register0 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set >20*pixel.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

6.3.6.30 0x0164 LCD CPU Panel Trigger Register1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

6.3.6.31 0x0168 LCD CPU Panel Trigger Register2 (Default Value: 0x0020_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x20	START_DLY T_{dly} = (Start_Delay +1) * be_clk*8.
15	R/W	0x0	TRANS_START_MODE Select the FIFOs used in CPU mode.

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
			0: ECC_FIFO+TRI_FIFO 1: TRI_FIFO
14:13	R/W	0x0	SYNC_MODE Set the sync mode in CPU interface. 0x: Auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

6.3.6.32 0x016C LCD CPU Panel Trigger Register3 (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE When set as 01, Tri_Counter_Int occur in cycle of (Count_N+1) ×(Count_M+1) ×4 dclk. When set as 10 or 11, io0 is map as TE input 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor.
7:0	R/W	0x0	COUNTER_M The value of counter factor.

6.3.6.33 0x0170 LCD CPU Panel Trigger Register4 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN Enable the plug mode used in DSI command mode. 0: disable 1:enable
27:25	/	/	/

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
24	R/W	0x0	A1_First_Valid Valid in first Block.
23:0	R/W	0x0	D23_TO_D0_First_Valid Valid in first Block.

6.3.6.34 0x0174 LCD CPU Panel Trigger Register5 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	A1_NON_First_Valid Valid in Block except first.
23:0	R/W	0x0	D23_TO_D0_NON_First_Valid Valid in Block except first.

6.3.6.35 0x01F0 LCD Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, the LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, the LCD controller allow dram controller to change frequency. The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE Select the save mode 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM (If 3D FIFO is bypassed, this mode is not available.) 011: safe at 2 and safe at sync active 100: safe at line

6.3.6.36 0x0228 LCD FSYNC Generate Control Register (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: FSYNC_GEN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:8	R/W	0x0	SENSOR_DIS_TIME Delay 0–2047 Hsync Period When HSYNC_POL_SEL is 0, the actual delay is sensor_dis_time-1. When HSYNC_POL_SEL is 1, the actual delay is sensor_dis_time.
7	/	/	/
6	R/W	0x0	SENSOR_ACT1_VALUE Sensor Active1 Value 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	SENSOR_ACT0_VALUE Sensor Active0 Value 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	SENSOR_DIS_VALUE Sensor Disable Value 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	HSYNC_POL_SEL Hsync Polarity Select 0: normal 1: opposite hsync to hysnc counter
1	R/W	0x0	SEL_VSYNC_EN Select Vsync Enable 0: select vsync falling edge to start state machine 1: select vsync rising edge to start state machine
0	R/W	0x0	FSYNC_GEN_EN Fsync Generate Enable 0: disable 1: enable

6.3.6.37 0x022C LCD FSYNC Generate Delay Register (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/

Offset: 0x022C			Register Name: FSYNC_GEN_DLY_REG
Bit	Read/Write	Default/Hex	Description
27:16	R/W	0x0	SENSOR_ACT0_TIME Delay 0-4095 Pixel clk Period The actual delay is sensor_act0_time+1.
15:12	/	/	/
11:0	R/W	0x0	SENSOR_ACT1_TIME Delay 0-4095 Pixel clk Period The actual delay is sensor_act1_time+1.

6.3.6.38 0x0230 LCD Sync Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: LCD_SYNC_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	LCD_CTRL_WORK_MODE LCD Controller Work mode 0: Single DSI mode 1:Dual DSI mode
7:5	/	/	/
4	R/W	0x0	LCD_CYRL_SYNC_MASTER_SLAVE LCD Controller Sync Master Slave 0: Master 1: Slave Note: Only use in Single DSI mode.
3:1	/	/	/
0	R/W	0x0	LCD_CTRL_SYNC_MODE LCD Controller Sync Mode 0: Sync in the first time 1: Sync every frame Note: Only use in Single DSI mode.

6.3.6.39 0x0234 LCD Sync Position Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x0	LCD_Sync_Pixel_Num Set the pixel number of master LCD controller which is used to trigger the slave LCD controller to start working. This value is the number of pixels between the trigger point and the end of the line.

Offset: 0x0234			Register Name: LCD_SYNC_POS_REG
Bit	Read/Write	Default/Hex	Description
			Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) Note: Only use in Single DSI mode.
15:12	/	/	/
11:0	R/W	0x0	LCD_Sync_Line_Num Set the line number of master LCD controller which is used to trigger the slave LCD controller to start working. Note: It is only set in master LCD controller. It is not necessarily to set in slave LCD controller. Tri pos = Tline*LCD_Sync_Line_Num+Tpixel*(HT-LCD_Sync_Pixel_Num) Note: Only use in Single DSI mode.

6.3.6.40 0x0238 LCD Slave Stop Position Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name:LCD_SLAVE_STOP_POS_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
7:0	R/W	0x0	STOP_VAL Set the stop position of the slave LCD.This value is the number of pixels between the stop position and the end of the HFP. Stop_pos = HFP - Stop_val. NOTE:0<Stop_pos<HFP-2 Note: Only use in Single DSI mode.

6.4 TCON TV

6.4.1 Overview

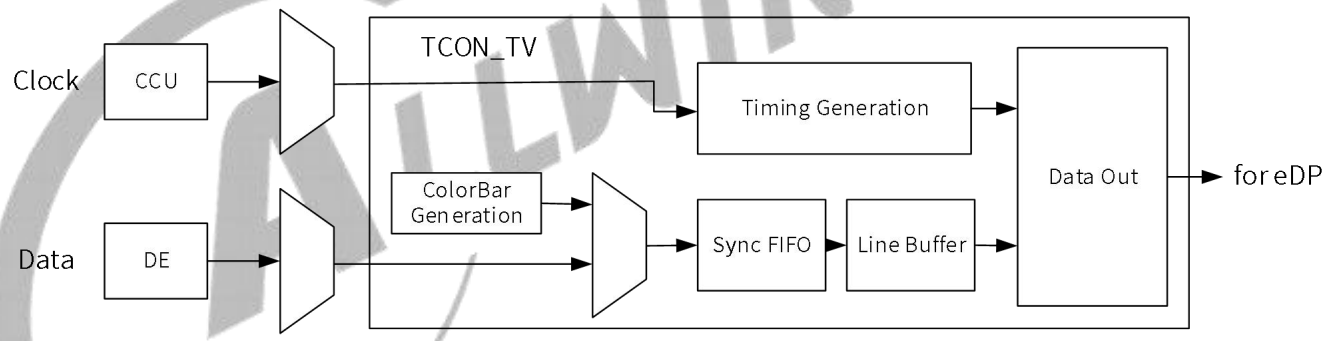
The Timing Controller_TV（TCON_TV）is a module that processes video signals received from systems using a complicated arithmetic and then generates control signals and transmits them to the eDP1.3.

The TCON_TV includes the following features:

- One TCON TV controller (TCON_TV1) for eDP1.3
- Up to 2.5K@60Hz
- Output format:
  - 8-bit or 10-bit pixel depth
  - HV

6.4.2 Block Diagram

Figure 6-16 TCON_TV Block Diagram



6.4.3 Functional Description

6.4.3.1 Clock Sources

The following table describes the clock sources of TCON_TV.

Table 6-15 TCON_TV Clock Sources

Clock Sources	Description	Module
PLL_VIDEO0(4x)	By default, PLL_VIDEO0(4x) is 1188 MHz.	CCU
PLL_VIDEO1(4x)	By default, PLL_VIDEO1(4x) is 1188 MHz.	
PLL_VIDEO2(4x)	By default, PLL_VIDEO2(4x) is 1188 MHz.	
PLL_VIDEO3(4x)	By default, PLL_VIDEO3(4x) is 1188 MHz.	
PLL_PERI0(2x)	By default, PLL_PERI0(2x) is 1.2 GHz.	

6.4.3.2 Panel Interface

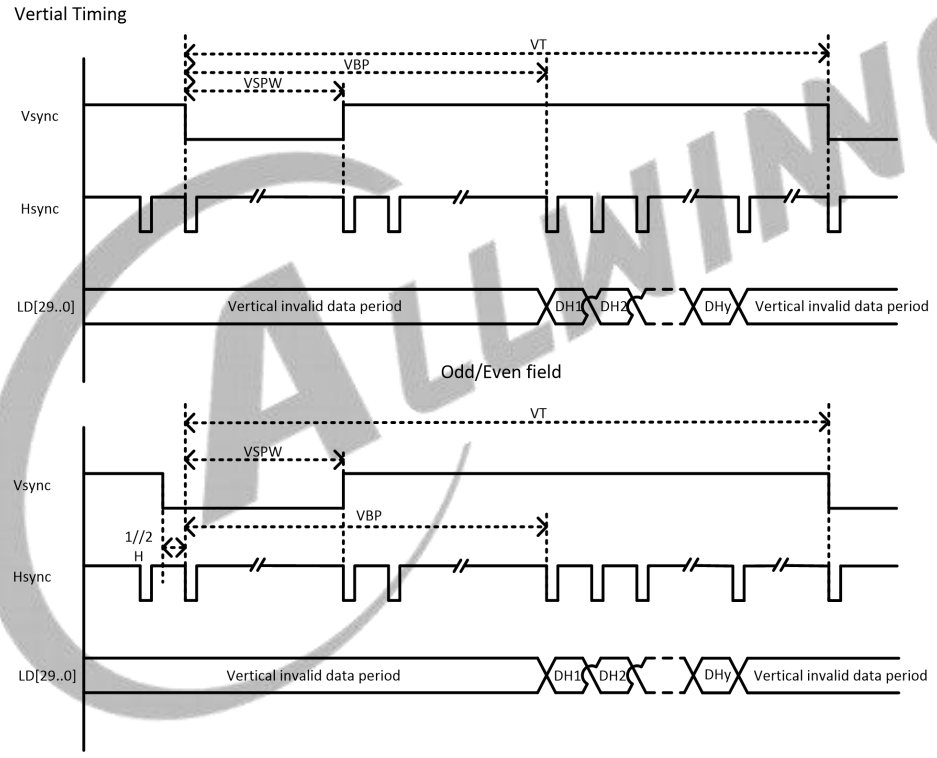
HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications. Its signals are defined as:

Table 6-16 HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[29..0]	30Bit RGB/YUV output from input FIFO for panel	O

HV control signals are active low.

Figure 6-17 HV Interface Vertical Timing



6.4.4 Register List

Module Name	Base Address
TCON_TV1	0x05504000

Register Name	Offset	Description
TV_GCTL_REG	0x000	TV Global Control Register
TV_GINT0_REG	0x004	TV Global Interrupt Register0

Register Name	Offset	Description
TV_GINT1_REG	0x008	TV Global Interrupt Register1
TV_SRC_CTL_REG	0x040	TV Source Control Register
TV_CTL_REG	0x090	TV Control Register
TV_BASIC0_REG	0x094	TV Basic Timing Register0
TV_BASIC1_REG	0x098	TV Basic Timing Register1
TV_BASIC2_REG	0x09C	TV Basic Timing Register2
TV_BASIC3_REG	0x0A0	TV Basic Timing Register3
TV_BASIC4_REG	0x0A4	TV Basic Timing Register4
TV_BASIC5_REG	0x0A8	TV Basic Timing Register5
TV_IO_POL_REG	0x088	TV SYNC Signal Polarity Register
TV_IO_TRI_REG	0x08C	TV ISYNC Signal IO Control Register
TV_DEBUG_REG	0x0FC	TV Debug Register
TV_CEU_CTL_REG	0x100	TV CEU Control Register
TV_CEU_COEF_MUL_REG	0x110+N*0x04	TV CEU Coefficient Register0 (N=0,1,2,4,5,6,8,9,10)
TV_CEU_COEF_RANG_REG	0x140+N*0x04	TV CEU Coefficient Register2 (N=0,1,2)
TV_SAFE_PERIOD_REG	0x1F0	TV Safe Period Register
TV_FILL_CTL_REG	0x300	TV Fill Data Control Register
TV_FILL_BEGIN_REG	0x304+N*0x0C	TV Fill Data Begin Register (N=0,1,2)
TV_FILL_END_REG	0x308+N*0x0C	TV Fill Data End Register (N=0,1,2)
TV_FILL_DATA_REG	0x30C+N*0x0C	TV Fill Data Value Register (N=0,1,2)
TV_FILL_DATA2_REG	0x328	TV Fill Data2 Value Register
TV_FILL_DATA3_REG	0x32C	TV Fill Data3 Value Register
TV_DATA_IO_POL0_REG	0x330	TCON Data IO Polarity Control 0
TV_DATA_IO_POL1_REG	0x334	TCON Data IO Polarity Control 1
TV_DATA_ IO_TRI0_REG	0x338	TCON Data IO Enable Control 0
TV_DATA_ IO_TRI1_REG	0x33C	TCON Data IO Enable Control 1
TV_PIXELDEPTH_MODE_REG	0x340	TV Pixeldepth Mode Control Register

6.4.5 Register Description

6.4.5.1 0x0000 TV Global Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TV_GCTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TV_EN 0: Disable

Offset: 0x0000			Register Name: TV_GCTL_REG
Bit	Read/Write	Default/Hex	Description
			1: Enable When it is disabled, the module will be reset to idle state.
30:0	/	/	/

6.4.5.2 0x0004 TV Global Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TV_GINT0_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0	TV_VB_INT_EN 0: Disable 1: Enable
29	/	/	/
28	R/W	0	TV_LINE_INT_EN 0: disable 1: enable
27:15	/	/	/
14	R/W0C	0	TV_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W0C	0	TV_LINE_INT_FLAG trigger when SY1 match the current TV scan line Write 0 to clear it.
11:0	/	/	/

6.4.5.3 0x0008 TV Global Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TV_GINT1_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0	TV_LINE_INT_NUM Scan line for TV line trigger (including inactive lines) Setting it for the specified line for trigger 1. SY1 is write- only when LINE_TRG1 is disabled.

6.4.5.4 0x0040 TV Source Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0	TV_SRC_SEL: 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

6.4.5.5 0x0090 TV Control Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TV_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TV_EN 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0	START_DELAY This is for DE.
3:2	/	/	/
1	R/W	0	TV_SRC_SEL 0: Reserved 1: BLUE data The priority of this bit is higher than TV_SRC_SEL(bit[2:0]) in TV_SRC_CTL_REG.
0	/	/	/

6.4.5.6 0x0094 TV Basic Timing Register0 (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: TV_BASIC0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	XI Source width is X+1
15:12	/	/	/
11:0	R/W	0	YI Source height is Y+1

6.4.5.7 0x0098 TV Basic Timing Register1 (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	LS_XO Width is LS_XO+1
15:12	/	/	/
11:0	R/W	0	LS_YO Width is LS_YO+1 LS_YO = TV_YI

6.4.5.8 0x009C TV Basic Timing Register2 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TV_BASIC2_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	TV_XO Width is TV_XO+1
15:12	/	/	/
11:0	R/W	0	TV_YO Height is TV_YO+1

6.4.5.9 0x00A0 TV Basic Timing Register3 (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0	HT Horizontal Total Time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0	HBP Horizontal Back Porch Thbp = (HBP +1) * Thdclk

6.4.5.10 0x00A4 TV Basic Timing Register4 (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	Read/Write	Default/Hex	Description
28:16	R/W	0	VT Vertical Total Time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0	VBP Vertical Back Porch (in HD line) Tvbp = (VBP +1) * Th

6.4.5.11 0x00A8 TV Basic Timing Register5 (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TV_BASIC5_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0	HSPW Horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	VSPW Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th VT/2 > (VSPW+1)

6.4.5.12 0x0088 TV SYNC Signal Polarity Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0	IO3_INV 0: Not invert 1: Invert
26	R/W	0	IO2 INV 0: Not invert 1: Invert
25	R/W	0	IO1_INV 0: Not invert 1: Invert
24	R/W	0	IO0_INV 0: Not invert 1: Invert

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
23:0	/	/	/

6.4.5.13 0x008C TV ISYNC Signal IO Control Register (Default Value: 0x0F00_0000)

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable
26	R/W	1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable
25	R/W	1	IO1_OUTPUT_TRI_EN 1: Disable 0: Enable
24	R/W	1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable
23:0	/	/	/

6.4.5.14 0x00FC TV Debug Register (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TV_DEBUG_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0	TV_FIFO_UNDER_FLOW
29	/	/	/
28	R	0	TV_FIELD_POLARITY 0: Second field 1: First field
27:12	/	/	/
13	R/W	0	LINE_BUF _BYPASS 0: Used 1: Bypass
12	/	/	/
11:0	R	0	TV_CURRENT_LINEQUE

6.4.5.15 0x0100 TV CEU Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TV_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	CEU_EN 0: Bypass 1: Enable
30:0	/	/	/

6.4.5.16 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10) TV CEU Coefficient Register0 (Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	CEU_COEF_MUL_VALUE 1.CEU_Coef_Mul_Value only can be 0 or 1 2. REG Map: N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb
7:0	/	/	/

6.4.5.17 0x0140+N*0x04 (N=0,1,2) TV CEU Coefficient Register2 (Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0,1,2)			Register Name: TV_CEU_COEF_RANG_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	CEU_COEF _RANGE_MIN Unsigned 12bit value, range of [0,4095]
15:12	/	/	/
11:0	R/W	0	CEU COEF _RANGE_MAX Unsigned 12bit value, range of [0,4095]

6.4.5.18 0x01F0 TV Safe Period Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0	SAFE_PERIOD_FIFO_NUM
15:4	R/W	0	SAFE_PERIOD_LINE
3	/	/	/
2:0	R/W	0	SAFE_PERIOD_MODE 0: Unsafe 1: Safe 2: Safe at LINE_BUF_CURR_NUM > SAFE_PERIOD_FIFO_NUM 3: Safe at 2 and safe at sync active 4: Safe at line

6.4.5.19 0x0300 TV Fill Data Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TV_FILL_EN 0: Bypass 1: Enable
30:0	/	/	/

6.4.5.20 0x0304+N*0x0C (N=0,1,2) TV Fill Data Begin Register (Default Value: 0x0000_0000)

Offset: 0x0304+N*0x0C (N=0,1,2)			Register Name: TV_FILL_BEGIN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	FILL_BEGIN

6.4.5.21 0x0308+N*0x0C (N=0,1,2) TV Fill Data End Register (Default Value: 0x0000_0000)

Offset: 0x0308+N*0x0C (N=0,1,2)			Register Name: TV_FILL_END_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	FILL_END

6.4.5.22 0x030C+N*0x0C (N=0-2) TV Fill Data Value Register (Default Value: 0x0000_0000)

Offset: 0x030C+N*0x0C (N=0-2)			Register Name: TV_FILL_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	FILL_VALUE bit31-0

6.4.5.23 0x0328 TV Fill Data2 Value Register (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: TV_FILL_DATA2_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0	0x318 FILL_VALUE bit47-bit32
15:0	R/W	0	0x30C FILL_VALUE bit47-bit32

6.4.5.24 0x032C TV Fill Data3 Value Register (Default Value: 0x0000_0000)

Offset: 0x032C			Register Name: TV_FILL_DATA3_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0	0x324 Fill_Value bit47-bit32

6.4.5.25 0x0330 TCON Data IO Polarity Control 0 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: TV_DATA_IO_POL0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	R/Cb CHANNEL DATA_INV bit [11:0] 0: Normal polarity 1: Invert the specify output
15:12	/	/	/
11:0	R/W	0	G/Y CHANNEL DATA_INV bit [11:0] 0: Normal polarity 1: Invert the specify output

6.4.5.26 0x0334 TCON Data IO Polarity Control 1 (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: TV_DATA_IO_POL1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	B/Cr CHANNEL DATA_INV bit [11:0] 0: Normal polarity

Offset: 0x0334			Register Name: TV_DATA_IO_POL1_REG
Bit	Read/Write	Default/Hex	Description
			1: Invert the specify output
15:0	/	/	/

6.4.5.27 0x0338 TCON Data IO Enable Control 0 (Default Value: 0x0fff_0fff)

Offset: 0x0338			Register Name: TV_DATA_IO_TRI0_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xfff	R/Cb CHANNEL DATA_OUTPUT_TRI_EN 1: Disable 0: Enable
15:12	/	/	/
11:0	R/W	0xfff	G/Y CHANNEL DATA_OUTPut_TRI_EN 1: Disable 0: Enable

6.4.5.28 0x033C TCON Data IO Enable Control 1 (Default Value: 0x0fff_0000)

Offset: 0x033C			Register Name: TV_DATA_IO_TRI1_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xfff	B/Cr CHANNEL DATA_OUTPUT_TRI_EN 1: Disable 0: Enable
15:0	/	/	/

6.4.5.29 0x0340 TV Pixeldepth Mode Control Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0	COLORBAR PIXELDEPTH MODE This bit is only valid when colorbar outputs. 0: 8-bit mode Transmits colorbar pattern of 8-bit mode, when the source is internal colorbar. 1: 10-bit mode Transmits colorbar pattern of 10-bit mode, when the source is internal colorbar.

Offset: 0x0340			Register Name: TV_PIXELDEPTH_MODE_REG
Bit	Read/Write	Default/Hex	Description
			2: 12-bit mode Transmits colorbar pattern of 12-bit mode, when the source is internal colorbar. 3: Reserved

Contents

Figure

Tables

7 Video Input Interfaces

7.1 CSIC

7.1.1 Overview

The CMOS Sensor Interface Controller (CSIC) is an image or video data receiver, which can receive image or video data via camera interface and store the data in memory directly.

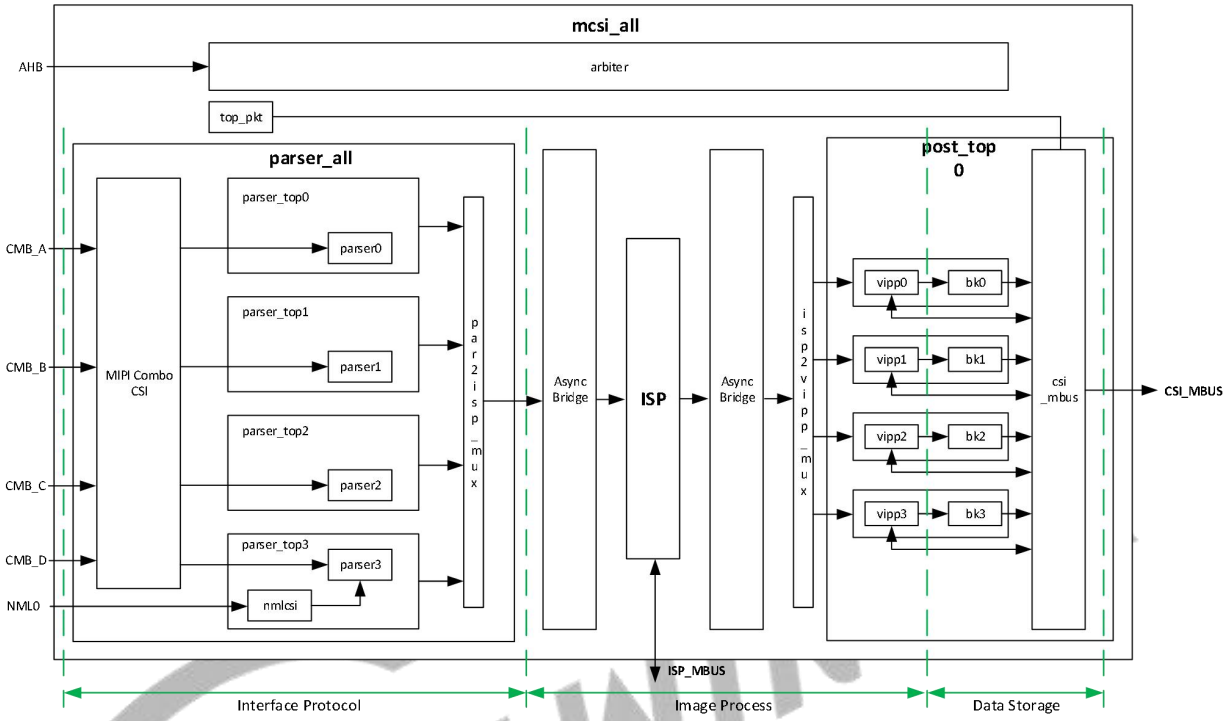
The CSIC includes the following features:

- MIPI CSI supports the following
  - 8M@30fps RAW12 2F-WDR, size up to 3264(H) x 2448(V)
  - 4+ 4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI Interface
    - MIPI CSI2 V1.1
    - MIPI DPHY V1.1
    - 2.0 Gbit/s per lane
  - Crop function
  - Frame-rate decreasing via software
- Parallel CSI supports the following
  - 16-bit digital camera interface
  - 8/10/12/16-bit width
  - BT.656, BT.601, BT.1120 interface
  - Dual Data Rate (DDR) sample mode with pixel clock up to 148.5MHz
  - ITU-R BT.656 up to 4*720P@30fps
  - TU-R BT.1120 up to 4*1080P@30fps
- BK supports the following:
  - 4-lane BK and BK0-3 supports 4-lane time-multiplexing
  - 4 DMA controllers for 4 video stream storage
    - Conversion of interlaced input to progressive output
    - Data conversion supports: YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400
    - Horizontal and vertical flip
- BK doesn't support anti-aliasing and noise reduction

7.1.2 Block Diagram

The following figure shows block diagram of the CSIC.

Figure 7-1 CSIC Block Diagram



7.1.3 Functional Description

7.1.3.1 External Signals

Table 7-1 CSIC External Signals

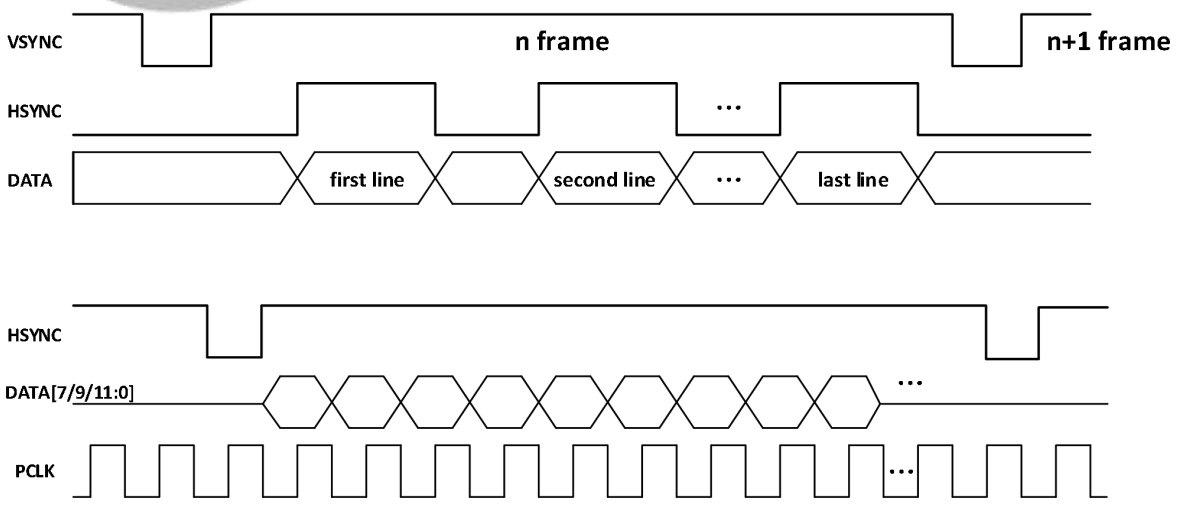
Signal Name	Description	Type
MIPI CSI		
MCSIA-D0N	MIPI CSI Controller A Data0 Negative Signal	AI
MCSIA-D0P	MIPI CSI Controller A Data0 Positive Signal	AI
MCSIA-D1N	MIPI CSI Controller A Data1 Negative Signal	AI
MCSIA-D1P	MIPI CSI Controller A Data1 Positive Signal	AI
MCSIA-CKN	MIPI CSI Controller A Clock Negative Signal	AI
MCSIA-CKP	MIPI CSI Controller A Clock Positive Signal	AI
MCSI0-MCLK	Master Clock for MIPI Sensor	O
MCSIB-D0N	MIPI CSI Controller B Data0 Negative Signal	AI
MCSIB-D0P	MIPI CSI Controller B Data0 Positive Signal	AI
MCSIB-D1N	MIPI CSI Controller B Data1 Negative Signal	AI
MCSIB-D1P	MIPI CSI Controller B Data1 Positive Signal	AI
MCSIB-CKN	MIPI CSI Controller B Clock Negative Signal	AI
MCSIB-CKP	MIPI CSI Controller B Clock Positive Signal	AI

Signal Name	Description	Type
MCSI1-MCLK	Master Clock for MIPI Sensor	O
MCSIC-D0N	MIPI CSI Controller C Data0 Negative Signal	AI
MCSIC-D0P	MIPI CSI Controller C Data0 Positive Signal	AI
MCSIC-D1N	MIPI CSI Controller C Data1 Negative Signal	AI
MCSIC-D1P	MIPI CSI Controller C Data1 Positive Signal	AI
MCSIC-CKN	MIPI CSI Controller C Clock Negative Signal	AI
MCSIC-CKP	MIPI CSI Controller C Clock Positive Signal	AI
MCSI2-MCLK	Master Clock for MIPI Sensor	O
MCSID-D0N	MIPI CSI Controller D Data0 Negative Signal	AI
MCSID-D0P	MIPI CSI Controller D Data0 Positive Signal	AI
MCSID-D1N	MIPI CSI Controller D Data1 Negative Signal	AI
MCSID-D1P	MIPI CSI Controller D Data1 Positive Signal	AI
MCSID-CKN	MIPI CSI Controller D Clock Negative Signal	AI
MCSID-CKP	MIPI CSI Controller D Clock Positive Signal	AI
MCSI3-MCLK	Master Clock for MIPI Sensor	O
CSI-SM-HS	MIPI CSI Slave Mode Horizontal SYNC	O
CSI-SM-VS	MIPI CSI Slave Mode Vertical SYNC	O
Parallel CSI		
NCSI-PCLK	Parallel CSI Pixel Clock	I
NCSI-MCLK	Parallel CSI Master Clock	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI-D[15:0]	Parallel CSI Data Bit	I

7.1.3.2 CSIC Input Timing

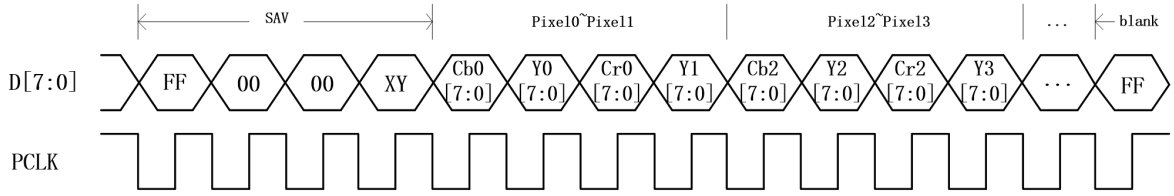
The following figure shows the timing of 8bit CMOS Sensor Interface, in this figure clock active at the rising edge, VSYNC valid at positive, HSYNC valid at positive.

Figure 7-2 8-bit DC Sensor Interface Timing



The following figure shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT.656).

Figure 7-3 8-bit YCbCr4:2:2 with Embedded Syncs (BT.656)



The following table shows the header code of BT.656.

Table 7-2 BT.656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

The following table shows the Header Data Bit Definition of BT.656.

Table 7-3 BT.656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

7.1.3.3 CSIC FIFO Distribution

Table 7-4 CSIC FIFO Distribution

Input format	YUV422/YUV420		Raw
Output format	Planar	UV combined	Raw
FIFO0	Y	Y	All pixels data
FIFO1	Cb (U)	CbCr (UV)	-
FIFO2	Cr (V)	-	-

7.1.3.4 Pixel Format Arrangement

The following figures show the Pixel Format Arrangement.

Figure 7-4 RAW-8 Format

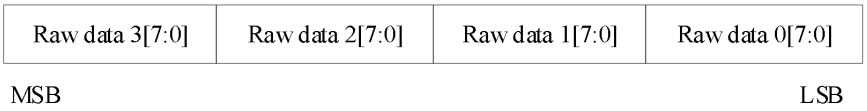


Figure 7-5 Y Format

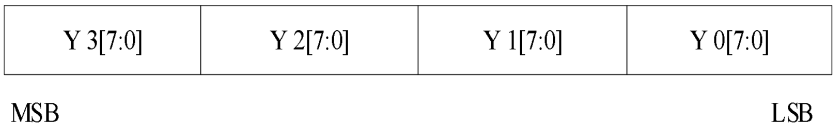
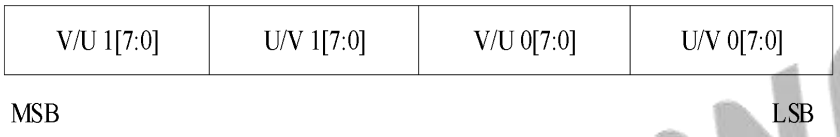


Figure 7-6 UV-Combined Format



7.1.3.5 Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

- For YUV422 format, pixel unit is a YU/YV combination.
- For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
- For Bayer and RAW format, pixel unit is a R/G/B single component.

7.1.3.6 Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of Y0U0Y1V1 will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of Y1U0Y0V1 will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

7.1.4 Programming Guidelines

7.1.4.1 Key Points for Async Bridge Configuration

- If ISP uses work clock with lower frequency than that of parser and post.

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1'b1 to enable async bridge

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1'b1 to make CSI parser work in CSI clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1'b1 to make CSI post work in CSI clock.

- If ISP uses work clock with the same frequency as parser and post

Step 1 Configure the field ISP_BRIDGE_EN (bit [3]) of CSIC_TOP_EN_REG as 1'b0 to disable and bypass async bridge.

Step 2 Configure the field MCSI_PARSER_CLK_MODE (bit [0]) of CCU_CLK_MODE_REG as 1'b0 to make CSI parser work in ISP core clock.

Step 3 Configure the field MCSI_POST_CLK_MODE (bit [1]) of CCU_CLK_MODE_REG as 1'b0 to make CSI post work in ISP core clock.

7.1.4.2 Configuration Notes

- The CCU_CLK_GATING_DISABLE bit (bit [31]) of CCU_CLK_MODE_REG register is configured as 0 by default, that is, the clock in CSIC CCU is gated off by default.
- The MCSI_POST_CLK_MODE bit (bit [1]) and MCSI_PARSER_CLK_MODE bit (bit [0]) of CCU_CLK_MODE_REG register are configured as 1 by default, that is, CSI post and CSI parser work in CSI clock by default.
- The sequence of CSI reset, CSIC clock enable, and PPU power-on is as follows:

  CSIC reset -> PPU power-on -> CSIC clock enable (including: ISP_Clock, CSI Clock, ISP MCLK, CSI MCLK, CSI BUS GATING, and CSI Master0/1/2/3 Clock)

- There are two soft reset bits for MBUS:

Table 7-5 Soft Reset bits for MBUS

Bits	Regsiters	Description
MISP_MBUS_RST (bit [8], high active)	CCU_ISP_CLK_EN_REG	Reset the MBUS interface logic circuit in ISP.
MCSI_POST0_MBUS_RST (bit [20], high active)	CSIC_CCU_POST0_CLK_EN_REG	Reset the MBUS interface logic circuit in POST0.

7.1.5 Register List

There are four groups of registers in CSIC.

Module Name	Base Address
CSIC_CCU	0x05800000
CSIC_TOP	0x05800800
CSIC_PHY	
PHY COMMON	0x05810000
PHYA DIGITAL LAYER	0x05810100
PHYB DIGITAL LAYER	0x05810200
PHYC DIGITAL LAYER	0x05810300
PHYD DIGITAL LAYER	0x05810400
PORT0 PAYLOAD LAYER	0x05811000
PORT1 PAYLOAD LAYER	0x05811400
PORT2 PAYLOAD LAYER	0x05811800
PORT3 PAYLOAD LAYER	0x05811C00
CSIC_ PARSER	
CSIC_PARSER0	0x05820000
CSIC_PARSER1	0x05821000
CSIC_PARSER2	0x05822000
CSIC_PARSER3	0x05823000
CSIC_DMA	
CSIC_DMA0	0x05830000
CSIC_DMA1	0x05831000
CSIC_DMA2	0x05832000
CSIC_DMA3	0x05833000

7.1.5.1 CSIC_CCU Register List

Module Name	Base Address
CSIC_CCU	0x05800000

Register Name	Offset	Description
CSIC_CCU_CLK_MODE_REG	0x0000	CSIC CCU Clock Mode Register
CSIC_CCU_PARSER_CLK_EN_REG	0x0004	CSIC CCU Parser Clock Enable Register
CSIC_CCU_POST0_CLK_EN_REG	0x000C	CSIC CCU Post0 Clock Enable Register
CSIC_CCU_CHFREQ_CLK_CTRL_REG	0x0014	CSIC CCU Chfreq Clock Control Register

7.1.5.2 CSIC_TOP Register List

Module Name	Base Address

Module Name	Base Address
CSIC_TOP	0x05800800

Register Name	Offset	Description
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_ISP2_INPUT0_SEL_REG	0x0050	CSIC ISP2 Input0 Select Register
CSIC_ISP2_INPUT1_SEL_REG	0x0054	CSIC ISP2 Input1 Select Register
CSIC_ISP2_INPUT2_SEL_REG	0x0058	CSIC ISP2 Input2 Select Register
CSIC_ISP2_INPUT3_SEL_REG	0x005C	CSIC ISP2 Input3 Select Register
CSIC_ISP3_INPUT0_SEL_REG	0x0060	CSIC ISP3 Input0 Select Register
CSIC_ISP3_INPUT1_SEL_REG	0x0064	CSIC ISP3 Input1 Select Register
CSIC_ISP3_INPUT2_SEL_REG	0x0068	CSIC ISP3 Input2 Select Register
CSIC_ISP3_INPUT3_SEL_REG	0x006C	CSIC ISP3 Input3 Select Register
CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG	0x0070	CSIC ISP Bridge Buffer Maxuse Counter Clear Register
CSIC_ISP0_BRG01_BUF_MAXUSE_CNT_REG	0x0074	CSIC ISP0 Bridge01 Buffer Maxuse Counter Register
CSIC_ISP0_BRG23_BUF_MAXUSE_CNT_REG	0x0078	CSIC ISP0 Bridge23 Buffer Maxuse Counter Register
CSIC_ISP0_BRG_INT_EN_REG	0x0084	CSIC ISP0 Bridge Interrupt Enable Register
CSIC_ISP0_BRG_INT_PD_REG	0x008C	CSIC ISP0 Bridge Interrupt Pending Register
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_BIST_CTRL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_ADDR_REG	0x00E4	CSIC BIST Start Address Register
CSIC_BIST_END_ADDR_REG	0x00E8	CSIC BIST End Address Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register

Register Name	Offset	Description
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_CHFREQ_CFG0_REG	0x0108	CSIC Change Frequency Configuration 0 Register
CSIC_CHFREQ_CFG1_REG	0x010C	CSIC Change Frequency Configuration 1 Register
CSIC_CHFREQ_OBS_REG	0x0110	CSIC Change Frequency Observation Register
CSIC_CHFREQ_INT_REG	0x0114	CSIC Change Frequency Interrupt Register
CSIC_CHFREQ_DBG_OBS_REG	0x0118	CSIC Change Frequency Debug Observation Register
CSIC_FEATURE_LIST_REG	0x01F0	CSIC Feature List Register

7.1.5.3 CSIC_PHY Register List

PHY COMMON

Module Name	Base Address
PHY COMMON	0x05810000
PHYA DIGITAL LAYER	0x05810100
PHYB DIGITAL LAYER	0x05810200
PHYC DIGITAL LAYER	0x05810300
PHYD DIGITAL LAYER	0x05810400
PORT0 PAYLOAD LAYER	0x05811000
PORT1 PAYLOAD LAYER	0x05811400
PORT2 PAYLOAD LAYER	0x05811800
PORT3 PAYLOAD LAYER	0x05811C00

Register Name	Offset	Description
PHY_TOP_CTL_REG	0x0000	PHY Top Control Register
PHY_TRESCAL_REG	0x0004	PHY Terminal Resistor Calibration Register

PHY DIGITAL LAYER

Module Name	Base Address
PHYA DIGITAL LAYER	0x05810100
PHYB DIGITAL LAYER	0x05810200
PHYC DIGITAL LAYER	0x05810300
PHYD DIGITAL LAYER	0x05810400

Register Name	Offset	Description

Register Name	Offset	Description
PHY_CTL_REG	0x0000	PHY Control Register
PHY_EQ_REG	0x0004	PHY Equalization Register
PHY_OFSCAL_REG0	0x0008	PHY Offset Calibration Register0
PHY_OFSCAL_REG1	0x000C	PHY Offset Calibration Register1
PHY_OFSCAL_REG2	0x0010	PHY Offset Calibration Register2
PHY_DESKEW_REG0	0x0014	PHY Deskew Register0
PHY_DESKEW_REG1	0x0018	PHY Deskew Register1
PHY_DESKEW_REG2	0x001C	PHY Deskew Register2
PHY_TERM_CTL_REG	0x0020	PHY Terminal Control Register
PHY_HS_CTL_REG	0x0024	PHY High Speed Control Register
PHY_S2P_CTL_REG	0x0028	PHY Serial To Parallel Control Register
PHY_MIPIRX_CTL_REG	0x002C	PHY MIPIRX Control Register
PHY_MIPIRX_SYNC_TIMEOUT_REG	0x0030	PHY MIPIRX Synchronization Timeout Register
PHY_FREQ_CNT _REG	0x0034	PHY Frequency Counter Register
PHY_MIPI_LP_TIMEOUT_REG	0x0038	PHY MIPI LP Timeout Register
PHY_MIPI_ULPSEXIT_REG0	0x0040	PHY MIPI ULPSEXIT Register0
PHY_INT_EN_REG	0x0080	PHY Interrupt Enable Register
PHY_INT_PD_REG	0x0084	PHY Interrupt Pending Register

PORT PAYLOAD LAYER

Module Name	Base Address
PORT0 PAYLOAD LAYER	0x05811000
PORT1 PAYLOAD LAYER	0x05811400
PORT2 PAYLOAD LAYER	0x05811800
PORT3 PAYLOAD LAYER	0x05811C00

Register Name	Offset	Description
PORT_CTL_REG	0x0000	PORT Control Register
PORT_LANE_MAP_REG0	0x0004	PORT Lane Mapping Register0
PORT_WDR_MODE_REG	0x000C	PORT WDR Mode Register
PORT_FID_SEL_REG	0x0010	PORT Frame ID Select Register
PORT_MIPI_CFG_REG	0x0100	PORT MIPI Configuration Register
PORT_MIPI_NO_UNPAK_NUM_REG	0x0104	PORT MIPI No Unpacket Number Register
PORT_MIPI_DI_REG	0x0108	PORT MIPI Data Identity Register
PORT_MIPI_USER_DT_REG	0x010C	PORT MIPI User Data Type Register
PORT_MIPI_CH0_DT_TRIG_EN_REG	0x0110	PORT MIPI Channel0 Data Type Trigger Register
PORT_MIPI_CH0_INT_EN_REG	0x0114	PORT MIPI Channel0 Interrupt Enable Register

Register Name	Offset	Description
PORT_MIPI_CH0_INT_PD_REG	0x0118	PORT MIPI Channel0 Interrupt Pending Register
PORT_MIPI_CH0_PH_REG	0x011C	PORT MIPI Channel0 Packet Header Register
PORT_MIPI_CH0_ECC_REG	0x0120	PORT MIPI Channel0 ECC Register
PORT_MIPI_CH0_CKSUM_REG	0x0124	PORT MIPI Channel0 Checksum Register
PORT_MIPI_CH0_FRM_NUM_REG	0x0128	PORT MIPI Channel0 Frame Number Register
PORT_MIPI_CH0_LINE_NUM_REG	0x012C	PORT MIPI Channel0 Line Number Register
PORT_MIPI_CH1_DT_TRIG_EN_REG	0x0130	PORT MIPI Channel1 Data Type Trigger Register
PORT_MIPI_CH1_INT_EN_REG	0x0134	PORT MIPI Channel1 Interrupt Enable Register
PORT_MIPI_CH1_INT_PD_REG	0x0138	PORT MIPI Channel1 Interrupt Pending Register
PORT_MIPI_CH1_PH_REG	0x013C	PORT MIPI Channel1 Packet Header Register
PORT_MIPI_CH1_ECC_REG	0x0140	PORT MIPI Channel1 ECC Register
PORT_MIPI_CH1_CKSUM_REG	0x0144	PORT MIPI Channel1 Checksum Register
PORT_MIPI_CH1_FRM_NUM_REG	0x0148	PORT MIPI Channel1 Frame Number Register
PORT_MIPI_CH1_LINE_NUM_REG	0x014C	PORT MIPI Channel1 Line Number Register
PORT_MIPI_CH2_DT_TRIG_EN_REG	0x0150	PORT MIPI Channel2 Data Type Trigger Register
PORT_MIPI_CH2_INT_EN_REG	0x0154	PORT MIPI Channel2 Interrupt Enable Register
PORT_MIPI_CH2_INT_PD_REG	0x0158	PORT MIPI Channel2 Interrupt Pending Register
PORT_MIPI_CH2_PH_REG	0x015C	PORT MIPI Channel2 Packet Header Register
PORT_MIPI_CH2_ECC_REG	0x0160	PORT MIPI Channel2 ECC Register
PORT_MIPI_CH2_CKSUM_REG	0x0164	PORT MIPI Channel2 Checksum Register
PORT_MIPI_CH2_FRM_NUM_REG	0x0168	PORT MIPI Channel2 Frame Number Register
PORT_MIPI_CH2_LINE_NUM_REG	0x016C	PORT MIPI Channel2 Line Number Register
PORT_MIPI_CH3_DT_TRIG_EN_REG	0x0170	PORT MIPI Channel3 Data Type Trigger Register
PORT_MIPI_CH3_INT_EN_REG	0x0174	PORT MIPI Channel3 Interrupt Enable Register
PORT_MIPI_CH3_INT_PD_REG	0x0178	PORT MIPI Channel3 Interrupt Pending Register
PORT_MIPI_CH3_PH_REG	0x017C	PORT MIPI Channel3 Packet Header Register
PORT_MIPI_CH3_ECC_REG	0x0180	PORT MIPI Channel3 ECC Register
PORT_MIPI_CH3_CKSUM_REG	0x0184	PORT MIPI Channel3 Checksum Register
PORT_MIPI_CH3_FRM_NUM_REG	0x0188	PORT MIPI Channel3 Frame Number Register
PORT_MIPI_CH3_LINE_NUM_REG	0x018C	PORT MIPI Channel3 Line Number Register
PORT_MIPI_LANE_ERR_INT_EN_REG	0x01F0	PORT MIPI Lane Error Interrupt Register
PORT_MIPI_LANE_ERR_INT_PD_REG	0x01F4	PORT MIPI Lane Error Interrupt Pending Register

7.1.5.4 CSIC_PARSER Register List

Module Name	Base Address

Module Name	Base Address
CSIC_PARSER0	0x05820000
CSIC_PARSER1	0x05821000
CSIC_PARSER2	0x05822000
CSIC_PARSER3	0x05823000

Register Name	Offset	Description
CSIC_PRS_EN_REG	0x0000	CSIC Parser Enable Register
CSIC_PRS_NCSIC_IF_CFG_REG	0x0004	CSIC Parser NCSIC Interface Configuration Register
CSIC_PRS_CAP_REG	0x000C	CSIC Parser Capture Register
CSIC_PRS_SIGNAL_STA_REG	0x0010	CSIC Parser Signal Status Register
CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	CSIC Parser NCSIC BT656 Header Configuration Register
CSIC_PRS_CAP_FRM_MSK_0_REG	0x0018	CSIC Parser Capture Frame Mask 0 Register
CSIC_PRS_CAP_FRM_MSK_1_REG	0x001C	CSIC Parser Capture Frame Mask 1 Register
CSIC_PRS_CH0_IN_DMSK_PERIOD_REG	0x0020	CSIC Parser Channel_0 Input Dmask Setting Register
CSIC_PRS_CH0_INFMT_REG	0x0024	CSIC Parser Channel_0 Input Format Register
CSIC_PRS_CH0_OUTPUT_HSIZE_REG	0x0028	CSIC Parser Channel_0 Output Horizontal Size Register
CSIC_PRS_CH0_OUTPUT_VSIZE_REG	0x002C	CSIC Parser Channel_0 Output Vertical Size Register
CSIC_PRS_CH0_INPUT_PARA0_REG	0x0030	CSIC Parser Channel_0 Input Parameter0 Register
CSIC_PRS_CH0_INPUT_PARA1_REG	0x0034	CSIC Parser Channel_0 Input Parameter1 Register
CSIC_PRS_CH0_INPUT_PARA2_REG	0x0038	CSIC Parser Channel_0 Input Parameter2 Register
CSIC_PRS_CH0_INPUT_PARA3_REG	0x003C	CSIC Parser Channel_0 Input Parameter3 Register
CSIC_PRS_CH0_INT_EN_REG	0x0040	CSIC Parser Channel_0 Interrupt Enable Register
CSIC_PRS_CH0_INT_STA_REG	0x0044	CSIC Parser Channel_0 Interrupt Status Register
CSIC_PRS_CH0_LINE_TIME_REG	0x0048	CSIC Parser Channel_0 Line Time Register
CSIC_PRS_CH0_FRM_PRE_MSK_REG	0x004C	CSIC Parser Channel_0 Frame Pre Mask Setting Register
CSIC_PRS_CH1_IN_DMSK_PERIOD_REG	0x0120	CSIC Parser Channel_1 Input Dmask Setting Register
CSIC_PRS_CH1_INFMT_REG	0x0124	CSIC Parser Channel_1 Input Format Register

Register Name	Offset	Description
CSIC_PRS_CH1_OUTPUT_HSIZE_REG	0x0128	CSIC Parser Channel_1 Output Horizontal Size Register
CSIC_PRS_CH1_OUTPUT_VSIZE_REG	0x012C	CSIC Parser Channel_1 Output Vertical Size Register
CSIC_PRS_CH1_INPUT_PARA0_REG	0x0130	CSIC Parser Channel_1 Input Parameter0 Register
CSIC_PRS_CH1_INPUT_PARA1_REG	0x0134	CSIC Parser Channel_1 Input Parameter1 Register
CSIC_PRS_CH1_INPUT_PARA2_REG	0x0138	CSIC Parser Channel_1 Input Parameter2 Register
CSIC_PRS_CH1_INPUT_PARA3_REG	0x013C	CSIC Parser Channel_1 Input Parameter3 Register
CSIC_PRS_CH1_INT_EN_REG	0x0140	CSIC Parser Channel_1 Interrupt Enable Register
CSIC_PRS_CH1_INT_STA_REG	0x0144	CSIC Parser Channel_1 Interrupt Status Register
CSIC_PRS_CH1_LINE_TIME_REG	0x0148	CSIC Parser Channel_1 Line Time Register
CSIC_PRS_CH1_FRM_PRE_MSK_REG	0x014C	CSIC Parser Channel_1 Frame Pre Mask Setting Register
CSIC_PRS_CH2_IN_DMSK_PERIOD_REG	0x0220	CSIC Parser Channel_2 Input Dmask Setting Register
CSIC_PRS_CH2_INFMT_REG	0x0224	CSIC Parser Channel_2 Input Format Register
CSIC_PRS_CH2_OUTPUT_HSIZE_REG	0x0228	CSIC Parser Channel_2 Output Horizontal Size Register
CSIC_PRS_CH2_OUTPUT_VSIZE_REG	0x022C	CSIC Parser Channel_2 Output Vertical Size Register
CSIC_PRS_CH2_INPUT_PARA0_REG	0x0230	CSIC Parser Channel_2 Input Parameter0 Register
CSIC_PRS_CH2_INPUT_PARA1_REG	0x0234	CSIC Parser Channel_2 Input Parameter1 Register
CSIC_PRS_CH2_INPUT_PARA2_REG	0x0238	CSIC Parser Channel_2 Input Parameter2 Register
CSIC_PRS_CH2_INPUT_PARA3_REG	0x023C	CSIC Parser Channel_2 Input Parameter3 Register
CSIC_PRS_CH2_INT_EN_REG	0x0240	CSIC Parser Channel_2 Interrupt Enable Register
CSIC_PRS_CH2_INT_STA_REG	0x0244	CSIC Parser Channel_2 Interrupt Status Register
CSIC_PRS_CH2_LINE_TIME_REG	0x0248	CSIC Parser Channel_2 Line Time Register
CSIC_PRS_CH2_FRM_PRE_MSK_REG	0x024C	CSIC Parser Channel_2 Frame Pre Mask Setting Register
CSIC_PRS_CH3_IN_DMSK_PERIOD_REG	0x0320	CSIC Parser Channel_3 Input Dmask Setting Register
CSIC_PRS_CH3_INFMT_REG	0x0324	CSIC Parser Channel_3 Input Format Register

Register Name	Offset	Description
CSIC_PRS_CH3_OUTPUT_HSIZE_REG	0x0328	CSIC Parser Channel_3 Output Horizontal Size Register
CSIC_PRS_CH3_OUTPUT_VSIZE_REG	0x032C	CSIC Parser Channel_3 Output Vertical Size Register
CSIC_PRS_CH3_INPUT_PARA0_REG	0x0330	CSIC Parser Channel_3 Input Parameter0 Register
CSIC_PRS_CH3_INPUT_PARA1_REG	0x0334	CSIC Parser Channel_3 Input Parameter1 Register
CSIC_PRS_CH3_INPUT_PARA2_REG	0x0338	CSIC Parser Channel_3 Input Parameter2 Register
CSIC_PRS_CH3_INPUT_PARA3_REG	0x033C	CSIC Parser Channel_3 Input Parameter3 Register
CSIC_PRS_CH3_INT_EN_REG	0x0340	CSIC Parser Channel_3 Interrupt Enable Register
CSIC_PRS_CH3_INT_STA_REG	0x0344	CSIC Parser Channel_3 Interrupt Status Register
CSIC_PRS_CH3_LINE_TIME_REG	0x0348	CSIC Parser Channel_3 Line Time Register
CSIC_PRS_CH3_FRM_PRE_MSK_REG	0x034C	CSIC Parser Channel_3 Frame Pre Mask Setting Register
CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	CSIC Parser NCSIC RX Signal0 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG	0x050C	CSIC Parser NCSIC RX Signal3 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG	0x0510	CSIC Parser NCSIC RX Signal4 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	CSIC Parser NCSIC RX Signal5 Delay Adjust Register
CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	CSIC Parser NCSIC RX Signal6 Delay Adjust Register
CSIC_PRS_SYNC_EN_REG	0x0520	CSIC Parser SYNC EN Register
CSIC_PRS_SYNC_CFG_REG	0x0524	CSIC Parser SYNC CFG Register
SIC_PRS_VS_WAIT_N_REG	0x0528	CSIC Parser VS WAIT N Register
CSIC_PRS_VS_WAIT_M_REG	0x052C	CSIC Parser VS WAIT M Register
CSIC_PRS_XSYNC_ENABLE_REG	0x0540	CSIC Parser XSYNC ENABLE Register
CSIC_PRS_XVS_PERIOD_REG	0x0544	CSIC Parser XVS Period Register
CSIC_PRS_XHS_PERIOD_REG	0x0548	CSIC Parser XHS Period Register
CSIC_PRS_XVS_LENGTH_REG	0x054C	CSIC Parser XVS LENGTH Register
CSIC_PRS_XHS_LENGTH_REG	0x0550	CSIC Parser XHS LENGTH Register
CSIC_PRS_SYNC_DLY_REG	0x0554	CSIC Parser SYNC DELAY Register

7.1.5.5 CSIC DMA Register List

Module Name	Base Address

Module Name	Base Address
CSIC_DMA0	0x05830000
CSIC_DMA1	0x05831000
CSIC_DMA2	0x05832000
CSIC_DMA3	0x05833000

Register Name	Offset	Description
CSIC_DMA_TOP_REG	0x0000	CSIC DMA TOP Register
CSIC_DMA_MUL_CH_CFG_REG	0x0004	CSIC DMA Multi-Channel Configuration Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0010	CSIC DMA Frame Rate Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0014	CSIC DMA Accumulated and Internal Clock Counter Register
CSIC_DMA_FS_FRM_CNT_REG	0x0020	CSIC DMA Fsync Frame Counter Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register
CSIC_DMA_VE_FRM_CNT_REG	0x0050	CSIC DMA VE Frame Counter Value Register
CSIC_DMA_VE_LINE_CNT_REG	0x0054	CSIC DMA VE Line Counter Value Register
CSIC_DMA_VE_CUR_FRM_ADDR_REG	0x0058	CSIC DMA VE Current Frame Address Register
CSIC_DMA_VE_LAST_FRM_ADDR_REG	0x005C	CSIC DMA VE Last Frame Address Register
CSIC_DMA_FIFO_STAT_REG	0x0080	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x0084	CSIC DMA FIFO Threshold Register
CSIC_DMA_TOP_INT_EN_REG	0x0100	CSIC DMA TOP Interrupt Enable Register
CSIC_DMA_TOP_INT_STA_REG	0x0104	CSIC DMA TOP Interrupt Status Register
CSIC_DMA_VER_REG	0x01F0	CSIC DMA Version Register
CSIC_DMA_FEATURE_REG	0x01F4	CSIC DMA Feature List Register
CSIC_DMA_CH0_EN_REG	0x0200	CSIC DMA Channel0 Enable Register
CSIC_DMA_CH0_CFG_REG	0x0204	CSIC DMA Channel0 Configuration Register
CSIC_DMA_CH0_FRM_LOST_CNT_REG	0x0208	CSIC DMA Channel0 Frame Lost Counter Register
CSIC_DMA_CH0_FRM_MSK_CFG_REG	0x020C	CSIC DMA Channel0 Frame Mask Configuration Register
CSIC_DMA_CH0_HSIZE_REG	0x0210	CSIC DMA Channel0 Horizontal Size Register
CSIC_DMA_CH0_VSIZE_REG	0x0214	CSIC DMA Channel0 Vertical Size Register
CSIC_DMA_CH0_VCROP_CFG_REG	0x0218	CSIC DMA Channel0 Vertical Crop Mode Register
CSIC_DMA_CH0_F0_BUFA_REG	0x0220	CSIC DMA Channel0 FIFO 0 Output Buffer-A

Register Name	Offset	Description
		Address Register
CSIC_DMA_CH0_F0_BUFA_RESULT_REG	0x0224	CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F1_BUFA_REG	0x0228	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH0_F1_BUFA_RESULT_REG	0x022C	CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH0_F2_BUFA_REG	0x0230	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH0_F2_BUFA_RESULT_REG	0x0234	CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH0_BUF_LEN_REG	0x0238	CSIC DMA Channel0 Buffer Length Register
CSIC_DMA_CH0_FLIP_SIZE_REG	0x023C	CSIC DMA Channel0 Flip Size Register
CSIC_DMA_CH0_CAP_STA_REG	0x024C	CSIC DMA Channel0 Capture Status Register
CSIC_DMA_CH0_INT_EN_REG	0x0250	CSIC DMA Channel0 Interrupt Enable Register
CSIC_DMA_CH0_INT_STA_REG	0x0254	CSIC DMA Channel0 Interrupt Status Register
CSIC_DMA_CH0_LINE_CNT_REG	0x0258	CSIC DMA Channel0 Line Counter Register
CSIC_DMA_CH0_ABN_FRM_NUM_REG	0x025C	CSIC DMA Channel0 Abnormal Frame Number Register
CSIC_DMA_CH0_LINE_STAT_REG	0x0268	CSIC DMA Channel0 Line Statistic Register
CSIC_DMA_CH0_PCLK_STAT_REG	0x0270	CSIC DMA Channel0 PCLK Statistic Register
CSIC_DMA_CH0_ABN_MSK_REG	0x0298	CSIC DMA Channel0 Abnormal Mask Register
CSIC_DMA_CH0_PIXELS_ADD_EN_REG	0x029C	CSIC DMA Channel0 Pixels Add Enable Register
CSIC_DMA_CH0_PIXELS_ADD_VAL_REG	0x02A0	CSIC DMA Channel0 Pixels Add Value Register
The following resgisters are only for DMA0-DMA3.		
CSIC_DMA_CH1_EN_REG	0x0400	CSIC DMA Channel1 Enable Register
CSIC_DMA_CH1_CFG_REG	0x0404	CSIC DMA Channel1 Configuration Register
CSIC_DMA_CH1_FRM_LOST_CNT_REG	0x0408	CSIC DMA Channel1 Frame Lost Counter Register
CSIC_DMA_CH1_FRM_MSK_CFG_REG	0x040C	CSIC DMA Channel1 Frame Mask Configuration Register
CSIC_DMA_CH1_HSIZE_REG	0x0410	CSIC DMA Channel1 Horizontal Size Register
CSIC_DMA_CH1_VSIZE_REG	0x0414	CSIC DMA Channel1 Vertical Size Register
CSIC_DMA_CH1_VCROP_CFG_REG	0x0418	CSIC DMA Channel1 Vertical Crop Mode Register
CSIC_DMA_CH1_F0_BUFA_REG	0x0420	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH1_F0_BUFA_RESULT_REG	0x0424	CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register

Register Name	Offset	Description
CSIC_DMA_CH1_F1_BUFA_REG	0x0428	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH1_F1_BUFA_RESULT_REG	0x042C	CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH1_F2_BUFA_REG	0x0430	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH1_F2_BUFA_RESULT_REG	0x0434	CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH1_BUF_LEN_REG	0x0438	CSIC DMA Channel1 Buffer Length Register
CSIC_DMA_CH1_FLIP_SIZE_REG	0x043C	CSIC DMA Channel1 Flip Size Register
CSIC_DMA_CH1_CAP_STA_REG	0x044C	CSIC DMA Channel1 Capture Status Register
CSIC_DMA_CH1_INT_EN_REG	0x0450	CSIC DMA Channel1 Interrupt Enable Register
CSIC_DMA_CH1_INT_STA_REG	0x0454	CSIC DMA Channel1 Interrupt Status Register
CSIC_DMA_CH1_LINE_CNT_REG	0x0458	CSIC DMA Channel1 Line Counter Register
CSIC_DMA_CH1_ABN_FRM_NUM_REG	0x045C	CSIC DMA Channel1 Abnormal Frame Number Register
CSIC_DMA_CH1_LINE_STAT_REG	0x0468	CSIC DMA Channel1 Line Statistic Register
CSIC_DMA_CH1_PCLK_STAT_REG	0x0470	CSIC DMA Channel1 PCLK Statistic Register
CSIC_DMA_CH1_ABN_MSK_REG	0x0498	CSIC DMA Channel1 Abnormal Mask Register
CSIC_DMA_CH1_PIXELS_ADD_EN_REG	0x049C	CSIC DMA Channel1 Pixels Add Enable Register
CSIC_DMA_CH1_PIXELS_ADD_VAL_REG	0x04A0	CSIC DMA Channel1 Pixels Add Value Register
CSIC_DMA_CH2_EN_REG	0x0600	CSIC DMA Channel2 Enable Register
CSIC_DMA_CH2_CFG_REG	0x0604	CSIC DMA Channel2 Configuration Register
CSIC_DMA_CH2_FRM_LOST_CNT_REG	0x0608	CSIC DMA Channel2 Frame Lost Counter Register
CSIC_DMA_CH2_FRM_MSK_CFG_REG	0x060C	CSIC DMA Channel2 Frame Mask Configuration Register
CSIC_DMA_CH2_HSIZE_REG	0x0610	CSIC DMA Channel2 Horizontal Size Register
CSIC_DMA_CH2_VSIZE_REG	0x0614	CSIC DMA Channel2 Vertical Size Register
CSIC_DMA_CH2_VCROP_CFG_REG	0x0618	CSIC DMA Channel2 Vertical Crop Mode Register
CSIC_DMA_CH2_F0_BUFA_REG	0x0620	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH2_F0_BUFA_RESULT_REG	0x0624	CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH2_F1_BUFA_REG	0x0628	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH2_F1_BUFA_RESULT_REG	0x062C	CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register

Register Name	Offset	Description
CSIC_DMA_CH2_F2_BUFA_REG	0x0630	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH2_F2_BUFA_RESULT_REG	0x0634	CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_CH2_BUF_LEN_REG	0x0638	CSIC DMA Channel2 Buffer Length Register
CSIC_DMA_CH2_FLIP_SIZE_REG	0x063C	CSIC DMA Channel2 Flip Size Register
CSIC_DMA_CH2_CAP_STA_REG	0x064C	CSIC DMA Channel2 Capture Status Register
CSIC_DMA_CH2_INT_EN_REG	0x0650	CSIC DMA Channel2 Interrupt Enable Register
CSIC_DMA_CH2_INT_STA_REG	0x0654	CSIC DMA Channel2 Interrupt Status Register
CSIC_DMA_CH2_LINE_CNT_REG	0x0658	CSIC DMA Channel2 Line Counter Register
CSIC_DMA_CH2_ABN_FRM_NUM_REG	0x065C	CSIC DMA Channel2 Abnormal Frame Number Register
CSIC_DMA_CH2_LINE_STAT_REG	0x0668	CSIC DMA Channel2 Line Statistic Register
CSIC_DMA_CH2_PCLK_STAT_REG	0x0670	CSIC DMA Channel2 PCLK Statistic Register
CSIC_DMA_CH2_ABN_MSK_REG	0x0698	CSIC DMA Channel2 Abnormal Mask Register
CSIC_DMA_CH2_PIXELS_ADD_EN_REG	0x069C	CSIC DMA Channel2 Pixels Add Enable Register
CSIC_DMA_CH2_PIXELS_ADD_VAL_REG	0x06A0	CSIC DMA Channel2 Pixels Add Value Register
CSIC_DMA_CH3_EN_REG	0x0800	CSIC DMA Channel3 Enable Register
CSIC_DMA_CH3_CFG_REG	0x0804	CSIC DMA Channel3 Configuration Register
CSIC_DMA_CH3_FRM_LOST_CNT_REG	0x0808	CSIC DMA Channel3 Frame Lost Counter Register
CSIC_DMA_CH3_FRM_MSK_CFG_REG	0x080C	CSIC DMA Channel3 Frame Mask Configuration Register
CSIC_DMA_CH3_HSIZE_REG	0x0810	CSIC DMA Channel3 Horizontal Size Register
CSIC_DMA_CH3_VSIZE_REG	0x0814	CSIC DMA Channel3 Vertical Size Register
CSIC_DMA_CH3_VCROP_CFG_REG	0x0818	CSIC DMA Channel3 Vertical Crop Mode Register
CSIC_DMA_CH3_F0_BUFA_REG	0x0820	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register
CSIC_DMA_CH3_F0_BUFA_RESULT_REG	0x0824	CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F1_BUFA_REG	0x0828	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register
CSIC_DMA_CH3_F1_BUFA_RESULT_REG	0x082C	CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_CH3_F2_BUFA_REG	0x0830	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register
CSIC_DMA_CH3_F2_BUFA_RESULT_REG	0x0834	CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register

Register Name	Offset	Description
CSIC_DMA_CH3_BUF_LEN_REG	0x0838	CSIC DMA Channel3 Buffer Length Register
CSIC_DMA_CH3_FLIP_SIZE_REG	0x083C	CSIC DMA Channel3 Flip Size Register
CSIC_DMA_CH3_CAP_STA_REG	0x084C	CSIC DMA Channel3 Capture Status Register
CSIC_DMA_CH3_INT_EN_REG	0x0850	CSIC DMA Channel3 Interrupt Enable Register
CSIC_DMA_CH3_INT_STA_REG	0x0854	CSIC DMA Channel3 Interrupt Status Register
CSIC_DMA_CH3_LINE_CNT_REG	0x0858	CSIC DMA Channel3 Line Counter Register
CSIC_DMA_CH3_ABN_FRM_NUM_REG	0x085C	CSIC DMA Channel3 Abnormal Frame Number Register
CSIC_DMA_CH3_LINE_STAT_REG	0x0868	CSIC DMA Channel3 Line Statistic Register
CSIC_DMA_CH3_PCLK_STAT_REG	0x0870	CSIC DMA Channel3 PCLK Statistic Register
CSIC_DMA_CH3_ABN_MSK_REG	0x0898	CSIC DMA Channel3 Abnormal Mask Register
CSIC_DMA_CH3_PIXELS_ADD_EN_REG	0x089C	CSIC DMA Channel3 Pixels Add Enable Register
CSIC_DMA_CH3_PIXELS_ADD_VAL_REG	0x08A0	CSIC DMA Channel3 Pixels Add Value Register

7.1.6 CSIC CCU Register Description

7.1.6.1 0x0000 CSIC CCU Clock Mode Register (Default Value:0x0000_0003)

Offset: 0x0000			Register Name: CCU_CLK_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CCU_CLK_GATING_DISABLE 0: CCU Clock Gating Registers(0x0004-0x0010) effect 1:CCU Clock Gating Registers(0x0004-0x0010) not effect
30:2	/	/	/
1	R/W	0x1	MCSI_POST_CLK_MODE 0: CSI Post works in ISP core clock 1: CSI Post works in CSI clock
0	R/W	0x1	MCSI_PARSER_CLK_MODE 0: CSI Parser works in ISP core clock 1: CSI Parser works in CSI clock

7.1.6.2 0x0004 CSIC CCU Parser Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MCSI_COMBO0_CLK_ENABLE

Offset: 0x0004			Register Name: CSIC_CCU_PARSER_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Combo0 clock disable 1: Combo0 clock enable
7:4	/	/	/
3	R/W	0x0	MCSI_PARSER3_CLK_ENABLE 0: CSI Parser3 clock disable 1: CSI Parser3 clock enable
2	R/W	0x0	MCSI_PARSER2_CLK_ENABLE 0: CSI Parser2 clock disable 1: CSI Parser2 clock enable
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE Parser0 clock gating 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

7.1.6.3 0x0008 CSIC CCU ISP Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x0008			Register Name: CCU_ISP_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	MISP_MBUS_RST 0: ISP0 MBUS reset de-assert 1: ISP0 MBUS reset assert
7:5	/	/	/
4	R/W	0x0	MISP0_BRIDGE_CLK_ENABLE 0: ISP0 bridge clock disable 1: ISP0 bridge clock enable
3:1	/	/	/
0	R/W	0x0	MISP0_CLK_ENABLE 0: ISP0 clock disable 1: ISP0 clock enable

7.1.6.4 0x000C CSIC CCU Post0 Clock Enable Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	MCSI_POST0_MBUS_RST

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: POST0 MBUS reset de-assert 1: POST0 MBUS reset assert
19:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE Post0 clock gating 0: POST0 clock disable 1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0: VIPP1 clock disable 1: VIPP1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE 0: VIPP0 clock disable 1: VIPP0 clock enable, when MCSI_POST0_CLK_ENABLE is set to 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE 0: BK3 clock disable 1: BK3 clock enable, when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable, when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE BK1 clock gating 0: BK1 clock disable 1: BK1 clock enable, when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE BK0 clock gating 0: BK0 clock disable

Offset: 0x000C			Register Name: CSIC_CCU_POST0_CLK_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: BK0 clock enable, when MCSI_POST0_CLK_ENABLE is 1

7.1.6.5 0x0014 CSIC CCU Chfreq Clock Control Register (Default Value:0x0000_1700)

Offset: 0x0014			Register Name: CSIC_CCU_CHFREQ_CLK_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x00	FACTOR_N Factor N N= FACTOR_N +1. FACTOR_N is from 0 to 31.
15:13	/	/	/
12:8	R/W	0x17	FACTOR_M Factor M M= FACTOR_M +1. FACTOR_M is from 0 to 31.
7:1	/	/	/
0	R/W	0x0	CHFREQ_CLK_GATING. Gating Clock. 0: Clock is OFF 1: Clock is ON CHFREQ_CLK = Clock Source/M/N. Clock Source is clk24m.

7.1.7 CSIC TOP Register Description

7.1.7.1 0x0000 CSIC TOP Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_TOP_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ISP_BRIDGE_EN Enable Async Bridge from parser to ISP and ISP to post, when ISP uses different clock source from csi_top_clk 0: Disable 1: Enable
2:0	/	/	/

7.1.7.2 0x0004 CSIC Pattern Generation Enable Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_PTN_GEN_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSIC Pattern Generating Start 0: Finish other: Start Software writes this bit to “1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to “0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern Generation Enable

7.1.7.3 0x0008 CSIC Pattern Control Register (Default Value:0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 101: NCSIC3 110: COMBO others: Reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH Pattern Generator output data width 00:8bit 01:10bit 10:12bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000: MIPI 1-lane

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			0001: MIPI 2-lane 0010: MIPI 3-lane 0011: MIPI 4-lane 0100:NCSIC with max 12-bit data ({field,vsyn,hsyn,1'b0,data[11:0]}) 0101:NCSIC with max 16-bit data ({12'h0,field,vsyn,hsyn,1'b0,data[15:0]}) 0110:NCSIC with max 24-bit data ({field,vsyn,hsyn,5'h0,data[23:0]}) 0111: Reserved 1000:BT656 8 bits' width 1001:BT656 16 bits' width 1010:BT656 24 bits' width 1011: Reserved 1100: BAYER 12 bits for ISPFE 1101: UYVY422 12 bits for ISPFE 1110: UYVY420 12 bits for ISPFE 1111:Reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

7.1.7.4 0x0010 CSIC_PTN_VBLANK_CYCLE Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PTN_VBLANK_CYCLE
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PTN_VBLANK_CYCLE Set clock cycles between two pattern as vblank

7.1.7.5 0x0020 CSIC Pattern Generation Length Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

7.1.7.6 0x0024 CSIC Pattern Generation Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

7.1.7.7 0x0028 CSIC Pattern ISP Size Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size, only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size, only valid for ISP mode pattern generation.

7.1.7.8 0x0030 CSIC ISP0 Input0 Select Register (Default Value:0x0000_0000)

Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	ISP0 Input0 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
			Others: Reserved

7.1.7.9 0x0034 CSIC ISP0 Input1 Select Register (Default Value:0x0000_0001)

Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x1	ISP0 Input1 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.10 0x0038 CSIC ISP0 Input2 Select Register (Default Value:0x0000_0002)

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x2	ISP0 Input2 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
			1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.11 0x003C CSIC ISP0 Input3 Select Register (Default Value:0x0000_0003)

Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	ISP0 Input3 select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Others: Reserved

7.1.7.12 0x0040 CSIC ISP1 Input0 Select Register (Default Value:0x0000_0004)

Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x4	ISP1 Input0 Select

Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
			0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.13 0x0044 CSIC ISP1 Input1 Select Register (Default Value:0x0000_0005)

Offset :0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x5	ISP1 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3

Offset :0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
			Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.14 0x0048 CSIC ISP1 Input2 Select Register (Default Value:0x0000_0006)

Offset :0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x6	ISP1 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.15 0x004C CSIC ISP1 Input3 Select Register (Default Value:0x0000_0007)

Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x7	ISP1 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1

Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
			0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP1 exists. ISP1 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.16 0x0050 CSIC ISP2 Input0 Select Register (Default Value:0x0000_0008)

Offset :0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x8	ISP2 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.17 0x0054 CSIC ISP2 Input1 Select Register (Default Value:0x0000_0009)

Offset :0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x9	ISP2 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.18 0x0058 CSIC ISP2 Input2 Select Register (Default Value:0x0000_000a)

Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xa	ISP2 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3

Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
			1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.19 0x005C CSIC ISP2 Input3 Select Register (Default Value:0x0000_000b)

Offset :0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xb	ISP2 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP2 exists. ISP2 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.20 0x0060 CSIC ISP3 Input0 Select Register (Default Value:0x0000_000c)

Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xc	ISP3 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1

Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
			0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.21 0x0064 CSIC ISP3 Input1 Select Register (Default Value:0x0000_000d)

Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xd	ISP3 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP3 exists. ISP3 is a virtual concept here

Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
			and serves as the data path-to ISP MUX.

7.1.7.22 0x0068 CSIC ISP3 Input2 Select Register (Default Value:0x0000_000e)

Offset :0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xe	ISP3 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.

7.1.7.23 0x006C CSIC ISP3 Input3 Select Register (Default Value:0x0000_000f)

Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0xf	ISP3 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0

Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
			0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 1000: input from Parser2 CH0 1001: input from Parser2 CH1 1010: input from Parser2 CH2 1011: input from Parser2 CH3 1100: input from Parser3 CH0 1101: input from Parser3 CH1 1110: input from Parser3 CH2 1111: input from Parser3 CH3 **Note: No physical ISP3 exists. ISP3 is a virtual concept here and serves as the data path-to ISP MUX.**

7.1.7.24 0x0070 CSIC ISP Bridge Buffer Maxuse Counter Clear Register (Default Value:0x0000_0000)

Offset :0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ISP0_BRG3_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
2	R/W	0x0	ISP0_BRG2_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
1	R/W	0x0	ISP0_BRG1_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
0	R/W	0x0	ISP0_BRG0_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear

7.1.7.25 0x0074 CSIC ISP0 Bridge01 Buffer Maxuse Counter Register (Default Value:0x0000_0000)

Offset :0x0074			Register Name: CSIC_ISP0_BRG01_BUF_MAXUSE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	ISP0_BRG1_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG0_BUF_MAXUSE_CNT

7.1.7.26 0x0078 CSIC ISP0 Bridge23 Buffer Maxuse Counter Register (Default Value:0x0000_0000)

Offset :0x0078			Register Name: CSIC_ISP0_BRG23_BUF_MAXUSE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:16	RO	0x0	ISP0_BRG3_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG2_BUF_MAXUSE_CNT

7.1.7.27 0x0084 CSIC ISP0 Bridge Interrupt Enable Register (Default Value:0x0000_0000)

Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x0	ISP0_BRG3_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge3 Slow to Fast Side
26	R/W	0x0	ISP0_BRG2_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge2 Slow to Fast Side
25	R/W	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:20	/	/	/
19	R/W	0x0	ISP0_BRG3_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge3 Fast to Slow Side
18	R/W	0x0	ISP0_BRG2_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge2 Fast to Slow Side
17	R/W	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:12	/	/	/
11	R/W	0x0	ISP0_BRG3_BUF_OV_INT_EN ISP0 Bridge3 Buffer overflow interrupt enable

Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	ISP0_BRG2_BUF_OV_INT_EN ISP0 Bridge2 Buffer overflow interrupt enable
9	R/W	0x0	ISP0_BRG1_BUF_OV_INT_EN ISP0 Bridge1 Buffer overflow interrupt enable
8	R/W	0x0	ISP0_BRG0_BUF_OV_INT_EN ISP0 Bridge0 Buffer overflow interrupt enable
7:4	/	/	/
3	R/W	0x0	ISP0_BRG3_RS_INT_EN ISP0 Bridge3 Read clock too slow interrupt enable
2	R/W	0x0	ISP0_BRG2_RS_INT_EN ISP0 Bridge2 Read clock too slow interrupt enable
1	R/W	0x0	ISP0_BRG1_RS_INT_EN ISP0 Bridge1 Read clock too slow interrupt enable
0	R/W	0x0	ISP0_BRG0_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable

7.1.7.28 0x008C CSIC ISP0 Bridge Interrupt Pending Register (Default Value:0x0000_0000)

Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W1C	0x0	ISP0_BRG3_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge3 Slow to Fast Side
26	R/W1C	0x0	ISP0_BRG2_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge2 Slow to Fast Side
25	R/W1C	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W1C	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:20	/	/	/
19	R/W1C	0x0	ISP0_BRG3_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge3 Fast to Slow Side
18	R/W1C	0x0	ISP0_BRG2_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge2 Fast to Slow Side

Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W1C	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:12	/	/	/
11	R/W1C	0x0	ISP0_BRG3_BUF_OV_INT_PD ISP0 Bridge3 Buffer overflow interrupt pending
10	R/W1C	0x0	ISP0_BRG2_BUF_OV_INT_PD ISP0 Bridge2 Buffer overflow interrupt pending
9	R/W1C	0x0	ISP0_BRG1_BUF_OV_INT_PD ISP0 Bridge1 Buffer overflow interrupt pending
8	R/W1C	0x0	ISP0_BRG0_BUF_OV_INT_PD ISP0 Bridge0 Buffer overflow interrupt pending
7:4	/	/	/
3	R/W1C	0x0	ISP0_BRG3_RS_INT_PD ISP0 Bridge3 Read clock too slow interrupt pending
2	R/W1C	0x0	ISP0_BRG2_RS_INT_PD ISP0 Bridge2 Read clock too slow interrupt pending
1	R/W1C	0x0	ISP0_BRG1_RS_INT_PD ISP0 Bridge1 Read clock too slow interrupt pending
0	R/W1C	0x0	ISP0_BRG0_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending

7.1.7.29 0x00A0 CSIC DMA0 Input Select Register (Default Value:0x0000_0000)

Offset :0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA0 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0

Offset :0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
			1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.30 0x00A4 CSIC DMA1 Input Select Register (Default Value:0x0000_0000)

Offset :0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA1 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.31 0x00A8 CSIC DMA2 Input Select Register (Default Value:0x0000_0000)

Offset :0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA2 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1 1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 **Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.**

7.1.7.32 0x00AC CSIC DMA3 Input Select Register (Default Value:0x0000_0000)

Offset :0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	DMA3 Input select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 1000: input from ISP2 CH0 1001: input from ISP2 CH1

Offset :0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	Read/Write	Default/Hex	Description
			1010: input from ISP2 CH2 1011: input from ISP2 CH3 1100: input from ISP3 CH0 1101: input from ISP3 CH1 1110: input from ISP3 CH2 1111: input from ISP3 CH3 Note: No physical ISP1/2/3 exists. ISP1/2/3 is a virtual concept here and serves as the data path-to ISP MUX. This register should be configured together with CSIC_ISP1/2/3_INPUT0/1/2/3_SEL_REG.

7.1.7.33 0x00E0 CSIC BIST Control Register (Default Value:0x0000_0200)

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0:NO effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle
9	R	0x1	BIST_STOP BIST STOP 0: Running 1:Stop
8	R	0x0	BIST_BUSY BIST Busy 0: IDLE 1:Busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select
4	R/W	0x0	BIST_ADDR_MODE_SEL BIST Address Mode Select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write Data Pattern 000:0x00000000 001:0x55555555 010:0x33333333

Offset: 0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST Enable. A positive will trigger the BIST to start.

7.1.7.34 0x00E4 CSIC BIST Start Address Register (Default Value:0x0000_0000)

Offset: 0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST Start Address BIST Start Address. It is 32-bit aligned.

7.1.7.35 0x00E8 CSIC BIST End Address Register (Default Value:0x0000_0000)

Offset: 0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST END Address BIST END Address. It is 32-bit aligned.

7.1.7.36 0x00EC CSIC BIST Data Mask Register (Default Value:0x0000_0000)

Offset: 0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0: Unmask 1:Mask

7.1.7.37 0x00F0 CSIC MBUS REQ MAX Register (Default Value:0x000f_0f0f)

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
31:21	R	0x000	Reserved
20:16	R/W	0x0f	MISP_MEM_REQ_MAX (no use actually, fixed as 16) Maximum of request commands for the master granted in MISP_MEM arbiter is N+1.
15:5	/	/	/

Offset: 0x00F0			Register Name: CSIC_MBUS_REQ_MAX_REG
Bit	Read/Write	Default/Hex	Description
4:0	R/W	0x0f	MCSI_MEM_REQ_MAX Maximum of request commands for the master granted in MCSI_MEM arbiter is N+1.

7.1.7.38 0x0100 CSIC Multi-Frame Mode Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	MULF_STATUS Multi-Frame Mode Status indicates each DMA in frame done pending or not
23:16	/	/	/
15:8	R/W	0x0	MULF_CS Chip Selection for Multi-Frame Mode indicates which DMA is in selected
7:1	/	/	/
0	R/W	0x0	MULF_EN Multi-Frame Mode Enable

7.1.7.39 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	MULF_ERR_PD Multi-Frame Mode Frame Error Interrupt Pending
16	R/W1C	0x0	MULF_DONE_PD Multi-Frame Mode Frame Done Interrupt Pending
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN Multi-Frame Mode Frame Error Interrupt Enable
0	R/W	0x0	MULF_DONE_EN Multi-Frame Mode Frame Done Interrupt Enable

7.1.7.40 0x0108 CSIC Change Frequency Configuration 0 Register (Default Value:0x0001_0000)

Offset: 0x0108			Register Name: CSIC_CHFREQ_CFG0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0001	CHFREQ_PAR2ISP_SEL

Offset: 0x0108			Register Name: CSIC_CHFREQ_CFG0_REG
Bit	Read/Write	Default/Hex	Description
			Chfreq_par2isp select. Each bit corresponds to one channel. When the channel has data stream passing through, the corresponding bit must be set to 1. [19:16]->par2isp0 ch3, ch2, ch1, ch0 [23:20]->par2isp1 ch3, ch2, ch1, ch0 [27:24]->par2isp2 ch3, ch2, ch1, ch0 [31:28]->par2isp3 ch3,ch2,ch1,ch0
15:6	/	/	/
5	R/W	0x0	CHFREQ_BK_DONE_SRC Chfreq_bk done source select. 0: Select bk_frm_end as source 1: Select bk_frm_done as source
4	R/W	0x0	CHFREQ_PULSE_CNT_SCLR_EN Chfreq_pulse Cent Self-Clear Enable 0: Disable pulse cnt self clear 1: Enable pulse cnt self clear
3	R/W	0x0	CHFREQ_RDY_MASK 0: Unmask 1: Mask assert, keep chfreq_rdy output as 0
2	R/W	0x0	CHFREQ_SELECT Chfreq_rdy output source select 0: New implementation 1: Old implementation
1	R/W	0x0	CHFREQ_ALLOW Chfreq Allow Signal 0: Keep chfreq_rdy output as 0 1: Allow chfreq logic when CHFREQ_EN is asserted or all of bk*_en, mvipp*_en, and isp_en are set as 0, CHFREQ_ALLOW will not take effect.
0	R/W	0x0	CHFREQ_RST Soft reset for chfreq logic. 0: Assert 1:De-assert

7.1.7.41 0x010C CSIC Change Frequency Configuration 1 Register (Default Value:0x0000_0064)

Offset: 0x010C			Register Name: CSIC_CHFREQ_CFG1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x0000	CHFREQ_WAIT_DONE_TIME

Offset: 0x010C			Register Name: CSIC_CHFREQ_CFG1_REG
Bit	Read/Write	Default/Hex	Description
			The time between hardware chfreq frm_done assert and mcsi chfrq_rdy assert. Take one chfreq_clk cycle as the unit, which is 1 us by default.
15:0	R/W	0x0064	CHFREQ_DDR_TIME The time for DDR to complete frequency change. Take one chfreq_clk cycle as a unit, which is 1 us by default.

7.1.7.42 0x0110 CSIC Change Frequency Observation Register (Default Value:0x0000_0000)

Offset: 0x0110			Register Name: CSIC_CHFREQ_OBS_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0000	CHFREQ_FRM_DONE_TIME The time for frm done after frm_end, measured by hardware. Take one chfreq_clk cycle as the unit, which by default is 1 us.
15:0	R	0x0000	CHFREQ_VBLANK_LENGTH Vblank length measured by hardware. Take one chfreq_clk cycle as the unit, which by default is 1 us.

7.1.7.43 0x0114 CSIC Change Frequency Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0114			Register Name: CSIC_CHFREQ_INT_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W1C	0x0	CHFREQ_FRM_DONE_NUM_ERR_PD Change Frequency Frame Done Number Error Interrupt Pending
17	R/W1C	0x0	CHFREQ_FRM_END_NUM_ERR_PD Change Frequency Frame End Number Error Interrupt Pending
16	R/W1C	0x0	CHFREQ_FRM_STR_NUM_ERR_PD Change Frequency Frame Start Number Error Interrupt Pending
15:3	/	/	/
2	R/W	0x0	CHFREQ_FRM_DONE_NUM_ERR_EN Change Frequency Frame Done Number Error

Offset: 0x0114			Register Name: CSIC_CHFREQ_INT_REG
Bit	Read/Write	Default/Hex	Description
			Interrupt Enable
1	R/W	0x0	CHFREQ_FRM_END_NUM_ERR_EN Change Frequency Frame End Number Error Interrupt Enable
0	R/W	0x0	CHFREQ_FRM_STR_NUM_ERR_EN Change Frequency Frame Start Number Error Interrupt Enable

7.1.7.44 0x0118 CSIC Change Frequency Debug Observation Register (Default Value:0x0000_2101)

Offset: 0x0118			Register Name: CSIC_CHFREQ_DBG_OBS_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	CHFREQ_RSTN_T
26	R	0x0	ISP_RSTN_T
25	R	0x0	PAR_RSTN_T
24	R	0x0	POST_RSTN_T
23	R	0x0	ISP_EN_POST_S
22:18	R	0x0	FRM_DONE_SRC_NUM
17:13	R	0x1	FRM_STR_SRC_NUM
12:8	R	0x1	FRM_END_SRC_NUM
7	R	0x0	POST_EN_S
6	R	0x0	ISP_EN_S
5	R	0x0	CHFREQ_ALLOW_S
4	R	0x0	FIRST_FRM_END_RECEIVED
3	R	0x0	VBLANK_LENGTH_VALID
2	R	0x0	IN_VBLANK
1	R	0x0	FRM_DONE_TIME_VALID
0	R	0x1	CHFREQ_RDY

7.1.7.45 0x01F0 CSIC Feature List Register (Default Value:0x4411_4600)

Offset: 0x01F0			Register Name: CSIC_FEATURE_LIST_REG
Bit	Read/Write	Default/Hex	Description
31:28	R	0x4	PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x4	MCSI_NUM Only can be read when version register read enable is on.

Offset: 0x01F0			Register Name: CSIC_FEATURE_LIST_REG
Bit	Read/Write	Default/Hex	Description
23:20	R	0x1	NCSI_NUM Only can be read when version register read enable is on.
19:16	R	0x1	ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x6	DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

7.1.8 CSIC_PHY COMMON Register Description

7.1.8.1 0x0000 PHY Top Control Register (Default Value: 0x006_0500)

Offset:0x0000			Register Name: PHY_TOP_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:29	R/W	0x0	PHY_LINK_MODE PHY Link Selection 2'b00: 4 x 2-lane Links 2'b01: 2 x 2-lane + 1 x 4-lane(phya+phyb) Link 2'b10: 2 x 2-lane + 1 x 4-lane(phyc+phyd) Link 2'b11: 2 x 4-lane(phya+phyb, phyc+phyd) Link
28:27	/	/	/
26:24	R/W	0x0	PRBS_SEL PRBS Test Interface Selection 0x0: PHYA PRBS 0x1: PHYB PRBS 0x2: PHYC PRBS 0x3: PHYD PRBS Other: Reserved
23:12	/	/	/
11:10	R/W	0x1	PHY_VREF_0P2 PHY 0.2V Terminal Resistor Reference Voltage Fine Trimming Every step is 25 mV.

Offset:0x0000			Register Name: PHY_TOP_CTL_REG
Bit	Read/Write	Default/Hex	Description
9:8	R/W	0x1	PHY_VREF_0P9 PHY 0.9V LDO Reference Voltage Fine Trimming Every step is 50 mV.
7:4	/	/	/
3	R/W	0x0	PHY_LVLDO_EN PHY 0.9V LDO Enable (High Active)
2	R/W	0x0	PHY_VREF_EN PHY Reference Voltage Enable
1	R/W	0x0	PHY_RSTN PHY Analog Layer Digital Circuit Reset (Low Active)
0	R/W	0x0	PHY_PWDNZ PHY Analog Layer Power Reset (Low Active)

7.1.8.2 0x0004 PHY Terminal Resistor Calibration Register (Default Value: 0x0000_00a5)

Offset:0x0004			Register Name: PHY_TRESCAL_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R	0x0	PHY_TRESCAL_RESULT PHY Terminal Resistor Calibration Result In automatic calibration mode, the result is automatic calibration output value. In software calibration mode, the result is the value of PHY0_TRESCAL_SET bit.
15:9	/	/	/
8:4	R/W	0xa	PHY_TRESCAL_SET PHY Terminal Resistor Software Calibration Set Value
3	R	0x0	PHY_TRESCAL_FLAG PHY Terminal Resistor Calibration Flag In automatic calibration mode, when the value of this bit is 1, the automatic calibration is completed. This bit is fixed as 1 in software calibration mode.
2	R/W	0x1	PHY_TRESCAL_RESETN PHY Terminal Resistor Calibration Reset This bit is only valid for automatic calibration, low active.
1	R/W	0x0	PHY_TRESCAL_SOFT

Offset:0x0004			Register Name: PHY_TRESCAL_REG
Bit	Read/Write	Default/Hex	Description
			PHY Terminal Resistor Software Calibration Enable (High Active)
0	R/W	0x1	PHY_TRESCAL_AUTO PHY Terminal Resistor Automatic Calibration Enable (High Active)

7.1.9 CSIC_PHY DIGITAL LAYER Register Description

7.1.9.1 0x0000 PHY Control Register (Default Value: 0x0004_0000)

Offset:0x0000			Register Name: PHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PHY0_WORK_MODE 0: Every lane works in MIPI mode.
27	/	/	/
26	R/W	0x0	PHY0_IBIAS_EN PHY0 Reference Current Enable (High Active)
25:20	/	/	/
19	R/W	0x0	PHY0_VCM PHY0 Common Voltage Selection 0: 200mV（MIPI） 1: Reserved
18:16	R/W	0x4	PHY0_HS_REFI Obtain faster speed of every lane by adjusting PHY0 HSRX reference current. The larger the value of this bit, the faster the speed of every lane.
15:13	/	/	/
12	R/W	0x0	PHY0_LP_REFI Adjust the threshold voltage window size by adjusting LPRX reference current, which is able to filter LP noise signals effectively.
11:9	/	/	/
8	R/W	0x0	PHY_LANECK_EN PHY Clock Lane Enable
7:6	/	/	/
5:4	R/W	0x0	PHY_LANEDT_EN PHY Data Lane0-1 Enable
3:1	/	/	/
0	R/W	0x0	PHY_EN

Offset:0x0000			Register Name: PHY_CTL_REG
Bit	Read/Write	Default/Hex	Description
			PHY Digital Layer Enable (High Active)

7.1.9.2 0x0004 PHY Equalization Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: PHY_EQ_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	PHY_EQ_LANECK0 PHY clock lane0 comparator equalization compensation value
23:20	/	/	/
19:18	R/W	0x0	PHY_EQ_LANED1 PHYC data lane1 comparator equalization compensation value
17:16	R/W	0x0	PHY_EQ_LANED0 PHY data lane0 comparator equalization compensation value
15:5	/	/	/
4:4	R/W	0x0	PHY_EQ_CK_EN PHY clock lane comparator equalization enable (high active)
3:0	R/W	0x0	PHY_EQ_DT_EN PHY data lane0-1 comparator equalization enable (high active) Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: reserved

7.1.9.3 0x0008 PHY Offset Calibration Register0 (Default Value: 0x0010_0010)

Offset:0x0008			Register Name: PHY_OFSCAL_REG0
Bit	Read/Write	Default/Hex	Description
31:39	/	/	/
28	R	0x0	PHY0_OFSCAL_FLAG PHY0 Offset Calibration Flag In automatic calibration mode, when the value of this bit is 1, the automatic calibration is completed. This bit is fixed as 1 in software calibration mode.

Offset:0x0008			Register Name: PHY_OFSCAL_REG0
Bit	Read/Write	Default/Hex	Description
27:21	/	/	/
20	R/W	0x1	PHY0_OFSCAL_RESETN PHY0 Offset Calibration Reset The comparator offset of every lane restarts to calibrate after reset. **Note: This bit is only valid for automatic calibration mode.**
19:13	/	/	/
12	R/W	0x0	PHY0_OFSCAL_SOFT PHY0 offset software calibration enable (high active)
7:6	/	/	/
4	R/W	0x1	PHY_OFSCAL_AUTO PHY0 offset automatic calibration enable (high active)
3:0	/	/	/

7.1.9.4 0x000C PHY Offset Calibration Register1 (Default Value: 0x0120_0000)

Offset: 0x000C			Register Name: PHY_OFSCAL_REG1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R/W	0x12	PHY0_OFSCAL_SET PHY0 offset software calibration set value
19:0	/	/	/

7.1.9.5 0x0010 PHY Offset Calibration Register2(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PHY_OFSCAL_REG2
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R	0x0	PHY0_OFSCAL_RESULT PHY0 offset calibration result In automatic calibration mode, the result is automatic calibration output value. In software calibration mode, the result is the value of PHY0_OFSCAL_SET bit.
19:0	/	/	/

7.1.9.6 0x0014 PHY Deskew Register0 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: PHY_DESKEW_REG0
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	PHY0_DESKEW_STEP PHY0 data lane initial deskew step precision 00: Every step is 1. 01: Every step is 2. 10: Every step is 4. 11: Reserved
7:6	/	/	/
5:4	R/W	0x0	PHY_DESKEW_PERIOD_EN PHY data lane0-1 period deskew automatic delay enable (high active)
3:2	/	/	/
1:0	R/W	0x0	PHY_DESKEW_EN PHY data lane0-1 deskew automatic delay enable (high active)

7.1.9.7 0x0018 PHY Deskew Register1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PHY_DESKEW_REG1
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:20	R/W	0x0	PHY_DESKEW_LANECK0_SET PHY clock lane0 delay
19:10	/	/	/
9:5	R/W	0x0	PHY_DESKEW_LANED1_SET PHY data lane1 delay This bit is valid when PHY_DESKEW_EN[1] =1.
4:0	R/W	0x0	PHY_DESKEW_LANED0_SET PHY data lane0 delay This bit is valid when PHY_DESKEW_EN[0] =0.

7.1.9.8 0x001C PHY Deskew Register2(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PHY_DESKEW_REG2
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
24:20	R	0x0	PHY_DESKEW_LANECK0_RESULT PHY clock lane0 deskew delay result

Offset: 0x001C			Register Name: PHY_DESKEW_REG2
Bit	Read/Write	Default/Hex	Description
			The value of this bit is equal to the value of PHY_DESKEW_LANECK0_SET bit.
19:10	/	/	/
9:5	R	0x0	PHY_DESKEW_LANED1_RESULT PHY data lane1 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK1_SET bit, when PHY_DESKEW_EN[1] =1.
4:0	R	0x0	PHY_DESKEW_LANED0_RESULT PHY data lane0 deskew delay result The value of this bit is equal to the value of PHY_DESKEW_LANECK0_SET bit, when PHY_DESKEW_EN[0] =0.

7.1.9.9 0x0020 PHY Terminal Control Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PHY_TERM_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_TERM_EN_DLY These bits are to set the delay of every clock lane and data lane from high-speed RX (LP11-LP01-LP00) request is received to the terminal resistor is enabled in hardware auto-enable mode. These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:5	/	/	/
4	R/W	0x0	PHY_TERMCK_EN PHY Clock Lane Terminal Resistor Software Enable 0: Hardware auto-enable 1: Software enable
3:0	R/W	0x0	PHY_TERMDT_EN PHY Data Lane 0-1 Terminal Resistor Software Enable 0: Hardware auto-enable 1: Software enable Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved

7.1.9.10 0x0024 PHY High Speed Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PHY_HS_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_HS_DLY These bits are to set the delay of every clock lane and data lane from high-speed RX (LP11-LP01-LP00) request is received to the high-speed comparator is enabled in hardware auto-enable mode. These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:13	/	/	/
12	R/W	0x0	PHY_HSCK_POLAR PHY Clock Lane HSRX Signal Inversion 0: HSRX Signal is not inverse. 1: HSRX Signal is inverse.
11:8	R/W	0x0	PHY_HSDT_POLAR PHY Data Lane0-1 HSRX Signal Inversion 0: HSRX Signal is not inverse. 1: HSRX Signal is inverse.
7:5	/	/	/
4	R/W	0x0	PHY_HSCK_EN PHY Clock Lane High-Speed Mode Software Enable (High Active) 0: Hardware auto-enable 1: Software enable
3:0	R/W	0x0	PHY_HSDT_EN PHY Data Lane0-1 High-Speed Mode Software Enable (High Active) 0: Hardware auto-enable 1: Software enable Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved

7.1.9.11 0x0028 PHY Serial to Parallel Control Register (Default Value: 0x0000_0A00)

Offset: 0x0028			Register Name: PHY_S2P_CTL_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x0028			Register Name: PHY_S2P_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_S2P_DLY These bits are to set the delay of every data lane from high-speed RX request is received to the S2P circuit is enabled in hardware auto-enable mode (HS_Settle). These bits are only valid for MIPI CSI. The unit is cmb_clk cycle.
15:10	/	/	/
9:8	R/W	0x2	PHY0_S2P_WIDTH PHY0 S2P Circuit Output Width 00: 2 bits 01: 4 bits 1X: 8 bits
7:4	/	/	/
3:0	R/W	0x0	PHY_S2P_EN PHY Data Lane0-1 S2P Circuit Software Enable 0: Hardware auto-enable 1: Software enable Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved

7.1.9.12 0x002C PHY MIPIRX Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PHY_MIPIRX_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PHY0_MIPILP_DBC_EN PHY0 LPRX Debounce Circuit Enable (High Active)
15:13	/	/	/
12	R/W	0x0	PHY_MIPI_LPCK_EN PHY Clock Lane LPRX Enable 0: Disable LPRX 1: Enable LPRX
11:8	R/W	0x0	PHY_MIPI_LPDT_EN PHY Data Lane 0-1 LPRX Enable 0: Disable LPRX 1: Enable LPRX

Offset: 0x002C			Register Name: PHY_MIPIRX_CTL_REG
Bit	Read/Write	Default/Hex	Description
			Bit0: data lane0 enable Bit1: data lane1 enable Bit2/3: Reserved
7:5	/	/	/
4	R/W	0x0	PHY0_MIPIHS_8B9B 0: No 8B9B decoding when receiving bytes in PHY0 MIPI high-speed mode. 1: 8B9B decoding when receiving bytes in PHY0 MIPI high-speed mode.
3	/	/	/
2	R/W	0x0	PHY0_MIPIHS_SYNC_MODE 0: The Sync-Sequence must be 0xb8 in PHY0 MIPI high-speed mode. 1: The Sync-Sequence allows 1-bit difference from 0xb8 in PHY0 MIPI high-speed mode.
1	/	/	/
0	R/W	0x0	PHY0_MIPIHS_ENDIAN This bit is to set which one of the big-endian and little-endian to receive data in PHY0 MIPI high-speed mode. 0: LSB First 1: MSB First

7.1.9.13 0x0030 PHY MIPIRX Synchronization Timeout Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PHY_MIPIRX_SYNC_TIMEOUT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_MIPIHS_SYNC_TOSET The PHY_NOSYNC_ERR_D0_PD bit and PHY_NOSYNC_ERR_D1_PD bit will generate interrupts when the Sync-Sequence (0xb8) is unable to be detected after PHY0 data lane switching from LP mode to HS mode for a period of time configured by this bit. The unit is 16 byte_clk cycles.
15:1	/	/	/
0	R/W	0x0	PHY0_MIPIHS_SYNC_TOEN PHY0 data lane HS Sync-Sequence Detection Time Out Enable (High Active)

7.1.9.14 0x0034 PHY Frequency Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PHY_FREQ_CNT _REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PHY_FREQ_CNT The value of these bits is the number of cmb_clk cycle during 1000 PHY byte clk cycles, which is used for byte clk frequency conversion of PHY0 or PHY1. The unit is cmb_clk cycle.
15:1	/	/	/
0	R/W	0x0	PHY0_FREQ_EN PHY0 byte_clk frequency detection enable (high active)

7.1.9.15 0x0038 PHY MIPI LP Timeout Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PHY_MIPI_LP_TIMEOUT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PHY0_MIPI_LP_TIMEOUT_SET By default, the LP value will be refreshed when PHY0 MIPI LP signal bounce occurs. After enabling PHY0_MIPI_LP_TIMEOUT_EN bit, even if the signal bounce does not occur, the LP value will be refreshed after the time set by this bit. The unit is cmb_clk cycle.
15:1	/	/	/
0	R/W	0x0	PHY0_MIPI_LP_TIMEOUT_EN By default, the LP value will be refreshed when PHY0 MIPI LP signal bounce occurs. After enabling this bit, even if the signal bounce does not occur, the LP value will be refreshed after the time set by the PHY0_MIPI_LP_TIMEOUT_SET bit.

7.1.9.16 0x0040 PHY MIPI ULPSEXIT Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PHY_MIPI_ULPSEXIT_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY0_MIPI_ULPS_EN Enter ULPS status after the ULPS instruction is detected by PHY0 lane.

Offset: 0x0040			Register Name: PHY_MIPI_ULPSEXIT_REG0
Bit	Read/Write	Default/Hex	Description
30:20	/	/	/
19:0	R/W	0x0	PHY0_MIPI_ULPSEXIT PHY0 lane needs to keep detecting Mark 1 signal for a certain period of time before exiting ULPS status. The unit is cmb_clk cycle.

7.1.9.17 0x0080 PHY Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PHY_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	PHY_LP_CK0_CMD_EN PHY Clock Lane0 Interrupt Enable An interrupt is to be generated after recognizable LP commands are received by PHY clock lane0.
15:14	/	/	/
13	R/W	0x0	PHY_LP_D1_CMD_EN PHY Data Lane1 Interrupt Enable An interrupt is to be generated after recognizable LP commands are received by PHY data lane1.
12	R/W	0x0	PHY_LP_D0_CMD_EN PHY Data Lane0 Interrupt Enable An interrupt is to be generated after recognizable LP commands are received by PHY data lane0.
11:10	/	/	/
9	R/W	0x0	PHY_NOSYNC_ERR_D1_EN PHY Sync-Sequence Error Interrupt Enable An interrupt is to be generated, if the Sync-Sequence is unable to be detected a period of time after data lane1 is switched from LP mode to HS mode.
8	R/W	0x0	PHY_NOSYNC_ERR_D0_EN PHY Sync-Sequence Error Interrupt Enable An interrupt is to be generated, if the Sync-Sequence is unable to be detected a period of time after data lane0 is switched from LP mode to HS mode.
7:6	/	/	/
5	R/W	0x0	PHY_SYNC_ERR_D1_EN

Offset: 0x0080			Register Name: PHY_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			This bit is to enable the interrupt generation when 1-bit error is detected in the data lane1 Sync-Sequence.
4	R/W	0x0	PHY_SYNC_ERR_D0_EN This bit is to enable the interrupt generation when 1-bit error is detected in the data lane0 Sync-Sequence.
3:2	/	/	/
1	R/W	0x0	PHY_SOTDET_D1_EN Generate an interrupt after the Sync-Sequence is detected in Data lane1.
0	R/W	0x0	PHY_SOTDET_D0_EN Generate an interrupt after the Sync-Sequence is detected in Data lane0.

7.1.9.18 0x0084 PHY Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: PHY_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W1C	0x0	PHY_LP_CK0_CMD_PD Generate an interrupt after PHY clock lane0 receives recognizable LP commands.
15:14	/	/	/
13	R/W1C	0x0	PHY_LP_D1_CMD_PD Generate an interrupt after PHY clock lane1 receives recognizable LP commands.
12	R/W1C	0x0	PHY_LP_D0_CMD_PD Generate an interrupt after PHY data lane0 receives recognizable LP commands.
11:10	/	/	/
9	R/W1C	0x0	PHY_NOSYNC_ERR_D1_PD Generate an interrupt when the Sync-Sequence is unable to be detected a period of time after data lane1 is switched from LP mode to HS mode.
8	R/W1C	0x0	PHY_NOSYNC_ERR_D0_PD Generate an interrupt when the Sync-Sequence is unable to be detected a period of time after data lane0 is switched from LP mode to HS mode.
7:6	/	/	/

Offset: 0x0084			Register Name: PHY_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
5	R/W1C	0x0	PHY_SYNC_ERR_D1_PD Generate an interrupt after 1-bit error is detected in the data lane1 Sync-Sequence.
4	R/W1C	0x0	PHY_SYNC_ERR_D0_PD Generate an interrupt after 1-bit error is detected in the data lane0 Sync-Sequence.
3:2	/	/	/
1	R/W1C	0x0	PHY_SOTDET_D1_PD Generate an interrupt after the Sync-Sequence is detected in data lane1.
0	R/W1C	0x0	PHY_SOTDET_D0_PD Generate an interrupt after the Sync-Sequence is detected in data lane0.

7.1.10 CSIC_PHY PORT PAYLOAD LAYER Register Description

7.1.10.1 0x0000 PORT Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: PORT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT_OUT_NUM 0: Output 1 data every valid 1: Output 2 data every valid
30:18	/	/	/
17:16	R/W	0x0	PORT_CHANNEL_NUM 0: 1 channel 1: 2 channels 2: 3 channels 3: 4 channels
15:12	/	/	/
11:8	R/W	0x0	PORT_LANE_NUM MIPI: 1-4 PORT0 and PORT2 support maximum 4 lanes. PORT1 and PORT3 support maximum 2 lanes.
7:6	/	/	/
5:4	R/W	0x0	PORT_WORK_MODE 00: PORT channels work in MIPI mode. 01: Reserved
3:1	/	/	/
0	R/W	0x0	PORT_EN

Offset: 0x0000			Register Name: PORT_CTL_REG
Bit	Read/Write	Default/Hex	Description
			PORT Channel Enable (High Active)

7.1.10.2 0x0004 PORT Lane Mapping Register0 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0x0	PORT_LANE3_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE3 0x1: Set lane1 (PHYA lane1) as PORT LANE3 0x4: Set lane4 (PHYB lane0) as PORT LANE3 0x5: Set lane5 (PHYB lane1) as PORT LANE3 0x8: Set lane8 (PHYC lane0) as PORT LANE3 0x9: Set lane9 (PHYC lane1) as PORT LANE3 0xc: Set lane12 (PHYD lane0) as PORT LANE3 0xd: Set lane13 (PHYD lane1) as PORT LANE3
11:8	R/W	0x0	PORT_LANE2_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE2 0x1: Set lane1 (PHYA lane1) as PORT LANE2 0x4: Set lane4 (PHYB lane0) as PORT LANE2 0x5: Set lane5 (PHYB lane1) as PORT LANE2 0x8: Set lane8 (PHYC lane0) as PORT LANE2 0x9: Set lane9 (PHYC lane1) as PORT LANE2 0xc: Set lane12 (PHYD lane0) as PORT LANE2 0xd: Set lane13 (PHYD lane1) as PORT LANE2
7:4	R/W	0x0	PORT_LANE1_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE1 0x1: Set lane1 (PHYA lane1) as PORT LANE1 0x4: Set lane4 (PHYB lane0) as PORT LANE1 0x5: Set lane5 (PHYB lane1) as PORT LANE1 0x8: Set lane8 (PHYC lane0) as PORT LANE1 0x9: Set lane9 (PHYC lane1) as PORT LANE1 0xc: Set lane12 (PHYD lane0) as PORT LANE1 0xd: Set lane13 (PHYD lane1) as PORT LANE1
3:0	R/W	0x0	PORT_LANE0_ID 0x0: Set lane0 (PHYA lane0) as PORT LANE0 0x1: Set lane1 (PHYA lane1) as PORT LANE0 0x4: Set lane4 (PHYB lane0) as PORT LANE0 0x5: Set lane5 (PHYB lane1) as PORT LANE0 0x8: Set lane8 (PHYC lane0) as PORT LANE0 0x9: Set lane9 (PHYC lane1) as PORT LANE0

Offset: 0x0004			Register Name: PORT_LANE_MAP_REG0
Bit	Read/Write	Default/Hex	Description
			0xc: Set lane12 (PHYD lane0) as PORT LANE0 0xd: Set lane13 (PHYD lane1) as PORT LANE0

7.1.10.3 0x000C PORT WDR Mode Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PORT_WDR_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PORT_WDR_MODE 0x0: Normal mode, No WDR, MIPI VC, or MIPIDT. 0x2: Pixel data mode, distinguish the multi-channel WDR/HR images through the first pixel data of each line. others：Reserved

7.1.10.4 0x0010 PORT Frame ID Select Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PORT_FID_SEL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PORT_FID_MODE 0: Identify the Frame in bit cs mode. For example, identify Frame0 when FID [0] =1, identify Frame1 when FID [1] =1. 1: Identify the Frame in bit value mode. For example, identify Frame0 when FID [0] =0, identify Frame1 when FID [0] =1.
30:20	/	/	/
19:16	R/W	0x0	PORT_FID_MAP_EN FID Mapping Enable Bit19: FID3_MAP_EN Bit18: FID2_MAP_EN Bit17: FID1_MAP_EN Bit16: FID0_MAP_EN
15:12	R/W	0x0	PORT_FID3_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID3 in the first pixel data of every line.
11:8	R/W	0x0	PORT_FID2_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID2 in the first

Offset: 0x0010			Register Name: PORT_FID_SEL_REG
Bit	Read/Write	Default/Hex	Description
			pixel data of every line.
7:4	R/W	0x0	PORT_FID1_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID1 in the first pixel data of every line.
3:0	R/W	0x0	PORT_FID0_MAP These bits indicate the bit position with a 16-bit high-order aligned address for FID0 in the first pixel data of every line.

7.1.10.5 0x0100 PORT MIPI Configuration Register (Default Value: 0x4920_0000)

Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:26	R/W	0x12	MIPI_REAR_EMB_DTYPE MIPI Rear Embedded Data Type Value
25:20	R/W	0x12	MIPI_FRONT_EMB_DTYPE MIPI Front Embedded Data Type Value
19	R/W	0x0	MIPI_EMB_MAP The MIPI received embedded data is output in a certain format. 0: Output in the pixel format of the corresponding channel. 1: Output in RAW8 format.
18	/	/	/
17:16	R/W	0x0	MIPI_YUV_SEQ MIPI YUV Format Transmission Sequence 00: YUYV 01: YVYU 10: UYVY 11: VYUY
15:10	/	/	/
9	R/W	0x0	MIPI_FRAME_SYNC_ONLY_FS MIPI Frame Synchronization only for Frame Start 0: No support 1: Support
8	R/W	0x0	MIPI_LINE_SYNC_EN MIPI Line Synchronization Enable 0: Generate line sync signals based on long packets 1: Generate line sync signals based on short

Offset: 0x0100			Register Name: PORT_MIPI_CFG_REG
Bit	Read/Write	Default/Hex	Description
			packets
7	R/W	0x0	MIPI_PL_BITORD MIPI RX Payload Bit Sequence 0: LSb First 1: MSb First
6	R/W	0x0	MIPI_PH_BITORD MIPI Packet Header Bit Sequence (for ECC checksum) 0: LSb First, for example, {WC [15:8], WC[7:0], DI[7:0]} 1: MSb First, for example,{WC[8:15],WC[0:7], DI[0:7]}
5:4	R/W	0x0	MIPI_PH_BYTEORD MIPI Packet Header Byte Sequence (for ECC check) 0: {WCH, WCL, DI} 1: {DI, WCH, WCL} 2: {WCL, WCH, DI} 3: {DI,WCL,WCH}
3	R/W	0x0	MIPI_USER_DEF_EN MIPI USER Define Data Type Enable
2	R/W	0x0	EMBED_EN embed data receiving enable and output in the pixel format of the corresponding channel.
1	R/W	0x0	MIPI_NO_UNPACK_ALL MIPI_UNPACK_EN=0: Receive data directly without unpacking. MIPI_NO_UNPACK_ALL=0: Only receive effective high-speed data without unpacking and output them from PORT Channel0 in RAW8 format. MIPI_NO_UNPACK_ALL =1: Receive rxhs_active, rxhs_valid, and rxhs_data[7:0] simultaneously as RX data and output them from PORT Channel0 in {2'h0，rxhs_active, rxhs_valid, rxhs_data[7:0]} sequence in RAW12 format.
0	R/W	0x0	MIPI_UNPACK_EN MIPI CSI2 Protocol Unpack Enable

7.1.10.6 0x0104 PORT MIPI No Unpacket Number Register (Default Value: 0x0000_0000)

Offset: 0x0104	Register Name: PORT_MIPI_NO_UNPAK_NUM_REG

Bit	Read/Write	Default/Hex	Description
31:00	R/W	0x0	MIPI_NO_UNPAK_NUM_REG This bit indicates the number of received raw data. The unit is pixel component.

7.1.10.7 0x0108 PORT MIPI Data Identity Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PORT_MIPI_DI_REG
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	MIPI_CH3_VC MIPI Channel3 VC Number Set
29:24	R/W	0x0	MIPI_CH3_DT MIPI Channel3 Data Type Set
23:22	R/W	0x0	MIPI_CH2_VC MIPI channel2 VC Number Set
21:16	R/W	0x0	MIPI_CH2_DT MIPI Channel2 Data Type Set
15:14	R/W	0x0	MIPI_CH1_VC MIPI Channel1 VC Number Set
13:8	R/W	0x0	MIPI_CH1_DT MIPI Channel1 Data Type Set
7:6	R/W	0x0	MIPI_CH0_VC MIPI channel0 VC Number Set
5:0	R/W	0x0	MIPI_CH0_DT MIPI Channel0 Data Type Set/Real Mapping of USER Define Data Type

7.1.10.8 0x010C PORT MIPI User Data Type Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PORT_MIPI_USER_DT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_USER3_DT_EN Channel3 MIPI USER Define Data Type Enable
30	/	/	/
29:24	R/W	0x0	MIPI_USER3_DT Channel3 MIPI USER Define Data Type This bit is to identify the data belonging to channel3, which is unpacked into the data type set by the MIPI_CH3_DT bit following CSI2 protocol.
23	R/W	0x0	MIPI_USER2_DT_EN Channel2 MIPI USER Define Data Type Enable
22	/	/	/

Offset: 0x010C			Register Name: PORT_MIPI_USER_DT_REG
Bit	Read/Write	Default/Hex	Description
21:16	R/W	0x0	MIPI_USER2_DT Channel2 MIPI USER Define Data Type This bit is to identify the data belonging to channel2, which is unpacked into the data type set by the MIPI_CH2_DT bit following CSI2 protocol.
15	R/W	0x0	MIPI_USER1_DT_EN Channel1 MIPI USER Define Data Type Enable
14	/	/	/
13:8	R/W	0x0	MIPI_USER1_DT Channel1 MIPI USER Define Data Type This bit is to identify the data belonging to channel1, which is unpacked into the data type set by the MIPI_CH1_DT bit following CSI2 protocol.
7	R/W	0x0	MIPI_USER0_DT_EN Channel0 MIPI USER Define Data Type
6	/	/	/
5:0	R/W	0x0	MIPI_USER0_DT Channel0 MIPI USER Define Data Type This bit is to identify the data belonging to channel0, which is unpacked into the data type set by the MIPI_CH0_DT bit following CSI2 protocol.

7.1.10.9 0x0110 PORT MIPI Channel0 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0
28:20	/	/	/

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked

Offset: 0x0110			Register Name: PORT_MIPI_CH0_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.10 0x0114 PORT MIPI Channel0 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PORT_MIPI_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN

Offset: 0x0114			Register Name: PORT_MIPI_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

7.1.10.11 0x0118 PORT MIPI Channel0 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PORT_MIPI_CH0_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD

Offset: 0x0118			Register Name: PORT_MIPI_CH0_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
			ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.12 0x011C PORT MIPI Channel0 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PORT_MIPI_CH0_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.13 0x0120 PORT MIPI Channel0 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PORT_MIPI_CH0_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC

Offset: 0x0120			Register Name: PORT_MIPI_CH0_ECC_REG
Bit	Read/Write	Default/Hex	Description
			MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.14 0x0124 PORT MIPI Channel0 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PORT_MIPI_CH0_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.15 0x0128 PORT MIPI Channel0 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PORT_MIPI_CH0_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.16 0x012C PORT MIPI Channel0 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PORT_MIPI_CH0_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.17 0x0130 PORT MIPI Channel1 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable:

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS

Offset: 0x0130			Register Name: PORT_MIPI_CH1_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.18 0x0134 PORT MIPI Channel1 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: PORT_MIPI_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable

Offset: 0x0134			Register Name: PORT_MIPI_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: Enable

7.1.10.19 0x0138 PORT MIPI Channel1 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: PORT_MIPI_CH1_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.20 0x013C PORT MIPI Channel1 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PORT_MIPI_CH1_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter

Offset: 0x013C			Register Name: PORT_MIPI_CH1_PH_REG
Bit	Read/Write	Default/Hex	Description
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.21 0x0140 PORT MIPI Channel1 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PORT_MIPI_CH1_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.22 0x0144 PORT MIPI Channel1 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PORT_MIPI_CH1_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.23 0x0148 PORT MIPI Channel1 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PORT_MIPI_CH1_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.24 0x014C PORT MIPI Channel1 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x014C			Register Name: PORT_MIPI_CH1_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x014C			Register Name: PORT_MIPI_CH1_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.25 0x0150 PORT MIPI Channel2 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field Polarity 0: Positive (frm num [0] =1 indicate odd, =0 indicate even) 1: Negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked 1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked 1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable:

Offset: 0x0150			Register Name: PORT_MIPI_CH2_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.26 0x0154 PORT MIPI Channel2 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: PORT_MIPI_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable

Offset: 0x0154			Register Name: PORT_MIPI_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

7.1.10.27 0x0158 PORT MIPI Channel2 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PORT_MIPI_CH2_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt

Offset: 0x0158			Register Name: PORT_MIPI_CH2_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.28 0x015C PORT MIPI Channel2 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PORT_MIPI_CH2_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.29 0x0160 PORT MIPI Channel2 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PORT_MIPI_CH2_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.30 0x0164 PORT MIPI Channel2 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PORT_MIPI_CH2_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.31 0x0168 PORT MIPI Channel2 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PORT_MIPI_CH2_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.32 0x016C PORT MIPI Channel2 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: PORT_MIPI_CH2_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.33 0x0170 PORT MIPI Channel3 Data Type Trigger Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MIPI_FIELD_REV Field polarity 0: positive (frm num [0] =1 indicate odd, =0 indicate even) 1: negative (frm num [0] =0 indicate odd, =1 indicate even) This bit is only valid when MIPI_SRC_IS_FIELD = 1.
30	R/W	0x0	MIPI_SRC_IS_FIELD 0: The MIPI input is progressive data. 1: The MIPI input is interlaced data.
29	R/W	0x0	MIPI_RAW_EXTEND Data Type RAW24/20/16 to RAW12/10/8 0: Masked 1: Enable
28:20	/	/	/
19	R/W	0x0	RAW RAW Long Packet Data Type 0x28 to 0x2F Trigger Enable: 0: Masked

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: Enabled
18	R/W	0x0	RGB RGB Long Packet Data Type 0x20 to 0x27 Trigger Enable: 0: Masked 1: Enabled
17	R/W	0x0	YUV YUV Long Packet Data Type 0x18 to 0x1F Trigger Enable: 0: Masked 1: Enabled
16	R/W	0x0	GL Generic 8bit Long Packet Data Type 0x10 to 0x17 Trigger Enable: 0: Masked 1: Enabled
15	R/W	0x0	GS7 Generic 8bit Short Packet Data Type 0x0F Trigger Enable: 0: Masked 1: Enabled
14	R/W	0x0	GS6 Generic Short Packet Data Type 0x0E Trigger Enable: 0: Masked 1: Enabled
13	R/W	0x0	GS5 Generic Short Packet Data Type 0x0D Trigger Enable: 0: Masked 1: Enabled
12	R/W	0x0	GS4 Generic Short Packet Data Type 0x0C Trigger Enable: 0: Masked 1: Enabled
11	R/W	0x0	GS3 Generic Short Packet Data Type 0x0B Trigger Enable: 0: Masked 1: Enabled
10	R/W	0x0	GS2 Generic Short Packet Data Type 0x0A Trigger Enable: 0: Masked

Offset: 0x0170			Register Name: PORT_MIPI_CH3_DT_TRIG_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: Enabled
9	R/W	0x0	GS1 Generic Short Packet Data Type 0x09 Trigger Enable: 0: Masked 1: Enabled
8	R/W	0x0	GS0 Generic Short Packet Data Type 0x08 Trigger Enable: 0: Masked 1: Enabled
7:4	/	/	/
3	R/W	0x0	LE Data Type 0x03 Trigger Enable: 0: Masked 1: Enabled
2	R/W	0x0	LS Data Type 0x02 Trigger Enable: 0: Masked 1: Enabled
1	R/W	0x0	FE Data Type 0x01 Trigger Enable: 0: Masked 1: Enabled
0	R/W	0x0	FS Data Type 0x00 Trigger Enable: 0: Masked 1: Enabled

7.1.10.34 0x0174 PORT MIPI Channel3 Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PORT_MIPI_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	EOT_ERR_INT_EN EOT error interrupt enable
11	R/W	0x0	CHKSUM_ERR_INT_EN Checksum error interrupt enable
10	R/W	0x0	ECC_ERR_INT_EN ECC error interrupt enable
9	R/W	0x0	ECC_WRN_INT_EN ECC warning interrupt enable

Offset: 0x0174			Register Name: PORT_MIPI_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
8	R/W	0x0	LINE_SYNC_ERR_INT_EN Line synchronization error interrupt enable
7	R/W	0x0	FRAME_SYNC_ERR_INT_EN Frame synchronization error interrupt enable
6	R/W	0x0	EMBED_SYNC_INT_EN Embedded data interrupt enable
5	R/W	0x0	LINE_END_SYNC_INT_EN LE synchronization interrupt enable
4	R/W	0x0	LINE_START_SYNC_INT_EN LS synchronization interrupt enable
3	R/W	0x0	FRAME_END_SYNC_INT_EN FE synchronization interrupt enable
2	R/W	0x0	FRAME_START_SYNC_INT_EN FS synchronization interrupt enable 0: Disable 1: Enable
1	R/W	0x0	PF_SYNC_INT_EN Packet Footer detected interrupt enable 0: Disable 1: Enable
0	R/W	0x0	PH_SYNC_INT_EN Packet Header update interrupt enable 0: Disable 1: Enable

7.1.10.35 0x0178 PORT MIPI Channel3 Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PORT_MIPI_CH3_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	EOT_ERR_INT_PD EOT error interrupt
11	R/W1C	0x0	CHKSUM_ERR_INT_PD Checksum error interrupt
10	R/W1C	0x0	ECC_ERR_INT_PD ECC error interrupt
9	R/W1C	0x0	ECC_WRN_INT_PD ECC warning interrupt
8	R/W1C	0x0	LINE_SYNC_ERR_INT_PD Line synchronization error interrupt

Offset: 0x0178			Register Name: PORT_MIPI_CH3_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	FRAME_SYNC_ERR_INT_PD Frame synchronization error interrupt
6	R/W1C	0x0	EMBED_SYNC_INT_PD Embedded data interrupt
5	R/W1C	0x0	LINE_END_SYNC_INT_PD LE synchronization interrupt
4	R/W1C	0x0	LINE_START_SYNC_INT_PD LS synchronization interrupt
3	R/W1C	0x0	FRAME_END_SYNC_INT_PD FE synchronization interrupt
2	R/W1C	0x0	FRAME_START_SYNC_INT_PD FS synchronization interrupt
1	R/W1C	0x0	PF_SYNC_INT_PD Packet Footer detected interrupt
0	R/W1C	0x0	PH_SYNC_INT_PD Packet Header update interrupt

7.1.10.36 0x017C PORT MIPI Channel3 Packet Header Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PORT_MIPI_CH3_PH_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CUR_WC MIPI current Word Counter
15:8	/	/	/
7:6	R	0x0	MIPI_CUR_VC MIPI current Virtual Channel
5:0	R	0x0	PORT_MIPI_CUR_DT MIPI current Data Type

7.1.10.37 0x0180 PORT MIPI Channel3 ECC Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PORT_MIPI_CH3_ECC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	MIPI_CAL_ECC MIPI calculated ECC
15:8	/	/	/
7:0	R	0x0	MIPI_RXD_ECC MIPI received ECC

7.1.10.38 0x0184 PORT MIPI Channel3 Checksum Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: PORT_MIPI_CH3_CKSUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	MIPI_CAL_CKSUM MIPI calculated Checksum
15:0	R	0x0	MIPI_RXD_CKSUM MIPI received Checksum

7.1.10.39 0x0188 PORT MIPI Channel3 Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: PORT_MIPI_CH3_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	FRAME_NUM Update when FRAME_START_SYNC_INT_PD and FRAME_END_SYNC_INT_PD comes

7.1.10.40 0x018C PORT MIPI Channel3 Line Number Register (Default Value: 0x0000_0000)

Offset: 0x018C			Register Name: PORT_MIPI_CH3_LINE_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	LINE_NUM Update when LINE_START_SYNC_INT_PD and LINE_END_SYNC_INT_PD comes

7.1.10.41 0x01F0 PORT MIPI Lane Error Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: PORT_MIPI_LANE_ERR_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0x0	MIPI_LANE_ACT_NO_VLD_INT_EN Data lane0-3 receive no valid data when act high interrupt enable
3:0	R/W	0x0	MIPI_LANE_FIFO_OVERFLOW_INT_EN Data lane0-3 FIFO overflow interrupt enable

7.1.10.42 0x01F4 PORT MIPI Lane Error Interrupt Pending Register (Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: PORT_MIPI_LANE_ERR_INT_PD_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W1C	0x0	MIPI_LANE_ACT_NO_VLD_INT_PD Data lane0-3 receive no valid data when act high interrupt
3:0	R/W1C	0x0	MIPI_LANE_FIFO_OVERFLOW_INT_PD Data lane0-3 FIFO overflow interrupt

7.1.11 CSIC_PARSER Register Description

7.1.11.1 0x0000 CSIC Parser Enable Register (Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/
16	R/W	0x0	NCSIC_EN NCSI Controller Enable 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN NCSI Pixel Clock Gating 0: Gate pclk input 1:Enable pclk input
14:4	/	/	/
3:2	R/W	0x0	PRS_CH_MODE Parser channel mode 00: Parser output channel 0-3 corresponding from input channel 0-3 01: Parser output channel 0-3 all from input channel 0 10: Parser output channel0 and 2 from input channel 0, output channel1 and 3 from input channel 1 11: Reserved
1	R/W	0x0	PRS_MODE Parser Mode 0: NCSI

Offset: 0x0000			Register Name: CSIC_PRS_EN_REG
Bit	Read/Write	Default/Hex	Description
			1: MCSI
0	R/W	0x0	PRS_EN Parser Enable 0: Reset and disable the parser module 1: Enable the parser module

7.1.11.2 0x0004 CSIC Parser NCSIC Interface Configuration Register (Default Value:0x0105_0080)

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER YUV420 Input Line Order 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30	R/W	0x0	ONLY_ACT_CARE 1:only care V active period
29	R/W	0x0	YUV422_SEP When input format is YUV422 16bit or Bt1120, set this bit to transfer YU,YV(2 components for each clock cycle) to Y,U,Y,V(1 component for each clock cycle)
28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode, the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:20	R/W	0x0	SRC_TYPE Bit 20-23 corresponding to the Source types for channel0-3 0: Progressed 1: Interlaced
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: Negative (field=0 indicate odd, field=1 indicate even) 1: Positive (field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	FIELD_DT_MODE only valid when CSI_IF is YUV and source type is interlaced 00:by both field and vsync 01:by field 10:by vsync 11:reserved
13	R/W	0x0	DDR_SAMPLE_MODE_EN Dual Data Rate Sample Mode Enable 0: Disable 1:Enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D [11:4] will be rearranged to D [11:2] +2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D [9:8], D [7:0] 01: D [9:2], 6'bx+D [1:0] 10: D [7:0], D [9:8] +6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH Input Data Width 000: 8-bit data bus 001: 10-bit data bus 010: 12-bit data bus 011: 8+2bit data bus 100: 2x8/16bit data bus 101:14-bit data bus 110:20-bit data bus, only for packet generator 111:24 bit data bus, only for packet generator
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and

Offset: 0x0004			Register Name: CSIC_PRS_NCSIC_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
			YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	/	/	/
4:0	R/W	0x0	CSI_IF YUV (separate syncs): 00000: YUYV422/YUV420 or RAW (All data in one data bus) 00001: 2x8 bit YUYV422 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16bit BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16bit BT656(BT1120 like) 2 channels (All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16bit BT656(BT1120 like) 4 channels (All data interleaved in one data bus) Others: Reserved

7.1.11.3 0x0008 CSIC Parser MCSIC Interface Configuration Register (Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/
7:6	R/W	0X2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5:0	/	/	/

7.1.11.4 0x000C CSIC Parser Capture Register (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:26	R/W	0x0	CH3_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH3_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_1_REG bit [31:16]. Show an example as following. When CH3_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_1_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CAP_FRM_MSK_1_REG bit[22:16] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
25	R/W	0x0	CH3_VCAP_ON

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
			Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/WAC	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.
23:22	/	/	/
21:18	R/W	0x0	CH2_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH2_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_1_REG bit [15:0]. Show an example as following. When CH2_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_1_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_PRS_CAP_FRM_MSK_1_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
			image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	R/WAC	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.
15:14	/	/	/
13:10	R/W	0x0	CH1_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH1_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_0_REG bit [31:16]. Show an example as following. When CH1_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_0_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CAP_FRM_MSK_0_REG bit[22:16] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
			next frame.
8	R/WAC	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.
7:6	/	/	/
5:2	R/W	0x0	CH0_FPS_DS_PRD Fps down sample period 0: period is 1 frames 1: period is 2 frames 2: period is 3 frames 3: period is 4 frames 4: period is 5 frames …… 15: period is 16 frames Note: CH0_FPS_DS_PRD should be used together with CSIC_PRS_CAP_FRM_MSK_0_REG bit [15:0]. Show an example as following. When CH0_FPS_DS_PRD is configured as 4'd6, CSIC_PRS_CAP_FRM_MSK_0_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_PRS_CAP_FRM_MSK_0_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is wrote to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/WAC	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0.

Offset: 0x000C			Register Name: CSIC_PRS_CAP_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self-cleared.

7.1.11.5 0x0010 CSIC Parser Signal Status Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_PRS_SIGNAL_STA_REG
Bit	Read/Write	Default/Hex	Description
31	R	0x0	FIFO_FULL Indicates the NCSI IN Async FIFO FULL 0: Not Full 1:Full
30:28	R	0x0	PCLK_CNT Indicates the NCSI Pclk is toggle or not
27	R	0x0	VSYNC_STA Indicates the NCSI Vsync Signal status 0: Low 1:High
26	R	0x0	HSYNC_STA Indicates the NCSI Hsync Signal status 0: Low 1:High
25	R	0x0	FIELD_STA Indicates the NCSI Field Signal status 0: Low 1:High
24	R	0x0	DATA_VALID_STA Indicates the NCSI Data Valid Signal status(n=0-15), MSB for D15, LSB for D0 0: Low 1: High
23:0	R	0x0	DATA_STA Indicates the NCSI Data Signal status(n=0-15), MSB for D15, LSB for D0 0: Low 1: High

7.1.11.6 0x0014 CSIC Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: CSIC_PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

7.1.11.7 0x0018 CSIC Parser Capture Frame Mask 0 Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: CSIC_PRS_CAP_FRM_MSK_0_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CH1_FRAME_DATA_MASK Only [CH1_FPS_DS_PRD+16:16] are valid
15:0	R/W	0x0	CH0_FRAME_DATA_MASK Only [CH0_FPS_DS_PRD:0] are valid

7.1.11.8 0x001C CSIC Parser Capture Frame Mask 1 Register (Default Value:0x0000_0000)

Offset: 0x001C			Register Name: CSIC_PRS_CAP_FRM_MSK_1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	CH3_FRAME_DATA_MASK Only [CH3_FPS_DS_PRD+16:16] are valid
15:0	R/W	0x0	CH2_FRAME_DATA_MASK Only [CH2_FPS_DS_PRD:0] are valid

7.1.11.9 0x0020 CSIC Parser Channel_0 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PRS_CH0_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH0 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH0_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH0_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH0_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.10 0x0024 CSIC Parser Channel_0 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0024			Register Name: CSIC_PRS_CH0_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

7.1.11.11 0x0028 CSIC Parser Channel_0 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0028			Register Name: CSIC_PRS_CH0_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.12 0x002C CSIC Parser Channel_0 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x002C			Register Name: CSIC_PRS_CH0_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.13 0x0030 CSIC Parser Channel_0 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_PRS_CH0_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 0 0: Progress 1: Interlace

7.1.11.14 0x0034 CSIC Parser Channel_0 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_PRS_CH0_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.15 0x0038 CSIC Parser Channel_0 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: CSIC_PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.16 0x003C CSIC Parser Channel_0 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: CSIC_PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.17 0x0040 CSIC Parser Channel_0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	IN_VB_CHG_INT_EN

Offset: 0x0040			Register Name: CSIC_PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	IN_Y_CHG_INT_EN
4	R/W	0x0	IN_HB_CHG_INT_EN
3	R/W	0x0	IN_X_CHG_INT_EN
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.18 0x0044 CSIC Parser Channel_0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W1C	0x0	IN_VB_CHG_PD
5	R/W1C	0x0	IN_Y_CHG_PD
4	R/W1C	0x0	IN_HB_CHG_PD
3	R/W1C	0x0	IN_X_CHG_PD
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

7.1.11.19 0x0048 CSIC Parser Channel_0 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_PRS_CH0_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH0_HBLK_TIME

Offset: 0x0048			Register Name: CSIC_PRS_CH0_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
			Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

7.1.11.20 0x004C CSIC Parser Channel_0 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x004C			Register Name: CSIC_PRS_CH0_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN This bit needs to be set after configurating FRM_PRE_MSK_NUM bit. 0: Disable frame pre mask 1: Enable frame pre mask

7.1.11.21 0x0120 CSIC Parser Channel_1 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0120			Register Name: CSIC_PRS_CH1_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH1 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH1_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6,

Offset: 0x0120			Register Name: CSIC_PRS_CH1_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
			CSIC_PRS_CH1_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH1_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.22 0x0124 CSIC Parser Channel_1 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0124			Register Name: CSIC_PRS_CH1_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid. Pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

7.1.11.23 0x0128 CSIC Parser Channel_1 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0128			Register Name: CSIC_PRS_CH1_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.

Offset: 0x0128			Register Name: CSIC_PRS_CH1_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.24 0x012C CSIC Parser Channel_1 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x012C			Register Name: CSIC_PRS_CH1_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.25 0x0130 CSIC Parser Channel_1 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0130			Register Name: CSIC_PRS_CH1_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 1 0: Progress 1:Interlace

7.1.11.26 0x0134 CSIC Parser Channel_1 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0134			Register Name: CSIC_PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/

Offset: 0x0134			Register Name: CSIC_PRS_CH1_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.27 0x0138 CSIC Parser Channel_1 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0138			Register Name: CSIC_PRS_CH1_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.28 0x013C CSIC Parser Channel_1 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x013C			Register Name: CSIC_PRS_CH1_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.29 0x0140 CSIC Parser Channel_1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable

Offset: 0x0140			Register Name: CSIC_PRS_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.30 0x0144 CSIC Parser Channel_1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0144			Register Name: CSIC_PRS_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

7.1.11.31 0x0148 CSIC Parser Channel_1 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0148			Register Name: CSIC_PRS_CH1_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle.
15:0	R	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle.

7.1.11.32 0x014C CSIC Parser Channel_1 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x014C			Register Name: CSIC_PRS_CH1_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1

Offset: 0x014C			Register Name: CSIC_PRS_CH1_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
			00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN This bit needs to be set after configuring FRM_PRE_MSK_NUM bit. 0: Disable frame pre mask 1: Enable frame pre mask

7.1.11.33 0x0220 CSIC Parser Channel_2 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: CSIC_PRS_CH2_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1 0001: 2 0010: 3 ... 1111: 16 CH2 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH2_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH2_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH2_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.34 0x0224 CSIC Parser Channel_2 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0224			Register Name: CSIC_PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid

Offset: 0x0224			Register Name: CSIC_PRS_CH2_INFMT_REG
Bit	Read/Write	Default/Hex	Description
			pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

7.1.11.35 0x0228 CSIC Parser Channel_2 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0228			Register Name: CSIC_PRS_CH2_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.36 0x022C CSIC Parser Channel_2 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.

Offset: 0x022C			Register Name: CSIC_PRS_CH2_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.37 0x0230 CSIC Parser Channel_2 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_PRS_CH2_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 2 0: Progress 1: Interlace

7.1.11.38 0x0234 CSIC Parser Channel_2 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_PRS_CH2_INPUT_PARA1_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.39 0x0238 CSIC Parser Channel_2 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0238			Register Name: CSIC_PRS_CH2_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.40 0x023C CSIC Parser Channel_2 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x023C			Register Name: CSIC_PRS_CH2_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.41 0x0240 CSIC Parser Channel_2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0240			Register Name: CSIC_PRS_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.42 0x0244 CSIC Parser Channel_2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3

Offset: 0x0244			Register Name: CSIC_PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
			register update, this flag set to 1. Write 1 to clear.

7.1.11.43 0x0248 CSIC Parser Channel_2 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0248			Register Name: CSIC_PRS_CH2_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle.
15:0	R	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle.

7.1.11.44 0x024C CSIC Parser Channel_2 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x024C			Register Name: CSIC_PRS_CH2_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN Should be set after configuring FRM_PRE_MSK_NUM 0: disable frame pre mask 1: enable frame pre mask

7.1.11.45 0x0320 CSIC Parser Channel_3 Input Dmask Setting Register (Default Value:0x0000_0000)

Offset: 0x0320			Register Name: CSIC_PRS_CH3_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	IN_DMSK_PERIOD Input Dmask Period 0000: 1

Offset: 0x0320			Register Name: CSIC_PRS_CH3_IN_DMSK_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
			0001: 2 0010: 3 ... 1111: 16 CH3 IN_DMSK_PERIOD should be used together with CSIC_PRS_CH3_INFMT_REG bit [31:16]. For example, when IN_DMSK_PERIOD is configured as 4'd6, CSIC_PRS_CH3_INFMT_REG bit [22:16] will take effect and bit [31:23] will be ignored. If CSIC_PRS_CH3_INFMT_REG bit [22:16] is configured as 7'b1011011, dvld high cycle 0, 1, 3, 4, 6, 7, 8, 10, 11, 13...will be dropped. Depending on AIDB btype bit[8], one dvld high cycle may transfer one pixel or two pixels.

7.1.11.46 0x0324 CSIC Parser Channel_3 Input Format Register (Default Value:0x0000_0003)

Offset: 0x0324			Register Name: CSIC_PRS_CH3_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PIXEL_DATA_MASK Only [IN_DMSK_PERIOD+16:16] are valid pixel data masks for every (IN_DMSK_PERIOD+1) dvld high cycles of one line
15:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

7.1.11.47 0x0328 CSIC Parser Channel_3 Output Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0328			Register Name: CSIC_PRS_CH3_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HOR_MASK_MODE 0: The Area defined by HOR_START and HOR_LEN is

Offset: 0x0328			Register Name: CSIC_PRS_CH3_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
			not Masked 1: The Area defined by HOR_START and HOR_LEN is Masked
30	/	/	/
29:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.11.48 0x032C CSIC Parser Channel_3 Output Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x032C			Register Name: CSIC_PRS_CH3_OUTPUT_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_MASK_MODE 0: The Area defined by VER_START and VER_LEN is not Masked 1: The Area defined by VER_START and VER_LEN is Masked
30	/	/	/
29:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.11.49 0x0330 CSIC Parser Channel_3 Input Parameter0 Register (Default Value:0x0000_0000)

Offset: 0x0330			Register Name: CSIC_PRS_CH3_INPUT_PARA0_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE Actual Input Source Type of Channel 3 0: Progress 1:Interlace

7.1.11.50 0x0334 CSIC Parser Channel_3 Input Parameter1 Register (Default Value:0x0000_0000)

Offset: 0x0334	Register Name: CSIC_PRS_CH3_INPUT_PARA1_REG

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VT Input Frame Vertical Total INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT Input Frame Horizontal Total INPUT_HT = INPUT_HB+INPUT_X

7.1.11.51 0x0338 CSIC Parser Channel_3 Input Parameter2 Register (Default Value:0x0000_0000)

Offset: 0x0338			Register Name: CSIC_PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB Input Frame Vertical Blanking
15:14	/	/	/
13:0	R	0x0	INPUT_HB Input Frame Horizontal Blanking

7.1.11.52 0x033C CSIC Parser Channel_3 Input Parameter3 Register (Default Value:0x0000_0000)

Offset: 0x033C			Register Name: CSIC_PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y Input Frame Vertical Size
15:14	/	/	/
13:0	R	0x0	INPUT_X Input Frame Horizontal Size

7.1.11.53 0x0340 CSIC Parser Channel_3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.

Offset: 0x0340			Register Name: CSIC_PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	INPUT_PARA1_INT_EN Input Parameter1 update interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	INPUT_PARA0_INT_EN Input Parameter0 update interrupt Enable 0: Disable 1: Enable

7.1.11.54 0x0344 CSIC Parser Channel_3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0344			Register Name: CSIC_PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

7.1.11.55 0x0348 CSIC Parser Channel_3 Line Time Register (Default Value:0x0000_0000)

Offset: 0x0348			Register Name: CSIC_PRS_CH3_LINE_TIME_REG
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	R	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

7.1.11.56 0x034C CSIC Parser Channel_3 Frame Pre Mask Setting Register (Default Value:0x0000_0000)

Offset: 0x034C			Register Name: CSIC_PRS_CH3_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x034C			Register Name: CSIC_PRS_CH3_FRM_PRE_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	FRM_PRE_MSK_NUM 00000000: 0 00000001: 1 00000010: 2 ... 11111111: 255
3:1	/	/	/
0	R/W	0x0	FRM_PRE_MSK_EN This bit needs to be set after the FRM_PRE_MSK_NUM bit is configured. 0: Disable frame pre mask 1: Enable frame pre mask

7.1.11.57 0x0500 CSIC Parser NCSIC RX Signal0 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	FILED_DLY 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	VSYNC_DLY 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	HSYNC_DLY 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	PCLK_DLY 32 Step for adjust, 1 step = 0.2ns

7.1.11.58 0x050C CSIC Parser NCSIC RX Signal3 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns

Offset: 0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.59 0x0510 CSIC Parser NCSIC RX Signal4 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.60 0x0514 CSIC Parser NCSIC RX Signal5 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns

Offset: 0x0514			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.61 0x0518 CSIC Parser NCSIC RX Signal6 Delay Adjust Register (Default Value:0x0000_0000)

Offset: 0x0518			Register Name: CSIC_PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

7.1.11.62 0X0520 CSIC Parser SYNC EN Register (Default Value:0x0000_0000)

Offset :0X0520			Register Name: CSIC_PRS_SYNC_EN_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
19:16	R/W	0x0	VSYNC_MODE Input vsync signal Source select 0: Vsync signals all from 1 parser 1: Vsync signals from 2 parser 2: Vsync signals from 4 parser others: Reserved
15:12	/	/	/
11:8	R/W	0x0	VSYNC_SEL Generate sync signal Benchmark select

Offset :0X0520			Register Name: CSIC_PRS_SYNC_EN_REG
Bit	Read/Write	Default/Hex	Description
			Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	VSYNC_USED Parser input vsync signal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	FSYNC_OUT_SEL Parser sent sync signal via by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	FSYNC_MODE Parser sync signal source select 0: From outside 1: Generate by self
0	R/W	0x0	FSYNC_FUN_EN Enable Parser sent sync signal 0: Disable 1: Enable

7.1.11.63 0X0524 CSIC Parser SYNC CFG Register (Default Value:0x0000_0000)

Offset :0X0524			Register Name: CSIC_PRS_SYNC_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	FSYNC_PUL_WID Sync signal pulse width $N*T_{24M}$ $N*T_{24M} \geqslant 4*Tpclk$
15:0	R/W	0x0	FYSNC_DISTANCE The interval of two sync signal

7.1.11.64 0X0528 CSIC Parser VS WAIT N Register (Default Value:0x0000_0000)

Offset :0X0528	Register Name: CSIC_PRS_VS_WAIT_N_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come, the max wait time.

7.1.11.65 0X052C CSIC Parser VS WAIT M Register (Default Value:0x0000_0000)

Offset :0X052C			Register Name: CSIC_PRS_VS_WAIT_M_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode, sync comes at the different time, these bits indicate the max wait time.

7.1.11.66 0X0540 CSIC Parser XSYNC ENABLE Register (Default Value:0x0000_0000)

Offset: 0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:8	R/W	0x0	XVS_TO_XHS_T The period of XHS delay to XVS, ${XVS_TO_XHS_T}+1 master clock cycles, no more than XHS_LEN
7:5	/	/	/
4	R/W	0x0	XVS_XHS_OUT_SEL When sensor works in slave mode, this bit select XVS and XHS to output. 0: XHS0, XVS0 1: XHS1,XVS1
3	R/W	0x0	XVS_POL When sensor works in slave mode, this bit set polarity of XVS. 0: Negative 1: Positive
2	R/W	0x0	XHS_POL When sensor works in slave mode, this bit set polarity of XHS. 0: Negative 1: Positive
1	R/W	0x0	XVS_OUT_EN When sensor works in slave mode, this bit enables output XVS to sensor 0: Disable 1: Enable
0	R/W	0x0	XHS_OUT_EN

Offset: 0X0540			Register Name: CSIC_PRS_XSYNC_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
			When sensor works in slave mode, this bit enables output XHS to sensor 0: Disable 1: Enable

7.1.11.67 0X0544 CSIC Parser XVS Period Register (Default Value:0x0000_0000)

Offset: 0X0544			Register Name: CSIC_PRS_XVS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_T The period of XVS signal, ${XVS_T}+2 master clock cycles

7.1.11.68 0X0548 CSIC Parser XHS Period Register (Default Value:0x0000_0000)

Offset: 0X0548			Register Name: CSIC_PRS_XHS_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_T The period of XHS signal, ${XHS_T}+2 master clock cycles

7.1.11.69 0X054C CSIC Parser XVS LENGTH Register (Default Value:0x0000_0000)

Offset: 0X054C			Register Name: CSIC_PRS_XVS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XVS_LEN The valid length of XVS signal, ${XVS_LEN}+1 master clock cycles

7.1.11.70 0X0550 CSIC Parser XHS LENGTH Register (Default Value:0x0000_0000)

Offset: 0X0550			Register Name: CSIC_PRS_XHS_LENGTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	XHS_LEN The valid length of XHS signal, ${XHS_LEN}+1 master clock cycles

7.1.11.71 0X0554 CSIC Parser SYNC DELAY Register (Default Value:0x0000_0000)

Offset: 0X0554			Register Name: CSIC_PRS_SYNC_DLY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SYNC_DLY The XHS/XVS will sent after, ${SYNC_DLY}+1 master clock cycles, no more than XVS_LEN

7.1.12 CISC_DMA Register Description

7.1.12.1 0x0000 CSIC DMA TOP Register (Default Value:0x7000_0000)

Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	VER_EN CSIC DMA Version Register Read Enable: 0: Disable 1: Enable
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: hardware 1: software
29	R/W	0x1	BUF_LENGTH_CFG_MODE buffer length set by software or calculated by hardware 0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:17	/	/	/
16	R/W	0x0	FRM_END_SEL 0: Select mcsi_bk_frm_end_in 1: Select dma_frm_end
15	/	/	/
14:13	R/W	0x0	VE_ONLINE_CH_SEL Select BK Channel for VE Online handshake
12	R/W	0x0	VE_ONLINE_HANDSHAKE_EN Set this bit to Enable frame and line counter for VE online handshake

Offset: 0x0000			Register Name: CSIC_DMA_TOP_REG
Bit	Read/Write	Default/Hex	Description
11:10	/	/	/
9:8	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 0: 256 bytes (if hflip is enable, always select 256 bytes) 1: 512 bytes 2: 1k bytes 3: 2k bytes(not Support For DMA1\2\3)
7	/	/	/
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FS_FRM_CNT_EN When BK_TOP_EN enable, this bit set 1 indicate the Frame counter start to add. 0: Disable 1: Enable
4:3	/	/	/
2	R/W	0x0	FRM_RATE_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	FRM_RATE_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN Module Enable 0: Disable 1: Enable

7.1.12.2 0x0004 CSIC DMA Multi-Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R	0x0	CUR_OUT_CH When Multi-Channel enable, this field indicates the Current Output Channel ID
19:18	/	/	/

Offset: 0x0004			Register Name: CSIC_DMA_MUL_CH_CFG_REG
Bit	Read/Write	Default/Hex	Description
17:16	R	0x0	CUR_IN_CH When Multi-Channel enable, this field indicates the Current Input Channel ID
15:1	/	/	/
0	R/W	0x0	MUL_CH_EN DMA off-line multi-channel enable 0: disable 1: enable

7.1.12.3 0x0010 CSIC DMA Frame Rate Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	FRM_RATE_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

7.1.12.4 0x0014 CSIC DMA Accumulated and Internal Clock Counter Register (Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time

Offset: 0x0014			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	Read/Write	Default/Hex	Description
			for updating the double buffer address registers.

7.1.12.5 0x0020 CSIC DMA Fsync Frame Counter Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_FS_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	FS_FRM_CNT_CLR When the bit set to 1,Frame cnt clear to 0
30:16	R/W	0x0	FS_FRM_CNT_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15	/	/	/
14:0	R	0x0	FS_FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the reg full ,it cleared to 0 . When parser sent a sync signal, it clear to 0

7.1.12.6 0x0040 CSIC DMA Video Input Timeout Threshold0 Register (Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH0 Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , Time Unit is a 12M clock period.

7.1.12.7 0x0044 CSIC DMA Video Input Timeout Threshold1 Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	VI_TO_TH1 Video Input Timeout Threshold1

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	Read/Write	Default/Hex	Description
			Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

7.1.12.8 0x0048 CSIC DMA Video Input Timeout Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	VI_TCNT_VAL Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter

7.1.12.9 0x0050 CSIC DMA VE Frame Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_VE_FRM_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R	0x0	FRM_DONE_CNT Indicates How Many Frame which Stored in DDR
15:8	/	/	/
7:0	R	0x0	FRM_ST_CNT Indicates the Frame Number which is Storing

7.1.12.10 0x0054 CSIC DMA VE Line Counter Value Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_VE_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_DONE_CNT Indicates How Many Line which Stored in DDR
15:14	/	/	/
13:0	R	0x0	LINE_ST_CNT Indicates the Line Number which is Storing

7.1.12.11 0x0058 CSIC DMA VE Current Frame Address Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_VE_CUR_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CUR_FRM_ADDR Indicates the FIFO0 Address Which Current Frame is Storing

7.1.12.12 0x005C CSIC DMA VE Last Frame Address Register (Default Value:0x0000_0000)

Offset: 0x005C			Register Name: CSIC_DMA_VE_LAST_FRM_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LAST_FRM_ADDR Indicates the FIFO0 Address Which Last Frame is Stored

7.1.12.13 0x0080 CSIC DMA FIFO Statistic Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone. Unit is byte.

7.1.12.14 0x0084 CSIC DMA FIFO Threshold Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change. Unit is byte.

7.1.12.15 0x0100 CSIC DMA TOP Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_DMA_TOP_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

Offset: 0x0100			Register Name: CSIC_DMA_TOP_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time.
1	R/W	0x0	CLR_FS_FRM_CNT_INT_EN Set a INT When Clear FS Frame cnt.
0	R/W	0x0	FS_PUL_INT_EN Set an INT when a Fsync signal received

7.1.12.16 0x0104 CSIC DMA TOP Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_DMA_TOP_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time
1	R/W1C	0x0	CLR_FRAME_CNT_INT_PD Set a INT When Clear FS Frame cnt.
0	R/W1C	0x0	FS_PUL_INT_PD Set an INT when a Fsync signal received

7.1.12.17 0x01F0 CSIC DMA Version Register (Default Value:0x0014_0100)

Offset: 0x01F0			Register Name: CSIC_DMA_VER_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:12	R	0x140	VER_BIG_VER Big Version of hardware circuit. Only can be read when version register read enable is on.
11:0	R	0x100	VER_SMALL_VER Small Version of hardware circuit. Only can be read when version register read enable is on.

7.1.12.18 0x01F4 CSIC DMA Feature List Register (Default Value:0x0000_0040)

Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R	0x4	DMA0_CHNUM

Offset: 0x01F4			Register Name: CSIC_DMA_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
			Channel numbers (note: for DMA0-DMA3, DMA0/1/2/3_CHNUM=4; for DMA4-DMA5, DMA4/5_CHNUM=1)
3:2	/	/	/
1	R	0x0	DMA0_EMBEDDED_LBC LBC Feature Existence 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC FBC Feature Existence 0: No Embedded FBC 1: Embedded FBC

7.1.12.19 0x0200 CSIC DMA Channel0 Enable Register (Default Value:0x0000_0000)

Offset: 0x0200			Register Name: CSIC_DMA_CH0_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:1	/	/	/
0	R/W	0x0	CAP_EN Video in Capture Enable 0: Disable 1: Enable

7.1.12.20 0x0204 CSIC DMA Channel0 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
			sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0.

Offset: 0x0204			Register Name: CSIC_DMA_CH0_CFG_REG
Bit	Read/Write	Default/Hex	Description
			01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames …… 15: 16 frames CH0 FPS_DS_PRD should be used together with CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[15:0]. For example, when CH0 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH0_FRM_MSK_CFG_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_DMA_CH0_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.21 0x0208 CSIC DMA Channel0 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0208			Register Name: CSIC_DMA_CH0_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

7.1.12.22 0x020C CSIC DMA Channel0 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x020C			Register Name: CSIC_DMA_CH0_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.23 0x0210 CSIC DMA Channel0 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0210			Register Name: CSIC_DMA_CH0_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.24 0x0214 CSIC DMA Channel0 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0214			Register Name: CSIC_DMA_CH0_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.12.25 0x0218 CSIC DMA Channel0 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0218			Register Name: CSIC_DMA_CH0_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop

Offset: 0x0218			Register Name: CSIC_DMA_CH0_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
			When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.26 0x0220 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0220			Register Name: CSIC_DMA_CH0_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.27 0x0224 CSIC DMA Channel0 FIFO 0 Output Buffer-A Address Result Register (Default 0x0224 Value:0x0000_0000)

Offset: 0x0224			Register Name: CSIC_DMA_CH0_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address FIFO. Only used for debug.

7.1.12.28 0x0228 CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0228			Register Name: CSIC_DMA_CH0_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

7.1.12.29 0x022C CSIC DMA Channel0 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x022C			Register Name: CSIC_DMA_CH0_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address FIFO. Only used for debug.

7.1.12.30 0x0230 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0230			Register Name: CSIC_DMA_CH0_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.31 0x0234 CSIC DMA Channel0 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0234			Register Name: CSIC_DMA_CH0_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address FIFO. Only used for debug.

7.1.12.32 0x0238 CSIC DMA Channel0 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0238			Register Name: CSIC_DMA_CH0_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.

Offset: 0x0238			Register Name: CSIC_DMA_CH0_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.33 0x023C CSIC DMA Channel0 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x023C			Register Name: CSIC_DMA_CH0_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.34 0x024C CSIC DMA Channel0 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x024C			Register Name: CSIC_DMA_CH0_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.35 0x0250 CSIC DMA Channel0 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN Vsync Flag

Offset: 0x0250			Register Name: CSIC_DMA_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this IRQ come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4:3	/	/	/
2	R/W	0x0	FIFO_OF_INT_EN FIFO Overflow The bit is set when the FIFO occurs an overflow.
1	R/W	0x0	FD_INT_EN Frame Done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.36 0x0254 CSIC DMA Channel0 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag

Offset: 0x0254			Register Name: CSIC_DMA_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4:3	/	/	/
2	R/W1C	0x0	FIFO_OF_PD FIFO θ overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

7.1.12.37 0x0258 CSIC DMA Channel0 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0258			Register Name: CSIC_DMA_CH0_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user, when internal line counter reach the set value, the LC_PD will set.

7.1.12.38 0x025C CSIC DMA Channel0 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first

Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is

Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use

Offset: 0x025C			Register Name: CSIC_DMA_CH0_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			this field.
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x028c REG and 0x0294 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.39 0x0268 CSIC DMA Channel0 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0268			Register Name: CSIC_DMA_CH0_LINE_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current hsync.
15:0	/	/	/

7.1.12.40 0x0270 CSIC DMA Channel0 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for

Offset: 0x0270			Register Name: CSIC_DMA_CH0_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
			each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.41 0x0298 CSIC DMA Channel0 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK

Offset: 0x0298			Register Name: CSIC_DMA_CH0_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
			Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.42 0x029C CSIC DMA Channel0 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x029C			Register Name: CSIC_DMA_CH0_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels' miss error

Offset: 0x029C			Register Name: CSIC_DMA_CH0_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
			happens. 0: Disable ADD 1: Enable ADD

7.1.12.43 0x02A0 CSIC DMA Channel0 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x02A0			Register Name: CSIC_DMA_CH0_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

7.1.12.44 0x0400 CSIC DMA Channel1 Enable Register (Default Value:0x0000_0000)

Offset: 0x0400			Register Name: CSIC_DMA_CH1_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:1	/	/	/
0	R/W	0x0	CAP_EN Video in Capture Enable 0: Disable 1: Enable

7.1.12.45 0x0404 CSIC DMA Channel1 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined (UV sequence) 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111: frame planar YCbCr 422 UV combined (UV sequence) 1000: filed planar YCbCr 422 UV combined (VU sequence) 1001: field planar YCbCr 420 UV combined (VU sequence)

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1010: frame planar YCbCr 420 UV combined (VU sequence) 1011: frame planar YCbCr 422 UV combined (VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined (UV sequence) 0110: frame planar YCbCr 420 UV combined (UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined (VU sequence) 1010: frame planar YCbCr 420 UV combined (VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0: Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0: Disable 1:Enable

Offset: 0x0404			Register Name: CSIC_DMA_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames ..... 15: 16 frames Note: CH1 FPS_DS_PRD should be used together with CSIC_DMA_CH1_FRM_MSK_CFG_REG bit [15:0]. For example, when CH1 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH1_FRM_MSK_CFG_REG bit [6:0] will take effect and bit [15:7] will be ignored. If CSIC_DMA_CH1_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.46 0x0408 CSIC DMA Channel1 Frami Lost Counter Register (Default Value:0x0001_0000)

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/

Offset: 0x0408			Register Name: CSIC_DMA_CH1_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

7.1.12.47 0x040C CSIC DMA Channel1 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x040C			Register Name: CSIC_DMA_CH1_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.48 0x0410 CSIC DMA Channel1 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0410			Register Name: CSIC_DMA_CH1_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.49 0x0414 CSIC DMA Channel1 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0414			Register Name: CSIC_DMA_CH1_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA

Offset: 0x0414			Register Name: CSIC_DMA_CH1_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
			mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.12.50 0x0418 CSIC DMA Channel1 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0418			Register Name: CSIC_DMA_CH1_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.51 0x0420 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0420			Register Name: CSIC_DMA_CH1_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.52 0x0424 CSIC DMA Channel1 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0424			Register Name: CSIC_DMA_CH1_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or

Offset: 0x0424			Register Name: CSIC_DMA_CH1_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
			FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.53 0x0428 CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0428			Register Name: CSIC_DMA_CH1_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

7.1.12.54 0x042C CSIC DMA Channel1 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x042C			Register Name: CSIC_DMA_CH1_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.55 0x0430 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0430			Register Name: CSIC_DMA_CH1_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.56 0x0434 CSIC DMA Channel1 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0434	Register Name: CSIC_DMA_CH1_F2_BUFA_RESULT_REG

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.57 0x0438 CSIC DMA Channel1 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0438			Register Name: CSIC_DMA_CH1_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.58 0x043C CSIC DMA Channel1 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x043C			Register Name: CSIC_DMA_CH1_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.59 0x044C CSIC DMA Channel1 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field

Offset: 0x044C			Register Name: CSIC_DMA_CH1_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
			0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.60 0x0450 CSIC DMA Channel1 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN

Offset: 0x0450			Register Name: CSIC_DMA_CH1_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.61 0x0454 CSIC DMA Channel1 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles,

Offset: 0x0454			Register Name: CSIC_DMA_CH1_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
			only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

7.1.12.62 0x0458 CSIC DMA Channel1 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0458	Register Name: CSIC_DMA_CH1_LINE_CNT_REG

Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

7.1.12.63 0x045C CSIC DMA Channel1 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as

Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame

Offset: 0x045C			Register Name: CSIC_DMA_CH1_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x048c REG and 0x0494 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.64 0x0468 CSIC DMA Channel1 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0468			Register Name: CSIC_DMA_CH1_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

7.1.12.65 0x0470 CSIC DMA Channel1 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0470	Register Name: CSIC_DMA_CH1_PCLK_STAT_REG

Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.66 0x0498 CSIC DMA Channel1 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0498			Register Name: CSIC_DMA_CH1_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame.

Offset: 0x0498			Register Name: CSIC_DMA_CH1_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.67 0x049C CSIC DMA Channel1 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x049C			Register Name: CSIC_DMA_CH1_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Offset: 0x049C			Register Name: CSIC_DMA_CH1_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.68 0x04A0 CSIC DMA Channel1 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x04A0			Register Name: CSIC_DMA_CH1_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

7.1.12.69 0x0600 CSIC DMA Channel2 Enable Register (Default Value:0x0000_0000)

Offset: 0x0600			Register Name: CSIC_DMA_CH2_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:1	/	/	/
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

7.1.12.70 0x0604 CSIC DMA Channel2 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
			0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence)

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip.

Offset: 0x0604			Register Name: CSIC_DMA_CH2_CFG_REG
Bit	Read/Write	Default/Hex	Description
			0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS_PRD Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames ..... 15: 16 frames Note: CH2 FPS_DS_PRD should be used together with CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH2 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH2_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.71 0x0608 CSIC DMA Channel2 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/

Offset: 0x0608			Register Name: CSIC_DMA_CH2_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

7.1.12.72 0x060C CSIC DMA Channel2 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x060C			Register Name: CSIC_DMA_CH2_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.73 0x0610 CSIC DMA Channel2 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0610			Register Name: CSIC_DMA_CH2_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.74 0x0614 CSIC DMA Channel2 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START

Offset: 0x0614			Register Name: CSIC_DMA_CH2_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
			Vertical line start. data is valid from this line.

7.1.12.75 0x0618 CSIC DMA Channel2 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0618			Register Name: CSIC_DMA_CH2_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.76 0x0620 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0620			Register Name: CSIC_DMA_CH2_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.77 0x0624 CSIC DMA Channel2 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0624			Register Name: CSIC_DMA_CH2_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.78 0x0628 CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0628			Register Name: CSIC_DMA_CH2_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address.

7.1.12.79 0x062C CSIC DMA Channel2 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x062C			Register Name: CSIC_DMA_CH2_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.80 0x0630 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0630			Register Name: CSIC_DMA_CH2_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.81 0x0634 CSIC DMA Channel2 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0634			Register Name: CSIC_DMA_CH2_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.82 0x0638 CSIC DMA Channel2 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0638			Register Name: CSIC_DMA_CH2_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.83 0x063C CSIC DMA Channel2 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x063C			Register Name: CSIC_DMA_CH2_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.84 0x064C CSIC DMA Channel2 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x064C			Register Name: CSIC_DMA_CH2_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.85 0x0650 CSIC DMA Channel2 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/

Offset: 0x0650			Register Name: CSIC_DMA_CH2_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.86 0x0654 CSIC DMA Channel2 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/

Offset: 0x0654			Register Name: CSIC_DMA_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

7.1.12.87 0x0658 CSIC DMA Channel2 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0658			Register Name: CSIC_DMA_CH2_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

7.1.12.88 0x065C CSIC DMA Channel2 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int

Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one. Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the

Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one.

Offset: 0x065C			Register Name: CSIC_DMA_CH2_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x068c REG and 0x0694 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.89 0x0668 CSIC DMA Channel2 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0668			Register Name: CSIC_DMA_CH2_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

7.1.12.90 0x0670 CSIC DMA Channel2 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0670			Register Name: CSIC_DMA_CH2_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.91 0x0698 CSIC DMA Channel2 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.

Offset: 0x0698			Register Name: CSIC_DMA_CH2_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame. 0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.92 0x069C CSIC DMA Channel2 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x069C			Register Name: CSIC_DMA_CH2_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.93 0x06A0 CSIC DMA Channel2 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x06A0			Register Name: CSIC_DMA_CH2_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE

Offset: 0x06A0			Register Name: CSIC_DMA_CH2_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
			Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

7.1.12.94 0x0800 CSIC DMA Channel3 Enable Register (Default Value:0x0000_0000)

Offset: 0x0800			Register Name: CSIC_DMA_CH3_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	FRM_DROP_EN Drop Frame when vsync comes but buffer address is not ready 0: Not Drop 1: Drop
7:2	/	/	/
1	R/W	0x0	LBC_EN LBC Function Enable 0: Disable 1: Enable
0	R/W	0x0	CAP_EN Video In Capture Enable 0: Disable 1: Enable

7.1.12.95 0x0804 CSIC DMA Channel3 Configuration Register (Default Value:0x0000_0000)

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00-0xff
23:22	/	/	/
21	R/W	0x0	YUV10to8_EN YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV10_STO_FMT YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: raw-8 0001: raw-10 0010: raw-12 0011: raw-14 0100: raw-16 0101: raw-20 0110: raw-24 0111: reserved 1000: rgb565 1001: rgb888 1010: prgb888 others: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400 1110: reserved

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
			1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111-1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011-1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS_PRD

Offset: 0x0804			Register Name: CSIC_DMA_CH3_CFG_REG
Bit	Read/Write	Default/Hex	Description
			Fps down sample period 0: 1 frames 1: 2 frames 2: 3 frames 3: 4 frames 4: 5 frames ..... 15: 16 frames Note: CH3 FPS_DS_PRD should be used together with CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[15:0]. Show an example as following. When CH3 FPS_DS_PRD is configured as 4'd6, CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[6:0] will take effect and bit[15:7] will be ignored. If CSIC_DMA_CH3_FRM_MSK_CFG_REG bit[6:0] is configured as 7'b1011011, frame 0,frame 1, frame 3,frame 4, frame 6, frame 7,frame 8, frame 10,frame 11, frame 13...will be dropped.
5:2	R/W	0x0	CAP_FRONT_MASK_NUM Indicates the frame number masked after CAP_EN set.
1:0	/	/	/

7.1.12.96 0x0808 CSIC DMA Channel3 Frame Lost Counter Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: CSIC_DMA_CH3_FRM_LOST_CNT_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FRM_LOST_CNT_EN When set 1, FRM_LOST_CNT is enable; when set 0, FRM_LOST_CNT is cleared
30:8	/	/	/
7:0	R	0x0	FRM_LOST_CNT Once a new frame comes when the buffer address not ready and FRM_DROP_EN set, or when the last frame still processing, the new frame is dropped and the FRM_LOST_CNT increases when FRM_LOST_CNT_EN set.

7.1.12.97 0x080C CSIC DMA Channel3 Frame Mask Configuration Register (Default Value:0x0000_0000)

Offset: 0x080C			Register Name: CSIC_DMA_CH3_FRM_MSK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	FRAME_DATA_MASK Only [FPS_DS_PRD:0] are valid

7.1.12.98 0x0810 CSIC DMA Channel3 Horizontal Size Register (Default Value:0x0500_0000)

Offset: 0x0810			Register Name: CSIC_DMA_CH3_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

7.1.12.99 0x0814 CSIC DMA Channel3 Vertical Size Register (Default Value:0x02d0_0000)

Offset: 0x0814			Register Name: CSIC_DMA_CH3_VSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2d0	VER_LEN When BK_TOP_EN enable, DMA_EN enable, these bits indicate Valid line number of a frame in DMA mode.
15:14	/	/	/
13:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

7.1.12.100 0x0818 CSIC DMA Channel3 Vertical Crop Mode Register (Default Value:0x0000_0000)

Offset: 0x0818			Register Name: CSIC_DMA_CH3_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	FLD_FRM_VCROP_EN 0: disable field frame vcrop 1: enable field frame vcrop

Offset: 0x0818			Register Name: CSIC_DMA_CH3_VCROP_CFG_REG
Bit	Read/Write	Default/Hex	Description
			When input frame is of field type and V crop wants to be implemented, this bit should be configured as 1. (note: only even lines crop is supported for field input V crop)

7.1.12.101 0x0820 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0820			Register Name: CSIC_DMA_CH3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F0_BUFA When LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When LBC_EN enable, these bits indicate the output buffer address in LBC mode.

7.1.12.102 0x0824 CSIC DMA Channel3 FIFO 0 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0824			Register Name: CSIC_DMA_CH3_F0_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.103 0x0828 CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0828			Register Name: CSIC_DMA_CH3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F1_BUFA FIFO 1 output buffer-A address in DMA mode.

7.1.12.104 0x082C CSIC DMA Channel3 FIFO 1 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x082C			Register Name: CSIC_DMA_CH3_F1_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.105 0x0830 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Register (Default Value:0x0000_0000)

Offset: 0x0830			Register Name: CSIC_DMA_CH3_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

7.1.12.106 0x0834 CSIC DMA Channel3 FIFO 2 Output Buffer-A Address Result Register (Default Value:0x0000_0000)

Offset: 0x0834			Register Name: CSIC_DMA_CH3_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

7.1.12.107 0x0838 CSIC DMA Channel3 Buffer Length Register (Default Value:0x0280_0500)

Offset: 0x0838			Register Name: CSIC_DMA_CH3_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x280	BUF_LEN_C DMA_MODE: Buffer length of chroma C in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y in ONLY Y line. Unit is byte.

Offset: 0x0838			Register Name: CSIC_DMA_CH3_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x500	BUF_LEN DMA_MODE: Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte.

7.1.12.108 0x083C CSIC DMA Channel3 Flip Size Register (Default Value:0x02d0_0500)

Offset: 0x083C			Register Name: CSIC_DMA_CH3_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE set 0
15:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE set 0

7.1.12.109 0x084C CSIC DMA Channel3 Capture Status Register (Default Value:0x0000_0000)

Offset: 0x084C			Register Name: CSIC_DMA_CH3_CAP_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	/	/	/
0	R	0x0	CAP_STA capture in progress Indicates the CSI is capturing image data. The bit is set at the start of the first frame after enabling frame capture.

7.1.12.110 0x0850 CSIC DMA Channel3 Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	LACK_HBLANK_INT_EN Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W	0x0	LINE_REDUNDANT_INT_EN Set an INT when the amount of lines in one frame is more than expected.
21	R/W	0x0	LINE_MISS_INT_EN Set an INT when the amount of lines in one frame is less than expected.
20	R/W	0x0	PIXEL_REDUNDANT_INT_EN Set an INT when the amount of pixels in one line is more than expected.
19	R/W	0x0	PIXEL_MISS_INT_EN Set an INT when the amount of pixels in one line is less than expected.
18	R/W	0x0	BUF_ADDR_OVERFLOW_INT_EN Set an INT when buffer address is overwrite before used
17	R/W	0x0	BUF_ADDR_UNDERFLOW_INT_EN Set an INT when new frame comes but buffer address is not ready
16	R/W	0x0	LBC_HBLKMIN_INT_EN Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W	0x0	FRM_LOST_INT_EN Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD , only use in BUF Address FIFO MODE
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load

Offset: 0x0850			Register Name: CSIC_DMA_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
			the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	LI_OF_INT_EN Line information FIFO(16 lines) overflow.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is wrote to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been wrote to buffer. For video capture, the bit is set when the last frame has been wrote to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

7.1.12.111 0x0854 CSIC DMA Channel3 Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0854	Register Name: CSIC_DMA_CH3_INT_STA_REG

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W1C	0x0	LACK_HBLANK_INT_PD Set an INT when trying filling dummy for missed pixels at the end of the line but hblank is too short.
22	R/W1C	0x0	LINE_REDUNDANT_INT_PD Set an INT when the amount of lines in one frame is more than expected.
21	R/W1C	0x0	LINE_MISS_INT_PD Set an INT when the amount of lines in one frame is less than expected.
20	R/W1C	0x0	PIXEL_REDUNDANT_INT_PD Set an INT when the amount of pixels in one line is more than expected.
19	R/W1C	0x0	PIXEL_MISS_INT_PD Set an INT when the amount of pixels in one line is less than expected.
18	R/W1C	0x0	BUF_ADDR_OVERFLOW_INT_PD Set an INT when buffer address is overwrite before used
17	R/W1C	0x0	BUF_ADDR_UNDERFLOW_INT_PD Set an INT when new frame comes but buffer address is not ready
16	R/W1C	0x0	LBC_HBLKMIN_INT_PD Set an INT when hblanking less than 48 bk_clk cycles, only use in LBC Mode
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT once frame is in when last frame processing or Buffer Address FIFO is empty (only use in BUF Address FIFO MODE)
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO no more than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	LI_OF_PD

Offset: 0x0854			Register Name: CSIC_DMA_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
			Line information FIFO(16 lines) overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

7.1.12.112 0x0858 CSIC DMA Channel3 Line Counter Register (Default Value:0x0000_0000)

Offset: 0x0858			Register Name: CSIC_DMA_CH3_LINE_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

7.1.12.113 0x085C CSIC DMA Channel3 Abnormal Frame Number Register (Default Value:0x0000_0000)

Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R	0x0	LACK_HBLANK_FRM_NUM The frame number for the earliest lack hblank int which has not been cleared. After lack hblank int is cleared, the coming lack hblank int will be treated as the new earliest one.

Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			Show an example. Imaging a scene that lack hblank int happens in frame 0, frame 1 and frame2, and clear action for lack hblank int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LACK_HBLANK_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
15:12	R	0x0	LINE_REDUNDANT_FRM_NUM The frame number for the earliest line redundant int which has not been cleared. After line redundant int is cleared, the coming line redundant int will be treated as the new earliest one. Show an example. Imaging a scene that line redundant int happens in frame 0, frame 1 and frame2, and clear action for line redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
11:8	R	0x0	LINE_MISS_FRM_NUM The frame number for the earliest line miss int which has not been cleared. After line miss int is cleared, the coming line miss int will be treated as the new earliest one. Show an example. Imaging a scene that line miss int

Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			happens in frame 0, frame 1 and frame2, and clear action for line miss int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed LINE_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
7:4	R	0x0	PIXEL_REDUNDANT_FRM_NUM The frame number for the earliest pixel redundant int which has not been cleared. After pixel redundant int is cleared, the coming pixel redundant int will be treated as the new earliest one. Show an example. Imaging a scene that pixel redundant int happens in frame 0, frame 1 and frame2, and clear action for pixel redundant int is first implemented between frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_REDUNDANT_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.
3:0	R	0x0	PIXEL_MISS_FRM_NUM The frame number for the earliest pixel miss int which has not been cleared. After pixel miss int is cleared, the coming pixel miss int will be treated as the new earliest one. Show an example. Imaging a scene that pixel miss int happens in frame 0, frame 1 and frame2, and clear action for pixel miss int is first implemented between

Offset: 0x085C			Register Name: CSIC_DMA_CH3_ABN_FRM_NUM_REG
Bit	Read/Write	Default/Hex	Description
			frame 1 and frame 2. Before int clear action happens, frame 0 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 0. After int clear action happens, frame 2 will be treated as the earliest one and the content in this filed PIXEL_MISS_FRM_NUM equals to the frame number of frame 2. Note: This field is only for debug. It should be used with 0x088c REG and 0x0894 REG which are invisible to customers and invisible in this spec. Please consult to the designer if you want to use this field.

7.1.12.114 0x0868 CSIC DMA Channel3 Line Statistic Register (Default Value:0x0000_0000)

Offset: 0x0868			Register Name: CSIC_DMA_CH3_FIFO_STAT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	LINE_INDEX Indicates the line index in current vsync.
15:0	/	/	/

7.1.12.115 0x0870 CSIC DMA Channel3 PCLK Statistic Register (Default Value:0x0000_0000)

Offset: 0x0870			Register Name: CSIC_DMA_CH3_PCLK_STAT_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x0	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

7.1.12.116 0x0898 CSIC DMA Channel3 Abnormal Mask Register (Default Value:0x0000_0000)

Offset: 0x0898	Register Name: CSIC_DMA_CH3_ABN_MSK_REG

Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	FRM_DONE_INT_MSK_EN Decide whether the FD_INT of this frame will be masked or not once any abnormal condition happens during this frame. 0: Disable MSK 1: Enable MSK
4	R/W	0x0	LINE_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
3	R/W	0x0	LINE_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once line miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
2	R/W	0x0	PIXEL_REDUNDANT_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel redundant error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
1	R/W	0x0	PIXEL_MISS_MSK_EN Decide whether the remaining data in this frame will be dropped or not once pixel miss error happens in this frame. 0: Disable MSK 1: Enable MSK Note: this field takes effect only when VSYN_ABN_MSK_EN is set as 1.
0	R/W	0x0	VSYN_ABN_MSK_EN Decide whether the remaining data in this frame will be dropped or not once abnormal happens in this frame.

Offset: 0x0898			Register Name: CSIC_DMA_CH3_ABN_MSK_REG
Bit	Read/Write	Default/Hex	Description
			0: Disable MSK 1: Enable MSK Note: When VSYN_ABN_MSK_EN is set as 1 and one of the following conditions happens, the remaining data in this frame will be dropped. And the next frame will be received as normal. 1, when trying to fill dummy for pixel miss and LACK_HBLANK happens. 2, when PIXEL_REDUNDANT happens and PIXEL_REDUNDANT_MSK_EN is set as 1. 3, when PIXEL_MISS happens, LACK_HBLANK no happen and PIXEL_MISS_MSK_EN is set as 1. 4, when LINE_REDUNDANT happens and LINE_REDUNDANT_MSK_EN is set as 1. 5, when LINE_MISS happens and LINE_MISS_MSK_EN is set as 1.

7.1.12.117 0x089C CSIC DMA Channel3 Pixels Add Enable Register (Default Value:0x0000_0000)

Offset: 0x089C			Register Name: CSIC_DMA_CH3_PIXELS_ADD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PIXELS_ADD_EN Decide whether dummy pixels will be added in the end of the line or not once pixels miss error happens. 0: Disable ADD 1: Enable ADD

7.1.12.118 0x08A0 CSIC DMA Channel3 Pixels Add Value Register (Default Value:0x0000_0000)

Offset: 0x08A0			Register Name: CSIC_DMA_CH3_PIXELS_ADD_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PIXELS_ADD_VALUE Decide the value of dummy pixels when PIXELS_ADD_EN is set as 1

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8 Interfaces

8.1 CIR Receiver (CIR_RX)

8.1.1 Overview

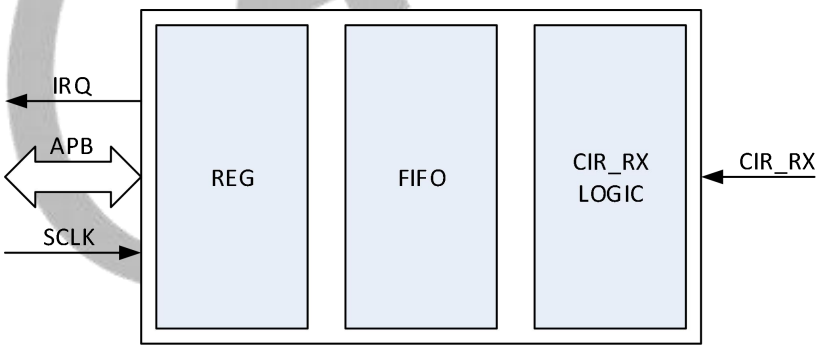
The Consumer Infrared (CIR) receiver captures pulse from the IR Receiver module and uses the Run-Length Code (RLC) to encode the pulse.

The CIR receiver has the following features:

- One CIR_RX interface in CPUX domain and one CIR_RX interface in CPUS domain
- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz
- Supports interrupt and DMA mode

8.1.2 Block Diagram

Figure 8-1 CIR Receiver Block Diagram



The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal, the rest 7 bits are used for the length of RLC. The maximum length of the RLC is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

8.1.3 Functional Description

8.1.3.1 External Signals

The following table describes the external signals of CIR Receiver.

Table 8-1 CIR Receiver External Signals

Signal Name	Description	Type
IR-RX	Consumer Infrared Receiver	I
S-IR-RX	Consumer infrared receiver	I

8.1.3.2 Clock Sources

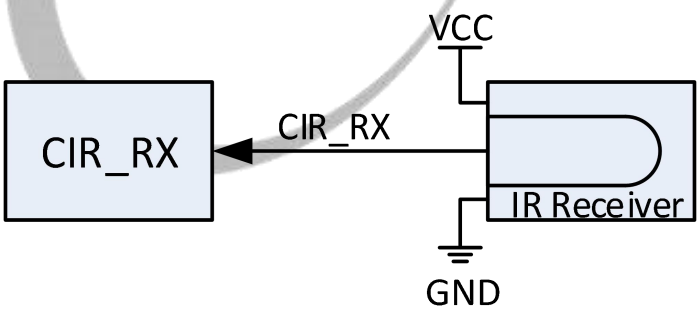
The following table describes the clock sources of CIR Receiver.

Table 8-2 CIR Receiver Clock Sources

Clock Sources	Description	Module
CIR_RX		
CLK32K	By default, CLK32K is 32.768 kHz.	CCU
HOSC	By default, HOSC is 24 MHz.	CCU
S_CIRRX		
CLK32K	By default, CLK32K is 32.768 kHz.	PRCM
CLK24M	By default, CLK24M is 24 MHz.	PRCM

8.1.3.3 Typical Application

Figure 8-2 CIR Receiver Application Diagram



8.1.3.4 NEC Protocol Format

Figure 8-3 NEC Protocol

The CIR receiver module is a timer with a capture function.

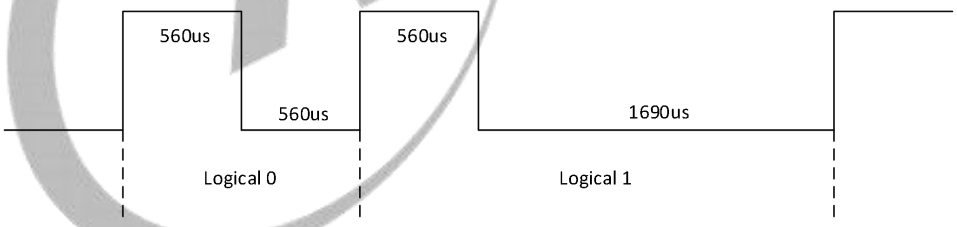
When CIR_RX signals satisfy the Active Threshold (ATHR), the CIR receiver can start to capture. In the process, the signal is ignored if the pulse width of the signal is less than NTHR. When CIR_RX signals satisfy ITHR (Idle Threshold), the capture process is stopped and the Receiver Packet End interrupt is generated, then the Receiver Packet End Flag is asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of the Run-Length Code. The MSB bit of a byte is the polarity of pulse, and the rest 7 bits is pulse width by taking Sample Clock as a basic unit. This is the code form of the RLC-Byte. When the level changes or the pulse width counter overflows, the RLC-Byte is buffered to FIFO. The CIR_RX module receives the infrared signals transmitted by the infrared remote control, the software decodes the signals.

8.1.3.5 Operating Mode

Sample Clock

Figure 8-4 Logical '0' and Logical '1' of NEC Protocol



For NEC protocol, a logical "1" takes 2.25 ms (560 us+1680 us) to transmit, while a logical "0" is only half of that, being 1.12 ms (560 us+560 us).

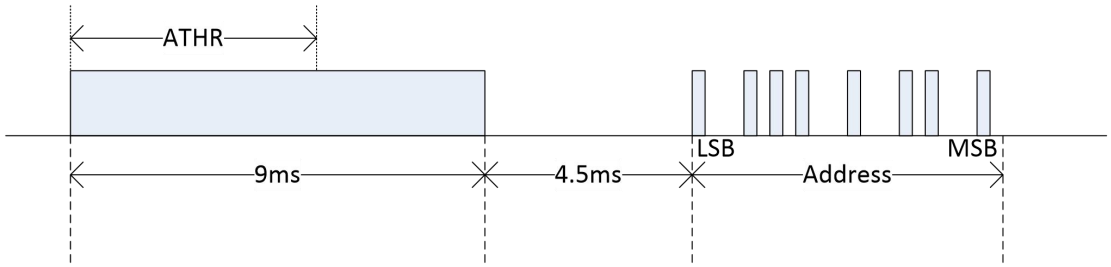
For example, if the sample clock is 31.25 kHz, a sample cycle is 32 us, then 18 sample cycles are 560 us. So the RLC of 560 us low level is 0x12 (b'00010010), the RLC of 560 us high level is 0x92 (b'10010010). Then a logical "1" takes code 0x12 (b'00010010) and code 0xb5 (b'10110101) to transmit, a logical "0" takes code 0x12 and code 0x92 to transmit.

Active Threshold (ATHR)

When the CIR receiver is in Idle state, if the electrical level of the IR-RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then the CIR receiver takes the

starting of the signal as a lead code, and the CIR receiver turns into an active state and starts to capture IR-RX signals.

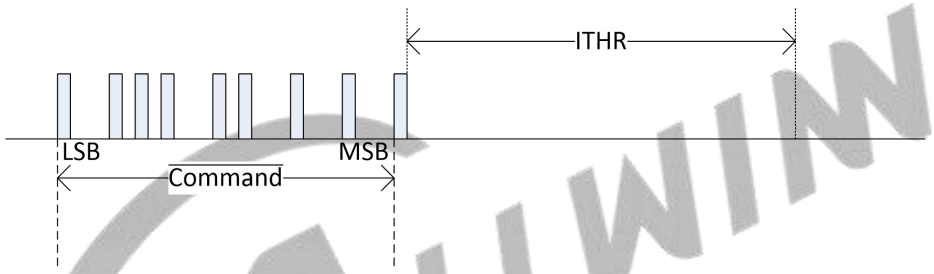
Figure 8-5 ATHR Definition



Idle Threshold (ITHR)

If the electrical level of IR-RX signals has no change, and the duration reaches this threshold, then the CIR receiver enters into Idle state and ends this capture.

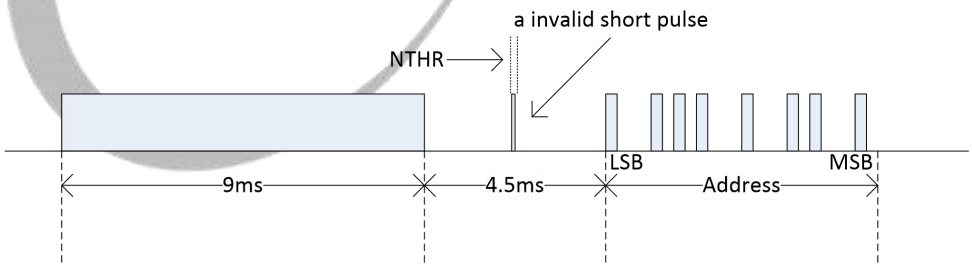
Figure 8-6 ITHR Definition



Noise Threshold (NTHR)

In the capture process, the pulse is ignored if the pulse width is less than the Noise Threshold.

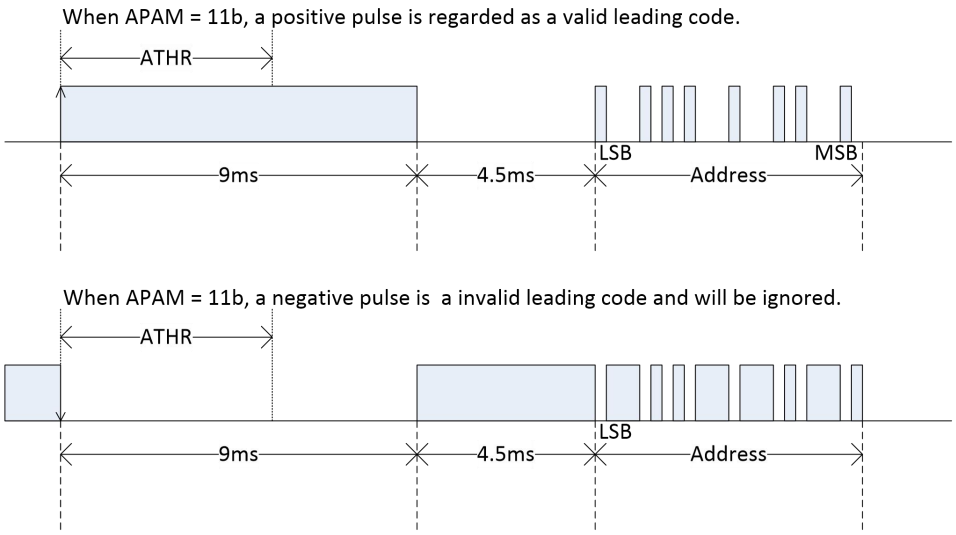
Figure 8-7 NTHR Definition



Active Pulse Accept Mode (APAM)

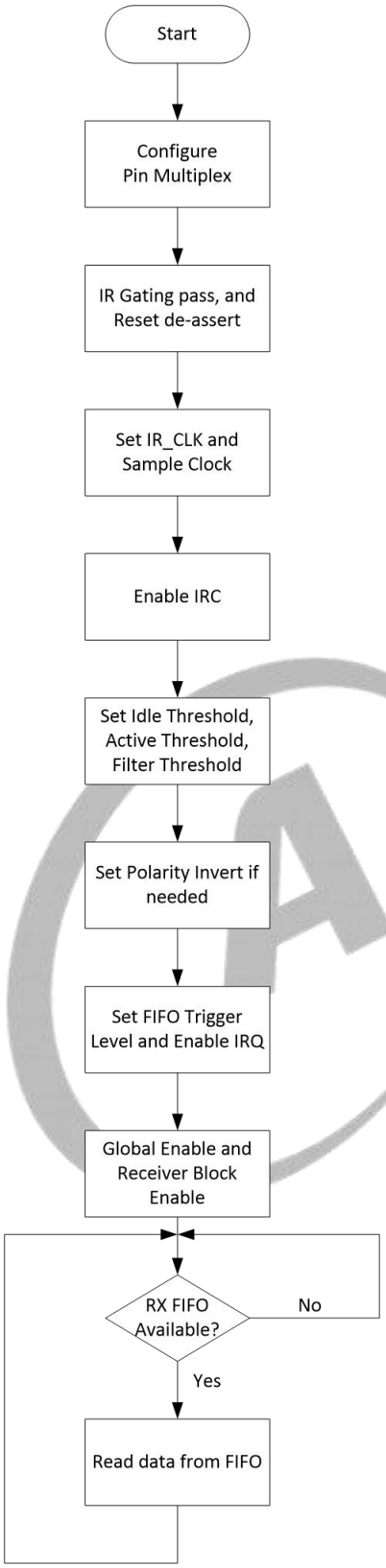
The APAM is used to fit the type of lead code. If a pulse does not fit the type of lead code, it is not regarded as a lead code even if the pulse width reaches ATHR.

Figure 8-8 APAM Definition



8.1.4 Programming Guidelines

Figure 8-9 CIR Receiver Process



8.1.5 Register List

Module Name	Base Address
S_CIRRX	0x0704 0000
IRRX	0x0200 5000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Receiver Control Register
CIR_RXCTL	0x0010	CIR Receiver Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_CONFIG	0x0034	CIR Receiver Configure Register
CIR_STORE0	0x0080	CIR Receiver Store Register0
CIR_STORE1	0x0084	CIR Receiver Store Register1
CIR_STORE2	0x0088	CIR Receiver Store Register2
CIR_STORE3	0x008C	CIR Receiver Store Register3

8.1.6 Register Description

8.1.6.1 0x0000 CIR Receiver Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	Read/Write	Default/HEX	Description
31:8	/	/	/
7:6	R/W	0x0	APAM Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code. 10: Only negative pulse is valid as a leading code. 11: Only positive pulse is valid as a leading code.
5:4	R/W	0x0	CEN CIR ENABLE 00-10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable

Offset: 0x0000			Register Name: CIR_CTL
Bit	Read/Write	Default/HEX	Description
			A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

8.1.6.2 0x0010 CIR Receiver Configure Register (Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXCTL
Bit	Read/Write	Default/HEX	Description
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert. 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

8.1.6.3 0x0020 CIR Receiver FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	Read/Write	Default/HEX	Description
31:8	/	/	/
7:0	R	0x0	RBF Receiver Byte FIFO

8.1.6.4 0x002C CIR Receiver Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	Read/Write	Default/HEX	Description
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when

Offset: 0x002C			Register Name: CIR_RXINT
Bit	Read/Write	Default/HEX	Description
			condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

8.1.6.5 0x0030 CIR Receiver Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	Read/Write	Default/HEX	Description
31:15	/	/	/
14:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1-byte available data in RX FIFO 2: 2-byte available data in RX FIFO ... 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0x0: Idle 0x1: busy
6:5	/	/	/
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a '1'.

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	Read/Write	Default/HEX	Description
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7'b0000,000 and 8'b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a '1'.
0	R/W1C	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a '1'.

8.1.6.6 0x0034 CIR Receiver Configure Register (Default Value: 0x0000_1828)

Offset: 0x0034			Register Name: CIR_CONFIG
Bit	Read/Write	Default/HEX	Description
31	/	/	/
30:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0x0:ATHR in Unit of (Sample Clock) 0x1:ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1) *(ATHC? Sample Clock: 128*Sample Clock)).
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the

<table>
<tr><td colspan="3">Offset: 0x0034</td><td>Register Name: CIR_CONFIG</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/HEX</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xa</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0: all samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0x0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>IR_CLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IR_CLK /128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>IR_CLK /256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IR_CLK /512</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>IR_CLK</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
</table>

8.1.6.7 0x0080 CIR Receiver Store Register0 (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_STORE0
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV0

Offset: 0x0080			Register Name: CIR_STORE0
Bit	Read/Write	Default/HEX	Description
			Receiver Store Value 0

8.1.6.8 0x0084 CIR Receiver Store Register1 (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CIR_STORE1
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV1 Receiver Store Value 1

8.1.6.9 0x0088 CIR Receiver Store Register2 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: CIR_STORE2
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV2 Receiver Store Value 2

8.1.6.10 0x008C CIR Receiver Store Register3 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: CIR_STORE3
Bit	Read/Write	Default/HEX	Description
31:0	R/W	0x0	SV3 Receiver Store Value 3

8.2 CIR Transmitter (CIR_TX)

8.2.1 Overview

The CIR transmitter (CIR_TX) can transfer arbitrary waves which can be modulated with configurable carrier waves such as 38 kHz. CIR_TX only uses lower 8 bits of the 32-bit registers. CIR_TX stores a 16-bit number in 2 registers, where one register contains the higher 8 bits while the other contains the lower 8 bits.

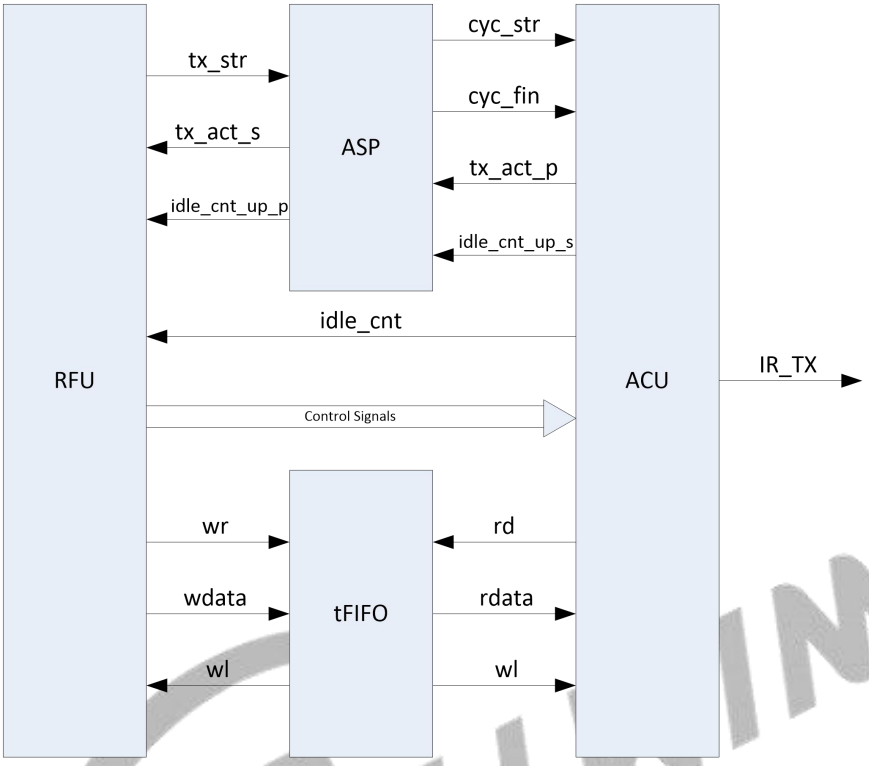
The CIR_TX has the following features:

- One CIR_TX interface in CPUX domain
- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Full physical layer implementation
- Arbitrary wave generator
- Configurable carrier frequency
- Handshake mode and waiting mode of DMA
- 128 bytes FIFO for data buffer
- Supports Interrupts and DMA

8.2.2 Block Diagram

The following figure shows a block diagram of the CIR_TX.

Figure 8-10 CIR_TX Block Diagram



8.2.3 Functional Description

8.2.3.1 External Signals

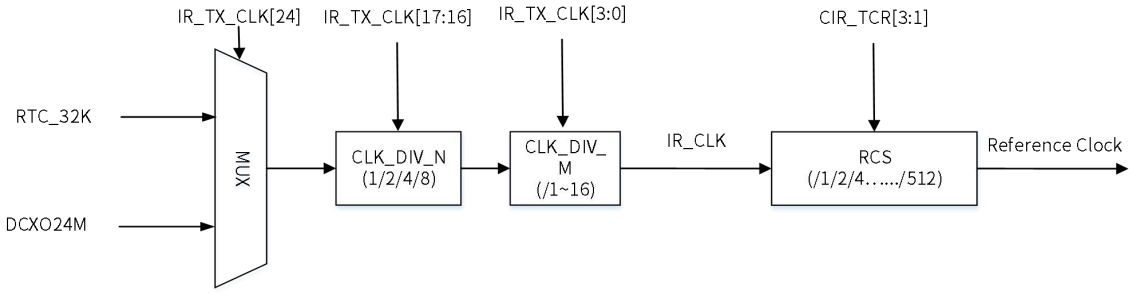
The following table describes the external signals of CIR_TX.

Table 8-3 CIR_TX External Signals

Signal Name	Description	Type
IR-TX	Consumer Infrared Receiver	I

8.2.3.2 Clock Sources

Figure 8-11 CIR_TX Clock Description



8.2.3.3 Function Implementation

The CIR_TX is used to generate a waveform of arbitrary length, arbitrary shape, and no high-speed requirement, and it can change the data into the high-/low-level sequence of a certain length. Every transmitting data is in bytes, the Bit[7] of a byte means whether the level of a transmitting wave is high or low, the Bit[6:0] is the length of this wave. If the current transmitting frequency-division is 1, 0x88 is a high level of 8 cycles, 0x08 is a low level of 8 cycles. If the current transmitting frequency-division is 4, 0x88 is a high level of 32 cycles, 0x08 is a low level of 32 cycles.

The CIR_TX has two transmission modes: non-cycle transmission, and cycle transmission.

The non-cycle transmission is to transmit all the data in TX_FIFO until the FIFO is empty.

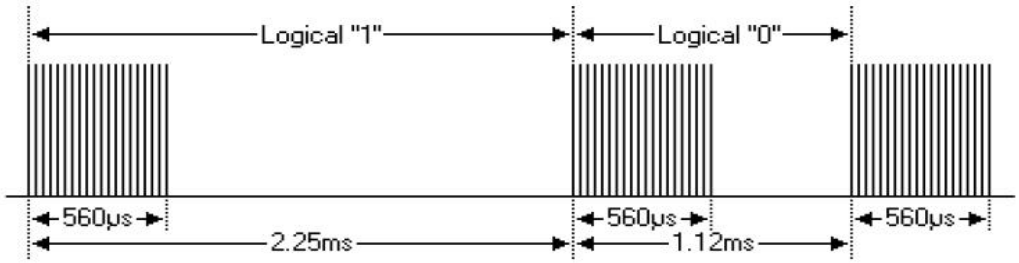
The cycle transmission is to transmit all the data in TX_FIFO, after the transmission completion, wait for a certain time to recover the data in TX_FIFO and then send it until a stop signal is detected. The data recovery in FIFO is implemented by clearing the read pointer.

8.2.3.4 Timing Diagram

The IR remote control contains many protocols designed by different manufacturers. Here to NEC protocol as an example, the CIR_TX module uses a variable pulse-width modulation technique to encompass the various formats of infrared encoding for remote-control applications. A message is started by a 9 ms AGC burst, which is used to set the gain of the earlier CIR receivers. This AGC burst is then followed by a 4.5 ms space, which is then followed by the address and command.

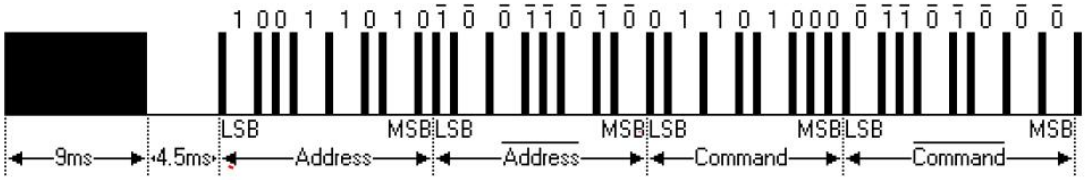
Bit definition: the logical “1” takes 2.25 ms to transmit, while a logical “0” is only 1.12 ms.

Figure 8-12 Definitions of Logical “1” and Logical “0”



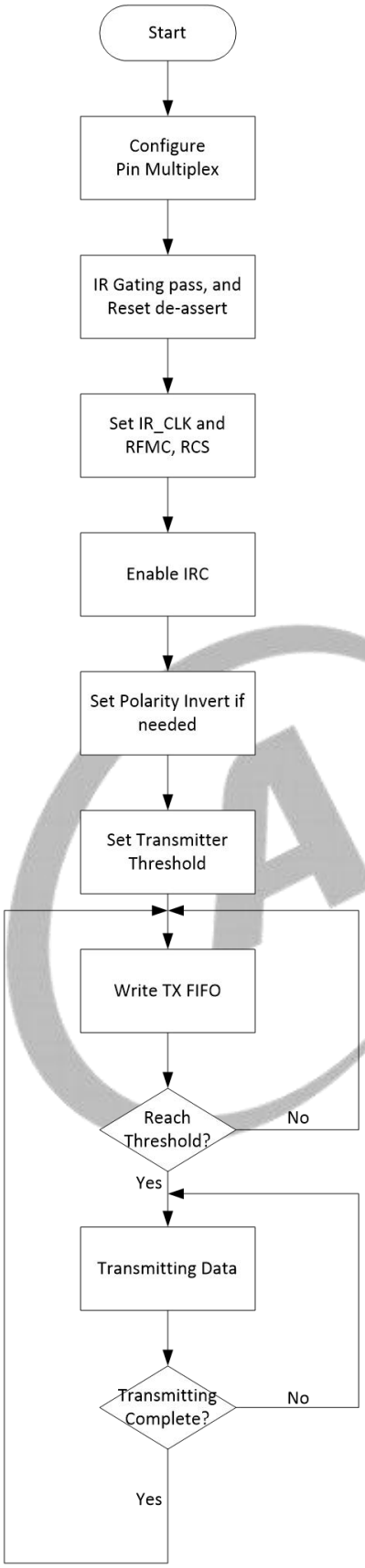
Timing for a message:

Figure 8-13 CIR Message Timing Diagram



8.2.4 Programming Guidelines

Figure 8-14 CIR Transmitter Process



8.2.5 Register List

Module Name	Base Address
CIR_TX	0x0200 3000

Register Name	Offset	Description
CIR_TGLR	0x0000	CIR Transmit Global Register
CIR_TMCR	0x0004	CIR Transmit Modulation Control Register
CIR_TCR	0x0008	CIR Transmit Control Register
CIR_IDC_H	0x000C	CIR Transmit Idle Duration Threshold Register
CIR_IDC_L	0x0010	CIR Transmit Idle Duration Threshold Register
CIR_TICR_H	0x0014	CIR Transmit Idle Counter Register
CIR_TICR_L	0x0018	CIR Transmit Idle Counter Register
CIR_TEL	0x0020	CIR TX FIFO empty Level Register
CIR_TXINT	0x0024	CIR Transmit Interrupt Control Register
CIR_TAC	0x0028	CIR Transmit FIFO Available Counter Register
CIR_TXSTA	0x002C	CIR Transmit Status Register
CIR_TXT	0x0030	CIR Transmit Threshold Register
CIR_DMA	0x0034	CIR DMA Control Register
CIR_TXFIFO	0x0080	CIR Transmit FIFO Data Register

8.2.6 Register Description

8.2.6.1 0x0000 CIR Transmitter Global Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_TGLR
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0x0	IMS Internal Modulation Select 0: the transmitting signal is not modulated 1: the transmitting signal is modulated internally
6:5	R/W	0x0	DRMC Duty ratio of modulated carrier is high level /low level. 0: low level is the one time of high level 1: low level is the two times of high level 2: low level is the three times of high level 3: reserved
4:3	/	/	/
			TPPI Transmit Pulse Polarity Invert

Offset: 0x0000			Register Name: CIR_TGLR
Bit	Read/Write	Default	Description
2	R/W	0x0	0: Not invert transmit pulse 1: Invert transmit pulse
1	R/W	0x0	TR Transmit Reset When this bit is set, the transmitting is reset. The FIFO will be flush, the TIC filed and CSS field will be clean during Transmit Reset. This field will automatically clean when the Transmit Reset is finished, and the CIR transmitter will state Idle .
0	R/W	0x0	TXEN Transmit Block Enable 0: Disable the CIR Transmitter 1: Enable the CIR Transmitter

8.2.6.2 0x0004 CIR Transmitter Modulation Control Register (Default Value:0x0000_009E)

Offset: 0x0004			Register Name: CIR_TMCR
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x9E	RFMC Reference Frequency of modulated carrier. Reference Frequency of modulated carrier based on a division of a fixed functional clock(FCLK). The range of the modulated carrier is usually 30KHZ to 60KHz.The most consumer electronics is 38KHz. The default modulated carrier is 38KHz when FCLK is 12MHz. RFMC= FCLK/((N+1)*(DRMC+2)).

8.2.6.3 0x0008 CIR Transmitter Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CIR_TCR
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0x0	CSS Cyclical Pulse Start/Stop Control Start to transmit when set to '1', 0: Stop when cleared to '0'. From start to stop, all data in FIFO must be transmitted. 1: Start.
6:4	/	/	/

Offset: 0x0008			Register Name: CIR_TCR
Bit	Read/Write	Default	Description
3:1	R/W	0x0	RCS Reference Clock Select for CIR Transmit 000: CIR Transmit reference clock is ir_clk 001: CIR Transmit reference clock is ir_clk/2 010: CIR Transmit reference clock is ir_clk/4 011: CIR Transmit reference clock is ir_clk/8 100: CIR Transmit reference clock is ir_clk/64 101: CIR Transmit reference clock is ir_clk/128 110: CIR Transmit reference clock is ir_clk/256 111: CIR Transmit reference clock is ir_clk/512
0	R/W	0x0	TTS Type of the transmission signal 0: The transmitting wave is single non-cyclical pulse. 1: The transmitting wave is cyclical short-pulse.

8.2.6.4 0x000C CIR Transmitter Idle Duration Counter Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CIR_IDC_H
Bit	Read/Write	Default	Description
31:8	/	/	/
3:0	R/W	0x0	IDC_H Idle Duration Counter threshold (High 4 bit) Idle Duration = 128*IDC*Ts (IDC = 0-4095)

8.2.6.5 0x0010 CIR Transmitter Idle Duration Counter Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CIR_IDC_L
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	IDC_L Idle Duration Counter threshold (Low 8 bit) Idle Duration = 128*IDC*Ts (IDC = 0-4095)

8.2.6.6 0x0014 CIR Transmitter Idle Counter Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CIR_TICR_H
Bit	Read/Write	Default	Description
31:8	/	/	/

Offset: 0x0014			Register Name: CIR_TICR_H
Bit	Read/Write	Default	Description
7:0	R	0x0	TIC_H Transmit Idle Counter_H (High 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

8.2.6.7 0x0018 CIR Transmitter Idle Counter Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CIR_TICR_L
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x0	TIC_L Transmit Idle Counter_L (Low 8 bit) Count in 128*Ts (Sample Duration, 1/Fs) when transmitter is idle, and it should be reset when the transmitter active. When this counter reaches the maximum value (0xFFFF), it will stop automatically, and should not be cleared to zero.

8.2.6.8 0x0020 CIR Transmitter FIFO Empty Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_TEL
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	TEL TX FIFO empty Level for DRQ and IRQ. TRIGGER_LEVEL = TEL + 1

8.2.6.9 0x0024 CIR Transmitter Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CIR_TXINT
Bit	Read/Write	Default	Description
31:3	/	/	/

Offset: 0x0024			Register Name: CIR_TXINT
Bit	Read/Write	Default	Description
2	R/W	0x0	DRQ_EN TX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails.
1	R/W	0x0	TAI_EN TX FIFO Available Interrupt Enable 0: Disable 1:Enable
0	R/W	0x0	TPEI_EN Transmit Packet End Interrupt Enable for Cyclical Pulse 0: Disable 1: Enable TUI_EN Transmitter FIFO under run Interrupt Enable for Non-cyclical Pulse 0: Disable 1: Enable

8.2.6.10 0x0028 CIR Transmitter FIFO Available Counter Register (Default Value: 0x0000_0080)

Offset: 0x0028			Register Name: CIR_TAC
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0x80	TAC TX FIFO Available Space Counter 0x00: No available space in TX FIFO 0x01: 1-byte available space in TX FIFO 0x02: 2-byte available space in TX FIFO ... 0x80: 128 byte available space in TX FIFO

8.2.6.11 0x002C CIR Transmitter Status Register (Default Value: 0x0000_0002)

Offset: 0x002C			Register Name: CIR_TXSTA
Bit	Read/Write	Default	Description
31:4	/	/	/
3	R	0x0	STCT Status of CIR Transmitter 0x0: Idle 0x1: Active This bit will automatically set when the controller begins transmit the data in the FIFO. The “1” will last when the data in the FIFO. It will automatically be cleaned to “0” when all data in the FIFO is transmitted. The bit is for debug. Output Level of Idle state determined by level of the last data output.
2	R	0x0	DRQ DMA Request Flag When set to ‘1’, the TX FIFO DRQ is asserted if the number of the transmitting data in the FIFO is less than the RAL. The DRQ is de-asserted when condition fails. This bit is for debug.
1	R/W	0x1	TAI TX FIFO Available Interrupt Flag 0: TX FIFO not available by its level 1: TX FIFO available by its level This bit can be cleared by software writing ‘1’.
0	R/W	0x0	TPE Transmitter Packet End Flag for Cyclical Pulse 0: Transmissions of address, control and data fields not completed 1: Transmissions of address, control and data fields completed TUR Transmitter FIFO Under Run Flag for Non-cyclical Pulse 0: No transmitter FIFO under run 1: Transmitter FIFO under run This bit is cleared by writing a ‘1’.

8.2.6.12 0x0030 CIR Transmitter Threshold Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_TXT
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0x0	NCTT Non-cyclical Pulse Transmit Threshold The controller will trigger transmitting the data in the FIFO when the data byte number has reaches the Transmit Threshold set in this field.

8.2.6.13 0x0034 CIR Transmitter DMA Control Register (Default Value: 0x0000_00A5)

Offset: 0x0034			Register Name: CIR_DMA_CTL
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0xA5	DMA Handshake configuration 0xA5: DMA wait cycle mode 0xEA: DMA handshake mode

8.2.6.14 0x0080 CIR Transmitter FIFO Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: CIR_TXFIFO
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	W	0x0	Transmit Byte FIFO When the transmitting is trigger, the data in the FIFO will be transmitted until the data number has been transmitted finished.

8.3 GMAC

8.3.1 Overview

The Gigabit Medium Access Controller (GMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000 Mbit/s external PHY with RMII/RGMII interface in full-duplex and half-duplex modes. The internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors.

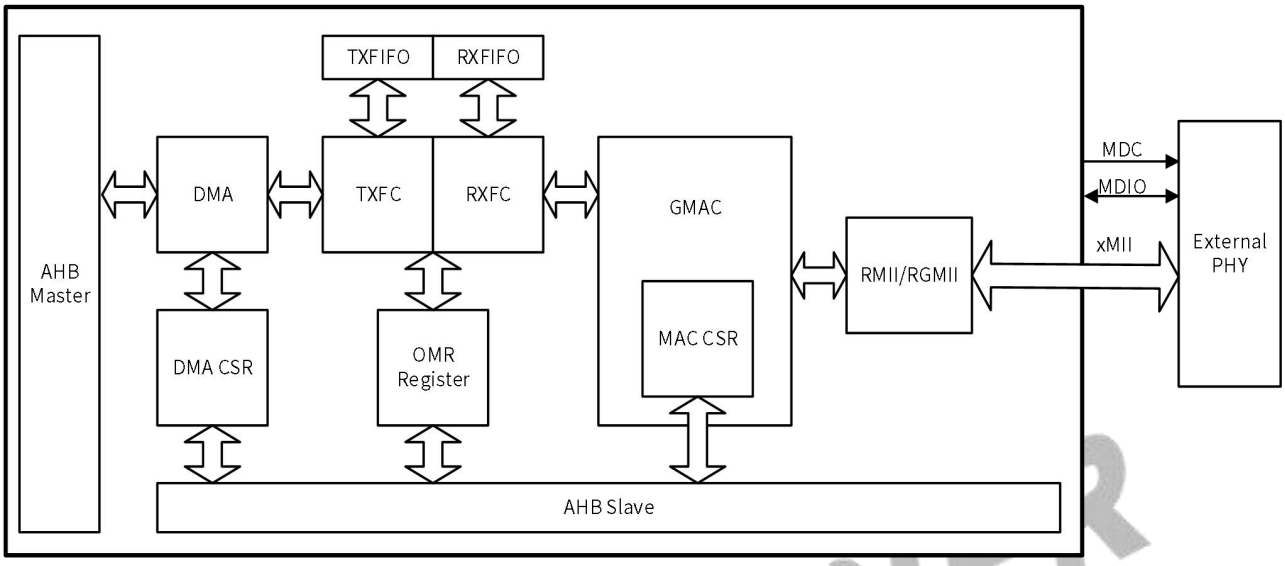
The GMAC has the following features:

- One GMAC interface (GMAC) for connecting external Ethernet PHY
- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operations
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
  - Supports linked-list descriptor list structure
  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
  - Comprehensive status reporting for normal operation and transfers with errors
- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions
- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies

8.3.2 Block Diagram

The following figure shows the block diagram of GMAC.

Figure 8-15 GMAC Block Diagram



8.3.3 Functional Description

8.3.3.1 External Signals

The following table describes the pin list of GMAC.

Table 8-4 GMAC External Siganls

Signal Name	Description	Type
RGMII0-RXD0/RMII0-RXD0	RGMII/RMII Receive Data0	I
RGMII0-RXD1/RMII0-RXD1	RGMII/RMII Receive Data1	I
RGMII0-RXD2/RMII0-NULL	RGMII Receive Data2	I
RGMII0-RXD3/RMII0-NULL	RGMII Receive Data3	I
RGMII0-RXCK/ RMII0-NULL	RGMII Receive Clock	I
RGMII0-RXCTRL/RMII0-CRS-DV	RGMII Receive Control/RMII Carrier Sense Receive Data Valid	I
RGMII0-CLKIN/RMII0-RXER	RGMII Transmit Clock from External/RMII Receive Error	I
RGMII0-TXD0/RMII0-TXD0	RGMII/RMII Transmit Data0	O
RGMII0-TXD1/RMII0-TXD1	RGMII/RMII Transmit Data1	O
RGMII0-TXD2/RMII0-NULL	RGMII Transmit Data2	O
RGMII0-TXD3/RMII0-NULL	RGMII Transmit Data3	O
RGMII0-TXCK/RMII0-TXCK	RGMII/RMII Transmit Clock For RGMII, IO type is output;	I/O

Signal Name	Description	Type
	For RMII, IO type is input	
RGMII0-TXCTRL/RMII0-TXEN	RGMII Transmit Control/RMII Transmit Enable	O
RGMII0-MDC	RGMII Management Data Clock	O
RGMII0-MDIO	RGMII Management Data Input/ Output	I/O
RGMII0-EPHY-25M	25 MHz Output for GMAC PHY	O

8.3.3.2 Clock Sources

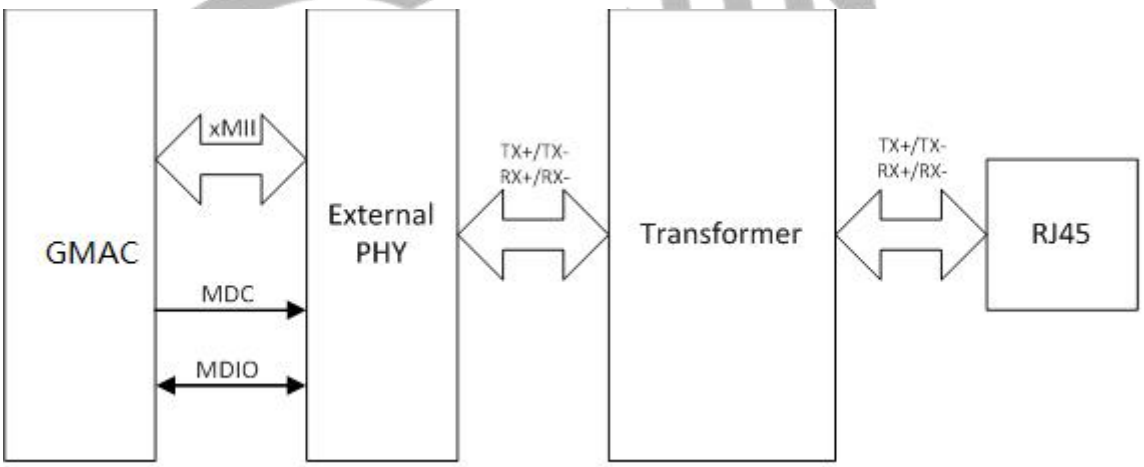
GMAC has two clock sources. The following table describes the clock sources of the GMAC.

Table 8-5 GMAC Clock Sources

Clock Sources	Description	Module
AHB	Bus clock. The bus frequency is 200 MHz.	CCU
GMAC_25M	GMAC 25M clock. The default value is 25 MHz.	

8.3.3.3 Typical Application

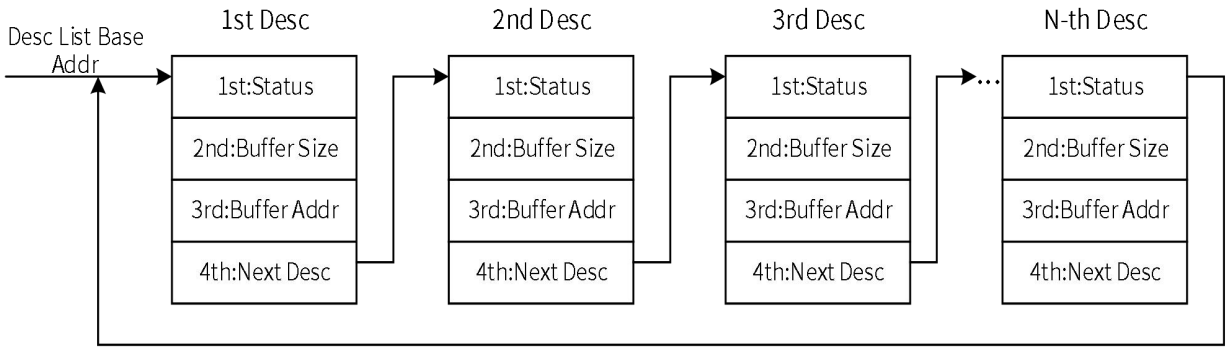
Figure 8-16 GMAC Typical Application



8.3.3.4 GMAC RX/TX Descriptor

The internal DMA of GMAC transfers data between host memory and internal RX/TX FIFO by a linked list of descriptors. Each descriptor consists of four words and contains some necessary information to transfer TX and RX frames. The following figure shows the descriptor list structure. The address of each descriptor must be 32-bit aligned.

Figure 8-17 GMAC RX/TX Descriptor List



8.3.3.5 TX Descriptor

1st Word of TX Descriptor

Bits	Description
31	TX_DESC_CTL When set, the current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in the buffer of the current descriptor are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of the header for the transmitted frame is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of the transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of the payload for the transmitted frame is wrong.
11	Reserved
10	TX_CRS_ERR When set, the carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of a collision after the contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR

Bits	Description
	When set, the frame is aborted because of the TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the GMAC defers the frame transmission.

2nd Word of TX Descriptor

Bits	Description
31	TX_INT_CTL When it is set and the current frame has been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When it is set, the current descriptor is the last one of the current frame.
29	FIR_DESC When it is set, the current descriptor is the first one of the current frame.
28:27	CHECKSUM_CTL These bits control to insert checksum in the transmit frame.
26	CRC_CTL When it is set, the CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of the buffer specified by the current descriptor.

3rd Word of TX Descriptor

Bits	Description
31:0	BUF_ADDR The address of the buffer specified by the current descriptor.

4th Word of TX Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of the next descriptor. It must be 32-bit aligned.

8.3.3.6 RX Descriptor

1st Word of RX Descriptor

Bits	Description
31	RX_DESC_CTL When it is set, the current descriptor can be used by DMA. This bit is cleared by DMA when the complete frame is received or the buffer of the current descriptor is full.
30	RX_DAF_FAIL When it is set, the current frame does not pass the DA filter.

Bits	Description
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for the current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of the received frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When it is set, the current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When it is set, the current fame does not pass the SA filter.
12	Reserved
11	RX_OVERFLOW_ERR When it is set, a buffer overflow error occurred and the current frame is wrong.
10	Reserved
9	FIR_DESC When it is set, the current descriptor is the first descriptor of the current frame.
8	LAST_DESC When it is set, the current descriptor is the last descriptor of the current frame.
7	RX_HEADER_ERR When it is set, the checksum of the frame header is wrong.
6	RX_COL_ERR When it is set, there is a late collision during the reception in half-duplex mode.
5	Reserved
4	RX_LENGTH_ERR When it is set, the length of the current frame is wrong.
3	RX_PHY_ERR When it is set, the receive error signal from PHY is asserted during the reception.
2	Reserved
1	RX_CRC_ERR When it is set, the CRC field of the received frame is wrong.
0	RX_PAYLOAD_ERR When it is set, the checksum or length of the payload for the received frame is wrong.

2nd Word of RX Descriptor

Bits	Description
31	RX_INT_CTL When it is set and a frame has been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of the buffer is specified by the current descriptor.

3rd Word of RX Descriptor

Bits	Description
31:0	BUF_ADDR The address of the buffer specified by the current descriptor.

4th Word of RX Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of the next descriptor. This field must be 32-bit aligned.

8.3.4 Programming Guidelines

8.3.4.1 GMAC System Configuration

Perform the following steps:

Step 1 Write 0 to GMAC_BGR_REG[bit16] to assert the module reset.

Step 2 Write 1 to GMAC_BGR_REG[bit16] to deassert the module reset.

Step 3 Write 1 to GMAC_BGR_REG[bit0] to enable the bus clock of the module.

Step 4 Configure the pin interfaces of GMAC by setting GPIO module.

Step 5 Configure GMAC_EPHY_CLK_REG0 Configuration Value to set the transmission clock source of RGMII/RMII.

- For RGMII RXCLK/CLK125M:

In RGMII mode, in addition to the configuration of the transmission clock source, it is generally necessary to adjust the timing by configuring the transmission clock delay, reception clock delay, transmission clock reverse, reception clock reverse.

- Write 0 to the bit [13] and write 1 to the bit [2] to select the RGMII interface.
- If selecting RXCLK as the clock source of RGMII, write 2 to the bit [1:0]; if selecting CLK125M as the clock source of RGMII, write 1 to the bit [1:0].
- Write 0 to the bit [3], write 0 to the bit [4], write 31 to the bit [9:5], and write 7 to the bit [12:10] to transmit the reception sequence adjustment.

- For RMII TXCLK:

- Write 1 to the bit [13] and write 0 to the bit [2] to select the RMII interface.
- Write 0 to the bit [0] to select TXCLK as the clock source of RMII.

The configuration value of GMAC_EPHY_CLK_REG0 can refer to the following table.

Table 8-6 GMAC_EPHY_CLK_REG0 Configuration Value

GMAC_EPHY	PHY_SEL	RMII_EN	ETXDC	ERXDC	ERXIE	ETXIE	RMII/RGMII	ETCS

	Bit15	Bit13	Bit[12:10]	Bit[9:5]	Bit4	Bit3	Bit2	Bit[1:0]
RGMII	0	0	7	31	0	0	1	1/2
RMII	0	1	0	0	0	0	0	0

8.3.4.2 GMAC Initialization

Step 1 Write 1 to GMAC_BASIC_CTL1[bit0] to perform the software reset.

Step 2 Write 1 to GMAC_BASIC_CTL1[bit1] to set the DMA priority of TX/RX.

Step 3 Configure GMAC_TX_CTL1 and GMAC_RX_CTL1 to set the configuration of DMA TX and DMA RX.

Step 4 Configure GMAC_INT_EN to set the corresponding interrupts and shield the needless interrupts.

Step 5 Configure GMAC_TX_DMA_LIST and GMAC_RX_DMA_LIST to set the first address of the TX descriptor and the RX descriptor, respectively.

Step 6 Configure GMAC_TX_CTL0 and GMAC_RX_CTL0 to set the TX and RX parameters. Configure GMAC_BASIC_CTL0 to set the speed, duplex mode, loopback configuration. (If enabled the auto-negotiation, the configuration is performed as a result of the negotiation)

Step 7 Configure GMAC_RX_FRM_FLT to set the RX frame filter.

Step 8 Configure GMAC_TX_FLOW_CTL and GMAC_RX_CTL0 to set the control mechanism of TX and RX.

Step 9 Clear all interrupt flags.

Step 10 Write 1 to GMAC_TX_CTL0[bit31] and write 1 to GMAC_RX_CTL0[bit31] to enable the TX and RX functions.

8.3.5 Register List

Module Name	Base Address
GMAC	0x04500000

Register Name	Offset	Description
GMAC_BASIC_CTL0	0x0000	GMAC Basic Control Register0
GMAC_BASIC_CTL1	0x0004	GMAC Basic Control Register1
GMAC_INT_STA	0x0008	GMAC Interrupt Status Register
GMAC_INT_EN	0x000C	GMAC Interrupt Enable Register
GMAC_TX_CTL0	0x0010	GMAC Transmit Control Register0
GMAC_TX_CTL1	0x0014	GMAC Transmit Control Register1

Register Name	Offset	Description
GMAC_TX_FLOW_CTL	0x001C	GMAC Transmit Flow Control Register
GMAC_TX_DMA_DESC_LIST	0x0020	GMAC Transmit Descriptor List Address Register
GMAC_RX_CTL0	0x0024	GMAC Receive Control Register0
GMAC_RX_CTL1	0x0028	GMAC Receive Control Register1
GMAC_RX_DMA_DESC_LIST	0x0034	GMAC Receive Descriptor List Address Register
GMAC_RX_FRM_FLT	0x0038	GMAC Receive Frame Filter Register
GMAC_RX_HASH0	0x0040	GMAC Hash Table Register0
GMAC_RX_HASH1	0x0044	GMAC Hash Table Register1
GMAC_MII_CMD	0x0048	GMAC Management Interface Command Register
GMAC_MII_DATA	0x004C	GMAC Management Interface Data Register
GMAC_ADDR_HIGH0	0x0050	GMAC MAC Address High Register0
GMAC_ADDR_LOW0	0x0054	GMAC MAC Address Low Register0
GMAC_ADDR_HIGHN	0x0050+0x08*N (N=1–7)	GMAC MAC Address High Register N (N=1–7)
GMAC_ADDR_LOWN	0x0054+0x08*N (N=1–7)	GMAC MAC Address Low Register N (N=1–7)
GMAC_TX_DMA_STA	0x00B0	GMAC Transmit DMA Status Register
GMAC_TX_CUR_DESC	0x00B4	GMAC Current Transmit Descriptor Register
GMAC_TX_CUR_BUF	0x00B8	GMAC Current Transmit Buffer Address Register
GMAC_RX_DMA_STA	0x00C0	GMAC Receive DMA Status Register
GMAC_RX_CUR_DESC	0x00C4	GMAC Current Receive Descriptor Register
GMAC_RX_CUR_BUF	0x00C8	GMAC Current Receive Buffer Address Register
GMAC_RGMII_STA	0x00D0	GMAC RGMII Status Register

8.3.6 Register Description

8.3.6.1 0x0000 GMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GMAC_BASIC_CTL0
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:2	R/W	0x0	SPEED GMAC Working Speed 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s

Offset: 0x0000			Register Name: GMAC_BASIC_CTL0
Bit	Read/Write	Default/Hex	Description
			11: 100 Mbit/s
1	R/W	0x0	LOOPBACK GMAC Loopback Mode for Test 0: Disable 1: Enable
0	R/W	0x0	DUPLEX GMAC Transfer Mode 0: Half-duplex 1: Full-duplex

8.3.6.2 0x0004 GMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: GMAC_BASIC_CTL1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA Priority 0: Same priority 1: RX priority is over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset All clock inputs must be valid before soft reset. This bit is cleared internally when the reset operation is completed fully. Before writing any register, this bit should read a 0.

8.3.6.3 0x0008 GMAC Interrupt Status Register (Default Value: 0x4000_0000)

Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	R	0x2000	Reserved
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending

Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
			Write '1' to clear it.
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First Data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, the length of the received frame is greater than 2048 bytes (10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, the RX DMA cannot acquire the next RX descriptor and RX DMA FSM is suspended. The ownership of the next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when the RX_DMA_START is written or the next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains running.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P

Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	Read/Write	Default/Hex	Description
			Total interrupt pending which the frame is transmitted to FIFO 0: No Pending 1: Pending Write '1' to clear it.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire the next TX descriptor and the TX DMA FSM is suspended. The ownership of the next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to TX_DMA_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.

8.3.6.4 0x000C GMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: GMAC_INT_EN
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN

Offset: 0x000C			Register Name: GMAC_INT_EN
Bit	Read/Write	Default/Hex	Description
			Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN

Offset: 0x000C			Register Name: GMAC_INT_EN
Bit	Read/Write	Default/Hex	Description
			Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

8.3.6.5 0x0010 GMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GMAC_TX_CTL0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disabled, the transmission will continue until the current transmission finishes.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

8.3.6.6 0x0014 GMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GMAC_TX_CTL1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0.
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission 1: Start and run TX DMA
29:11	/	/	/

Offset: 0x0014			Register Name: GMAC_TX_CTL1
Bit	Read/Write	Default/Hex	Description
10:8	R/W	0x0	TX_TH Threshold value of TX DMA FIFO When TX_MD is 0, the transmission starts when the frame size in TX DMA FIFO is greater than the threshold. In addition, the full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX starts after the TX DMA FIFO bytes is greater than the TX_TH 1: TX starts after the TX DMA FIFO is located a full frame
0	R/WAC	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO 0: Enable 1: Disable

8.3.6.7 0x001C GMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: GMAC_TX_FLOW_CTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After the transmission is completed, this bit will be cleared automatically. Before writing TX_FLOW_CTRL register, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic re-transmission of the pause frame. The threshold values should be always less than PAUSE_TIME.

Offset: 0x001C			Register Name: GMAC_TX_FLOW_CTL
Bit	Read/Write	Default/Hex	Description
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate the Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

8.3.6.8 0x0020 GMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GMAC_TX_DMA_LIST
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_DESC_LIST The base address of the transmission descriptor list It must be 32-bit aligned.

8.3.6.9 0x0024 GMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GMAC_RX_CTL0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2048 bytes (JUMBO_FRM_EN==0) Up to 10240 bytes (JUMBO_FRM_EN==1) 1: Up to 16384 bytes Any bytes after that is cut off.
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable

Offset: 0x0024			Register Name: GMAC_RX_CTL0
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable Jumbo frames of 9018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length of field value is less than or equal to 1500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with the address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decodes the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

8.3.6.10 0x0028 GMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GMAC_RX_CTL1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RX_DMA_START When set, the RX DMA will work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finishing the received current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable

Offset: 0x0028			Register Name: GMAC_RX_CTL1
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable, base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 Only valid when RX_MD == 0, the full frames with a length less than the threshold are transferred automatically.
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When the bit is set to 1, it indicates forward undersized frames with no error and length less than 64 bytes.
1	R/W	0x0	RX_MD Receive Mode 0: RX starts to read after the RX DMA FIFO byte is greater than RX_TH 1: RX starts to read after the RX DMA FIFO is located a full frame
0	R/W	0x0	FLUSH_RX_FRM

Offset: 0x0028			Register Name: GMAC_RX_CTL1
Bit	Read/Write	Default/Hex	Description
			Flush Receive Frames 0: Enable when the receive descriptors/buffers are unavailable 1: Disable

8.3.6.11 0x0034 GMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GMAC_RX_DMA_LIST
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_DESC_LIST The base address of the received descriptor list It must be 32-bit aligned.

8.3.6.12 0x0038 GMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GMAC_RX_FRM_FLT
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive all
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when passing the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST

Offset: 0x0038			Register Name: GMAC_RX_FRM_FLT
Bit	Read/Write	Default/Hex	Description
			Filter Multicast Frames Set 0: By comparing the DA field in DA MAC address registers 1: According to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: By comparing the DA field in DA MAC address registers 1: According to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of the SA filter. In addition, if the SA field of the received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass frames whose SA field matches SA MAC address registers 1: Pass frames whose SA field does not match SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it passes the address register filter or the hash filter (set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter (pass or fail) in the receive status word

8.3.6.13 0x0040 GMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: GMAC_RX_HASH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for the received frame filter.

8.3.6.14 0x0044 GMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: GMAC_RX_HASH1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for the received frame filter.

8.3.6.15 0x0048 GMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: GMAC_MII_CMD
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divider Ratio The MDC Clock is divided from the AHB clock. 000: 16 001: 32 010: 64 011: 128 Others: Reserved
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/WAC	0x0	MII_BUSY MII Status

Offset: 0x0048			Register Name: GMAC_MII_CMD
Bit	Read/Write	Default/Hex	Description
			0: Writing 0 is no valid, and reading 0 indicates the read/write operation is finished 1: Writing 1 starts the read/write operation, and reading 1 indicates busy.

8.3.6.16 0x004C GMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: GMAC_MII_DATA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

8.3.6.17 0x0050 GMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: GMAC_ADDR_HIGH0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16 bits of the 1st MAC address.

8.3.6.18 0x0054 GMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: GMAC_ADDR_LOW0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

8.3.6.19 0x0050+0x08*N GMAC MAC Address High Register N (Default Value: 0x0000_FFFF)

Offset: 0x0050+0x08*N (N=1-7)			Register Name: GMAC_ADDR_HIGHN
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: Used to compare with the destination address of

Offset: 0x0050+0x08*N (N=1-7)			Register Name: GMAC_ADDR_HIGHN
Bit	Read/Write	Default/Hex	Description
			the received frame 1: Used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of the MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH The upper 16 bits of the MAC address.

8.3.6.20 0x0054+0x08*N GMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x08*N (N=1-7)			Register Name: GMAC_ADDR_LOWN
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32 bits of MAC address N (N: 1–7).

8.3.6.21 0x00B0 GMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: GMAC_TX_DMA_STA
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, when reset or disable TX DMA 001: RUN_FETCH_DESC, fetching TX DMA descriptor 010: RUN_WAIT_STA, waiting for the status of TX frame 011: RUN_TRANS_DATA, passing the frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, closing TX descriptor 110: SUSPEND, TX descriptor is unavailable or TX DMA FIFO underflow

8.3.6.22 0x00B4 GMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: GMAC_TX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TX_DMA_CUR_DESC The address of current transmit descriptor.

8.3.6.23 0x00B8 GMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: GMAC_TX_DMA_CUR_BUF
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	TX_DMA_CUR_BUF The address of current transmit DMA buffer.

8.3.6.24 0x00C0 GMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: GMAC_RX_DMA_STA
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, when reset or disable RX DMA 001: RUN_FETCH_DESC, fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, waiting for the frame 100: SUSPEND, RX descriptor is unavailable 101: RUN_CLOSE_DESC, closing RX descriptor 110: Reserved 111: RUN_TRANS_DATA, passing the frame from host memory to RX DMA FIFO

8.3.6.25 0x00C4 GMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: GMAC_RX_DMA_CUR_DESC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DMA_CUR_DESC The address of current receive descriptor

8.3.6.26 0x00C8 GMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8	Register Name: GMAC_RX_DMA_CUR_BUF

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DMA_CUR_BUF The address of current receive DMA buffer

8.3.6.27 0x00D0 GMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: GMAC_RGMII_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of the RGMII interface 0: Down 1: Up
2:1	R	0x0	RGMII_LINK_SPD The link speed of the RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of the RGMII interface 0: Half-Duplex 1: Full-Duplex

8.4 General Purpose ADC (GPADC)

8.4.1 Overview

The General Purpose ADC (GPADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection. This ADC is a type of successive approximation register (SAR) A/D converter.

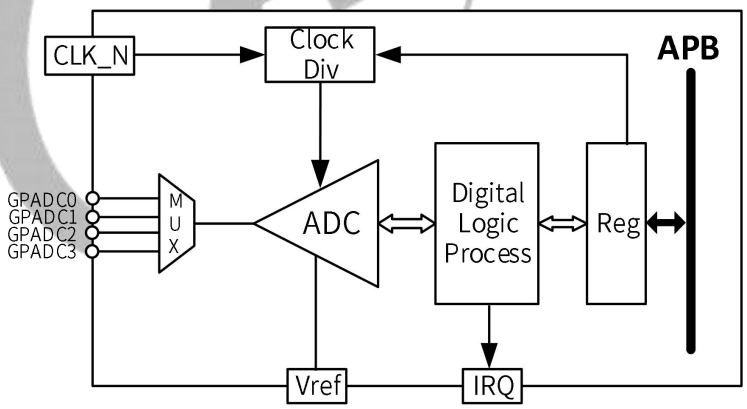
The GPADC has the following features:

- 4-ch successive approximation register (SAR) analog-to-digital converter (ADC)
- 64 FIFO depth of data register
- 12-bit sampling resolution and 10-bit precision
- Power reference voltage: AVCC, analog input voltage range: 0 to AVCC
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode
- Input voltage: 0 V to 1.8 V

8.4.2 Block Diagram

The following table shows the block diagram of the GPADC.

Figure 8-18 GPADC Block Diagram



8.4.3 Functional Description

8.4.3.1 External Signals

The following table describes the external signals of the GPADC.

Table 8-7 GPADC External Signals

Signal Name	Description	Type
GPADC0	General Purpose ADC Input Channel 0/ BROM Boot Select	AI
GPADC1	General Purpose ADC Input Channel 1	AI
GPADC2	General Purpose ADC Input Channel 2	AI
GPADC3	General Purpose ADC Input Channel 3	AI
VCM-ADC	External Capacitor Connection	A I/O
VREFN-ADC	GPADC Reference Voltage (Negative)	P
VREFP-ADC	GPADC Reference Voltage (Positive)	P

8.4.3.2 Clock Sources

The GPADC has one clock source. The following table describes the clock source for GPADC. Users can see section 2.5 Clock Controller Unit (CCU) for clock setting, configuration, and gating information.

Table 8-8 GPADC Clock Sources

Clock Sources	Description	module
HOSC	The default frequency is 24 MHz	CCU

8.4.3.3 GPADC Work Mode

- Single conversion mode

The GPADC completes one conversion in a specified channel, the converted data is updated at the data register of the corresponding channel.

- Continuous conversion mode

The GPADC has continuous conversion in a specified channel until the software stops, the converted data is updated at the data register of the corresponding channel.

- Burst conversion mode

The GPADC samples and converts in a specified channel, and sequentially stores the results in FIFO.

8.4.3.4 Clock and Timing Requirements

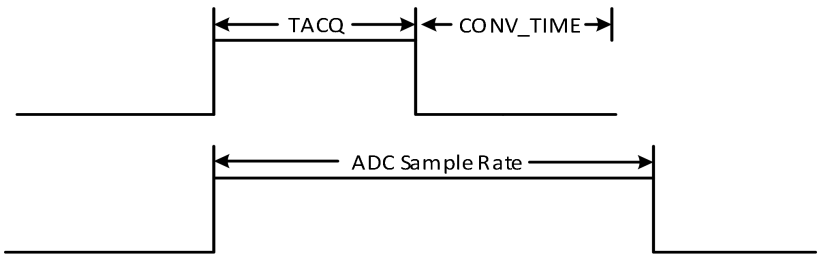
CLK_IN = 24 MHz

CONV_TIME (Conversion Time) = 1/(24MHz/13Cycles) =0.542 (us)

TACQ (ADC acquiring time) > 10RC (R is output impedance of ADC sample circuit, C = 6.4 pF)

ADC Sample Frequency > TACQ+CONV_TIME

Figure 8-19 GPADC Clock and Timing Requirement



8.4.3.5 GPADC Calculate Formula

GPADC calculate formula: GPADC_DATA = Vin/VREF*4095

Where:

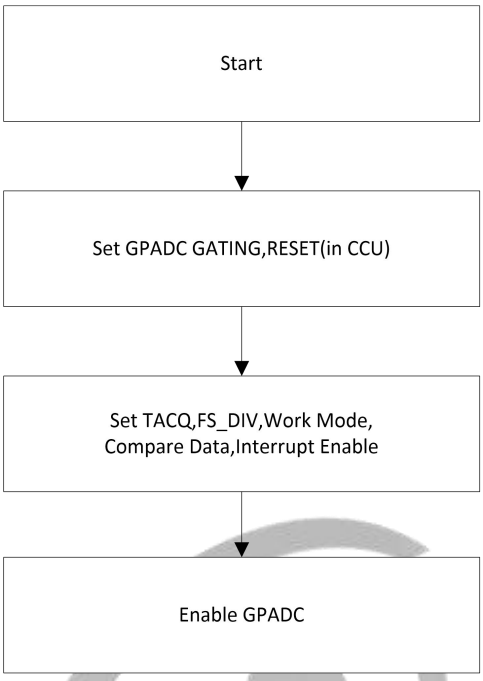
VREF = 1.8 V

8.4.4 Programming Guidelines

8.4.4.1 Initializing GPADC

The GPADC initial process is as follows.

Figure 8-20 GPADC Initial Process



Query Mode

Take channel0 for example:

Step 1 Write 0x1 to the bit [16] of GPADC_BGR_REG to dessert reset.

Step 2 Write 0x1 to the bit [0] of GPADC_BGR_REG to enable the GPADC clock.

Step 3 Write 0x2F to the bit [15:0] of GP_SR_CON to set the acquiring time of ADC.

Step 4 Write 0x1DF to the bit [31:16] of GP_SR_CON to set the ADC sample frequency divider.

Step 5 Write 0x2 to the bit [19:18] of GP_CTRL to set the continuous conversion mode.

Step 6 (Optional) If you need to configure the sampling frequency for each channel, follow these steps:

a) Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency set in step4 is multiplied by this value to get the actual sampling frequency. For detailed configuration information, please refer to section 8.4.4.2 Configuring Sampling Frequency.

b) Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0.

Step 7 Write 0x1 to the bit [0] of GP_CS_EN to enable the analog input channel.

Step 8 Write 0x1 to the bit [16] of GP_CTRL to enable the ADC function.

Step 9 Read the bit [0] of GP_DATA_INTS, if the bit is 1, then data conversion is complete.

Step 10 Read the bit [11:0] of GP_CH0_DATA, and calculate voltage value based on GPADC formula.

Interrupt Mode

Take channel0 for example:

Step 1 Write 0x1 to the bit [16] of GPADC_BGR_REG to dessert reset.

Step 2 Write 0x1 to the bit [0] of GPADC_BGR_REG to enable the GPADC clock.

Step 3 Write 0x2F to the bit [15:0] of GP_SR_CON to set the acquiring time of ADC.

Step 4 Write 0x1DF to the bit [31:16] of GP_SR_CON to set the ADC sample frequency divider.

Step 5 Write 0x2 to the bit [19:18] of GP_CTRL to set the continuous conversion mode.

Step 6 (Optional) If you need to configure the sampling frequency for each channel, follow these steps:

a) Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency set in step4 is multiplied by this value to get the actual sampling frequency. For detailed configuration information, please refer to section 8.4.4.2 Configuring Sampling Frequency.

b) Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0. Write 0x1 to the bit [0] of GP_CS_EN to enable the analog input channel.

Step 7 Write 0x1 to the bit [0] of GP_DATA_INTC to enable the GPADC data interrupt.

Step 8 Set the GIC module based on the IRQ 93.

Step 9 Put interrupt handler address into interrupt vector table based on the IRQ 93.

Step 10 Write 0x1 to the bit16 of GP_CTRL to enable the ADC function.

Step 11 Read the bit [11:0] of GP_CH0_DATA from the interrupt handler, calculate voltage value based on GPADC formula.

8.4.4.2 Configuring Sampling Frequency

The sampling frequency is only configurable in continue conversion mode. Note that the sampling frequency for each channel is only able to be configured as a multiple of 32 kHz and the total sampling frequency (sum of the sampling frequency of each channel) should be less than or equal to 1 MHz.

The sampling frequency configuration steps are as follows.

Step 1 If GPADC function is enabled, Configure the ADC_EN bit (bit [16]) of GP_CTRL (offset: 0x0004) register to disable ADC function.

Step 2 Configure the FS_DIV bit (bit [31:16]) of GP_SR_CON (offset: 0x0000) register to set the initial sampling frequency of each channel.

Step 3 Configure GP_SMP_TMS (offset: 0x00C0) register to set GP_SMP_TMS value. The initial sampling frequency is multiplied by this value to get the actual sampling frequency.

NOTE

All GPADC channels should be configured simultaneously.

The following are the all available sampling frequencies for each channel and corresponding GP_SMP_TMS values.

Table 8-9 GP_SMP_TMS Value Corresponding to Each Sampling Frequency

Sampling frequency	GP_SMP_TMS Value	Sampling frequency	GP_SMP_TMS Value
32 kHz	1	544 kHz	17
64 kHz	2	576 kHz	18
96 kHz	3	608 kHz	19
128 kHz	4	640 kHz	20
160 kHz	5	672 kHz	21
192 kHz	6	704 kHz	22
224 kHz	7	736 kHz	23
256 kHz	8	768 kHz	24
288 kHz	9	800 kHz	25
320 kHz	10	832 kHz	26
352 kHz	11	864 kHz	27
384 kHz	12	896 kHz	28
416 kHz	13	928 kHz	29
448 kHz	14	960 kHz	30
480 kHz	15	992 kHz	31
512 kHz	16	/	/

Step 4 Configure the GP_CH_SMP_BYP bit (bit {0}) of GP_SMP_BYP (offset: 0x00D0) register as 0.

Step 5 Configure the ADC_EN bit (bit [16]) of GP_CTRL (offset: 0x0004) register to enable ADC function.

8.4.5 Register List

Module Name	Base Address
GPADC	0x0200_9000

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register
GP_CH2_CMP_DATA	0x0048	GPADC CH2 Compare Data Register
GP_CH3_CMP_DATA	0x004C	GPADC CH3 Compare Data Register
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register
GP_CH2_DATA	0x0088	GPADC CH2 Data Register
GP_CH3_DATA	0x008C	GPADC CH3 Data Register
GP_SMP_TMS0	0x00C0	GPADC Sampling Times0 Register Description
GP_SMP_BYP	0x00D0	GPADC Channel Sample Rate Setting Bypass Register Description
GP_COMP_EN	0x00FC	GPADC Reference Voltage Source Select Register

8.4.6 Register Description

8.4.6.1 0x0000 GPADC Sample Rate Configure Register Description (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	Read/Write	Default/Hex	Description
31: 16	R/W	0x1DF	FS_DIV ADC Sample Frequency Divider CLK_IN/(n+1) Default value: 50K

Offset: 0x0000			Register Name: GP_SR_CON
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x2F	TACQ ADC Acquiring Time (n+1)/CLK_IN Default value: 2 us

8.4.6.2 0x0004 GPADC Control Register Description (Default Value: 0x0080_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	ADC_FIRST_DLY ADC First Convert Delay setting ADC conversion of each channel is delayed by N samples.
23	R/W	0x1	ADC_AUTOCALI_EN ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias Adjust the bandwidth of the ADC amplifier.
19:18	R/W	0x0	GP_MODE GPADC Work Mode 00: Single conversion mode 01: Single-cycle conversion mode 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: start Calibration, it is clear to 0 after calibration
16	R/W	0x0	ADC_EN ADC Function Enable Before the bit is enabled, configure ADC parameters including the work mode and channel number, etc. 0: Disable 1: Enable When selecting a single conversion mode, the bit can be cleared automatically after the switch is completed.
15:0	/	/	/

8.4.6.3 0x0008 GPADC Compare and Select Enable Register Description (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GP_CS_EN
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	ADC_CH3_CMP_EN Channel 3 Compare Enable 0: Disable 1: Enable
18	R/W	0x0	ADC_CH2_CMP_EN Channel 2 Compare Enable 0: Disable 1: Enable
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0x0	ADC_CH3_SELECT Analog input channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CH2_SELECT Analog input channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CH1_SELECT Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x0	ADC_CH0_SELECT Analog input channel 0 Select 0: Disable 1: Enable

8.4.6.4 0x000C GPADC FIFO Interrupt Control Register Description (Default Value: 0x0000_1F00)

Offset: 0x000C	Register Name: GP_FIFO_INTC

Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	FIFO_DATA_DRQ_EN ADC FIFO Date DRQ Enable 0: Disable 1: Enable
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/WAC	0x0	FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self-clear to '0'.
3:0	/	/	/

8.4.6.5 0x0010 GPADC FIFO Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING. ADC FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
16	R/W1C	0x0	FIFO_DATA_PENDING. ADC FIFO Data Available Pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt
15:14	/	/	/
13:8	R	0x0	RXA_CNT. ADC FIFO available Sample Word Counter
7:0	/	/	/

8.4.6.6 0x0014 GPADC FIFO Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	GP_FIFO_DATA GPADC Data in FIFO

8.4.6.7 0x0018 GPADC Calibration Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GP_CDATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x000	GP_CDATA GPADC Calibration Data

8.4.6.8 0x0020 GPADC Data Low Interrupt Configure Register Description (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CH3_LOW_IRQ_EN Channel 3 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_LOW_IRQ_EN Channel 2 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_LOW_IRQ_EN Channel 1 Voltage Low Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_LOW_IRQ_EN Channel 0 Voltage Low Available Interrupt Enable 0: Disable 1: Enable

8.4.6.9 0x0024 GPADC Data High Interrupt Configure Register Description (Default Value: 0x0000_0000)

Offset: 0x0024	Register Name: GP_DATAH_INTC

Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CH3_HIG_IRQ_EN Channel 3 Voltage High Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_HIG_IRQ_EN Channel 2 Voltage High Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_HIG_IRQ_EN Channel 1 Voltage High Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_HIG_IRQ_EN Channel 0 Voltage High Available Interrupt Enable 0: Disable 1: Enable

8.4.6.10 0x0028 GPADC DATA Interrupt Configure Register Description (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	CH3_DATA_IRQ_EN Channel 3 Data Available Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	CH2_DATA_IRQ_EN Channel 2 Data Available Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	CH1_DATA_IRQ_EN Channel 1 Data Available Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	CH0_DATA_IRQ_EN Channel 0 Data Available Interrupt Enable 0: Disable 1: Enable

8.4.6.11 0x0030 GPADC Data Low Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	CH3_LOW_PENGDING Channel 3 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_LOW_PENGDING Channel 2 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_LOW_PENGDING Channel 1 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_LOW_PENGDING Channel 0 Voltage Low Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

8.4.6.12 0x0034 GPADC Data High Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	CH3_HIG_PENGDING Channel 3 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_HIG_PENGDING Channel 2 Voltage High Available Interrupt Status

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	Read/Write	Default/Hex	Description
			0: NO Pending IRQ 1: Channel 2 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_HIG_PENGDING Channel 1 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_HIG_PENGDING Channel 0 Voltage High Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

8.4.6.13 0x0038 GPADC Data Interrupt Status Register Description (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W1C	0x0	CH3_DATA_PENGDING Channel 3 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 3 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
2	R/W1C	0x0	CH2_DATA_PENGDING Channel 2 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 2 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
1	R/W1C	0x0	CH1_DATA_PENGDING Channel 1 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 1 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
0	R/W1C	0x0	CH0_DATA_PENGDING

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	Read/Write	Default/Hex	Description
			Channel 0 Data Available Interrupt Status 0: NO Pending IRQ 1: Channel 0 Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails

8.4.6.14 0x0040 GPADC CH0 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0040			Register Name: GP_CH0_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

8.4.6.15 0x0044 GPADC CH1 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0044			Register Name: GP_CH1_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

8.4.6.16 0x0048 GPADC CH2 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x0048			Register Name: GP_CH2_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH2_CMP_HIG_DATA Channel 2 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH2_CMP_LOW_DATA Channel 2 Voltage Low Value

8.4.6.17 0x004C GPADC CH3 Compare Data Register Description (Default Value: 0x0BFF_0400)

Offset: 0x004C			Register Name: GP_CH3_CMP_DATA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0xBFF	CH3_CMP_HIG_DATA Channel 3 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH3_CMP_LOW_DATA Channel 3 Voltage Low Value

8.4.6.18 0x0080 GPADC CH0 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GP_CH0_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

8.4.6.19 0x0084 GPADC CH1 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

8.4.6.20 0x0088 GPADC CH2 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: GP_CH2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH2_DATA Channel 2 Data

8.4.6.21 0x008C GPADC CH3 Data Register Description (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: GP_CH3_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

Offset: 0x008C			Register Name: GP_CH3_DATA
Bit	Read/Write	Default/Hex	Description
11:0	R	0x000	GP_CH3_DATA Channel 3 Data

8.4.6.22 0x00C0 GPADC Sampling Times0 Register Description (Default Value 0x0000_0000)

Offset: 0x00C0			Register Name: GP_SMP_TMS0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x0	GP_ CH3_SMP_TMS GPADC Channel 3 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
23：22	/	/	/
21:16	R/W	0x0	GP_ CH2_SMP_TMS GPADC Channel 2 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
15：14	/	/	/
13:8	R/W	0x0	GP_ CH1_SMP_TMS GPADC Channel 1 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved
7:6	/	/	/
5:0	R/W	0x0	GP_ CH0_SMP_TMS GPADC Channel 0 Sampling Times Register 0: 0 (channel disable) 1: 1 ... 31:31 Other :reserved

8.4.6.23 0x00D0 GPADC Channel Sample Rate Setting Bypass Register Description (Default Value 0x00D0 0x0000_0001)

Offset: 0x00D0			Register Name: GP_SMP_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	GP_ CH_SMP_BYP GPADC Channel Sample Rate Setting Bypass Register 0: Enable sampling rate setting 1: Disable sampling rate setting

8.4.6.24 0x00FC GPADC Reference Voltage Source Select Register Description (Default Value 0x0000_0001)

Offset: 0x00FC			Register Name: GP_RVLT_SEL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	GP_RVLT_SEL GPADC Reference Voltage Source Selector 0: External LDO 1: Internal LDO

8.5 GPIO

8.5.1 Overview

The general purpose input/output (GPIO) is one of the blocks controlling the chip multiplexing pins. The A523 supports 10 groups of GPIO pins. Each pin can be configured as input or output and these pins are used to generate input signals or output signals for special purposes.

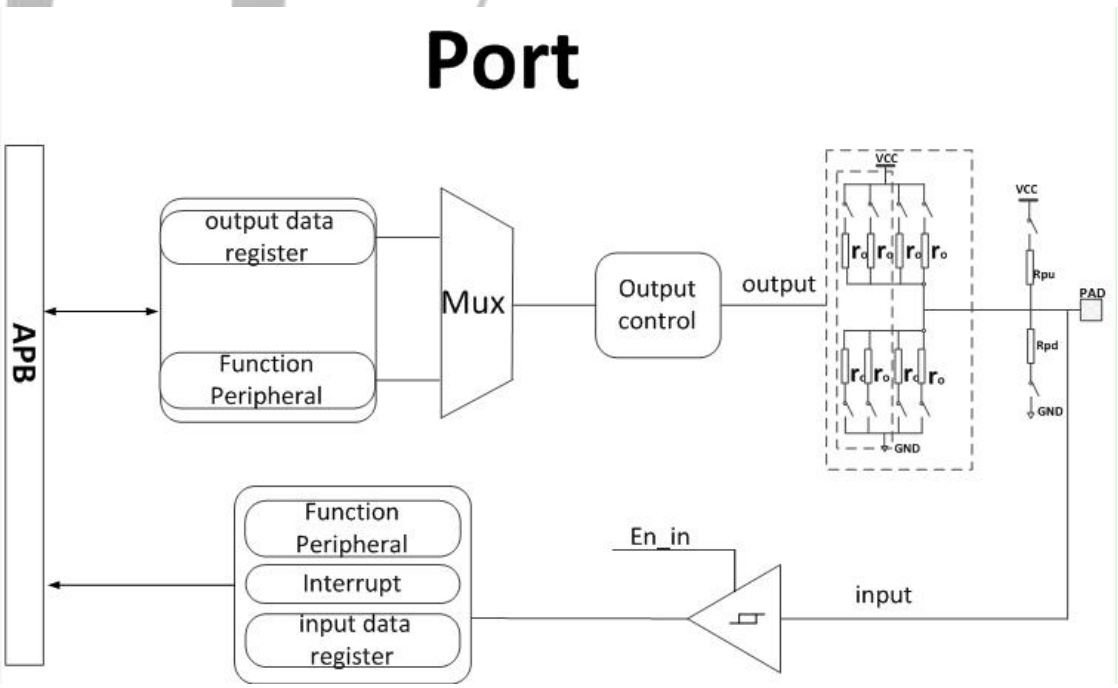
The GPIO has the following features:

- 10 groups of ports (PB, PC, PD, PE, PF, PG, PH, PK, PL, PM)
- Software control for each signal pin
- Data input (capture)/output (drive)
- Each GPIO peripheral can produce an interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 158 interrupts
- Configurable interrupt edges

8.5.2 Block Diagram

The following figure shows the block diagram of the GPIO.

Figure 8-21 GPIO Block Diagram



The GPIO consists of the digital part (GPIO, external interface) and IO analog part (output buffer, dual pull down, pad). The digital part can select the output interface by the MUX switch; the analog part can configure pull up/down and buffer strength.

When executing GPIO read state, the GPIO reads the current level of the pin into the internal register bus. When not executing GPIO read state, the external pin and the internal register bus are off-status, which is high-impedance.

8.5.3 Functional Description

8.5.3.1 Multi-function Port

The A523 includes 158 multi-functional input/output port pins. There are 10 ports as listed below.

Table 8-10 Multi-function Port

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Typical Power Supply
PB	15	Schmitt	CMOS	UART/TWI/ OWA/I2S/ SPI/JTAG/PWM/LCD	3.3 V
PC	17	Schmitt	CMOS	NAND/SDC/SPI/SPIFC	3.3 V/1.8 V
PD	24	Schmitt	CMOS	LCD/PWM/LVDS/SPI/DSI/UART/PWM	3.3 V/1.8 V
PE	16	Schmitt	CMOS	MCSI/TWI/UART/PLL_LOCK_DBG /PWM/I2S/ SPI/LEDC/ LCD/NCSI	3.3 V/1.8 V
PF	7	Schmitt	CMOS	SDC /JTAG/UART/I2S	3.3 V/1.8 V
PG	15	Schmitt	CMOS	SDC/UART/PCIE/I2S	3.3 V/1.8 V
PH	20	Schmitt	CMOS	TWI/UART/DMIC/CIR/ SPI/I2S/LEDC/OWA/RGMII0/RMII0/PCIE	3.3 V
PK	24	Schmitt	CMOS	MCSI /TWI/UART/PWM/NCSI	3.3V/1.8 V
PL	14	Schmitt	CMOS	CIR/JTAG/TWI/UART/PWM /JTAG/I2S/DMIC/SPI	3.3 V/1.8 V
PM	6	Schmitt	CMOS	UARY/TWI/PWM/CIR/JTAG	3.3 V/1.8 V

8.5.3.2 GPIO Multiplex Function

Table 8-11 to Table 8-20 show the multiplex function pins of the A523.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function7 to Function13 are reserved.

Table 8-11 PB Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PB0	I/O	UART2-TX	SPI2-CS0	JTAG-MS	LCD0-D0	PWM6	PB-EINT0
PB1	I/O	UART2-RX	SPI2-CLK	JTAG-CK	LCD0-D1	PWM7	PB-EINT1
PB2	I/O	UART2-RTS	SPI2-MOSI	JTAG-DO	LCD0-D8		PB-EINT2
PB3	I/O	UART2-CTS	SPI2-MISO	JTAG-DI	LCD0-D9		PB-EINT3
PB4	I/O	TWI1-SCK	I2S0-MCLK		PWM8		PB-EINT4
PB5	I/O	TWI1-SDA	I2S0-BCLK		PWM9		PB-EINT5
PB6	I/O		I2S0-LRCK		PWM10		PB-EINT6
PB7	I/O	OWA-IN	I2S0-DOUT0	I2S0-DIN1	LCD0-D16	PWM11	PB-EINT7
PB8	I/O	OWA-OUT	I2S0-DIN0	I2S0-DOUT1	LCD0-D17	PWM0	PB-EINT8
PB9	I/O	UART0-TX	TWI0-SCK		I2S0-DIN2	I2S0-DOUT2	PB-EINT9
PB10	I/O	UART0-RX	TWI0-SDA	PWM1	I2S0-DIN3	I2S0-DOUT3	PB-EINT10
PB11	I/O	TWI5-SCK	UART7-RTS	SPI1-CS0	PWM2		PB-EINT11
PB12	I/O	TWI5-SDA	UART7-CTS	SPI1-CLK	PWM3		PB-EINT12
PB13	I/O	TWI4-SCK	UART7-TX	SPI1-MOSI	PWM4		PB-EINT13
PB14	I/O	TWI4-SDA	UART7-RX	SPI1-MISO	PWM5		PB-EINT14

Table 8-12 PC Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PC0	I/O	NAND-WE	SDC2-DS				PC-EINT0
PC1	I/O	NAND-ALE	SDC2-RST				PC-EINT1
PC2	I/O	NAND-CLE		SPI0-MOSI	SPIF-MOSI		PC-EINT2
PC3	I/O	NAND-CE1		SPI0-CS0	SPIF-CS0		PC-EINT3
PC4	I/O	NAND-CE0		SPI0-MISO	SPIF-MISO		PC-EINT4
PC5	I/O	NAND-RE	SDC2-CLK				PC-EINT5
PC6	I/O	NAND-RB0	SDC2-CMD				PC-EINT6
PC7	I/O	NAND-RB1		SPI0-CS1	SPIF-DQS		PC-EINT7
PC8	I/O	NAND-DQ7	SDC2-D3		SPIF-D7		PC-EINT8
PC9	I/O	NAND-DQ6	SDC2-D4		SPIF-D6		PC-EINT9
PC10	I/O	NAND-DQ5	SDC2-D0		SPIF-D5		PC-EINT10
PC11	I/O	NAND-DQ4	SDC2-D5		SPIF-D4		PC-EINT11
PC12	I/O	NAND-DQS		SPI0-CLK	SPIF-CLK		PC-EINT12
PC13	I/O	NAND-DQ3	SDC2-D1				PC-EINT13
PC14	I/O	NAND-DQ2	SDC2-D6				PC-EINT14
PC15	I/O	NAND-DQ1	SDC2-D2	SPI0-WP	SPIF-WP		PC-EINT15
PC16	I/O	NAND-DQ0	SDC2-D7	SPI0-HOLD	SPIF-HOLD		PC-EINT16

Table 8-13 PD Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PD0	I/O	LCD0-D2	LVDS0-D0P	DSI0-D0P	PWM0		PD-EINT0
PD1	I/O	LCD0-D3	LVDS0-D0N	DSI0-D0N	PWM1		PD-EINT1
PD2	I/O	LCD0-D4	LVDS0-D1P	DSI0-D1P	PWM2		PD-EINT2
PD3	I/O	LCD0-D5	LVDS0-D1N	DSI0-D1N	PWM3		PD-EINT3
PD4	I/O	LCD0-D6	LVDS0-D2P	DSI0-CKP	PWM4		PD-EINT4
PD5	I/O	LCD0-D7	LVDS0-D2N	DSI0-CKN	PWM5		PD-EINT5
PD6	I/O	LCD0-D10	LVDS0-CKP	DSI0-D2P	PWM6		PD-EINT6
PD7	I/O	LCD0-D11	LVDS0-CKN	DSI0-D2N	PWM7		PD-EINT7
PD8	I/O	LCD0-D12	LVDS0-D3P	DSI0-D3P	PWM8		PD-EINT8
PD9	I/O	LCD0-D13	LVDS0-D3N	DSI0-D3N	PWM9		PD-EINT9
PD10	I/O	LCD0-D14	LVDS1-D0P	DSI1-D0P	PWM10	SPI1-CS0/DBI-CSX	PD-EINT10
PD11	I/O	LCD0-D15	LVDS1-D0N	DSI1-D0N	PWM11	SPI1-CLK/DBI-SCLK	PD-EINT11
PD12	I/O	LCD0-D18	LVDS1-D1P	DSI1-D1P	PWM12	SPI1-MOSI/DBI-SDO	PD-EINT12
PD13	I/O	LCD0-D19	LVDS1-D1N	DSI1-D1N	PWM13	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PD-EINT13

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PD14	I/O	LCD0-D20	LVDS1-D2P	DSI1-CKP	PWM14	UART3-TX	PD-EINT14
PD15	I/O	LCD0-D21	LVDS1-D2N	DSI1-CKN	PWM15	UART3-RX	PD-EINT15
PD16	I/O	LCD0-D22	LVDS1-CKP	DSI1-D2P	PWM16	UART3-RTS	PD-EINT16
PD17	I/O	LCD0-D23	LVDS1-CKN	DSI1-D2N	PWM17	UART3-CTS	PD-EINT17
PD18	I/O	LCD0-CLK	LVDS1-D3P	DSI1-D3P	PWM18	UART4-TX	PD-EINT18
PD19	I/O	LCD0-DE	LVDS1-D3N	DSI1-D3N	PWM19	UART4-RX	PD-EINT19
PD20	I/O	LCD0-HSYNC	PWM2	UART2-TX	UART7-RTS	UART4-RTS	PD-EINT20
PD21	I/O	LCD0-VSYNC	PWM3	UART2-RX	UART7-CTS	UART4-CTS	PD-EINT21
PD22	I/O	PWM1	SPI1-HOLD/DBI-DCX/DBI-WRX	UART2-RTS	UART7-TX	TWI0-SCK	PD-EINT22
PD23	I/O	PWM0	SPI1-WP/DBI-TE	UART2-CTS	UART7-RX	TWI0-SDA	PD-EINT23

Table 8-14 PE Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PE0	I/O	MCSI0-MCLK					PE-EINT0
PE1	I/O	TWI2-SCK	UART4-TX				PE-EINT1
PE2	I/O	TWI2-SDA	UART4-RX				PE-EINT2
PE3	I/O	TWI3-SCK	UART4-RTS				PE-EINT3
PE4	I/O	TWI3-SDA	UART4-CTS				PE-EINT4
PE5	I/O	MCSI1-MCLK	PLL-LOCK-DBG	I2S2-MCLK	LEDC		PE-EINT5
PE6	I/O			I2S2-BCLK	LCD0-TRIG	NCSI-D8	PE-EINT6
PE7	I/O			I2S2-LRCK	LCD1-TRIG	NCSI-D9	PE-EINT7
PE8	I/O			I2S2-DOUT0		NCSI-D10	PE-EINT8
PE9	I/O			I2S2-DIN0		NCSI-D11	PE-EINT9
PE10	I/O	MCSI3-MCLK	PWM3			NCSI-D12	PE-EINT10
PE11	I/O	TWI1-SCK	UART5-RTS	SPI2-CS0	UART6-TX	NCSI-D13	PE-EINT11
PE12	I/O	TWI1-SDA	UART5-CTS	SPI2-CLK	UART6-RX	NCSI-D14	PE-EINT12
PE13	I/O	TWI4-SCK	UART5-TX	SPI2-MOSI	UART6-RTS	CSI0-XVS-FSYNC	PE-EINT13
PE14	I/O	TWI4-SDA	UART5-RX	SPI2-MISO	UART6-CTS	CSI1-XVS-FSYNC	PE-EINT14
PE15	I/O	MCSI2-MCLK	PWM2			NCSI-D15	PE-EINT15

Table 8-15 PF Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PF0	I/O	SDC0-D1	JTAG-MS		I2S3-DIN0	I2S3-DOUT1	PF-EINT0
PF1	I/O	SDC0-D0	JTAG-DI		I2S3-DOUT0	I2S3-DIN1	PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX		I2S3-DIN2	I2S3-DOUT2	PF-EINT2
PF3	I/O	SDC0-CMD	JTAG-DO		I2S3-LRCK		PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX		I2S3-DIN3	I2S3-DOUT3	PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK		I2S3-BCLK		PF-EINT5
PF6	I/O				I2S3-MCLK		PF-EINT6

Table 8-16 PG Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PG0	I/O	SDC1-CLK					PG-EINT0
PG1	I/O	SDC1-CMD					PG-EINT1
PG2	I/O	SDC1-D0	PCIE0-PERSTN				PG-EINT2
PG3	I/O	SDC1-D1	PCIE0-WAKEN				PG-EINT3
PG4	I/O	SDC1-D2	PCIE0-CLKREQN				PG-EINT4
PG5	I/O	SDC1-D3					PG-EINT5
PG6	I/O	UART1-TX					PG-EINT6
PG7	I/O	UART1-RX					PG-EINT7
PG8	I/O	UART1-RTS					PG-EINT8
PG9	I/O	UART1-CTS					PG-EINT9
PG10	I/O		I2S1-MCLK				PG-EINT10
PG11	I/O		I2S1-BCLK				PG-EINT11
PG12	I/O		I2S1-LRCK				PG-EINT12
PG13	I/O		I2S1-DOUT0	I2S1-DIN1			PG-EINT13
PG14	I/O		I2S1-DIN0	I2S1-DOUT1			PG-EINT14

Table 8-17 PH Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PH0	I/O	TWI0-SCK			RGMII0-RXD1/RMII0-RXD1		PH-EINT0
PH1	I/O	TWI0-SDA			RGMII0-RXD0/RMII0-RXD0		PH-EINT1

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PH2	I/O	TWI1-SCK		I2S2-DIN3	RGMII0-RXCTL/RMII0-CRS-DV	I2S2-DOUT3	PH-EINT2
PH3	I/O	TWI1-SDA	IR-TX	I2S2-DIN2	RGMII0-CLKIN/RMII0-RXER	I2S2-DOUT2	PH-EINT3
PH4	I/O	UART3-TX	SPI1-CS0		RGMII0-TXD1/RMII0-TXD1		PH-EINT4
PH5	I/O	UART3-RX	SPI1-CLK	LEDC	RGMII0-TXD0/RMII0-TXD0		PH-EINT5
PH6	I/O	UART3-RTS	SPI1-MOSI	OWA-IN	RGMII0-TXCK/RMII0-TXCK		PH-EINT6
PH7	I/O	UART3-CTS	SPI1-MISO	OWA-OUT	RGMII0-TXCTL/RMII0-TXEN		PH-EINT7
PH8	I/O	DMIC-CLK	SPI2-CS0	I2S2-MCLK	I2S2-DIN2		PH-EINT8
PH9	I/O	DMIC-DATA0	SPI2-CLK	I2S2-BCLK	RGMII0-MDC		PH-EINT9
PH10	I/O	DMIC-DATA1	SPI2-MOSI	I2S2-LRCK	RGMII0-MDIO		PH-EINT10
PH11	I/O	DMIC-DATA2	SPI2-MISO	I2S2-DOUT0	I2S2-DIN1	PCIE0-PERSTN	PH-EINT11
PH12	I/O	DMIC-DATA3	TWI3-SCK	I2S2-DIN0	I2S2-DOUT1	PCIE0-WAKEN	PH-EINT12
PH13	I/O		TWI3-SDA	I2S3-MCLK	RGMII0-EPHY-25M		PH-EINT13
PH14	I/O			I2S3-BCLK	RGMII0-RXD3/RMII0-NULL		PH-EINT14
PH15	I/O			I2S3-LRCK	RGMII0-RXD2/RMII0-NULL		PH-EINT15
PH16	I/O		I2S3-DOUT0	I2S3-DIN1	RGMII0-RXCK/RMII0-NULL	CLK-FANOUT0	PH-EINT16
PH17	I/O		I2S3-DOUT1	I2S3-DIN0	RGMII0-TXD3/RMII0-NULL		PH-EINT17
PH18	I/O	IR-TX	I2S3-DOUT2	I2S3-DIN2	RGMII0-TXD2/RMII0-NULL		PH-EINT18
PH19	I/O	IR-RX	I2S3-DOUT3	I2S3-DIN3	LEDC	PCIE0-CLKREQN	PH-EINT19

Table 8-18 PK Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PK0	I/O	MCSIA-D0N					PK-EINT0
PK1	I/O	MCSIA-D0P					PK-EINT1
PK2	I/O	MCSIA-D1N					PK-EINT2
PK3	I/O	MCSIA-D1P					PK-EINT3
PK4	I/O	MCSIA-CKN	TWI2-SCK				PK-EINT4
PK5	I/O	MCSIA-CKP	TWI2-SDA				PK-EINT5
PK6	I/O	MCSIB-D0N					PK-EINT6
PK7	I/O	MCSIB-D0P					PK-EINT7
PK8	I/O	MCSIB-D1N					PK-EINT8
PK9	I/O	MCSIB-D1P					PK-EINT9
PK10	I/O	MCSIB-CKN	TWI3-SCK				PK-EINT10
PK11	I/O	MCSIB-CKP	TWI3-SDA				PK-EINT11
PK12	I/O	MCSIC-D0N	UART7-TX	TWI4-SCK	NCSI-PCLK		PK-EINT12
PK13	I/O	MCSIC-D0P	UART7-RX	TWI4-SDA	NCSI-MCLK		PK-EINT13
PK14	I/O	MCSIC-D1N	UART7-RTS	UART5-RTS	NCSI-HSYNC		PK-EINT14
PK15	I/O	MCSIC-D1P	UART7-CTS	UART5-CTS	NCSI-VSYNC		PK-EINT15
PK16	I/O	MCSIC-CKN	TWI5-SCK	UART5-TX	NCSI-D0		PK-EINT16
PK17	I/O	MCSIC-CKP	TWI5-SDA	UART5-RX	NCSI-D1		PK-EINT17
PK18	I/O	MCSID-D0N	MCSI0-MCLK	UART6-TX	NCSI-D2		PK-EINT18
PK19	I/O	MCSID-D0P	TWI2-SCK	UART6-RX	NCSI-D3		PK-EINT19
PK20	I/O	MCSID-D1N	TWI2-SDA	UART6-RTS	NCSI-D4		PK-EINT20
PK21	I/O	MCSID-D1P	MCSI1-MCLK	UART6-CTS	NCSI-D5		PK-EINT21
PK22	I/O	MCSID-CKN	TWI3-SCK	PWM6	NCSI-D6		PK-EINT22
PK23	I/O	MCSID-CKP	TWI3-SDA	PWM7	NCSI-D7		PK-EINT23

Table 8-19 PL Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PL0	I/O	S-TWI0-SCK					PL-EINT0
PL1	I/O	S-TWI0-SDA					PL-EINT1
PL2	I/O	S-UART0-TX	S-UART1-TX	S-PWM2			PL-EINT2
PL3	I/O	S-UART0-RX	S-UART1-RX	S-PWM3			PL-EINT3
PL4	I/O	S-JTAG-MS		S-PWM4	S-I2S0-BCLK		PL-EINT4
PL5	I/O	S-JTAG-CK		S-PWM5	S-I2S0-LRCK	S-DMIC-DATA3	PL-EINT5
PL6	I/O	S-JTAG-DO	S-PWM6	S-I2S0-DIN1	S-I2S0-DOUT0	S-DMIC-DATA2	PL-EINT6
PL7	I/O	S-JTAG-DI	S-PWM7	S-I2S0-DOUT1	S-I2S0-DIN0	S-DMIC-DATA1	PL-EINT7
PL8	I/O	S-TWI1-SCK		S-RJTAG-MS	S-I2S0-MCLK	S-DMIC-DATA0	PL-EINT8
PL9	I/O	S-TWI1-SDA		S-RJTAG-CK	S-PWM1	S-DMIC-CLK	PL-EINT9
PL10	I/O	S-PWM0		S-RJTAG-DO	S-DMIC-DATA0	S-SPI0-CS0	PL-EINT10
PL11	I/O	S-IR-RX		S-RJTAG-DI	S-DMIC-DATA1	S-SPI0-CLK	PL-EINT11
PL12	I/O	S-TWI2-SCK	S-PWM8	S-UART0-TX	S-DMIC-DATA2	S-SPI0-MOSI	PL-EINT12
PL13	I/O	S-TWI2-SDA	S-PWM9	S-UART0-RX	S-DMIC-DATA3	S-SPI0-MISO	PL-EINT13

Table 8-20 PM Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PM0	I/O	S-UART0-TX	S-UART1-TX	S-PWM2			PM-EINT0
PM1	I/O	S-UART0-RX	S-UART1-RX	S-PWM3			PM-EINT1
PM2	I/O	S-TWI1-SCK	S-RJTAG-MS	S-PWM6			PM-EINT2
PM3	I/O	S-TWI1-SDA	S-RJTAG-CK	S-PWM7			PM-EINT3
PM4	I/O	S-PWM8	S-RJTAG-DO	S-TWI2-SCK			PM-EINT4
PM5	I/O	S-IR-RX	S-RJTAG-DI	S-TWI2-SDA	S-PWM9		PM-EINT5

8.5.3.3 Port Function

The Port Controller supports 10 GPIOs, every GPIO can configure as Input, Output, Function Peripheral, IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 8-21 Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/: non-configure, configuration is invalid

Y: configure

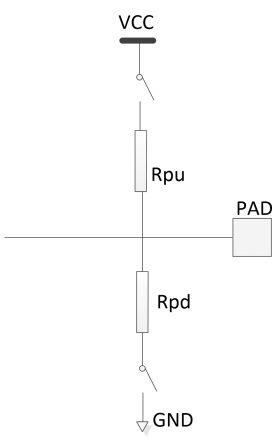
X: Select configuration according to the actual situation

N: Forbid to configure

8.5.3.4 Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

Figure 8-22 Pull up/down Logic



High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, the software configures the switch on Rpu and Rpd as off, and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by resistance, the resistance has a current-limiting function. When pulling up, the switch on Rpu is conducted by software configuration, the IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is conducted by software configuration, the IO is pulled down to GND by Rpd.

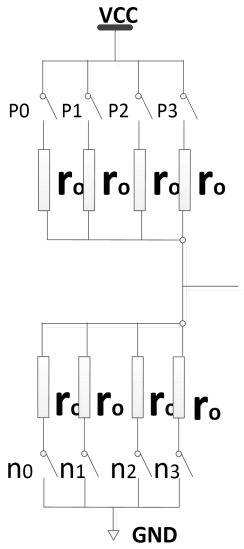
The pull-up/down of each IO is weak pull-up/down.

The setting of pull-down, pull-up, high-impedance is decided by the external circuit.

8.5.3.5 Buffer Strength

Each IO can be set as different buffer strength. The IO buffer diagram is as follows.

Figure 8-23 IO Buffer Strength Diagram



When output high level, the n0, n1, n2, n3 of NMOS is off, the p0, p1, p2, p3 of PMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the p0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the p0, p1, and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, the p0, p1, p2, and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0, p1, p2, p3 of PMOS is off, the n0, n1, n2, n3 of NMOS is on. When the buffer strength is set to 0 (buffer strength is weakest), only the n0 is on, the output impedance is maximum, the impedance value is r0. When the buffer strength is set to 1, only the n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When the buffer strength is 2, only the n0, n1, and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When the buffer strength is 3, the n0, n1, n2, and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between the output driver circuit and the port is unconnected, the driver configuration is invalid.

8.5.3.6 Interrupt

Each group IO has an independent interrupt number. The IO within-group uses one interrupt number when one IO generates interrupt, the GPIO pins sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

The interrupt trigger of GPIO supports the following trigger types.

- Positive Edge: When a low level changes to a high level, the interrupt will generate. No matter how long a high level keeps, the interrupt generates only once.
- Negative Edge: When a high level changes to a low level, the interrupt will generate. No matter how long a low level keeps, the interrupt generates only once.
- High Level: Just keep a high level and the interrupt will always generate.
- Low Level: Just keep a low level and the interrupt will always generate.
- Double Edge: Positive and negative edge.

External Interrupt Configure Register is used to configure the trigger type.

The GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using a lower sample clock, to reach the debounce effect because the dither frequency of the signal is higher than the sample frequency.

Set the sample clock source by PIO_INT_CLK_SELECT and the prescale factor by DEB_CLK_PRE_SCALE.

8.5.4 Programming Guidelines

8.5.4.1 Disable

The steps to disable I/O pins are as follows:

Step 1 Write FFFF to the Px_SELECT bit of the Px_CFG register to disable the I/O pins.

Step 2 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins. In this case, the default status of I/O pins is logic-high.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins. In this case, the default status of I/O pins is logic-low.

8.5.4.2 Input

The steps to configure I/O pins as inputs are as follows:

Step 1 Write 0000 to the Px_SELECT bit of the Px_CFG register to enable input function.

Step 2 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins.

Step 3 Configure the Px_DAT bit of the Px_DAT register to read the pin status.

- If the external input is driven, the value of the Px_DAT bit is the external input value.
- If the external input is not driven, the value of the Px_DAT bit is 1 when the I/O pins are pulled up and is 0 when pins are pulled down.

8.5.4.3 Output

The steps to configure I/O pins as outputs are as follows:

Step 1 Write 0001 to the Px_SELECT bit of the Px_CFG register to enable outputput function.

Step 2 If it is needed to set the buffer strength of the I/O pins, configure the Px_DRV bit of the Px_DRV register.

- When the Px_DRV bit is configured as 00, the buffer strength is the weakest.
- When the Px_DRV bit is configured as 11, the buffer strength is the strongest.
- The default value of the Px_DRV register is 01.

Step 3 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins.

Step 4 Configure the Px_DAT bit of the Px_DAT register to output 1 or 0 to the I/O pins.

- If output function is enabled, the pin status is the same as the corresponding bit.
- If output function is disabled, the value of the Px_DAT bit is 1 when the I/O pins are pulled up and is 0 when pins are pulled down.

8.5.4.4 Interrupt

The steps to configure I/O pins as interrupt pins are as follows:

Step 1 Write 1110 to the Px_SELECT bit of the Px_CFG register to enable interrupt function.

Step 2 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins. in this case, if external pins are not driven, the input level is high by default.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins. In this case, if external pins are not driven, the input level is low by default.

Step 3 Configure the EINTx_CFG bit of Px_INT_CFG register to set the interrupt generation mode.

Step 4 Configure Px_INT_DEB regsiter to set debounce parameters including sample clock source and prescale factor.

Step 5 Write 1 to the EINTx_STATUS bit of the Px_INT_STA register to clear IRQ pending.

Step 6 Write 1 to the EINTx_CTL bit of the Px_INT_CTL register to enable interrupt.

Step 7 After an interrupt is processed, repeat Step5 to clrear IRQ pending and wait for next interrupt operation.

Step 8 Write 0 to the EINTx_CTL bit of the Px_INT_CTL register to disable interrupt function.

8.5.4.5 Multi Function

The steps to configure I/O pins as for function multiplexing are as follows:

Step 1 Configrue the Px_SELECT bit of the Px_CFG register to select the funciton needed.

Step 2 Configure the Px_DRV bit of the Px_DRV register to set buffer strength depending on the characteristic of the selected funciton.

Step 3 If it is needed to control whether the I/O pins are pulled up or pulled down, configure Px_PULL register.

- Write 2'b01 to the Px_PULL bit of Px_PULL register to pull up the I/O pins.
- Write 2'b10 to the Px_PULL bit of Px_PULL register to pull down the I/O pins.
- If external pins are driven, the pin status is the same as the corresponding bit.
- If external pins are not driven, the value of the Px_DAT bit is 1 when the I/O pins are pulled up and 0 when pins are pulled down.

8.5.4.6 Power Configuation

Configuring Group Power Volatge

A523 only supports to set group power voltage in PF ports, which is able to be set as 3.3 V or 1.8V by configuring GPIO_POW_VAL_SET_CTL register. The group power voltage in other ports is un configurable and depended on the peripheral circuit.

Configuring Group Withstand Voltage

Configuring group withstand voltage intends to ensure that the internal withstand circuit voltage is consistent with group voltage. There are two modes, adaptive mode and manual mode, for users. In adaptive mode, the interl withstand circuit will adjust group withstand mode automatically depending on the detected GPIO voltage. The default mode is manual mode and it is recommended to choose manual mode in A523.

The following steps describe how to configure group withstand voltage.

- **Adptive Mode**

The following table shows the configuration for registers in adptive mode.

Bit	Register
Px_PWR_MOD_SEL bit = 0	GPIO_POW_MOD_SEL
VCC_Px_WS_VOL_MOD_SEL bit = 0	GPIO_POW_MS_CTL

- **Manual Mode (Recommended)**

Step 1 Before using GPIO, read GPIO_POW_VAL register to obtain current group voltage.

- If the current power supply is 1.8V, continue from Step2.
- If the current power supply is 3.3V, continue from Step4.

Step 2 Read the PB_PWR_VAL bit (bit [1]) of GPIO_POW_VAL register to obtain current group voltage.

Step 3 Configure withstand voltage.

The following table shows the corresponding withstand voltage for each group voltage and corresponding configuration register.

Group Voltage	Withstand Voltage	Bit	Register
1.8V	1.8V	Px_PWR_MOD_SEL bit = 0	GPIO_POW_MOD_SEL
		VCC_Px_WS_VOL_MOD_SEL bit = 1	GPIO_POW_MS_CTL
2.5V	3.3V	Px_PWR_MOD_SEL bit = 1	GPIO_POW_MOD_SEL
3.3V	3.3V	Px_PWR_MOD_SEL bit = 1	GPIO_POW_MOD_SEL

Step 4 After the I/O pins are power-on, repeat Step2 and Step3 to configure withstand voltage according to the actual group voltage.

Step 5 When adjusting group voltage during usage, follow the steps blow to configure withstand voltage.

- If the group voltage is to be switched from 1.8 V to 3.3 V, configure withstand voltage to 3.3 V before switching.
- If the group voltage is to be switched from 3.3 V to 1.8 V, configure withstand voltage to 1.8 V after switching.

8.5.5 Register List

There are two groups of registers for GPIO.

Module Name	Base Address
GPIO	0x0200 0000
S_GPIO	0x0702 2000

8.5.5.1 GPIO Register List

Module Name	Base Address
GPIO	0x0200 0000

Register Name	Offset	Description
PB_CFG0	0x0030	PB Configure Register 0
PB_CFG1	0x0034	PB Configure Register 1
PB_CFG2	0x0038	PB Configure Register 2
PB_CFG3	0x003C	PB Configure Register 3
PB_DAT	0x0040	PB Data Register
PB_DRV0	0x0044	PB Multi_Driving Register 0
PB_DRV1	0x0048	PB Multi_Driving Register 1
PB_DRV2	0x004C	PB Multi_Driving Register 2
PB_DRV3	0x0050	PB Multi_Driving Register 3
PB_PUL0	0x0054	PB Pull Register 0
PB_PUL1	0x0058	PB Pull Register 1
PC_CFG0	0x0060	PC Configure Register 0
PC_CFG1	0x0064	PC Configure Register 1
PC_CFG2	0x0068	PC Configure Register 2
PC_CFG3	0x006C	PC Configure Register 3
PC_DAT	0x0070	PC Data Register
PC_DRV0	0x0074	PC Multi_Driving Register 0
PC_DRV1	0x0078	PC Multi_Driving Register 1
PC_DRV2	0x007C	PC Multi_Driving Register 2
PC_DRV3	0x0080	PC Multi_Driving Register 3
PC_PUL0	0x0084	PC Pull Register 0
PC_PUL1	0x0088	PC Pull Register 1
PD_CFG0	0x0090	PD Configure Register 0
PD_CFG1	0x0094	PD Configure Register 1
PD_CFG2	0x0098	PD Configure Register 2
PD_CFG3	0x009C	PD Configure Register 3
PD_DAT	0x00A0	PD Data Register
PD_DRV0	0x00A4	PD Multi_Driving Register 0
PD_DRV1	0x00A8	PD Multi_Driving Register 1
PD_DRV2	0x00AC	PD Multi_Driving Register 2
PD_DRV3	0x00B0	PD Multi_Driving Register 3
PD_PUL0	0x00B4	PD Pull Register 0
PD_PUL1	0x00B8	PD Pull Register 1
PE_CFG0	0x00C0	PE Configure Register 0
PE_CFG1	0x00C4	PE Configure Register 1
PE_CFG2	0x00C8	PE Configure Register 2

Register Name	Offset	Description
PE_CFG3	0x00CC	PE Configure Register 3
PE_DAT	0x00D0	PE Data Register
PE_DRV0	0x00D4	PE Multi_Driving Register 0
PE_DRV1	0x00D8	PE Multi_Driving Register 1
PE_DRV2	0x00DC	PE Multi_Driving Register 2
PE_DRV3	0x00E0	PE Multi_Driving Register 3
PE_PUL0	0x00E4	PE Pull Register 0
PE_PUL1	0x00E8	PE Pull Register 1
PF_CFG0	0x00F0	PF Configure Register 0
PF_CFG1	0x00F4	PF Configure Register 1
PF_CFG2	0x00F8	PF Configure Register 2
PF_CFG3	0x00FC	PF Configure Register 3
PF_DAT	0x0100	PF Data Register
PF_DRV0	0x0104	PF Multi_Driving Register 0
PF_DRV1	0x0108	PF Multi_Driving Register 1
PF_DRV2	0x010C	PF Multi_Driving Register 2
PF_DRV3	0x0110	PF Multi_Driving Register 3
PF_PUL0	0x0114	PF Pull Register 0
PF_PUL1	0x0118	PF Pull Register 1
PG_CFG0	0x0120	PG Configure Register 0
PG_CFG1	0x0124	PG Configure Register 1
PG_CFG2	0x0128	PG Configure Register 2
PG_CFG3	0x012C	PG Configure Register 3
PG_DAT	0x0130	PG Data Register
PG_DRV0	0x0134	PG Multi_Driving Register 0
PG_DRV1	0x0138	PG Multi_Driving Register 1
PG_DRV2	0x013C	PG Multi_Driving Register 2
PG_DRV3	0x0140	PG Multi_Driving Register 3
PG_PUL0	0x0144	PG Pull Register 0
PG_PUL1	0x0148	PG Pull Register 1
PH_CFG0	0x0150	PH Configure Register 0
PH_CFG1	0x0154	PH Configure Register 1
PH_CFG2	0x0158	PH Configure Register 2
PH_CFG3	0x015C	PH Configure Register 3
PH_DAT	0x0160	PH Data Register
PH_DRV0	0x0164	PH Multi_Driving Register 0
PH_DRV1	0x0168	PH Multi_Driving Register 1
PH_DRV2	0x016C	PH Multi_Driving Register 2
PH_DRV3	0x0170	PH Multi_Driving Register 3
PH_PUL0	0x0174	PH Pull Register 0
PH_PUL1	0x0178	PH Pull Register 1
PK_CFG0	0x0500	PK Configure Register 0

Register Name	Offset	Description
PK_CFG1	0x0504	PK Configure Register 1
PK_CFG2	0x0508	PK Configure Register 2
PK_CFG3	0x050C	PK Configure Register 3
PK_DAT	0x0510	PK Data Register
PK_DRV0	0x0514	PK Multi_Driving Register 0
PK_DRV1	0x0518	PK Multi_Driving Register 1
PK_DRV2	0x051C	PK Multi_Driving Register 2
PK_DRV3	0x0520	PK Multi_Driving Register 3
PK_PUL0	0x0524	PK Pull Register 0
PK_PUL1	0x0528	PK Pull Register 1
PB_INT_CFG0	0x0220	PB External Interrupt Configure Register 0
PB_INT_CFG1	0x0224	PB External Interrupt Configure Register 1
PB_INT_CFG2	0x0228	PB External Interrupt Configure Register 2
PB_INT_CFG3	0x022C	PB External Interrupt Configure Register 3
PB_INT_CTL	0x0230	PB External Interrupt Control Register
PB_INT_STA	0x0234	PB External Interrupt Status Register
PB_INT_DEB	0x0238	PB External Debounce Configure Register
PC_INT_CFG0	0x0240	PC External Interrupt Configure Register 0
PC_INT_CFG1	0x0244	PC External Interrupt Configure Register 1
PC_INT_CFG2	0x0248	PC External Interrupt Configure Register 2
PC_INT_CFG3	0x024C	PC External Interrupt Configure Register 3
PC_INT_CTL	0x0250	PC External Interrupt Control Register
PC_INT_STA	0x0254	PC External Interrupt Status Register
PC_INT_DEB	0x0258	PC External Debounce Configure Register
PD_INT_CFG0	0x0260	PD External Interrupt Configure Register 0
PD_INT_CFG1	0x0264	PD External Interrupt Configure Register 1
PD_INT_CFG2	0x0268	PD External Interrupt Configure Register 2
PD_INT_CFG3	0x026C	PD External Interrupt Configure Register 3
PD_INT_CTL	0x0270	PD External Interrupt Control Register
PD_INT_STA	0x0274	PD External Interrupt Status Register
PD_INT_DEB	0x0278	PD External Debounce Configure Register
PE_INT_CFG0	0x0280	PE External Interrupt Configure Register 0
PE_INT_CFG1	0x0284	PE External Interrupt Configure Register 1
PE_INT_CFG2	0x0288	PE External Interrupt Configure Register 2
PE_INT_CFG3	0x028C	PE External Interrupt Configure Register 3
PE_INT_CTL	0x0290	PE External Interrupt Control Register
PE_INT_STA	0x0294	PE External Interrupt Status Register
PE_INT_DEB	0x0298	PE External Debounce Configure Register
PF_INT_CFG0	0x02A0	PF External Interrupt Configure Register 0
PF_INT_CFG1	0x02A4	PF External Interrupt Configure Register 1
PF_INT_CFG2	0x02A8	PF External Interrupt Configure Register 2
PF_INT_CFG3	0x02AC	PF External Interrupt Configure Register 3

Register Name	Offset	Description
PF_INT_CTL	0x02B0	PF External Interrupt Control Register
PF_INT_STA	0x02B4	PF External Interrupt Status Register
PF_INT_DEB	0x02B8	PF External Debounce Configure Register
PG_INT_CFG0	0x02C0	PG External Interrupt Configure Register 0
PG_INT_CFG1	0x02C4	PG External Interrupt Configure Register 1
PG_INT_CFG2	0x02C8	PG External Interrupt Configure Register 2
PG_INT_CFG3	0x02CC	PG External Interrupt Configure Register 3
PG_INT_CTL	0x02D0	PG External Interrupt Control Register
PG_INT_STA	0x02D4	PG External Interrupt Status Register
PG_INT_DEB	0x02D8	PG External Debounce Configure Register
PH_INT_CFG0	0x02E0	PH External Interrupt Configure Register 0
PH_INT_CFG1	0x02E4	PH External Interrupt Configure Register 1
PH_INT_CFG2	0x02E8	PH External Interrupt Configure Register 2
PH_INT_CFG3	0x02EC	PH External Interrupt Configure Register 3
PH_INT_CTL	0x02F0	PH External Interrupt Control Register
PH_INT_STA	0x02F4	PH External Interrupt Status Register
PH_INT_DEB	0x02F8	PH External Debounce Configure Register
PK_INT_CFG0	0x0340	PK External Interrupt Configure Register 0
PK_INT_CFG1	0x0344	PK External Interrupt Configure Register 1
PK_INT_CFG2	0x0348	PK External Interrupt Configure Register 2
PK_INT_CFG3	0x034C	PK External Interrupt Configure Register 3
PK_INT_CTL	0x0350	PK External Interrupt Control Register
PK_INT_STA	0x0354	PK External Interrupt Status Register
PK_INT_DEB	0x0358	PK External Debounce Configure Register
GPIO_POW_MOD_SEL	0x0380	GPIO Group Withstand Voltage Mode Select Register
GPIO_POW_MS_CTL	0x0384	GPIO Group Withstand Voltage Mode Select Control Register
GPIO_POW_VAL	0x0388	GPIO Group Power Value Register
GPIO_POW_VAL_SET_CTL	0x0390	GPIO Group Power Voltage Select Control Register

8.5.5.2 S_GPIO Register List

Module Name	Base Address
S_GPIO	0x0702 2000

Register Name	Offset	Description
PL_CFG0	0x0000	PL Configure Register 0
PL_CFG1	0x0004	PL Configure Register 1
PL_CFG2	0x0008	PL Configure Register 2
PL_CFG3	0x000C	PL Configure Register 3

Register Name	Offset	Description
PL_DAT	0x0010	PL Data Register
PL_DRV0	0x0014	PL Multi_Driving Register 0
PL_DRV1	0x0018	PL Multi_Driving Register 1
PL_DRV2	0x001C	PL Multi_Driving Register 2
PL_DRV3	0x0020	PL Multi_Driving Register 3
PL_PUL0	0x0024	PL Pull Register 0
PL_PUL1	0x0028	PL Pull Register 1
PM_CFG0	0x0030	PM Configure Register 0
PM_CFG1	0x0034	PM Configure Register 1
PM_CFG2	0x0038	PM Configure Register 2
PM_CFG3	0x003C	PM Configure Register 3
PM_DAT	0x0040	PM Data Register
PM_DRV0	0x0044	PM Multi_Driving Register 0
PM_DRV1	0x0048	PM Multi_Driving Register 1
PM_DRV2	0x004C	PM Multi_Driving Register 2
PM_DRV3	0x0050	PM Multi_Driving Register 3
PM_PUL0	0x0054	PM Pull Register 0
PM_PUL1	0x0058	PM Pull Register 1
PL_INT_CFG0	0x0200	PL External Interrupt Configure Register 0
PL_INT_CFG1	0x0204	PL External Interrupt Configure Register 1
PL_INT_CFG2	0x0208	PL External Interrupt Configure Register 2
PL_INT_CFG3	0x020C	PL External Interrupt Configure Register 3
PL_INT_CTL	0x0210	PL External Interrupt Control Register
PL_INT_STA	0x0214	PL External Interrupt Status Register
PL_INT_DEB	0x0218	PL External Debounce Configure Register
PM_INT_CFG0	0x0220	PM External Interrupt Configure Register 0
PM_INT_CFG1	0x0224	PM External Interrupt Configure Register 1
PM_INT_CFG2	0x0228	PM External Interrupt Configure Register 2
PM_INT_CFG3	0x022C	PM External Interrupt Configure Register 3
PM_INT_CTL	0x0230	PM External Interrupt Control Register
PM_INT_STA	0x0234	PM External Interrupt Status Register
PM_INT_DEB	0x0238	PM External Debounce Configure Register
GPIO_POW_MOD_SEL	0x0340	GPIO Group Withstand Voltage Mode Select Register
GPIO_POW_MS_CTL	0x0344	GPIO Group Withstand Voltage Mode Select Control Register
GPIO_POW_VAL	0x0348	GPIO Group Power Value Register
GPIO_POW_VAL_SET_CTL	0x0350	GPIO Group Power Voltage Select Control Register

8.5.6 GPIO Register Description

8.5.6.1 0x0030 PB Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0030			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PB7_SELECT PB7 Select 0000: Input 0001: Output 0010: OWA-IN 0011: I2S0-DOUT0 0100: I2S0-DIN1 0101: LCD0-D16 0110: PWM11 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT7 1111: IO Disable
27:24	R/W	0xF	PB6_SELECT PB6 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S0-LRCK 0100: Reserved 0101: PWM10 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT6 1111: IO Disable
23:20	R/W	0xF	PB5_SELECT PB5 Select 0000: Input 0001: Output 0010: TWI1-SDA 0011: I2S0-BCLK 0100: Reserved 0101: PWM9 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PB-EINT5 1111: IO Disable
19:16	R/W	0xF	PB4_SELECT PB4 Select 0000: Input 0001: Output 0010: TWI1-SCK 0011: I2S0-MCLK 0100: Reserved 0101: PWM8 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved

Offset: 0x0030			Register Name: PB_CFG0	
Bit	Read/Write	Default/Hex	Description	
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PB-EINT4	1111: IO Disable
15:12	R/W	0xF	PB3_SELECT PB3 Select 0000: Input 0010: UART2-CTS 0100: JTAG-DI 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT3	 0001: Output 0011: SPI2-MISO 0101: LCD0-D9 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PB2_SELECT PB2 Select 0000: Input 0010: UART2-RTS 0100: JTAG-DO 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT2	 0001: Output 0011: SPI2-MOSI 0101: LCD0-D8 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PB1_SELECT PB1 Select 0000: Input 0010: UART2-RX 0100: JTAG-CK 0110: PWM7 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT1	 0001: Output 0011: SPI2-CLK 0101: LCD0-D1 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PB0_SELECT PB0 Select 0000: Input 0010: UART2-TX 0100: JTAG-MS 0110: PWM6 1000: Reserved 1010: Reserved	 0001: Output 0011: SPI2-CS 0101: LCD0-D0 0111: Reserved 1001: Reserved 1011: Reserved

Offset: 0x0030			Register Name: PB_CFG0	
Bit	Read/Write	Default/Hex	Description	
			1100: Reserved 1110: PB-EINT0	1101: Reserved 1111: IO Disable

8.5.6.2 0x0034 PB Configure Register 1 (Default Value: 0x0FFF_FFFF)

Offset: 0x0034			Register Name: PB_CFG1	
Bit	Read/Write	Default/Hex	Description	
31:28	/	/	/	
27:24	R/W	0xF	PB14_SELECT PB14 Select 0000: Input 0010: TWI4-SDA 0100: SPI1-MISO 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT14	 0001: Output 0011: UART7-RX 0101: PWM5 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
23:20	R/W	0xF	PB13_SELECT PB13 Select 0000: Input 0010: TWI4-SCK 0100: SPI1-MOSI 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT13	 0001: Output 0011: UART7-TX 0101: PWM4 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PB12_SELECT PB12 Select 0000: Input 0010: TWI5-SDA 0100: SPI1-CLK 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT12	 0001: Output 0011: UART7-CTS 0101: PWM3 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PB11_SELECT PB11 Select 0000: Input	 0001: Output

Offset: 0x0034			Register Name: PB_CFG1	
Bit	Read/Write	Default/Hex	Description	
			0010: TWI5-SCK 0100: SPI1-CS0 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT11	0011: UART7-RTS 0101: PWM2 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PB10_SELECT PB10 Select 0000: Input 0010: UART0-RX 0100: PWM1 0110: I2S0-DOUT3 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT10	 0001: Output 0011: TWI0-SDA 0101: I2S0-DIN3 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PB9_SELECT PB9 Select 0000: Input 0010: UART0-TX 0100: Reserved 0110: I2S0-DOUT2 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT9	 0001: Output 0011: TWI0-SCK 0101: I2S0-DIN2 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PB8_SELECT PB8 Select 0000: Input 0010: OWA-OUT 0100: I2S0-DOUT1 0110: PWM0 1000: Reserved 1010: Reserved 1100: Reserved 1110: PB-EINT8	 0001: Output 0011: I2S0-DIN0 0101: LCD0-D17 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.3 0x0038 PB Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0038	Register Name: PB_CFG2

Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.4 0x003C PB Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PB_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.5 0x0040 PB Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PB_DAT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	0	PB_DAT PB Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.6 0x0044 PB Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0044			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PB7_DRV PB7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PB6_DRV PB6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PB5_DRV PB5 Multi_Driving Select

Offset: 0x0044			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
			00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PB4_DRV PB4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PB3_DRV PB3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PB2_DRV PB2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PB1_DRV PB1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PB0_DRV PB0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.7 0x0048 PB Multi_Driving Register 1 (Default Value: 0x0111_1111)

Offset: 0x0048			Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PB14_DRV PB14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PB13_DRV PB13 Multi_Driving Select

Offset: 0x0048			Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
			00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PB12_DRV PB12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PB11_DRV PB11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PB10_DRV PB10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PB9_DRV PB9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PB8_DRV PB8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.8 0x004C PB Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: PB_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.9 0x0050 PB Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: PB_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.10 0x0054 PB Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PB14_PULL PB14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PB13_PULL PB13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PB12_PULL PB12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PB11_PULL PB11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PB10_PULL PB10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PB9_PULL PB9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PB8_PULL PB8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PB7_PULL PB7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PB6_PULL PB6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PB5_PULL PB5 Pull_up or down Select

Offset: 0x0054			Register Name: PB_PUL0
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PB4_PULL PB4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PB3_PULL PB3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PB2_PULL PB2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PB1_PULL PB1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PB0_PULL PB0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.11 0x0058 PB Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PB_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.12 0x0060 PC Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0060			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PC7_SELECT PC7 Select 0000: Input 0001: Output 0010: NAND-RB1 0011: Reserved 0100: SPI0-CS1 0101: SPIF-DQS 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved

Offset: 0x0060			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
			1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT7 1111: IO Disable
27:24	R/W	0xF	PC6_SELECT PC6 Select 0000: Input 0001: Output 0010: NAND-RB0 0011: SDC2-CMD 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT6 1111: IO Disable
23:20	R/W	0xF	PC5_SELECT PC5 Select 0000: Input 0001: Output 0010: NAND-RE 0011: SDC2-CLK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT5 1111: IO Disable
19:16	R/W	0xF	PC4_SELECT PC4 Select 0000: Input 0001: Output 0010: NAND-CE0 0011: Reserved 0100: SPI0-MISO 0101: SPIF-MISO 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT4 1111: IO Disable
15:12	R/W	0xF	PC3_SELECT PC3 Select 0000: Input 0001: Output 0010: NAND-CE1 0011: Reserved 0100: SPI0-CS0 0101: SPIF-CS0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved

Offset: 0x0060			Register Name: PC_CFG0
Bit	Read/Write	Default/Hex	Description
			1100: Reserved 1101: Reserved 1110: PC-EINT3 1111: IO Disable
11:8	R/W	0xF	PC2_SELECT PC2 Select 0000: Input 0001: Output 0010: NAND-CLE 0011: Reserved 0100: SPI0-MOSI 0101: SPIF-MOSI 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT2 1111: IO Disable
7:4	R/W	0xF	PC1_SELECT PC1 Select 0000: Input 0001: Output 0010: NAND-ALE 0011: SDC2-RST 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT1 1111: IO Disable
3:0	R/W	0xF	PC0_SELECT PC0 Select 0000: Input 0001: Output 0010: NAND-WE 0011: SDC2-DS 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT0 1111: IO Disable

8.5.6.13 0x0064 PC Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0064			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PC15_SELECT PC15 Select 0000: Input 0001: Output 0010: NAND-DQ1 0011: SDC2-D2

Offset: 0x0064			Register Name: PC_CFG1	
Bit	Read/Write	Default/Hex	Description	
			0100: SPI0-WP	0101: SPIF-WP
			0110: Reserved	0111: Reserved
			1000: Reserved	1001: Reserved
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PC-EINT15	1111: IO Disable
27:24	R/W	0xF	PC14_SELECT PC14 Select 0000: Input 0010: NAND-DQ2 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC-EINT14	 0001: Output 0011: SDC2-D6 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
23:20	R/W	0xF	PC13_SELECT PC13 Select 0000: Input 0010: NAND-DQ3 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC-EINT13	 0001: Output 0011: SDC2-D1 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PC12_SELECT PC12 Select 0000: Input 0010: NAND-DQS 0100: SPI0-CLK 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PC-EINT12	 0001: Output 0011: Reserved 0101: SPIF-CLK 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PC11_SELECT PC11 Select 0000: Input 0010: NAND-DQ4 0100: Reserved	 0001: Output 0011: SDC2-D5 0101: SPIF-D4

Offset: 0x0064			Register Name: PC_CFG1
Bit	Read/Write	Default/Hex	Description
			0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT11 1111: IO Disable
11:8	R/W	0xF	PC10_SELECT PC10 Select 0000: Input 0001: Output 0010: NAND-DQ5 0011: SDC2-D0 0100: Reserved 0101: SPIF-D5 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT10 1111: IO Disable
7:4	R/W	0xF	PC9_SELECT PC9 Select 0000: Input 0001: Output 0010: NAND-DQ6 0011: SDC2-D4 0100: Reserved 0101: SPIF-D6 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT9 1111: IO Disable
3:0	R/W	0xF	PC8_SELECT PC8 Select 0000: Input 0001: Output 0010: NAND-DQ7 0011: SDC2-D3 0100: Reserved 0101: SPIF-D7 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT8 1111: IO Disable

8.5.6.14 0x0068 PC Configure Register 2 (Default Value: 0x0000_000F)

Offset: 0x0068			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/

Offset: 0x0068			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0xF	PC16_SELECT PC16 Select 0000: Input 0001: Output 0010: NAND-DQ0 0011: SDC2-D7 0100: SPI0-HOLD 0101: SPIF-HOLD 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PC-EINT16 1111: IO Disable

8.5.6.15 0x006C PC Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: PC_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.16 0x0070 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: PC_DAT
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:0	R/W	0	PC_DAT PC Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.17 0x0074 PC Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0074			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PC7_DRV PC7 Multi_Driving Select

Offset: 0x0074			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
			00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PC6_DRV PC6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PC5_DRV PC5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC4_DRV PC4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC3_DRV PC3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC2_DRV PC2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC1_DRV PC1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PC0_DRV PC0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.18 0x0078 PC Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0078	Register Name: PC_DRV1

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PC15_DRV PC15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PC14_DRV PC14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PC13_DRV PC13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PC12_DRV PC12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PC11_DRV PC11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PC10_DRV PC10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PC9_DRV PC9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PC8_DRV PC8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.19 0x007C PC Multi_Driving Register 2 (Default Value: 0x0000_0001)

Offset: 0x007C			Register Name: PC_DRV2
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	PC16_DRV PC16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.20 0x0080 PC Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: PC_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.21 0x0084 PC Pull Register 0 (Default Value: 0x0000_5140)

Offset: 0x0084			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PC15_PULL PC15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PC14_PULL PC14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PC13_PULL PC13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PC12_PULL PC12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PC11_PULL PC11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull_up or down Select

Offset: 0x0084			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x1	PC7_PULL PC7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x1	PC6_PULL PC6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PC5_PULL PC5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x1	PC4_PULL PC4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PC2_PULL PC2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up

Offset: 0x0084			Register Name: PC_PUL0
Bit	Read/Write	Default/Hex	Description
			10: Pull_down 11: Reserved

8.5.6.22 0x0088 PC Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PC_PUL1
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	PC16_PULL PC16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.23 0x0090 PD Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0090			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PD7_SELECT PD7 Select 0000: Input 0001: Output 0010: LCD0-D11 0011: LVDS0-CKN 0100: DSI0-D2N 0101: PWM7 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT7 1111: IO Disable
27:24	R/W	0xF	PD6_SELECT PD6 Select 0000: Input 0001: Output 0010: LCD0-D10 0011: LVDS0-CKP 0100: DSI0-D2P 0101: PWM6 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT6 1111: IO Disable
23:20	R/W	0xF	PD5_SELECT PD5 Select 0000: Input 0001: Output 0010: LCD0-D7 0011: LVDS0-D2N

Offset: 0x0090			Register Name: PD_CFG0	
Bit	Read/Write	Default/Hex	Description	
			0100: DSI0-CKN 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT5	0101: PWM5 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PD4_SELECT PD4 Select 0000: Input 0010: LCD0-D6 0100: DSI0-CKP 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT4	 0001: Output 0011: LVDS0-D2P 0101: PWM4 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PD3_SELECT PD3 Select 0000: Input 0010: LCD0-D5 0100: DSI0-D1N 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT3	 0001: Output 0011: LVDS0-D1N 0101: PWM3 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PD2_SELECT PD2 Select 0000: Input 0010: LCD0-D4 0100: DSI0-D1P 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT2	 0001: Output 0011: LVDS0-D1P 0101: PWM2 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PD1_SELECT PD1 Select 0000: Input 0010: LCD0-D3 0100: DSI0-D0N	 0001: Output 0011: LVDS0-D0N 0101: PWM1

Offset: 0x0090			Register Name: PD_CFG0	
Bit	Read/Write	Default/Hex	Description	
			0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT1	0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PD0_SELECT PD0 Select 0000: Input 0010: LCD0-D2 0100: DSI0-D0P 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT0	 0001: Output 0011: LVDS0-D0P 0101: PWM0 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.24 0x0094 PD Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0094			Register Name: PD_CFG1	
Bit	Read/Write	Default/Hex	Description	
31:28	R/W	0xF	PD15_SELECT PD15 Select 0000: Input 0010: LCD0-D21 0100: DSI1-CKN 0110: UART3-RX 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT15	 0001: Output 0011: LVDS1-D2N 0101: PWM15 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
27:24	R/W	0xF	PD14_SELECT PD14 Select 0000: Input 0010: LCD0-D20 0100: DSI1-CKP 0110: UART3-TX 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT14	 0001: Output 0011: LVDS1-D2P 0101: PWM14 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
23:20	R/W	0xF	PD13_SELECT	

Offset: 0x0094			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
			PD13 Select 0000: Input 0001: Output 0010: LCD0-D19 0011: LVDS1-D1N 0100: DSI1-D1N 0101: PWM13 0110:SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT13 1111: IO Disable
19:16	R/W	0xF	PD12_SELECT PD12 Select 0000: Input 0001: Output 0010: LCD0-D18 0011: LVDS1-D1P 0100: DSI1-D1P 0101: PWM12 0110: SPI1-MOSI/DBI-SDO 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT12 1111: IO Disable
15:12	R/W	0xF	PD11_SELECT PD11 Select 0000: Input 0001: Output 0010: LCD0-D15 0011: LVDS1-D0N 0100: DSI1-D0N 0101: PWM11 0110: SPI1-CLK/DBI-SCLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT11 1111: IO Disable
11:8	R/W	0xF	PD10_SELECT PD10 Select 0000: Input 0001: Output 0010: LCD0-D14 0011: LVDS1-D0P 0100: DSI1-D0P 0101: PWM10 0110: SPI1-CS/DBI-CSX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved

Offset: 0x0094			Register Name: PD_CFG1	
Bit	Read/Write	Default/Hex	Description	
			1110: PD-EINT10	1111: IO Disable
7:4	R/W	0xF	PD9_SELECT PD9 Select 0000: Input 0010: LCD0-D13 0100: DSI0-D3N 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT9	 0001: Output 0011: LVDS0-D3N 0101: PWM9 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PD8_SELECT PD8 Select 0000: Input 0010: LCD0-D12 0100: DSI0-D3P 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT8	 0001: Output 0011: LVDS0-D3P 0101: PWM8 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.25 0x0098 PD Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x0098			Register Name: PD_CFG2	
Bit	Read/Write	Default/Hex	Description	
31:28	R/W	0xF	PD23_SELECT PD23 Select 0000: Input 0010: PWM0 0100: UART2-CTS 0110: TWI0-SDA 1000: Reserved 1010: Reserved 1100: Reserved 1110: PD-EINT23	 0001: Output 0011: SPI1-WP/DBI-TE 0101: UART7-RX 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
27:24	R/W	0xF	PD22_SELECT PD22 Select 0000: Input 0010: PWM1 0011: SPI1-HOLD/DBI-DCX/DBI-WRX	 0001: Output

Offset: 0x0098			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
			0100: UART2-RTS 0101: UART7-TX 0110: TWI0-SCK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT22 1111: IO Disable
23:20	R/W	0xF	PD21_SELECT PD21 Select 0000: Input 0001: Output 0010: LCD0-VSYNC 0011: PWM3 0100: UART2-RX 0101: UART7-CTS 0110: UART4-CTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT21 1111: IO Disable
19:16	R/W	0xF	PD20_SELECT PD20 Select 0000: Input 0001: Output 0010: LCD0-HSYNC 0011: PWM2 0100: UART2-TX 0101: UART7-RTS 0110: UART4-RTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT20 1111: IO Disable
15:12	R/W	0xF	PD19_SELECT PD19 Select 0000: Input 0001: Output 0010: LCD0-DE 0011: LVDS1-D3N 0100: DSI1-D3N 0101: PWM19 0110: UART4-RX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT19 1111: IO Disable
11:8	R/W	0xF	PD18_SELECT PD18 Select 0000: Input 0001: Output 0010: LCD0-CLK 0011: LVDS1-D3P 0100: DSI1-D3P 0101: PWM18

Offset: 0x0098			Register Name: PD_CFG2
Bit	Read/Write	Default/Hex	Description
			0110: UART4-TX 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT18 1111: IO Disable
7:4	R/W	0xF	PD17_SELECT PD17 Select 0000: Input 0001: Output 0010: LCD0-D23 0011: LVDS1-CKN/PLL-TEST-CKN 0100: DSI1-D2N 0101: PWM17 0110: UART3-CTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT17 1111: IO Disable
3:0	R/W	0xF	PD16_SELECT PD16 Select 0000: Input 0001: Output 0010: LCD0-D22 0011: LVDS1-CKP/PLL-TEST-CKP 0100: DSI1-D2P 0101: PWM16 0110: UART3-RTS 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PD-EINT16 1111: IO Disable

8.5.6.26 0x009C PD Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PD_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.27 0x00A0 PD Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	PD_DAT

Offset: 0x00A0			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
			PD Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.28 0x00A4 PD Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00A4			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD7_DRV PD7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD6_DRV PD6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD5_DRV PD5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD4_DRV PD4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD3_DRV PD3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD2_DRV

Offset: 0x00A4			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
			PD2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD1_DRV PD1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD0_DRV PD0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.29 0x00A8 PD Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00A8			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD15_DRV PD15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD14_DRV PD14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD13_DRV PD13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD12_DRV PD12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD11_DRV

Offset: 0x00A8			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
			PD11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD10_DRV PD10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD9_DRV PD9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD8_DRV PD8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.30 0x00AC PD Multi_Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x00AC			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PD23_DRV PD23 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PD22_DRV PD22 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PD21_DRV PD21 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PD20_DRV

Offset: 0x00AC			Register Name: PD_DRV2
Bit	Read/Write	Default/Hex	Description
			PD20 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PD19_DRV PD19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PD18_DRV PD18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PD17_DRV PD17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PD16_DRV PD16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.31 0x00B0 PD Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PD_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.32 0x00B4 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PD15_PULL PD15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull_up or down Select

Offset: 0x00B4			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up

Offset: 0x00B4			Register Name: PD_PUL0
Bit	Read/Write	Default/Hex	Description
			10: Pull_down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.33 0x00B8 PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PD_PUL1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	R/W	0x0	PD23_PULL PD23 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PD22_PULL PD22 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull_up or down Select

Offset: 0x00B8			Register Name: PD_PUL1
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.34 0x00C0 PE Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C0			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PE7_SELECT PE7 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-LRCK 0101: LCD1-TRIG 0110: NCSI-D9 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT7 1111: IO Disable
27:24	R/W	0xF	PE6_SELECT PE6 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-BCLK 0101: LCD0-TRIG 0110: NCSI-D8 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT6 1111: IO Disable
23:20	R/W	0xF	PE5_SELECT PE5 Select

Offset: 0x00C0			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
			0000: Input 0001: Output 0010: MCSI1-MCLK 0011: PLL-LOCK-DBG 0100: I2S2-MCLK 0101: LEDC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT5 1111: IO Disable
19:16	R/W	0xF	PE4_SELECT PE4 Select 0000: Input 0001: Output 0010: TWI3-SDA 0011: UART4-CTS 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT4 1111: IO Disable
15:12	R/W	0xF	PE3_SELECT PE3 Select 0000: Input 0001: Output 0010: TWI3-SCK 0011: UART4-RTS 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT3 1111: IO Disable
11:8	R/W	0xF	PE2_SELECT PE2 Select 0000: Input 0001: Output 0010: TWI2-SDA 0011: UART4-RX 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT2 1111: IO Disable
7:4	R/W	0xF	PE1_SELECT PE1 Select 0000: Input 0001: Output

Offset: 0x00C0			Register Name: PE_CFG0	
Bit	Read/Write	Default/Hex	Description	
			0010: TWI2-SCK 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT1	0011: UART4-TX 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PE0_SELECT PE0 Select 0000: Input 0010: MCSI0-MCLK 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT0	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.35 0x00C4 PE Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x00C4			Register Name: PE_CFG1	
Bit	Read/Write	Default/Hex	Description	
31:28	R/W	0xF	PE15_SELECT PE15 Select 0000: Input 0010: MCSI2-MCLK 0100: Reserved 0110: NCSI-D15 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT15	 0001: Output 0011: PWM2 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
27:24	R/W	0xF	PE14_SELECT PE14 Select 0000: Input 0010: TWI4-SDA 0100: SPI2-MISO 0110: CSI1-XVS-FSYNC 1000: Reserved 1010: Reserved 1100: Reserved	 0001: Output 0011: UART5-RX 0101: UART6-CTS 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved

Offset: 0x00C4			Register Name: PE_CFG1	
Bit	Read/Write	Default/Hex	Description	
			1110: PE-EINT14	1111: IO Disable
23:20	R/W	0xF	PE13_SELECT PE13 Select 0000: Input 0010: TWI4-SCK 0100: SPI2-MOSI 0110: CSI0-XVS-FSYNC 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT13	 0001: Output 0011: UART5-TX 0101: UART6-RTS 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PE12_SELECT PE12 Select 0000: Input 0010: TWI1-SDA 0100: SPI2-CLK 0110: NCSI-D14 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT12	 0001: Output 0011: UART5-CTS 0101: UART6-RX 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PE11_SELECT PE11 Select 0000: Input 0010: TWI1-SCK 0100: SPI2-CS0 0110: NCSI-D13 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT11	 0001: Output 0011: UART5-RTS 0101: UART6-TX 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PE10_SELECT PE10 Select 0000: Input 0010: MCSI3-MCLK 0100: Reserved 0110: NCSI-D12 1000: Reserved 1010: Reserved 1100: Reserved 1110: PE-EINT10	 0001: Output 0011: PWM3 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00C4			Register Name: PE_CFG1
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PE9_SELECT PE9 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-DIN0 0101: Reserved 0110: NCSI-D11 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT9 1111: IO Disable
3:0	R/W	0xF	PE8_SELECT PE8 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S2-DOUT0 0101: Reserved 0110: NCSI-D10 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PE-EINT8 1111: IO Disable

8.5.6.36 0x00C8 PE Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: PE_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.37 0x00CC PE Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PE_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.38 0x00D0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0	PE_DAT

Offset: 0x00D0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
			PE Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.39 0x00D4 PE Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x00D4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PE7_DRV PE7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE6_DRV PE6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE5_DRV PE5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE4_DRV PE4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE3_DRV PE3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE2_DRV

Offset: 0x00D4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
			PE2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE1_DRV PE1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE0_DRV PE0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.40 0x00D8 PE Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x00D8			Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PE15_DRV PE15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PE14_DRV PE14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PE13_DRV PE13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PE12_DRV PE12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PE11_DRV

Offset: 0x00D8			Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
			PE11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PE10_DRV PE10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PE9_DRV PE9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PE8_DRV PE8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.41 0x00DC PE Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x00DC			Register Name: PE_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.42 0x00E0 PE Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PE_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.43 0x00E4 PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PE15_PULL PE15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x00E4			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
29:28	R/W	0x0	PE14_PULL PE14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PE13_PULL PE13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PE4_PULL

Offset: 0x00E4			Register Name: PE_PUL0
Bit	Read/Write	Default/Hex	Description
			PE4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.44 0x00E8 PE Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PE_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.45 0x00F0 PF Configure Register 0 (Default Value: 0x0FFF_FFFF)

Offset: 0x00F0			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	PF6_SELECT PF6 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: Reserved 0101: I2S3-MCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved

Offset: 0x00F0			Register Name: PF_CFG0	
Bit	Read/Write	Default/Hex	Description	
			1110: PF-EINT6	1111: IO Disable
23:20	R/W	0xF	PF5_SELECT PF5 Select 0000: Input 0010: SDC0-D2 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF-EINT5	 0001: Output 0011: JTAG-CK 0101: I2S3-BCLK 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
19:16	R/W	0xF	PF4_SELECT PF4 Select 0000: Input 0010: SDC0-D3 0100: Reserved 0110: I2S3-DOUT3 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF-EINT4	 0001: Output 0011: UART0-RX 0101: I2S3-DIN3 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PF3_SELECT PF3 Select 0000: Input 0010: SDC0-CMD 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF-EINT3	 0001: Output 0011: JTAG-DO 0101: I2S3-LRCK 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PF2_SELECT PF2 Select 0000: Input 0010: SDC0-CLK 0100: Reserved 0110: I2S3-DOUT2 1000: Reserved 1010: Reserved 1100: Reserved 1110: PF-EINT2	 0001: Output 0011: UART0-TX 0101: I2S3-DIN2 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

Offset: 0x00F0			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
7:4	R/W	0xF	PF1_SELECT PF1 Select 0000: Input 0001: Output 0010: SDC0-D0 0011: JTAG-DI 0100: Reserved 0101: I2S3-DOUT0 0110: I2S3-DIN1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT1 1111: IO Disable
3:0	R/W	0xF	PF0_SELECT PF0 Select 0000: Input 0001: Output 0010: SDC0-D1 0011: JTAG-MS 0100: Reserved 0101: I2S3-DIN0 0110: I2S3-DOUT1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PF-EINT0 1111: IO Disable

8.5.6.46 0x00F4 PF Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PF_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.47 0x00F8 PF Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PF_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.48 0x00FC PF Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: PF_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.49 0x0100 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R/W	0	PF_DAT PF Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.50 0x0104 PF Multi_Driving Register 0 (Default Value: 0x0111_1111)

Offset: 0x0104			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PF6_DRV PF6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PF5_DRV PF5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PF4_DRV PF4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PF3_DRV PF3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PF2_DRV PF2 Multi_Driving Select

Offset: 0x0104			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
			00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PF1_DRV PF1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PF0_DRV PF0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.51 0x0108 PF Multi_Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PF_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.52 0x010C PF Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PF_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.53 0x0110 PF Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PF_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.54 0x0114 PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PF_PUL0
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up

Offset: 0x0114			Register Name: PF_PUL0
Bit	Read/Write	Default/Hex	Description
			10: Pull_down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.55 0x0118 PF Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PF_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.56 0x0120 PG Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0120			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PG7_SELECT PG7 Select 0000: Input 0001: Output 0010: UART1-RX 0011: Reserved

Offset: 0x0120			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
			0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT7 1111: IO Disable
27:24	R/W	0xF	PG6_SELECT PG6 Select 0000: Input 0001: Output 0010: UART1-TX 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT6 1111: IO Disable
23:20	R/W	0xF	PG5_SELECT PG5 Select 0000: Input 0001: Output 0010: SDC1-D3 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT5 1111: IO Disable
19:16	R/W	0xF	PG4_SELECT PG4 Select 0000: Input 0001: Output 0010: SDC1-D2 0011: PCIE0-CLKREQN 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT4 1111: IO Disable
15:12	R/W	0xF	PG3_SELECT PG3 Select 0000: Input 0001: Output 0010: SDC1-D1 0011: PCIE0-WAKEN

Offset: 0x0120			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description
			0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT3 1111: IO Disable
11:8	R/W	0xF	PG2_SELECT PG2 Select 0000: Input 0001: Output 0010: SDC1-D0 0011: PCIE0-PERSTN 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT2 1111: IO Disable
7:4	R/W	0xF	PG1_SELECT PG1 Select 0000: Input 0001: Output 0010: SDC1-CMD 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT1 1111: IO Disable
3:0	R/W	0xF	PG0_SELECT PG0 Select 0000: Input 0001: Output 0010: SDC1-CLK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT0 1111: IO Disable

8.5.6.57 0x0124 PG Configure Register 1 (Default Value: 0x0FFF_FFFF)

Offset: 0x0124			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description

Offset: 0x0124			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	PG14_SELECT PG14 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-DIN0 0100: I2S1-DOUT1 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT14 1111: IO Disable
23:20	R/W	0xF	PG13_SELECT PG13 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-DOUT0 0100: I2S1-DIN1 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT13 1111: IO Disable
19:16	R/W	0xF	PG12_SELECT PG12 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-LRCK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT12 1111: IO Disable
15:12	R/W	0xF	PG11_SELECT PG11 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-BCLK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT11 1111: IO Disable

Offset: 0x0124			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
11:8	R/W	0xF	PG10_SELECT PG10 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S1-MCLK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT10 1111: IO Disable
7:4	R/W	0xF	PG9_SELECT PG9 Select 0000: Input 0001: Output 0010: UART1-CTS 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT9 1111: IO Disable
3:0	R/W	0xF	PG8_SELECT PG8 Select 0000: Input 0001: Output 0010: UART1-RTS 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PG-EINT8 1111: IO Disable

8.5.6.58 0x0128 PG Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PG_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.59 0x012C PG Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x012C	Register Name: PG_CFG3

Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.60 0x0130 PG Data Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PG_DAT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	0	PG_DAT PG Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.61 0x0134 PG Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0134			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PG7_DRV PG7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PG6_DRV PG6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PG5_DRV PG5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PG4_DRV PG4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

Offset: 0x0134			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:12	R/W	0x1	PG3_DRV PG3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PG2_DRV PG2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PG1_DRV PG1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PG0_DRV PG0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.62 0x0138 PG Multi_Driving Register 1 (Default Value: 0x0111_1111)

Offset: 0x0138			Register Name: PG_DRV1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x1	PG14_DRV PG14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PG13_DRV PG13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PG12_DRV PG12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

Offset: 0x0138			Register Name: PG_DRV1
Bit	Read/Write	Default/Hex	Description
15:14	/	/	/
13:12	R/W	0x1	PG11_DRV PG11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PG10_DRV PG10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PG9_DRV PG9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PG8_DRV PG8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.63 0x013C PG Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PG_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.64 0x0140 PG Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PG_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.65 0x0144 PG Pull Register 0 (Default Value: 0x0000_0554)

Offset: 0x0144			Register Name: PG_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	PG14_PULL

Offset: 0x0144			Register Name: PG_PUL0
Bit	Read/Write	Default/Hex	Description
			PG14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PG13_PULL PG13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PG10_PULL PG10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x1	PG5_PULL PG5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x1	PG4_PULL PG4 Pull_up or down Select

Offset: 0x0144			Register Name: PG_PUL0
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x1	PG3_PULL PG3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x1	PG2_PULL PG2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x1	PG1_PULL PG1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.66 0x0148 PG Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PG_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.67 0x0150 PH Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PH7_SELECT PH7 Select 0000: Input 0001: Output 0010: UART3-CTS 0011: SPI1-MISO 0100: OWA-OUT 0101: RGMII0-TXCTL/RMII0-TXEN 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT7 1111: IO Disable

Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
27:24	R/W	0xF	PH6_SELECT PH6 Select 0000: Input 0001: Output 0010: UART3-RTS 0011: SPI1-MOSI 0100: OWA-IN 0101: RGMII0-TXCK/RMII0-TXCK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT6 1111: IO Disable
23:20	R/W	0xF	PH5_SELECT PH5 Select 0000: Input 0001: Output 0010: UART3-RX 0011: SPI1-CLK 0100: LEDC 0101: RGMII0-TXD0/RMII0-TXD0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT5 1111: IO Disable
19:16	R/W	0xF	PH4_SELECT PH4 Select 0000: Input 0001: Output 0010: UART3-TX 0011: SPI1-CS0 0100: Reserved 0101: RGMII0-TXD1/RMII0-TXD1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT4 1111: IO Disable
15:12	R/W	0xF	PH3_SELECT PH3 Select 0000: Input 0001: Output 0010: TWI1-SDA 0011: IR-TX 0100: I2S2-DIN2 0101: RGMII0-CLKIN/RMII0-RXER 0110: I2S2-DOUT2 0111: Reserved 1000: Reserved 1001: Reserved

Offset: 0x0150			Register Name: PH_CFG0
Bit	Read/Write	Default/Hex	Description
			1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH_EINT3 1111: IO Disable
11:8	R/W	0xF	PH2_SELECT PH2 Select 0000: Input 0001: Output 0010: TWI1-SCK 0011: Reserved 0100: I2S2-DIN3 0101: RGMII0-RXCTL/RMII0-CRS-DV 0110: I2S2-DOUT3 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT2 1111: IO Disable
7:4	R/W	0xF	PH1_SELECT PH1 Select 0000: Input 0001: Output 0010: TWI0-SDA 0011: Reserved 0100: Reserved 0101: RGMII0-RXD0/RMII0-RXD0 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT1 1111: IO Disable
3:0	R/W	0xF	PH0_SELECT PH0 Select 0000: Input 0001: Output 0010: TWI0-SCK 0011: Reserved 0100: Reserved 0101: RGMII0-RXD1/RMII0-RXD1 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT0 1111: IO Disable

8.5.6.68 0x0154 PH Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0154			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description

Offset: 0x0154			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PH15_SELECT PH15 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S3-LRCK 0101: RGMII0-RXD2/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT15 1111: IO Disable
27:24	R/W	0xF	PH14_SELECT PH14 Select 0000: Input 0001: Output 0010: Reserved 0011: Reserved 0100: I2S3-BCLK 0101: RGMII0-RXD3/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT14 1111: IO Disable
23:20	R/W	0xF	PH13_SELECT PH13 Select 0000: Input 0001: Output 0010: Reserved 0011: TWI3-SDA 0100: I2S3-MCLK 0101: RGMII0-EPHY-25M 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT13 1111: IO Disable
19:16	R/W	0xF	PH12_SELECT PH12 Select 0000: Input 0001: Output 0010: DMIC-DATA3 0011: TWI3-SCK 0100: I2S2-DIN0 0101: I2S2-DOUT1 0110: PCIE0-WAKEN 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved

Offset: 0x0154			Register Name: PH_CFG1	
Bit	Read/Write	Default/Hex	Description	
			1100: Reserved	1101: Reserved
			1110: PH-EINT12	1111: IO Disable
15:12	R/W	0xF	PH11_SELECT PH11 Select 0000: Input 0010: DMIC-DATA2 0100: I2S2-DOUT0 0110: PCIE0-PERSTN 1000: Reserved 1010: Reserved 1100: Reserved 1110: PH-EINT11	 0001: Output 0011: SPI2-MISO 0101: I2S2-DIN1 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PH10_SELECT PH10 Select 0000: Input 0010: DMIC-DATA1 0100: I2S2-LRCK 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PH-EINT10	 0001: Output 0011: SPI2-MOSI 0101: RGMII0-MDIO 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PH9_SELECT PH9 Select 0000: Input 0010: DMIC-DATA0 0100: I2S2-BCLK 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PH-EINT9	 0001: Output 0011: SPI2-CLK 0101: RGMII0-MDC 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PH8_SELECT PH8 Select 0000: Input 0010: DMIC-CLK 0100: I2S2-MCLK 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved	 0001: Output 0011: SPI2-CS0 0101: I2S2-DIN2 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved

Offset: 0x0154			Register Name: PH_CFG1
Bit	Read/Write	Default/Hex	Description
			1110: PH-EINT8 1111: IO Disable

8.5.6.69 0x0158 PH Configure Register 2 (Default Value: 0x0000_FFFF)

Offset: 0x0158			Register Name: PH_CFG2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0xF	PH19_SELECT PH19 Select 0000: Input 0001: Output 0010: IR-RX 0011: I2S3-DOUT3 0100: I2S3-DIN3 0101: LEDC 0110: PCIE0-CLKREQN 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT19 1111: IO Disable
11:8	R/W	0xF	PH18_SELECT PH18 Select 0000: Input 0001: Output 0010: IR-TX 0011: I2S3-DOUT2 0100: I2S3-DIN2 0101: RGMII0-TXD2/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT18 1111: IO Disable
7:4	R/W	0xF	PH17_SELECT PH17 Select 0000: Input 0001: Output 0010: Reserved 0011: I2S3-DOUT1 0100: I2S3-DIN0 0101: RGMII0-TXD3/RMII0-NULL 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT17 1111: IO Disable
3:0	R/W	0xF	PH16_SELECT PH16 Select

Offset: 0x0158			Register Name: PH_CFG2
Bit	Read/Write	Default/Hex	Description
			0000: Input 0001: Output 0010: Reserved 0011: I2S3-DOUT0 0100: I2S3-DIN1 0101: RGMII0-RXCK/RMII0-NULL 0110: CLK-FANOUT0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PH-EINT16 1111: IO Disable

8.5.6.70 0x015C PH Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: PH_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.71 0x0160 PH Data Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PH_DAT
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0	PH_DAT PH Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.72 0x0164 PH Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0164			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PH7_DRV PH7 Multi_Driving Select 00: Level0 01: Level1

Offset: 0x0164			Register Name: PH_DRV0
Bit	Read/Write	Default/Hex	Description
			10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PH6_DRV PH6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH5_DRV PH5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH4_DRV PH4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH3_DRV PH3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH2_DRV PH2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH1_DRV PH1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH0_DRV PH0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.73 0x0168 PH Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0168	Register Name: PH_DRV1

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PH15_DRV PH15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PH14_DRV PH14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PH13_DRV PH13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PH12_DRV PH12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PH11_DRV PH11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH10_DRV PH10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH9_DRV PH9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH8_DRV PH8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.74 0x016C PH Multi_Driving Register 2 (Default Value: 0x0000_1111)

Offset: 0x016C			Register Name: PH_DRV2
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x1	PH19_DRV PH19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PH18_DRV PH18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PH17_DRV PH17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PH16_DRV PH16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.75 0x0170 PH Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PH_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.76 0x0174 PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PH15_PULL PH15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up

Offset: 0x0174			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
			10: Pull_down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

Offset: 0x0174			Register Name: PH_PUL0
Bit	Read/Write	Default/Hex	Description
7:6	R/W	0x0	PH3_PULL PH3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.77 0x0178 PH Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PH_PUL1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x0	PH19_PULL PH19 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PH18_PULL PH18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PH17_PULL PH17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PH16_PULL PH16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.78 0x0500 PK Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0500			Register Name: PK_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK7_SELECT PK7 Select 0000: Input 0001: Output 0010: MCSIB-D0P 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT7 1111: IO Disable
27:24	R/W	0xF	PK6_SELECT PK6 Select 0000: Input 0001: Output 0010: MCSIB-D0N 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT6 1111: IO Disable
23:20	R/W	0xF	PK5_SELECT PK5 Select 0000: Input 0001: Output 0010: MCSIA-CKP 0011: TWI2-SDA 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT5 1111: IO Disable
19:16	R/W	0xF	PK4_SELECT PK4 Select 0000: Input 0001: Output 0010: MCSIA-CKN 0011: TWI2-SCK 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved

Offset: 0x0500			Register Name: PK_CFG0	
Bit	Read/Write	Default/Hex	Description	
			1110: PK-EINT4	1111: IO Disable
15:12	R/W	0xF	PK3_SELECT PK3 Select 0000: Input 0010: MCSIA-D1P 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT3	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PK2_SELECT PK2 Select 0000: Input 0010: MCSIA-D1N 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT2	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PK1_SELECT PK1 Select 0000: Input 0010: MCSIA-D0P 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT1	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PK0_SELECT PK0 Select 0000: Input 0010: MCSIA-D0N 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT0	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.79 0x0504 PK Configure Register 1 (Default Value: 0xFFFF_FFFF)

Offset: 0x0504			Register Name: PK_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK15_SELECT PK15 Select 0000: Input 0001: Output 0010: MCSIC-D1P 0011: UART7-CTS 0100: UART5-CTS 0101: NCSI-VSYNC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT15 1111: IO Disable
27:24	R/W	0xF	PK14_SELECT PK14 Select 0000: Input 0001: Output 0010: MCSIC-D1N 0011: UART7-RTS 0100: UART5-RTS 0101: NCSI-HSYNC 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT14 1111: IO Disable
23:20	R/W	0xF	PK13_SELECT PK13 Select 0000: Input 0001: Output 0010: MCSIC-D0P 0011: UART7-RX 0100: TWI4-SDA 0101: NCSI-MCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT13 1111: IO Disable
19:16	R/W	0xF	PK12_SELECT PK12 Select 0000: Input 0001: Output 0010: MCSIC-D0N 0011: UART7-TX 0100: TWI4-SCK 0101: NCSI-PCLK 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved

Offset: 0x0504			Register Name: PK_CFG1	
Bit	Read/Write	Default/Hex	Description	
			1110: PK-EINT12	1111: IO Disable
15:12	R/W	0xF	PK11_SELECT PK11 Select 0000: Input 0010: MCSIB-CKP 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT11	 0001: Output 0011: TWI3-SDA 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PK10_SELECT PK10 Select 0000: Input 0010: MCSIB-CKN 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT10	 0001: Output 0011: TWI3-SCK 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PK9_SELECT PK9 Select 0000: Input 0010: MCSIB-D1P 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT9	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PK8_SELECT PK8 Select 0000: Input 0010: MCSIB-D1N 0100: Reserved 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT8	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.80 0x0508 PK Configure Register 2 (Default Value: 0xFFFF_FFFF)

Offset: 0x0508			Register Name: PK_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PK23_SELECT PK23 Select 0000: Input 0001: Output 0010: MCSID-CKP 0011: TWI3-SDA 0100: PWM7 0101: NCSI-D7 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT23 1111: IO Disable
27:24	R/W	0xF	PK22_SELECT PK22 Select 0000: Input 0001: Output 0010: MCSID-CKN 0011: TWI3-SCK 0100: PWM6 0101: NCSI-D6 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT22 1111: IO Disable
23:20	R/W	0xF	PK21_SELECT PK21 Select 0000: Input 0001: Output 0010: MCSID-D1P 0011: MIPI-MCLK1 0100: UART6-CTS 0101: NCSI-D5 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PK-EINT21 1111: IO Disable
19:16	R/W	0xF	PK20_SELECT PK20 Select 0000: Input 0001: Output 0010: MCSID-D1N 0011: TWI2-SDA 0100: UART6-RTS 0101: NCSI-D4 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved

Offset: 0x0508			Register Name: PK_CFG2	
Bit	Read/Write	Default/Hex	Description	
			1110: PK-EINT20	1111: IO Disable
15:12	R/W	0xF	PK19_SELECT PK19 Select 0000: Input 0010: MCSID-D0P 0100: UART6-RX 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT19	 0001: Output 0011: TWI2-SCK 0101: NCSI-D3 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PK18_SELECT PK18 Select 0000: Input 0010: MCSID-D0N 0100: UART6-TX 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT18	 0001: Output 0011: MIPI-MCLK0 0101: NCSI-D2 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PK17_SELECT PK17 Select 0000: Input 0010: MCSIC-CKP 0100: UART5-RX 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT17	 0001: Output 0011: TWI5-SDA 0101: NCSI-D1 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
3:0	R/W	0xF	PK16_SELECT PK16 Select 0000: Input 0010: MCSIC-CKN 0100: UART5-TX 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PK-EINT16	 0001: Output 0011: TWI5-SCK 0101: NCSI-D0 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable

8.5.6.81 0x050C PK Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x050C			Register Name: PK_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.82 0x0510 PK Data Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: PK_DAT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	PK_DAT PK Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.6.83 0x0514 PK Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0514			Register Name: PK_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK7_DRV PK7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK6_DRV PK6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK5_DRV PK5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK4_DRV

Offset: 0x0514			Register Name: PK_DRV0
Bit	Read/Write	Default/Hex	Description
			PK4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK3_DRV PK3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK2_DRV PK2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK1_DRV PK1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK0_DRV PK0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.84 0x0518 PK Multi_Driving Register 1 (Default Value: 0x1111_1111)

Offset: 0x0518			Register Name: PK_DRV1
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK15_DRV PK15 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK14_DRV PK14 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK13_DRV

Offset: 0x0518			Register Name: PK_DRV1
Bit	Read/Write	Default/Hex	Description
			PK13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK12_DRV PK12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK11_DRV PK11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK10_DRV PK10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK9_DRV PK9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK8_DRV PK8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.85 0x051C PK Multi_Driving Register 2 (Default Value: 0x1111_1111)

Offset: 0x051C			Register Name: PK_DRV2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PK23_DRV PK23 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PK22_DRV

Offset: 0x051C			Register Name: PK_DRV2
Bit	Read/Write	Default/Hex	Description
			PK22 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
23:22	/	/	/
21:20	R/W	0x1	PK21_DRV PK21 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PK20_DRV PK20 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PK19_DRV PK19 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PK18_DRV PK18 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PK17_DRV PK17 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PK16_DRV PK16 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.6.86 0x0520 PK Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: PK_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.87 0x0524 PK Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	PK15_PULL PK15 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
29:28	R/W	0x0	PK14_PULL PK14 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
27:26	R/W	0x0	PK13_PULL PK13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PK12_PULL PK12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PK11_PULL PK11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PK10_PULL PK10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PK9_PULL PK9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PK8_PULL PK8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PK7_PULL PK7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PK6_PULL PK6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up

Offset: 0x0524			Register Name: PK_PUL0
Bit	Read/Write	Default/Hex	Description
			10: Pull_down 11: Reserved
11:10	R/W	0x0	PK5_PULL PK5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PK4_PULL PK4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PK3_PULL PK3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PK2_PULL PK2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PK1_PULL PK1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PK0_PULL PK0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.88 0x0528 PK Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0528			Register Name: PK_PUL1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	R/W	0x0	PK23_PULL PK23 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PK22_PULL PK22 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PK21_PULL PK21 Pull_up or down Select

Offset: 0x0528			Register Name: PK_PUL1
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PK20_PULL PK20 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PK19_PULL PK19 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PK18_PULL PK18 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PK17_PULL PK17 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PK16_PULL PK16 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.6.89 0x0220 PB External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

Offset: 0x0220			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x0220			Register Name: PB_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.90 0x0224 PB External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PB_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode

Offset: 0x0224			Register Name: PB_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.91 0x0228 PB External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PB_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.92 0x022C PB External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C	Register Name: PB_INT_CFG3

Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.93 0x0230 PB External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PB_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable

Offset: 0x0230			Register Name: PB_INT_CTL
Bit	Read/Write	Default/Hex	Description
			1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.94 0x0234 PB External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0234			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS

Offset: 0x0234			Register Name: PB_INT_STA
Bit	Read/Write	Default/Hex	Description
			External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.95 0x0238 PB External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PB_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.6.96 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x0240			Register Name: PC_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.97 0x0244 PC External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge

Offset: 0x0244			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge

Offset: 0x0244			Register Name: PC_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.98 0x0248 PC External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: PC_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.99 0x024C PC External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: PC_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.100 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_CTL

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
			External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable

Offset: 0x0250			Register Name: PC_INT_CTL
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.101 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending

Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
			Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0254			Register Name: PC_INT_STA
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.102 0x0258 PC External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/

Offset: 0x0258			Register Name: PC_INT_DEB
Bit	Read/Write	Default/Hex	Description
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24 MHz

8.5.6.103 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge

Offset: 0x0260			Register Name: PD_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.104 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0264	Register Name: PD_INT_CFG1

Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge

Offset: 0x0264			Register Name: PD_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.105 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0268			Register Name: PD_INT_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.106 0x026C PD External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: PD_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.107 0x0270 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_CTL External INT23 Enable 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL

Offset: 0x0270			Register Name: PD_INT_CTL
Bit	Read/Write	Default/Hex	Description
			External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.108 0x0274 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
			External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit

Offset: 0x0274			Register Name: PD_INT_STA
Bit	Read/Write	Default/Hex	Description
			0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.109 0x0278 PD External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: PD_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

8.5.6.110 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0280			Register Name: PE_INT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.111 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x0284			Register Name: PE_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.112 0x0288 PE External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: PE_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.113 0x028C PE External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: PE_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.114 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable

Offset: 0x0290			Register Name: PE_INT_CTL
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.115 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending

Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
			Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x0294			Register Name: PE_INT_STA
Bit	Read/Write	Default/Hex	Description
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.116 0x0298 PE External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/

Offset: 0x0298			Register Name: PE_INT_DEB
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.6.117 0x02A0 PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x02A0			Register Name: PF_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.118 0x02A4 PF External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02A4			Register Name: PF_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.119 0x02A8 PF External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PF_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.120 0x02AC PF External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: PF_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.121 0x02B0 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.122 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_INT_STA
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.123 0x02B8 PF External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.6.124 0x02C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x02C0			Register Name: PG_INT_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.125 0x02C4 PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

Offset: 0x02C4			Register Name: PG_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.126 0x02C8 PG External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02C8			Register Name: PG_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.127 0x02CC PG External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02CC			Register Name: PG_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.128 0x02D0 PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable

Offset: 0x02D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
			1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable

Offset: 0x02D0			Register Name: PG_INT_CTL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.129 0x02D4 PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending

Offset: 0x02D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
			Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit. 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

Offset: 0x02D4			Register Name: PG_INT_STA
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.130 0x02D8 PG External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PG_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.6.131 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

Offset: 0x02E0			Register Name: PH_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.132 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge

Offset: 0x02E4			Register Name: PH_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.133 0x02E8 PH External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: PH_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

Offset: 0x02E8			Register Name: PH_INT_CFG2
Bit	Read/Write	Default/Hex	Description
			0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.134 0x02EC PH External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: PH_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.135 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable

Offset: 0x02F0			Register Name: PH_INT_CTL
Bit	Read/Write	Default/Hex	Description
			1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.136 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS External INT15 Pending Bit

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
			0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending

Offset: 0x02F4			Register Name: PH_INT_STA
Bit	Read/Write	Default/Hex	Description
			1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.137 0x02F8 PH External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x02F8	Register Name: PH_INT_DEB

Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/dW	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.6.138 0x0340 PK External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PK_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge

Offset: 0x0340			Register Name: PK_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.139 0x0344 PK External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0344	Register Name: PK_INT_CFG1

Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge

Offset: 0x0344			Register Name: PK_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.140 0x0348 PK External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT23_CFG External INT23 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x0348			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

Offset: 0x0348			Register Name: PK_INT_CFG2
Bit	Read/Write	Default/Hex	Description
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.6.141 0x034C PK External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x034C			Register Name: PK_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.6.142 0x0350 PK External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	EINT23_CTL External INT23 Enable 0: Disable 1: Enable
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable

Offset: 0x0350			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL

Offset: 0x0350			Register Name: PK_INT_CTL
Bit	Read/Write	Default/Hex	Description
			External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.6.143 0x0354 PK External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
23	R/W	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
22	R/W	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W	0x0	EINT15_STATUS

Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
			External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS External INT7 Pending Bit

Offset: 0x0354			Register Name: PK_INT_STA
Bit	Read/Write	Default/Hex	Description
			0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.6.144 0x0358 PK External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: PK_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.6.145 0x0380 GPIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0380			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x1	VCCIO_PWR_MOD_SEL VCC_IO POWER MODE Select 1: 3.3V 0: 1.8V
11	/	/	/
10	R/W	0x1	PK_PWR_MOD_SEL PK_POWER MODE Select 1: 3.3V 0: 1.8V If PK_Port Power Source select VCC_IO, this bit is invalid
9	R/W	0x1	PJ_PWR_MOD_SEL PJ_POWER MODE Select 1: 3.3V 0: 1.8V If PJ_Port Power Source select VCC_IO, this bit is invalid
8	R/W	0x1	PI_PWR_MOD_SEL PI_POWER MODE Select 1: 3.3V 0: 1.8V If PI_Port Power Source select VCC_IO, this

Offset: 0x0380			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
			bit is invalid
7	/	/	/
6	R/W	0x1	PG_PWR_MOD_SEL PG_POWER MODE Select 1: 3.3V 0: 1.8V If PG_Port Power Source select VCC_IO, this bit is invalid
5	R/W	0x1	PF_PWR_MOD_SEL PF_POWER MODE Select 1: 3.3V 0: 1.8V If PF_Port Power Source select VCC_IO, this bit is invalid
4	R/W	0x1	PE_PWR_MOD_SEL PE_POWER MODE Select 1: 3.3V 0: 1.8V If PE_Port Power Source select VCC_IO, this bit is invalid
3	R/W	0x1	PD_PWR_MOD_SEL PD_POWER MODE Select 1: 3.3V 0: 1.8V If PD_Port Power Source select VCC_IO, this bit is invalid
2	R/W	0x1	PC_PWR_MOD_SEL PC_POWER MODE Select 1: 3.3V 0: 1.8V If PC_Port Power Source select VCC_IO, this bit is invalid
1	R/W	0x1	PB_PWR_MOD_SEL PB_POWER MODE Select 1: 3.3V 0: 1.8V If PB_Port Power Source select VCC_IO, this bit is invalid
0	/	/	/

8.5.6.146 0x0384 GPIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0384			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL VCC_IO Withstand Voltage Mode Select Control 0: Enable 1: Disable
11	/	/	/
10	R/W	0x0	VCC_PK_WS_VOL_MOD_SEL VCC_PK Withstand Voltage Mode Select Control. 0: Enable 1: Disable
9	R/W	0x0	VCC_PJ_WS_VOL_MOD_SEL VCC_PJ Withstand Voltage Mode Select Control 0: Enable 1: Disable
8	R/W	0x0	VCC_PI_WS_VOL_MOD_SEL VCC_PI Withstand Voltage Mode Select Control 0: Enable 1: Disable
7	/	/	/
6	R/W	0x0	VCC_PG_WS_VOL_MOD_SEL VCC_PG Withstand Voltage Mode Select Control 0: Enable 1: Disable
5	R/W	0x0	VCC_PF_WS_VOL_MOD_SEL VCC_PF Withstand Voltage Mode Select Control 0: Enable 1: Disable
4	R/W	0x0	VCC_PE_WS_VOL_MOD_SEL VCC_PE Withstand Voltage Mode Select Control 0: Enable 1: Disable

Offset: 0x0384			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
3	R/W	0x0	VCC_PD_WS_VOL_MOD_SEL VCC_PD Withstand Voltage Mode Select Control 0: Enable 1: Disable
2	R/W	0x0	VCC_PC_WS_VOL_MOD_SEL VCC_PC Withstand Voltage Mode Select Control 0: Enable 1: Disable
1	R/W	0x0	VCC_PB_WS_VOL_MOD_SEL VCC_PB Withstand Voltage Mode Select Control 0: Enable 1: Disable
0	/	/	/

8.5.6.147 0x0388 GPIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0388			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	VCCIO_PWR_VAL VCC_IO Power Value
15:11	/	/	/
10	R	0x0	PK_PWR_VAL PK_Port Power Value 0:3.3V 1:1.8V If PK_Port Power Source select VCC_IO, this bit is invalid
9	R	0x0	PJ_PWR_VAL PJ_Port Power Value 0:3.3V 1:1.8V If PJ_Port Power Source select VCC_IO, this bit is invalid
8	R	0x0	PI_PWR_VAL PI_Port Power Value 0:3.3V 1:1.8V

Offset: 0x0388			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
			If PI_Port Power Source select VCC_IO, this bit is invalid
7	/	/	/
6	R	0x0	PG_PWR_VAL PG_Port Power Value 0:3.3V 1:1.8V If PG_Port Power Source select VCC_IO, this bit is invalid
5	R	0x0	PF_PWR_VAL PF_Port Power Value 0:3.3V 1:1.8V If PF_Port Power Source select VCC_IO, this bit is invalid
4	R	0x0	PE_PWR_VAL PE_Port Power Value 0:3.3V 1:1.8V If PE_Port Power Source select VCC_IO, this bit is invalid
3	R	0x0	PD_PWR_VAL PD_Port Power Value 0:3.3V 1:1.8V If PD_Port Power Source select VCC_IO, this bit is invalid
2	R	0x0	PC_PWR_VAL PC_Port Power Value 0:3.3V 1:1.8V If PC_Port Power Source select VCC_IO, this bit is invalid
1	R	0x0	PB_PWR_VAL PB_Port Power Value 0:3.3V 1:1.8V If PB_Port Power Source select VCC_IO, this bit is invalid
0	/	/	/

8.5.6.148 0x0390 GPIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0390			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control 0: 1.8V 1: 3.3V

8.5.7 S_GPIO Register Description

8.5.7.1 0x0000 PL Configure Register 0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0xF	PL7_SELECT PL7 Select 0000: Input 0001: Output 0010: S-JTAG-DI 0011: S-PWM7 0100: S-I2S0-DOUT1 0101: S-I2S0-DIN0 0110: S-DMIC-DATA1 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT7 1111: IO Disable
27:24	R/W	0xF	PL6_SELECT PL6 Select 0000: Input 0001: Output 0010: S-JTAG-DO 0011: S-PWM6 0100: S-I2S0-DIN1 0101: S-I2S0-DOUT0 0110: S-DMIC-DATA2 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT6 1111: IO Disable
23:20	R/W	0xF	PL5_SELECT PL5 Select 0000: Input 0001: Output 0010: S-JTAG-CK 0011: Reserved 0100: S-PWM5 0101: S-I2S0-LRCK 0110: S-DMIC-DATA3 0111: Reserved

Offset: 0x0000			Register Name: PL_CFG0	
Bit	Read/Write	Default/Hex	Description	
			1000: Reserved	1001: Reserved
			1010: Reserved	1011: Reserved
			1100: Reserved	1101: Reserved
			1110: PL-EINT5	1111: IO Disable
19:16	R/W	0xF	PL4_SELECT PL4 Select 0000: Input 0010: S-JTAG-MS 0100: S-PWM4 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PL-EINT4	 0001: Output 0011: Reserved 0101: S-I2S0-BCLK 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
15:12	R/W	0xF	PL3_SELECT PL3 Select 0000: Input 0010: S-UART0-RX 0100: S-PWM3 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PL-EINT3	 0001: Output 0011: S-UART1-RX 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
11:8	R/W	0xF	PL2_SELECT PL2 Select 0000: Input 0010: S-UART0-TX 0100: S-PWM2 0110: Reserved 1000: Reserved 1010: Reserved 1100: Reserved 1110: PL-EINT2	 0001: Output 0011: S-UART1-TX 0101: Reserved 0111: Reserved 1001: Reserved 1011: Reserved 1101: Reserved 1111: IO Disable
7:4	R/W	0xF	PL1_SELECT PL1 Select 0000: Input 0010: S-TWI0-SDA 0100: Reserved 0110: Reserved 1000: Reserved	 0001: Output 0011: Reserved 0101: Reserved 0111: Reserved 1001: Reserved

Offset: 0x0000			Register Name: PL_CFG0
Bit	Read/Write	Default/Hex	Description
			1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT1 1111: IO Disable
3:0	R/W	0xF	PL0_SELECT PL0 Select 0000: Input 0001: Output 0010: S-TWI0-SCK 0011: Reserved 0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT0 1111: IO Disable

8.5.7.2 0x0004 PL Configure Register 1 (Default Value: 0x00FF_FFFF)

Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0xF	PL13_SELECT PL13 Select 0000: Input 0001: Output 0010: S-TWI2-SDA 0011: S-PWM9 0100: S-UART0-RX 0101: S-DMIC-DATA3 0110: S-SPI0-MISO 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT13 1111: IO Disable
19:16	R/W	0xF	PL12_SELECT PL12 Select 0000: Input 0001: Output 0010: S-TWI2-SCK 0011: S-PWM8 0100: S-UART0-TX 0101: S-DMIC-DATA2 0110: S-SPI0-MOSI 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT12 1111: IO Disable

Offset: 0x0004			Register Name: PL_CFG1
Bit	Read/Write	Default/Hex	Description
15:12	R/W	0xF	PL11_SELECT PL11 Select 0000: Input 0001: Output 0010: S-IR-RX 0011: Reserved 0100: S-RJTAG-DI 0101: S-DMIC-DATA1 0110: S-SPI0-CLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT11 1111: IO Disable
11:8	R/W	0xF	PL10_SELECT PL10 Select 0000: Input 0001: Output 0010: S-PWM0 0011: Reserved 0100: S-RJTAG-DO 0101: S-DMIC-DATA0 0110: S-SPI0-CS0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT10 1111: IO Disable
7:4	R/W	0xF	PL9_SELECT PL9 Select 0000: Input 0001: Output 0010: S-TWI1-SDA 0011: Reserved 0100: S-RJTAG-CK 0101: S-PWM1 0110: S-DMIC-CLK 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT9 1111: IO Disable
3:0	R/W	0xF	PL8_SELECT PL8 Select 0000: Input 0001: Output 0010: S-TWI1-SCK 0011: Reserved 0100: S-RJTAG-MS 0101: S-I2S0-MCLK 0110: S-DMIC-DATA0 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PL-EINT8 1111: IO Disable

8.5.7.3 0x0008 PL Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PL_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.4 0x000C PL Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PL_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.5 0x0010 PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	PL_DAT PL Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.7.6 0x0014 PL Multi_Driving Register 0 (Default Value: 0x1111_1111)

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x1	PL7_DRV PL7 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
27:26	/	/	/
25:24	R/W	0x1	PL6_DRV PL6 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

Offset: 0x0014			Register Name: PL_DRV0
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21:20	R/W	0x1	PL5_DRV PL5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PL4_DRV PL4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PL3_DRV PL3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PL2_DRV PL2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PL1_DRV PL1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PL0_DRV PL0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.7.7 0x0018 PL Multi_Driving Register 1 (Default Value: 0x0011_1111)

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PL13_DRV PL13 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

Offset: 0x0018			Register Name: PL_DRV1
Bit	Read/Write	Default/Hex	Description
19:18	/	/	/
17:16	R/W	0x1	PL12_DRV PL12 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PL11_DRV PL11 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PL10_DRV PL10 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PL9_DRV PL9 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PL8_DRV PL8 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.7.8 0x001C PL Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PL_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.9 0x0020 PL Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PL_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.10 0x0024 PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x0	PL13_PULL PL13 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
25:24	R/W	0x0	PL12_PULL PL12 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
23:22	R/W	0x0	PL11_PULL PL11 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
21:20	R/W	0x0	PL10_PULL PL10 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
19:18	R/W	0x0	PL9_PULL PL9 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
15:14	R/W	0x0	PL7_PULL PL7 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull_up or down Select

Offset: 0x0024			Register Name: PL_PUL0
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x1	PL1_PULL PL1 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.7.11 0x0028 PL Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PL_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.12 0x0030 PM Configure Register 0 (Default Value: 0x00FF_FFFF)

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0xF	PM5_SELECT PM5 Select 0000: Input 0001: Output 0010: S-IR-RX 0011: R-JTAG-DI 0100: S-TWI2-SDA 0101: S-PWM9 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT5 1111: IO Disable

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
19:16	R/W	0xF	PM4_SELECT PM4 Select 0000: Input 0001: Output 0010: S-PWM8 0011: R-JTAG-DO 0100: S-TWI2-SCK 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT4 1111: IO Disable
15:12	R/W	0xF	PM3_SELECT PM3 Select 0000: Input 0001: Output 0010: S-TWI1-SDA 0011: R-JTAG-CK 0100: S-PWM7 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT3 1111: IO Disable
11:8	R/W	0xF	PM2_SELECT PM2 Select 0000: Input 0001: Output 0010: S-TWI1-SCK 0011: R-JTAG-MS 0100: S-PWM6 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT2 1111: IO Disable
7:4	R/W	0xF	PM1_SELECT PM1 Select 0000: Input 0001: Output 0010: S-UART0-RX 0011: S-UART1-RX 0100: S-PWM3 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT1 1111: IO Disable
3:0	R/W	0xF	PM0_SELECT

Offset: 0x0030			Register Name: PM_CFG0
Bit	Read/Write	Default/Hex	Description
			PM0 Select 0000: Input 0001: Output 0010: S-UART0-TX 0011: S-UART1-TX 0100: S-PWM2 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Reserved 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: PM-EINT0 1111: IO Disable

8.5.7.13 0x0034 PM Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PM_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.14 0x0038 PM Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PM_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.15 0x003C PM Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PM_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.16 0x0040 PM Data Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PM_DAT
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0	PM_DAT PM Data If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit

Offset: 0x0040			Register Name: PM_DAT
Bit	Read/Write	Default/Hex	Description
			value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

8.5.7.17 0x0044 PM Multi_Driving Register 0 (Default Value: 0x0011_1111)

Offset: 0x0044			Register Name: PM_DRV0
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:20	R/W	0x1	PM5_DRV PM5 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
19:18	/	/	/
17:16	R/W	0x1	PM4_DRV PM4 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
15:14	/	/	/
13:12	R/W	0x1	PM3_DRV PM3 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
11:10	/	/	/
9:8	R/W	0x1	PM2_DRV PM2 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
7:6	/	/	/
5:4	R/W	0x1	PM1_DRV PM1 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3
3:2	/	/	/
1:0	R/W	0x1	PM0_DRV PM0 Multi_Driving Select 00: Level0 01: Level1 10: Level2 11: Level3

8.5.7.18 0x0048 PM Multi_Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: PM_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.19 0x004C PM Multi_Driving Register 2 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: PM_DRV2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.20 0x0050 PM Multi_Driving Register 3 (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: PM_DRV3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.21 0x0054 PM Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PM_PUL0
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:10	R/W	0x0	PM5_PULL PM5 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
9:8	R/W	0x0	PM4_PULL PM4 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
7:6	R/W	0x0	PM3_PULL PM3 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
5:4	R/W	0x0	PM2_PULL PM2 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
3:2	R/W	0x0	PM1_PULL PM1 Pull_up or down Select

Offset: 0x0054			Register Name: PM_PUL0
Bit	Read/Write	Default/Hex	Description
			00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved
1:0	R/W	0x0	PM0_PULL PM0 Pull_up or down Select 00: Pull_up/down disable01: Pull_up 10: Pull_down 11: Reserved

8.5.7.22 0x0058 PM Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PM_PUL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.23 0x0200 PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PL_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)