Offset: 0x0200			Register Name: PL_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.7.24 0x0204 PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

Offset: 0x0204			Register Name: PL_INT_CFG1
Bit	Read/Write	Default/Hex	Description
			0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.7.25 0x0208 PL External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PL_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.26 0x020C PL External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PL_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.27 0x0210 PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable

Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
			1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable

Offset: 0x0210			Register Name: PL_INT_CTL
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.7.28 0x0214 PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_INT_STA
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W	0x0	EINT7_STATUS

Offset: 0x0214			Register Name: PL_INT_STA
Bit	Read/Write	Default/Hex	Description
			External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.7.29 0x0218 PL External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.7.30 0x0220 PM External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PM_INT_CFG0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative)

Offset: 0x0220			Register Name: PM_INT_CFG0
Bit	Read/Write	Default/Hex	Description
			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge(Positive/Negative) Others: Reserved

8.5.7.31 0x0224 PM External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PM_INT_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.32 0x0228 PM External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PM_INT_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.33 0x022C PM External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PM_INT_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.5.7.34 0x0230 PM External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PM_INT_CTL
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

8.5.7.35 0x0234 PM External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PM_INT_STA
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	EINT5_STATUS

Offset: 0x0234			Register Name: PM_INT_STA
Bit	Read/Write	Default/Hex	Description
			External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

8.5.7.36 0x0238 PM External Debounce Configure Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PM_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre_scale n The selected clock source is prescaled by 2^n
3:1	/	/	/
0	R/W	0x0	GPIO_INT_CLK_SELECT

Offset: 0x0238			Register Name: PM_INT_DEB
Bit	Read/Write	Default/Hex	Description
			GPIO Interrupt Clock Select 0: LOSC 32 kHz 1: HOSC 24 MHz

8.5.7.37 0x0340 GPIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0003)

Offset: 0x0340			Register Name: GPIO_POW_MOD_SEL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VCCIO_PWR_MOD_SEL VCC-IO POWER MODE Select 1: 3.3V 0: 1.8V
11:2	/	/	/
1	R/W	0x1	PM_PWR_MOD_SEL PM_POWER MODE Select 1: 3.3V 0: 1.8V If PM_Port Power Source select VCC-IO, this bit is invalid
0	R/W	0x1	PL_PWR_MOD_SEL PL_POWER MODE Select 1: 3.3V 0: 1.8V If PL_Port Power Source select VCC_IO, this bit is invalid

8.5.7.38 0x0344 GPIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VCCIO_WS_VOL_MOD_SEL VCC_IO Withstand Voltage Mode Select Control 0: Enable 1: Disable
11:2	/	/	/
1	R/W	0x0	VCC_PM_WS_VOL_MOD_SEL

Offset: 0x0344			Register Name: GPIO_POW_MS_CTL
Bit	Read/Write	Default/Hex	Description
			VCC_PM Withstand Voltage Mode Select Control 0: Enable 1: Disable
0	R/W	0x0	VCC_PL_WS_VOL_MOD_SEL VCC_PL Withstand Voltage Mode Select Control 0: Enable 1: Disable

8.5.7.39 0x0348 GPIO Group Power Value Register (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: GPIO_POW_VAL
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R	0x0	VCCIO_PWR_VAL VCC_IO Power Value
15:2	/	/	/
1	R	0x0	PM_PWR_VAL PM_Port Power Value If PM_Port Power Source select VCC_IO, this bit is invalid
0	R	0x0	PL_PWR_VAL PL_Port Power Value If PL_Port Power Source select VCC_IO, this bit is invalid

8.5.7.40 0x0350 GPIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: GPIO_POW_VAL_SET_CTL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x1	VCC_PF_PWR_VOL_SEL VCC_PF Power Voltage Select Control 0: 1.8V 1: 3.3V

8.6 LEDC

8.6.1 Overview

The LEDC is used to control the external LED lamp.

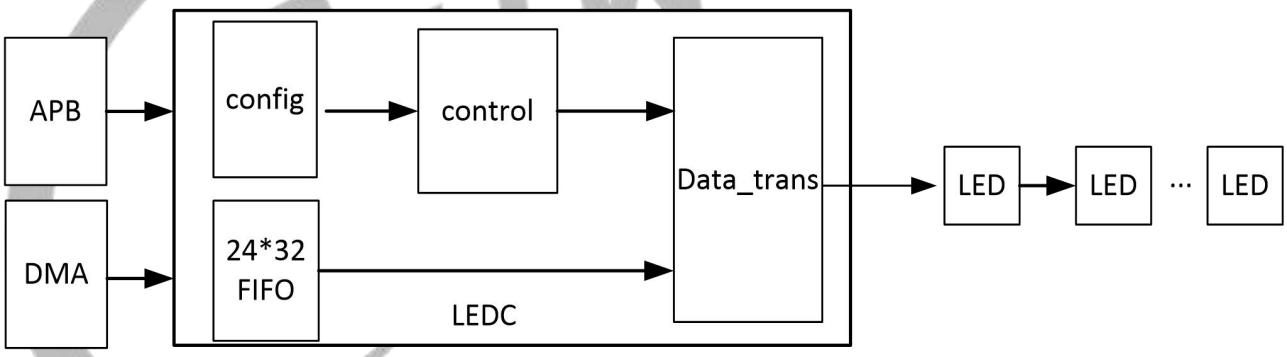
The LEDC has the following features:

- Configurable LED output high-/low-level width
- Configurable LED reset time
- Configurable interval time for packets and frame data
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s
- Configurable RGB display mode

8.6.2 Block Diagram

The following figure shows a block diagram of the LEDC.

Figure 8-24 LEDC Block Diagram



LEDC contains the following sub-blocks:

Table 8-22 LEDC Sub-blocks

Sub-block	Description
config	register configuration
control	LEDC timing control and status control
FIFO	24-bit width x 32 depth
Data_trans	Convert input data to the 0 and 1 characters of LED

8.6.3 Functional Description

8.6.3.1 External Signals

The following table describes the external signals of the LEDC.

Table 8-23 LEDC External Signals

Signal Name	Description	Type
LEDC	Intelligent Control LED Signal Output	O

8.6.3.2 Clock Sources

The following table describes the clock sources of the LEDC.

Table 8-24 LEDC Clock Sources

Clock Sources	Description	module
HOSC	24 MHz	CCU
PERI0_600M	Peripheral Clock. The default value is 600 MHz	

8.6.3.3 Reset

The following table describes the reset of the LEDC.

Table 8-25 LEDC Reset

Reset signal	Source
LEDC_RST	CCU

8.6.3.4 LEDC Timing

Figure 8-25 LEDC Package Output Timing Diagram

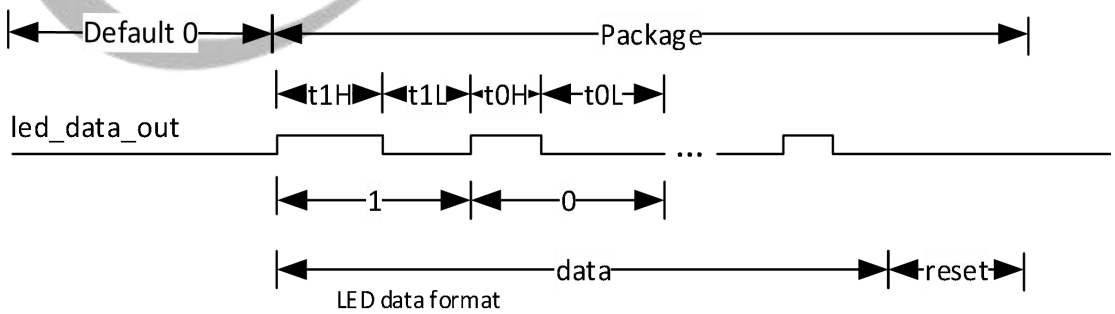


Figure 8-26 LEDC 1-frame Output Timing Diagram

8.6.3.5 LEDC Input Data Structure

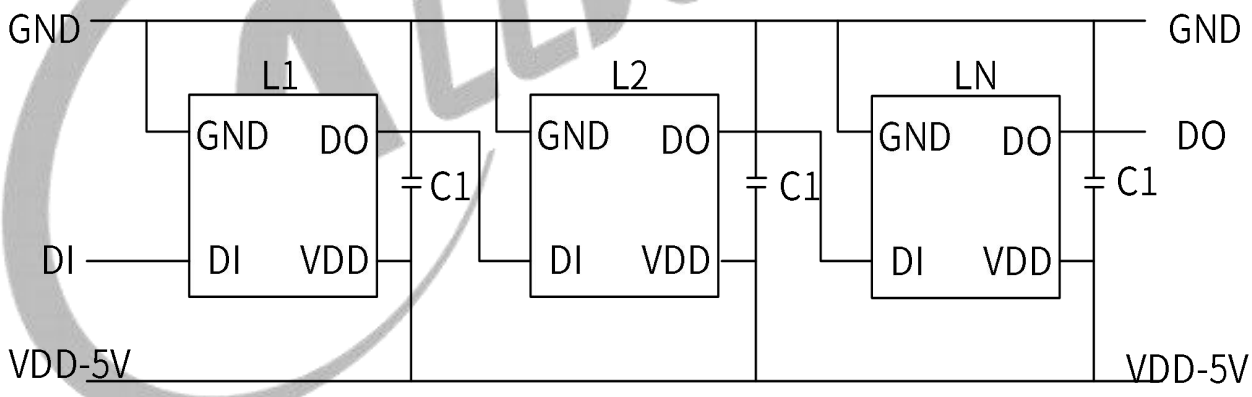
The RGB mode of LEDC data is configurable. By default, the data is sent in GRB order, and the higher bit is transmitted first.

Figure 8-27 LEDC Input Data Structure

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0

8.6.3.6 LEDC Typical Circuit

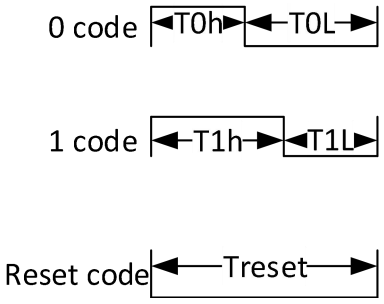
Figure 8-28 LEDC Typical Circuit



C1 is the filter capacitor of LED light, and its value is usually 100 Nf.

8.6.3.7 LEDC Data Input Code

Figure 8-29 LEDC Data Input Code



8.6.3.8 LEDC Data Transfer Time

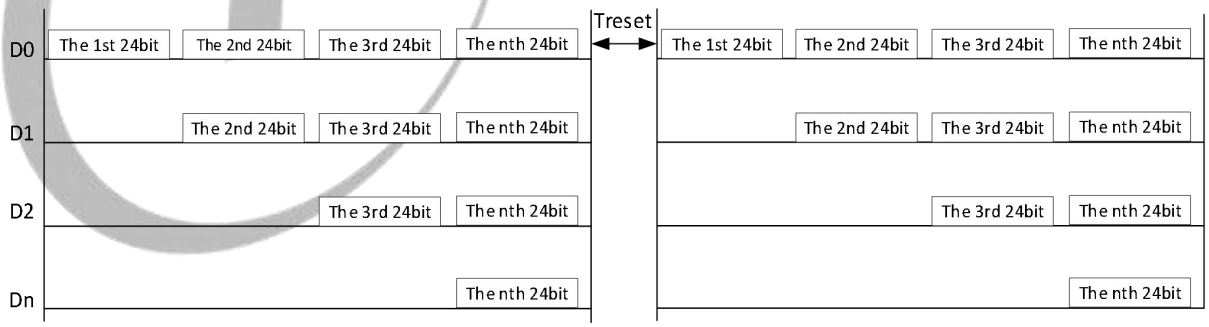
The time parameter of the typical LED specification shows as follows.

Table 8-26 Time Parameters of Typical LED Specification

T0H	0 code, high-level time	220 ns to 380 ns
T0L	0 code, low-level time	580 ns to 1.6 us
T1H	1 code, high-level time	580 ns to 1.6 us
T1L	1 code, low-level time	220 ns to 420 ns
RESET	Frame unit, low-level time	> 280 us

8.6.3.9 LEDC Data Transfer Mode

Figure 8-30 LEDC Data Transfer Mode



8.6.3.10 LEDC Parameter

- PAD rate > 800 kbit/s
- LED number supported: $T_{0\text{-}code}$: 800 ns to 1980 ns, $T_{1\text{-}code}$: 800 ns to 2020 ns

When the LED refresh rate is 30 frame/s, LED number supported is (1 s/30-280 us)/ ((800 ns to 2020 ns) *24) =1023 to 681.

When the LED refresh rate is 60 frame/s, LED number supported is (1 s/60-280 us)/ ((800 ns to 2020 ns) *24) =853 to 337.

8.6.3.11 LEDC Data Transfer

The LEDC supports DMA data transfer mode or CPU data transfer mode. The DMA data transfer mode is set by LEDC_DMA_EN

- Data transfer in DMA mode

When the valid space of internal FIFO is greater than the setting FIFO free space threshold, the LEDC sends DMA_REQ to require DMA to transfer data from DRAM to LEDC. The maximum data transfer size in DMA mode is 16 words. (The internal FIFO level is 32.)

- Data transfer in CPU mode

When the valid space of internal FIFO is greater than the setting FIFO free space threshold, the LEDC sends LEDC_CPUREQ_INT to require CPU to transfer data to LEDC. The transfer data size in CPU mode is controlled by software. The internal FIFO destination address is 0x06700014. The data width is 32-bit. (The lower 24-bit is valid.)

8.6.3.12 LEDC Interrupt

Module Name	Description
FIFO_OVERFLOW_INT	FIFO overflow interrupt. The data written by external is more than the maximum storage space of LED FIFO, the LEDC will be in data loss state. At this time, software needs to deal with the abnormal situation. The processing mode is as follows. The software can query LED_FIFO_DATA_REG to determine which data has been stored in the internal FIFO of LEDC. The LEDC performs soft_reset operation to refresh all data.
FIFO_CPUREQ_INT	FIFO request CPU data interrupt When FIFO data is less than a threshold, the interrupt will be reported to the CPU.
LEDC_TRANS_FINISH_INT	Data transfer complete interrupt The value indicates that the data configured as total_data_length has been transferred completely.

LEDC interrupt usage scenario:

- CPU mode

The software can enable GLOBAL_INT_EN, FIFO_CPUREQ_INT_EN, WAITDATA_TIMEOUT_INT_EN, FIFO_OVERFLOW_INT_EN, LEDC_TRANS_FINISH_INT_EN, and cooperate with LEDC_FIFO_TRIG_LEVEL to use. When FIFO_CPUREQ_INT is set to 1, the software can configure data of LEDC_FIFO_TRIG_LEVEL to LEDC.

- DMA mode

The software can enable GLOBAL_INT_EN, WAITDATA_TIMEOUT_INT_EN, FIFO_OVERFLOW_INT_EN, LEDC_TRANS_FINISH_INT_EN, and cooperate with

LEDC_FIFO_TRIG_LEVEL to use. When DMA receives LEDC DMA_REQ, DMA can transfer data of LEDC_FIFO_TRIG_LEVEL to LEDC.

8.6.4 Programming Guidelines

8.6.4.1 LEDC Normal Configuration Process

Step 1 Configure LEDC_CLK and bus pclk.

Step 2 Configure the written LEDC data.

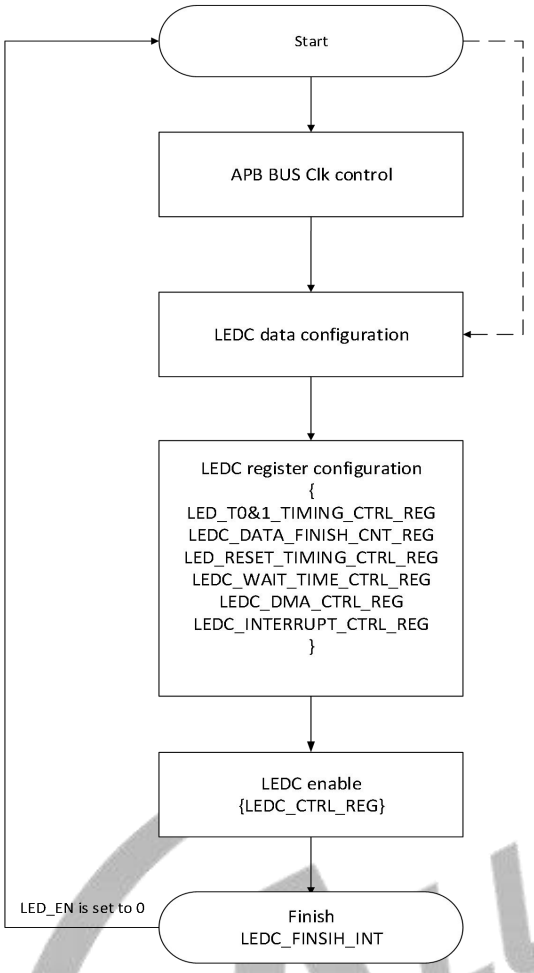
Step 3 Configure LED_T01_TIMING_CTRL_REG, LEDC_DATA_FINISH_CNT_REG, LED_RESET_TIMING_CTRL_REG, LEDC_WAIT_TIME0_CTRL_REG, LEDC_DMA_CTRL_REG, LEDC_INTERRUPT_CTRL_REG. Configure 0-code, 1-code, reset time, LEDC waiting time, and the number of external connected LEDC and the threshold of DMA transfer data.

Step 4 Configure LEDC_CTRL_REG to enable LEDC_EN, the LEDC will start to output data.

Step 5 When the LEDC interrupt is pulled up, it indicates the configured data has transferred complete, at this time LED_EN will be set to 0, and the read/write point of LEDC FIFO is cleared to 0.

Step 6 Repeat step1, 2, 3, 4 to re-execute a new round of configuration, enable LEDC_EN, the LEDC will start new data transfer.

Figure 8-31 LEDC Normal Configuration Process



8.6.4.2 LEDC Abnormal Scene Processing Flow

WAITDATA_TIMEOUT Abnormal Status

Step 1 When WAITDATA_TIMEOUT_INT appears, it indicates the internal FIFO data request of LEDC cannot obtain a response, at this time if the default output level is low, then the external LED may think there was a reset operation and cause LED data to be flushed incorrectly.

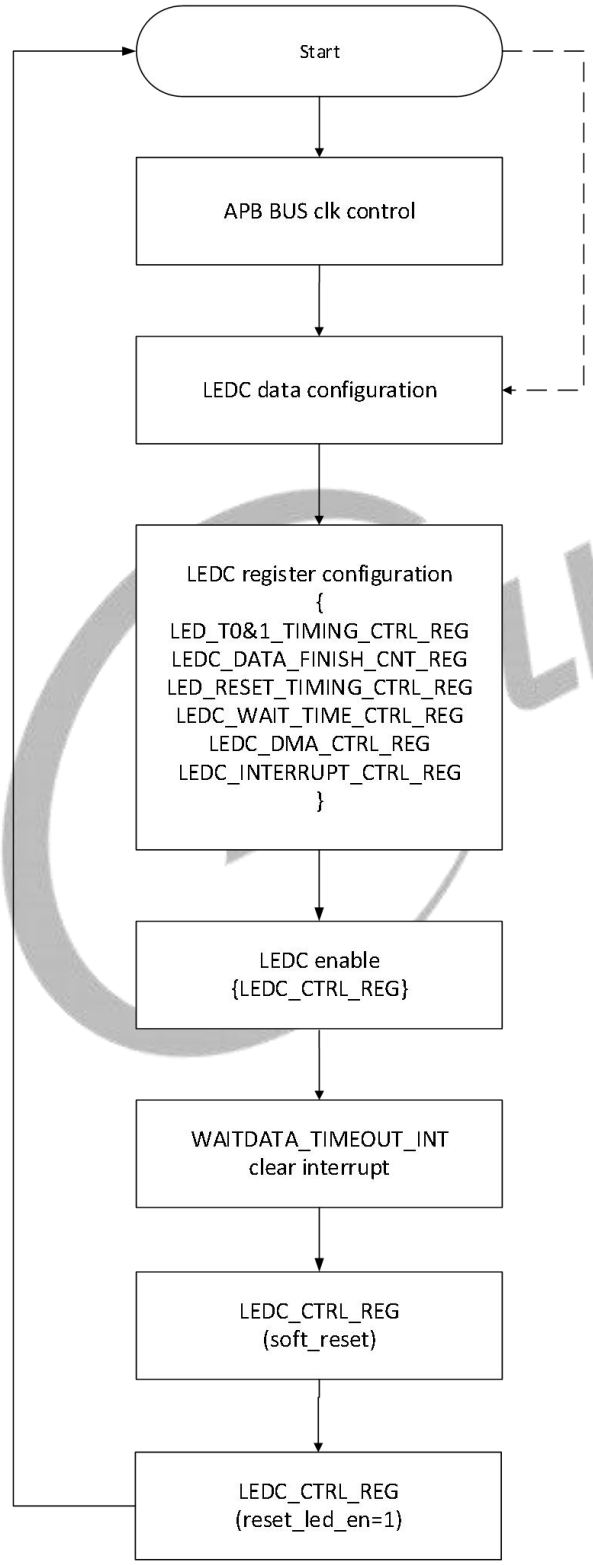
Step 2 The LEDC needs to be performed soft_reset operation (LEDC_SOFT_RESET=1); after soft_reset, the LEDC_EN will be pulled-down automatically, all internal status register and control state machine will return to the idle state, the LEDC FIFO read & write point is cleared to 0, the LEDC interrupt is cleared.

Step 3 Setting reset_led_en to 1 indicates LEDC can actively send a reset operation to ensure the external LED lamp in the right state.

Step 4 The software reads the status of reset_led_en, when the status value is 1, it indicates LEDC does not perform the transmission of LED reset operation; when the status value is 0, the LEDC completes the transmission of LED reset operation.

Step 5 When LEDC reset operation finishes, the LEDC data and register configuration need to be re-operated to start re-transmission data operation.

Figure 8-32 LEDC Timeout Abnormal Processing Flow



FIFO Overflow Abnormal Status

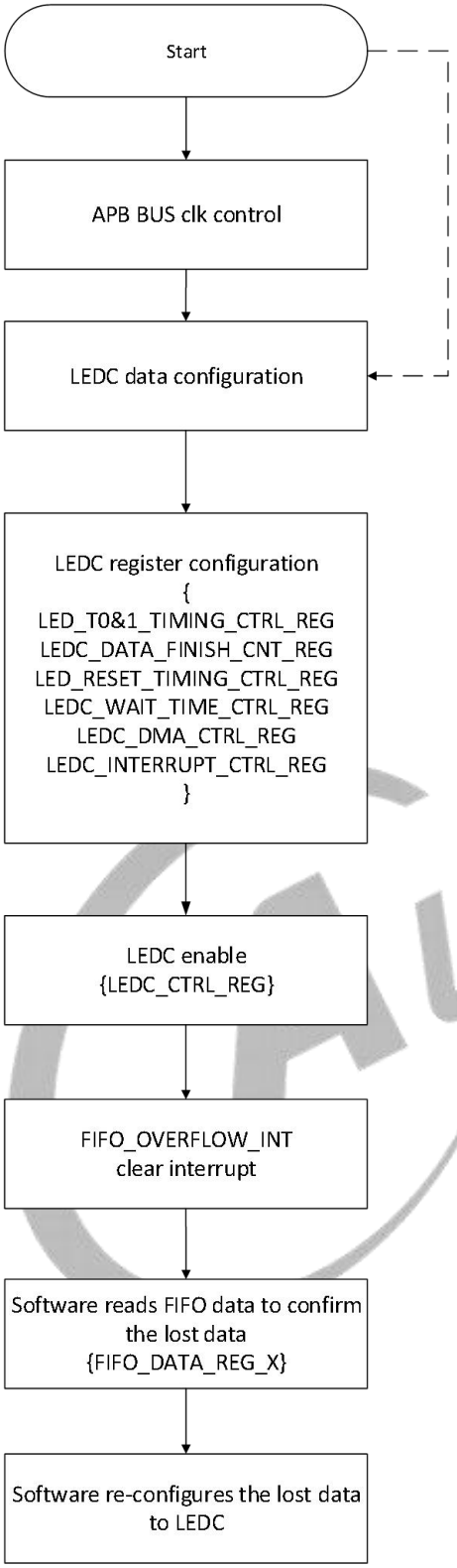
Step 1 When FIFO_OVERFLOW_INT appears, it indicates the data configured by software exceeds the LEDC FIFO space, at this time the redundant data will be lost.

Step 2 The software needs to read data in LEDC_FIFO_DATA_X to confirm the lost data.

Step 3 The software re-configures the lost data to the LEDC.

Step 4 If the software uses the soft_reset operation, the operation is the same with the timeout abnormal processing flow.

Figure 8-33 FIFO Overflow Abnormal Processing Flow



8.6.5 Register List

Module Name	Base Address
LEDC	0x02008000

Register Name	Offset	Description
LEDC_CTRL_REG	0x0000	LEDC Control Register
LED_T01_TIMING_CTRL_REG	0x0004	LEDC T0 & T1 Timing Control Register
LEDC_DATA_FINISH_CNT_REG	0x0008	LEDC Data Finish Counter Register
LED_RESET_TIMING_CTRL_REG	0x000C	LEDC Reset Timing Control Register
LEDC_WAIT_TIME0_CTRL_REG	0x0010	LEDC Wait Time0 Control Register
LEDC_DATA_REG	0x0014	LEDC Data Register
LEDC_DMA_CTRL_REG	0x0018	LEDC DMA Control Register
LEDC_INT_CTRL_REG	0x001C	LEDC Interrupt Control Register
LEDC_INT_STS_REG	0x0020	LEDC Interrupt Status Register
LEDC_WAIT_TIME1_CTRL_REG	0x0028	LEDC Wait Time1 Control Register
LEDC_FIFO_DATA_REG	0x0030+0x04 *N	LEDC FIFO Data Register

8.6.6 Register Description

8.6.6.1 0x0000 LEDC Control Register (Default Value: 0x0000_003C)

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	TOTAL_DATA_LENGTH Total length of transfer data (range: 0 to 8K, unit: 32-bit, only low 24-bit is valid) The field is recommended to be set to an integer multiple of (LED_NUM+1). If TOTAL_DATA_LENGTH is greater than (LED_NUM+1), but non-integer multiple, the last frame of data will transfer data less than (LED_NUM+1).
15:11	/	/	/
10	R/WAC	0x0	RESET_LED_EN Write operation: The software writes 1 to the bit, the CPU triggers LEDC to transfer a reset to LED. Only when LEDC is in IDLE status, the reset can be performed. After the reset finished, the control state machine returns to the IDLE status. To return LEDC to the IDLE status, it also needs to be used with SOFT_RESET.

<table>
<tr><td colspan="3">Offset: 0x0000</td><td>Register Name: LEDC_CTRL_REG</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>When the software sets the bit, the software can read the bit to check if the reset is complete.
Read operation:
0: LEDC completes the transmission of the LED reset operation
1: LEDC does not complete the transmission of the LED reset operation</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8:6</td><td>R/W</td><td>0x0</td><td>LED_RGB_MODE
000 GRB (bypass)
001 GBR
010 RGB
011 RBG
100 BGR
101 BRG
By default, the software configures data to LEDC according to GRB (MSB) mode, the LEDC internal combines data to output to the external LED.
Other modes configure as follows.
<table>
<tr><td>Software Input Mode</td><td>Configuration</td><td>LEDC Output Mode</td></tr>
<tr><td rowspan="6">GRB</td><td>000</td><td>GRB</td></tr>
<tr><td>001</td><td>GBR</td></tr>
<tr><td>010</td><td>RGB</td></tr>
<tr><td>011</td><td>RBG</td></tr>
<tr><td>100</td><td>BGR</td></tr>
<tr><td>101</td><td>BRG</td></tr>
<tr><td rowspan="6">GBR</td><td>000</td><td>GBR</td></tr>
<tr><td>001</td><td>GRB</td></tr>
<tr><td>010</td><td>BGR</td></tr>
<tr><td>011</td><td>BRG</td></tr>
<tr><td>100</td><td>RGB</td></tr>
<tr><td>101</td><td>RBG</td></tr>
<tr><td rowspan="6">RGB</td><td>000</td><td>RGB</td></tr>
<tr><td>001</td><td>RBG</td></tr>
<tr><td>010</td><td>GRB</td></tr>
<tr><td>011</td><td>GBR</td></tr>
<tr><td>100</td><td>BRG</td></tr>
<tr><td>101</td><td>BGR</td></tr>
<tr><td>RBG</td><td>000</td><td>RBG</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0000</td><td colspan="3">Register Name: LEDC_CTRL_REG</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td colspan="3">Description</td></tr>
<tr><td></td><td></td><td></td><td colspan="3"><table>
<tr><td rowspan="5"></td><td>001</td><td>RGB</td></tr>
<tr><td>010</td><td>BRG</td></tr>
<tr><td>011</td><td>BGR</td></tr>
<tr><td>100</td><td>GRB</td></tr>
<tr><td>101</td><td>GBR</td></tr>
<tr><td rowspan="6">BGR</td><td>000</td><td>BGR</td></tr>
<tr><td>001</td><td>BRG</td></tr>
<tr><td>010</td><td>GBR</td></tr>
<tr><td>011</td><td>GRB</td></tr>
<tr><td>100</td><td>RBG</td></tr>
<tr><td>101</td><td>RGB</td></tr>
<tr><td rowspan="6">BRG</td><td>000</td><td>BRG</td></tr>
<tr><td>001</td><td>BGR</td></tr>
<tr><td>010</td><td>RBG</td></tr>
<tr><td>011</td><td>RGB</td></tr>
<tr><td>100</td><td>GBR</td></tr>
<tr><td>101</td><td>GRB</td></tr>
</table></td></tr>
<tr><td>5</td><td>R/W</td><td>0x1</td><td colspan="3">LED_MSB_TOP
Adjust sequence of the combined GRB data
0: LSB
1: MSB</td></tr>
<tr><td>4</td><td>R/W</td><td>0x1</td><td colspan="3">LED_MSB_G
MSB control for Green data
0: LSB
1: MSB</td></tr>
<tr><td>3</td><td>R/W</td><td>0x1</td><td colspan="3">LED_MSB_R
MSB control for Red data
0: LSB
1: MSB</td></tr>
<tr><td>2</td><td>R/W</td><td>0x1</td><td colspan="3">LED_MSB_B
MSB control for Blue data
0: LSB
1: MSB</td></tr>
<tr><td>1</td><td>R/W1C</td><td>0x0</td><td colspan="3">LEDC_SOFT_RESET
LEDC soft reset
Write 1 to clear it automatically.
The ranges of LEDC soft reset include the following points: all internal status registers, the control state machine returns to in idle status, the LEDC FIFO read & write point is cleared to 0, the LEDC interrupt is cleared; and the affected registers are followed.</td></tr>
</table>

Offset: 0x0000			Register Name: LEDC_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			1.LEDC_CTRL_REG (LEDC_EN is cleared to 0); 2. PLL_T0&1_TIMING_CTRL_REG remains unchanged; 3. LEDC_DATA_FINISH_CNT_REG (LEDC_DATA_FINISH_CNT is cleared to 0); 4.LED_RESET_TIMING_CTRL_REG remains unchanged; 5. LEDC_WAIT_TIME_CTRL_REG remains unchanged; 6. LEDC_DMA_CTRL_REG remains unchanged; 7. LEDC_INTERRUPT_CTRL_REG remains unchanged; 8.LEDC_INT_STS _REG is cleared to 0; 9. LEDC_CLK_GATING_REG remains unchanged; 10.LEDC_FIFO_DATA_REG remains unchanged;
0	R/W	0x0	LEDC_EN LEDC Enable 0: Disable 1: Enable That the bit is enabled indicates LEDC can be started when LEDC data finished transmission or LEDC_EN is cleared to 0 by hardware in LEDC_SOFT_RESET situation.

8.6.6.2 0x0004 LEDC T0 & T1 Timing Control Register (Default Value: 0x0286_01D3)

Offset: 0x0004			Register Name: LED_T01_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:21	R/W	0x14	T1H_TIME LED T1H time Unit: cycle (24 MHz), t1h_time =42 ns*(N+1) The default value is 882 ns, the range is 80 ns–2560 ns. N: 1–3F. When is 0, t1h_time = 3F
20:16	R/W	0x6	T1L_TIME LED T1L time Unit: cycle (24 MHz), t1l_time =42 ns*(N+1) The default value is 294 ns, the range is 80 ns–1280 ns. N: 1–1F. When is 0, t1l_time = 1F
15:11	/	/	/

Offset: 0x0004			Register Name: LED_T01_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
10:6	R/W	0x7	T0H_TIME LED T0h time Unit: cycle (24 MHz), t0h_time =42 ns*(N+1) The default value is 336 ns, the range is 80 ns–1280 ns. N: 1–1F. When is 0, t0h_time = 1F
5:0	R/W	0x13	T0L_TIME LED T0l time Unit: cycle (24 MHz), t0L_time =42 ns*(N+1) The default value is 840 ns, the range is 80 ns–2560 ns. N: 1–3F. When is 0, t0L_time = 3F

8.6.6.3 0x0008 LEDC Data Finish Counter Register (Default Value: 0x1D4C_0000)

Offset: 0x0008			Register Name: LEDC_DATA_FINISH_CNT_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x1D4C	LED_WAIT_DATA_TIME The value is the time that internal FIFO in LEDC is waiting for data. When the time is exceeded, the LEDC will send the wait_data_timeout_int interrupt. (This is an abnormal situation, software needs to reset LEDC.) The value is about 300 us by default. The adjust range is 80 ns–655 us. led_wait_data_time=42ns*(N+1). N: 1–1FFF. When the field is 0, LEDC_WAIT_DATA_TIME=1FFF
15:13	/	/	/
12:0	R	0x0	LED_DATA_FINISH_CNT The value is the total LED data that have been sent. (Range: 0–8k)

8.6.6.4 0x000C LEDC Reset Timing Control Register (Default Value: 0x1D4C_0000)

Offset: 0x000C			Register Name: LED_RESET_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x1D4C	TR_TIME

Offset: 0x000C			Register Name: LED_RESET_TIMING_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			Reset time control of LED lamp Unit: cycle (24 MHz), tr_time=42 ns*(N+1) The default value is 300 us. The adjust range is 80 ns–327 us. N: 1–1FFF If the value is 0, TR_TIME=1FFF.
15:10	/	/	/
9:0	R/W	0x0	LED_NUM The value is the number of external LED lamp. Maximum up to 1024. The default value 0 indicates that 1 LED lamp is external connected. The range is from 0 to 1023.

8.6.6.5 0x0010 LEDC Wait Time 0 Control Register (Default Value: 0x0000_00FF)

Offset: 0x0010			Register Name: LEDC_WAIT_TIME0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	WAIT_TIM0_EN WAIT_TIME0 enable When it is 1, the controller automatically inserts waiting time between LED package data. 0: Disable 1: Enable
7:0	R/W	0xFF	TOTAL_WAIT_TIME0 Waiting time between 2 LED data. The LEDC output is low level. The adjust range is 80 ns–10 us. wait_time0=42 ns*(N+1) Unit: cycle(24 MHz) N: 1–FF

8.6.6.6 0x0014 LEDC Data Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: LEDC_DATA_REG
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	LEDC DATA LED display data (the lower 24-bit is valid)

8.6.6.7 0x0018 LEDC DMA Control Register (Default Value: 0x0000_002F)

Offset: 0x0018			Register Name: LEDC_DMA_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x1	LEDC_DMA_EN LEDC DMA request enable 0: Disable request of DMA transfer data 1: Enable request of DMA transfer data
4:0	R/W	0x0F	LEDC_FIFO_TRIG_LEVEL The remaining space of internal FIFO in LEDC The internal FIFO in LEDC is 24*32. When the remaining space of internal FIFO in LEDC is more than or equal to LEDFIFO_TRIG_LEVEL, the DMA or the CPU request will generate. The default value is 15. The adjusted value is from 1 to 31. The recommended configuration is 7 or 15. When the configuration value is 0, LEDFIFO_TRIG_LEVEL=F.

8.6.6.8 0x001C LEDC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: LEDC_INTERRUPT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	GLOBAL_INT_EN Global interrupt enable 0: Disable 1: Enable
4	R/W	0x0	FIFO_OVERFLOW_INT_EN FIFO overflow interrupt enable When the data written by the software is more than the internal FIFO level of LEDC, the LEDC is in the data loss state. 0: Disable 1: Enable
3	R/W	0x0	WAITDATA_TIMEOUT_INT_EN The internal FIFO in LEDC cannot get data because of some abnormal situation, after the time of led_wait_data_time, the interrupt will be enabled. 0: Disable 1: Enable
2	/	/	/

Offset: 0x001C			Register Name: LEDC_INTERRUPT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
1	R/W	0x0	FIFO_CPUREQ_INT_EN FIFO request CPU data interrupt enable 0: Disable 1: Enable
0	R/W	0x0	LED_TRANS_FINISH_INT_EN Data transmission complete interrupt enable 0: Disable 1: Enable

8.6.6.9 0x0020 LEDC Interrupt Status Register (Default Value: 0x0002_0000)

Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R	0x1	FIFO_EMPTY FIFO empty status flag
16	R	0x0	FIFO_FULL FIFO full status flag
15:10	R	0x0	FIFO_WLW FIFO internal valid data depth It indicates the space FIFO has been occupied.
9:5	/	/	/
4	R/W1C	0x0	FIFO_OVERFLOW_INT FIFO overflow interrupt The data written by external is more than the maximum storage space of LED FIFO, the LEDC will be in the data loss state. At this time, the software needs to deal with the abnormal situation. The processing mode is as follows. The software can query LED_FIFO_DATA_REG to determine which data has been stored in the internal FIFO of LEDC. The LEDC performs soft_reset operation to refresh all data. 0: FIFO not overflow 1: FIFO overflow
3	R/W1C	0x0	WAITDATA_TIMEOUT_INT When internal FIFO of LEDC cannot get data because of some abnormal situation, after led_wait_data_time, the timeout interrupt is set, the LEDC is in WAIT_DATA state; in the course of

Offset: 0x0020			Register Name: LEDC_INT_STS_REG
Bit	Read/Write	Default/Hex	Description
			wait_data, if the new data arrives, the LEDC will continue to send data, at this time software needs to notice whether the waiting time of LEDC exceeds the operation time of reset. If the waiting time of LEDC exceeds the operation time of reset (this is equivalent to reset operation sent by LEDC), the LED may enter in refresh state, the data has not been sent. 0: LEDC not timeout 1: LEDC timeout
2	/	/	/
1	R/W1C	0x0	FIFO_CPUREQ_INT FIFO request CPU data interrupt When FIFO data is less than the threshold, the interrupt will be reported to the CPU. 0: FIFO does not request that CPU transfers data 1: FIFO requests that CPU transfers data
0	R/W1C	0x0	LED_TRANS_FINISH_INT Data transfer complete interrupt The value indicates that the data configured as total_data_length is transferred completely. 0: Data is not transferred completely 1: Data is transferred completely

8.6.6.10 0x0028 LEDC Wait Time 1 Control Register (Default Value: 0x01FF_FFFF)

Offset: 0x0028			Register Name: LEDC_WAIT_TIME1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WAIT_TIM1_EN 0: Disable 1: Enable WAIT_TIME1 enable When the bit is 1, the controller automatically inserts the waiting time between the LED frame data.
30:0	R/W	0x01FFFFFF	TOTAL_WAIT_TIME1 Waiting time between 2 frame data. The LEDC output is low level. The adjust range is 80 ns– 85 s. wait_time1=42 ns*(N+1) Unit: cycle (24 MHz) N: 0x80–0x7FFFFFFF

Offset: 0x0028			Register Name: LEDC_WAIT_TIME1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			If the value is 0, TOTAL_WAIT_TIME1=0x7FFFFFFF

8.6.6.11 0x0030+N*0x04 LEDC FIFO Data Register X (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x04 (N=0–31)			Register Name: LEDC_FIFO_DATA_X
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	LEDC_FIFO_DATA_X Internal FIFO data of LEDC The lower 24-bit is valid.

8.7 Low rate ADC (LRADC)

8.7.1 Overview

The low rate analog-to-digital converter (LRADC) can convert the external signal into a certain proportion of digital value, to realize the measurement of analog signal, which can be applied to power detection and key detection.

The LRADC has the following features:

- 2-ch LRADC input
- 6-bit resolution
- Sampling rate up to 2 KHz
- Supports hold key and general key
- Support normal, continue and single work mode
- Power supply voltage:1.8V, power reference voltage:1.35V

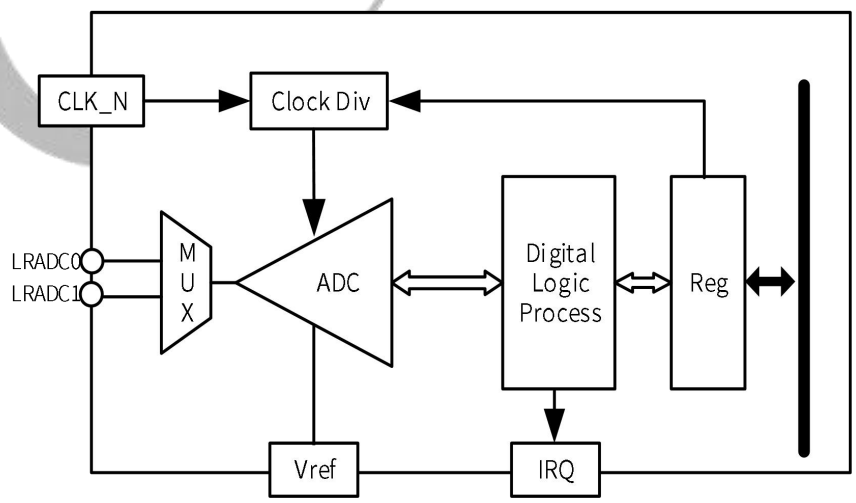
NOTE

The LRADC has a 6-bit resolution, 1-bit offset error, and 1-bit precision error. After the LRADC calibrates 1-bit offset error, the LRADC has 5-bit precision.

8.7.2 Block Diagram

The following figure shows the block diagram of the LRADC.

Figure 8-34 LRADC Block Diagram



8.7.3 Functional Description

8.7.3.1 External Signals

The following table describes the external signals of the LRADC. The LRADC pin is the analog input signal.

Table 8-27 LRADC External Signals

Signal Name	Description	Type
LRADC0	Low Rate ADC	AI
LRADC1	Low Rate ADC	AI

8.7.3.2 Clock Source

The LRADC has one clock source. The following table describes the clock source for LRADC.

Table 8-28 LRADC Clock Sources

Clock Source	Description
LOSC	32.768 kHz LOSC

8.7.3.3 LRADC Working Mode

- Normal Mode

The LRADC gathers 8 samples, the average value of these 8 samples is updated in the data register, and the data interrupt sign is enabled. It is sampled repeatedly according to this mode until the LRADC is disabled.

- Continuous Mode

The LRADC gathers 8 samples every other 8*(N+1) sample cycle. The average value of every 8 samples is updated in the data register, and the data interrupt sign is enabled. (N is defined in the bit [19:16] of LRADC_CTRL).

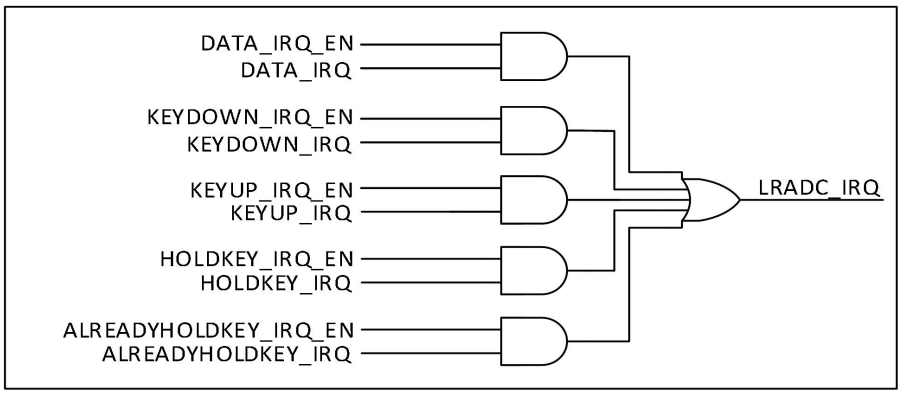
- Single Mode

The LRADC gathers 8 samples, and the average value of these 8 samples is updated in the data register, and the data interrupt sign is enabled at the same time, then the LRADC stops sample.

8.7.3.4 Interrupt

Each LRADC channel has five interrupt sources and five interrupt enable controls.

Figure 8-35 LRADC Interrupt



When the input voltage is between LEVEL A (1.35 V) and LEVEL B (control by the bit [5:4] of LRADC_CTRL), the IRQ1 can be generated. When the input voltage is lower than LEVEL B, the IRQ2 can be generated.

If the controller receives IRQ1 and does not receive IRQ2 at the same time, then the controller will generate Hold Key Pending, otherwise Data IRQ Pending.

The Hold KEY usually is used for the self-locking key. When the self-locking key holds a locking status, the controller receives the IRQ2, then the controller will generate Already Hold Pending.

8.7.3.5 Calculation Formula

Calculation formula: LRADC_DATA = Vin/VREF*63, VREF=1.35 V

8.7.4 Programming Guidelines

8.7.4.1 Normal Detecting

Perform the following steps for normal detecting mode:

Step 1 Configure LRADC_BGR_REG[LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG[LRADC_RST] to 1 to deassert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG[LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 0 to set the normal mode.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

8.7.4.2 Single Detecting

Perform the following steps for the single detecting mode:

Step 1 Configure LRADC_BGR_REG[LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG[LRADC_RST] to 1 to deassert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG[LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 1 to set the single mode.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

8.7.4.3 Continuous Detecting

Perform the following steps for continuous detecting mode:

Step 1 Configure LRADC_BGR_REG[LRADC_GATING] to 0 to disable the clock of LRADC.

Step 2 Configure LRADC_BGR_REG[LRADC_RST] to 1 to deassert the reset of LRADC.

Step 3 Configure LRADC_BGR_REG[LRADC_GATING] to 1 to enable the clock of LRADC.

Step 4 Configure LRADC_CTRL[LRADC_SAMPLE_RATE] to set the appropriate sampling frequency.

Step 5 Configure LRADC_CTRL[LEVELB_VOL] to set the appropriate voltage threshold.

Step 6 Configure LRADC_CTRL[FIRST_CONVER_DLY] and LRADC_CTRL[LEVELA_B_CNT] to set the appropriate debounce value.

Step 7 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 8 Configure LRADC_CTRL[KEY_MODE_SELECT] to 2 to set the continuous mode, and configure LRADC_CTRL[CONTINUE_TIME_SELECT] to set a sampling interval.

Step 9 Configure LRADC_INTC to enable the corresponding interrupt.

Step 10 Configure LRADC_CTRL[LRADC_HOLD_KEY_EN] to 1.

Step 11 Read the corresponding key voltage value from LRADC_DATA when the CPU receives the LRADC interrupt.

8.7.5 Register List

Module Name	Base Address
LRADC	0x02009800

Register Name	Offset	Description
LRADC_CTRL	0x0000	LRADC Control Register
LRADC_INTC	0x0004	LRADC Interrupt Control Register
LRADC_INTS	0x0008	LRADC Interrupt Status Register
LRADC_DATA0	0x000C	LRADC Data Register0
LRADC_DATA1	0x0010	LRADC Data Register1

8.7.6 Register Description

8.7.6.1 0x0000 LRADC Control Register (Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x1	FIRST_CONVERT_DLY ADC First Convert Delay Setting ADC conversion is delayed by n samples.
23:22	R/W	0x0	CHANNEL_SEL Select the channel that be enabled 00: channel 0 only 01: channel 1 only 10: channel 1 and channel 0
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT Continuous Mode Time Select One of 8*(N+1) sample as a valuable sample data.
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	Read/Write	Default/Hex	Description
			Key Mode Select 00: Normal Mode 01: Single Mode 10: Continuous Mode
11:8	R/W	0x1	LEVELA_B_CNT Level A to Level B time threshold select Judge the ADC convert value from level A to level B in n+1 samples.
7	R/W	0x0	LRADC_HOLD_KEY_EN LRADC Hold KEY Enable 0: Disable 1: Enable
6	R/W	0x1	LRADC_CHANNEL_EN LRADC Channel Enable 0: Disable 1: Enable
5:4	R/W	0x2	LEVELB_VOL Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (1.286V) 01: 0x39 (1.221V) 10: 0x36 (1.157V) 11: 0x33 (1.093V)
3:2	R/W	0x2	LRADC_SAMPLE_RATE LRADC Sample Rate 00: 2 kHz 01: 1 kHz 10: 500 Hz 11: 250 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN LRADC Enable 0: Disable 1: Enable

8.7.6.2 0x0004 LRADC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	ADC1_KEYUP_IRQ_EN

Offset: 0x0004			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
			ADC1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN ADC1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC1_HOLD_IRQ_EN ADC1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYDOWN_EN ADC1 Key Down Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN ADC1 Data IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN ADC0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN ADC0 Already Hold Key IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN ADC0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN ADC0 Data IRQ Enable 0: Disable 1: Enable

8.7.6.3 0x0008 LRADC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W1C	0x0	ADC1_KEYUP_PENDING ADC1 Key up pending Bit When general Key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
11	R/W1C	0x0	ADC1_ALRDY_HOLD_PENDING ADC1 Already Hold Pending Bit When hold Key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
10	R/W1C	0x0	ADC1_HOLDKEY_PENDING ADC1 Hold Key Pending Bit When Hold Key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
9	R/W1C	0x0	ADC1_KEYDOWN_PENDING ADC1 Key Down IRQ Pending Bit When General Key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
8	R/W1C	0x0	ADC1_DATA_PENDING ADC1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
			Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
7:5	/	/	/
4	R/W1C	0x0	ADC0_KEYUP_PENDING ADC0 Key up Pending Bit When the general key is pulled up, and the corresponding interrupt is enabled, the status bit is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W1C	0x0	ADC0_ALRDY_HOLD_PENDING ADC0 Already Hold Pending Bit When the hold key is pulled down and the general key is pulled down, and the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC0_HOLDKEY_PENDING ADC0 Hold Key Pending Bit When the hold key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W1C	0x0	ADC0_KEYDOWN_PENDING ADC0 Key Down IRQ Pending Bit When the general key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	ADC0_DATA_PENDING ADC0 Data IRQ Pending Bit

Offset: 0x0008			Register Name: LRADC_INTS
Bit	Read/Write	Default/Hex	Description
			0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

8.7.6.4 0x000C LRADC Data Register (Default Value: 0x0000_003F)

Offset: 0x000C			Register Name: LRADC_DATA0
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x3F	LRADC0_DATA LRADC0 Data

8.7.6.5 0x0010 LRADC Data Register (Default Value: 0x0000_003F)

Offset: 0x0010			Register Name: LRADC_DATA1
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x3F	LRADC1_DATA LRADC1 Data

8.8 USB2.0 DRD

8.8.1 Overview

The USB2.0 dual-role device (USB2.0 DRD) supports both device and host functions which can also be configured as a Host-only or Device-only controller. It complies with the USB2.0 Specification.

For saving CPU bandwidth, the DMA interface of the DRD module can also support the external DMA controller to do the data transfer between the memory and the DRD FIFO. The DRD core also supports USB power saving functions.

The USB2.0 DRD has the following features:

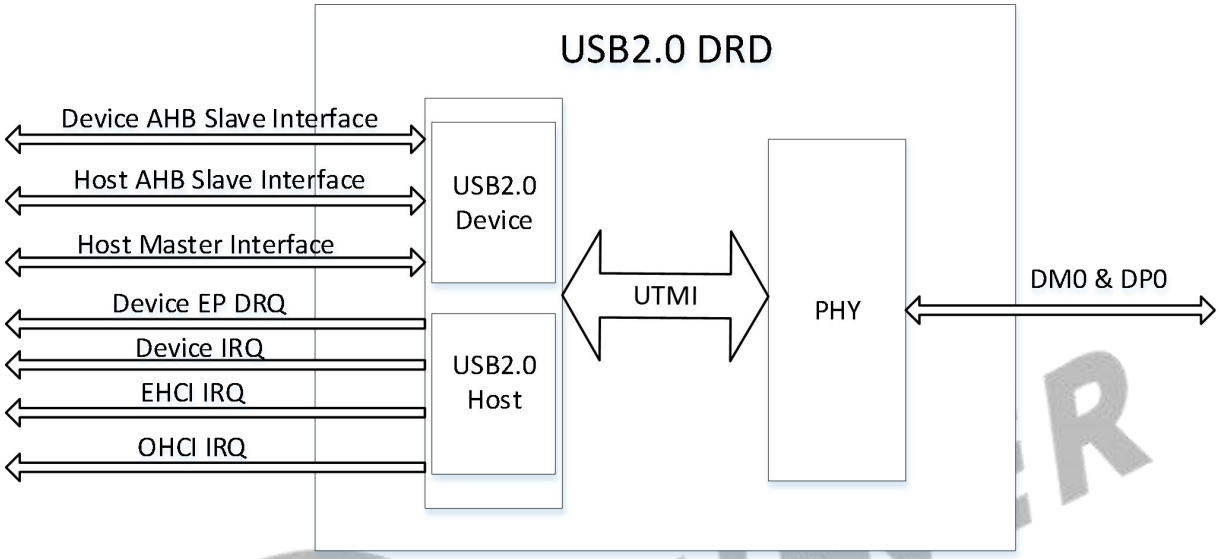
- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- USB Host that supports the following:
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root port shared between EHCI and OHCI
- USB Device that supports the following:
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
  - Supports bi-directional endpoint0 (EP0) for Control transfer
  - Up to 10 user-configurable endpoints (EP1 IN/OUT, EP2 IN/OUT, EP3 IN/OUT, EP4 IN/OUT, EP5 IN/OUT) for Bulk transfer, Isochronous transfer and Interrupt transfer
  - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)
  - Supports interface to an external Normal DMA controller for every EP
- Supports an internal DMA controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral modes
- Includes automatic PING capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities

- Device and host controller share an 8K SRAM and a physical PHY

8.8.2 Block Diagram

The following figure shows the block diagram of USB2.0 DRD Controller.

Figure 8-36 USB2.0 DRD Controller Block Diagram



8.8.3 Functional Description

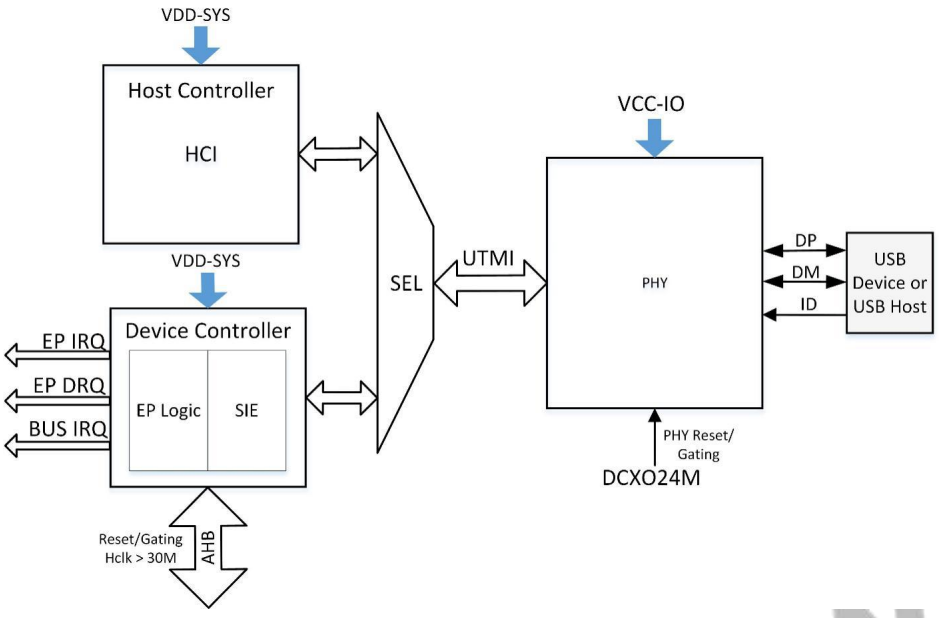
8.8.3.1 External Signals

Table 8-29 USB2.0 DRD External Signals

Signal Name	Description	Type
USB0-DM	USB2.0 Data Signal DM	A I/O
USB0-DP	USB2.0 Data Signal DP	A I/O
USB0-REXT	USB2.0 External Reference Resistor	AO
VCC33-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host	P
VCC33-18-USB	3.3 V/1.8V Analog Power Supply for USB2.0 DRD and USB2.0 Host	P
VDD09-USB	0.9 V USB Digital Power Supply	p

8.8.3.2 Controller and PHY Connection Diagram

Figure 8-37 USB2.0 DRD Controller and PHY Connection Diagram



8.8.4 Register List

There are two groups of registers in USB2.0 DRD.

Module Name	Base Address
USB0 (0x0410 0000---0x041F FFFF)	
USB_DRD_DEVICE	0x04100000
USB_DRD_HOST	0x04101000

8.8.4.1 USB_DRD_DEVICE Register List

Module Name	Base Address
USB_DRD_DEVICE	0x04100000

Register Name	Offset	Description
USB_EPFIFOn	0x0000+N *0x0004 (N=0,1,2,3 ,4,5)	USB FIFO Entry for Endpoint N
USB_GCS	0x0040	USB Global Control and Status Register
USB_EPINTF	0x0044	USB Endpoint Interrupt Flag Register
USB_EPINTE	0x0048	USB Endpoint Interrupt Enable Register
USB_BUSINTF	0x004C	USB Bus Interrupt Flag Register
USB_BUSINTE	0x0050	USB Bus Interrupt Enable Register

Register Name	Offset	Description
USB_FNUM	0x0054	USB Frame Number Register
USB_TESTC	0x007C	USB Test Control Register
USB_CSR0	0x0080	USB EP0 Control and Status Register
USB_TXCSR	0x0080	USB EP1-5 Tx Control and Status Register
USB_RXCSR	0x0084	USB EP1-5 Rx Control and Status Register
USB_COUNT0	0x0088	USB EP0 Rx Counter Register
USB_RXCOUNT	0x0088	USB EP1-5 Rx Counter Register
USB_ATTR0	0x008C	USB EP0 Attribute Register
USB_EPATTR	0x008C	USB EP1-5 Attribute Register
USB_TXFIFO	0x0090	USB EP1-5 TxFIFO Setting Register
USB_RXFIFO	0x0094	USB EP1-5 RxFIFO Setting Register
USB_FADDR	0x0098	USB Function Address Register
USB_ISCR	0x0400	USB Interface Status and Control Register
USB_PHY_CTL	0x0410	USB PHY Control Register
USB_PHY_TEST	0x0414	USB PHY Test Register
USB_PHY_TUNE	0x0418	USB PHY Tune Register
USB_PHY_SEL	0x0420	USB PHY Select Register
USB_PHY_STA	0x0424	USB PHY Status Register
USB_DMA_INTE	0x0500	USB DMA Interrupt Enable Register
USB_DMA_INTS	0x0504	USB DMA Interrupt Status Register
USB_DMA_CHAN_CFG	0x0540+N*0x0010(N=0-7)	USB DMA Channel Configuration Register
USB_DMA_SDRAM_ADD	0x0544+N*0x0010(N=0-7)	USB DMA SDRAM Start Address Register
USB_DMA_BC	0x0548+N*0x0010(N=0-7)	USB DMA Byte Counter Register
USB_DMA_RESIDUAL_BC	0x054C+N*0x0010(N=0-7)	USB DMA RESIDUAL Byte Counter Register

8.8.4.2 USB_DRD_HOST Register List

Module Name	Base Address
USB_DRD_HOST	0x04101000

EHCI

Register Name	Offset	Description
E_CAPLENGTH	0x0000	EHCI Identification Register

Register Name	Offset	Description
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000C	EHCI Companion Port Route Description
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_PERIODICLISTBASE	0x0024	EHCI Periodic Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Current Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status and Control Register

OHCI

Register Name	Offset	Description
O_HcRevision	0x0400	OHCI Revision Register
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register
O_HcHCCA	0x0418	OHCI HCCA Register
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Register
O_HcControlHeadED	0x0420	OHCI Control Head ED Register
O_HcControlCurrentED	0x0424	OHCI Control Current ED Register
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Register
O_HcBulkCurrentED	0x042C	OHCI Bulk Current ED Register
O_HcDoneHead	0x0430	OHCI Done Head Register
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
O_HcRhDescriptorA	0x0448	OHCI Root Hub DescriptorA Register
O_HcRhDesriptorB	0x044C	OHCI Root Hub DescriptorB Register
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register

HCI

Register Name	Offset	Description

Register Name	Offset	Description
USB_CTRL	0x0800	HCI Interface Register
HCI_CTRL3	0x0808	HCI Control 3 Register
PHY_CTRL	0x0810	PHY Control Register
PHY_TEST	0x0814	PHY Test Register
PHY_TUNE	0x0818	PHY Tune Register
PHY_STA	0x0824	PHY Status Register
USB_SPDCR	0x0828	HCI SIE Port Disable Control Register

8.8.5 USB_DRD_Device Register Description

8.8.5.1 0x0000+N*0x04(N=0-5) USB FIFO Entry for Endpoint N (Default Value:0x0000_0000)

Offset: 0x0000+N*0x04(N=0-5)			Register Name: USB_EPFIFOn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	EPnFIFO FIFO Entry for Endpoint n

8.8.5.2 0x0040 USB Global Control and Status Register (Default Value:0x0000_0020)

Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TX_EDMA 1'b0: DMA_REQ signal for all IN Endpoints will be de-asserted when MAXP bytes have been written to and endpoint. This is late mode. 1'b1: DMA_REQ signal for all IN Endpoints will be de-asserted when MAXP-8 bytes have been written to an endpoint. This is early mode.
30	R/W	0	RX_EDMA 1'b0: DMA_REQ signal for all OUT Endpoints will be de-asserted when MAXP bytes have been read to an endpoint. This is late mode. 1'b1: DMA_REQ signal for all OUT Endpoints will be de-asserted when MAXP-8 bytes have been read to and endpoint. This is early mode.
29	/	/	/
28:25	R/W	0	BUS_DRQ_SEL USB DMA Request Signal Source Select 4'b0000: Select TX Endpoint 1 DRQ 4'b0001: Select RX Endpoint 1 DRQ 4'b0010: Select TX Endpoint 2 DRQ

<table>
<tr><th colspan="3">Offset: 0x0040</th><th>Register Name: USB_GCS</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>4’b0011: Select RX Endpoint 2 DRQ
4’b0100: Select TX Endpoint 3 DRQ
4’b0101: Select RX Endpoint 3 DRQ
4’b0110: Select TX Endpoint 4 DRQ
4’b0111: Select RX Endpoint 4 DRQ
4’b1000: Select TX Endpoint 5 DRQ
4’b1001: Select RX Endpoint 5 DRQ</td></tr>
<tr><td>24</td><td>R/W</td><td>0</td><td>FIFO_BUS_SEL
0: CPU bus for FIFO Access,
1: DMA bus for FIFO operation.</td></tr>
<tr><td>23:20</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0x0</td><td>EPIND
Endpoint Index
Index is a 4-bit register that determines which endpoint control/status registers are accessed. Before accessing an endpoint’s control/status registers at 0x0080-0x00BF, the endpoint number should be written to the Index register to ensure that correct control/status registers in the memory map.
Note: The valid value for Index register is 0-5.</td></tr>
<tr><td>15</td><td>R</td><td>0</td><td>BDev
B-Device
0 => ‘A’ device;
1 => ‘B’ device;
Only valid while a session is in progress.
Note: If the core is in Force_Host mode (i.e. a session has been started with USB_TMCTL.7=1), this bit will indicate the state of the HOSTDISCON input signal from the PHY.</td></tr>
<tr><td>14:13</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>12:11</td><td>R</td><td>0x0</td><td>VBus
These bits encode the current VBus level as follows:
<table>
<tr><th>D4</th><th>D3</th><th>Meaning</th></tr>
<tr><td>0</td><td>0</td><td>Below SessionEnd</td></tr>
<tr><td>0</td><td>1</td><td>Above SessionEnd, below AValid</td></tr>
<tr><td>1</td><td>0</td><td>Above AValid, below VBusValid</td></tr>
<tr><td>1</td><td>1</td><td>Above VBusValid</td></tr>
</table></td></tr>
<tr><td>10</td><td>R</td><td>0</td><td>HostMode
Host Mode</td></tr>
</table>

Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
			This bit is set when the USB/DRD is acting as a Host.
9	/	/	/
8	R/W	0	Session When operating as an 'A' device, this bit is set or cleared by the CPU to start or end a session. When operating as an 'B' device, this bit is set/cleared by the USB/DRD when a session starts/ends. It is also set by the CPU to initiate the Session Request Protocol. When the USB/DRD is in Suspend mode, the bit may be cleared by the CPU to perform a software disconnect. **Note: Clearing this bit when the core is not suspending will result in undefined behavior.**
7	R/W	0	IsoUpdateEn Isochronous Update Enable When set by the CPU, the USB/DRD will wait for an SOF token from the Tx packet ready before sending the packet. If an IN token is received before an SOF token, then a zero length data packet will be send. **Note: This bit only affects endpoints performing Isochronous transfer.**
6	R/W	0	SoftConn Soft Connect The USB D+/D- line is enabled when this bit is set by CPU and tri-stated when this bit is cleared by CPU. **Note: Only valid in Peripheral Mode (but not means 'B' Device).**
5	R/W	1	HSEN High-speed Mode Enable When set by CPU, the USB/DRD will negotiate for High-speed mode when the device is reset by host. If not set, the device will only operate in Full-speed mode.
4	R	0	HSFLAG High-speed Mode Flag When set, this read-only bit indicates High-speed mode successfully negotiated during USB reset. And this bit becomes valid when USB Reset completes (as indicated by USB reset interrupt).
3	R	0	Reset

Offset: 0x0040			Register Name: USB_GCS
Bit	Read/Write	Default/Hex	Description
			This bit is set when Reset Signaling is present on the bus.
2	R/W	0	Resume Set by the CPU to generate Resume signaling when the function is in Suspend mode. The CPU should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling.
1	R	0	SuspendM Suspend Mode This bit is set on entry into Suspend mode.
0	R/W	0	SuspendMEn Enable SuspendM Set by the CPU to enable the SUSPENDM output of UTMI+ bus.

8.8.5.3 0x0044 USB Endpoint Interrupt Flag Register (Default Value:0x0000_0000)

Offset: 0x0044			Register Name: USB_EPINTF
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R	0	EP5Rx Rx Endpoint 5 interrupt flag
20	R	0	EP4Rx Rx Endpoint 4 interrupt flag
19	R	0	EP3Rx Rx Endpoint 3 interrupt flag
18	R	0	EP2Rx Rx Endpoint 2 interrupt flag
17	R	0	EP1Rx Rx Endpoint 1 interrupt flag
16:6	/	/	/
5	R	0	EP5Tx Tx Endpoint 5 interrupt flag
4	R	0	EP4Tx Tx Endpoint 4 interrupt flag
3	R	0	EP3Tx Tx Endpoint 3 interrupt flag
2	R	0	EP2Tx Tx Endpoint 2 interrupt flag
1	R	0	EP1Tx

Offset: 0x0044			Register Name: USB_EPINTF
Bit	Read/Write	Default/Hex	Description
			Tx Endpoint 1 interrupt flag
0	R	0	EP0 Endpoint 0 interrupt flag

8.8.5.4 0x0048 USB Endpoint Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0048			Register Name: USB_EPINTE
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0	EP5Rx Rx Endpoint 5 interrupt enable
20	R/W	0	EP4Rx Rx Endpoint 4 interrupt enable
19	R/W	0	EP3Rx Rx Endpoint 3 interrupt enable
18	R/W	0	EP2Rx Rx Endpoint 2 interrupt enable
17	R/W	0	EP1Rx Rx Endpoint 1 interrupt enable
16:6	/	/	/
5	R/W	0	EP5Tx Tx Endpoint 5 interrupt enable
4	R/W	0	EP4Tx Tx Endpoint 4 interrupt enable
3	R/W	0	EP3Tx Tx Endpoint 3 interrupt enable
2	R/W	0	EP2Tx Tx Endpoint 2 interrupt enable
1	R/W	0	EP1Tx Tx Endpoint 1 interrupt enable
0	R/W	0	EP0 Endpoint 0 interrupt enable

8.8.5.5 0x004C USB Bus Interrupt Flag Register (Default Value:0x0000_0000)

Offset: 0x004C			Register Name: USB_BUSINTF
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	VBusError Set when VBus drops below the VBus Valid threshold

Offset: 0x004C			Register Name: USB_BUSINTF
Bit	Read/Write	Default/Hex	Description
			during a session. **Note: Only valid when USB/DRD is 'A' device.**
6	R	0	SessionRequest Set when Session Request signaling has been detected. **Note: Only valid when USB/DRD is 'A' device.**
5	R	0	Disconnect Set in Host mode when a device disconnect is detected. Set in Peripheral mode when a session ends. **Note: Valid at all transaction speeds.**
4	R	0	Connect Set in host mode when a device connection is detected. **Note: Only valid in Host mode. Valid at all transaction speeds.**
3	R	0	SOF Set when a new frame starts.
2	R	0	ResetBabble Reset Set in Peripheral mode when Reset signaling is detected on the bus. Babble Set in Host mode when babble is detected. **Note: Only active after first SOF has been sent.**
1	R	0	Resume Set when Resume signaling is detected on the bus while the USB/DRD is in Suspend mode.
0	R	0	Suspend Set when Suspend signaling is detected on the bus. **Note: Only valid in Peripheral mode.**

8.8.5.6 0x0050 USB Bus Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: USB_BUSINTE
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	VBusError VBusError interrupt enable
6	R/W	0	Session Request Session Request interrupt enable

Offset: 0x0050			Register Name: USB_BUSINTE
Bit	Read/Write	Default/Hex	Description
5	R/W	0	Disconnect Disconnect interrupt enable
4	R/W	0	Connect Connect interrupt enable
3	R/W	0	SOF SOF interrupt enable
2	R/W	0	ResetBabble Reset Reset interrupt enable Babble Babble interrupt enable
1	R/W	0	Resume Resume interrupt enable
0	R/W	0	Suspend Suspend interrupt enable

8.8.5.7 0x0054 USB Frame Number Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: USB_FNUM
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x000	FRNUM Frame Number Hold the last received frame number.

8.8.5.8 0x007C USB Test Control Register (Default Value:0x0000_0000)

NOTE

Only one of Bits 0-6 should be set at any time.

Offset: 0x007C			Register Name: USB_TESTC
Bit	Read/Write	Default/Hex	Description
31:24	/	0	/
23:16	R	/	FSM USB Operation Finite State Machine for Debug
15:11	/	/	/
10	R/W	0	EXTRXACT Extend Rx Active Signal for safe

<table>
<tr><td colspan="3">Offset: 0x007C</td><td>Register Name: USB_TESTC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>9</td><td>R/W</td><td>0</td><td>RESUME_SE0
Resume from SE0 Enable</td></tr>
<tr><td>8</td><td>R/W</td><td>0</td><td>TM1
Test Mode Enable for Simulation.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>Force_Host
The CPU sets this bit to instruct the core to enter Host mode when the Session bit (Bit 0 of USB_DEVCTL) is set, regardless of whether it is connected to any peripheral. The state of the CID input, HostDisconnect and Linestate signals are ignored. The core will then remain in Host mode until the Session bit is cleared, even if a device is disconnected, and if the Force_Host bit remains set, will re-enter Host mode the next time the Session bit is set.
While in this mode, the status if the HOSTDISCON signal from the PHY may be read from bit 7 of the USB_DEVCTL (in 0x0060) register.
The operating speed is determined from the Force_HS and Force_FS bits as follows:
<table>
<tr><td>Force_HS</td><td>Force_FS</td><td>Operating Speed</td></tr>
<tr><td>0</td><td>0</td><td>Low Speed</td></tr>
<tr><td>0</td><td>1</td><td>Full Speed</td></tr>
<tr><td>1</td><td>0</td><td>High Speed</td></tr>
<tr><td>1</td><td>1</td><td>Undefined</td></tr>
</table></td></tr>
<tr><td>6</td><td>W</td><td>0</td><td>FIFO_Access
The CPU sets this bit to transfer the packet in the Endpoint 0 Tx FIFO to the Endpoint 0 Rx FIFO. It is cleared automatically.
Note: Writing ‘0’ to this bit will be ignored.</td></tr>
<tr><td>5</td><td>R/W</td><td>0</td><td>Force_FS
The CPU sets this bit either in conjunction with bit 7 above or to force the USB/DRD into Full-speed mode when it receive a USB reset.</td></tr>
<tr><td>4</td><td>R/W</td><td>0</td><td>Force_HS
The CPU sets this bit either in conjunction with bit 7 above or to force the USB/DRD into High-speed mode when it receive a USB reset.</td></tr>
<tr><td>3</td><td>R/W</td><td>0</td><td>Test_Packet
(High-speed mode) The CPU sets this bit to enter</td></tr>
</table>

Offset: 0x007C			Register Name: USB_TESTC
Bit	Read/Write	Default/Hex	Description
			Test_Packet test mode. In the mode, the USB/DRD repetitively transmits on the bus a 53-byte test packet, the form of which is defined in the Universal Serial Bus Specification Revision 2.0, Section 7.1.20. **Note: The text packet has a fixed format and must be loaded into the Endpoint 0 FIFO before the test mode is entered.**
2	R/W	0	Test_K (High-speed mode) The CPU sets this bit to enter the Test_K test mode. In this mode, the USB/DRD transmits a continuous K on the bus.
1	R/W	0	Test_J (High-speed mode) The CPU sets this bit to enter the Test_J est mode. In this mode, the USB/DRD transmits a continuous J on the bus.
0	R/W	0	Test_SE0_NAK (High-speed mode) The CPU sets this bit to enter the Test_SE0_NAK test mode. In this mode, the USB/DRD remains in High-speed mode but responds to any valid IN token with a NAK.

8.8.5.9 0x0080 USB EP0 Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: USB_CSR0
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	W	0	FlushFIFO The CPU writes a '1' to this bit to flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset, and the TxPktRdy/RxPktRdy bit (below) is cleared. **Note: (i)Writing '0' to this bit is ignored. (ii)Flush FIFO should only be used when TxPktRdy/RxPktRdy is set, at other times, it may cause data to be corrupted.**
23	W	0	ServicedSetupEnd The CPU writes a '1' to this bit to clear the SetupEnd bit. It is cleared automatically.
22	W	0	ServicedRxPktRdy The CPU writes a 1 to this bit to clear the RxPktRdy bit. It is cleared automatically.
21	W	0	SendStall

Offset: 0x0080			Register Name: USB_CSR0
Bit	Read/Write	Default/Hex	Description
			The CPU writes a '1' to this bit to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically. **Note: The FIFO should be flushed before SendStall is set.**
20	R	0	SetupEnd This bit will be set when a control transaction ends before the DataEnd bit has been set. An interrupt will be generated and the FIFO flushed at this time. The bit is cleared by the CPU writing a '1' to the ServicedSetupEnd bit.
19	W	0	DataEnd The CPU sets this bit: When setting TxPktRdy for the last data packet. When clearing RxPktRdy after unloading the last data packet. When setting TxPktRdy for a zero length data packet. It is cleared automatically.
18	R/W	0	SentStall This bit is set when a STALL handshake is transmitted. The CPU should clear this bit.
17	R/W	0	TxPktRdy The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data packet has been transmitted. An interrupt is also generated at this point (if enabled).
16	R	0	RxPktRdy This bit is set when a data packet has been received. An interrupt is generated (if enabled) when this bit is set. The CPU clears this bit by setting the ServicedRxPktRdy bit.
15:0	/	/	/

8.8.5.10 0x0080 USB EP1 to 5 TX Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0	AutoSet If CPU sets this bit, TxPktRdy will be automatically set when data of maximum packet size (value in the

Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
			USB_TXMAXP) is loaded into the Tx FIFO. If a packet of less than the maximum packet size is loaded, then TxPktRdy will have to be set manually. **Note: Should not be set for high-bandwidth Isochronous/Interrupt endpoints.**
30	R/W	0	ISO The CPU sets this bit to enable the Tx endpoint for Isochronous transfers, and clears it to enable the Tx endpoint for Bulk or Interrupt transfers. **Note: This is only has any effect in Peripheral mode. In Host mode, it always returns zero.**
29	R/W	0	Mode The CPU sets this bit to enable the endpoint direction as Tx, and clears the bit to enable it as Rx. **Note: This bit only has any affect where the same endpoint FIFO is used for Tx and Rx transactions.**
28	R/W	0	DMAReqEnab The CPU sets this bit to enable the DMA request for the Tx endpoint.
27	R/W	0	FrcDataTog The CPU sets this bit to force the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This can be used by Interrupt Tx endpoints that are used to communicate rate feedback for Isochronous endpoints.
26	R/W	0	DMAReqMode The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0. **Note: This bit must not be cleared either before or in the same cycle as the above DMAReqEnab bit is cleared.**
25:24	/	/	/
23	R/W	0	IncompTx When the endpoint is being used for high-bandwidth Isochronous/Interrupt transfers, this bit is set to indicate where a large packet has been split into 2 or 3 packets for transmission but insufficient IN tokens have been received to send all the parts. **Note: In anything other than a high-bandwidth transfer, this bit will always return 0. And writing '1'**

Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
			to this bit is ignored.
22	W	0	ClrDataTog The CPU writes a 1 to this bit to reset the endpoint data toggle to 0. It is cleared automatically. **Note: Writing '0' to this bit is ignored.**
21	R/W	0	SentStall This bit is set when a STALL handshake is transmitted. The FIFO is flushed and the TxPktRdy bit is cleared. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
20	R/W	0	SendStall The CPU writes a 1 to this to issue a STALL handshake to an IN token. The CPU clears this bit to terminate the stall condition. **Note: (i)The FIFO should be flushed before SendStall is set. (ii)This bit has no effect where the endpoint is being used for Isochronous transfers.**
19	W	0	FlushFIFO The CPU writes a 1 to this bit to flush the latest packet from the endpoint Tx FIFO. The FIFO pointer is reset, the TxPktRdy bit (below) is cleared and an interrupt is generated. May be set simultaneously with TxPktRdy to abort the packet that is currently being loaded into the FIFO. **Note: (i)Writing '0' to this bit is ignored. (ii)Flush FIFO should only be used when TxPktRdy is set, at other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.**
18	R/W	0	UnderRun The USB sets this bit if an IN token is received when the TxPktRdy bit not set. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
17	R/W	0	FIFONotEmpty The USB sets this bit when there is at least 1 packet in the Tx FIFO. **Note: Writing '1' to this bit is ignored.**
16	R/W	0	TxPktRdy The CPU sets this bit after loading a data packet into the FIFO. It is cleared automatically when a data

Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
			packet has been transmitted. An interrupt is also generated at this point (if enabled). TxPktRdy is also automatically cleared prior to loading a second packet to a double buffered FIFO. **Note: Writing '0' to this bit is ignored.**
15:11	R/W	0x00	PacketCount In the case of Bulk endpoints with the packet splitting option enabled, the Packet Count can be up to 32 and defines the maximum number of USB packets of specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. If the packet splitting option is not enabled, Packet Count is not implemented. For Isochronous/Interrupt endpoints operating in High-speed mode and with the High-bandwidth option enabled, Packet Count may only either 2 or 3 (corresponding to bit 11 or bit 12 set, respectively) and it specifies the maximum number of such transactions that can be take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB/DRD will automatically split any data packet written to the FIFO into up to 2 or 3 USB packet, each containing the specified payload (or less). For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bit 11 and 12 are ignored. **Note: Value for this bits is (Packet Count - 1), but not Packet Count.**
10:0	R/W	0x000	MaximumPayload These bits define the maximum payload (in bytes) transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. **Note: (i) The value written to Maximum Payload (multiplied by Packet Count in the case of high-bandwidth Isochronous/Interrupt transfer) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint, a mismatch could cause**

Offset: 0x0080			Register Name: USB_TXCSR
Bit	Read/Write	Default/Hex	Description
			unexpected result. (ii)The total amount of data represented by the value written to this register (Maximum payload × Packet Count) must not exceed the FIFO size for Tx endpoint, and should not exceed half the FIFO size if double-buffering is required.

8.8.5.11 0x0084 USB EP1 to 5 Rx Control and Status Register (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
31	R/W	0	AutoClear If CPU sets this bit then the RxPktRdy will be automatically cleared when data of maximum packet size (value in the USB_TXMAXP) is unloaded from the Rx FIFO. If a packet of less than the maximum packet size is unloaded, then RxPktRdy will have to be cleared manually. **Note: Should not be set for high-bandwidth Isochronous endpoints.**
30	R/W	0	ISO The CPU sets this bit to enable the Rx endpoint for Isochronous transfers, and clears it to enable the Rx endpoint for Bulk or Interrupt transfers.
29	R/W	0	DMAReqEnab The CPU sets this bit to enable the DMA request for the Rx endpoint.
28	R/W	0	DisNyet_PIDError DisNyet Bulk/Interrupt Transactions: The CPU sets this bit to disable the sending of NYET handshakes. When set, all successfully received Rx packets are ACK'd including at the point at which the FIFO becomes full. **Note: This bit only has any affect in High-speed mode, in which mode it should be set for all Interrupt endpoints.** PIDError ISO Transactions: The core sets this bit to indicate a PID error in the received packet.
27	R/W	0	DMAReqMode The CPU sets this bit to select DMA Request Mode 1 and clears it to select DMA Request Mode 0.

Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
			Note: This bit must not be cleared in the same cycle as the above RxPktRdy(or DMAReqEnab) bit is cleared.
26:25	/	/	/
24	R/W	0	IncompRx This bit will be set in a high-bandwidth Isochronous/Interrupt transfer if the packet received is incomplete. It will be cleared when RxPktRdy is cleared. **Note: (i) Writing '1' to this bit is forbidden. (ii) In anything other than a high-bandwidth transfer, this bit will always return 0.**
23	W	0	ClrDataTog The CPU writes a '1' to this bit to reset the endpoint data toggle to 0. It is cleared automatically. **Note: Writing '0' to this bit is ignored.**
22	R/W	0	SentStall This bit is set when a STALL handshake is transmitted. The CPU should clear this bit. **Note: Writing '1' to this bit is ignored.**
21	R/W	0	SendStall The CPU writes a '1' to this to issue a STALL handshake. The CPU clears this bit to terminate the stall condition. **Note: (i)The FIFO should be flushed before SendStall is set. (ii)This bit has no effect where the endpoint is being used for Isochronous transfers.**
20	W	0	FlushFIFO The CPU writes a '1' to this bit to flush the next packet to be read from the endpoint Rx FIFO. The FIFO pointer is reset and the RxPktRdy bit (below) is cleared. **Note: (i) Writing '0' to this bit is ignored. (ii) Flush FIFO should only be used when RxPktRdy is set, at other times, it may cause data to be corrupted. Also note that, if the FIFO is double-buffered, FlushFIFO may need to be set twice to completely clear the FIFO.**
19	R	0	DataError This bit is set when RxPktRdy is set if the data packet has a CRC or bit-stuff error. It is cleared when

Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
			RxPktRdy is cleared. **Note: This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns zero.**
18	R/W	0	OverRun The USB sets this bit if an OUT token can not be loaded into the Rx FIFO. The CPU should clear this bit. **Note: (i) Writing '1' to this bit is ignored. (ii) This bit is only valid when the endpoint is operating in ISO mode. In bulk mode, it always returns zero.**
17	R	0	FIFOFull The USB sets this bit when no more packets can be loaded into the Rx FIFO.
16	R/W	0	RxPktRdy This bit is set when a data packet has been received. The CPU should clear this bit when the packet has been unloaded from the Rx FIFO. An interrupt is generated when the bit is set. **Note: Writing '1' to this bit is ignored.**
15:11	R/W	0x00	PacketCount In the case of Bulk endpoints with the packet combining option enabled, the Packet Count can be up to 32 and defines the maximum number of USB packets of specified payload which are to be combined into a single data packet within the FIFO. For Isochronous/Interrupt endpoints operating in High-speed mode and with the High-bandwidth option enabled, Packet Count may only either 2 or 3 (corresponding to bit 11 or bit 12 set, respectively) and it specifies the maximum number of such transactions that can be take place in a single microframe. If either bit 11 or bit 12 is non-zero, the USB/DRD will automatically combine the separate USB packets received in any microframe into a single packet within the Rx FIFO. For Isochronous/Interrupt transfers in Full-speed mode or if High-bandwidth is not enabled, bit 11 and 12 are ignored. **Note: Value for this bits is (Packet Count - 1), but not Packet Count.**
10:0	R/W	0x000	MaximumPayload

Offset: 0x0084			Register Name: USB_RXCSR
Bit	Read/Write	Default/Hex	Description
			These bits define the maximum payload (in bytes) transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-speed and High-speed operations. **Note: (i) The value written to Maximum Payload (multiplied by Packet Count in the case of high-bandwidth Isochronous/Interrupt transfer) must match the value given in the wMaxPacketSize field of the Standard Endpoint Descriptor for the associated endpoint, a mismatch could cause unexpected result. (ii) The total amount of data represented by the value written to this register (Maximum payload × Packet Count) must not exceed the FIFO size for OUT endpoint, and should not exceed half the FIFO size if double-buffering is required.**

8.8.5.12 0x0088 USB EP0 Rx Counter Register (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: USB_COUNT0
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0x00	RxCount0 Endpoint 0 Rx Count These bits indicate the number of received data bytes in the Endpoint 0 FIFO. **Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (of USB_CSR0) is set.**

8.8.5.13 0x0088 USB EP1 to 5 Rx Counter Register (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: USB_RXCOUNT
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	RqPktCount Sets the number of packets of size MaxP that are to be transferred in a block transfer. **Note: Only used in Host mode when AutoReq (of**

Offset: 0x0088			Register Name: USB_RXCOUNT
Bit	Read/Write	Default/Hex	Description
			USB_RXCSR) is set. Has no effect in Peripheral mode or AutoReq is not set.
15:13	/	/	/
12:0	R	0x0000	RxCount Endpoint Rx Count These bits hold the number of data bytes in the packet currently in line to be read from the Rx FIFO. If the packet was transmitted as multiple bulk packets, the number given will be for the combined packet. Note: The value returned changes as the FIFO is unloaded and is only valid while RxPktRdy (of USB_RXCSR) is set.

8.8.5.14 0x0090 USB EP1 to 5 TxFIFO Setting Register (Default Value:0x0000_0000)

Offset: 0x0090			Register Name: USB_TXFIFO
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0000	AD AD [12:0] Start address of the endpoint FIFO is in units of 8 bytes, and it equals (AD[12:0]*8).
15:5	/	/	/
4	R/W	0	DPB Defines whether double-packet buffering supported. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.
3:0	R/W	0x0	SZ SZ [3:0] Maximum packet size to be allowed for (*before any* splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission) is $2^{(SZ\,[3:0]\,+3)}$ bytes, and the valid values for SZ [3:0] are 0x0–0x09. If DPB=0, the FIFO will also this size; if DPB=1, the FIFO will be twice this size.

8.8.5.15 0x0094 USB EP1 to 5 RxFIFO Setting Register (Default Value:0x0000_0000)

Offset: 0x0094	Register Name: USB_RXFIFO

Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0000	AD AD [12:0] Start address of the endpoint FIFO is in units of 8 bytes, and it equals (AD[12:0]*8).
15:5	/	/	/
4	R/W	0	DPB Defines whether double-packet buffering supported. When '1', double-packet buffering is supported. When '0', only single-packet buffering is supported.
3:0	R/W	0x0	SZ SZ [3:0] Maximum packet size to be allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission) is $2^{(SZ\ [3:0]\ +3)}$ bytes, and the valid values for SZ [3:0] are 0x0–0x09. If DPB=0, the FIFO will also this size; if DPB=1, the FIFO will be twice this size.

8.8.5.16 0x0098 USB Function Address Register (Default Value:0x0000_0000)

Offset: 0x0098			Register Name: USB_FADDR
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	RW	0x00	FADDR The function address in peripheral mode. This field is reset to zero after a USB bus reset, and should be updated by software after Set_Address Command during USB enumeration.

8.8.5.17 0x0400 USB Interface Status and Control Register (Default Value:0x0000_0000)

Offset: 0x0400			Register Name: USB_ISCR
Bit	Read/Write	Default/Hex	Description
31	/	0	/
30	R	-	VBUSLS USB VBUS Valid Status detected from Line State
29	R	-	VBUSEX USB VBUS Valid Status detected from external VBUS input
28	R	-	IDEX

Offset: 0x0400			Register Name: USB_ISCR
Bit	Read/Write	Default/Hex	Description
			USB ID Status detected from external ID input
27:26	R	-	LS USB Line Status [27]—DM [26]—DP
25	R	-	VBUS USB VBUS Status merged from both internal and external
24	R	-	ID USB ID Status merged from both internal and external
23:18	/	0	/
17	R/W	0	IDPullupEn ID pull up enable 0: disable 1: enable ID pull up
16	R/W	0	DataPullupEn DP/DM pull up enable 0: DP/DM pull up disable 1: DP/DM pull up enable
15:14	R/W	0	ForceID Force ID 0x: use external ID Status 10: force ID to LOW 11: force ID to HIGH
13:12	R/W	0	ForceVBUS Force VBUS Valid 0x: use external VBUS Valid Status from VBUS Input or Line State 10: Force VBUS Valid to LOW 11: Force VBUS Valid to HIGH
11:10	R/W	0	VBUSSEL External VBUS Valid Source Select 0x: External VBUS Valid detected from VBUS Input 10: External VBUS Valid detected from DP/DM Input 11: External VBUS Valid detected from either VBUS or DP/DM input
9:8	/	0	/
7	R/W	0	WakeupEn USB Wakeup Enable 0: Disable

Offset: 0x0400			Register Name: USB_ISCR
Bit	Read/Write	Default/Hex	Description
			1: Enable
6	R/W	0	VBUSCDS VBUS Input Change Detect Status This bit is set by hardware after VBUS input changed when VBUS change detect is enable. Writing '1' will clear this bit.
5	R/W	0	IDCDS ID Input Change Detect Status This bit is set by hardware after ID input changed when ID change detect is enable. Writing '1' will clear this bit.
4	R/W	0	DATACDS DP/DM Input Change Detect Status This bit is set by hardware after DP/DM input changed when DP/DM change detect is enable. Writing '1' will clear this bit.
3	R/W	0	WakeupIE USB Wakeup IRQ Enable 1: Enable USB Wakeup IRQ 0: Disable USB Wakeup IRQ If this bit is set to zero, an USB wakeup event (VBUS/ID/DP/DM change) will generate an USB wakeup request to wakeup the system, but not generate an USB wakeup IRQ to CPU.
2	R/W	0	VBUSCDE VBUS Input Change Detect enable 0: Disable; 1: Enable
1	RW	0	IDCDE ID Input Change Detect enable 0: Disable; 1: Enable
0	R/W	0	DATACDE DP/DM Input Change Detect enable 0: Disable; 1: Enable

8.8.5.18 0x0410 USB PHY Control Register (Default Value:0x0000_0008)

Offset: 0x0410			Register Name: USB_PHY_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	VREGBYPASS
7	R/W	0	LOOPBACKENB

Offset: 0x0410			Register Name: USB_PHY_CTL
Bit	Read/Write	Default/Hex	Description
6	R/W	0	IDPULLUP
5	R/W	0	VBUSVLDEXT
4	R/W	1	VBUSVLDEXTSEL
3	R/W	1	SIDDQ 1: Write 1 to disable phy. 0: Write 0 to enable phy.
2	R/W	0	COMMONN
1:0	R/W	0	VATESTENB

8.8.5.19 0x0414 USB PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0414			Register Name: USB_PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

8.8.5.20 0x0418 USB PHY Tune Register (Default Value:0x05B3_33D4)

Offset: 0x0418			Register Name: USB_PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.8.5.21 0x0420 USB PHY Select Register (Default Value:0x0000_0001)

Offset: 0x0420			Register Name: USB_PHY_SEL
Bit	Read/Write	Default/Hex	Description
31:1	/	/	Reserved
0	R/W	0x1	OTG_SEL 1: Phy is connected to OTG SIE 0: Phy is connected to HCI SIE

8.8.5.22 0x0424 USB PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0424			Register Name: USB_PHY_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0	TESTDATAOUT

8.8.5.23 0x0500 USB DMA Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0500			Register Name: USB_DMA_INTE
Bit	Read/Write	Default/Hex	Description
31:8	/	/	Reserved
7	R/W	0x0	USB_DMA7_PKG_INT_EN DMA7 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
6	R/W	0x0	USB_DMA6_PKG_INT_EN DMA6 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
5	R/W	0x0	USB_DMA5_PKG_INT_EN DMA5 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
4	R/W	0x0	USB_DMA4_PKG_INT_EN DMA4 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
3	R/W	0x0	USB_DMA3_PKG_INT_EN DMA3 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
2	R/W	0x0	USB_DMA2_PKG_INT_EN

Offset: 0x0500			Register Name: USB_DMA_INTE
Bit	Read/Write	Default/Hex	Description
			DMA2 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
1	R/W	0x0	USB_DMA1_PKG_INT_EN DMA1 Package End Transfer Interrupt Enable 0: Disable 1: Enable.
0	R/W	0x0	USB_DMA0_PKG_INT_EN DMA0 Package End Transfer Interrupt Enable 0: Disable 1: Enable.

8.8.5.24 0x0504 USB DMA Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x0504			Register Name: USB_DMA_INTS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	Reserved
7	R/W	0x0	USB_DMA7_PKG_INT_STA DMA7 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
6	R/W	0x0	USB_DMA6_PKG_INT_STA DMA6 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
5	R/W	0x0	USB_DMA5_PKG_INT_STA DMA5 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
4	R/W	0x0	USB_DMA4_PKG_INT_STA DMA4 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
3	R/W	0x0	USB_DMA3_PKG_INT_STA DMA3 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect

Offset: 0x0504			Register Name: USB_DMA_INTS
Bit	Read/Write	Default/Hex	Description
			1: Pending.
2	R/W	0x0	USB_DMA2_PKG_INT_STA DMA2 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
1	R/W	0x0	USB_DMA1_PKG_INT_STA DMA1 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.
0	R/W	0x0	USB_DMA0_PKG_INT_STA DMA0 Package End Transfer Interrupt Status. Set 1 to the bit will clean it. 0: No effect 1: Pending.

8.8.5.25 0x0540+N*0x10(N=0-7) USB DMA Channel Configuration Register (Default Value:0x0000_0000)

Offset: 0x0540+N*0x10(N=0-7)			Register Name: USB_DMA_CHAN_CFG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DMA_EN DMA Channel Enable If set to 1, DMA will start the data transfer between the source and the destination. The bit will hold on until the DMA finished. It will be cleared automatically. Set 0 to this bit will stop the corresponding DMA channel and reset its state machine.
30:27	/	/	/
26:16	R/W	0x0	DMA_BST_LEN DMA Burst Length The value setting on this field should be equated to the USB max packet length of the corresponding endpoint.
15:5	/	/	/
4	R/W	0x0	DMA_DIR DMA Transfer Direction 0: SDRAM to USB FIFO 1: USB FIFO to SDRAM
3:0	R/W	0x0	DMA_FOR_EP

Offset: 0x0540+N*0x10(N=0-7)			Register Name: USB_DMA_CHAN_CFG
Bit	Read/Write	Default/Hex	Description
			DMA Channel for Endpoint The Endpoint number setting on this field selects the DMA channel for the corresponding endpoint.

8.8.5.26 0x0544+N*0x10(N=0-7) USB DMA SDRAM Start Address Register (Default Value:0x0000_0000)

Offset: 0x0544+N*0x10(N=0-7)			Register Name: USB_DMA_SDRAM_ADD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMA_SDRAM_STR_ADDR DMA SDRAM Start Address The SDRAM start address for the DMA channel transfer between the SDRAM and USB FIFO.

8.8.5.27 0x0548+N*0x10(N=0-7) USB DMA Byte Counter Register (Default Value:0x0000_0000)

Offset: 0x0548+N*0x10(N=0-7)			Register Name: USB_DMA_BC
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	DMA_BC DMA Byte Counter

8.8.5.28 0x054C+N*0x10(N=0-7) USB DMA RESIDUAL Byte Counter Register (Default Value:0x0000_0000)

Offset: 0x054C+N*0x10(N=0-7)			Register Name: USB_DMA_RESIDUAL_BC
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R/W	0x0	DMA_RESIDUAL_BC DMA Residual Byte Counter This field contains the residual byte count in current transfer.

8.8.6 EHCI Register Description

8.8.6.1 0x0000 EHCI Identification Register (Default Value:0x10)

Offset:0x0000			Register Name: E_CAPLENGTH
Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to

Offset:0x0000			Register Name: E_CAPLENGTH
Bit	Read/Write	Default/Hex	Description
			register base to find the beginning of the Operational Register Space.

8.8.6.2 0x0002 EHCI Host Interface Version Number Register (Default Value:0x0100)

Offset: 0x0002			Register Name: E_HCIVERSION
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0100	HCIVERSION This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.8.6.3 0x0004 EHCI Host Control Structural Parameter Register (Default Value:0x0000_1101)

Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R	0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	1	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	1	Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0	Port Routing Rules

Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
			This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value: 0 — Meaning: The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. Value: 1 — Meaning: The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. This field will always be '0'.
6:4	/	/	/
3:0	R	1	N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

8.8.6.4 0x0008 EHCI Host Control Capability Parameter Register (Default Value:0x0000_a026)

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R	0xa0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
7:4	R	0x2	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	1	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	1	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

8.8.6.5 0x000C EHCI Companion Port Route Description (Default Value:0x0000_0000)

Offset: 0x000C			Register Name: E_HCSPPORTROUTE
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules

Offset: 0x000C			Register Name: E_HCSPPORTROUTE
Bit	Read/Write	Default/Hex	Description
			field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.8.6.6 0x0010 EHCI USB Command Register (Default Value:0x0008_0b00)

<table>
<tr><td colspan="3">Offset: 0x0010</td><td>Register Name: USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:24</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x08</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table>
<tr><td>Value</td><td>Minimum Interrupt Interval</td></tr>
<tr><td>0x00</td><td>Reserved</td></tr>
<tr><td>0x01</td><td>1 micro-frame</td></tr>
<tr><td>0x02</td><td>2 micro-frame</td></tr>
<tr><td>0x04</td><td>4 micro-frame</td></tr>
<tr><td>0x08</td><td>8 micro-frame(default, equates to 1 MS)</td></tr>
<tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr>
<tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr>
<tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr>
</table>
Any other value in this register yields undefined</td></tr>
</table>

Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
			results. The default value in this field is 0x08. Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.
15:12	/	/	/
11	R	1	Asynchronous Schedule Park Mode Enable(OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.
10	/	/	/
9:8	R	0x3	Asynchronous Schedule Park Mode Count(OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0	Light Host Controller Reset(OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the

<table>
<tr><th colspan="3">Offset: 0x0010</th><th>Register Name: USBCMD</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0</td><td>Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-
Ware must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:
<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0010</td><td>Register Name: USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index
Register should be used for the Frame List Current index. Values mean:
<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr><tr><td>01b</td><td>512 elements(2048byts)</td></tr><tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
<tr><td>1</td><td>R/W</td><td>0</td><td>Host Controller Reset
This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.
When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state.
This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.
Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.</td></tr>
<tr><td>0</td><td>R/W</td><td>0</td><td>Run/Stop
When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively</td></tr>
</table>

Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
			pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

8.8.6.7 0x0014 EHCI USB Status Register (Default Value:0x0000_1000)

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero, then the status of the Asynchronous Schedule is disabled. If this bit is a one, then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero, then the status of the Periodic Schedule is disabled. If this bit is a one, then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0	Reclamation

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
			This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
			system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition (e.g. error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

8.8.6.8 0x0018 EHCI USB Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will

Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
			issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

8.8.6.9 0x001C EHCI Frame Index Register (Default Value:0x0000_0000)

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

Offset: 0x001C			Register Name: E_FRINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It Means that each location of the frame list is accessed 8 times (frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

Offset: 0x001C			Register Name: E_FRINDEX
Bit	Read/Write	Default/Hex	Description
			USBCMD[Frame List Size] / Number Elements / N 00b / 1024 / 12 01b / 512 / 11 10b / 256 / 10 11b / Reserved /

8.8.6.10 0x0024 EHCI Periodic Frame List Base Address Register (Default Value:0x0000_0000)

NOTE

Writes must be Dword Writes.

Offset: 0x0024			Register Name: E_PERIODICLISTBASE
Bit	Read/Write	Default/Hex	Description
31:12	R/W		Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

8.8.6.11 0x0028 EHCI Current Asynchronous List Address Register (Default Value:0x0000_0000)

NOTE

Writes must be Dword Writes.

Offset: 0x0028			Register Name: E_ASYNCLISTADDR
Bit	Read/Write	Default/Hex	Description

Offset: 0x0028			Register Name: E_ASYNCLISTADDR
Bit	Read/Write	Default/Hex	Description
31:5	R/W		Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

8.8.6.12 0x0050 EHCI Configure Flag Register (Default Value:0x0000_0000)

NOTE

This register is not use in the normal implementation.

Offset: 0x0050			Register Name: E_CONFIGFLAG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value / Meaning 0 / Port routing control logic default-routs each port to an implementation dependent classic host controller. 1 / Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

8.8.6.13 0x0054 EHCI Port Status and Control Register (Default Value:0x0000_2000)

NOTE

This register is only reset by hardware or in response to a host controller reset.

Offset: 0x0054	Register Name: E_PORTSC

<table>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>31:22</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>21</td><td>R/W</td><td>0</td><td>Wake on Disconnect Enable(WKDSCNNT_E)
Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>20</td><td>R/W</td><td>0</td><td>Wake on Connect Enable(WKCNNT_E)
Writing this bit to a one enable the port to be sensitive to device connects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0</td><td>Port Test Control
The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow:
<table>
<tr><td>Bits</td><td>Test Mode</td></tr>
<tr><td>0000b</td><td>The port is NOT operating in a test mode.</td></tr>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-1111b</td><td>Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.</td></tr>
<tr><td>15:14</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>13</td><td>R/W</td><td>1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11:10</td><td>R</td><td>0</td><td>Line Status</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0054</td><td>Register Name: E_PORTSC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8</td><td>R/W</td><td>0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit.
Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0054</td><td>Register Name: E_PORTSC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table><tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr><tr><td>0x</td><td>Disable</td></tr><tr><td>10</td><td>Enable</td></tr><tr><td>11</td><td>Suspend</td></tr></table>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
• Software sets the Force Port Resume bit to a zero(from a one).
• Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>6</td><td>R/W</td><td>0</td><td>Force Port Resume
1 = Resume detected/driven on port. 0 = No resume</td></tr>
</table>

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
			(K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0	Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0	Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0	Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
			changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0	Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (Disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0	Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
			current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

8.8.7 OHCI Register Description

8.8.7.1 0x0400 OHCI Revision Register (Default Value:0x10)

Offset: 0x0400				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	/	/	/	/
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

8.8.7.2 0x0404 OHCI Control Register (Default Value:0x0000_0000)

Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported

<table>
<tr><td colspan="3">Offset: 0x0404</td><td colspan="2">Register Name: O_HcControl</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.</td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>InterruptRouting
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt is routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB
<table><tr><td>00b</td><td>USBReset</td></tr><tr><td>01b</td><td>USBResume</td></tr><tr><td>10b</td><td>USBOperational</td></tr><tr><td>11b</td><td>USBSuspend</td></tr></table>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus.
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.
HC enters USBSUSPEND after a software reset, whereas it enters
USBRESET after a hardware reset. The latter also resets the Root
Hub and asserts subsequent reset signaling to downstream ports.</td></tr>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>BulkListEnable
This bit is set to enable the processing of the Bulk list in the next</td></tr>
</table>

Offset: 0x0404				Register Name: O_HcControl
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.
4	R/W	R	0x0	ControlListEnable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
3	R/W	R	0x0	IsochronousEnable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the

<table>
<tr><td colspan="3">Offset: 0x0404</td><td colspan="2">Register Name: O_HcControl</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
<table>
<tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr>
<tr><td>0</td><td>1:1</td></tr>
<tr><td>1</td><td>2:1</td></tr>
<tr><td>2</td><td>3:1</td></tr>
<tr><td>3</td><td>4:1</td></tr>
</table>
The default value is 0x0.</td></tr>
</table>

8.8.7.3 0x0408 OHCI Command Status Register (Default Value:0x0000_0000)

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list.

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

8.8.7.4 0x040C OHCI Interrupt Status Register (Default Value:0x0000_0000)

Offset: 0x040C	Register Name: O_HcInterruptStatus

Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be Incremented.

8.8.7.5 0x0410 OHCI Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Write back Done Head
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Scheduling Overrun

8.8.7.6 0x0414 OHCI Interrupt Disable Register (Default Value:0x0000_0000)

Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Write back Done Head
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Scheduling Overrun

8.8.7.7 0x0418 OHCI HCCA Register (Default Value:0x0000_0000)

Offset: 0x0418				Register Name: O_HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA [31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA [7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

8.8.7.8 0x041C OHCI Period Current ED Register (Default Value:0x0000_0000)

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED [31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.7.9 0x0420 OHCI Control Head ED Register (Default Value:0x0000_0000)

Offset: 0x0420				Register Name: O_HcControlHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		

Offset: 0x0420				Register Name: O_HcControlHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD [31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.7.10 0x0424 OHCI Control Current ED Register (Default Value:0x0000_0000)

Offset: 0x0424				Register Name: HcControlCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED [31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.7.11 0x0428 OHCI Bulk Head ED Register (Default Value:0x0000_0000)

Offset: 0x0428				Register Name: O_HcBulkHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED [31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.7.12 0x042C OHCI Bulk Current ED Register (Default Value:0x0000_0000)

Offset: 0x42C				Register Name: O_HcBulkCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED [31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.7.13 0x0430 OHCI Done Head Register (Default Value:0x0000_0000)

Offset: 0x0430				Register Name: O_HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead [31:4] When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0	R	R	0x0	HcDoneHead [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.8.7.14 0x0434 OHCI Frame Interval Register (Default Value:0x0000_2EDF)

Offset: 0x0434				Register Name: O_HcFmInterval
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its

Offset: 0x0434				Register Name: O_HcFmInterval
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.8.7.15 0x0438 OHCI Frame Remaining Register (Default Value:0x0000_0000)

Offset: 0x0438				Register Name: O_HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

8.8.7.16 0x043C OHCI Frame Number Register (Default Value:0x0000_0000)

Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/
15:0	R	R/W	0x0	FrameNumber This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a

Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

8.8.7.17 0x0440 OHCI Periodic Start Register (Default Value:0x0000_0000)

Offset: 0x0440				Register Name: O_HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 0x2A3F (0x3e67). When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.8.7.18 0x0444 OHCI LS Threshold Register (Default Value:0x0000_0628)

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	/
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.8.7.19 0x0448 OHCI Root Hub DescriptorA Register (Default Value:0x0200_1201)

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 Over-current status is reported collectively for all downstream ports. 1 No overcurrent protection supported.
11	R/W	R	0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 Over-current status is reported collectively for all downstream ports. 1 Over-current status is reported on per-port basis.
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0 All ports are powered at the same time.

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				1 Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
8	R/W	R	0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 Ports are power switched. 1 Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

8.8.7.20 0x044C OHCI Root Hub DescriptorB Register (Default Value:0x0000_0000)

Offset: 0x044C				Register Name: O_HcRhDescriptorB
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the

Offset: 0x044C				Register Name: O_HcRhDescriptorB
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. ... Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. ... Bit15 Device attached to Port #15.

8.8.7.21 0x0450 OHCI Root Hub Status Register (Default Value:0x0000_0000)

Offset: 0x0450				Register Name: O_HcRhStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0	(write)ClearRemoteWakeupEnable Write a '1' clears DeviceRemoteWakeupEnable. Write a '0' has no effect.
30:18	/	/	/	/
17	R/W	R	0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as '0'. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0),

<table>
<tr><td colspan="3">Offset: 0x0450</td><td colspan="2">Register Name: O_HcRhStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>This bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.</td></tr>
<tr><td>15</td><td>R/W</td><td>R</td><td>0x0</td><td>(read)DeviceRemoteWakeupEnable
This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt.
<table><tr><td>0</td><td>ConnectStatusChange is not a remote wakeup event.</td></tr><tr><td>1</td><td>ConnectStatusChange is a remote wakeup event.</td></tr></table>
(write)SetRemoteWakeupEnable
Writing a ‘1’ sets DeviceRemoveWakeupEnable.
Writing a ‘0’ has no effect.</td></tr>
<tr><td>14:2</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>1</td><td>R</td><td>R/W</td><td>0x0</td><td>OverCurrentIndicator
This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal.
If per-port overcurrent protection is implemented this bit is always ‘0’</td></tr>
<tr><td>0</td><td>R/W</td><td>R</td><td>0x0</td><td>(Read)LocalPowerStatus
When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as ‘0’.
(Write)ClearGlobalPower
When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.</td></tr>
</table>

8.8.7.22 0x0454 OHCI Root Hub Port Status Register (Default Value:0x0000_0100)

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortEnableStatus 1 change in PortEnableStatus
16	R/W	R/W	0x0	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If

<table>
<tr><td colspan="3">Offset: 0x0454</td><td colspan="2">Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.
<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>
Note: If the DeviceRemovable[NDP] bit is set, this bit is set only
after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>-</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.
<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls
this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set,</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0454</td><td colspan="2">Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>only
Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.

Note: This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0454</td><td colspan="2">Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>
(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set,</td></tr>
</table>

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 port is disabled 1 port is enabled (write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0 No device connected 1 Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read '1' when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).

8.8.8 HCI Contgroller and PHY Interface Description

8.8.8.1 0x0800 HCI Interface Register (Default Value:0x0000_0000)

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB Standby Clock Sel 0x0: normal mode USB clock as usual 0x1: standby mode USB clock switch to RC 16M clock

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
30:29	/	/	/
28	R	1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0	OHCI count select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time
24	R/W	0	Simulation mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect
23:21	/	/	/
20	R/W	0	EHCI HS force Set 1 to this field force the EHCI enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19	/	/	/
18	R/W	0	1: within 2us of the Resume-K to SE0 transition 0: random time value of the resume-K to SE0 transition
17:13	/	/	/
12	R/W	0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: do not use INCR8,use other enabled INCRX or unspecified length burst INCR
9	R/W	0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: do not use INCR4,use other enabled INCRX or

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
			unspecified length burst INCR
8	R/W	0	AHB Master interface INCRX align enable 1: start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of 11:9 is enabled
7:4	/	/	/
3	R/W	0x0	RC Clock Gating 0x0: clock gated 0x1: clock ungated
2	R/W	0x0	RC Generation Enable 0x0: disable 0x1: enable
1	/	/	/
0	R/W	0	ULPI bypass enable。 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

8.8.8.2 0x0808 HCI Control 3 Register (Default Value:0x0000_0000)

Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
31:17	/	/	Reserved.
16	R/W1C	0	Linestate Change Detect 0: Linestate change not detected. 1: Linestate change detected. Write '1' to clear.
15:10	/	/	Reserved.
9	R/W	0	Forcesusp 1: Susp_Sel is valid. PHY could be configured into suspend mode when Susp_Sel = 0. 0: Susp_Sel is invalid.
8	R/W	0	Susp_Sel 1: Normal operating mode (PHY) 0: Suspend Mode (PHY) This bit is valid when forcesusp=1.
7:4	/	/	/
3	R/W	0	Remote Wakeup Enable 1: Enable 0: Disable

Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
2	/	/	Reserved.
1	R/W	0	Linestate Change Interrupt Enable 1: Enable 0: Disable
0	R/W	0	Linestate Change Detect Enable 1: Enable 0: Disable

8.8.8.3 0x0810 PHY Control Register (Default Value: 0x0000_0018)

Offset: 0x0810			Register Name: PHY_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	VREGBYPASS
7	R/W	0	LOOPBACKENB
6	R/W	0	IDPULLUP
5	R/W	0	VBUSVLDEXT
4	R/W	1	VBUSVLDEXTSEL
3	R/W	1	SIDDQ 1: Write 1 to disable PHY. 0: Write 0 to enable PHY.
2	R/W	0	COMMONN
1:0	R/W	0	VATESTENB

8.8.8.4 0x0814 PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0814			Register Name: PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

8.8.8.5 0x0818 PHY Tune Register (Default Value:0x05B3_33D4)

Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description

Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.8.8.6 0x0824 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: PHY_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0	TESTDATAOUT

8.8.8.7 0x0828 HCI SIE Port Disable Control Register (Default Value:0x0000_0003)

Offset: 0x0828			Register Name: USB_SPDCR
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:5	/	/	/
4	R/W	0	resume_sel When set k-se0 transition 2us, setting this bit to 1, which is cooperated with ss_utmi_backward_enb_i.
3:2	/	/	/
1:0	R/W	0x3	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 Frames

8.9 USB2.0 HOST

8.9.1 Overview

The USB Host Controller is fully compliant with USB 2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification Revision 1.0 and Open Host Controller Interface (OHCI) Specification Release 1.0a.

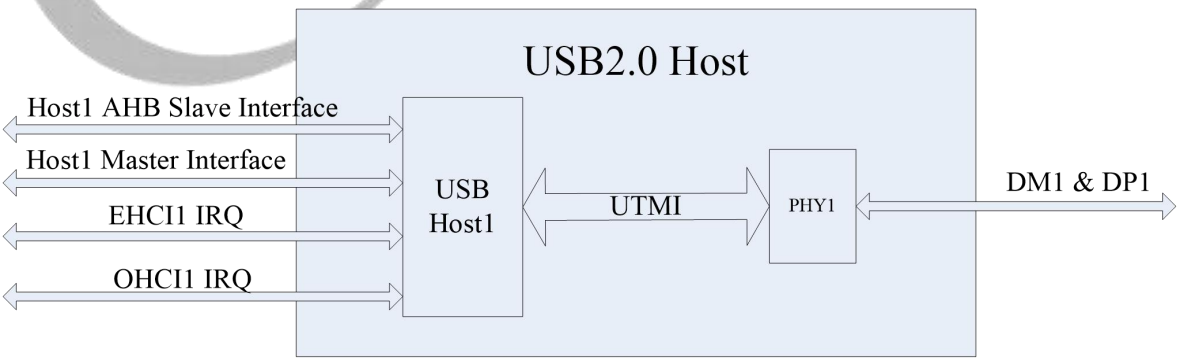
The USB2.0 host controller includes the following features:

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY
- Industry-standard AMBA High-Performance Bus (AHB), fully compliant with the AMBA Specification, Revision 2.0.
- 32-bit Little Endian AMBA AHB Slave Bus for Register Access
- 32-bit Little Endian AMBA AHB Master Bus for Memory Access
- An internal DMA Controller for data transfer with memory
- Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
- Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
- Supports the UTMI+ Level 3 interface and 8-bit bidirectional data buses
- Supports only 1 USB Root port shared between EHCI and OHCI

8.9.2 Block Diagram

The following figure shows the block diagram of USB2.0 Host Controller.

Figure 8-38 USB2.0 Host Controller Block Diagram



8.9.3 Functional Description

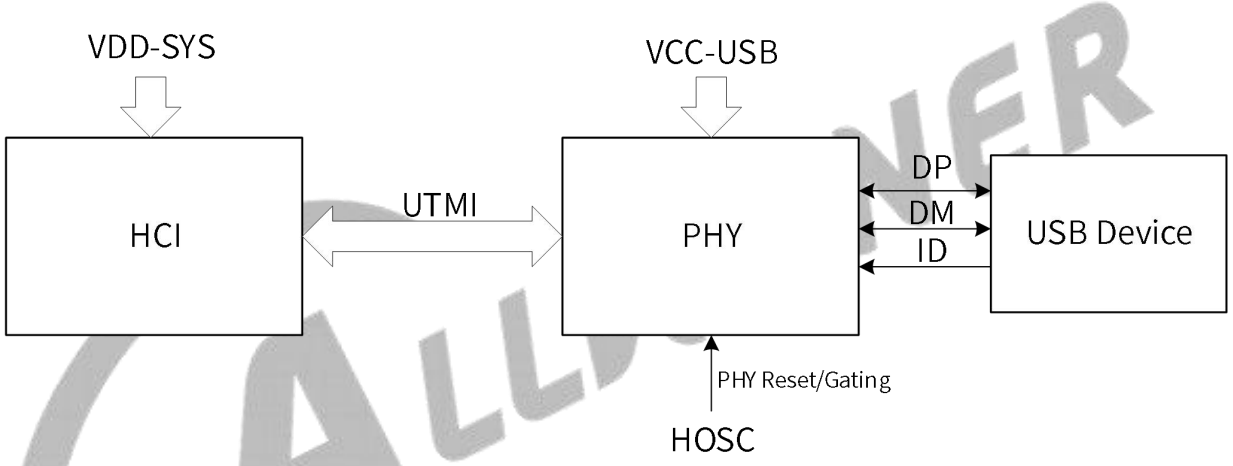
8.9.3.1 External Signals

Table 8-30 USB2.0 Host External Signals

Signal Name	Description	Type
USB1-DM	USB2.0 Data Signal DM	A I/O
USB1-DP	USB2.0 Data Signal DP	A I/O
USB1-REXT	USB2.0 External Reference Resistor AO	AO

8.9.3.2 Controller and PHY Connection Diagram

Figure 8-39 USB2.0 Host Controller and PHY Connection Diagram



8.9.4 Register List

Module Name	Base Address
USB1	0x04200000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x0000	EHCI Capability register Length Register
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000c	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register

Register Name	Offset	Description
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x0020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x0024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x0418	OHCI HCCA Base
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Base
O_HcControlHeadED	0x0420	OHCI Control Head ED Base
O_HcControlCurrentED	0x0424	OHCI Control Current ED Base
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x042C	OHCI Bulk Current ED Base
O_HcDoneHead	0x0430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x0448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x044C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register
HCI Controller and PHY Interface Register		
USB_CTRL	0x0800	HCI Interface Register
HCI_CTRL3	0x0808	HCI Control 3 Register
PHY_CTRL	0x0810	PHY Control Register
PHY_TEST	0x0814	PHY Test Register
PHY_TUNE	0x0818	PHY Tune Register
PHY_STA	0x0824	PHY Status Register
USB_SPDCR	0x0828	HCI SIE Port Disable Control Register

8.9.5 EHCI Register Description

8.9.5.1 0x0000 EHCI Identification Register (Default Value:0x10)

Offset:0x0000			Register Name: E_CAPLENGTH
Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

8.9.5.2 0x0002 EHCI Host Interface Version Number Register (Default Value:0x0100)

Offset: 0x0002			Register Name: E_HCIVERSION
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0100	HCIVERSION This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.9.5.3 0x0004 EHCI Host Control Structural Parameter Register (Default Value:0x0000_1101)

Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R	0x0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	0x1	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0x1	Number of Port per Companion Controller (N_PCC)

Offset: 0x0004			Register Name: E_HCSPARAMS
Bit	Read/Write	Default/Hex	Description
			This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0x0	Port Routing Rules This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value: 0 — Meaning: The first N_PCC ports are routed to the lowes numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. Value: 1 — Meaning: The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. This field will always be '0'.
6:4	/	/	/
3:0	R	0x1	N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

8.9.5.4 0x0008 EHCI Host Control Capability Parameter Register (Default Value:0x0000_A026)

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R	0xA0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space

Offset: 0x0008			Register Name: E_HCCPARAMS
Bit	Read/Write	Default/Hex	Description
			of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R	0x2	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	0x1	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	0x1	Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

8.9.5.5 0x000C EHCI Companion Port Route Description (Default Value:0x0000_0000)

Offset: 0x000C	Register Name: E_HCSP-PORTROUTE

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.9.5.6 0x0010 EHCI USB Command Register (Default Value:0x0008_0B00)

<table>
<tr><th colspan="3">Offset: 0x0010</th><th>Register Name: E_USBCMD</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td>31:24</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x08</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table>
<tr><th>Value</th><th>Minimum Interrupt Interval</th></tr>
<tr><td>0x00</td><td>Reserved</td></tr>
<tr><td>0x01</td><td>1 micro-frame</td></tr>
<tr><td>0x02</td><td>2 micro-frame</td></tr>
<tr><td>0x04</td><td>4 micro-frame</td></tr>
<tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr>
<tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr>
<tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr>
<tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr>
</table></td></tr>
</table>

Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
			Any other value in this register yields undefined results. The default value in this field is 0x08 . Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.
15:12	/	/	/
11	R	0x1	Asynchronous Schedule Park Mode Enable (OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.
10	/	/	/
9:8	R	0x3	Asynchronous Schedule Park Mode Count (OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0x0	Light Host Controller Reset (OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host
6	R/W	0x0	Interrupt on Async Advance Doorbell

<table>
<tr><td colspan="3">Offset: 0x0010</td><td>Register Name: E_USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>0x0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0010</td><td>Register Name: E_USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>in the Frame Index
Register should be used for the Frame List Current index. Values mean:
<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr><tr><td>01b</td><td>512 elements(2048byts)</td></tr><tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
<tr><td>1</td><td>R/W</td><td>0x0</td><td>Host Controller Reset
This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.
When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state.
This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.
Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.</td></tr>
<tr><td>0</td><td>R/W</td><td>0x0</td><td>Run/Stop
When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after</td></tr>
</table>

Offset: 0x0010			Register Name: E_USBCMD
Bit	Read/Write	Default/Hex	Description
			software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

8.9.5.7 0x0014 EHCI USB Status Register (Default Value:0x0000_1000)

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0x0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HC Halted This bit is a zero whenever the Run/Stop bit is a one.

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
			The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0x0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0x0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion

Offset: 0x0014			Register Name: E_USBSTS
Bit	Read/Write	Default/Hex	Description
			of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

8.9.5.8 0x0018 EHCI USB Interrupt Enable Register (Default Value:0x0000_0000)

Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the

Offset: 0x0018			Register Name: E_USBINTR
Bit	Read/Write	Default/Hex	Description
			USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

8.9.5.9 0x001C EHCI Frame Index Register (Default Value:0x0000_0000)

Offset: 0x001C			Register Name: E_FRINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times (frames or Micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

8.9.5.10 0x0024 EHCI Periodic Frame List Base Address Register (Default Value:0x0000_0000)

Offset: 0x0024			Register Name: E_PERIODICLISTBASE
Bit	Read/Write	Default/Hex	Description

Offset: 0x0024			Register Name: E_PERIODICLISTBASE
Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4 Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

NOTE

Writes must be Dword Writes.

8.9.5.11 0x0028 EHCI Current Asynchronous List Address Register (Default Value:0x0000_0000)

Offset: 0x0028			Register Name: E_ASYNCLISTADDR
Bit	Read/Write	Default/Hex	Description
31:5	R/W	0x0	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

8.9.5.12 0x0050 EHCI Configure Flag Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: E_CONFIGFLAG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/

Offset: 0x0050			Register Name: E_CONFIGFLAG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	Configure Flag (CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 — Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 — Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

NOTE

This register is not used in the normal implementation.

8.9.5.13 0x0054 EHCI Port Status and Control Register (Default Value:0x0000_2000)

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	Wake on Disconnect Enable (WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0x0	Wake on Connect Enable (WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0x0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follows: Bits: 0000b — Test Mode: The port is NOT operating in a test mode.

<table>
<tr><td colspan="3">Offset: 0x0054</td><td colspan="2">Register Name: E_PORTSC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td colspan="2">Description</td></tr>
<tr><td></td><td></td><td></td><td colspan="2">
<table>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-1111b</td><td>Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.
</td></tr>
<tr><td>15:14</td><td>/</td><td>/</td><td colspan="2">/</td></tr>
<tr><td>13</td><td>R/W</td><td>0x1</td><td colspan="2">Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>/</td><td colspan="2">/</td></tr>
<tr><td>11:10</td><td>R</td><td>0x0</td><td colspan="2">Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th colspan="3">Offset: 0x0054</th><th>Register Name: E_PORTSC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8</td><td>R/W</td><td>0x0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes.
Note: When software writes this bit to a one , it must also write a zero to the Port Enable bit.

Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table>
<tr><th>Bits[Port Enables, Suspend]</th><th>Port State</th></tr>
<tr><td>0x</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
</table></td></tr>
</table>

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
			11 Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: ① Software sets the Force Port Resume bit to a zero(from a one). ② Software sets the Port Reset bit to a one(from a zero). If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'.
6	R/W	0x0	Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
			port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0x0	Over-current Change This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	Over-current Active 0 = This port does not have an over-current condition 1 = This port currently has an over-current condition This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0x0	Port Enable/Disable Change 1 = Port enabled/disabled status has changed 0 = No change For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	Port Enabled/Disabled 1=Enable 0=Disable Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (Disconnect event or other fault condition) or by host software. Note that the bit status does not change

Offset: 0x0054			Register Name: E_PORTSC
Bit	Read/Write	Default/Hex	Description
			until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0x0	Connect Status Change 1=Change in Current Connect Status 0=No change Indicates a change has occurred in the current connect status of the port. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

NOTE

This register is only reset by hardware or in response to a host controller reset.

8.9.6 OHCI Register Description

8.9.6.1 0x0404 OHCI Control Register (Default Value: 0x0000_0000)

Offset: 0x0404				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		

<table>
<tr><th colspan="3">Offset: 0x0404</th><th colspan="2">Register Name: O_HcRevision</th></tr>
<tr><th rowspan="2">Bit</th><th colspan="2">Read/Write</th><th rowspan="2">Default/Hex</th><th rowspan="2">Description</th></tr>
<tr><th>HCD</th><th>HC</th></tr>
<tr><td>31:11</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>10</td><td>R/W</td><td>R</td><td>0x0</td><td>RemoteWakeupEnable
This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>RemoteWakeupConnected
This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.</td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>InterruptRouting
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB
<table><tr><td>00b</td><td>USBReset</td></tr><tr><td>01b</td><td>USBResume</td></tr><tr><td>10b</td><td>USBOperational</td></tr><tr><td>11b</td><td>USBSuspend</td></tr></table>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus.
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after</td></tr>
</table>

Offset: 0x0404				Register Name: O_HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	R/W	R	0x0	BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, the processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcBulkCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcBulkCurrentED* before re-enabling processing of the list.
4	R/W	R	0x0	ControlListEnable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, the processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcControlCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcControlCurrentED* before re-enabling processing of the list.
3	R/W	R	0x0	IsochronousEnable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable

<table>
<tr><td colspan="4">Offset: 0x0404</td><td colspan="2">Register Name: O_HcRevision</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2" colspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td colspan="2">This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>R</td><td>0x0</td><td colspan="2">ControlBulkServiceRatio
This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
<table>
<tr><td>CBSR</td><td>No. of Control EDs Over Bulk EDs Served</td></tr>
<tr><td>0</td><td>1:1</td></tr>
<tr><td>1</td><td>2:1</td></tr>
<tr><td>2</td><td>3:1</td></tr>
<tr><td>3</td><td>4:1</td></tr>
</table>
The default value is 0x0.</td></tr>
</table>

8.9.6.2 0x0408 OHCI Command Status Register (Default Value: 0x0000_0000)

<table>
<tr><td colspan="4">Offset: 0x0408</td><td colspan="2">Register Name: O_HcCommandStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2" colspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td>31:18</td><td>/</td><td>/</td><td>0x0</td><td colspan="2">Reserved</td></tr>
<tr><td>17:16</td><td>R</td><td>R/W</td><td>0x0</td><td colspan="2">SchedulingOverrunCount
These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problem.</td></tr>
<tr><td>15:4</td><td>/</td><td>/</td><td>/</td><td colspan="2">/</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td colspan="2">OwershipChangeRequest
This bit is set by an OS HCD to request a change of</td></tr>
</table>

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				control of the HC. When set HC will set the **OwnershipChange** field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	**BulklListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as **BulkListFilled** is 0, HC will not start processing the Bulk list. If **BulkListFilled** is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set **BulkListFilled** to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set **BulkListFilled**, then **BulkListFilled** will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as **ControlListFilled** is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set **ControlListFilled** to 0. If HC finds a TD on the list, then HC will set **ControlListFilled** to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set **ControlListFilled**, then **ControlListFilled** will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	**HostControllerReset** This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is

Offset: 0x0408				Register Name: O_HcCommandStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

8.9.6.3 0x040C OHCI Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:7	/	/	/	/
6	R/W	R/W	0x0	**RootHubStatusChange** This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[**NumberofDownstreamPort**] has changed.
5	R/W	R/W	0x0	**FrameNumberOverflow** This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	**UnrecoverableError** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	**ResumeDetected** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	**StartofFrame** This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	**WritebackDoneHead** This bit is set immediately after HC has written

Offset: 0x040C				Register Name: O_HcInterruptStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				HcDoneHead to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	**SchedulingOverrun** This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the **SchedulingOverrunCount** of *HcCommandStatus* to be incremented.

8.9.6.4 0x0410 OHCI Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Resume Detected

Offset: 0x0410				Register Name: O_HcInterruptEnable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Write back Done Head
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore 1 Enable interrupt generation due to Scheduling Overrun

8.9.6.5 0x0414 OHCI Interrupt Disable Register (Default Value: 0x0000_0000)

Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore

Offset: 0x0414				Register Name: O_HcInterruptDisable
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				1 Disable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Write back Done Head
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore 1 Disable interrupt generation due to Scheduling Overrun

8.9.6.6 0x0418 OHCI HCCA Register (Default Value: 0x0000_0000)

Offset: 0x0418				Register Name: O_HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA [31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA [7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

8.9.6.7 0x041C OHCI Period Current ED Register (Default Value: 0x0000_0000)

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		

Offset: 0x041C				Register Name: O_HcPeriodCurrentED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED [31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.6.8 0x0420 OHCI Control Head ED Register (Default Value: 0x0000_0000)

Offset: 0x0420				Register Name: O_HcControlHeadED
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD [31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.6.9 0x0424 OHCI Control Current ED Register (Default Value: 0x0000_0000)

Offset: 0x0424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list

Offset: 0x0424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.6.10 0x0428 OHCI Bulk Head ED Register (Default Value: 0x0000_0000)

Offset: 0x0428				Register Name: O_HcBulkHeadED[BHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED [31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.6.11 0x042C OHCI Bulk Current ED Register (Default Value: 0x0000_0000)

Offset: 0x042C			Register Name: O_HcBulkCurrentED[BCED]
Bit	Read/Write	Default/Hex	Description

	HCD	HC		
31:4	R/W	R/W	0x0	**BulkCurrentED [31:4]** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the **ControlListFilled** of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the **BulkListEnable** of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	**BulkCurrentED [3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.6.12 0x0430 OHCI Done Head Register (Default Value: 0x0000_0000)

Offset: 0x0430				Register Name: O_HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	**HcDoneHead [31:4]** When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the **WritebackDoneHead** of *HcInterruptStatus*.
3:0	R	R	0x0	**HcDoneHead [3:0]** Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.9.6.13 0x0434 OHCI Frame Interval Register (Default Value: 0x0000_2EDF)

Offset: 0x0434			Register Name: O_HcFmInterval Register
Bit	Read/Write	Default/Hex	Description

	HCD	HC		
31	R/W	R	0x0	**FrameIntervalToggler** HCD toggles this bit whenever it loads a new value to **FrameInterval**.
30:16	R/W	R	0x0	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the **HostControllerReset** field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.9.6.14 0x0438 OHCI Frame Remaining Register (Default Value: 0x0000_0000)

Offset: 0x0438				Register Name: O_HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	**FrameRemaining Toggle** This bit is loaded from the **FrameIntervalToggle** field of *HcFmInterval* whenever **FrameRemaining** reaches 0. This bit is used by HCD for the synchronization between **FrameInterval** and **FrameRemaining**.
30:14	/	/	/	/
13:0	R	RW	0x0	**FramRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

8.9.6.15 0x043C OHCI Frame Number Register (Default Value: 0x0000_0000)

Offset: 0x043C				Register Name: O_HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/
15:0	R	R/W	0x0	**FrameNumber** This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the **FrameNumber** at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the **StartofFrame** in *HcInterruptStatus.*

8.9.6.16 0x0440 OHCI Periodic Start Register (Default Value: 0x0000_0000)

Offset: 0x0440				Register Name: O_HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*. A typical value will be 0x2A3F (or 0x3e67). When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.9.6.17 0x0444 OHCI LS Threshold Register (Default Value: 0x0000_0628)

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	/

Offset: 0x0444				Register Name: O_HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
11:0	R/W	R	0x0628	**LSThreshold** This field contains a value which is compared to the **FrameRemaining** field prior to initiating a Low Speed transaction. The transaction is started only if **FrameRemaining** this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.9.6.18 0x0448 OHCI Root Hub DescriptorA Register (Default Value: 0x0200_1201)

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	**PowerOnToPowerGoodTime[POTPGT]** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	0x1	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the **OverCurrentProtectionMode** field specifies global or per-port reporting. **0** — Over-current status is reported collectively for all downstream ports. **1** — No overcurrent protection supported.
11	R/W	R	0x0	**OverCurrentProtectionMode** This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as **PowerSwitchingMode**. This field is valid only if the **NoOverCurrentProtection** field is cleared. 0 — Over-current status is reported collectively for all downstream ports. 1 — Over-current status is reported on per-port basis.
10	R	R	0x0	**Device Type** This bit specifies that the Root Hub is not a compound

Offset: 0x0448				Register Name: O_HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	0x1	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the **NoPowerSwitching** field is cleared. 0: All ports are powered at the same time. 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the **PortPowerControlMask** bit is set, the port responds only to port power commands (**Set/ClearPortPower**). If the port mask is cleared, then the port is controlled only by the global power switch (**Set/ClearGlobalPower**).
8	R/W	R	0x0	**NoPowerSwithcing** These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the **PowerSwitchingMode** specifies global or per-port switching. **0**: Ports are power switched. **1**: Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

8.9.6.19 0x044C HcRhDescriptorB Register (Default Value: 0x0000_0000)

Offset: 0x044C				Register Name: O_HcRhDescriptorB Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask

Offset: 0x044C				Register Name: O_HcRhDescriptorB Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. ... Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. ... Bit15 Device attached to Port #15.

8.9.6.20 0x0450 HcRhStatus Register (Default Value: 0x0000_0000)

Offset: 0x0450				Register Name: O_HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	**(write)ClearRemoteWakeupEnable** Write a '1' clears **DeviceRemoteWakeupEnable.** Writing a '0' has no effect.
30:18	/	/	/	/
17	R/W	R	0x0	**OverCurrentIndicatorChang** This bit is set by hardware when a change has occurred to the **OverCurrentIndicator** field of this register. The HCD clears this bit by writing a '1'. Writing a '0' has no effect.

<table>
<tr><td colspan="4">Offset: 0x0450</td><td>Register Name: O_HcRhStatus Register</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td>16</td><td>R/W</td><td>R</td><td>0x0</td><td>(read)LocalPowerStartusChange
The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’.
(write)SetGlobalPower
In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.</td></tr>
<tr><td>15</td><td>R/W</td><td>R</td><td>0x0</td><td>(read)DeviceRemoteWakeupEnable
This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt.
<table><tr><td>0</td><td>ConnectStatusChange is not a remote wakeup event.</td></tr><tr><td>1</td><td>ConnectStatusChange is a remote wakeup event.</td></tr></table>
(write)SetRemoteWakeupEnable
Writing a ‘1’ sets DeviceRemoveWakeupEnable.
Writing a ‘0’ has no effect.</td></tr>
<tr><td>14:2</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>1</td><td>R</td><td>R/W</td><td>0x0</td><td>OverCurrentIndicator
This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal.
If per-port overcurrent protection is implemented this bit is always ‘0’</td></tr>
<tr><td>0</td><td>R/W</td><td>R</td><td>0x0</td><td>(Read)LocalPowerStatus
When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as ‘0’.
(Write)ClearGlobalPower
When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to ‘1’ to</td></tr>
</table>

Offset: 0x0450				Register Name: O_HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
				turn off power to all ports (clear **PortPowerStatus**). In per-port power mode, it clears **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a '0' has no effect.

8.9.6.21 0x0454 HcRhPortStatus Register (Default Value: 0x0000_0100)

Offset: 0x0454				Register Name: O_HcRhPortStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:21	/	/	/	/
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.

<table>
<tr><td colspan="3">Offset: 0x0454</td><td colspan="2">Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td><table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table></td></tr>
<tr><td>16</td><td>R/W</td><td>R/W</td><td>0x0</td><td>ConnectStatusChange
This bit is set whenever a connect or disconnect event occurs. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>
Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0454</td><td colspan="2">Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td>PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls
this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.

Note: This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured</td></tr>
</table>

<table>
<tr><td colspan="3">Offset: 0x0454</td><td colspan="2">Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>
(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes</td></tr>
</table>

<table>
<tr><td colspan="4">Offset: 0x0454</td><td>Register Name: O_HcRhPortStatus</td></tr>
<tr><td rowspan="2">Bit</td><td colspan="2">Read/Write</td><td rowspan="2">Default/Hex</td><td rowspan="2">Description</td></tr>
<tr><td>HCD</td><td>HC</td></tr>
<tr><td></td><td></td><td></td><td></td><td>PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
<table><tr><td>0</td><td>port is disabled</td></tr><tr><td>1</td><td>port is enabled</td></tr></table>
(write)SetPortEnable
The HCD sets PortEnableStatus by writing a ‘1’. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.</td></tr>
<tr><td>0</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)CurrentConnectStatus
This bit reflects the current state of the downstream port.
<table><tr><td>0</td><td>No device connected</td></tr><tr><td>1</td><td>Device connected</td></tr></table>
(write)ClearPortEnable
The HCD writes a ‘1’ to clear the PortEnableStatus bit. Writing ‘0’ to this bit has no effect. The CurrentConnectStatus is not affected by any write.
Note: This bit is always read ‘1’ when the attached device is nonremovalble (DviceRemoveable[NumberDownstreamPort]).</td></tr>
</table>

8.9.7 HCI Contgroller and PHY Interface Description

8.9.7.1 0x0800 HCI Interface Register (Default Value: 0x1000_0000)

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USB Standby Clock Sel 0x0: normal mode usb clock as usual 0x1: standby mode usb clock switch to RC 16M clock

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
30:29	/	/	Reserved
28	R	1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0	OHCI count select 1: Simulation mode. The counters will be much shorter then real time 0: Normal mode. The counters will count full time
24:19	/	/	/
18	R/W	0	1: Within 2 us of the resume-K to SE0 transition 0: Random time value of the resume-K to SE0 transition
17:13	/	/	/
12	R/W	0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0	AHB Master interface INCR16 enable 1: Use INCR16 when appropriate 0: Do not use INCR16, use other enabled INCRX or unspecified length burst INCR
10	R/W	0	AHB Master interface INCR8 enable 1: Use INCR8 when appropriate 0: Do not use INCR8, use other enabled INCRX or unspecified length burst INCR
9	R/W	0	AHB Master interface burst type INCR4 enable 1: Use INCR4 when appropriate 0: Do not use INCR4, use other enabled INCRX or unspecified length burst INCR
8	R/W	0	AHB Master interface INCRX align enable 1: Start INCRx burst only on burst x-align address 0: Start burst on any double word boundary Note: This bit must enable if any bit of bit[11:9] is enabled
7:4	/	/	/
3	R/W	0x0	RC Clock Gating 0x0: clock gated 0x1: clock ungated

Offset: 0x0800			Register Name: USB_CTRL
Bit	Read/Write	Default/Hex	Description
2	R/W	0x0	RC Generation Enable 0x0: disable 0x1: enable
1	/	/	/
0	R/W	0	ULPI bypass enable 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

8.9.7.2 0x0808 HCI Control 3 Register (Default Value: 0x0001_0000)

Offset: 0x0808			Register Name: HCI_CTRL3
Bit	Read/Write	Default/Hex	Description
31:17	/	/	Reserved
16	R/W1C	0	Linestate Change Detect 0: Linestate change not detected 1: Linestate change detected Write '1' to clear.
15:10	/	/	Reserved
9	R/W	0	Forcesusp 1: Susp_Sel is valid. PHY could be configured into suspend mode when Susp_Sel = 0. 0: Susp_Sel is invalid.
8	R/W	0	Susp_Sel 1: Normal operating mode(PHY) 0: Suspend Mode(PHY) This bit is valid when forcesusp=1.
7:4	/	/	/
3	R/W	0	Remote Wakeup Enable 1: Enable 0: Disable
2	/	/	Reserved
1	R/W	0	Linestate Change Interrupt Enable 1: Enable 0: Disable
0	R/W	0	Linestate Change Detect Enable 1: Enable 0: Disable

8.9.7.3 0x0810 PHY Control Register (Default Value: 0x0000_0018)

Offset: 0x0810			Register Name: PHY_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	VREGBYPASS
7	R/W	0	LOOPBACKENB
6	R/W	0	IDPULLUP
5	R/W	0	VBUSVLDEXT
4	R/W	1	VBUSVLDEXTSEL
3	R/W	1	SIDDQ 1: Write 1 to disable phy. 0: Write 0 to enable phy.
2	R/W	0	COMMONN
1:0	R/W	0	VATESTENB

8.9.7.4 0x0814 PHY Test Register (Default Value:0x0000_0000)

Offset: 0x0814			Register Name: PHY_TEST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR
7:0	R/W	0x0	TESTDATAIN

8.9.7.5 0x0818 PHY Tune Register (Default Value:0x05B3_33D4)

Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]

Offset: 0x0818			Register Name: PHY_TUNE
Bit	Read/Write	Default/Hex	Description
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.9.7.6 0x0824 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x0824			Register Name: PHY_STA
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0	TESTDATAOUT

8.9.7.7 0x0828 HCI SIE Port Disable Control Register (Default Value: 0x0000_0000)

Offset: 0x0828			Register Name: USB_SPDCR
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:5	/	/	/
4	R/W	0	resume_sel When set k-se0 transition 2 us, setting this bit to 1, which is cooperated with ss_utmi_backward_enb_i.
3:2	/	/	/
1:0	R/W	0	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 frames

8.10 PCIe2.1&USB3.1 Top System

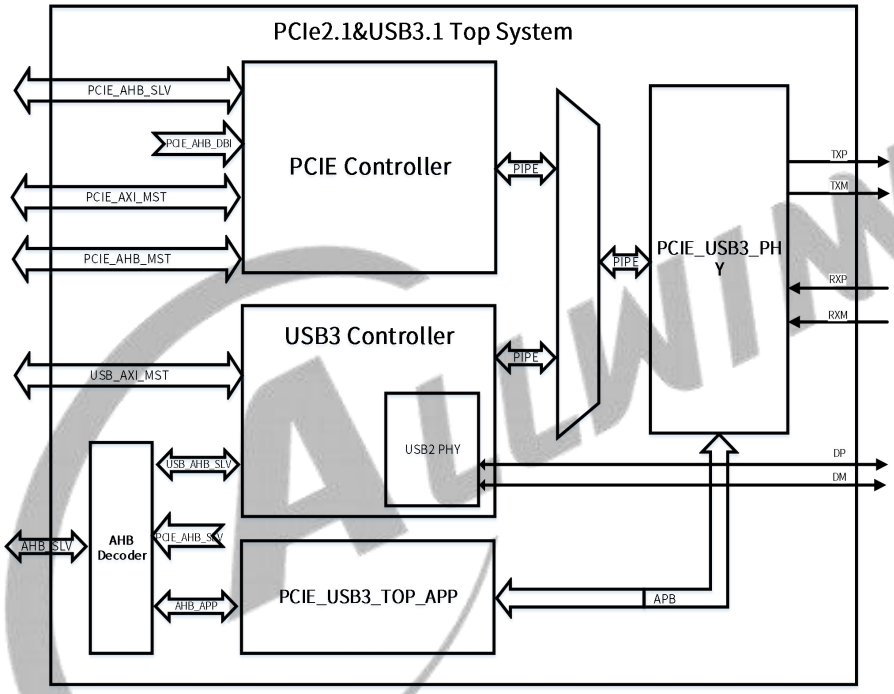
8.10.1 Overview

The PCIe2.1&USB3.1 top system integrates a PCIe2.1 RC controller and a USB3.1 DRD controller with a Combo PHY which supports PCIe GEN1 GEN2 and USB3.1 GEN1 speed and is shared through PIPE interface.

8.10.2 Block Diagram

The following figure shows the block diagram of PCIe2.1&USB3.1 top system.

Figure 8-40 PCIe2.1&USB3.1 Top System Block Diagram



NOTE

This chapter foucuses on the 1 PCIe2.1&USB3.1 combo PHY. For the detailed description of PCIe2.1 and USB3.1 DRD, please refer to section 8.12 PCIe2.1 and section 8.11 USB3.1 DRD.

8.10.3 Register List

Module Name	Base Address
PCIE_USB3_TOP_APP	0x04F00000

Register Name	Offset	Description

Register Name	Offset	Description
PCIEBGR	0x0004	PCIE Bus Gating Reset Register
USB3BGR	0x0008	USB3 Bus Gating Reset Register
PHYCTL	0x0010	PHY Control Register
PHYSTS0	0x0080	PHY Status Register 0
PHYSTS1	0x0084	PHY Status Register 1
PHYSTS2	0x0088	PHY Status Register 2

8.10.4 Register Description

8.10.4.1 0x0004 PCIE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PCIEBGR
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	PCIE_ACLK_EN PCIE AXI Clock Enable
16	R/W	0x0	PCIE_HCLK_EN PCIE AHB Clock Enable
15:2	/	/	/
1	R/W	0x0	PCIE_PERSTN
0	R/W	0x0	PCIE_POWER_UP_RSTN

8.10.4.2 0x0008 USB3 Bus Gating Reset Register (Default Value:0x0000_0000)

Offset: 0x0008			Register Name: USB3BGR
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	USB3_ACLK_EN USB3 AXI Clock Enable
16	R/W	0x0	USB3_HCLK_EN USB3 AHB Clock Enable
15:1	/	/	/
0	R/W	0x0	USB3_RESETN

8.10.4.3 0x0010 PHY Control Register (Default Value:0x0000_0000)

Offset: 0x0010			Register Name: PHYCTL
Bit	Read/Write	Default/Hex	Description

Offset: 0x0010			Register Name: PHYCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY_USE_SEL 0: PHY used by PCIE 1: PHY used by USB3
30	R/W	0x0	PHY_REFCLK_SEL 0: PHY uses internal single end reference clock 1: PHY uses external differential reference clock
29:17	/	/	/
16	R/W	0x0	PHY_BIST_EN
15:10	/	/	/
9	R/W	0x0	PHY_PIPE_RSTN_SW
8	R/W	0x0	PHY_PIPE_RSTN_SEL 0: PHY PIPE resetn is controlled by PCIE or USB3 Controller 1: PHY PIPE resetn is controlled by PHY_PIPE_RSTN_SW
7:5	/	/	/
4	R/W	0x0	PHY_PIPE_CLK_INVERT
3:1	/	/	/
0	R/W	0x0	PHY_RSTN Combo PHY Power On RESET_N

8.10.4.4 0x0080 PHY Status Register 0 (Default Value:0x0000_0000)

Offset: 0x0080			Register Name: PHYSTS0
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PHY_PIPE_PHYSTATUS_ASSERT_PENDING
30	R	0x0	PHY_PIPE_PHYSTATUS
29:2	/	/	/
1	R	0x0	PHY_BIST_PASS
0	R	0x0	PHY_BIST_DONE

8.10.4.5 0x0084 PHY Status Register 1 (Default Value:0x0000_0000)

Offset: 0x0084			Register Name: PHYSTS1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHY_PIPE_RX_DBG_EN
30:7	/	/	/
6	R	0x0	PHY_PIPE_RXELECIDLE
5	R	0x0	PHY_PIPE_RXVALID
4	R	0x0	PHY_PIPE_RXDATAVALID

Offset: 0x0084			Register Name: PHYSTS1
Bit	Read/Write	Default/Hex	Description
3:0	R	0x0	PHY_PIPE_RXDATAK

8.10.4.6 0x0088 PHY Status Register 2 (Default Value:0x0000_0000)

Offset: 0x0088			Register Name: PHYSTS2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PHY_PIPE_RXDATA

8.11 USB3.1 DRD

8.11.1 Overview

The USB3.1 DRD is a Dual-Role Device (DRD) controller, which supports both device and host functions which can also be configured as a host-only or device-only controller, fully compliant with the USB 3.1 Specification. It can support super-speed (SS, 5-Gbit/s), high-speed (HS, 480-Mbit/s), full-speed (FS, 12-Mbit/s), and low-speed (LS, 1.5-Mbit/s) transfers in Host mode. It can support super-speed (SS, 5-Gbit/s), high-speed (HS, 480-Mbit/s), and full-speed (FS, 12-Mbit/s) in Device mode. Standard USB transceiver can be used through its UTMI+ interface and PIPE interface.

The USB3 DRD controller includes the following features:

- Compliant with USB3.1 GEN1 Specification
- One USB 2.0 UTMI+ PHY (USB2)
- One USB3.1 PIPE PHY (USB3)
- USB3.1 DRD Device mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s) and Full-Speed (FS, 12-Mbit/s) for USB2.0 PHY
- USB3.1 DRD HOST mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) for USB2.0 PHY
- Support Device or Host operation at a time
- AXI interface for DMA operation
- Reading and writing access to Control and Status Registers (CSRs) through AHB Slave interface
- Up to 10 Endpoints, including bi-directional control Endpoint 0 in Device mode:
  - 5 IN Endpoints: User EP1 IN, EP2 IN, EP3 IN, EP4 IN, Control EP0 IN
  - 5 OUT Endpoints: User EP1 OUT, EP2 OUT, EP3 OUT, EP4 OUT, Control EP0 OUT
- Simultaneous IN and OUT transfer in Super-Speed mode
- Dual-port interfaces for TX data buffering, RX data prefetching, descriptor caching, and register caching
- Three RAMs: RX data FIFO RAM, TX data FIFO RAM, and descriptor/register Cache RAM
- Hardware handles all data transfer
- Implements both static and dynamic power reduction techniques at multiple levels

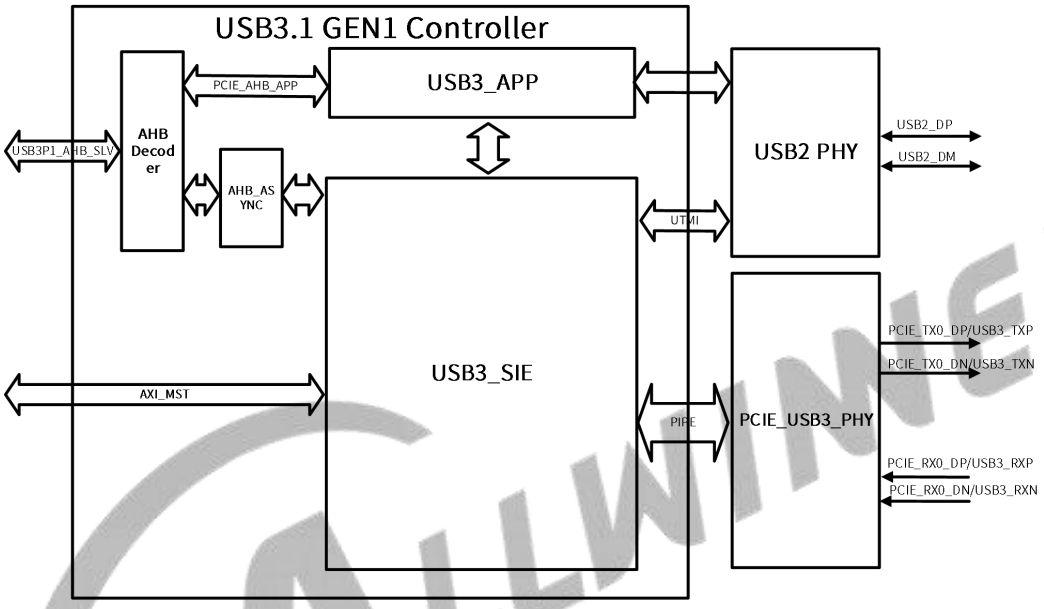
NOTE

USB2.0 PHY and USB3.1 PHY share the same controller. They cannot be used simultaneously.

8.11.2 Block Diagram

The following figure shows the block diagram of USB3.1 DRD Controller

Figure 8-41 USB3.1 DRD Controller Block Diagram



8.11.3 Functional Description

8.11.3.1 External Signals

Table 8-31 USB3.1 DRD External Signals

Signal Name	Description	Type
USB2-DM	USB2.0 Data Signal DM	A I/O
USB2-DP	USB2.0 Data Signal DP	A I/O
USB2-REXT	USB2.0 External Reference Resistor	AO
USB3-RXN	USB3.1 SuperSpeed Differential Signal of RX (Negative)	AI
USB3-RXP	USB3.1 SuperSpeed Differential Signal of RX (Positive)	AI
USB3-TXN	SuperSpeed Differential Signal of TX (Negative)	AO
USB3-TXP	USB3.1 SuperSpeed Differential Signal of TX (Positive)	AO
VCC33-USB-2	3.3 V Power Supply for USB2.0 PHY	P
VCC33-18-USB-2	3.3 V/1.8 V Power Supply for USB2.0 PHY	P

NOTE

For detailed functional information, please refer to *USB3.1 Specification, USB2.0 Specification,* and *eXtensible Host Controller Interface (XHCI) Specification, Version 1.1.*

8.11.4 Register List

There are four groups of registers in USB3.1 DRD.

Register Class	Offset
USB3 (0x04D0 0000---0x04EF FFFF)	
xHCI Registers	0x00000000 - 0x00007FFF
Global Registers	0x0000C100 - 0x0000C6FF
Device Registers	0x0000C700 - 0x0000CBFF
Application Registers	0x0010 0000 - 0x001007FF

8.11.4.1 xHCI Register List

Register Class	Base Address
xHCI Registers	0x04D0 0000-0x04D0 7FFF

Register Name	Offset	Description
xHCI Capability Registers		
HCCLVER	0x0000	xHC Capability Length and Version Register
HCSPARAMS1	0x0004	xHC Structural Parameter 1 Register
HCSPARAMS2	0x0008	xHC Structural Parameters 2 Register
HCSPARAMS3	0x000C	xHC Structural Parameters 3 Register
HCCPARAMS	0x0010	xHC Capability Parameters Register
DBOFF	0x0014	xHC Doorbell Offset Register
RTSOFF	0x0018	xHC Runtime Register Space Offset Register
HCCPARAMS2	0x001C	xHC Capability Parameters 2 Register
xHCI Operational Registers		
HCUSBCMD	0x0020	xHC USB Command Register
HCUSBSTS	0x0024	xHC USB Status Register
HCPAGESIZE	0x0028	xHC Page Size Register
HCDNCTRL	0x0034	xHC Device Notification Control Register
HCCRCLR	0x0038	xHC Command Ring Control Low Register
HCCRCHR	0x003C	XHC Command Ring Control High Register
HCDCBAAPLR	0x0050	xHC Device Context Base Address Array Pointer Low Register
HCDCBAAPHR	0x0054	xHC Device Context Base Address Array Pointer High

Register Name	Offset	Description
		Register
HCCONFIG	0x0058	xHC Configure Register
HCPORT1SC	0x0420	xHC Port1 Status and Control Register (USB2 Protocol)
HCPORT1PMSC	0x0424	xHC Port1 PM Status and Control Register (USB2 Protocol)
HCPORT1LI	0x0428	xHC Port1 Link Info Register (USB2 Protocol)
HCPORT2SC	0x0430	xHC Port2 Status and Control Register (USB3 Protocol)
HCPORT2PMSC	0x0434	XHC Port2 PM Status and Control Register (USB3 Protocol)
HCPORT2LI	0x0438	xHC Port2 Link Info Register (USB3 Protocol)
xHCI Runtime Registers		
HCMFINDEX	0x1000	xHC Microframe Index Register
HCIMAN0	0x1020	xHC Interrupt 0 Management Register
HCIMOD0	0x1024	xHC Interrupt 0 Moderation Register
HCERSTSZ0	0x1028	xHC Interrupt 0 Event Ring Segment Table Size Register
HCERSTBAL0	0x1030	xHC Interrupt 0 Event Ring Segment Table Base Address Low Register
HCERSTBAH0	0x1034	xHC Interrupt 0 Event Ring Segment Table Base Address High Register
HCERDPL0	0x1038	xHC Interrupt 0 Event Ring Dequeue Pointer Low Register
HCERDPH0	0x103C	xHC Interrupt 0 Event Ring Dequeue Pointer High Register
xHCI Doorbell Registers		
HCDBRn (n = 0 to 64)	0x2000+4*n	XHC Doorbell Register n (n=0, 1,……, 64)
xHCI Extended Capabilities Registers		
HCUSBLEGSUP	0x0440	xHC USB Legacy Support Capability Register
HCUSBLEGCTRLSTS	0x0444	xHC USB Legacy Support Control/Status Register
HCSPC1REV	0x0490	xHC Support Protocol Capability 1 Revision Register
HCSPC1STR	0x0494	xHC Support Protocol Capability 1 String Register
HCSPC1PRT	0x0498	xHC Support Protocol Capability 1 Port Register
HCSPC2REV	0x04A0	xHC Support Protocol Capability 2 Revision Register
HCSPC2STR	0x04A4	xHC Support Protocol Capability 2 String Register
HCSPC2PRT	0x04A8	xHC Support Protocol Capability 3 Port Register

8.11.4.2 Global Register List

Register Class	Base Address
Global Registers	0x04D0 C100 - 0x04D0 C6FF

Register Name	Offset	Description
GSBUSCFG0	0xC100	Global Soc Bus Configuration Register 0
GSBUSCFG1	0xC104	Global Soc Bus Configuration Register 1
GTXTHRCFG	0xC108	Global Tx Threshold Control Register
GRXTHRCFG	0xC10C	Global Rx Threshold Control Register
GCTL	0xC110	Global Core Control Register
GPMSTS	0xC114	Global Power Management Status Register
GSTS	0xC118	Global Status Register
GUCTL1	0xC11C	Global User Control Register 1
GID	0xC120	Global ID Register
GGPIO	0xC124	Global General Purpose Input/Output Register
GUID	0xC128	Global User ID Register
GUCTL	0xC12C	Global User Control Register
GBUSERRADDR_Lo	0xC130	Global Bus Error Address Low Register
GBUSERRADDR_Hi	0xC134	Global Bus Error Address High Register
GPRTBIMAP_Lo	0xC138	Global Super Speed Port to Bus Instance Mapping Low Register
GPRTBIMAP_Hi	0xC13C	Global Super Speed Port to Bus Instance Mapping High Register
GDBGFIFOSPACE	0xC160	Global Debug Queue/FIFO Space Available Register
GBMUCTL	0xC164	Global BMU Control Register
GDBGBMU	0xC16C	Global Debug BMU Register
GDBGLSPMUX	0xC170	Global Debug LSP MUX Register
GDBGLSP	0xC174	Global Debug LSP Register
GDBGEPINFO0	0xC178	Global Debug Endpoint Information Register 0
GDBGEPINFO1	0xC17C	Global Debug Endpoint Information Register 1
GPRTBIMAP_HS_Lo	0xC180	Global High Speed Port to Bus Instance Mapping Low Register
GPRTBIMAP_HS_Hi	0xC184	Global High Speed Port to Bus Instance Mapping High Register
GPRTBIMAP_FS_Lo	0xC188	Global Full Speed Port to Bus Instance Mapping Low Register
GPRTBIMAP_FS_Hi	0xC18C	Global Full Speed Port to Bus Instance Mapping High Register
GHMSOCBWOR	0xC190	Global Host Mode SoC Bandwidth Override Register

Register Name	Offset	Description
GUSB2PHYCFGn	0xC200	Global USB2 PHY Configuration Register
GUSB3PIPECTLn	0xC2C0	Global USB3 PIPE Control Register
GTXFIFOSIZ	0xC300+0x04*n (n=FIFO_number)	Global Transmit FIFO Size Register n (n=FIFO_number)
GRXFIFOSIZ0	0xC380+0x04*n (n=FIFO_number)	Global Receive FIFO Size Register n (n=FIFO_number)
GEVNTADLRn	0xC400+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Address Lower Register n (0<= n <= EventBuff_number)
GEVNTADHRn	0xC404+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Address Higher Register n (0<= n <= EventBuff_number)
GEVNTSIZn	0xC408+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Size Register n (0<= n <= EventBuff_number)
GEVNTCOUNTn	0xC40C+0x10*n (0<= n <= EventBuff_number)	Global Event Buffer Count Register n (0<= n <= EventBuff_number)
GTXFIFOPRIDEV	0xC610	Global Device Tx FIFO DMA Priority Register
GTXFIFOPRIHST	0xC618	Global Host Tx FIFO DMA Priority Register
GRXFIFOPRIHST	0xC61C	Global Host Rx FIFO DMA Priority Register
GDMAHLRATIO	0xC624	Global Host FIFO DMA High-Low Priority Ratio Register

8.11.4.3 Device Register List

Register Class	Base Address
Device Registers	0x04D0 C700 - 0x04D0 CBFF

Register Name	Offset	Description
DCFG	0xC700	Device Configuration Register
DCTL	0xC704	Device Control Register
DEVTEN	0xC708	Device Event Enable Register
DSTS	0xC70C	Device Status Register
DGCMDPAR	0xC710	Device Generic Command Parameter Register
DGCMD	0xC714	Device Generic Command Register
DCTL1	0xC718	Device Control Register 1
DALEPENA	0xC720	Device Active USB Endpoint Enable Register
DLDMENA	0xC724	Device LDM Request Control Register
DEPCMDPAR2_n (n=0 to 9)	0xC800+0x10*n	Device Physical Endpoint-n Command Parameter 2 Register

Register Name	Offset	Description
DEPCMDPAR1_n (n=0 to 9)	0xC804+0x0010*n	Device Physical Endpoint-n Command Parameter 1 Register
DEPCMDPAR0_n (n=0 to 9)	0xC808+0x0010*n	Device Physical Endpoint-n Command Parameter 0 Register
DEPCMD_n (n=0 to 9)	0xC80c+0x0010*n	Device Physical Endpoint-n Command Register
DEPIMOD	0xCA00	Device Interrupt Moderation Register

8.11.4.4 Application Register List

Register Class	Base Address
Application Registers	0x04E0 0000 - 0x04E007FF

Register Name	Offset	Description
U2_ISCR	0x100000	USB2.0 Interface Status and Control Register
U2_PHYCTL	0x100010	USB2.0 PHY Control Register
U2_PHYTST	0x100014	USB2.0 PHY TEST Register
U2_PHYTUNE	0x100018	USB2.0 PHY Tune Register
U2_PHYSTS	0x100024	USB2.0 PHY Status Register

8.11.5 xHCI Register Description

8.11.5.1 x0000 xHC Capability Length and Version Register (Default Value: 0x0110_0020)

Offset:0x0000			Register Name: HCCLVER
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0110	HCIVERSION HC Interface Version Number This is a 16-bits register containing a BCD encoding of the xHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.
15:8	/	/	/
7:0	R	0x20	CAPLENGTH Capability register Length This register is used as an offset to add to register base to find the beginning of the Operational Register Space.

8.11.5.2 0x0004 xHC Structural Parameters 1 Register (Default Value:0x0200_0140)

Offset: 0x0004			Register Name: HCSPARAMS1
Bit	Read/Write	Default/Hex	Description
31:24	R	0x02	MaxPorts Number of Ports This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Set that are addressable in the Operational Register Space
23:19	/	/	/
18:8	R	0x01	MaxIntrs Number of Interrupters This field specifies the number of Interrupters implemented on this host controller
7:0	R	0x40	MaxSlots Number of Device Slots This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support.

8.11.5.3 0x0008 xHC Structural Parameters 2 Register (Default Value: 0x1400_00F1)

Offset: 0x0008			Register Name: HCSPARAMS2
Bit	Read/Write	Default/Hex	Description
31:27	R	0x2	Max Scratchpad Bufs Lo Max Scratchpad Buffers Low This field indicates the low order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC
26	R	0x1	SPR Scratchpad Restore. If *Max Scratchpad Buffers* is > '0' then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If *Max Scratchpad Buffers* is = '0' then this flag shall be '0'. A value of '1' indicates that the xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events. A value of '0' indicates that the Scratchpad Buffer space may be freed and reallocated between power events.
25:21	R	0	Max Scratchpad Bufs Hi

Offset: 0x0008			Register Name: HCSPARAMS2
Bit	Read/Write	Default/Hex	Description
			Max Scratchpad Buffers High This field indicates the high order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC
20:8	/	/	/
7:4	R	0xF	ERST Max Event Ring Segment Table Max. This field determines the maximum value supported the Event Ring Segment Table Base Size registers, where: The maximum number of Event Ring Segment Table entries = $2^{\text{ERST Max}}$.
3:0	R	0x1	IST Isochronous Scheduling Threshold. The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/ microframes. If bit [3] of IST is cleared to '0', software can add a TRB no later than IST [2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to '1', software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed.

8.11.5.4 0x000C xHC Structural Parameters 3 Register (Default Value:0x0200_000A)

Offset: 0x000C			Register Name: HCSPARAMS3
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0200	U2DEL U2 Device Exit Latency Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 0000h Zero 0001h Less than 1 µs. 0002h Less than 2 µs. ... 07FFh Less than 2047 µs.

Offset: 0x000C			Register Name: HCSPARAMS3
Bit	Read/Write	Default/Hex	Description
			0800-FFFFh Reserved
15:8	/	/	/
7:0	R	0x0A	U1DEL U1 Device Exit Latency Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 μs 02h Less than 2 μs. ... 0Ah Less than 10 μs. 0B-FFh Reserved

8.11.5.5 0x0010 xHC Capability Parameters Register (Default Value:0x0110_FFCC)

Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	R	0x0110	xECP xHCI Extended Capabilities Pointer This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, for Base to the beginning of the first extended capability. Extended Capabilities Offset = xECP<<2 =0x0110<<2 = 0x0440.
15:12	R	0xF	MaxPSASize Maximum Primary Stream Array Size This field indentifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array Size = $2^{MaxPSASize+1}$. Valid *MaxPSASize* values are 0 to 15, where '0' indicates that Streams are not supported
11	R	0x1	CFC Contiguous Frame ID Capability This flag indicates that the host controller implementation is capable of matching the Frame ID of consecutive Isoch TDs.
10	R	0x1	SEC Stopped EDTLA Capability

Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
			This flag indicates that the host controller implementation Stream Context support a Stopped EDTLA field.
9	R	0x1	SPC Stopped - Short Packet Capability This flag indicates that the host controller implementation is capable of generating a *Stopped - Short Packet* Completion Code.
8	R	0x1	PAE Parse All Event Data This flag indicates whether the host controller implementation Parses all Event Data TRBs while advancing to the next TD after a Short Packet, or it skips all but the first Event Data TRB. A '1' in this bit indicates that all Event Data TRBs are parsed. A '0' in this bit indicates that only the first Event Data TRB is parsed
7	R	0x1	NSS No Secondary SID Support This flag indicates whether the host controller implementation supports Secondary Stream IDs. A '1' in this bit indicates that Secondary Stream ID decoding is not supported. A '0' in this bit indicates that Secondary Stream ID decoding is supported.
6	R	0x1	LTC Latency Tolerance Messaging Capability This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). A '1' in this bit indicates that LTM is supported. A '0' in this bit indicates that LTM is not supported.
5	R	0x0	LHRC Light HC Reset Capability This flag indicates whether the host controller implementation supports a Light Host Controller Reset. A '1' in this bit indicates that Light Host Controller Reset is supported. A '0' in this bit indicates that Light Host Controller Reset is not supported. The value of this flag affects the functionality of the *Light Host Controller Reset* (LHCRST) flag in the USBCMD register

Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
4	R	0x0	PIND Port Indicators This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	R	0x1	PPC Port Power Control This flag indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the *PP* flag in each port status and control register
2	R	0x1	CSZ Context Size If this bit is set to '1', then the xHC uses 64-byte Context data structures. If this bit is cleared to '0', then the xHC uses 32-byte Context data structures. Note: This flag does *not* apply to Stream Contexts.
1	R	0x0	BNC BW Negotiation Capability This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: Value Description 0 BW Negotiation not implemented 1 BW Negotiation implemented
0	R	0x0	AC64 64-bit Addressing Capability This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: Value Description 0 32-bit address memory pointers implemented

Offset: 0x0010			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
			1 64-bit address memory pointers implemented If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.

8.11.5.6 0x0014 xHC Doorbell Offset Register (Default Value: 0x0000_2000)

Offset: 0x0014			Register Name: HCDBOFF
Bit	Read/Write	Default/Hex	Description
31:2	R	0x800	DBOFF Doorbell Array Offset This field defines the offset in Dwords of the Doorbell Array base address from the Base
1:0	/	/	/

8.11.5.7 0x0018 xHC Runtime Register Space Offset Register (Default Value: 0x0000_1000)

Offset: 0x0018			Register Name: HCRTSOFF
Bit	Read/Write	Default/Hex	Description
31:5	R	0x80	RTSOFF Runtime Register Space Offset This field defines the 32-byte offset of the xHCI Runtime Registers from the Base.
4:0	/	/	/

8.11.5.8 0x001C xHC Capability Parameters 2 Register (Default Value: 0x0000_003F)

Offset: 0x001C			Register Name: HCCPARAMS2
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	CIC Configuration Information Capability. This bit indicates if the xHC supports extended Configuration Information. When this bit is 1, the *Configuration Value*, *Interface Number*, and *Alternate Setting* fields in the Input Control Context

Offset: 0x001C			Register Name: HCCPARAMS2
Bit	Read/Write	Default/Hex	Description
			are supported. When this bit is 0, the extended Input Control Context fields are not supported.
4	R	0x1	LEC Large ESIT Payload Capability. This bit indicates whether the xHC supports ESIT Payloads greater than 48K bytes. When this bit is '1', ESIT Payloads greater than 48K bytes are supported. When this bit is '0', ESIT Payloads greater than 48K bytes are not supported.
3	R	0x1	CTC Compliance Transition Capability. This bit indicates whether the xHC USB3 Root Hub ports support the *Compliance Transition Enabled* (CTE) flag. When this bit is '1', USB3 Root Hub port state machine transitions to the Compliance substate shall be explicitly enabled software. When this bit is '0', USB3 Root Hub port state machine transitions to the Compliance substate are automatically enabled.
2	R	0x1	FSC Force Save Context Capability. This bit indicates whether the xHC supports the *Force Save Context Capability*. When this bit is '1', the *Save State* operation shall save any cached Slot, Endpoint, Stream or other Context information to memory.
1	R	0x1	CMC Configure Endpoint Command Max Exit Latency Too Large Capability. This bit indicates whether a *Configure Endpoint Command* is capable of generating a *Max Exit Latency Too Large Capability Error*. When this bit is '1', a *Max Exit Latency Too Large Capability Error* may be returned by a *Configure Endpoint Command*. When this bit is '0', a *Max Exit Latency Too Large Capability Error* shall not be returned by a *Configure Endpoint Command*. This capability is enabled by the *CME* flag in the USBCMD register.
0	R	0x1	U3C U3 Entry Capability. This bit indicates whether the xHC Root Hub ports

Offset: 0x001C			Register Name: HCCPARAMS2
Bit	Read/Write	Default/Hex	Description
			support port Suspend Complete notification. When this bit is '1', *PLC* shall be asserted on any transition of *PLS* to the *U3* State.

8.11.5.9 0x0020 xHC USB Command Register (Default Value:0x0000_0000)

Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	CME CEM Enable When set to '1', a *Max Exit Latency Too Large Capability Error* may be returned by a *Configure Endpoint Command*. When cleared to '0', a *Max Exit Latency Too Large Capability Error* shall not be returned by a *Configure Endpoint Command.* This bit is *Reserved* if *CMC* = '0'.
12	R/W	0x0	SPE Stopped - Short Packet Enable When set to '1', the xHC may generate a *Stopped - Short Packet* Completion Code. This bit is *Reserved* if *CMC* = '0'.
11	R/W	0x0	EU3S Enable U3 MFINDEX Stop When set to '1', the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to '0' the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	R/W	0x0	EWE Enable Wrap Event When set to '1', the xHC shall generate a MFINDEX (Micro-Frame Index) Wrap Event every time the MFINDEX register transitions from 0x03FFF to 0. When cleared to '0' no MFINDEX Wrap Events are generated.
9	R/W	0x0	CRS Controller Restore State When set to '1', and HCHalted (HCH) = '1', then the xHC shall perform a Restore State operation and

Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
			restore its internal state. When set to '1' and Run/Stop (R/S) = '1' or HCHalted (HCH) = '0', or when cleared to '0', no Restore State operation shall be performed. This flag always returns '0' when read. Refer to the Restore State Status (RSS) flag in the HCUSBSTS register for information on Restore State completion. Note that undefined behavior may occur if a Restore State operation is initiated while Save State Status (SSS) = '1'.
8	R/W	0x0	CSS Controller Save State When written by software with '1' and *HCHalted* (HCH) = '1', then the xHC shall save any internal state (that may be restored by a subsequent Restore State operation) and if *FSC* = '1' any cached Slot, Endpoint, Stream, or other Context information (so that software may save it). When written by software with '1' and *HCHalted* (HCH) = '0', or written with '0', no Save State operation shall be performed. This flag always returns '0' when read. Refer to the *Save State Status* (SSS) flag in the USBSTS register for information on Save State completion. Note that undefined behavior may occur if a Save State operation is initiated while *Restore State Status* (RSS) = '1'.
7:4	/	/	/
3	R/W	0x0	HSEE Host System Error Enable When this bit is a '1', and the HSE bit in the HCUSBSTS register is a '1', the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.
2	R/W	0x0	INTE Interrupter Enable This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is a '1', then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the

Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
			next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism.
1	R/W	0x0	HCRST Host Controller Reset This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes a '1' to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports; however, a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller in order to return the host controller to an operational state. This bit is cleared to '0' by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a '0' to this bit and shall not write any xHC Operational or Runtime registers while HCRST is '1'. Note, the completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to '1' when the HCHalted (HCH) bit in the USBSTS register is a '0'. Attempting to reset an actively running host controller may result in undefined behavior.
0	R/W	0x0	RS Run/Stop 0x1: Run 0x0: Stop When set to '1'm the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to a '1'. When this bit is cleared to '0', the xHC completes any current or queued

Offset: 0x0020			Register Name: HCUSBCMD
Bit	Read/Write	Default/Hex	Description
			commands or TDs, and any USB transactions associated with them, then halts. The xHC shall halt within 16ms, after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the HCUSBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is '1'). Doing so may yield undefined results. Writing a '0' to this flag when the xHC is in the Running state (i.e. HCH='0') and any Event Rings are in the Event Ring Full state may yield undefined results.

8.11.5.10 0x0024 xHC USB Status Register (Default Value:0x0000_0001)

Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R	0x0	HCE Host Controller Error This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC.
11	R	0x0	CNR Controller Not Ready Software shall not write any Doorbell or Operational register of the xHC, other than the HCUSBSTS register, until CNR = '0'. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared ('0') until the next Chip Hardware Reset.
10	R/W1C	0x0	SRE Save/Restore Error If an error occurs during a Save or Restore operation this bit shall be set to '1'. This bit shall be cleared to '0' when a Save or Restore operation is initiated or when written with '1'.

Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
			Note: This bit can be cleared by software writing '1'.
9	R	0x0	RSS Restore State Status When the Controller Restore State (CRS) flag in the HCUSBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to '0'.
8	R	0x0	SSS Save State Status When the Controller Save State (CSS) flag in the HCUSBCMD register is written with '1' this bit shall be set to '1' and remain 1 while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to '0'.
7:5	/	/	/
4	R/W1C	0x0	PCD Port Change Detect The xHC sets this bit to a '1' when any port has a change bit transition from a '0' to a '1'. This bit is allowed to be maintained in the Aux Power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits. This bit provides system software an efficient means of determining if there has been Root Hub port activity. **Note: This bit can be cleared by software writing '1'.**
3	R/W1C	0x0	EINT Event Interrupt The xHC sets this bit to '1' when the Interrupt Pending (IP) bit of any Interrupter transitions from '0' to '1'. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition may occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition shall be lost. **Note: This bit can be cleared by software writing '1'.**
2	R/W1C	0x0	HSE

Offset: 0x0024			Register Name: HCUSBSTS
Bit	Read/Write	Default/Hex	Description
			Host System Error The xHC sets this bit to '1' when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the HCUSBCMD register is a '1', the xHC shall also assert out-of-band error signaling to the host. **Note: This bit can be cleared by software writing '1'.**
1	/	/	/
0	R	0x1	HCH HC Halted This bit is a '0' whenever the Run/Stop (R/S) bit is a '1'. The xHC sets this bit to '1' after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to '0', either by software or by the xHC hardware (e.g. internal error). If this bit is '1', then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC, and any received Transaction Packet shall be dropped.

8.11.5.11 0x0028 xHC Page Size Register (Default Value:0x0000_0001)

Offset: 0x0028			Register Name: HCPAGESIZE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0001	PageSize Page Size This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes.

8.11.5.12 0x0034 xHC Device Notification Control Register (Default Value:0x0000_0000)

Offset: 0x0034			Register Name: HCDNCTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

Offset: 0x0034			Register Name: HCDNCTRL
Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0000	NE Notification Enable (N0-N15) When a Notification Enable bit is set, a Device Notification Event shall be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), etc.

8.11.5.13 0x0038 xHC Command Ring Control Low Register (Default Value:0x0000_0000)

Offset: 0x0038			Register Name: HCCRCLR
Bit	Read/Write	Default/Hex	Description
31:6	R/W	0x00	CRPL Command Ring Pointer Low This field defines bit [31:6] of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = '1'. If the CRCR is written while the Command Ring is stopped (CCR = '0'), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CCR = '0') then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns '0'. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
5:4	/	/	/
3	R	0x0	CRR Command Ring Running This flag is set to '1' if the Run/Stop (R/S) bit is '1' and the Host Controller Doorbell register is written with

Offset: 0x0038			Register Name: HCCRCLR
Bit	Read/Write	Default/Hex	Description
			the DB Reason field set to Host Controller Command. It is cleared to '0' when the Command Ring is "stopped" after writing a '1' to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to '0'.
2	R/W1S	0x0	CA Command Abort Writing a '1' to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit always returns '0'.
1	R/W1S	0x0	CS Command Stop Writing a '1' to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = '0'. Reading this bit shall always return '0'.
0	R/W	0x0	RSC Ring Cycle State This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Writes to this flag are ignored if Command Ring Running (CRR) is '1'. If the HCCRC*R is written while the Command Ring is

Offset: 0x0038			Register Name: HCCRCLR
Bit	Read/Write	Default/Hex	Description
			stopped (CRR = '0'), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the HCCRC*R is not written while the Command Ring is stopped (CRR = '0'), then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns '0'.

8.11.5.14 0x003C xHC Command Ring Control High Register (Default Value:0x0000_0000)

Offset: 0x003C			Register Name: HCCRCHR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00	CRPH Command Ring Pointer High This field defines bit[63:32] of the initial value of the 64-bit Command Ring Dequeue Pointer.

8.11.5.15 0x0050 xHC Device Context Base Address Array Pointer Low Register (Default Value:0x0000_0000)

Offset: 0x0050			Register Name: HCDCBAAPLR
Bit	Read/Write	Default/Hex	Description
31:6	R/W	0x00	DCBAAPL Device Context Base Address Array Pointer Low This field defines bit [31:6] of the 64-bit base address of Device Context Pointer Array. A table of address pointers that reference Device Context structures for the device attached to the host. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
5:0	/	/	/

8.11.5.16 0x0054 xHC Device Context Base Address Array Pointer High Register (Default Value:0x0000_0000)

Offset: 0x0054			Register Name: HCDCBAAPHR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00	DCBAAPH Device Context Base Address Array Pointer High This field defines bit[63:32] of the 64-bit base address of Device Context Pointer Array.

8.11.5.17 0x0058 xHC Configure Register (Default Value:0x0000_0000)

Offset: 0x0058			Register Name: HCCONFIG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	CIE Configuration Information Enable When set to '1', the software shall initialize the *Configuration Value*, *Interface Number*, and *Alternate Setting* fields in the Input Control Context when it is associated with a Configure Endpoint Command. When this bit is '0', the extended Input Control Context fields are not supported.
8	R/W	0x0	U3E U3 Entry Enable When set to '1', the xHC shall assert the *PLC* flag ('1') when a Root Hub port transitions to the U3 State.
7:0	R/W	0x00	MaxSlotsEn Max Device Slots Enabled This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running (Run/Stop (R/S) = '1').

8.11.5.18 0x0420 xHC Port1 Status and Control Register (USB2 Protocol) (Default Value:0x0000_02A0)

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WPR Warm Port Reset When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be reserved.
30	R	0x0	DR Device Removable This flag indicates if this port has a removable device attached. 0: Device is removable 1: Device is non-removable
29:28	/	/	/
27	R/W	0x0	WOE Wake on Over-Current Enable Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events.
26	R/W	0x0	WDE Wake on Disconnect Enable Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events.
25	R/W	0x0	WCE Wake on Connect Enable Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events.
24	R	0x0	CAS Cold Attach Status This bit is set when Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable advance to the Enabled state. Software shall clear this bit by writing a '1' to WPR or

<table>
<tr><th colspan="3">Offset: 0x0420</th><th>Register Name: HCPORT1SC</th></tr>
<tr><th>Bit</th><th>Read/Write</th><th>Default/Hex</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>the xHC shall clear this bit if CCS transitions to ‘1’.
This flag is ‘0’ if PP is ‘0’ or for USB2 protocol ports.</td></tr>
<tr><td>23</td><td>R/W1C</td><td>0x0</td><td>CEC
Port Config Error Change
This flag indicates that the port failed to configure its link partner.
0: No Change
1: Port Config Error Detected
Software shall clear this bit by writing a ‘1’ to it.</td></tr>
<tr><td>22</td><td>R/W1C</td><td>0x0</td><td>PLC
Port Link State Change
This flag is set to ‘1’ due to the following PLS transitions:
<table>
<tr><th>Transition</th><th>Condition</th></tr>
<tr><td>U3 -> Resume</td><td>Wakeup signaling from a device</td></tr>
<tr><td>Resume -> Recovery -> U0</td><td>Device Resume complete (USB3 protocol ports only)</td></tr>
<tr><td>Resume -> U0</td><td>Device Resume complete (USB2 protocol ports only)</td></tr>
<tr><td>U3 -> Recovery -> U0</td><td>Software Resume complete (USB3 protocol ports only)</td></tr>
<tr><td>U3 -> U0</td><td>Software Resume complete (USB2 protocol ports only)</td></tr>
<tr><td>U2 -> U0</td><td>L1 Resume complete (USB2 protocol ports only)</td></tr>
<tr><td>U0 -> U0</td><td>L1 Entry Reject (USB2 protocol ports only)</td></tr>
<tr><td>Any state -> Inactive</td><td>Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM.</td></tr>
<tr><td>Any State -> U3</td><td>U3 Entry complete. Note: PLC is asserted only if U3E = ‘1’</td></tr>
</table>
Note that this flag shall not be set if the PLS</td></tr>
</table>

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			transition was due to software setting PP to ‘0’. '0' = No change. '1' = Link Status Changed. Software shall clear this bit by writing a '1' to it.
21	R/W1C	0x0	PRC Port Reset Change This flag is set to ‘1’ due a ‘1’ to ‘0’ transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to ‘1’ if the reset processing was forced to terminate due to software clearing PP or PED to '0'. ‘0’ = No change. ‘1’ = Reset complete. Software shall clear this bit by writing a ‘1’ to it.
20	R/W1C	0x0	OCC Over-Current Change This bit shall be set to a ‘1’ when there is a ‘0’ to ‘1’ or ‘1’ to ‘0’ transition of Over-Current Active (OCA). Software shall clear this bit by writing a ‘1’ to it.
19	R/W1C	0x0	WRC Warm Port Reset Change This bit is set when Warm Reset processing on this port completes. ‘0’ = No change. ‘1’ = Warm Reset complete. Note that this flag shall not be set to ‘1’ if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a ‘1’ to it. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be Reserved.
18	R/W1C	0x0	PEC Port Enabled/Disabled Change ‘1’ = change in *PED*. ‘0’ = No change. Note that this flag shall not be set if the PED transition was due to software setting PP to ‘0’. Software shall clear this bit by writing a ‘1’ to it. For a USB2 protocol port, this bit shall be set to ‘1’ only when the port is disabled due to the appropriate conditions existing at the EOF2 point For a USB3 protocol port, this bit shall never be set to ‘1’.
17	R/W1C	0x0	CSC

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			Connect Status Change '1' = Change in *CCS*. '0' = No change. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it.
16	R/W	0x0	LWS Port Link State Write Strobe When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14	R/W	0x0	PIC Port Indicator Control Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: 0: Port indicators are off 1: Amber 2: Green 3: Undefined This field is '0' if PP is '0'.
13:10	R	0x0	PSPD Port Speed This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate *Undefined Speed*. 0: Undefined Speed 1-15: Protocol Speed ID (PSI) 1: Full-speed 12 MB/s

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			2: Low-speed 1.5 Mb/s 3: High-speed 480 Mb/s 4: SuperSpeed 5 Gb/s. **Note: This field is invalid on a USB2 protocol port until after the port is reset.**
9	R/W	0x1	PP Port Power This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. 0: This port is in the Powered-off state. 1: This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' =on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power from the port).
8:5	R/W	0x5	PLS Port Link State Default = RxDetect ('5'). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field.

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			System software may also write this field to force a Disabled to Disconnected state transition of the port. Write value and Description: 0: The link shall transition to a U0 state from any of the U states. 2: USB2 protocol ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 10: USB3 protocol ports only. Shall enable a link transition to the Compliance state, i.e. *CTE* = '1'. 1, 4, 6-9,11-14: Ignored. 15: USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit sub-state, else ignored. **Note: The Port Link State Write Strobe (LWS) shall also be set to '1' to write this field.** **For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of '0' shall de-assert L1 signaling on the USB. Writing a value of '1' shall have no effect. The U1 state shall never be reported by a USB2 protocol port.** Read value and Meaning: 0: Link is in the U0 State

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect Stated 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12-14: Reserved 15: Link is in the Resume State This field is undefined if PP = '0'. **Note: Transitions between different states are not reflected until the transition is complete.**
4	R/W1S	0x0	PR Port Reset '1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to this flag to transition a USB2 port from the Polling state to the Enabled state. This flag is '0' if PP is '0'.
3	R	0x0	OCA Over-Current Active '1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
2	/	/	/
1	R/W1CS	0x0	PED

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			Port Enabled/Disabled Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bit. This flag is '0' if PP is '0'.
0	R	0x0	CCS Current Connect Status '1' = A device is connected to the port. '0' = A device is not connected. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be

Offset: 0x0420			Register Name: HCPORT1SC
Bit	Read/Write	Default/Hex	Description
			set to '1'. This flag is '0' if PP is '0'.

8.11.5.19 0x0424 xHC Port1 PM Status and Control Register (USB2 Protocol) (Default 0x0424 Value:0x0000_0000)

Offset: 0x0424			Register Name: HCPORT1PMSC
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	PTC Port Test Control (Test Mode) When this field is '0', the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB2 protocol port are: Value / Test Mode 0x0 / Test mode not enabled 0x1 / Test J_STATE 0x2 / Test K_STATE 0x3 / Test SE0_NAK 0x4 / Test Packet 0x5 / Test FORCE_ENABLE 0x6-0xE / Reserved 0xF / Port Test Control Error Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes.
27:17	/	/	/
16	R/W	0x0	HLE Hardware LPM Enable If this bit is set to '1', then hardware controlled LPM shall be enabled for this port. **Note: If the USB2 Hardware LMP Capability is not supported (HLC = '0') this field shall be Reserved.**
15:8	R/W	0x0	L1DS

<table>
<tr><td colspan="3">Offset: 0x0424</td><td>Register Name: HCPORT1PMSC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>L1 Device Slot
System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of ‘0’ indicates no device is present. The xHC uses this field to lookup information necessary to generate the LMP Token packet.</td></tr>
<tr><td>7:4</td><td>R/W</td><td>0x0</td><td>BESL
Best Effort Service Latency
System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1.</td></tr>
<tr><td>3</td><td>R/W</td><td>0x0</td><td>RWE
Remote Wake Enable
System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.</td></tr>
<tr><td>2:0</td><td>R</td><td>0x0</td><td>L1S
L1 Status
This field is used by software to determine whether an L1-based suspend request (LMP transition) was successful, specifically:
<table>
<tr><td>Value</td><td>Meaning</td></tr>
<tr><td>0x0</td><td>Invalid – This field shall be ignored by software.</td></tr>
<tr><td>0x1</td><td>Success – Port successfully transitioned to L1 (ACK)</td></tr>
<tr><td>0x2</td><td>Not Yet – Device is unable to enter L1 at this time (NYET)</td></tr>
<tr><td>0x3</td><td>Not Supported – Device does not support L1 transitions (STALL)</td></tr>
<tr><td>0x4</td><td>Timeout/Error – Device</td></tr>
<tr><td>0x5-0x7</td><td>Reserved</td></tr>
</table>
The value of this field is only valid when the port resides in the L0 or L1 state (PLS = ‘0’ or ‘2’).</td></tr>
</table>

8.11.5.20 0x0428 xHC Port1 Link Info Register (USB2 Protocol) (Default Value:0x0000_0000)

Offset: 0x0428			Register Name: HCPORT1LI
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.11.5.21 0x0430 xHC Port2 Status and Control Register (USB3 Protocol) (Default Value:0x000002A0)

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WPR Warm Port Reset When software writes a '1' to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to '1'. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return '0' when read. This flag only applies to USB3 protocol ports. For USB2 protocol ports it shall be reserved.
30	R	0x0	DR Device Removable This flag indicates if this port has a removable device attached. 0: Device is removable 1: Device is non-removable
29:28	/	/	/
27	R/W	0x0	WOE Wake on Over-Current Enable Writing this bit to a '1' enables the port to be sensitive to over-current conditions as system wake-up events.
26	R/W	0x0	WDE Wake on Disconnect Enable Writing this bit to a '1' enables the port to be sensitive to device disconnects as system wake-up events.
25	R/W	0x0	WCE Wake on Connect Enable Writing this bit to a '1' enables the port to be sensitive to device connects as system wake-up events.
24	R	0x0	CAS

<table>
<tr><td colspan="3">Offset: 0x0430</td><td>Register Name: HCPORT2SC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>Cold Attach Status
This bit is set when Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable advance to the Enabled state.
Software shall clear this bit by writing a '1' to WPR or the xHC shall clear this bit if CCS transitions to ‘1’.
This flag is ‘0’ if PP is ‘0’ or for USB2 protocol ports.</td></tr>
<tr><td>23</td><td>R/W</td><td>0x0</td><td>CEC
Port Config Error Change
This flag indicates that the port failed to configure its link partner.
0: No Change
1: Port Config Error Detected
Software shall clear this bit by writing a ‘1’ to it.</td></tr>
<tr><td>22</td><td>R/W</td><td>0x0</td><td>PLC
Port Link State Change
This flag is set to ‘1’ due to the following PLS transitions:
<table>
<tr><td>Transition</td><td>Condition</td></tr>
<tr><td>U3 -> Resume</td><td>Wakeup signaling from a device</td></tr>
<tr><td>Resume -> Recovery -> U0</td><td>Device Resume complete (USB3 protocol ports only)</td></tr>
<tr><td>Resume -> U0</td><td>Device Resume complete (USB2 protocol ports only)</td></tr>
<tr><td>U3 -> Recovery -> U0</td><td>Software Resume complete (USB3 protocol ports only)</td></tr>
<tr><td>U3 -> U0</td><td>Software Resume complete (USB2 protocol ports only)</td></tr>
<tr><td>U2 -> U0</td><td>L1 Resume complete (USB2 protocol ports only)</td></tr>
<tr><td>U0 -> U0</td><td>L1 Entry Reject (USB2 protocol ports only)</td></tr>
</table></td></tr>
</table>

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			<table><tr><td>Any state -> Inactive</td><td>Error (USB3 protocol ports only). Note: PLC is asserted only if there is an SS.Inactive.Disconnect.Detect to SS.Inactive.Quiet transition in the LTSSM.</td></tr><tr><td>Any State -> U3</td><td>U3 Entry complete. Note: *PLC* is asserted only if *U3E* = '1'</td></tr></table> Note that this flag shall not be set if the PLS transition was due to software setting PP to '0'.
21	R/W1C	0x0	PRC Port Reset Change This flag is set to '1' due a '1' to '0' transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. Note that this flag shall not be set to '1' if the reset processing was forced to terminate due to software clearing PP or PED to '0'. '0' = No change. '1' = Reset complete. Software shall clear this bit by writing a '1' to it.
20	R/W1C	0x0	OCC Over-Current Change This bit shall be set to a '1' when there is a '0' to '1' or '1' to '0' transition of Over-current Active (OCA). Software shall clear this bit by writing a '1' to it.
19	R/W1C	0x0	WRC Warm Port Reset Change This bit is set when Warm Reset processing on this port completes. '0' = No change. '1' = Warm Reset complete. Note that this flag shall not be set to '1' if the Warm Reset processing was forced to terminate due to software clearing PP or PED to '0'. Software shall clear this bit by writing a '1' to it. This bit only applies to USB3 protocol ports. For USB2 protocol ports it shall be Reserved.
18	R/W1C	0x0	PEC Port Enabled/Disabled Change Note that this flag shall not be set if the PED

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			transition was due to software setting PP to '0'. Software shall clear this bit by writing a '1' to it. For a USB2 protocol port, this bit shall be set to '1' only when the port is disabled due to the appropriate conditions existing at the EOF2 point For a USB3 protocol port, this bit shall never be set to '1'.
17	R/W1C	0x0	CSC Connect Status Change This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. Note that this flag shall not be set if the CCS transition was due to software setting PP to '0', or the CAS transition was due to software setting WPR to '1'. The xHC sets this bit to '1' for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it.
16	R/W	0x0	LWS Port Link State Write Strobe When this bit is set to '1' on a write reference to this register, this flag enables writes to the PLS field. When '0', write data in PLS field is ignored. Reads to this bit return '0'.
15:14	R/W	0x0	PIC Port Indicator Control Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS register is a '0'. If PIND bit is a '1', then the bit encodings are: 0: Port indicators are off 1: Amber 2: Green 3: Undefined This field is '0' if PP is '0'.
13:10	R	0x0	PSPD Port Speed

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			This field identifies the speed of the attached USB Device. This field is only relevant if a device is attached (CCS = '1') in all other cases this field shall indicate *Undefined Speed*. 0: Undefined Speed 1-15: Protocol Speed ID (PSI) 1: Full-speed 12 MB/s 2: Low-speed 1.5 Mb/s 3: High-speed 480 Mb/s 4: SuperSpeed 5 Gb/s. **Note: This field is invalid on a USB2 protocol port until after the port is reset.**
9	R/W	0x1	PP Port Power This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a '0' the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = '0' if PPC = '0'. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again, undefined behavior may occur if this procedure is not followed. 0: This port is in the Powered-off state. 1: This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS register is '1', then xHC has port power control switches and this bit represents the current setting of the switch ('0' = off, '1' =on). If the Port Power Control (PPC) flag in the HCCPARAMS register is '0', then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from a '1' to '0' (removing power

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			from the port).
8:5	R/W	0x5	PLS Port Link State Default = RxDetect (‘5’). This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write value and Description: 0: The link shall transition to a U0 state from any of the U states. 2: USB2 protocol ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 10: USB3 protocol ports only. Shall enable a link transition to the Compliance state, i.e. *CTE* = ‘1’. 1, 4, 6-9,11-14: Ignored. 15: USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit sub-state, else ignored. **Note: The Port Link State Write Strobe (LWS) shall also be set to ‘1’ to write this field.** **For USB2 protocol ports: Writing a value of '2' to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine**

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			if the transition to the U2 state was successful. Writing a value of '0' shall de-assert L1 signaling on the USB. Writing a value of '1' shall have no effect. The U1 state shall never be reported by a USB2 protocol port. Read value and Meaning: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect Stated 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12-14: Reserved 15: Link is in the Resume State This field is undefined if PP = '0'. Note: Transitions between different states are not reflected until the transition is complete.
4	R/W	0x0	PR Port Reset 1' = Port Reset signaling is asserted. '0' = Port is not in Reset. When software writes a '1' to this bit (from a '0') the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Spec. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. Note that software shall write a '1' to this flag to transition a USB2 port from the Polling state to the Enabled state. This flag is '0' if PP is '0'.
3	R	0x0	OCA Over-Current Active

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			'1' = This port currently has an over-current condition. '0' = This port does not have an over-current condition. This bit shall automatically transition from a '1' to a '0' when the over-current condition is removed.
2	/	/	/
1	R/W	0x0	PED Port Enabled/Disabled 1' = Enabled. '0' = Disabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing a '1' to this flag. A port may be disabled by software writing a '1' to this flag. This flag shall automatically be cleared to '0' by a disconnect event or other fault condition. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = '0') downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = '1') to transition PED to '1' and the port to the Enabled state. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to '1' upon the completion of successful link training. When the port is in the Disabled state, software shall write a '5' (RxDetect) to the PLS field to transition the port to the Disconnected state. PED shall automatically be cleared to '0' when PR is set to '1', and set to '1' when PR transitions from '1' to '0' after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. Note that when software writes this bit to a '1', it shall also write a '0' to the PR bit.

Offset: 0x0430			Register Name: HCPORT2SC
Bit	Read/Write	Default/Hex	Description
			This flag is '0' if PP is '0'.
0	R	0x0	CCS Current Connect Status '1' = A device is connected to the port. '0' = A device is not connected This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to '1'. This flag is '0' if PP is '0'.

8.11.5.22 0x0434 xHC Port2 PM Status and Control Register (USB3 Protocol) (Default Value:0x0000_0000)

Offset: 0x0434			Register Name: HCPORT2PMSC
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	FLA Force Link PM Accept When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted. When this bit is cleared to '0', the port shall generate a *Set Link Function* LMP with the Force_LinkPM_Accept bit de-asserted This flag shall be set to '0' by the assertion of PR to '1' or when CCS = transitions from '0' to '1'. Writes to this flag have no effect if PP = '0'. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from '0' to '1'. Refer to Sections 8.4.1, 10.4.2.2 and 10.4.2.9 of the USB3 specification for more details. Improper use of the SS Force_LinkPM_Accept functionality can impact the performance of the link significantly. This bit shall only be used for compliance and testing purposes. Software shall ensure that there are no pending packets at the link level before setting this bit. This flag is '0' if PP is '0'.
15:8	R/W	0x00	U2TO U2 Timeout

Offset: 0x0434			Register Name: HCPORT2PMSC
Bit	Read/Write	Default/Hex	Description
			Timeout value for U2 inactivity timer. If equal to 0xFF, the port is disabled from initiating U2 entry. This field shall be set to '0' by the assertion of PR to '1'. The following are permissible values: 0x00: Zero 0x01: 256 us 0x02: 512 us ... 0xFE: 65.024 ms 0xFF: Infinite A U2 Inactivity Timeout LMP shall be sent by the xHC to the device connected on this port when this field is written. Refer to Sections 8.4.3 and 10.4.2.10 of the USB3 specification for more details.
7:0	R/W	0x00	U1TO U1 Timeout Timeout value for U1 inactivity timer. If equal to 0xFF, the port is disabled from initiating U1 entry, this field shall be set to '0' by the assertion of PR to '1'. The following are permissible values: 0x00: Zero 0x01: 1 us 0x02: 1 us ... 0x7F: 127us 0x80-0xFE: Reserved 0xFF: Infinite

8.11.5.23 0x0438 xHC Port2 Link Info Register (USB3 Protocol) (Default Value:0x0000_0000)

Offset: 0x0438			Register Name: HCPORT2LI
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R	0x0	RLC Rx Lane Count This field that identifies the number of Receive Lanes negotiated by the port. This is a "zero-based" value, where 0 to 15 represents Lane Counts of 1 to

Offset: 0x0438			Register Name: HCPORT2LI
Bit	Read/Write	Default/Hex	Description
			16, respectively. This value is valid only when *CCS* = '1'. *RLC* shall equal '0' for a simplex Sublink.
19:16	R	0x0	TLC Tx Lane Count This field that identifies the number of Transmit Lanes negotiated by the port. This is a "zero-based" value, where 0 to 15 represents Lane Counts of 1 to 16, respectively. This value is valid only when *CCS* = '1'. *TLC* shall equal '0' for a simplex Sublink.
15:0	R	0x0000	LEC Link Error Count This field returns the number of link errors detected by the port. This value shall be reset to '0' by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from '1' to '0', or when CCS = transitions from '0' to '1'.

8.11.5.24 0x1000 xHC Microframe Index Register (Default Value:0x0000_0000)

Offset: 0x1000			Register Name: HCMFINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R	0x0000	MFI Micro-Frame Index The value in this register increments at the end of each micro-frame (e.g. 125us). Bits [13:3] may be used to determine the current 1ms. Frame index.

8.11.5.25 0x1020 xHC Interrupt 0 Management Register (Default Value:0x0000_0000)

Offset: 0x1020			Register Name: HCIMAN0
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	IE Interrupt Enable This flag specifies whether the interrupter is capable of generating an interrupt. When this bit and the IP bit are set, the interrupter shall generate an interrupt when the interrupter Moderation Counter reaches '0'. If this bit is '0', then the interrupter is

Offset: 0x1020			Register Name: HCIMAN0
Bit	Read/Write	Default/Hex	Description
			prohibited from generation interrupts.
0	R/W1C	0x0	IP Interrupt Pending This flag represents the current state of the interrupter. If IP = '1', an interrupt is pending for this interrupter. A '0' value indicates that no interrupt is pending for interrupter. This bit can be cleared by software writing '1'.

8.11.5.26 0x1024 xHC Interrupt 0 Moderation Register (Default Value:0x0000_0FA0)

Offset: 0x1024			Register Name: HCIMOD0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	IMODC Interrupt Moderation Counter Down counter. Loaded with the IMODI value whenever IP is cleared to '0', counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP flags = '1', and EHB = '0'. This counter may be directly written by software at any time to alter the interrupt rate.
15:0	R/W	0x0FA0	IMODI Interrupt Moderation Interval Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = '0', EHB = '0', and the Event Ring is not empty. The default value is 4000 (1ms).

8.11.5.27 0x1028 xHC Interrupt 0 Event Ring Segment Table Size Register (Default Value:0x0000_0000)

Offset: 0x1028			Register Name: HCERSTSZ0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	ERSTSZ Event Ring Segment Table Size This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment

Offset: 0x1028			Register Name: HCERSTSZ0
Bit	Read/Write	Default/Hex	Description
			Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing a value of '0' to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing a value of '0' to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

8.11.5.28 0x1030 xHC Interrupt 0 Event Ring Segment Table Base Address Low Register (Default 0x1030 Value:0x0000_0000)

Offset: 0x1030			Register Name: HCERSTBAL0
Bit	Read/Write	Default/Hex	Description
31:6	R/W	0x0000	ERSTBAL Event Ring Segment Table Base Address Low This field defines the low order bits [31:6] of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. For Secondary Interrupters: This field may be modified at any time. For the Primary Interrupter: This field shall not be modified if *HCHalted* (HCH) = '0'. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
5:0	/	/	/

8.11.5.29 0x1034 xHC Interrupt 0 Event Ring Segment Table Base Address High Register (Default 0x1034 Value:0x0000_0000)

Offset: 0x1034			Register Name: HCERSTBAH0
Bit	Read/Write	Default/Hex	Description

Offset: 0x1034			Register Name: HCERSTBAH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0000	ERSTBAH Event Ring Segment Table Base Address High This field defines the high order bits [63:32] of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine: EREP Advancement to the Start State. For Secondary Interrupters: This field may be modified at any time. For the Primary Interrupter: This field shall not be modified if *HCHalted* (HCH) = '0'. This field shall not be modified if HCHalted(HCH) = '0'.

8.11.5.30 0x1038 xHC Interrupt 0 Event Ring Dequeue Poiter Low Register (Default Value:0x0000_0000)

Offset: 0x1038			Register Name: HCERDPL0
Bit	Read/Write	Default/Hex	Description
31:4	R/W	0x0000	ERDPL Event Ring Dequeue Pointer Low This field defines the low order bits [31:4] of the start address of the current Event Ring Dequeue Pointer. **Note: If a system is incapable of issuing Qword accesses, then writes to the 64-bit address fields shall be performed using 2 Dword accesses; low Dword-first, high-Dword second.**
3	R/W1C	0x0	EHB Event Handler Busy This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	R/W	0x0	DESI Dequeue ERST Segment Index This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

8.11.5.31 0x103C xHC Interrupt 0 Event Ring Dequeue Pointer High Register (Default Value:0x0000_0000)

Offset: 0x103C			Register Name: HCERDPH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0000	ERDPH Event Ring Dequeue Pointer High This field defines the high order bits [63:32] of the start address of the current Event Ring Dequeue Pointer.

8.11.5.32 0x2000 + 4*n (N = 0-64) xHC Doorbell Register N (n=0, 1, ……, 64) (Default Value:0x0000_0000)

Offset: 0x2000 + 4*n (N = 0-64)			Register Name: HCDBRn (N = 0-64)
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	DBSID Doorbell Stream ID If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams > 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Command Doorbells. This field returns '0' when read.
15:8	/	/	/
7:0	R/W	0x00	DBT Doorbell Target This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Note that Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (n = 1-64)

Offset: 0x2000 + 4*n (N = 0-64)			Register Name: HCDBRn (N = 0-64)
Bit	Read/Write	Default/Hex	Description
			0: Reserved 1: Control EP0 Enqueue Pointer Update 2: EP 1 OUT Enqueue Pointer Update 3: EP 1 IN Enqueue Pointer Update 4: EP 2 OUT Enqueue Pointer Update 5: EP 2 IN Enqueue Pointer Update ... 30: EP 15 OUT Enqueue Pointer Update 31: EP 15 IN Enqueue Pointer Update 32-247: Reserved 248-255: Vendor Defined Host Controller Doorbell (n = 0) 0: Command Doorbell 1-247: Reserved 248-255: Vendor Defined This field returns '0' when read and should be treated as "undefined" by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to '0'.

8.11.5.33 0x0440 xHC USB Legacy Support Capability Register (Default Value:0x0000_0401)

Offset: 0x0440			Register Name: HCUSBLEGSUP
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	OOS HC OS Owned Semaphore System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'.
23:17	/	/	/
16	R/W	0x0	BOS HC BIOS Owned Semaphore The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
15:8	R	0x04	NCP

Offset: 0x0440			Register Name: HCUSBLEGSUP
Bit	Read/Write	Default/Hex	Description
			Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability..
7:0	R	0x01	CID Capability ID This field identifies the xHCI Extended capability. Refer to xHCI Spec for a list of the valid xHCI extended capabilities. This extended capability requires one additional 32-bit register for control/status information (HCIUSBLEGCTLSTS), and this register is located at offset xECP+0x04.

8.11.5.34 0x0444 xHC USB Legacy Support Control/Status Register (Default Value:0x0000_0000)

Offset: 0x0444			Register Name: HCUSBLEGCTRLSTS
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	SBAR SMI on BAR This bit is set to '1' whenever the Base Address Register (BAR) is written. This bit can be cleared by software writing '1'.
30	R/W1C	0x0	SPC SMI on PCI Command This bit is set to '1' whenever the PCI Command Register is written. This bit can be cleared by software writing '1'.
29	R/W1C	0x0	SOOC SMI on OS Ownership Change This bit is set to '1' whenever the HC OS Owned Semaphore bit in HCUSBLEGSUP register transitions from '1' to '0' or '0' to '1'. This bit can be cleared by software writing '1'.
28:21	/	/	/
20	R	0x0	SHSE SMI on Host System Error Shadow bit of Host System Error (HSE) bit in the HCUSBSTS register. To clear this bit to a '0', system software shall write a '1' to the Host System Error (HSE) bit in the

Offset: 0x0444			Register Name: HCUSBLEGCTRLSTS
Bit	Read/Write	Default/Hex	Description
			HCUSBSTS register.
19:17	/	/	/
16	R	0x0	SEI SMI on Event Interrupt Shadow bit of Event Interrupt (EINT) bit in the HCUSBSTS register. This bit follows the state the Event Interrupt (EINT) bit in the HCUSBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set.
15	R/W	0x0	SBE SMI on BAR Enable When this bit is a '1' AND SMI on BAR is '1', then the host controller will issue an SMI.
14	R/W	0x0	SPCE SMI on PCI Command Enable When this bit is a '1' AND SMI on PCI Command is '1', then the host controller will issue an SMI.
13	R/W	0x0	SOOE SMI on OS Ownership Enable When this bit is a '1' AND the OS Ownership Change bit is '1', the host controller will issue an SMI.
12:5	/	/	/
4	R/W	0x0	SHSEE SMI on Host System Error Enable When this bit is a '1', and the SMI on Host System Error bit in this register is a '1', the host controller will issue an SMI immediately.
3:1	/	/	/
0	R/W	0x0	USE USB SMI Enable When this bit is a '1', and the SMI on Event Interrupt bit in this register is a '1', the host controller will issue an SMI immediately.

8.11.5.35 0x0490 xHC Support Protocol Capability 1 Revision Register (Default Value:0x0200_0402)

Offset: 0x0490			Register Name: HCSPC1REV
Bit	Read/Write	Default/Hex	Description
31:24	R	0x02	MajorRev Minor Revision Minor Specification Release Number in

Offset: 0x0490			Register Name: HCSPC1REV
Bit	Read/Write	Default/Hex	Description
			Binary-Coded Decimal. This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	R	0x00	MinorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	R	0x04	NCP Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability..
7:0	R	0x02	CID Capability ID This field identifies the xHCI Extended capability. Refer to xHCI Spec for a list of the valid xHCI extended capabilities.

8.11.5.36 0x0494 xHC Support Protocol Capability 1 String Register (Default Value:0x2042_5355)

Offset: 0x0494			Register Name: HCSPC1STR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x20425355	NAME Name String This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined.

8.11.5.37 0x0498 xHC Support Protocol Capability 1 Port Register (Default Value:0x0001_0101)

Offset: 0x0498			Register Name: HCSPC1PRT
Bit	Read/Write	Default/Hex	Description
31:28	R	0x0	PSIC Protocol Speed ID Count This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains.
27:16	R	0x001	PD

Offset: 0x0498			Register Name: HCSPC1PRT
Bit	Read/Write	Default/Hex	Description
			Protocol Defined This field is reserved for protocol specific definitions.
15:8	R	0x01	CPCNT Compatible Port Count This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are '1' to MaxPorts.
7:0	R	0x01	CPOFF Compatible Port Offset This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

8.11.5.38 0x04A0 xHC Support Protocol Capability 2 Revision Register (Default Value:0x0300_0002)

Offset: 0x04A0			Register Name: HCSPC2REV
Bit	Read/Write	Default/Hex	Description
31:24	R	0x03	MajorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	R	0x00	MinorRev Minor Revision Minor Specification Release Number in Binary-Coded Decimal. This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	R	0x00	NCP Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability..
7:0	R	0x02	CID Capability ID This field identifies the xHCI Extended capability. Refer to xHCI Spec for a list of the valid xHCI extended capabilities.

8.11.5.39 0x04A4 xHC Support Protocol Capability 2 String Register (Default Value:0x2042_5355)

Offset: 0x04A4			Register Name: HCSPC2STR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x20425355	NAME Name String This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined.

8.11.5.40 0x04A8 xHC Support Protocol Capability 2 Port Register (Default Value:0x0000_0102)

Offset: 0x04A8			Register Name: HCSPC2PRT
Bit	Read/Write	Default/Hex	Description
31:28	R	0x0	PSIC Protocol Speed ID Count This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains.
27:16	R	0x000	PD Protocol Defined This field is reserved for protocol specific definitions.
15:8	R	0x01	CPCNT Compatible Port Count This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are '1' to MaxPorts.
7:0	R	0x02	CPOFF Compatible Port Offset This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

8.11.6 Global Register Description

8.11.6.1 0xC100 Global Soc Bus Configuration Register 0 (Default Value:0x0000_0001)

Offset: 0xC100			Register Name: GSBUSCFG0
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0	DatRdReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Data Read.

Offset: 0xC100			Register Name: GSBUSCFG0
Bit	Read/Write	Default/Hex	Description
			Input to BUS-GM.
27:24	R/W	0	DesRdReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Read. Input to BUS-GM.
23:20	R/W	0	DatWrReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Data Write. Input to BUS-GM.
19:16	R/W	0	DesWrReqInfo AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Write. Input to BUS-GM.
15:12	/	/	/
11	R/W	0	DatBigEnd Data Access is Big Endian This bit controls the endian mode for data accesses. 0: Little-endian (default) 1: Big-endian this bit must be set to zero.
10	R/W	0	DescBigend Descriptor Access is Big-Endian This bit controls the endian mode for descriptor accesses. 0: Little-endian (default) 1: Big-endian this bit must be set to zero.
9:8	/	/	/
7	R/W	0	INCR256BrstEna INCR256 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 256-beat burst.Input to BUS-GM.
6	R/W	0	INCR128BrstEna INCR128 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 128-beat burst.Input to BUS-GM.
5	R/W	0	INCR64BrstEna INCR64 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the

Offset: 0xC100			Register Name: GSBUSCFG0
Bit	Read/Write	Default/Hex	Description
			64-beat burst.Input to BUS-GM.
4	R/W	0	INCR32BrstEna INCR32 Burst Type Enable For the AHB/AXI configuration, if software set this bit to “1”, the AHB/AXI master uses INCR to do the 32-beat burst.Input to BUS-GM.
3	R/W	0	INCR16BrstEna INCR16 Burst Type Enable For the AHB/AXI configuration, if software set this bit to "1", the AHB/AXI master uses INCR to do the 16-beat burst.Input to BUS-GM.
2	R/W	0	INCR8BrstEna INCR8 Burst Type Enable For the AHB/AXI configuration, if software set this bit to "1", the AHB/AXI master uses INCR to do the 8-beat burst.Input to BUS-GM.
1	R/W	0	INCR4BrstEna INCR4 Burst Type Enable For the AXI configuration, when this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers. Input to BUS-GM.
0	R/W	1	INCRBrstEna Undefined Length INCR Burst Type Enable When enabled, this has higher priority than other burst types. For the AHB/AXI configuration. if this bit is set to “1”, AHB/AXI master tries to do only one INCR burst for each transfer unless it has to break it at a page boundary. If this bit is set to “0”, the AHB/AXI master may still use INCR burst type at the beginning and end bursts of transfers to align the address. The middle bursts are INCR4/8/16, depending when the type is enabled. Input to BUS-GM

8.11.6.2 0xC104 Global Soc Bus Configuration Register 1 (Default Value:0x0000_6F00)

Offset: 0xC104			Register Name: GSBUSCFG1
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16:13	R/W	0x3	ExtdPipeTransLimit AXI Pipelined Transfers Extended Burst Request Limit The {ExtdPipeTransLimit, PipeTransLimit} fields controls the number of outstanding extended pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 'h0: 1 request 'h1: 2 requests 'h2: 3 requests 'h3: 4 requests and, so on
12	R/W	0	EN1KPAGE 1k Page Boundary Enable By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
11:8	R/W	0xf	PipeTransLimit AXI Burst Request Limit The {ExtdPipeTransLimit, PipeTransLimit} fields controls the number of outstanding extended pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 'h0: 1 request 'h1: 2 requests 'h2: 3 requests 'h3: 4 requests

Offset: 0xC104			Register Name: GSBUSCFG1
Bit	Read/Write	Default/Hex	Description
			and, so on
7:0	/	/	/

8.11.6.3 0xC108 Global TX Threshold Control Register (Default Value:0x00F0_0000)

Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	UsbTxPktCntSel USB Async ESS Transmit Packet Threshold Enable - Host/Device Modes This field enables/disables the USB transmission multi-packet thresholding for Async endpoints: 0: USB transmission multi-packet thresholding is disabled; the controller starts transmission on the USB as soon as one packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The controller can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is valid in both host and device mode. It is only used for Enhanced SuperSpeed. In device mode, the controller can send ERDY on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO of a Bulk IN endpoint
25:21	R/W	0x7	USBTxPktCnt USB Async ESS Transmit Packet Threshold Count - Host/Device Modes This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction (burst) for Async endpoints. This field is only valid when the USB Async ESS Transmit Packet Threshold Enable field is set to one. For device mode, this field specifies the number of packets that must be in the TXFIFO before the controller can start transmission of ERDY for the corresponding USB transaction (burst) of Bulk IN

Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
			endpoint. Valid values for this field is 1 to 16. Note: In host mode, this field must be less than or equal to the USB Maximum TX Burst Size field. In device mode, this field must be less than or equal to the USB endpoint maximum Burst Size amongst all endpoints.
20:16	R/W	0x10	USBMaxTxBurstSize USB Async ESS Maximum TX Burst Size - Host Mode Only When USBTxPktCntSel is 1, this field specifies the Maximum ESS Bulk OUT burst that the controller can execute. When the system bus is slower than the USB, TXFIFO can underrun during a long burst. You can program a smaller value to this field to limit the TX burst size that the controller can execute. It only applies to ESS Bulk OUT endpoints in the host mode. Valid values are from 1 to 16. Note: This field can only be set to 2, 4, 8 or 16.
15	R/W	0x0	UsbTxThrNumPktSel_HS_Prd USB HS High Bandwidth Periodic Transmit Packet Threshold Enable - Host Mode Only This field enables/disables the USB HS High Bandwidth Periodic transmission multi-packet thresholding> 0: USB HS High Bandwidth Periodic transmission multi-packet thresholding is disabled; the controller can start transmission on the USB as soon as one packet has been fetched into the corresponding TXFIFO. 1: USB HS High Bandwidth Periodic transmission multi-packet thresholding is enabled. The controller can start transmission on the USB only after USB HS High Bandwidth Periodic Transmit Packet Threshold Count number of packets for the Periodic High Bandwidth USB transaction is already in the corresponding TXFIFO. This mode is valid in host mode for high speed high bandwidth periodic

Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
			endpoints
14:13	R/W	0x0	UsbTxThrNumPkt_HS_Prd USB HS High Bandwidth Periodic Transmit Packet Threshold Count - Host Mode Only This field specifies the number of packets that must be available in the TXFIFO before the controller can start transmission for the Periodic High Bandwidth USB transaction. This field is only valid when the USB HS High Bandwidth Periodic Transmit Packet Threshold Enable field is set to one. Valid values are from 1 to 3.
12:11	/	/	/
10	R/W	0x0	UsbTxThrNumPktSel_Prd USB Periodic ESS Transmit Packet Threshold Enable - Host Mode Only This field enables/disables the USB Periodic transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled; the controller starts transmission on the USB as soon as one packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The controller can start transmission on the USB only after USB Periodic ESS Transmit Packet Threshold Count amount of packets for the USB transaction (burst) has been fetched into the corresponding TXFIFO. It is used only for ESS.
9:5	R/W	0x0	UsbTxThrNumPkt_Prd USB Periodic ESS Transmit Packet Threshold Count - Host Mode Only This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction (burst). This field is valid only when the USB Periodic ESS Transmit Packet Threshold Enable field (UsbTxThrNumPktSel_Prd) is set to one. Valid values are from 1 to 16. Note: This field must be less than or equal to the USB Maximum Periodic TX Burst Size field.
4:0	R/W	0x0	UsbMaxTxBurstSize_Prd

Offset: 0xC108			Register Name: GTXTHRCFG
Bit	Read/Write	Default/Hex	Description
			USB Maximum Periodic ESS TX Burst Size - Host Mode Only When UsbTxThrNumPktSel_Prd is 1, this field specifies the Maximum Periodic OUT burst the controller can execute. When the system bus is slower than the USB, TXFIFO can underrun during a long burst. Note: This field can only be set to 2, 4, 8 or 16.

8.11.6.4 0xC10C Global RX Threshold Control Register (Default Value:0x00F0_0000)

Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0	USBRxPktCntSel USB Async ESS Receive Packet Threshold Enable - Host/Device Modes This field enables/disables the USB reception multi-packet thresholding: 0: The controller can only start reception on the USB when the RXFIFO has space for at least one packet. 1: The controller can only start reception on the USB when the RXFIFO has space for at least USBRxPktCnt amount of packets. This mode is valid in both host and device mode. It is only used for Enhanced SuperSpeed. In device mode, Setting this bit to 1 also enables the functionality of reporting NUMP in the ACK/ERDY TP based on the RXFIFO space instead of reporting a fixed NUMP derived from DCFG.NUMP for Bulk OUT endpoints. If you are using external buffer control (EBC) feature, disable this mode by setting USBRxPktCntSel to 0.
25:21	R/W	0x7	UsbRxPktCnt USB Async ESS Receive Packet Threshold Count - Host/Device Modes In host mode, this field specifies the space (in terms of the number of packets) that must be available in the RXFIFO before the controller can start the corresponding USB RX transaction (burst). In device mode, this field specifies the space (in

Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
			terms of the number of packets) that must be available in the RXFIFO before the controller can send ERDY for a flow-controlled Bulk OUT endpoints. This field is valid only when the USB Async ESS Receive Packet Threshold Enable field is set to 1. The valid values for this field are from 1 to 16. Note: This field must be less than or equal to the USB Maximum Receive Burst Size field.
20:16	R/W	0x10	UsbMaxRxBurstSize USB Async ESS Maximum Receive Burst Size - Host/Device Modes In host mode, this field specifies the Maximum Bulk IN burst the DWC_usb31 controller can perform. When the system bus is slower than the USB, RXFIFO can overrun during a long burst. You can program a smaller value to this field to limit the RX burst size that the controller can perform. It only applies to ESS Bulk endpoints in the host mode. In device mode, this field specifies the NUMP value that is sent in ERDY for a Bulk OUT endpoint. The programmed value should not exceed the RxFIFO size. This field is valid only when USBRxPktCntSel is 1. The valid values for this field are from 1 to 16.
15	R/W	0	UsbRxThrNumPktSel_HS_Prd USB HS High Bandwidth Periodic Receive Packet Threshold Enable - Host Mode Only This field enables/disables the USB reception multi-packet thresholding: 0: USB HS High Bandwidth Periodic Receive multi-packet thresholding is disabled; The controller can start reception on the USB as soon as the RXFIFO has space for one packet. 1: USB HS High Bandwidth Periodic Receive multi-packet thresholding is enabled; the controller can only start reception on the USB when the RXFIFO has space for at least UsbRxThrNumPkt_HS_Prd amount of packets. This mode is valid in host mode for high speed high bandwidth periodic endpoints.

Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
			In device mode, this field specifies the NUMP value that will be sent in ERDY for an OUT endpoint. This field is valid only when USBRxPktCntSel is one. The valid values for this field are from 1 to 16.
14:13	R/W	0x0	UsbRxThrNumPkt_HS_Prd USB HS High Bandwidth Periodic Receive Packet Threshold Count - Host Mode Only This field specifies the maximum number of packet space needed in the RXFIFO before the controller can start a HS Periodic High Bandwidth USB transaction. This field is valid only when USBRxPktCntSel_HS_Prd is 1. The valid values for this field are from 1 to 3.
12:11	/	/	/
10	R/W	0x0	UsbRxThrNumPktSel_Prd USB Periodic ESS Receive Packet Threshold Enable - Host Mode Only. This field should be programmed to 0 in Device mode. This field enables/disables the Periodic ESS USB reception multi-packet thresholding: 0: USB Periodic ESS Receive multi-packet thresholding is disabled; the controller can start reception on the USB as soon as the RXFIFO has space for one packet. 1: USB Periodic ESS Receive multi-packet thresholding is enabled; the controller can only start reception on the USB when the RXFIFO has space for at least UsbRxThrNumPkt_Prd amount of packets. This mode is valid only in host mode. It is only used for ESS.
9:5	R/W	0x0	UsbRxThrNumPkt_Prd USB Periodic ESS Receive Packet Threshold Count - Host Mode Only. This field should be programmed to 0 in Device mode. This field specifies the minimum number of packet space needed in the RXFIFO before the controller can start a ESS periodic high-bandwidth USB transaction. This field is valid only when the USB Periodic ESS Receive Packet Threshold Enable field

Offset: 0xC10C			Register Name: GRXTHRCFG
Bit	Read/Write	Default/Hex	Description
			is set to 1. Valid values are from 1 to 16. Note: This field must be less than or equal to the USB Maximum Periodic RX Burst Size field.
4:0	R/W	0x0	UsbMaxRxBurstSize_Prd USB Maximum Periodic ESS RX Burst Size - Host Mode Only. This field should be programmed to 0 in Device mode. When UsbRxThrNumPktSel_Prd is 1, this field specifies the Maximum ESS Periodic IN burst the controller can execute. When the system bus is slower than the USB, RXFIFO can overrun during a long burst.

8.11.6.5 0xC110 Global Core Control Register (Default Value:0x30C1_2004)

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
31:19	R/W	0x618	PwrDnScale Power Down Scale The USB3 suspend_clk input replaces pipe3_rx_pclk as a clock source to a small part of the USB3 core that operates when the SS PHY is in its lowest power (P3) state, and therefore does not provide a clock. The Power Down Scale field specifies how many suspend_clk periods fit into a 16 kHz clock period. When performing the division, truncate the remainders instead of rounding up. For example, when using an 8-bit/16-bit/32-bit PHY and 25-MHz Suspend clock, Power Down Scale = 25000 kHz/16 kHz = 13'd1562. Note: Minimum Suspend clock frequency is 32 kHz Maximum Suspend clock frequency is 125 MHz The LTSSM uses Suspend clock for 12-ms and 100-ms timers during suspend mode. According to the USB 3.1 specification, the accuracy on these timers is 0% to +50%. 12 ms + 0-+50% accuracy = 18 ms (Range is 12 ms - 18 ms) 100 ms + 0-+50% accuracy = 150 ms (Range is 100 ms

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
			- 150 ms). The suspend clock accuracy requirement is: (12,000/62.5) * (GCTL[31:19]) * actual suspend_clk_period should be between 12,000 and 18,000 (100,0000/62.5) * (GCTL[31:19]) * actual suspend_clk_period should be between 100,000 and 150,000 For example, if your suspend_clk frequency varies from 7.5 MHz to 10.5MHz, then the value needs to programmed is: Power Down Scale = 10500/16 = 657 (rounded up; and fastest frequency used)
18	R/W	0x0	MASTERFILTBYPASS Master Filter Bypass When this bit is set to 1'b1, irrespective of the parameter USB3_EN_BUS_FILTERS chosen, all the filters in the usb3_filter module will be bypassed. The double synchronizers to mac_clk preceding the filters will also be bypassed. For enabling the filters, this bit should be 1'b0.
17	R/W	0x0	BYPSSETADDR Bypass SetAddress in Device Mode When BYPSSETADDR bit is set, the device core uses the value in DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, this feature can be used to avoid sending an actual SET ADDRESS control transfer on the USB to make the device core respond to a new address. Note: This bit must be set for simulation purposes only. In the real hardware, this bit must be set to 1'b0.
16	R/W	0x1	U2RSTECN If the super speed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode.
15:14	R/W	0x0	FRMSCLDWN This field scales down device view of a

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
			SOF/USOF/ITP duration. For SS/HS mode: Value of 2'h3 implements interval to be 15.625 us Value of 2'h2 implements interval to be 31.25 us Value of 2'h1 implements interval to be 62.5 us Value of 2'h0 implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	R/W	0x02	PrtCapDir Port Capability Direction • 2'b01: for Host configurations • 2'b10: for Device configurations • 2'b00, 2'b11: not support **Note: For static Host-only or Device-only applications, use DRD Host or DRD Device mode.**
11	R/W	0x0	CoreSoftReset Core Soft Reset 1'b0 - No soft reset 1'b1 - Soft reset to core Clears the interrupts and all the CSRs except the following registers: - GCTL - GUCTL - GSTS - GGPIO - GUID - GUSB2PHYCFGn registers - GUSB3PIPECTLn registers - DCFG - DCTL - DEVTEN - DSTS When you reset PHYs (using GUBS3PHYCFG or GUSB3PIPECTL registers), you must keep the core in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets.
10	/	/	/
9	R/W	0x0	U1U2TimerScale Disable U1/U2 timer Scaledown If set to '1' along with GCTL[5:4] (ScaleDown) = 2'bX1 disables the scale down of U1/U2 inactive timer

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
			values. This is for simulation mode only.
8	R/W	0x0	DebugAttach Debug Attach When this bit is set: • SS Link proceeds directly to the Polling link state (after RUN/STOP in the DCTL register is asserted) without checking remote termination. • Link LFPS polling timeout is infinite • Polling timeout during TS1 is infinite (in case link is waiting for TXEQ to finish).
7:6	R/W	0x0	RAMClkSel RAM Clock Select 2'b00: bus clock 2'b01: pipe clock 2'b10: In device mode, pipe/2 clock. 2'b11: In device mode, selects mac2_clk as ram_clk when 8-bit UTMI or ULPI is used. (Not supported in 16-bit UTMI mode) In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00. Note: In device mode, if you set RAMClkSel to 2'b11 (mac2_clk), the controller internally switches the ram_clk to bus_clk when the link state changes to Suspend (L2 or L3), and switches the ram_clk back to mac2_clk when the link state changes to resume or U2. In host mode, this register field setting should not be modified. A value of 2 can be chosen only if the pipe data width is 8 or 16 bits. In this case the when the ram_clk is switched to pipe_clk, it uses pipe_clk/2 instead of pipe_clk. If a value of 3 is chosen for RAMClkSel, then when ram_clk is switched to pipe_clk, then pipe_clk is used without any divider. In device mode, when RAMClkSel != 2'b00, the bus_clk_early frequency can be a minimum of 1 MHz. This is tested in simulation and also in hardware with Linux, Microsoft Windows 8, and MCCI Windows7 host drivers. Only control and non

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
			periodic transfers are supported when bus_clk is 1 MHz. For periodic applications, the bus_clk_early minimum frequency is higher depending on your application and SoC bus. Even though 1 MHz has been tested with standard host drivers, Synopsys recommends 5 MHz minimum for ASIC designs to provide a margin or at least have a backup option to increase the bus_clk frequency to 5 MHz if needed.
5:4	R/W	0x0	ScaleDown Scale-Down Mode When Scale-Down mode is enabled for simulation, the core uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include: - Speed enumeration - HNP/SRP - Host mode suspend and resume 2'b10: Enables scale-down of Device mode suspend and resume timing values only. 2'b11: Enables bit 0 and bit 1 scale-down timing values. SS Mode 2'b00: Disables all scale-downs. Actual timing values are used. 2'b01: Enables scaled down SS timing and repeat values including: - Number of TxEq training sequences reduce to 8 - LFPS polling burst time reduce to 100 nS - LFPS warm reset receive reduce to 30 uS. - Refer to the rtl_vip_scaledown_mapping.xls file under <workspace>/sim/SoC_sim directory for the complete list.

Offset: 0xC110			Register Name: GCTL
Bit	Read/Write	Default/Hex	Description
			2'b10: No TxEq training sequences are sent. Overrides Bit 4. 2'b11: Enables bit 0 and bit 1 scale-down timing values.
3	R/W	0x0	DisScramble Disable Scrambling Transmit request to Link Partner on next transition to Recovery or Polling.
2	R/W	0x1	U2EXIT_LFPS If this bit is, 0: the link treats 248ns LFPS as a valid U2 exit. 1: the link waits for 8μs of LFPS before it detects a valid U2 exit.
1	R	0x0	GblHibernationEn This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	R/W	0x0	DsblClkGtng Disable Clock Gating When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.

8.11.6.6 0xC114 Global Power Management Status Register (Default Value:0x0000_0000)

Offset: 0xC114			Register Name: GPMSTS
Bit	Read/Write	Default/Hex	Description
31:28	W	0x0	PortSel This field selects the port number
27:17	/	/	/
16:12	R	0	U3Wakeup This field gives the following USB 3.1 port wakeup conditions: Bit [12]: Overcurrent Detected Bit [13]: Resume Detected Bit [14]: Connect Detected Bit [15]: Disconnect Detected

Offset: 0xC114			Register Name: GPMSTS
Bit	Read/Write	Default/Hex	Description
			Bit [16]: Last Connection State
11:10	/	/	/
9:0	R	0x0	U2Wakeup This field indicates the following USB 2.0 port wakeup conditions: Bit [0]: Overcurrent Detected Bit [1]: Resume Detected Bit [2]: Connect Detected Bit [3]: Disconnect Detected Bit [4]: Last Connection State Bit [5]: ID Change Detected Bit [6]: SRP Request Detected Bit [7]: ULPI Interrupt Detected Bit [8]: USB Reset Detected Bit [9]: Resume Detected Changed

8.11.6.7 0xC118 Global Status Register (Default Value:0x7E80_0002)

Offset: 0xC118			Register Name: GSTS
Bit	Read/Write	Default/Hex	Description
31:20	R	0x7e8	CBELT Current BELT Value In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
19:8	/	/	/
7	R	0	Host_IP Host Interrupt Pending This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
6	R	0	Device_IP Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.
5	R/W1C	0	CSRTimeout CSR Timeout When this bit is 1'b1, it indicates that software performed a write or read to a core register that could not be completed within

Offset: 0xC118			Register Name: GSTS
Bit	Read/Write	Default/Hex	Description
			`DWC_USB3_CSR_ACCESS_TIMEOUT bus clock cycles (default: 65535).
4	R/W1C	0	BusErrAddrVld Bus Error Address Valid Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	/	/	/
1:0	R	0x02	CurMod Current Mode of Operation Indicates the current mode of operation: 2'b00: Device mode 2'b01: Host mode

8.11.6.8 0xC11C Global User Control Register 1 (Default Value: 0x0000_1988)

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DEV_DECOUPLE_L1L2_EVT Enable this bit if you want to use L1 (LPM) events separately and not combine it with L2 events when operating in USB 2.0 speeds. 0: L1 and L2 events (suspend and resume) are not separated. For both L1 and L2 events, common suspend and resume events are generated. 1: L1 and L2 events are separated when operating in USB 2.0 mode. For L1 and L2 events, separate suspend and resume events are generated.
30	R/W	0x0	DS_RXDET_MAX_TOUT_CTRL This bit is used to control the tRxDetectTimeoutDFP timer for the Enhanced SuperSpeed link. 0: 12ms is used as tRxDetectTimeoutDFP 1: 120ms is used as the tRxDetectTimeoutDFP This bit is used only in host mode. For more details, refer to the *USB 3.1 Specification*.
29	R/W	0x0	FILTER_SE0_FSLS_EOP 0: Single sampling (utmi/ulpi clock) of linestate is

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
			checked for SE0 detection. 1: Feature enabled; Two samplings of linestate are checked for SE0 detection This bit is applicable for FS/LS operation. If this feature is enabled, SE0 on the linestate is validated for two consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode (FS): If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the controller ignores single SE0 glitch on the linestate during transmit. Only two or more SE0 is considered as a valid EOP on FS port. Host mode (FS/LS): If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the controller ignores single SE0 glitch on the linestate during transmit. Only two or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if linestate has SE0 glitches during transmission. This bit is quasi-static, that is, it must not be changed during operation.
28	R/W	0x0	TX_IPGAP_LINECHECK_DIS 0: The linestate transitioning from J to idle for HS mode treated as end of current packet. 1: Feature enabled; For detecting the HS end of packet, a fixed delay is used instead of linestate transition. This bit is applicable for HS operation of U2MAC. If this feature is enabled, then the 2.0 MAC operating in HS ignores the UTMI/ULPI linestate during transmission of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the linestate during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
			for device LPM handshake, the controller ignores the linestate after TX and waits for a fixed number of clocks (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap (between token to token/data) is added by 40 bit times of TXENDDELAY, and linestate is ignored during this 40 bit times delay. Enable this bit if linestate does not reflect the expected line state (J) during transmission. This bit is quasi-static, that is, it must not be changed during operation.
27	R/W	0x0	DEV_TRB_OUT_SPR_IND 0: Feature disabled; OUT TRB status does not set the Short Packet received bit 1: Feature enabled; OUT TRB status indicates Short Packet This bit is applicable for device mode only (and ignored in host mode). This feature can be enabled if the device application (software/hardware) wants to know whether a short packet is received for an OUT in the TRB status itself, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the {trbstatus, RSVD, SPR, PCM1, bufsize} dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, that is, it must not be changed during device operatio
26:25	/	/	/
24	R/W	0x0	DEV_L1_EXIT_BY_HW 0: Disables device L1 hardware exit logic 1: Feature enabled This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wakeup signaling to resume after going

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
			into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This hardware remote wake feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote-wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests through L1. This bit is quasi-static, it must not be changed during device operation.
23:21	R/W	0x0	IP_GAP_ADD_ON This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC. It should be programmed to a non-zero value only in case where you need to increase the default inter packet delay calculations in the USB 2.0 MAC module ${ldsg}_u2mac.v The inter packet delay is increased by number of utmi/ulpi clock cycles of this field value.
20:15	/	/	/
14	R/W	0x0	HW_LPM_CAP_DISABLE Disable hardware LPM capability in the xHCI capability register. When set, it disables hardware LPM capability in xHCI capability register.
13	R/W	0x0	HW_LPM_HLE_DISABLE Disable hardware LPM function in all USB 2.0 ports. When set, it disables hardware LPM function in

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
			all USB 2.0 ports.
12	R	0x1	DisUSB2RefClkGtng Disable ref_clk gating for USB 2.0 PHY (DisUSB2RefClkGtng) If ref_clk gating is disabled, then the ref_clk input cannot be turned off to the USB 2.0 PHY and controller. This is independent of the GCTL[DisClkGtng] setting. 1'b0: ref_clk gating enabled for USB 2.0 PHY 1'b1: ref_clk gating disabled for USB 2.0 PHY
11	R	0x1	DisRefClkGtng Disable ref_clk gating (DisRefClkGtng If the ref_clk gating is disabled then input ref_clk cannot be turned off to SSPHY and controller. This is independent of GCTL[DisClkGtng] setting. 1'b0: ref_clk gating Enabled for SSPHY 1'b1: ref_clk gating Disabled for SSPHY
10	R/W	0x0	RESUME_OPMODE_HS_HOST This bit is used only in host mode, and is for 2.0 opmode behaviour in HS Resume. When this bit is set to '1', the utmi/ulpi opmode will be changed to "normal" along with HS terminations after EOR. This is to support certain legacy UTMI/ULPI PHYs. When this bit is set to '0', the utmi/ulpi opmode will be changed to "normal" 2us after HS terminations change after EOR.
9	/	/	/
8	R/W	0x1	L1_SUSP_THRLD_EN_FOR_HOST This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: The device accepted BESL/BESLD value is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1.

Offset: 0xC11C			Register Name: GUCTL1
Bit	Read/Write	Default/Hex	Description
			The controller asserts utmi_sleep_n on L1 when one of the following is true: The device accepted BESL/BESLD value is less than the value in L1_SUSP_THRLD_FOR_HOST field. The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.
7:4	R/W	0x8	L1_SUSP_THRLD_FOR_HOST This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit. Note: Program this register field based on the UTMI/ULPI wakeup time in L1 suspend/sleep. In addition, for PCIe-based implementation, consider the DBESLD register value also.
3	R/W	0x1	HC_ERRATA_ENABLE Host ELD Enable (HELDEn) When this bit is set to 1, it enables the Exit Latency Delta (ELD) support defined in the xHCI 1.1. This bit is used only in the host mode. This bit has to be set to 1 in Host mode.
2	R/W	0x0	HC_PARCHK_DISABLE Host Parameter Check Disable (HParChkDisable) When this bit is set to '0', the xHC checks that the input slot/EP context fields comply to the *xHCI Specification*. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating 'PARAMETER ERROR'. When the bit is set to '1', the xHC does not perform parameter checks and does not generate 'PARAMETER ERROR' completion code.
1	/	/	/
0	R/W	0x0	LOA_FILTER_EN If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables.

8.11.6.9 0xC120 Global ID Register (Default Value: 0x3331_3130)

Offset: 0xC120			Register Name: GID
Bit	Read/Write	Default/Hex	Description
31:0	R	0x33313130	ID

8.11.6.10 0xC124 Global General Purpose Input/Output Register (Default Value:0x0000_0000)

Offset: 0xC124			Register Name: GGPIO
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0	GPO General Purpose Output This field's value is driven out on the gp_o[15:0] core output port.
15:0	R	0	GPI General Purpose Input This field's read value reflects the gp_i[15:0] core input value.

8.11.6.11 0xC128 Global User ID Register (Default Value:0x1234_5678)

Offset: 0xC128			Register Name: GUID
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x12345678	UserID Application-programmable ID field.

8.11.6.12 0xC12C Global User Control Register (Default Value:0x0A41_6802)

Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
31:22	R/W	0x29	REFCLKPER This field indicates the period of ref_clk, in terms of nano seconds. The valid programmable values of this field are as follows: 'h19: 25ns (integer corresponding to the supported ref_clk frequencies of 39.7 MHz) 'h29: 41ns (integer corresponding to the supported ref_clk frequency of 24 MHz) 'h32: 50ns (integer corresponding to the supported ref_clk frequency of 20 MHz)

Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
			'h34: 52ns (integer corresponding to the supported ref_clk frequency of 19.2MHz) 'h3A: 58ns (integer corresponding to the supported ref_clk frequency of 17 MHz) 'h3E: 62ns (integer corresponding to the supported ref_clk frequency of 16 MHz) This field needs to be updated during power-on initialization.
21	R/W	0	NoExtrDl No Extra Delay Between SOF and the First Packet Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host should wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 1'b0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1'b1: Host doesn't wait after a SOF before it sends the first USB packet.
20	R/W	0x0	DMAIgnoreHCE
19	R/W	0x0	IgnoreHCETimeout
18	R/W	0x0	EN_EXTD_TBC_CAP When set, the Extended TBC Capability is reported in HCCPARAMS2 if the DWC_USB31_EXTD_TBC_CAP_EN parameter is enabled.
17	R/W	0	SprsCtrlTransEn Sparse Control Transaction Enable Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1’b1, the host controller schedules transactions for a Control transfer in different microframes/frames.
16	R/W	0	ResBwHSEPS Reserving 85% Bandwidth for HS Periodic EPs

Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
			1'b0: HC reserves 80% of the bandwidth for periodic EPs. 1'b1: HC relaxes the bandwidth to 85% to accommodate two high-speed high-bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two high-bandwidth ISOC devices (HD Webcams) are connected and each device requires 1024-bytes X 3 packets per micro-frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 paylod per micro-frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host mode operation only. This field is ignored for device mode.
15	/	/	/
14	R/W	0	USBHstInAutoRetryEn Host IN Immediate Retry When set, this field enables the Immediate Retry feature. For IN transfers (non-isochronous) that encounter data packets with CRC errors or internal overrun scenarios, the immediate retry feature causes the Host controller to reply to the device with a non-terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP != 0). If the Immediate Retry feature is disabled, the controller will respond with a terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP = 0). 1'b0: Immediate Retry Disabled 1'b1: Immediate Retry Enabled
13	/	/	/
12	R/W	0x0	ExtCapSuptEN External Extended Capability Support Enable When set, this field enables extended capabilities to be implemented outside the controller. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in "Debug Capability" returns 16. A read to the first DWORD of the last internal

Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
			extended capability (the "xHCI Supported Protocol Capability for USB 3.1" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer field. This indicates there are no more capabilities.
11	R/W	0	InsrtExtrFSBODl Insert Extra Delay Between FS Bulk OUT Transactions Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b0: Host doesn't insert extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 1'b1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. **Note: Setting this bit to one will reduce the Bulk OUT transfer performance for FS devices.**
10:0	R/W	0x2	DTOUT Device Timeout (DTOUT) This field is Host mode parameter which determines how long the host waits for response from Enhanced SuperSpeed Device before considering the transaction to be timeout. Each count indicates duration in terms of 125us. For example a value of 1 indicates timeout at

Offset: 0xC12C			Register Name: GUCTL
Bit	Read/Write	Default/Hex	Description
			the minimum of 125us and maximum of 250us. The maximum value that can be programmed is 200 which sets 25ms as timeout time (minimum is 25ms and maximum is 25.125ms).

8.11.6.13 0xC130 Global Bus Error Address Low Register (Default Value:0x0000_0000)

Offset: 0xC130			Register Name: GBUSERRADDLR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	BusAddrLo This register contains the lower 32 bits of the first bus address that encountered a bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core.

8.11.6.14 0xC134 Global Bus Error Address High Register (Default Value:0x0000_0000)

Offset: 0xC134			Register Name: GBUSERRADDHR
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	BusAddrHi This register contains the higher 32 bits of the first bus address that encountered a bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the core.

8.11.6.15 0xC138 Global Super Speed Port to Bus Instance Mapping Low Register (Default Value:0x0000_0000)

Offset: 0xC138			Register Name: GPRTBIMAPLO
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	BINum1 SS USB Instance Number for Port 1 Application-programmable ID field.

8.11.6.16 0xC13C Global Super Speed Port to Bus Instance Mapping High Register (Default Value:0x0000_0000)

Offset: 0xC13C	Register Name: GPRTBIMAPHI

Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.11.6.17 0xC160 Global Debug Queue/FIFO Space Available Register (Default Value: 0x0042_0000)

Offset: 0xC160			Register Name: GDBDFIFOSPACE
Bit	Read/Write	Default/Hex	Description
31:16	R	0x43	Space Available
15:9	/	/	/
8:0	R/W	0x0	FIFO_Queue_Select • "FIFO/Queue Select[8:5] indicates the FIFO/Queue Type • "FIFO/Queue Select[4:0] indicates the FIFO/Queue Number For example, 9'b0_0010_0001 refers to RxFIFO_1 and 9'b0_0101_1110 refers to TxReqQ_30. 9'b0_0001_1111 to 9'b0_0000_0000: TxFIFO_31 to TxFIFO_0 9'b0_0011_1111 to 9'b0_0010_0000: RxFIFO_31 to RxFIFO_0 9'b0_0101_1111 to 9'b0_0100_0000: TxReqQ_31 to TxReqQ_0 9'b0_0111_1111 to 9'b0_0110_0000: RxReqQ_31 to RxReqQ_0 9'b0_1001_1111 to 9'b0_1000_0000: RxInfoQ_31 to RxInfoQ_0 9'b0_1010_0000: DescFetchQ_0 (for backwards compatibility) 9'b0_1010_0001: EventQ_0 (for backwards compatibility) 9'b0_1010_0010: ProtocolStatusQ_0 9'b0_1101_1111 to 9'b0_1110_0000: DescFetchQ_31 to DescFetchQ_0 9'b0_1111_1111 to 9'b0_1110_0000: WriteBack/EventQ_31 to WriteBack/EventQ_0 9'b1_0000_0111 to 9'b1_0000_0000: AuxEventQ_7 to AuxEventQ_0 (if EN_SEPARATE_DESC_QUEUES=1

8.11.6.18 0xC164 Global BMU Control Register (Default Value:0x9CC2_0026)

Offset: 0xC164			Register Name: GBMUCTL
Bit	Read/Write	Default/Hex	Description

Offset: 0xC164			Register Name: GBMUCTL
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x9CC2	/
15:6	R	0x0	/
5	R/W	0x1	separate_psq_en When DWC_USB31_EN_SEPARATE_PSQ_PER_DIR is enabled Separate internal process queue and state machine per direction is enabled when the bit is set to ?1?, BMU will process the plr_msg_type[PSQ_DIR] bit and pushes the messages to separate PSQ based on direction including special handling of control endpoint messages. when the bit is set to ?0?, BMU will ignore the plr_msg_type[PSQ_DIR] bit for all message types and pushes the messages to single PSQ to retain the legacy mode of operation.
4:3	R	0x0	/
2	R/W	0x1	axi_storder_en When DWC_USB31_AXI_STRICT_ORDER_EN parameter is enabled, both descriptor and data RxDMAs should be configured to use non-posted commands. For a given BI, descriptor/event RxDMA won't be issued until the previous issued data RxDMA is completed on the bus
1	R/W	0x1	active_id_en Active Id enabled
0	R/W	0x0	/

8.11.6.19 0xC16C Global Debug BMU Register (Default Value:0x0000_0000)

Offset: 0xC16C			Register Name: GDBGBMU
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	BMU_BCU Debug information
7:4	R	0x0	BMU_DCU Debug information
3:0	R	0x0	BMU_CCU Debug information

8.11.6.20 0xC170 Global Debug LSP MUX Register (Default Value:0x003F_0000)

Offset: 0xC170			Register Name: GDBGLSPMUX
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Offset: 0xC170			Register Name: GDBGLSPMUX
Bit	Read/Write	Default/Hex	Description
23:16	R/W	0x3F	“logic_analyzer_trace” Port MUX Select Currently only bits[21:16] are used. For details on how the mux controls the debug traces, refer to “assign logic_analyzer_trace =“ code section in the usb31.v file. A value of 6’h3F drives “0”s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
15	/	/	/
14:0	R/W	0x0	LSP Select In host mode: [14:0] - Selects the LSP debug information presented in the GDBGLSP register. In device mode: [3:0] - Device Endpoint Select (EPSELECT) Selects the Endpoint debug information presented in the GDBGEPINFO registers in device mode [7:4] - Device LSP Select (DEVSELECT) Selects the LSP debug information presented in the GDBGLSP register [14:8] - Host LSP Select Selects the LSP debug information presented in the GDBGLSP register

8.11.6.21 0xC174 Global Debug LSP Register (Default Value:0x0000_0000)

Offset: 0xC174			Register Name: GDBGLSP
Bit	Read/Write	Default/Hex	Description
31：0	R	0	LSP Debug Information This register is for internal use only.

8.11.6.22 0xC178 Global Debug Endpoint Information Register 0 (Default Value:0x0000_0000)

Offset: 0xC178			Register Name: GDBEPINFO0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	Endpoint Debug Information, bits [31:0] This register is for internal use only.

8.11.6.23 0xC17C Global Debug Endpoint Information Register 1 (Default Value:0x0000_0000)

Offset: 0xC17C			Register Name: GDBGEPINFO1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	Endpoint Debug Information, bits [63:32] This register is for internal use only.

8.11.6.24 0xC180 Global High Speed Port to Bus Instance Mapping Low Register (Default Value:0x0000_0000)

Offset: 0xC180			Register Name: GPRTBIMAPLR_HS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0	BINum1 HS USB Instance Number for Port 1 Application-programmable ID field.

8.11.6.25 0xC184 Global High Speed Port to Bus Instance Mapping High Register (Default Value:0x0000_0000)

Offset: 0xC184			Register Name: GPRTBIMAPHR_HS
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.11.6.26 0xC188 Global Full Speed Port to Bus Instance Mapping Low Register (Default Value:0x0000_0000)

Offset: 0xC188			Register Name: GPRTBIMAPLR_FS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	BINum1 FS USB Instance Number for Port 1 Application-programmable ID field.

8.11.6.27 0xC18C Global Full Speed Port to Bus Instance Mapping High Register (Default Value:0x0000_0000)

Offset: 0xC18C			Register Name: GPRTBIMAPHR_FS
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.11.6.28 0xC190 Global Host Mode SoC Bandwidth Override Register (Default Value:0x0000_0000)

Offset: 0xC190			Register Name: GHMSOCBWOR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ovrd_port_soc_bw Overrides the SoC bandwidth port values When this field is set 1, the ovrd_soc_common_rd_wr_bus, ovrd_ soc_rd_uF_kB_bandwidth, and ovrd_ soc_wr_uF_kB_bandwidth register values are used instead common_soc_rd_wr, soc_rd_uF_kB_bandwidth, and soc_wr_uF_kB_bandwidth input ports
30	R/W	0x0	ovrd_common_soc_rd_wr Override value for the common_soc_rd_wr port 1'b0: Separate SoC Bus for Read and Write 1'b1: Common SoC Bus for Read and Write
29:15	R/W	0x0	ovrd_soc_wr_uF_kB_bandwidth SoC Bus Write Bandwidth in KiloBytes/Micro-Frame Override value for the soc_wr_uF_kB_bandwidth port
14:0	R/W	0x0	ovrd_soc_rd_uF_kB_bandwidth SoC Bus Read Bandwidth in KiloBytes/Micro-Frame Override value for the soc_rd_uF_kB_bandwidth port

8.11.6.29 0xC200 Global USB2 PHY Configuration Register (Default Value:0x0000_2400)

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHYSOFTRST UTMI PHY Soft Reset Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI because ULPI PHYs are reset via their FunctionControl.Reset register, and the core automatically writes to this register when the core is reset (vcc_reset_n, USBCMD.HCRST, DCTL.SoftReset, or GCTL.SoftReset)
30:26	/	/	/
25	R/W	0x0	OVRD_FSLS_DISC_TIME Overriding the FS/LS disconnect time to 32us. If this value is 0, the FS/LS disconnect time is set to

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
			2.5us as per the USB specification. If this value is non-0, then the disconnect detection time is set to 32us. Normally this value is set to 0. But if the 2.0 PHYs introduce noise on UTMI linestate and cause SE0 gliches longer than 2.5us, then a false disconnect condition may get triggered. To avoid interoperability issues with these PHYs, this bit can be set to 1
24:22	R/W	0x0	LSTRD LS Turnaround Time (LSTRDTIM) This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 0: 2 bit times 1: 2.5 bit times 2: 3 bit times 3: 3.5 bit times 4: 4 bit times 5: 4.5 bit times 6: 5 bit times 7: 5.5 bit times **Note:** **This field is applicable only in Host mode.** **For normal operation (to work with most LS devices), it is recommended to set the value of this field to 3'h0 (2 bit times).** The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay (~1 LS bit time) from the delay requirement of the device.
21:19	R/W	0x2	LSIPD LS Inter-Packet Time (LSIPD) This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows:

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
			0: 2 bit times 1: 2.5 bit times 2: 3 bit times 3: 3.5 bit times 4: 4 bit times 5: 4.5 bit times 6: 5 bit times 7: 5.5 bit times **Note:** **This field is applicable only in Host mode.** **For normal operation (to work with most LS devices), it is recommended to set this field to 3'h2 (3 bit times).** The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay (~1 LS bit time) from the delay requirement of the device.
18	R/W	0x0	ULPIExtVbusIndicator ULPI External VBUS Indicator Indicates the ULPI PHY VBUS over-current indicator. • 1’b0: PHY uses an internal VBUS valid comparator. • 1’b1: PHY uses an external VBUS valid comparator.
17	R/W	0x0	ULPIExtVbusDrv ULPI External VBUS Drive Selects supply source to drive 5V on VBUS, in the ULPI PHY. • 1’b0: PHY drives VBUS with internal charge pump (default). • 1’b1: PHY drives VBUS with an external supply.
16	/	/	/
15	R/W	0x0	ULPIAutoRes ULPI Auto Resume Sets the AutoResume bit in Interface Control register on the ULPI PHY.

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
			• 1'b0: PHY does not use the AutoResume feature. • 1'b1: PHY uses the AutoResume feature.
14	/	/	/
13:10	R/W	0x09	USBTrdTim USB 2.0 Turnaround Time Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). These following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: • 4'h5: When the MAC interface is 16-bit UTMI+. • 4'h9: When the MAC interface is 8-bit UTMI+. If SoC bus does not require 60 MHz and USB turnaround time is not critical, this field can be set to a larger value.
9	R/W	0x0	XCVRDLY Transceiver Delay: Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 1 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. Note: If you enable the hibernation feature when the device controller comes out of power-off, you must re-initialize this bit with the appropriate value because the controller does not save and restore this bit value during hibernation. This bit is valid only in device mode.
8	R/W	0x0	EnblSlpM Enable utmi_sleep_n and utmi_l1_suspend_n The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
			L1 state. 1'b0: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n and utmi_l1_suspend_n assertion from the core is transferred to the external PHY. **Note: In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.**
7	R/W	0x0	PHYSel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select The application uses this bit to select a high-speed PHY or a full-speed transceiver. • 1'b0: USB 2.0 high-speed UTMI+ or ULPI PHY This bit is always 0, with Write Only access. • 1'b1: USB 1.1 full-speed serial transceiver This bit is always 1, with Write Only access. If both interface types are selected in global (parameters values are not zero), the application uses this bit to select the active interface is active, with Read-Write bit access. Note: USB 1.1 full-serial transceiver is not supported. This bit always reads as 1'b0.
6	R/W	0x0	SusPHY Suspend USB2.0 HS/FS/LS PHY When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. For DRD/OTG configurations, it is recommended that this bit is set to '0' during coreConsultant configuration. If it is set to '1', then the application should clear this bit after power-on reset. Application needs to set it to '1' after the core initialization is completed. For all other configurations, this bit can be set to '1' during core configuration.

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
			Note: In host mode, on reset, this bit is set to '1'. Software can override this bit after reset.
5	R/W	0x0	FSIntf Full-Speed Serial Interface Select The application uses this bit to select a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. • 1'b0: 6-pin unidirectional full-speed serial interface This bit is set to 0 with Read Only access. • 1'b1: 3-pin bidirectional full-speed serial interface This bit is set to 0 with Read Only access. Note: USB 1.1 full-speed serial interface is not supported. This bit always reads as 1'b0.
4	R/W	0x0	ULPI_UTMI_Sel ULPI or UTMI+ Select The application uses this bit to select a UTMI+ or ULPI Interface. • 1'b0: UTMI+ Interface • 1'b1: ULPI Interface
3	R/W	0x0	PHYIf PHY Interface If UTMI+ is selected, the application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. • 1'b0: 8 bits • 1'b1: 16 bits If ULPI is selected , this bit is reserved to '0'. Note: All the enabled 2.0 ports should have the same clock frequency as Port0 clock frequency (utmi_clk[0]). The UTMI 8-bit and 16-bit modes cannot be used together for different ports at the same time (that is, all the ports should be in 8-bit mode, or all of them should be in 16-bit mode, at a time). If any of the USB 2.0 ports is selected as ULPI port for operation, then all the USB 2.0 ports should be operating at 60 MHz.
2:0	R/W	0x0	TOutCal HS/FS Timeout Calibration The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time

Offset: 0xC200			Register Name: GUSB2PHYCFGn
Bit	Read/Write	Default/Hex	Description
			factor. This factor is added to the high-speed/full-speed interpacket timeout duration in the core to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the linestate condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: • One 30-MHz PHY clock = 16 bit times • One 60-MHz PHY clock = 8 bit times Full-speed operation: • One 30-MHz PHY clock = 0.4 bit times • One 60-MHz PHY clock = 0.2 bit times • One 48-MHz PHY clock = 0.25 bit times

8.11.6.30 0xC2C0 Global USB3 PIPE Control Register (Default Value:0x010C_0002)

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PHYSoftRst PHY soft-reset; to issue PHY reset, software should set this bit and reset this bit after meeting PHY reset timing.
30	R/W	0x0	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.1 cable. This bit enables placing the SS port link into a compliance state. By default, this bit should be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows:

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
			Disconnect any plugged in devices. Perform USBCMD.HCRST or power-on-chip reset. Set PORTSC.PP=0. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence (toggle the set GUSB3PIPECTL. HstPrtCmpl): Set GUSB3PIPECTL.HstPrtCmpl=0. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset.
29	R/W	0x0	U2P3ok Enable P3 entry during U2/SSInactive (U2P3ok). This is not recommended with Synopsys PHY which has P3 exit time of ~1ms and P2 exit time of ~100uS. This is recommended only if your PHYs P3 exit time is close to P2 exit time. Putting the ESS PHY in P3 during U2 would affect ESS Asynchronous endpoint performance and also this could prevent U2 entry if there are ESS periodic endpoints and their BInterval is in the sub milli-second range. rammer's Guide for more details. 0: During link state U2/ESS.Inactive, put PHY in P2 (Default) 1: During link state U2/ESS.Inactive, put PHY in P3 (Not recommended for Synopsys PHY). Note: For a port, if GUSB3PIPECTL[7]=1 and GUSB3PIPECTL[29]=1, set GUSB3PIPECTL[11] to 1
28	R/W	0x0	DisRxDetP3 Disabled receiver detection in P3 0: If PHY is in P3 and Core needs to perform receiver detection, Core will perform receiver detection in P3 1: If PHY is in P3 and Core needs to perform receiver detection, Core will change PHY power state to P2 and then perform receiver detection. After receiver detection, Core will change PHY power state to P3.
27	R/W	0x0	Ux_exit_in_Px Ux Exit in Px 0: The core does U1/U2/U3 exit in PHY power state

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
			P0 (default behavior) 1: The core does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively This bit is added for SS PHY workaround where SS PHY injects a glitch on pipe3_RxElecIdle while receiving Ux exit LFPS, and pipe3_PowerDown change is in progress. Note: This bit is used by third-party SS PHY, else it should be set to '0'.
26	R/W	0x0	ping_enhancement_en Ping Enhancement Enable When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for Downstream port only. Note: This bit is used by third-party SS PHY, else it should be set to '0'.
25	R/W	0x0	u1u2exitfail_to_recov U1U2exitfail to Recovery When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.
24	R/W	0x1	request_p1p2p3 Always Request P1/P2/P3 for U1/U2/U3 When set, the core always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the core does not request P1/P2/P3 power state change. Note: For third-party SS PHY, check with your PHY vendor, else this bit should be set to '1'.
23	R/W	0x0	StartRxdetU3RxDet Start Receiver Detection in U3/Rx.Detect If USB3_GUSB3PIPECTL_INIT[22] is set, and the link is in either U3 or Rx.Detect state, the core starts receiver detection on the rising edge of this bit. This

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
			can only be used for Downstream ports. This bit must be set to “0” for Upstream ports. This feature must not be enabled for normal operation.
22	R/W	0x0	DisRxDetU3RxDet Disable Receiver Detection in U3/Rx.Det When set, the core does not handle receiver detection in either U3 or Rx.Detect states. USB3_GUSB3PIPECTL_INIT[23] should be used to start receiver detection manually. This bit can only be used for Downstream port. This bit must be set to “0” for Upstream ports. This feature must not be enabled for normal operation.
21:19	R/W	0x0	Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (DWC_USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0. DWC_USB3_GUSB3PIPECTL_INIT[18] must be 1 to enable this functionality.
18	R/W	0x0	DELAYP1TRANS Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively • 1’b1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIlde is 1 and pipe3_RxValid is 0 • 1’b0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIlde and pipe3_RxValid. Note: This bit should be set to '1' for self PHY. It is also used by third-party SS PHY.
17	R/W	0x1	Suspend USB3.1 SS PHY When set, and if Suspend conditions are valid, the USB 3.1 PHY enters Suspend mode. For DRD/OTG configurations, it is recommended that this bit is set to ‘0’ during coreConsultant configuration. If it is set to ’1’, then the application should clear this bit after power-on reset. Application needs to set it to ’1’ after the core

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
			initialization is completed. For all other configurations, this bit can be set to '1' during core configuration.
16:15	R	0x0	DatWidth PIPE Data Width • 2'b00: 32 bits • 2'b01: 16 bits • 2'b10: 8 bits One clock after reset, these bits receive the value seen on the "pipe3_DataBusWidth".The simulation testbench uses the coreConsultant parameter to configure the VIP. These bits in the coreConsultant parameter should match your PHY data width and the "pipe_DataBusWidth" port.
14	R/W	0x0	AbortRxDetInU2 Abort Rx Detect in U2 When set, and the link state is U2, then the core will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for Downstream port only. **Note: This bit is used by third-party SS PHY. It should be set to '0' for self PHY.**
13	R/W	0x0	SkipRxDet Skip Rx Detect When set, the core skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
12	R/W	0x0	LFPSP0Algn LFPS P0 Align When this bit is set, LFPS during U1/U2/U3 exit is extended until data is ready at the PIPE to ensure the 20-ns gap between LFPS and SS/SSP.
11	R/W	0x0	P3P2TranOK P3 P2 Transitions OK When set, the core transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 specification. According to PIPE3 Specification, any direct

Offset: 0xC2C0			Register Name: GUSB3PIPECTLn
Bit	Read/Write	Default/Hex	Description
			transition between P3 and P2 is illegal. This bit is used only for some non-Synopsys PHYs that cannot do LFPS in P3. Note: This bit is used by third-party SS PHY. It should be set to '0' for self PHY.
10	R/W	0x0	P3ExSigP2 P3 Exit Signal in P2 (P3ExSigP2) When this bit is set, the controller always changes the PHY power state to P2, before attempting a U3 exit handshake.
9	R/W	0x0	LFPSFilt LFPS Filter When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.
8	R/W	0x0	RX_DETECT to Polling.LFPS Control 1'b0 (Default): Enables a 400µs delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1'b1: Disables the 400µs delay to start Polling LFPS after RX_DETECT.
7	/	/	/
6	R/W	0x0	TxSwing Tx Swing Refer to the PIPE specification.
5:3	R/W	0x0	TxMargin Tx Margin[2:0]
2:1	R/W	0x1	TxDeemphasis Tx Deemphasis The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode.
0	R/W	0x0	ElasticBufferMode Elastic Buffer Mode

8.11.6.31 0xC300+0x04*n Global Transmit FIFO Size Register n (Default Value: 0x0000_0043)

Offset: 0xC300+0x04*n (n=FIFO_number)			Register Name: GTXFIFOSIZ0
Bit	Read/Write	Default/Hex	Description

Offset: 0xC300+0x04*n (n=FIFO_number)			Register Name: GTXFIFOSIZ0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	TxFStAddr_n Transmit FIFOn RAM Start Address This field contains the memory start address for TxFIFOn.
15	/	/	/
14:0	R/W	0x43	TxFDep_n TxFIFOn Depth This value is in terms of depth*Tx RAM Data width. • Minimum value: 32 • Maximum value: 32,767

8.11.6.32 0xC380+0x04*n Global Receive FIFO Size Register n (Default Value: 0x0000_0413)

Offset: 0xC380+0x04*n (n=FIFO_number)			Register Name: GRXFIFOSIZ0
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	RxFStAddr_n RxFIFOn RAM Start Address This field contains the memory start address for RxFIFOn.
15	/	/	/
14:0	R/W	0x413	RxFDep_n RxFIFOn Depth This value is in terms of depth*Tx RAM Data width. • Minimum value: 32 • Maximum value: 16,384

8.11.6.33 0xC400+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Address Lower Register n (Default Value:0x0000_0000)

Offset: 0xC400+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTADLRn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EvntAdrLo Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

8.11.6.34 0xC404+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Address Higher Register n (Default Value:0x0000_0000)

Offset: 0xC404+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTADHRn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EvntAdrHi Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.

8.11.6.35 0xC408+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Size Register n (Default Value:0x0000_0000)

Offset: 0xC408+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTSIZn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EvntIntMask Event Interrupt Mask When set to '1', this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
30:16	/	/	/
15:0	R/W	0x0	EVNTSiz Event Buffer Size in bytes Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization.

8.11.6.36 0xC40C+0x10*n (0<= n <= EventBuff_number) Global Event Buffer Count Register n (Default Value:0x0000_0000)

Offset: 0xC40C+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTCOUNTn
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EVNT_HANDLER_BUSY Event Handler Busy Device software event handler busy indication. The controller sets this bit when the interrupt line is asserted due to pending events. Software clears this bit (with 1'b1) when it has finished processing the events (along with updating the EVNTCOUNT in this

Offset: 0xC40C+0x10*n (0<= n <= EventBuff_number)			Register Name: GEVNTCOUNTn
Bit	Read/Write	Default/Hex	Description
			register). The controller does not raise the interrupt line for a new event unless this bit is cleared. Note: When Interrupt moderation is disabled (that is, DEVICE_IMODI = 0), this bit is ignored.
30:16	/	/	/
15:0	R/W	0x0	EVNTCount Event Count When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. The interrupt line remains high when count is not 0.

8.11.6.37 0xC610 Global Device TX FIFO DMA Priority Register (Default Value:0x0000_0000)

Offset: 0xC610			Register Name: GTXFIFOPRIDEV
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0x0	gtxfifopridev Device TXFIFO priority This register specifies the relative DMA priority level among the Device TXFIFOs (one per IN endpoint). Each register bit[n] controls the priority (1: high, 0: low) of each TXFIFO[n]. When multiple TXFIFOs compete for DMA service at a given time (that is, multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. High-priority TXFIFOs are granted access using round-robin arbitration 2. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed. When configuring periodic IN endpoints, software must set register bit[n]=1, where n is the TXFIFO

Offset: 0xC610			Register Name: GTXFIFOPRIDEV
Bit	Read/Write	Default/Hex	Description
			assignment. This ensures that the DMA for isochronous or interrupt IN endpoints are prioritized over bulk or control IN endpoints. This register is present only when the controller is configured to operate in the device mode (includes DRD). The register size corresponds to the number of Device IN endpoints. Note Since the device mode uses only one RXFIFO, there is no Device RXFIFO DMA Priority Register.

8.11.6.38 0xC618 Global Host TX FIFO DMA Priority Register (Default Value:0x0000_0000)

Offset: 0xC618			Register Name: GTXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0x0	gtxfifoprihst Host TXFIFO priority This register specifies the relative DMA priority level among the Host TXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of TXFIFO[n] within a speed group. When multiple TXFIFOs compete for DMA service at a given time (i.e., multiple TXQs contain TX DMA requests and their corresponding TXFIFOs have space available), the TX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority TXFIFOs are granted access using round-robin arbitration b. Low-priority TXFIFOs are granted access using round-robin arbitration only after the high-priority TXFIFOs have no further processing to do (that is, either the TXQs are empty or the corresponding TXFIFOs are full). 2. The TX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants

Offset: 0xC618			Register Name: GTXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
			successive DMA requests to the same FIFO until the entire packet is completed. This register is present only when the controller is configured to operate in the host mode (includes DRD). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

8.11.6.39 0xC61C Global Host RX FIFO DMA Priority Register (Default Value:0x0000_0000)

Offset: 0xC61C			Register Name: GRXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
5:0	R/W	0x0	grxfifoprihst Host RXFIFO priority This register specifies the relative DMA priority level among the Host RXFIFOs (one per USB bus instance) within the associated speed group (SS or HS/FSLS). Each register bit[n] controls the priority (1: high, 0: low) of RXFIFO[n] within a speed group. When multiple RXFIFOs compete for DMA service at a given time (i.e., multiple RXQs contain RX DMA requests and their corresponding RXFIFOs have data available), the RX DMA arbiter grants access on a packet-basis in the following manner: 1. Among the FIFOs in the same speed group (SS or HS/FSLS): a. High-priority RXFIFOs are granted access using round-robin arbitration b. Low-priority RXFIFOs are granted access using round-robin arbitration only after high-priority RXFIFOs have no further processing to do (that is, either the RXQs are empty or the corresponding RXFIFOs do not have the required data). 2. The RX DMA arbiter prioritizes the SS speed group or HS/FSLS speed group according to the ratio programmed in the GDMAHLRATIO register. For scatter-gather packets, the arbiter grants successive DMA requests to the same FIFO until the entire packet is completed.

Offset: 0xC61C			Register Name: GRXFIFOPRIHST
Bit	Read/Write	Default/Hex	Description
			This register is present only when the controller is configured to operate in the host mode (includes DRD). The register size corresponds to the number of configured USB bus instances; for example, in the default configuration, there are 3 USB bus instances (1 SS, 1 HS, and 1 FSLS).

8.11.6.40 0xC624 Global Host FIFO DMA High-Low Priority Ratio Register (Default Value:0x0A0A_0101)

Offset: 0xC624			Register Name: GDMAHLRATIO
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0xa	hstrxfifo_mac RX MAC ESS Priority Count Specifies the Global Host FIFO MAC access Ratio Register's (GDMAHLRATIO) RX SS:HSFSLS Ratio power-on initialization value (bit[28:24]). This register specifies MAC write access count relation between ESS FIFOs vs HS+FSLS FIFOs. Specifically, FIFO access arbiter prioritizes the HS+FSLS FIFOs for one clock after the specified number of write access to the SS FIFOs.
23:21	/	/	/
20:16	R/W	0xa	hsttxfifo_mac TX MAC ESS Priority Count Specifies the Global Host FIFO MAC access Ratio Register's (GDMAHLRATIO) TX SS:HSFSLS Ratio power-on initialization value (bit[20:16]). This register specifies MAC read access count relation between ESS FIFOs vs HS+FSLS FIFOs. Specifically, FIFO read access arbiter prioritizes the HS+FSLS FIFOs for one clock after the specified number of read access to the SS FIFOs.
15:13	/	/	/
12:8	R/W	0x1	hstrxfifo_dma RX DMA ESS Priority Count Specifies the Global Host FIFO DMA access Ratio Register's (GDMAHLRATIO) RX SS:HSFSLS Ratio power-on initialization value (bit[12:8]). This register specifies the relative priority of the SS FIFOs vs. the HS+FSLS FIFOs. Specifically, the DMA

Offset: 0xC624			Register Name: GDMAHLRATIO
Bit	Read/Write	Default/Hex	Description
			arbiter prioritizes the HS/FSLS round-robin arbiter group for one packet after the specified number of packet grants to the ESS round-robin arbiter group. When a standard driver is used, such as the xHCI driver from Microsoft, this register must be initialized to meet system requirements before synthesizing the controller. If you are developing your own xHCI host driver, then this register can be configured by your driver. It is recommended to keep this value as 1 so that HS/FSLS gets same priority as ESS. The HS/FSLS bandwidth requirement is negligible compared to ESS, so keeping this value as 1 ensures USB 2.0 operation is not affected by high bandwidth ESS.
7:5	/	/	/
4:0	R/W	0x1	hsttxfifo_dma TX DMA ESS Priority Count Specifies the Global Host FIFO DMA access Ratio Register's (GDMAHLRATIO) TX SS:HSFSLS Ratio power-on initialization value (bit[4:0]). This register specifies the access weight of the SS FIFOs vs. the HS+FSLS FIFOs. Specifically, the DMA arbiter prioritizes the HS/FSLS round-robin arbiter group for one packet after the specified number of packet grants to the ESS round-robin arbiter group. When a standard driver is used, such as the xHCI driver from Microsoft, this register must be initialized to meet system requirements before synthesizing the controller. If you are developing your own xHCI host driver, then this register can be configured by your driver. It is recommended to keep this value as 1 so that HS/FSLS gets same priority as ESS. The HS/FSLS bandwidth requirement is negligible compared to ESS, so keeping this value as 1 ensures USB 2.0 operation is not affected by high bandwidth ESS.

8.11.7 Device Register Description

8.11.7.1 0xC700 Device Configuration Register (Default Value:0x0008_0805)

Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	ISPP Ignore Stream Packet Pending This bit only effect stream-capable bulk endpoints. When this bit is set to '0' and the controller receives a Data Packet with the Packet Pending (PP) bit set to '0' for OUT endpoints, or it receives an ACK with the NumP field set to '0' and PP set to '0' for IN endpoints, the core attempts to search for another stream (CStream) to initiate to the host. However, there are two situations where this behavior is not optimal: When the host is setting PP='0' even though it has not finished the stream, or When the endpoint on the device is configured with one transfer resource and therefore does not have any other streams to initiate to the host. When this bit is set to '1', the core ignores the Packet Pending bit for the purposes of stream selection and does not search for another stream when it receives DP(PP='0') or ACK(NumP='0', PP='0'). This can enhance the performance when the device system bus bandwidth is low or the host responds to the core's ERDY transmission very quickly.
22	R/W	0x0	LPMCAP LPM Capable The application uses this bit to control the USB Device LPM capabilities. If the core operates as a non-LPM-capable device, it cannot respond to LPM transactions. 0: LPM capability is not enabled. 1: LPM capability is enabled.
21:17	R/W	0x4	NUMP Number of Receive Buffer This bit indicates the number of receive buffers to be reported in the ACK TP. The usb3 controller uses this field if

Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
			GRXTHRCFG.USBRxPktCntSel is set to '0'. The application can program this value based on RxFIFO size, buffer sizes programmed in descriptors, and system latency. For an OUT endpoint, this field controls the number of receive buffers reported in the NumP field of the ACK TP transmitted by the controller.
16:12	R/W	0x0	INTRNUM Interrupt Number Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts are generated.
11:10	/	0x2	/
9:3	R/W	0x0	DEVADDR Device Address The application must perform the following: Program this field after every SetAddress control command. Reset this field to zero after USB reset.
2:0	R/W	0x5	DEVSPD Device Speed Indicates the speed at which the application requires the controller to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the controller is connected. 3'b101: Enhanced SuperSpeed (USB 3.1 PHY clock is 156.25 MHz or 312.5 MHz operating at 10Gbps) 3'b100: SuperSpeed (USB 3.1 PHY clock is 125 MHz or 250 MHz operating at 5Gbps) 3'b000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 3'b001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) Values: 0x5 (EnhancedSuperSpeed): Enhanced SuperSpeed (USB 3.1 PHY clock is 156.25 MHz or 312.5 MHz operating at 10Gbps) 0x4 (SuperSpeed): SuperSpeed (USB 3.1 PHY clock is

Offset: 0xC700			Register Name: DCFG
Bit	Read/Write	Default/Hex	Description
			125 MHz or 250 MHz operating at 5Gbps) 0x0 (HighSpeed): High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 0x1 (FullSpeed): Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz)

8.11.7.2 0xC704 Device Control Register (Default Value:0x0000_0000)

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RS Run/Stop Software writes 1 to this bit to start the device controller operation. To stop device controller operation, software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the STS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: After power-on reset and CSR initialization, software must write 1 to this bit to start the device controller. The controller will not signal connect to the host until this bit is set. Software uses this bit to control the device controller to perform a soft disconnect. When software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until software writes 1 to this bit. If software is attempting a connect after the soft disconnect, it should set DCTL[8:5] to 5 before reasserting the Run/Stop bit. When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller.

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
30	R/W	0x0	CSFTRST Core Soft Reset Resets the all clock domains as follows: This bit clears the interrupts and all the CSRs except GSTS, USB31_IP_NAME, GGPIO, GUID, GUSB2PHYCFGn registers, GUSB3PIPECTLn registers, DCFG, DCTL, DEVTEN, and DSTS registers. All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the core. This is a self-clearing bit; the core clears this bit after all necessary logic is reset in the core and all the PHY clocks are active/running after PHY reset, which may take several milliseconds depending on the PHY's clock latency. Software can have a poll rate of 1 ms or more to check if this bit has been cleared or not. Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation.
29	/	/	/
28:24	R/W	0x0	HIRDTH HIRD Threshold The core asserts output signals UTMI_L1_SUSPEND_n and UTMI_SLEEP_n on the basis of this signal: The core asserts UTMI_L1_SUSPEND_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: HIRD value is greater than or equal to the value in DCTL.HIRDTH[3:0]

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
			DCTL.HIRDTH[4] is set to '1' The core asserts UTMI_SLEEP_n on L1 when one of the following is true: If the HIRD value is less than HIRDTH[3:0] or HIRDTH[4] is set to '0'.
23:20	R/W	0xf	LPM_NYET_thres Bits [23:20]: LPM NYET Response Threshold (LPM_NYET_thres) Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The controller always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The controller responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). No data is pending in the TxFIFO and the RxFIFO is empty. The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0]
19	R/W	0x0	KeepConnect When '1', this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device core disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ('0'), or if the core should not disconnect when RunStop is set to 0 ('1'). This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2.
18	R/W	0x0	L1HibernationEn When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
			larger than the threshold programmed in DCTL.HIRD_Thres. The core will not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	W	0x0	CRS Controller Restore State This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'.
16	W	0x0	CSS Controller Save State This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'.
15:13	/	/	/
12	R/W	0x0	INITU2EN Initiate U2 Enable 0x0: May not initiate U2 0x1: May initiate U2 On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received. If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
11	R/W	0x0	ACCEPTU2EN Accept U2 Enable 0x0: Reject U2 except when Force_LinkPM_Accept bit is set 0x1: Core accepts transition to U2 state if nothing is pending on the application side. On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving a

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
			SetConfiguration command.
10	R/W	0x0	INITU1EN Initiate U1 Enable 0x0: May not initiate U1 0x1: May initiate U1 On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.
9	R/W	0x0	ACCEPTU1EN Accept U1 Enable 0x0: Reject U1 except when Force_LinkPM_Accept bit is set 0x1: Core accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving a SetConfiguration command.
8:5	R/W	0x0	ULSTCHGREQ USB/Link State Change Request Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Refer to the USB3 specification. Alternatively, you can force the local link directly into Compliance mode, by resetting the SS link with the RUN/STOP bit set to zero. If you then write “10” to the USB/Link State Change field and “1” to RUN/STOP, the Link will go to Compliance. Once you are in Compliance, you

Offset: 0xC704			Register Name: DCTL
Bit	Read/Write	Default/Hex	Description
			may alternately write “zero” and “10” to this field to advance the compliance pattern. In SS mode: Value Requested Link State Transition/Action 0 No Action 4 SS.Disabled 5 Rx.Detect 6 SS.Inactive 8 Recovery 10 Compliance Others Reserved In HS/FS/LS mode: Value Requested USB state transition 8 Remote wakeup request Others Reserved The Remote wakeup request should be issued 2μs after the device goes into suspend state (DSTS[21:18] is 3). Note: After coming out of hibernation, software should write 8 (Recovery) into this field to confirm exit from the suspended state
4:1	R/W	0x0	TSTCTL Test Control • 4’b000: Test mode disabled • 4’b001: Test_J mode • 4’b010: Test_K mode • 4’b011: Test_SE0_NAK mode • 4’b100: Test_Packet mode • 4’b101: Test_Force_Enable • Others: Reserved
0	/	/	/

8.11.7.3 0xC708 Device Event Enable Register (Default Value:0x0000_0000)

Offset: 0xC708			Register Name: DEVTEN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	LDMEVTEN LDM Response Event Enable. Enables interrupt when response to LDM request is received.

Offset: 0xC708			Register Name: DEVTEN
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	L1WKUPEVTEN L1 Resume Detected Event Enable.
13	/	/	/
12	R/W	0x0	VndrDevTstRcvEn Vendor Device Test LMP Received Event Enable
11:10	/	/	/
9	R/W	0x0	ErrticErrEn Erratic Error Event Enable
8	R/W	0x0	L1SUSPEN L1 Suspend Event Enable
7	R/W	0x0	SofEn Start of (micro-)Frame Enable For debug purpose only; normally software must disable this event.
6	R/W	0x0	U3L2L1SuspEn U3/L2-L1 Suspend Event Enable.
5	R/W	0x0	HibernationReqEvtEn This bit enables/disables the generation of the Hibernation Request Event.
4	R/W	0x0	WkUpEvtEn Resume/Remote Wakeup Detected Event Enable
3	R/W	0x0	ULStChgEn USB/Link State Change Event Enable
2	R/W	0x0	ConnectDoneEn Connect Done Enable
1	R/W	0x0	USBRstEn USB Reset Enable
0	R/W	0x0	DisconnEvtEn Disconnect Detected Event Enable

8.11.7.4 0xC70C Device Status Register (Default Value:0x0002_0004)

Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R	0x0	DCNRD Device Controller Not Ready The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it

Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
			takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when USB3_EN_PWROPT is set to 2 and GCTL[1].GblHibernationEn =1.
28	R/W1C	0x0	SRE Save/Restore Error This bit is currently not supported.
27:26	/	/	/
25	R	0x0	RSS Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the restore process, it will complete the command by setting DSTS.RSS to '0'.
24	R	0x0	SSS Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	R	0x0	CoreIdle Core Idle The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. **Note: While testing for Reset values, mask out the read value. This bit represents the changing state of the core and does not hold a static value.**
22	R	0x0	DevCtrlHlt Device Controller Halted This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to '0', the core is idle and the lower layer

Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
			finishes the disconnect process. When Halted =1, the core does not generate Device events.
21:18	R	0x0	USBLnkSt USB/Link State In SS mode: (LTSSM State) 0x0: U0 0x1: U1 0x2: U2 0x3: U3 0x4: SS_DIS 0x5: RX_DET 0x6: SS_INACT 0x7: POLL 0x8: RECOV 0x9: HRESET 0xA: CMPLY 0xB: LPBK 0xF: Resume/Reset In HS/FS/LS mode: 0x0: On state 0x2: Sleep state 0x3: Suspend state 0x4: Disconnected state (Default state) 0x5: Early Suspend state (valid only when Hibernation is disabled, GCTL [1]. GblHibernationEn =0) 0xE: Reset (valid only when Hibernation is disabled, GCTL [1]. GblHibernationEn =1) 0xF: Resume (valid only when Hibernation is disabled, GCTL [1]. GblHibernationEn=1) The Resume/Reset link state indicates that the core received a resume or USB reset request from the host while the link was in hibernation. Software must write '8' (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request. The Early Suspend link state is an early indication of device suspend in HS/FS. The link state changes to Early Suspend after detecting bus idle for 3ms.

Offset: 0xC70C			Register Name: DSTS
Bit	Read/Write	Default/Hex	Description
			In HS operation, this is an indication that the USB bus (that is, LineState) has been in idle (SE0) for 3ms. However, it does not confirm whether the next process is Suspend or Reset. The device checks the bus again after pull up enable delay and if the line state indicates Suspend (full speed J), then the device waits for additional time (~3ms) to indicate the actual Suspend state. In FS operation, this is an indication that the USB bus (that is, LineState) has been in idle (J) for 3ms. The device waits for additional time (~3ms of Idle) to indicate the actual Suspend state. When Hibernation is enabled, GCTL [1]. GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL [31].Run/Stop set to '1' and DSTS[29].DCNRD = 0.
17	R	0x1	RXFIFOEMP RxFIFO Empty
16:3	R	0x0000	SOFFN Frame/Micro-Frame Number of the Received SOF When the controller is operating at SuperSpeed/SuperSpeedPlus, [16:3] indicates the microframe/ITP number When the core is operating at high-speed, [16:6] indicates the frame number [5:3] indicates the microframe number When the core is operating at full- or low-speed, [16:14] is not used. Software can ignore these 3 bits [13:3] indicates the frame number
2:0	R	0x4	ConnectSpd Connected Speed Indicates the speed at which the core has come up after speed detection through a chirp sequence. 0x0: High-Speed (PHY clock is running at 30 or 60 MHz) 0x1: Full-Speed (PHY clock is running at 30 or 60 MHz) 0x4: Super-Speed (PHY clock is running at 125 or 250 MHz) Low-speed is not supported for device using a UTMI+ PHY

8.11.7.5 0xC710 Device Generic Command Parameter Register (Default Value:0x0000_0000)

Offset: 0xC710			Register Name: DGCMDPAR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	PAR Parameter [31:0] This register indicates the device command parameter. This must be programmed before or along with the device command.

8.11.7.6 0xC714 Device Generic Command Register (Default Value:0x0000_0000)

Offset: 0xC714			Register Name: DGCMD
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R	0x0	CMDSTS Command Status 1: CmdErr: Indicates that the device controller encountered an error while processing the command. 0: Indicates command success.
11	/	/	/
10	R/W	0x0	CMDACT Command Active The software sets this bit to '1' to enable the device controller to excute the generic command. The device controller clears this bit to '0' after executing the command.
9	/	/	/
8	R/W	0x0	CMDIOC Command Interrupt on Complete When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum.
7:0	R/W	0x00	CMDTYP Command Type Specifies the type of command the software driver is requesting the core to perfrom. 02h: Set Periodic Parameters 04h: Set Scratchpad Buffer Array Address Lo 05h: Set Scratchpad Buffer Array Address Hi 07h: Transmit Device Notification

Offset: 0xC714			Register Name: DGCMD
Bit	Read/Write	Default/Hex	Description
			09h: Selected FIFO Flush 0Ah: All FIFO Flush 0Ch: Set Endpoint NRDY 11h: Restart After Disconnect All other values are reserved.

8.11.7.7 0xC718 Device Control Register 1 (Default Value:0x0000_0000)

Offset: 0xC718			Register Name: DCTL1
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	EN_ENDXFER_ON_RJCT_STRM Enable bit for new reject stream flow. On receiving a reject stream(FFFF) on USB side, Controller updates the application SW with STREAMEVT_NOTFOUND with streamid as FFFF, On decoding this event application SW needs to apply an ENDXFER command which flushes all FIFO's . Until an ENDXFER is issued, Any stream packet received(on USB) will not lead to search of available streams in cache and release of ERDY.Controller writes STREAM_NOT_FOUND events until ENDXFER completion. 0: Feature disabled. No Reject status is updated to application SW. 1: Feature enabled, Reject staus is updated on receiving a reject stream(on USB).Decoding this event application SW needs to apply an ENDXFER.
1	R/W	0x0	DIS_CLRSPR_SXFER Disable bit to clear intrenal SPR bit during start transfer. If an End Transfer Command is issued during a transfer, there is a possibility that the internal SPR (short packet received/retry received) gets set, but not cleared. The SPR clearing is now done when the new Start Transfer command is issued. Using this register bit, you can disable the clearing of the SPR bit during a Start Transfer command. 0: The SPR bit is cleared when a Start Transfer command is issued (default value).

Offset: 0xC718			Register Name: DCTL1
Bit	Read/Write	Default/Hex	Description
			1: The SPR bit is not cleared when a Start Transfer command is issued.
0	/	/	/

8.11.7.8 0xC720 Device Active USB Endpoint Enable Register (Default Value:0x0000_0000)

Offset: 0xC720			Register Name: DALEPENA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	USBACTEP USB Active Endpoints This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0–15 and OUT endpoints 0– 15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN ... The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Application software clears these bits for all endpoints (other than EP0- OUT and EP0-IN) after detecting a USB reset. After receiving SetConfiguration and SetInterface request, the application must program endpoint registers accordingly and set these bits.

8.11.7.9 0xC724 Device LDM Request Control Register (Default Value:0x0000_0000)

Offset: 0xC724			Register Name:DLDMENA
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	LDMADJ LDM request interval duration This field indicates Link Delay adjustment in terms of nano-seconds

Offset: 0xC724			Register Name:DLDMENA
Bit	Read/Write	Default/Hex	Description
			After receiving Link Delay through LDM events the application must set these bits with average value. After receiving ClearFeature(LDM_ENABLE) the application must program and reset these bits.
15:8	R/W	0x0	LDMDUR LDM request interval duration This field indicates gap between two LDM request in terms of microframes After receiving SetFeature(LDM_ENABLE) the application must set these bits. After receiving ClearFeature(LDM_ENABLE) the application must program and reset these bits.
7:4	R/W	0x0	NOLOWPWRDUR No Low Power Duration After starting a transfer on an ESS ISOC endpoint, the application must program these bits. Each count represents the duration in terms of 8 ms. For example, a value of 3 represents 24 ms.
3:1	R/W	0x0	LDMRQS LDM number of requests This field indicates how many LDM requests Controller sends. A value of zero indicates request to send forever After receiving SetFeature(LDM_ENABLE) the application must set these bits. After receiving ClearFeature(LDM_ENABLE) the application must program and reset these bits
0	R/W	0x0	LDMENA LDM enabled This field indicates PTM protocol LDM request is enabled After receiving SetFeature(LDM_ENABLE) the application must set this bit. After receiving ClearFeature(LDM_ENABLE) the application must program and reset this bit. After receiving 4 consecutive timeout response to LDM, Hardware resets this bit.

8.11.7.10 0xC800 + 0x10*n (n=0-9) Device Physical Endpoint-n Command Parameter 2 Register (Default Value:0x0000_0000)

Offset: 0xC800 + 0x10*n (n=0-9)			Register Name: DEPCMDPAR2_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	PAR2 Parameter 2 This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

8.11.7.11 0xC804 + 0x10*n (n=0-9) Device Physical Endpoint-n Command Parameter 1 Register (Default Value:0x0000_0000)

Offset: 0xC804 + 0x10*n (n=0-9)			Register Name: DEPCMDPAR1_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	PAR1 Parameter 1 This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command.

8.11.7.12 0xC808 + 0x10*n (n=0-9) Device Physical Endpoint-n Command Parameter 0 Register (Default Value:0x0000_0000)

Offset: 0xC808 + 0x10*n (n=0-9)			Register Name: DEPCMDPAR0_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x00000000	PAR0 Parameter 0 This register indicates the physical endpoint command Parameter 0. This must be programmed before or along with the command. For commands needing only one 32-bit parameter, it must be programmed before issuing the command.

8.11.7.13 0xC80C + 0x10*n (n=0-9) Device Physical Endpoint-n Command Register (Default Value:0x0000_0000)

Offset: 0xC80C + 0x10*n (n=0-9)	Register Name: DEPCMD_n (n=0-31)

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	CMDPAR (W) Command Parameters, when this register is written: For Start Transfer command: [31:16]: Stream ID. The USB Stream ID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: [31:16]: Start Micro-Frame Number, indicates the (micro-)frame number to which the first TRB applies For Update Transfer, End Transfer, and Start New Configuration commands: [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command. EVTPAR (R) Event Parameters, when this register is read: For XferNotReady, XferComplete, and Stream events on Bulk Endpoints: [31:16]: StreamID. Applies only to bulk endpoints that support streams. This indicates the Stream ID of the transfer for which the event is generated For XferInProgress: [31:16]: Isochronous Microframe Number (IsocMicroFrameNum): Indicates the microframe number of the beginning of the interval that generated the XferInProgress event (debug purposes only) For XferNotReady events on Isochronous Endpoints: [31:16]: Isochronous Microframe Number (IsocMicroFrameNum). Indicates the microframe number during which the endpoint was not ready EPCmdCmplt events For all EPCmdCmplt events [27:24]: Command Type. The command type that completed (Valid only in a DEPEVT event. Undefined when read from the DEPCMD.EventParam field). For EPCmdCmplt events in response to Get Data Sequence command: [20:16]: Current Data Sequence Number (CurDatSeqNum). The endpoint's current data sequence number is returned in this field. For EPCmdCmplt event in response to Start Transfer command: [22:16]: Transfer Resource Index (XferRscIdx). The internal

Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
			hardware transfer resource index assigned to this transfer. This index must be used in all Update Transfer and End Transfer commands.
15:12	R/W	0x0	CMDSTS Command Completion Status Additional information about the completion of this command is available in this field. Within an XferNotReady event: • [15]: Indicates the reason why the XferNotReady event is generated: - 1'b0: XferNotActive: Host initiated a transfer, but the requested transfer is not present in the hardware - 1'b1: XferActive: Host initiated a transfer, the transfer is present, but no valid TRBs are available • [14]: Not Used • [13:12]: For control endpoints, indicates what stage was requested when the transfer was not ready: - 2'b00: SETUP Request - 2'b01: Control Data Request - 2'b10: Control Status Request Within an XferComplete or XferInProgress event: • [15]: LST bit of the completed TRB (XferComplete only) • [15]: MissedIsoc: Indicates the interval did not complete successfully (XferInProgress only) • [14]: IOC bit of the TRB that completed • [13]: Indicates the TRB completed with a short packet reception or the last packet of an isochronous interval • [12]: Indicates a Bus Error occurred If the host aborted the data stage or an isochronous time passed condition occurred, the EventStatus bits may all be '0', with the reason for the transfer completion reflected in the TRB Status field. Within a Stream Event: • [15:12]: - 4'h2: StreamNotFound: This stream event is issued when the stream-capable endpoint performed a search in its transfer resource cache, but could not find an active and ready stream. - 4'h1: StreamFound: This stream event is issued when the

Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
			stream-capable endpoint found an active and ready stream in its transfer resource cache, and initiated traffic for that stream to the host. The ID of the selected Stream is in the EventParam field. In response to a Start Transfer command: • [15:12]: - 4'h2: Indicates expiry of the bus time reflected in the Start Transfer command. - 4'h1: Indicates there is no transfer resource available on the endpoint. In response to a Set Transfer Resource (DEPXFERCFG) command: • [15:12]: - 4'h1: Indicates an error has occurred because software is requesting more transfer resources to be assigned than have been configured in the hardware.
11	R/W	0x0	ForceRM ForceRM: Only valid for End Transfer command ClearPendIN: Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued. Only valid for Clear Stall command Only applicable for SS and ESS mode of operation
10	R/W	0x0	CMDACT Command Active Software sets this bit to '1' to enable the device endpoint controller to execute the generic command. The device controller clears this bit to '0' when the CMDSTS field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	/	/	/
8	R/W	0x0	CMDIOC Command Interrupt on Complete When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command.

Offset: 0xC80C + 0x10*n (n=0-9)			Register Name: DEPCMD_n (n=0-31)
Bit	Read/Write	Default/Hex	Description
7:4	/	/	/
3:0	R/W	0x0	CMDTYP Command Type Specifies the type of command the software driver is requesting the core to perform. 0x0: Reserved 0x1: Set Endpoint Configuration, 64-bit Parameter 0x2: Set Endpoint Transfer Resource Configuration, 32-bit Parameter 0x3: Get Endpoint State, No Parameter Needed 0x4: Set Stall, No Parameter Needed 0x5: Clear Stall, No Parameter Needed 0x6: Start Transfer, 64-bit parameter 0x7: Update Transfer, No Parameter Needed 0x8: End Transfer, No Parameter Needed 0x9: Start New Configuration, No Parameter Needed

8.11.7.14 0xCA00 Device Interrupt Moderation Register (Default Value:0x0000_0000)

Offset: 0xCA00			Register Name: DEPIMOD
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0000	DEVICE_IMODC Interrupt Moderation Down Counter Loaded with the DEVICE_IMODI value, whenever the hardware interrupt(n) line is de-asserted from the asserted state, counts down to 0, and stops. The interrupt(n) is signaled whenever this counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events (that is, event count is non-zero). This counter may be directly written by software at any time to alter the interrupt rate.
15:0	R/W	0x0	DEVICE_IMODI Moderation Interval (DEVICE_IMODI) This field holds the minimum inter-interrupt interval between events. The interval is specified in terms of 250ns increments. A value of 0 disables the interrupt throttling logic and interrupts are generated immediately if event count becomes non-zero. In scaledown simulation mode, 4 ram clocks are

Offset: 0xCA00			Register Name: DEPIMOD
Bit	Read/Write	Default/Hex	Description
			used to time 250ns

8.11.8 Application Register Description

8.11.8.1 0x100000 USB2.0 Interface Status and Control Register (Default Value: 0x0000_0000)

Offset: 0x100000			Register Name:USB2_ISCR
Bit	Read/Write	Default/Hex	Description
31:27	R	0	BC_ID_Value_Status These fields indicate the Mult ID value.
26:25	R	0	USB Line Status [26]-DM [27]-DP
24	R	0	USB VBUS Status These filed indicate the VBUS status.
23:18	R/W	0	Forcerid 1xxxxx: Force the ID value of bit[22:18] output to SIE 0xxxxx: Select phy output the ID value to SIE
17:16	/	/	/
15:14	R/W	0	Force ID 0x: use external ID Status 10: force ID to LOW 11: force ID to HIGH
13:12	R/W	0	Force VBUS Valid (For SIE) 0x: use external VBUS Valid Status from VBUS Input or Line State 10: force VBUS Valid to LOW 11: force VBUS Valid to HIGH
11:10	R/W	0	External VBUS Valid Source Select 0x: External VBUS Valid detected from VBUS Input 10: External VBUS Valid detected from DP/DM Input 11: External VBUS Valid detected from either VBUS or DP/DM input
9	R/W	0	USB Wakeup Enable 0: Disable 1: Enable
8	R/W	0	USB Wakeup HOSC Enable 0: Disable 1: Enable
7	R/W1C	0	USB ID Mult Value Change Interrupt Status

Offset: 0x100000			Register Name:USB2_ISCR
Bit	Read/Write	Default/Hex	Description
			0 :No Change 1: Has Change
6	R/W1C	0	VBUS Input Change Detect Interrupt Status 0 :No Change 1: Has Change
5	R/W1C	0	ID Input Change Detect Interrupt Status 0 :No Change 1: Has Change
4	R/W1C	0	DP/DM Input Change Detect Interrupt Status 0 :No Change 1: Has Change
3	R/W	0	USB ID Mult Value Detect Enable 0 :Disable 1: Enable
2	R/W	0	VBUS Input Change Detect Interrupt Enable 0: Disable 1: Enable
1	R/W	0	ID Input Change Detect Interrupt Enable 0: Disable 1: Enable
0	R/W	0	DP/DM Input Change Detect Interrupt Enable 0: Disable 1: Enable

8.11.8.2 0x100010 USB2.0 PHY Control Register (Default Value: 0x0000_0018)

Offset: 0x100010			Register Name: USB2_PHYCTL
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
10	R/W	0x0	OTGDISABLE
9	R/W	0x0	DRVVBUS
8	R/W	0x0	VREGBYPASS
7	R/W	0x0	LOOPBACKENB
6	R/W	0x0	IDPULLUP
5	R/W	0x0	VBUSVLDEXT
4	R/W	0x1	VBUSVLDEXTSEL
3	R/W	0x1	SIDDQ
2	R/W	0x0	COMMONONN
1:0	R/W	0x0	VATESTENB

8.11.8.3 0x100014 USB2.0 PHY TEST Register (Default Value: 0x0000_0000)

Offset: 0x100014			Register Name: USB2_PHYTST
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	TESTBURNIN
13	R/W	0x0	TESTDATAOUTSEL
12	R/W	0x0	TESTCLK
11:8	R/W	0x0	TESTADDR[3:0]
7:0	R/W	0x0	TESTDATAIN[7:0]

8.11.8.4 0x100018 USB2.0 PHY Tune Register (Default Value: 0x05B3_33D4)

Offset: 0x100018			Register Name: USB2_PHYTUNE
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R/W	0x1	VDATREFTUNE[1:0]
25:23	R/W	0x3	COMPDISTUNE[2:0]
22:20	R/W	0x3	SQRXTUNE[2:0]
19	R/W	0x0	TXPREEMPPULSETUNE
18:16	R/W	0x3	OTGTUNE[2:0]
15:12	R/W	0x3	TXFSLSTUNE[3:0]
11:8	R/W	0x3	TXVREFTUNE[3:0]
7:6	R/W	0x3	TXHSXVTUNE[1:0]
5:4	R/W	0x1	TXRISETUNE[1:0]
3:2	R/W	0x1	TXRESTUNE[1:0]
1:0	R/W	0x0	TXPREEMPAMPTUNE[1:0]

8.11.8.5 0x100024 USB2.0 PHY Status Register (Default Value: 0x0000_0000)

Offset: 0x100024			Register Name: USB2_PHYSTS
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R	0x0	TESTDATAOUT[3:0]

8.12 PCIe2.1

8.12.1 Overview

The PCI Express Controller (PCIe) is a general purpose I/O interconnect, which provides low pin count, high reliability, and high-speed data transfer at rates of up to 5.0 Gbps per lane per direction.

Complies with PCI Express Base 2.1 Specification

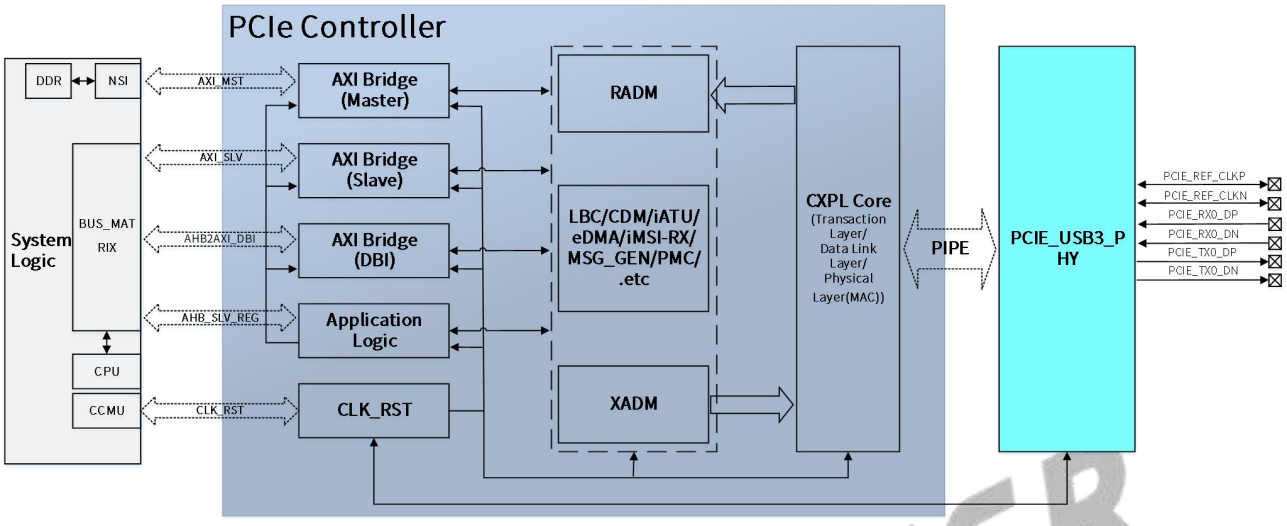
The PCIe controller includes the following features:

- All non-optional features of the PCI Express Base Specification, Revision 2.1
- Supports Gen1(2.5 Gbit/s), Gen2 (5.0 Gbit/s) speed
- Only supports Root Complex (RC) mode
- Up to 1 lane link width
- Configurable max_payload_size and supports 1024 bytes
- Internal Address Translation Unit (iATU) supports 8 inbound and 8 outbound address translation regions
- Embedded DMA with hardware flow control supports 4 write/read channels.
- MSI with Per-Vector Masking (PVM) and extended message data for MSI
- PCI Express Active State Power Management (ASPM)
- PCI Express Advanced Error Reporting (AER)

8.12.2 Block Diagram

The following figure shows the functional block diagram of the PCIe.

Figure 8-42 PCIe Block Diagram



The PCIe controller contains the following modules:

Table 8-32 PCIe Module

Module	Description
Common Express Port Logic (CXPL)	This module implements the basic functionality for the PCI Express physical, link, and transaction layers. The CXPL implements a large part of the transaction layer logic, all of the data link layer logic, and the MAC portion of the physical layer, including the link training and status state machine (LTSSM). The CXPL connects to the external PHY through the PIPE.
Transmit Application-Dependent Module (XADM)	This module implements the application-specific functionality of the PCI Express transaction layer for packet transmission. Its functions include: • TLP Arbitration • TLP Formation • Flow Control (FC) Credit checking The transmit path uses a cut-through architecture. It does not implement transmit buffering/queues (other than the retry buffer). The controller maintains an internal Target Completion Lookup Table to store certain TLP header information from the Rx request. Your application can use this information for transmitting completions.
Receive Application-Dependent Module (RADM)	This module implements application-specific functionality of the PCI Express transaction layer for packet reception. Its functions include:

Module	Description
	• Sorting/filtering of received TLPs. The filtering rules and routing are configurable. • Buffering and queuing of the received TLPs. • Routing of received TLP to the controller's receive interfaces. The RADM maintains a Receive Completion Lookup Table (LUT) for completion tracking and completion-timeout monitoring of Tx non-posted requests. It indicates a timeout when an expected Rx completion does not arrive within the timeout period.
Configuration-Dependent Module (CDM)	This module implements: • Standard PCI Express configuration space • Controller-specific register space (Port Logic Registers)
Power Management Controller (PMC)	This module implements the power management features of the PCIe controller.
Local Bus Controller (LBC) and Data Bus Interface (DBI)	The LBC module provides a mechanism for a link partner (in EP mode only) or a local CPU (through the DBI) to access: • Internal registers (in the CDM) • External application registers connected externally to the ELBI
Message Generation Module (MSG_GEN)	This module transmits messages generated by the controller.
Integrated MSI Receiver (iMSI-RX)	The AXI bridge provides an integrated MSI reception module to detect and terminate inbound MSI requests(received on the RX wire).
Embedded DMA (eDMA)	The RC system CPU, or the EP application CPU, can offload the transferring of large blocks of data to the embedded DMA controller1, leaving the CPU free to perform other tasks. You can configure the DMA to have one to eight read channels and one to eight write channels.
Internal Address Translation Unit (iATU)	The PCIe controller uses the iATU to implement a local address translation scheme that replaces the TLP address and TLP header fields in the current TLP request header.

8.12.3 Functional Description

8.12.3.1 External Signals

The following table describes the external signals of the PCIe.

Table 8-33 PCIe External Signals

Signal Name	Description	Type
PCIE-REF-CLKN	PCIe2.1 Differential Signal REFCLK (Negative)	A I/O
PCIE-REF-CLKP	PCIe2.1 Differential Signal REFCLK (Positive)	A I/O
PCIE-REXT	PCIe2.1 External Reference Resistor	AO

Signal Name	Description	Type
PCIE-RX0-DN	PCIe2.1 Differential Signal of RX (Negative)	A I/O
PCIE-RX0-DP	PCIe2.1 Differential Signal of RX (Positive)	A I/O
PCIE-TX0-DN	PCIe2.1 Differential Signal of TX (Negative)	A I/O
PCIE-TX0-DP	PCIe2.1 Differential Signal of TX (Positive)	A I/O
PCIE0-PERSTN	PCIe2.1 Warm Reset	O
PCIE0-WAKEN	PCIe2.1 Wake Up	I
PCIE0-CLKREQN	PCIe2.1 Clock Request from PCIe Peripheral	I
VCC18-PCIE	1.8 V Power Supply for PCIe2.1	P
VDD09-PCIE	0.9 V Power Supply for PCIe2.1	P

8.12.3.2 Clock Sources

The following table describes the clock sources of the PCIe.

Table 8-34 PCIe Clock Sources

Clock Sources	Description	Module
USB3_PCIE_REF_CLK	24 MHz, USB3.1 DRD&Pcie2.1 PHY reference clock.	CCU
AUX_CLK	24 MHz, working clock in low power mode of the PCIe.	
MBUS_CLK	600 MHz, PCIe AXI master/slave bus clock.	
AHB_CLK	200 MHz, PCIe bus clock.	
PIPE_CLK	62.5 MHz/ 125MHz, normal working clock for the PCIe controller operating in Gen1/Gen2 mode.	

8.12.3.3 PCIe Reference Clock

PCIe reference clock is a 100M differential clock supplied for the PCIe PHY. There are two clock sources.

- From Internal SoC

Configure PHY to use internal clock and enable the clock output via software. The REFCLKP/REFCLKN signal of PCIe controller serves as output signal and provides 100M differential clock for external EP.

- From External Clock Generator

Configure PHY to use external clock and disable the clock output via software. The REFCLKP/REFCLKN signal of PCIe controller serves as input signal and the external clock generator provides 100M differential clock for PHY.

8.12.3.4 PCIe Memory Mapping

The address space of PCIe controller can be partitioned into three spaces.

- Core Configuration Space (CCS): The configuration register space of the PCIe controller itself. It is also the standartd configuration register space defined by the PCIe specification.
- User Defined Space (UDS): The custom register space for the PCIe controller itself.
- Slave Command Space (SCS): Address space for configuraion transaction and memory transaction. The read and write operations of this space will be transformed by the PCIe controller into configuration read and write transactions or memory read and write transactions in PCIe domain. The PCIe command space segmentation is 0x20000000-0x2FFFFFFF.

8.12.3.5 ATU Operation

ATU is an address translation unit in PCIe controller and is used for transaction transformation and address translation. There are two types of ATU: Outbound ATU and Inbound ATU.

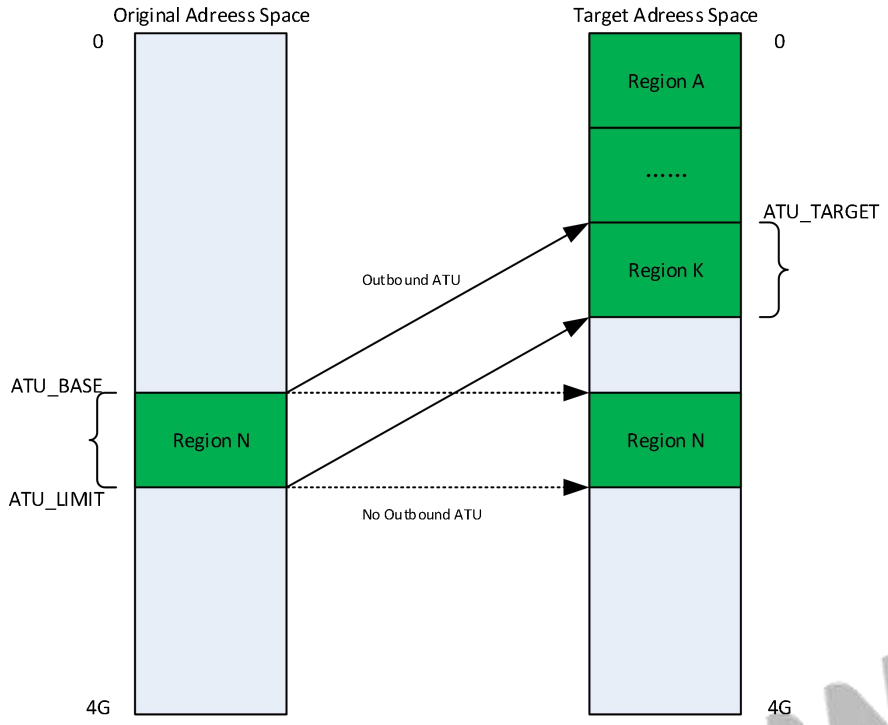
Outbound ATU

Outbound ATU is used to transform the read/write operation in CPU domain of the original address space into the read/write transaction in PCIe domain of the target address space. If the Outbound ATU is used, the original address in the CPU domain will be translated into another different address in the PCIe domain. If the Outbound ATU is not used, the PCIe controller will not perform address translation. The read/write operation initiated in the CPU domain will be transformed into the read/write transaction at the same address in the PCIe domain.

The following shows an example:

- When Outbound ATU is used, set address Region N in the CPU domain to be translated into Region K in PCIe domain. The read/write operation initiated at address Region N (CPU domain) will be transformed into the read/write transaction at address Region K (PCIe domain).
- When Outbound ATU is not used, read/write operation initiated at address Region N (CPU domain) will be transformed into the read/write transaction at address Region N (PCIe domain).

Figure 8-43 Outbound ATU



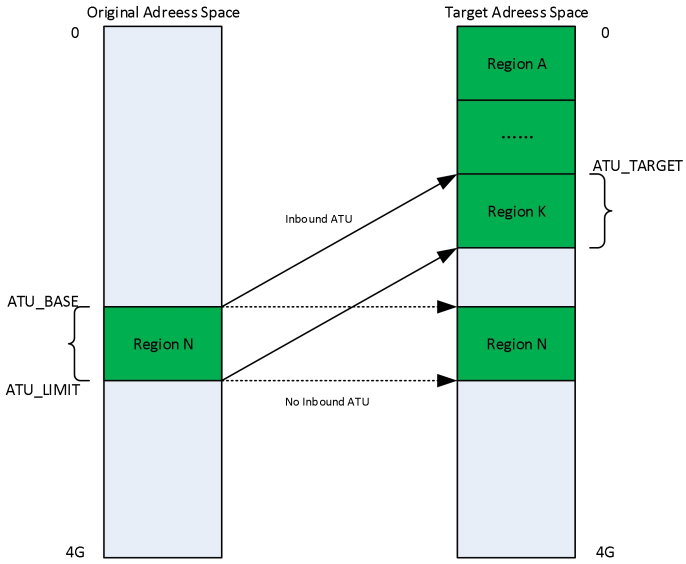
Inbound ATU

Inbound ATU is used to transform the read/write transaction in the PCIe domain of the original address space into the read/write operation in the CPU domain of the target address space. If Inbound ATU is used, the original address in the PCIe domain will be translated into another different address in the CPU domain. If the Inbound ATU is not used, the PCIe controller will not perform address translation. The read/write transaction initiated in the PCIe domain will be transformed into the read/write operation at the same address in the CPU domain.

The following shows an example:

- When Inbound ATU is used, set address Region N in the PCIe domain to be translated into Region K in the CPU domain. The read/write transaction initiated at address Region N (PCIe domain) will be transformed into the read/write operation at address Region K (CPU domain).
- When Inbound ATU is not used, read/write transaction initiated at address Region N (PCIe domain) will be transformed into the read/write operation at address Region N (CPU domain).

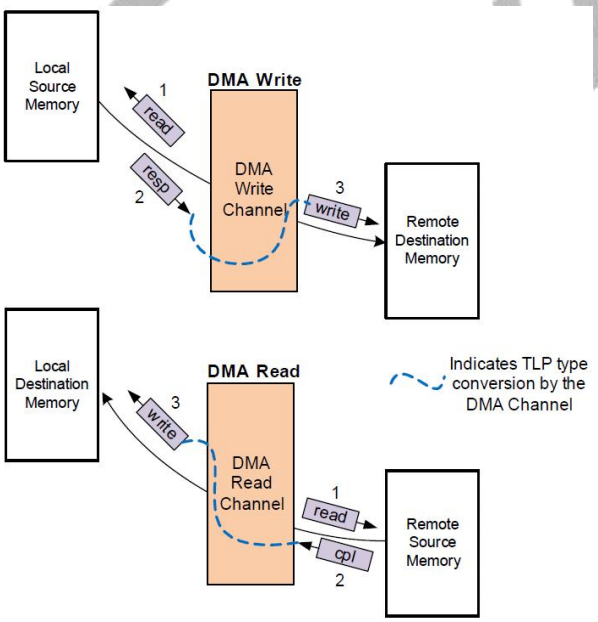
Figure 8-44 Inbound ATU



8.12.3.6 DMA Operation

There is a private DMA with read channels and write channels in the PCIe controller. The following figure deiscribes the DMA write and read process.

Figure 8-45 DMA Operation



- DMA Write Channel

  the DMA write channel is used for data transfer from local bus address space to the address space in the PCIe domain. First, DMA controller reads data from the local bus address space and writes them to the address space in the CPU domain. Then, the PCIe controller transforms the write operation initiated by DMA into a write transaction in the PCIe domain and writes data to the destination address space in the PCIe domain.

- DMA Read Channel

  The DMA read channel is used for data transfer from the address space in the PCIe domain to the local bus address space such as DRAM address space. If a read operation is initiated by DMA in the original address space of the CPU domain, the PCIe controller will transform the read operation into a read transaction in the PCIe domain and write data to the local bus address space.

8.12.3.7 MSI Operation

Message Signaled Interrupt (MSI) is a kind of mechanism that Endpoints send interrupt requests to the CPU connected with the Root Complex, which uses memory write transaction. The transaction message for transmitting interrupt information is MSI message.

Assume an Endpoint needs to send a MSI interrupt request to CPU. First, the Endpoint needs to initiate a memory write transaction in MSI address of PCIe domain, which will be transformed into a MSI interrupt signal to CPU by the PCIe controller after the transaction is detected. Software obtains the Endpoint sending interrupt request and its interrrupt vector according to the MSI message.

8.12.4 Register List

Module Name	Base Address
PCIE	0x04800000

Register Class	Offset
User Defined Registers	0x00400000 - 0x0047FFFF

Register Name	Offset	Description
MSTR_AWMISC_INFO_0	0x0100	PCIE AXI Master Write Misc Information Register0
MSTR_AWMISC_INFO_1	0x0104	PCIE AXI Master Write Misc Information Register1
MSTR_AWMISC_INFO_HDR_34DW_0	0x0108	PCIE AXI Master Write Misc Information Header Register0
MSTR_AWMISC_INFO_HDR_34DW_1	0x010C	PCIE AXI Master Write Misc Information Header Register1
MSTR_AWMISC_INFO_OTHER	0x0110	PCIE AXI Master Write Misc Information Other Register
MSTR_ARMISC_INFO_0	0x0120	PCIE AXI Master Read Misc Information Register0
MSTR_ARMISC_INFO_1	0x0124	PCIE AXI Master Read Misc Information Register1
MSTR_ARMISC_INFO_OTHER	0x0130	PCIE AXI Master Read Misc Information Other Register
MSTR_BMISC_INFO	0x0150	PCIE AXI Master Write Response Misc Information Register

Register Name	Offset	Description
MSTR_RMISC_INFO	0x0160	PCIE AXI Master Read Misc Information Register
PCIE_SLV_AWMISC_CTRL	0x0200	PCIE Write Transaction Control Register
SLV_AWMISC_INFO_ATU_BYP	0x0204	PCIE AXI SLAVE Write Misc Information ATU Register
SLV_AWMISC_INFO_HDR_34DW_0	0x0208	PCIE AXI SLAVE Write Misc Information Header Register0
SLV_AWMISC_INFO_HDR_34DW_1	0x020C	PCIE AXI SLAVE Write Misc Information Header Register1
SLV_AWMISC_INFO_OTHER_0	0x0210	PCIE AXI SLAVE Write Misc Information Other Register0
SLV_AWMISC_INFO_OTHER_1	0x0214	PCIE AXI SLAVE Write Misc Information Other Register1
SLV_ARMISC_CTRL	0x0220	PCIE AXI SLAVE Read Control Register
SLV_ARMISC_INFO_ATU_BYP	0x0224	PCIE AXI SLAVE Read Misc Information ATU Register
SLV_ARMISC_INFO_OTHER	0x0230	PCIE AXI SLAVE Read Misc Information Other Register
SLV_BMISC_INFO	0x0250	PCIE AXI Slave Write Response Misc Information Register
SLV_RMISC_INFO	0x0260	PCIE AXI Slave Read Response Misc Information Register
APP_CLK_REQ_N	0x0400	PCIE APP Clock Request Register
APP_INIT_RST	0x0500	PCIE APP Initial Reset Register
VEN_MSG_REQ	0x0700	PCIE VEN MSG Request Register
VEN_MSG_CFG_0	0x0704	PCIE VEN MSG Config Register0
VEN_MSG_CFG_1	0x0708	PCIE VEN MSG Config Register1
VEN_MSG_DATA_0	0x070C	PCIE VEN MSG Data Register0
VEN_MSG_DATA_1	0x0710	PCIE VEN MSG Data Register1
SII_ELEC	0x0A00	PCIE SII Electromechanical Register
FRS_READY	0x0B04	PCIE FRS READY Register
PCIE_LTSSM_ENABLE	0x0C00	PCIE LTSSM Enable Register
SII_INT_MASK_0	0x0E00	PCIE SII Interrupt Mask Register0
SII_INT_MASK_1	0x0E04	PCIE SII Interrupt Mask Register1
SII_INT_0	0x0E08	PCIE SII Interrupt Register0
SII_INT_1	0x0E0C	PCIE SII Interrupt Register1
SII_APP_PM_UNLOCK	0x1000	PCIE SII APP PM UNLOCK Register
SII_APP_PM_0	0x1100	PCIE SII Power Manage Register0

8.12.5 Register Description

8.12.5.1 0x0100 PCIE AXI Master Write Misc Information Register0 (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: MSTR_AWMISC_INFO_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_0 AXI Master Write Misc Information. AXI master write transaction associated miscellaneous information from the TLP received by the native PCIe controller. This is a signal that the application can optionally use. It is not part of the standard AXI interface. • Bus number, device number, function number, and register numbers are overlaid to the address bus when type is configuration transactions. • Message contents are also overlaid to the address bus for MSG TLPs. Bits [7:0] indicate the message code when the type is message. The bit fields are mapped as follows: • [7:0]: Reserved except for MSG TLP. Bits [7:0] indicate the message code when the type is message. • [8:6]: BAR number of TLP • [9]: TLP is an I/O • [10]: TLP is in ROM range • [13:11]: TLP's Function number. Function numbering starts at '0'. This field is not used when CX_SRIOV_ENABLE =1 or CX_ARI_ENABLE =1. • [14]: TLP's NS bit • [15]: TLP's RO bit • [18:16]: TLP's TC bits • [23:19]: TLP's TYPE • 31:24]: TLP's requester ID_0

8.12.5.2 0x0104 PCIE AXI Master Write Misc Information Register1 (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: MSTR_AWMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	MSTR_AWMISC_INFO_1 AXI Master Write Misc Information. AXI master write

Offset: 0x0104			Register Name: MSTR_AWMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
			transaction associated miscellaneous information from the TLP received by the native PCIe controller. This is a signal that the application can optionally use. It is not part of the standard AXI interface. • Bus number, device number, function number, and register numbers are overlaid to the address bus when type is configuration transactions. • Message contents are also overlaid to the address bus for MSG TLPs. Bits [7:0] indicate the message code when the type is message. The bit fields are mapped as follows: [8:0]: TLP's requester ID_1 [15:9]: TLP's TAG

8.12.5.3 0x0108 PCIE AXI Master Write Misc Information Header Register0 (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: MSTR_AWMISC_INFO_HDR_34DW_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_HDR_34DW_0 mstr_awmisc_info_hdr_34dw_status[31:0]

8.12.5.4 0x010C PCIE AXI Master Write Misc Information Header Register1 (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: MSTR_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_AWMISC_INFO_HDR_34DW_1 mstr_awmisc_info_hdr_34dw_status[63:32]

8.12.5.5 0x0110 PCIE AXI Master Write Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: MSTR_AWMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R	0x0	MSTR_AWMISC_INFO_LAST_DCMP_TLP mstr_awmisc_info_last_dcmp_tlp_status
26	R	0x0	MSTR_AWMISC_INFO_EP mstr_awmisc_info_ep_status
25	R	0x0	MSTR_AWMISC_INFO_NW mstr_awmisc_info_nw_status

Offset: 0x0110			Register Name: MSTR_AWMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
24	R	0x0	MSTR_AWMISC_INFO_IDO mstr_awmisc_info_ido_status
23:22	R	0x0	MSTR_AWMISC_INFO_ATS mstr_awmisc_info_ats_status[1:0]
21:16	R	0x0	MSTR_AWMISC_INFO_DMA mstr_awmisc_info_dma_status[5:0]
15:11	/	/	/
10:0	R	0x0	MSTR_AWMISC_INFO_TPH mstr_awmisc_info_tph_status[10:0]

8.12.5.6 0x0120 PCIE AXI Master Read Misc Information Register0 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: MSTR_ARMISC_INFO_0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	MSTR_ARMISC_INFO_0 mstr_armisc_info_status[31:0]

8.12.5.7 0x0124 PCIE AXI Master Read Misc Information Register1 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: MSTR_ARMISC_INFO_1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	MSTR_ARMISC_INFO_1 mstr_armisc_info_status[47:32]

8.12.5.8 0x0130 PCIE AXI Master Read Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: MSTR_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R	0x0	MSTR_ARMISC_INFO_ZEROREAD mstr_armisc_info_zeroread_status
27	R	0x0	MSTR_ARMISC_INFO_LAST_DCMP_TLP mstr_armisc_info_last_dcmp_tlp_status
26	/	/	/
25	R	0x0	MSTR_ARMISC_INFO_NW mstr_armisc_info_nw_status
24	R	0x0	MSTR_ARMISC_INFO_IDO mstr_armisc_info_ido_status

Offset: 0x0130			Register Name: MSTR_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
23:22	/	/	/
21:16	R	0x0	MSTR_ARMISC_INFO_DMA mstr_armisc_info_dma_status[5:0]
15:11	/	/	/
10:0	R	0x0	MSTR_ARMISC_INFO_TPH mstr_armisc_info_tph_status[10:0]

8.12.5.9 0x0150 PCIE AXI Master Write Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: MSTR_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	MSTR_BMISC_INFO_CPL_STAT AXI Master Write Response selection bus. This controls the response to be sent on the wire in the case of successful write requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. ▪ 00: SC (Successful Completion) ▪ 01: CA (Completer Abort) ▪ 10: UR (Unsupported Request) ▪ 11: SC (Successful Completion) Your application must drive the same value on mstr_bmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_bmisc_info_cpl_stat to UR: ▪ If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. ▪ If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.

8.12.5.10 0x0160 PCIE AXI Master Read Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: MSTR_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x0	MSTR_RMISC_INFO_CPL_STAT AXI Master Read Response selection bus. This bus

Offset: 0x0160			Register Name: MSTR_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
			controls the response sent on the PCIe wire in the case of successful read requests. The controller always sends a CA (Completer Abort) response when it receives SLVERR/DECERR. ▪ 00: SC (Successful Completion) ▪ 01: CA (Completer Abort) ▪ 10: UR (Unsupported Request) ▪ 11: SC (Successful Completion) Your application must drive the same value on mstr_rmisc_info_cpl_stat throughout the complete response. For a multi-beat response, when you set mstr_rmisc_info_cpl_stat to UR: ▪ If the first beat of the response produces a slave error/decode error, the controller sends a CPL with status as CA. ▪ If any beat (other than the first beat) of the response has a slave/decode error, the controller sends a CPL with status as UR.
15:13	/	/	/
12:0	R/W	0x0	MSTR_RMISC_INFO AXI Master Read Response Transaction Associated Misc Information. This is a signal that the application can optionally use. It is not part of standard AXI interface. All reserved bits must be connected to logic '0'. ▪ [1:0]: Reserved ▪ [2]: Reserved. ▪ [6:3]: Reserved ▪ [7]: TLP's EP bit ▪ [12:8]: Reserved.

8.12.5.11 0x0200 PCIE SLAVE Write Msic Control Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PCIE_SLV_AWMISC_CTRL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	AXI transaction is a DBI access. This is for SHARED DBI mode only.
20:13	R/W	0x00	MSG MSG Code of TLPs

Offset: 0x0200			Register Name: PCIE_SLV_AWMISC_CTRL
Bit	Read/Write	Default/Hex	Description
12:10	R/W	0x0	TC TC bits of TLPs
9	R/W	0x0	RO RO bit of TLPs
8	R/W	0x0	NS NS bit of TLPs
7	/	/	/
6	R/W	0x0	EP EP bit of TLPs
5	R/W	0x0	SERIALIZE_NP_REQ Serialize NP Requests
4:0	R/W	0x0	TYPE Type of TLPs

8.12.5.12 0x0204 PCIE AXI SLAVE Write Misc Information ATU Register (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: SLV_AWMISC_INFO_ATU_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_AWMISC_INFO_ATU_BYPASS AXI Slave Write Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit

8.12.5.13 0x0208 PCIE AXI SLAVE Write Misc Information Header Register0 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: SLV_AWMISC_INFO_HDR_34DW_0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SLV_AWMISC_INFO_HDR_34DW_0 slv_awmisc_info_hdr_34dw[31:0] ,AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. **Note: The data is in big endian format, that is, slv_awmisc_info_hdr_34dw[7:0] contains byte 15 of header DW.**

8.12.5.14 0x020C PCIE AXI SLAVE Write Misc Information Header Register1 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: SLV_AWMISC_INFO_HDR_34DW_1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SLV_AWMISC_INFO_HDR_34DW_1 slv_awmisc_info_atu_bypass[63:32] ,AXI Slave 3rd and 4th header DWs. The application drives this bus with the 3rd and 4th Header DWs it intends to send on a PCIe Msg/MsgD. **Note: The data is in big endian format.**

8.12.5.15 0x0210 PCIE AXI SLAVE Write Misc Information Other Register0 (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: SLV_AWMISC_INFO_OTHER_0
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	SLV_AWMISC_INFO_NW AXI Slave Write Transaction's Request ATS No Write (NW) Bit. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
24	R/W	0x0	SLV_AWMISC_INFO_IDO AXI Slave Write Transaction's IDO bit. Enables ID-base ordering on outbound requests. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
23:11	/	/	/
10:0	R/W	0x0	SLV_AWMISC_INFO_TPH AXI Slave Write Request TLP Processing Hints. The bits are mapped as follows: ▪ [0]: TH (TLP Processing Hint present) ▪ [2:1] PH (TLP Processing Hint) ▪ [10:3] ST (Steering Tag)

8.12.5.16 0x0214 PCIE AXI SLAVE Write Misc Information Other Register1 (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: SLV_AWMISC_INFO_OTHER_1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLV_AWMISC_INFO_P_TAG AXI Slave Write Request Tag. Sets the TAG number for output posted requests. It is expected that your

Offset: 0x0214			Register Name: SLV_AWMISC_INFO_OTHER_1
Bit	Read/Write	Default/Hex	Description
			application normally sets this to '0' except when generating ATS invalidate requests.

8.12.5.17 0x0220 PCIE AXI SLAVE Read Control Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: SLV_ARMISC_CTRL
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21	R/W	0x0	AXI transaction is a DBI access. This is for SHARED DBI mode only.
20:13	R/W	0x00	MSG TLP’s MSG Code
12:10	R/W	0x0	TC TLP’s TC bits
9	R/W	0x0	RO TLP’s RO bit
8	R/W	0x0	NS TLP’s NS bit
7	/	/	/
6	R/W	0x0	EP TLP’s EP bit
5	/	/	/
4:0	R/W	0x0	TYPE TLP’s TYPE

8.12.5.18 0x0224 PCIE AXI SLAVE Read Misc Information ATU Register (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: SLV_ARMISC_INFO_ATU_BYP
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	SLV_ARMISC_INFO_ATU_BYPASS AXI Slave Read Request Internal ATU Bypass. When set it indicates that this request should not be processed by the internal address translation unit

8.12.5.19 0x0230 PCIE AXI SLAVE Read Misc Information Other Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: SLV_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description

Offset: 0x0230			Register Name: SLV_ARMISC_INFO_OTHER
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	SLV_ARMISC_INFO_NW AXI Slave Read Transaction's Request AT No Write (NW) Bit. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
24	R/W	0x0	SLV_ARMISC_INFO_IDO AXI Slave Read Transaction's IDO bit. Enables ID-base ordering on outbound requests. This is a signal that the application can optionally use. It is not part of the standard AXI interface.
23:11	/	/	/
10:0	R/W	0x0	SLV_ARMISC_INFO_TPH AXI Slave Read Request TLP Processing Hints. The bits are mapped as follows: ▪ [0]: TH (TLP Processing Hint present) ▪ [2:1] PH (TLP Processing Hint) ▪ [10:3] ST (Steering Tag)

8.12.5.20 0x0250 PCIE AXI Slave Write Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: SLV_BMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R	0x0	SLV_BMISC_INFO_STATUS slv_bmisc_info_status

8.12.5.21 0x0260 PCIE AXI Slave Read Response Misc Information Register (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: SLV_RMISC_INFO
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R	0x0	SLV_RMISC_INFO_IDO_STATUS slv_rmisc_info_ido_status
23:11	/	/	/
10:0	R	0x0	MSTR_RMISC_INFO mstr_rmisc_info

8.12.5.22 0x0400 PCIE APP Clock Request Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: APP_CLK_REQ_N
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	APP_CLK_REQ_N Indicates that the application logic is ready to have reference clock removed. In designs which support reference clock removal through either L1 PM Sub-states or L1 CPM, the application should set this signal to 1'b when it is ready to have reference clock removed. If the application does not want to remove reference clock it should set this signal to 1'b0.

8.12.5.23 0x0500 PCIE APP Initial Reset Register (Default Value: 0x0000_0000)

Offset: 0x0500			Register Name: APP_INIT_RST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	APP_INIT_RST app_init_rst_ahb Request from your application to send a hot reset to the upstream port. The hot reset request is sent when a single cycle pulse is applied to this pin. In an upstream port, you should set this input to '0'. Note: This signal is not used by the controller to set the SBR field in the BRIDGE_CTRL_INT_PIN_INT_LINE_REG register. During the transition from DL_Active to DL_inactive, assertion of app_init_rst signal indicates a Surprise Down Error, but setting of SBR field in the BRIDGE_CTRL_INT_PIN_INT_LINE_REG register through DBI does not trigger a Surprise Down Error.

8.12.5.24 0x0700 PCIE VEN MSG Request Register (Default Value: 0x0000_0000)

Offset: 0x0700			Register Name: VEN_MSG_REQ
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	VEN_MSG_REQ ven_msG_req_ahb, Request from your application to send a vendor-defined Message. Once asserted,

Offset: 0x0700			Register Name: VEN_MSG_REQ
Bit	Read/Write	Default/Hex	Description
			ven_msg_req must remain asserted until the controller asserts ven_msg_grant.

8.12.5.25 0x0704 PCIE VEN MSG Config Register0 (Default Value: 0x0000_0000)

Offset: 0x0704			Register Name: VEN_MSG_CFG_0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	VEN_MSG_CODE The Message Code for the vendor-defined Message TLP.
23:16	/	/	/
15:13	R/W	0x0	VEN_MSG_ATTR The Attributes field for the vendor-defined Message TLP. ▪ Width is three bits when CX_IDO_ENABLE =1 ▪ Width is two bits when CX_IDO_ENABLE =0
12:8	R/W	0x0	VEN_MSG_TYPE The Type field for the vendor-defined Message TLP.
7:6	R/W	0x0	VEN_MSG_FMT The Format field for the vendor-defined Message TLP. Should be set to 0x1.
5:3	R/W	0x0	VEN_MSG_TC The Traffic Class field for the vendor-defined Message TLP.
2	R/W	0x0	VEN_MSG_TD The TLP Digest (TD) bit for the vendor-defined Message TLP, valid when ven_msg_req is asserted.
1	R/W	0x0	VEN_MSG_EP The Poisoned TLP (EP) bit for the vendor-defined Message TLP.
0	/	/	/

8.12.5.26 0x0708 PCIE VEN MSG Config Register1 (Default Value: 0x0000_0000)

Offset: 0x0708			Register Name: VEN_MSG_CFG_1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	VEN_MSG_TAG Tag for the vendor-defined Message TLP.
15:13	/	/	/

Offset: 0x0708			Register Name: VEN_MSG_CFG_1
Bit	Read/Write	Default/Hex	Description
12:10	R/W	0x0	VEN_MSG_FUNC_NUM Function Number for the vendor-defined Message TLP. Function numbering starts at '0'.
9:0	R/W	0x0	VEN_MSG_LEN The Length field for the vendor-defined Message TLP (indicates length of data payload in dwords). Should be set to 0x0.

8.12.5.27 0x070C PCIE VEN MSG Data Register0 (Default Value: 0x0000_0000)

Offset: 0x070c			Register Name: VEN_MSG_DATA_0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VEN_MSG_DATA_0 fourth dwords of the Vendor Defined Message header where: ▪ Bytes 12-15 (fourth header dword) =ven_msg_data[31:0], where ven_msg_data[7:0] =byte 15

8.12.5.28 0x0710 PCIE VEN MSG Data Register1 (Default Value: 0x0000_0000)

Offset: 0x0710			Register Name: VEN_MSG_DATA_1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VEN_MSG_DATA_1 third dwords of the Vendor Defined Message header where: ▪ Bytes 8-11 (third header dword) =ven_msg_data[63:32]

8.12.5.29 0x0A00 PCIE SII Electromechanical Register (Default Value: 0x0000_0000)

Offset: 0x0A00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	SYS_EML_INTERLOCK_ENGAGED sys_eml_interlock_engaged [0] , System Electromechanical Interlock Engaged. Indicates whether the system electromechanical interlock is engaged and controls the state of the

Offset: 0x0A00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
			Electromechanical Interlock Status bit in the Slot Status register.
6	R/W	0x0	SYS_CMD_CPLED_INT sys_cmd_cpled_int[0] , Command completed Interrupt. Indicates that the Hot-Plug controller completed a command. There is a separate sys_cmd_cpled_int input bit for each function in your controller configuration
5	R/W	0x0	SYS_PRE_DET_CHGED sys_pre_det_chged[0] Presence Detect Changed. Indicates that the state of card present detector has changed. There is a separate sys_pre_det_chged input bit for each function in your controller configuration.
4	R/W	0x0	SYS_MRL_SENSOR_CHGED sys_mrl_sensor_chged[0] , MRL Sensor Changed. Indicates that the state of MRL sensor has changed. There is a separate sys_mrl_sensor_chged input bit for each function in your controller configuration.
3	R/W	0x0	SYS_PWR_FAULT_DET sys_pwr_fault_det[0] , Power Fault Detected. Indicates the power controller detected a power fault at this slot. There is a separate sys_pwr_fault_det input bit for each function in your controller configuration.
2	R/W	0x0	SYS_MRL_SENSOR_STATE sys_mrl_sensor_state[0] , MRL Sensor State. Indicates the state of the manually-operated retention latch (MRL) sensor: ▪ 0: MRL is closed ▪ 1: MRL is open There is a separate sys_mrl_sensor_state input bit for each function in your controller configuration.
1	R/W	0x0	SYS_PRE_DET_STATE sys_pre_det_state[0] , Presence Detect State. Indicates whether or not a card is present in the slot: ▪ 0: Slot is empty ▪ 1: Card is present in the slot There is a separate sys_pre_det_state input bit for each function in your controller configuration.
	R/W	0x0	SYS_ATTEN_BUTTON_PRESSED

Offset: 0x0A00			Register Name: SII_ELEC
Bit	Read/Write	Default/Hex	Description
0			sys_atten_button_pressed[0] , Attention Button Pressed. Indicates that the system attention button was pressed, sets the Attention Button Pressed bit in the Slot Status Register. There is a separate sys_atten_button_pressed input bit for each function in your controller configuration.

8.12.5.30 0x0B04 PCIE FRS READY Register (Default Value: 0x0000_0000)

Offset: 0x0B04			Register Name: FRS_READY
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W	0x0	APP_PF0_FRS_READY app_pf_frs_ready[0] Defers FRS messaging when set to '0'.
3:0	/	/	/

8.12.5.31 0x0C00 PCIE LTSSM Enable Register (Default Value: 0x0000_0040)

Offset: 0x0C00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	APP_DBI_RO_WR_DISABLE app_dbi_ro_wr_disable DBI Read-only Write Disable ▪ 0: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is read-write. ▪ 1: MISC_CONTROL_1_OFF.DBI_RO_WR_EN register field is forced to 0 and is read-only.
30:1	/	/	/
0	R/W	0x0	APP_LTSSM_ENABLE Link Training Enable 0: Disable link training 1: Enable link training Driven low by your application after cold, warm or hot reset to hold the LTSSM in the Detect state until your application is ready for the link training to begin. When your application has finished reprogramming the controller configuration registers using the DBI, it asserts app_ltssm_enable to allow the LTSSM to continue link establishment. Can also be used to

Offset: 0x0C00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
			delay hot resetting of the controller until you have read out any register status. Cold Reset: ▪ Optionally hold LTSSM and delay link training, so that you can reprogram some registers through DBI. ▪ Set app_ltssm_enable =0 before your application de-asserts Power-On Reset (power_up_rst_n). Best way is to set app_ltssm_enable =0 at power-up or at assertion of core_rst_n. ▪ Wait for de-assertion of core_rst_n, sticky_rst_n, and non_sticky_rst_n. ▪ Write any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Link training starts. Hot Reset (Link Down Reset) : ▪ Optionally delay reset of the controller, so that you can read some registers through DBI. ▪ Set app_ltssm_enable =0 immediately (combinatorially) upon falling edge of smlh_req_rst_not. ▪ Keep app_ltssm_enable =0 until bridge finishes "flushing mode". ▪ Read any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Reset of controller begins (sticky_rst is not asserted). ▪ Optionally hold LTSSM and delay link training, so that you can reprogram some registers through DBI. ▪ Set app_ltssm_enable =0 immediately (combinatorially) upon falling edge of core_rst_n. ▪ Write any register through DBI. ▪ Set app_ltssm_enable =1. ▪ Link training starts. ▪ **Note: For Hot Reset, you can do both or either of the above (delay reset and/or delay link training). If you do both, you must do in order presented.** ▪ **Note: You must only de-assert this signal using one of the recommended timings described in the "Reset Requirements" section in the Architecture chapter of the Databook** To do otherwise (that is, de-assert it outside of the Detect LTSSM state) causes the controller to be reset

Offset: 0x0C00			Register Name: PCIE_LTSSM_ENABLE
Bit	Read/Write	Default/Hex	Description
			and the LTSSM moves immediately back to the Detect state. This transition is outside of the PCIe Specification and it might cause a PIPE protocol violation.

8.12.5.32 0x0E00 PCIE SII Interrupt Mask Register0 (Default Value: 0x0000_0000)

Offset: 0x0E00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	RADM_MSG_LTR_EN_MASK 0: Mask 1: Not Mask
28	R/W	0x0	DEASSERT_INTD_GRT_EN_MASK 0: Mask 1: Not Mask
27	R/W	0x0	DEASSERT_INTC_GRT_EN_MASK 0: Mask 1: Not Mask
26	R/W	0x0	DEASSERT_INTB_GRT_EN_MASK 0: Mask 1: Not Mask
25	R/W	0x0	DEASSERT_INTA_GRT_EN_MASK 0: Mask 1: Not Mask
24	R/W	0x0	ASSERT_INTD_GRT_EN_MASK 0: Mask 1: Not Mask
23	R/W	0x0	ASSERT_INTC_GRT_EN_MASK 0: Mask 1: Not Mask
22	R/W	0x0	ASSERT_INTB_GRT_EN_MASK 0: Mask 1: Not Mask
21	R/W	0x0	ASSERT_INTA_GRT_EN_MASK 0: Mask 1: Not Mask
20	R/W	0x0	CFG_LINK_EQ_REQ_INT_EN_MASK 0: Mask 1: Not Mask

Offset: 0x0E00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
19	R/W	0x0	CFG_BW_MGT_MSI_EN_MASK 0: Mask 1: Not Mask
18	R/W	0x0	CFG_BW_MGT_INT_EN_MASK 0: Mask 1: Not Mask
17	R/W	0x0	CFG_LINK_AUTO_BW_MSI_EN_MASK 0: Mask 1: Not Mask
16	R/W	0x0	CFG_LINK_AUTO_BW_INT_EN_MASK 0: Mask 1: Not Mask
15	R/W	0x0	PF0_HP_MSI_EN_MASK 0: Mask 1: Not Mask
14	R/W	0x0	PF0_HP_INT_EN_MASK 0: Mask 1: Not Mask
13	R/W	0x0	PF0_HP_PME_EN_MASK 0: Mask 1: Not Mask
12	R/W	0x0	RADM_INTD_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
11	R/W	0x0	RADM_INTC_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
10	R/W	0x0	RADM_INTB_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
9	R/W	0x0	RADM_INTA_DEASSERTED_EN_MASK 0: Mask 1: Not Mask
8	R/W	0x0	RADM_INTD_ASSERTED_EN_MASK 0: Mask 1: Not Mask
7	R/W	0x0	RADM_INTC_ASSERTED_EN_MASK 0: Mask 1: Not Mask
6	R/W	0x0	RADM_INTB_ASSERTED_EN_MASK 0: Mask

Offset: 0x0E00			Register Name: SII_INT_MASK_0
Bit	Read/Write	Default/Hex	Description
			1: Not Mask
5	R/W	0x0	RADM_INTA_ASSERTED_EN_MASK 0: Mask 1: Not Mask
4	R/W	0x0	PF0_CFG_PME_MSI_EN_MASK 0: Mask 1: Not Mask
3	R/W	0x0	PF0_CFG_PME_INT_EN_MASK 0: Mask 1: Not Mask
2	R/W	0x0	PF0_CFG_AER_RC_ERR_MSI_MASK 0: Mask 1: Not Mask
1	R/W	0x0	PF0_CFG_AER_RC_ERR_INT_EN_MASK 0: Mask 1: Not Mask
0	R/W	0x0	PF0_CFG_VPD_INT_EN_MASK 0: Mask 1: Not Mask

8.12.5.33 0x0E04 PCIE SII Interrupt Mask Register1 (Default Value: 0x0000_0000)

Offset: 0x0E04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PCIE_WAKE_N_CLR_EN_MASK 0: Mask 1: Not Mask
30	R/W	0x0	WAKE_CLR_EN_MASK 0: Mask 1: Not Mask
29	R/W	0x0	RADM_PM_TO_ACK_CLR_EN_MASK 0: Mask 1: Not Mask
28	R/W	0x0	RADM_PM_PME_CLR_EN_MASK 0: Mask 1: Not Mask
27	R/W	0x0	RADM_FATAL_ERR_CLR_EN_MASK 0: Mask 1: Not Mask
26	R/W	0x0	RADM_NONFATAL_ERR_CLR_EN_MASK

Offset: 0x0E04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
			0: Mask 1: Not Mask
25	R/W	0x0	RADM_CORRECTABLE_ERR_CLR_EN_MASK 0: Mask 1: Not Mask
24	R/W	0x0	CFG_SYS_ERR_RC_CLR_EN_MASK 0: Mask 1: Not Mask
23:22	/	/	/
21	R/W	0x0	PF0_FRS_GRANT_EN_MASK 0: Mask 1: Not Mask
20	R/W	0x0	RADM_VENDOR_MSG_EN_MASK 0: Mask 1: Not Mask
19	/	/	/
18	R/W	0x0	PF0_FRSQ_MSI_EN_MASK 0: Mask 1: Not Mask
17	R/W	0x0	PF0_CFG_UP_DRS_TO_FRS_EN_MASK 0: Mask 1: Not Mask
16	R/W	0x0	PF0_CFG_DRS_MSI_EN_MASK 0: Mask 1: Not Mask
15:12	/	/	/
11	R/W	0x0	PCIE_PERI_AR_INT_EN_MASK 0: Mask 1: Not Mask
10	R/W	0x0	PCIE_PERI_AW_INT_EN_MASK 0: Mask 1: Not Mask
9	R/W	0x0	RADM_QOVERFLOW_1_EN_MASK 0: Mask 1: Not Mask
8	R/W	0x0	RADM_QOVERFLOW_0_EN_MASK 0: Mask 1: Not Mask
7:5	/	/	/
4	R/W	0x0	RTLH_RFC_UPD_0_EN_MASK 0: Mask

Offset: 0x0E04			Register Name: SII_INT_MASK_1
Bit	Read/Write	Default/Hex	Description
			1: Not Mask
3	R/W	0x0	LINK_REQ_RST_NOT_EN_MASK 0: Mask 1: Not Mask
2	/	/	/
1	R/W	0x0	RDLH_LINK_UP_INT_MASK RDLH Link Up Interrupt Mask 0: Mask 1: Not Mask
0	R/W	0x0	SMLH_LINK_UP_INT_MASK SMLH Link Up Interrupt Mask 0: Mask 1: Not Mask

8.12.5.34 0x0E08 PCIE SII Interrupt Register0 (Default Value: 0x0000_0000)

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W1C	0x0	RADM_MSG_LTR One-clock-cycle pulse that indicates that the controller received an LTR message. The controller makes the message header available the radm_msg_payload output. It is also available the app_ltr_latency output. When RX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then no separate indication is given for the second message.
28	R/W1C	0x0	DEASSERT_INTD_GRT The signal deassert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTD Message to the upstream device.
27	R/W1C	0x0	DEASSERT_INTC_GRT The signal deassert_intc_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTC Message to the upstream device.
26	R/W1C	0x0	DEASSERT_INTB_GRT The signal deassert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTB Message to the upstream device.
25	R/W1C	0x0	DEASSERT_INTA_GRT

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
			The signal deassert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Deassert_INTA Message to the upstream device.
24	R/W1C	0x0	ASSERT_INTD_GRT The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device.
23	R/W1C	0x0	ASSERT_INTC_GRT The signal assert_intd_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTD Message to the upstream device.
22	R/W1C	0x0	ASSERT_INTB_GRT The signal assert_intb_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTB Message to the upstream device.
21	R/W1C	0x0	ASSERT_INTA_GRT The signal assert_inta_grt is a one-clock-cycle pulse that indicates that the controller sent an Assert_INTA Message to the upstream device.
20	R/W1C	0x0	CFG_LINK_EQ_REQ_INT Interrupt indicating to your application that the Link Equalization Request bit in the Link Status 2 Register has been set and the Link Equalization Request Interrupt Enable (Link Control 3 Register bit 1) is set.
19	R/W1C	0x0	CFG_BW_MGT_MSI The controller sets this pin when following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The Link Bandwidth Management Status register (Link Control Status register bit 14) is updated ▪ The Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set. reuse-pragma beginAttr Description This pin is set as a notification when the Link Bandwidth Management Status register (Link Status register bit 14) is updated and the Link Bandwidth Management Interrupt Enable (Link Control register bit 10) is set and in addition the msi or msix aare enabled . This bit is not applicable to, and is reserved, for endpoint devices and upstream ports of Switches. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
18	R/W1C	0x0	CFG_BW_MGT_INT The controller asserts cfg_bw_mgt_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0, and ▪ The Bandwidth Management Interrupt Enable bit in the Link Control register is set to 1, and ▪ The Bandwidth Management Interrupt Status bit in the Link Status register is set to 1. The cfg_bw_mgt_msi output is a pulse signal (only asserted for one clock cycle); but cfg_bw_mgt_int is a level signal. For upstream port: Reserved.
17	R/W1C	0x0	CFG_LINK_AUTO_BW_MSI The controller sets this pin when following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The Link Autonomous Bandwidth Status register (Link Status register bit 15) is updated. ▪ The Link Autonomous Bandwidth Interrupt Enable (Link Control register bit 11) is set. The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked. For upstream port: Reserved. <ct:CX_IS_EP>Reserved.
16	R/W1C	0x0	CFG_LINK_AUTO_BW_INT The controller asserts cfg_link_auto_bw_int when all of the following conditions are true: ▪ The INTx assertion disable bit in the Command register is 0, and ▪ The Link Autonomous Bandwidth Interrupt Enable bit in the Link Control register is set to 1, and ▪ The Link Autonomous Bandwidth Interrupt Status bit in the Link Status register is set to 1. The cfg_link_auto_bw_msi output is a pulse signal (only asserted for one clock cycle); but cfg_link_auto_bw_int is a level signal. For upstream port: Reserved.

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
15	R/W1C	0x0	PF0_HP_MSI The controller asserts hp_msi (as a one-cycle pulse) when the logical AND of the following conditions transitions from false to true: ▪ MSI or MSI-X is enabled. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function. The controller pulses the hp_msi output only when any of the hot plug status bits change from 0 to 1 (as is hp_pme).
14	R/W1C	0x0	PF0_HP_INT The controller asserts hp_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ Hot-Plug interrupts are enabled in the Slot Control register. ▪ Any bit in the Slot Status register is equal to 1, and the associated event notification is enabled in the Slot Control register. There is one bit of hp_int for each configured function.hp_int[0]
13	R/W1C	0x0	PF0_HP_PME The controller asserts hp_pme when all of the following conditions are true: ▪ The PME Enable bit in the Power Management Control and Status register is set to 1. ▪ Any bit in the Slot Status register transitions from 0 to 1 and the associated event notification is enabled in the Slot Control register. The controller does not check if the PM state is D1, D2, or D3hot. It is up to your application to check the value pm_dstate to make sure the device is in D1, D2, or D3hot. There is one bit of hp_pme for each configured function. The controller pulses the hp_pme output only when any hot plug status bit changes from 0 to 1 (as is hp_msi). hp_int stays asserted as long as the status bit is set. In addition, it asserts hp_pme only if PME is enabled, but it does not

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
			matter if hot-plug interrupts are enabled.
12	R/W1C	0x0	RADM_INTD_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTD Message from the downstream device.
11	R/W1C	0x0	RADM_INTC_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTC Message from the downstream device.
10	R/W1C	0x0	RADM_INTB_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTB Message from the downstream device.
9	R/W1C	0x0	RADM_INTA_DEASSERTED One-clock-cycle pulse that indicates that the controller received a Deassert_INTA Message from the downstream device.
8	R/W1C	0x0	RADM_INTD_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTD Message from the downstream device.
7	R/W1C	0x0	RADM_INTC_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTC Message from the downstream device.
6	R/W1C	0x0	RADM_INTB_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTB Message from the downstream device.
5	R/W1C	0x0	RADM_INTA_ASSERTED One-clock-cycle pulse that indicates that the controller received an Assert_INTA Message from the downstream device.
4	R/W1C	0x0	PF0_CFG_PME_MSI The controller asserts cfg_pme_msi (as a one-cycle pulse) when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1.

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
			The controller does not check if the associated MSI vector (asserted cfg_pcie_cap_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
3	R/W1C	0x0	PF0_CFG_PME_INT The controller asserts cfg_pme_int when all of the following conditions are true: ▪ The INTx Assertion Disable bit in the Command register is 0. ▪ The PME Interrupt Enable bit in the Root Control register is set to 1. ▪ The PME Status bit in the Root Status register is set to 1. The cfg_pme_msi output is a pulse signal (only asserted for one clock cycle). But cfg_pme_int is a level signal; essentially an AND of the PME interrupt enable and receipt of the pm_pme message.
2	R/W1C	0x0	PF0_CFG_AER_RC_ERR_MSI The controller asserts cfg_aer_rc_err_msi for one clock cycle when all of the following conditions are true: ▪ MSI or MSI-X is enabled. ▪ A reported error condition causes a bit to be set in the Root Error Status register. ▪ The associated error message reporting enable bit is set in the Root Error Command register. The controller does not check if the associated MSI vector (asserted cfg_aer_int_msg_num) is unmasked. It is up to the application to check whether the vector is masked or unmasked.
1	R/W1C	0x0	PF0_CFG_AER_RC_ERR_INT Asserted when a reported error condition causes a bit to be set in the Root Error Status register and the associated error message reporting enable bit is set in the Root Error Command register. cfg_aer_rc_err_int is set when the RC internally generates an error or when an error message is received by the RC. Because the RC itself generates it, this needs to be propagated up to the system software which would then need to read the error registers to see which error occurred.

Offset: 0x0E08			Register Name: SII_INT_0
Bit	Read/Write	Default/Hex	Description
			Note: This signal is used when MSI/MSI-X is NOT enabled; otherwise see cfg_aer_rc_err_msi.
0	R/W1C	0x0	PF0_CFG_VPD_INT This pin is set as a one cycle pulse to notify your application to read the VPD registers. The sequence of events for a VPD read cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '0' indicating a read request. Your application fetches four bytes of data from the VPD Address location and transfers this to the VPD Data register. ▪ Your application sets the VPD Flag bit to '1' indicating the request is complete. The sequence of events for a VPD write cycle is: ▪ The controller sends a request (single-cycle pulse of the cfg_vpd_int signal) to your application to read or write vital product data. ▪ Your application reads the VPD Control and Capabilities register. ▪ The VPD Flag (bit 31) is set to '1' indicating a write request. Your application reads the VPD Data register and transfers this to the location specified by the VPD Address register. ▪ Your application sets the VPD Flag bit to '0' indicating the request is complete.

8.12.5.35 0x0E0C PCIE SII Interrupt Register1 (Default Value: 0x0000_0000)

Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	PCIE_WAKE_N remote wake (USP)
30	R/W1C	0x0	WAKE local wake. Wake up from power management unit. The controller generates wake to request the system to restore power and clock when a wakeup event has been detected such as apps_pm_xmt_pme,

Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
			apps_pm_vf_xmt_pme, or outband_pwrup_cmd. The wake signal is an active high signal and its rising edge should be detected to drive the WAKE# the connector. Assertion of wake could be for a single clock cycle or multiple clock cycles. Not used in RC mode.
29	R/W1C	0x0	RADM_PM_TO_ACK One-clock-cycle pulse that indicates that the controller received a PME_TO_Ack message. Upstream port: Reserved.
28	R/W1C	0x0	RADM_PM_PME One-clock-cycle pulse that indicates that the controller received a PM_PME message.
27	R/W1C	0x0	RADM_FATAL_ERR One-clock-cycle pulse that indicates that the controller received an ERR_FATAL message.
26	R/W1C	0x0	RADM_NONFATAL_ERR One-clock-cycle pulse that indicates that the controller received an ERR_NONFATAL message.
25	R/W1C	0x0	RADM_CORRECTABLE_ERR One-clock-cycle pulse that indicates that the controller received an ERR_COR message. The controller makes the message header available the radm_msg_payload output.
24	R/W1C	0x0	PF0_CFG_SYS_ERR_RC System error detected. A one-clock-cycle pulse that indicates if any device in the hierarchy reports any of the following errors and the associated enable bit is set in the Root Control register: ERR_COR, ERR_FATAL, ERR_NONFATAL. Also asserted when an internal error is detected. There is one bit of cfg_sys_err_rc assigned to each configured function.
23:22	/	/	/
21	R/W1C	0x0	PF0_FRS_GRANT Indicator of when an FRS message for this function has been scheduled for transmission.
20	R/W1C	0x0	RADM_VENDOR_MSG One-cycle pulse that indicates the controller received a vendor-defined message. The controller makes the message header available the radm_msg_payload

Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
			output. When FX_TLP > 1 and when two messages of the same type are received in the same clock cycle (back-to-back), then both bits are asserted.
19	/	/	/
18	R/W1C	0x0	PF0_FRSQ_MSI FRSQ Interrupt Pulse. The RC asserts this output when it receives an FRQ message or when the FRS queue overflows.
17	R/W1C	0x0	PF0_CFG_UP_DRS_TO_FRS DRS to FRS Pulse. The PCIe controller asserts the cfg_up_drs_to_frsoutput and sends an FRS message with the reason code set to 'DRS Message Received' when: ▪ It receives a DRS message, and ▪ PCIE_CAP_DRS_SIGNALING_CONTROL in INK_CONTROL_LINK_STATUS_REG is 2'b10
16	R/W1C	0x0	PF0_CFG_DRS_MSI DRS Message Received Interrupt Pulse. The PCIe controller asserts the cfg_drs_msi output when all of the following are true: ▪ It receives a DRS message ▪ PCIE_CAP_DRS_SIGNALING_CONTROL in INK_CON_TROL_LINK_STATUS_REG is 2'b01 ▪ MSI or MSI-X is enabled
15:12	/	/	/
11	R/W1C	0x0	PCIE_PERI_AR_INT PCIe read peripherals space(0-1G) int
10	R/W1C	0x0	PCIE_PERI_AW_INT PCIe write peripherals space(0-1G) int
9	R/W1C	0x0	RADM_QOVERFLOW_1 Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism.
8	R/W1C	0x0	RADM_QOVERFLOW_0 Pulse indicating that one or more of the P/NP/CPL receive queues have overflowed. There is a 1-bit indication for each configured virtual channel. You can connect this output to your internal error reporting mechanism.

Offset: 0x0E0C			Register Name: SII_INT_1
Bit	Read/Write	Default/Hex	Description
7:5	/	/	/
4	R/W1C	0x0	RTLH_RFC_UPD Indicates that the controller received a flow control update DLLP. Used for applications that implement flow Control outside the controller.
3	R/W1C	0x0	LINK_REQ_RST_NOT Reset request because the link has gone down or the controller received a hot-reset request. A low level indicates that the controller is requesting external logic to reset the controller because the PHY link is down. When the AXI bridge module is enabled the link reset request is delayed until all pending AXI transfers have completed. When the AXI Bridge module is not enabled the link reset request is sent immediately.
2	/	/	/
1	R/W1C	0x0	RDLH_LINK_UP Data link layer up/down indicator: This status from the flow control initialization state machine indicates that flow control has been initiated and the Data link layer is ready to transmit and receive packets. For multi-VC designs, this signal indicates status for VC0 only. ▪ 1: Link is up ▪ 0: Link is down
0	R/W1C	0x0	SMLH_LINK_UP PHY Link up/down indicator: ▪ 1: Link is up ▪ 0: Link is down

8.12.5.36 0x1000 PCIE SII APP PM UNLOCK Register (Default Value: 0x0000_0000)

Offset: 0x1000			Register Name: SII_APP_PM_UNLOCK
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	APP_UNLOCK_MSG app_unlock_msg_ahb Request from your application to generate an Unlock message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse

Offset: 0x1000			Register Name: SII_APP_PM_UNLOCK
Bit	Read/Write	Default/Hex	Description
			the same signal again, until the previous message has been transmitted.
0	R/W	0x0	APP_PM_XMT_TURNOFF apps_pm_xmt_turnoff_ahb Request from your application to generate a PM_Turn_Off message. You must assert this signal for one clock cycle. The controller does not return an acknowledgment or grant signal. You must not pulse the same signal again, until the previous message has been transmitted.

8.12.5.37 0x1100 PCIE SII Power Manage Register0 (Default Value: 0x0000_0000)

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	APP_L1SUB_DISABLE The application can set this input to 1'b1 to prevent entry to L1 Sub-states. This pin is used to gate the L1 sub-state enable bits from the L1 PM Substates Control 1 Register.
11	R/W	0x0	APP_L1_PWR_OFF_EN Application permits to gate power to parts of the controller in L1 state
10	R/W	0x0	ACK_EN_VMAIN Acknowledge from power switch responsible for autonomous power-gating in L1.2. This signal is syncronized using aux_clk and can be driven/supplied asynchronously to the controller in certain low-power modes.
9	R/W	0x0	TEST_BYPASS_LP Test mode override of isolation enable
8	R/W	0x0	APP_CLK_PM_EN Clock PM feature enabled by application. Used to inhibit the programming of the Clock PM in Link Control Register.
7	R/W	0x0	CLKREQ_IN_N Status of the CLKREQ# bidirectional CMOS board-level signal. Used by the controller to determine when to enter and exit L1 Substates when using the CLKREQ#-based mechanism.

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	APP_XFER_PENDING Indicates that your application has transfers pending and prevents the controller from entering L1. This is a level signal used to inform the controller about the state of external queues and pipeline stages that contain transactions to be transmitted by the controller. The controller uses this information to determine when to enter/exit L1. When this signal is asserted, it indicates that there are transactions outside the controller that the controller needs to transmit. When de-asserted, it indicates that there are no transactions outside the controller. The controller responds to an assertion on this signal as follows: ▪ Upstream Ports: Prevents generation of requests to enter L1. Triggers exit if already in L1. ▪ Downstream Ports: Triggers exit if already in L1. You can instruct the controller to exit L1 by asserting either or both of app_xfer_pending and app_req_exit_l1. The controller only samples app_req_exit_l1 when the controller is already in the L1 state.
5	R/W	0x0	APP_REQ_EXIT_L1 Application request to Exit L1. Request from your application to exit L1. It is only effective when L1 is enabled.
4	R/W	0x0	APP_READY_ENTR_L23 Application Ready to Enter L23. Indication from your application that it is ready to enter the L23 state. The app_ready_entr_l23 signal is provided for applications that must control L23 entry (in case certain tasks must be performed before going into L23). The controller delays sending PM_Enter_L23 (in response to PM_Turn_Off) until this signal becomes active. When this signal has been asserted by the application, it must be kept asserted until L2 entry has completed. Hardwire to 1 for applications that do not require this feature. **Note: The controller ignores this input in RC mode.**
3	R/W	0x0	APP_REQ_ENTR_L1_AHB Application request to Enter L1 ASPM state. The

Offset: 0x1100			Register Name: SII_APP_PM_0
Bit	Read/Write	Default/Hex	Description
			app_req_entr_l1 signal is for use by applications that need to control L1 entry instead of using the L1 entry timer as defined in the PCI Express Specification. It is only effective when L1 is enabled. The controller latches this request when in L0 or L0s; to be acted upon later. Note: The controller ignores this input in RC mode.
2	R/W	0x0	SYS_AUX_PWR_DET Auxiliary Power Detected. Used to report to the host software that auxiliary power (Vaux) is present.
1:0	/	/	/

8.13 Two Wire Interface (TWI)

8.13.1 Overview

The Two Wire Interface (TWI) provides an interface between a CPU and any TWI-bus-compatible device that connects via the TWI bus. The TWI is designed to be compatible with the standard I2C bus protocol. The communication of the TWI is carried out by a byte-wise mode based on interrupt polled handshaking. Each device on the TWI bus is recognized by a unique address and can operate as either transmitter or receiver, a device connected to the TWI bus can be considered as master or slave when performing data transfers. Note that a master device is a device that initiates a data transfer on the bus and generates the clock signals to permit the transfer. During this transfer, any device addressed by this master is considered a slave.

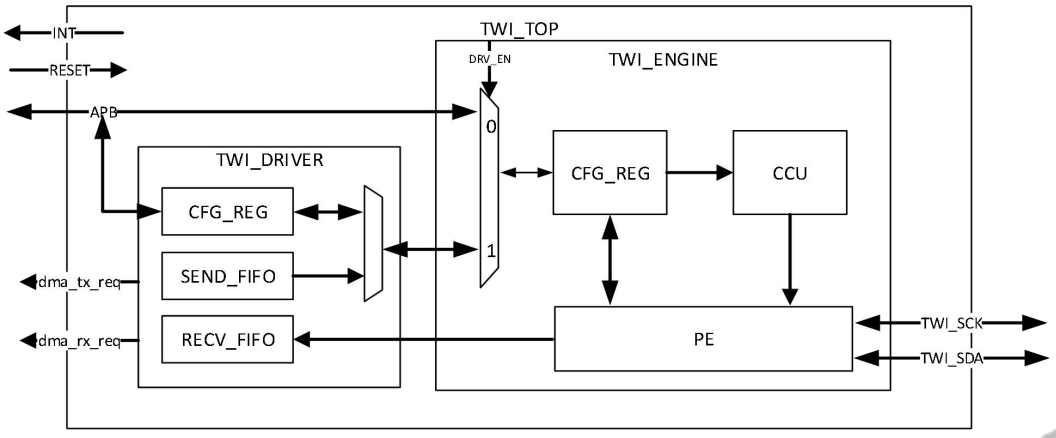
The TWI has the following features:

- Up to 9 TWI controllers
  - 6 TWI controllers in CPUX domain: TWI0, TWI1, TWI2, TWI3, TWI4, and TWI5
  - 3 TWI controllers in CPUS domain: S_TWI0, S_TWI1, and S_TWI2
- Compliant with I2C bus standard
- 7-bit and 10-bit device addressing modes
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports general call and start byte
- Master mode supports the following:
  - Bus arbitration in the case of multiple master devices
  - Clock synchronization and bit and byte waiting
  - Packet transmission and DMA
- Slave mode supports Interrupt on address detection

8.13.2 Block Diagram

the following figure shows the block diagram of TWI.

Figure 8-46 TWI Block Diagram



TWI contains the following sub-blocks:

Table 8-35 TWI Sub-blocks

Sub-block	Description
RESET	Module reset signal
INT	Module output interrupt signal
CFG_REG	Module configuration register in TWI
PE	Packet encoding/decoding
CCU	Module clock controller unit
SEND_FIFO	The register address bytes and the written data bytes are buffered in SEND_FIFO
RECV_FIFO	The read data bytes are buffered in RECV_FIFO

The controller includes TWI engine and TWI driver. Each time the TWI engine sends a START signal, a STOP signal, or a BYTE data, or a corresponding ACK, the TWI engine will generate an interrupt, and wait for the CPU to process and clear the interrupt before the next START, STOP, or BYTE, ACK transmission can be performed. Therefore, when a device communication is completed, many interrupts will be generated, and the CPU needs to wait for the previous interrupt before it can configure the next one. The TWI driver defines each communication with the device as a packet transmission. The CPU can directly configure the slave address, register address and data transmission for one or more package transmissions without waiting for interruption, then start the TWI driver, and the TWI driver can control the TWI engine to complete a pre-configured communication, and report an interrupt to the CPU after completion.

8.13.3 Functional Description

8.13.3.1 External Signals

The following table describes the external signals of the TWI. The TWIn-SCK and TWIn-SDA are bidirectional I/O, when the TWI is configured as a master device, the TWIn-SCK is an output pin; when the TWI is configurable as a slave device, the TWIn-SCK is an input pin. When using TWI, the corresponding PADs are selected as TWI function via section 8.5 GPIO.

Table 8-36 TWI External Signals

Signal Name	Description	Type
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O
TWI4-SCK	TWI4 Serial Clock Signal	I/O
TWI4-SDA	TWI4 Serial Data Signal	I/O
TWI5-SCK	TWI5 Serial Clock Signal	I/O
TWI5-SDA	TWI5 Serial Data Signal	I/O
S-TWI0-SCK	S-TWI0 Serial Clock Signal	I/O
S-TWI0-SDA	S-TWI0 Serial Data Signal	I/O
S-TWI1-SCK	S-TWI1 Serial Clock Signal	I/O
S-TWI1-SDA	S-TWI1 Serial Data Signal	I/O
S-TWI2-SCK	S-TWI1 Serial Clock Signal	I/O
S-TWI2-SDA	S-TWI1 Serial Data Signal	I/O

8.13.3.2 Clock Sources

Each TWI controller has an input clock source. The following table describes the clock sources for TWI. After selecting a proper clock, users must open the gating of TWI and release the corresponding reset bit.

For more details on the clock setting, configuration, and gating information, see section 2.5 Clock Controller Unit (CCU) and section 2.11 Power Reset Clock Management (PRCM).

Table 8-37 TWI Clock Sources

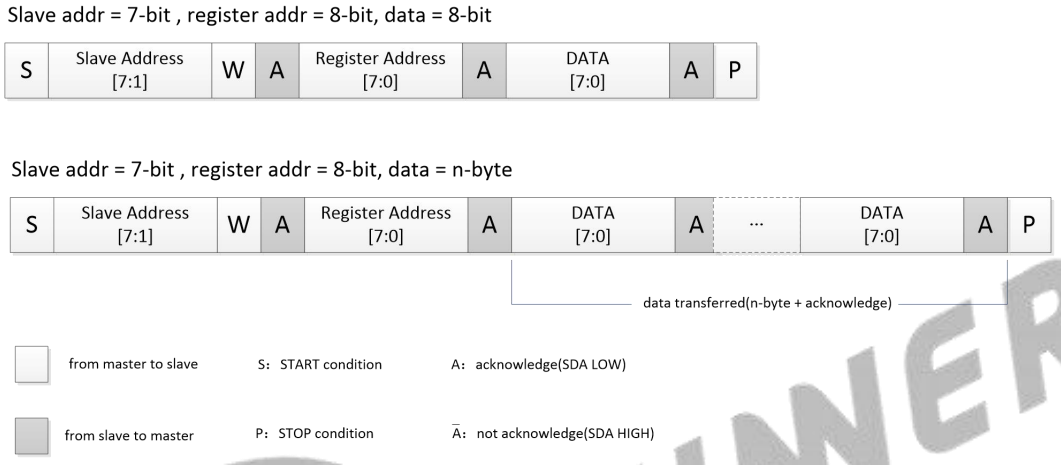
Clock Sources	Descsription	Module
APB1 Bus	TWI clock source. Refer to CCU for details on APB1.	CCU
APBS1 Bus	S_TWI clock source. Refer to PRCM for details on APBS1.	PRCM

8.13.3.3 Write/Read Timing in Standard and Extended Addressing Mode

This section is the 7-bit/10-bit addressing mode of the entire TWI protocol to read and write device registers. It can be achieved by directly using the TWI engine or using the TWI driver to control the TWI engine.

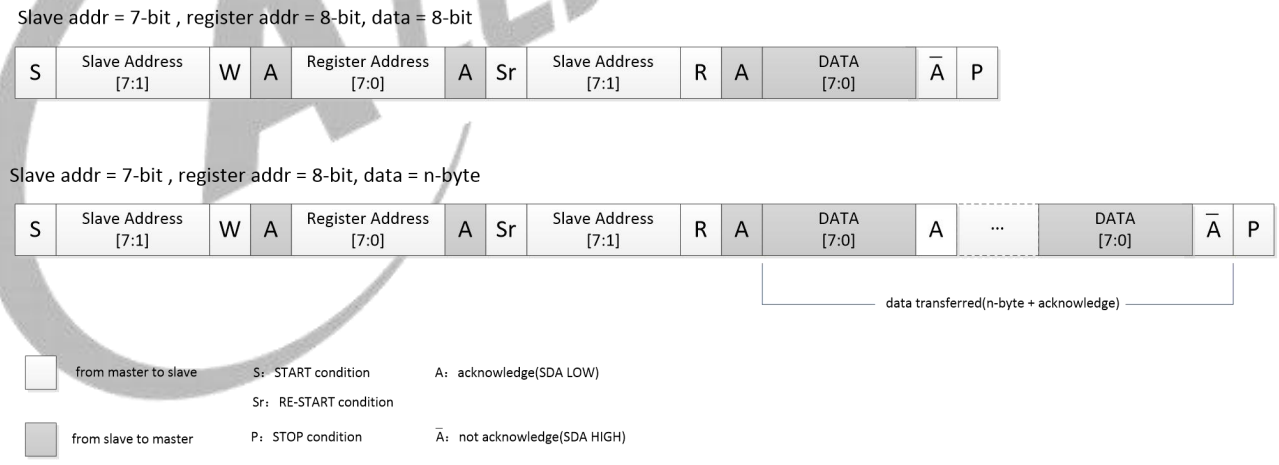
The following figure describes the write timing in 7-bit standard addressing mode.

Figure 8-47 Write Timing in 7-bit Standard Addressing Mode



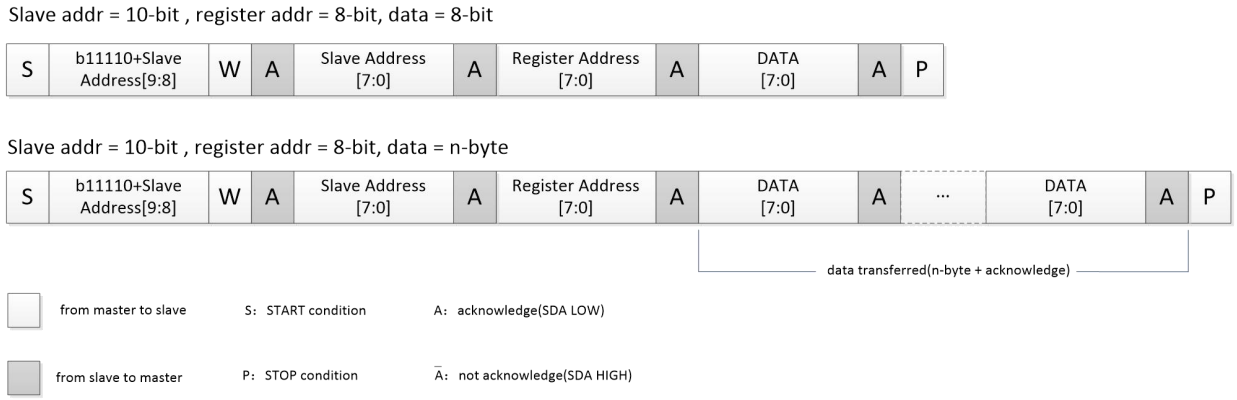
The following figure describes the read timing in 7-bit standard address mode.

Figure 8-48 Read Timing in 7-bit Standard Addressing Mode



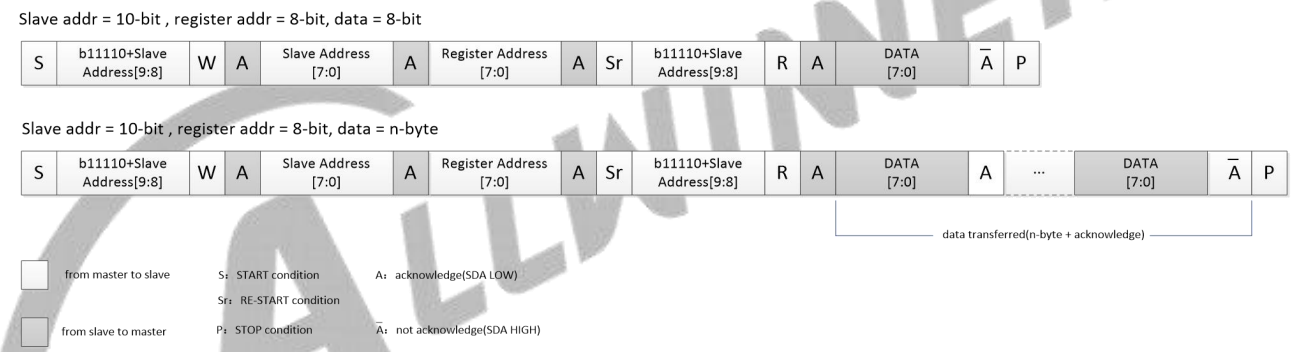
The following figure describes the write timing in 10-bit extended address mode.

Figure 8-49 Write Timing in 10-bit Extended Addressing Mode



The following figure describes the read timing in 10-bit extended address mode.

Figure 8-50 Read Timing in 10-bit Extended Addressing Mode



8.13.3.4 Write/Read Packet Transmission of TWI Driver

The TWI driver is only supported for master mode. When the TWI works in master mode, the TWI driver drives the TWI engine for one or more packet transmission instead of the CPU host. Packet transmission is defined in the following figures. The register address bytes and the written data bytes are buffered in SEND_FIFO, the read data bytes are buffered in RECV_FIFO.

Figure 8-51 TWI Driver Write Packet Transmission

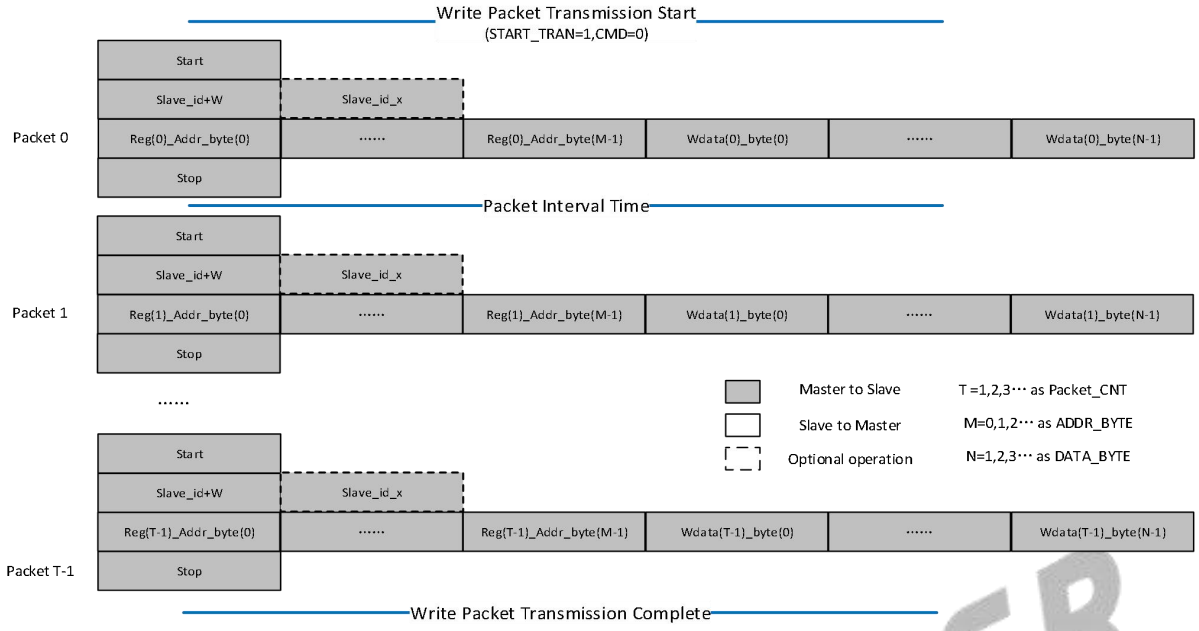
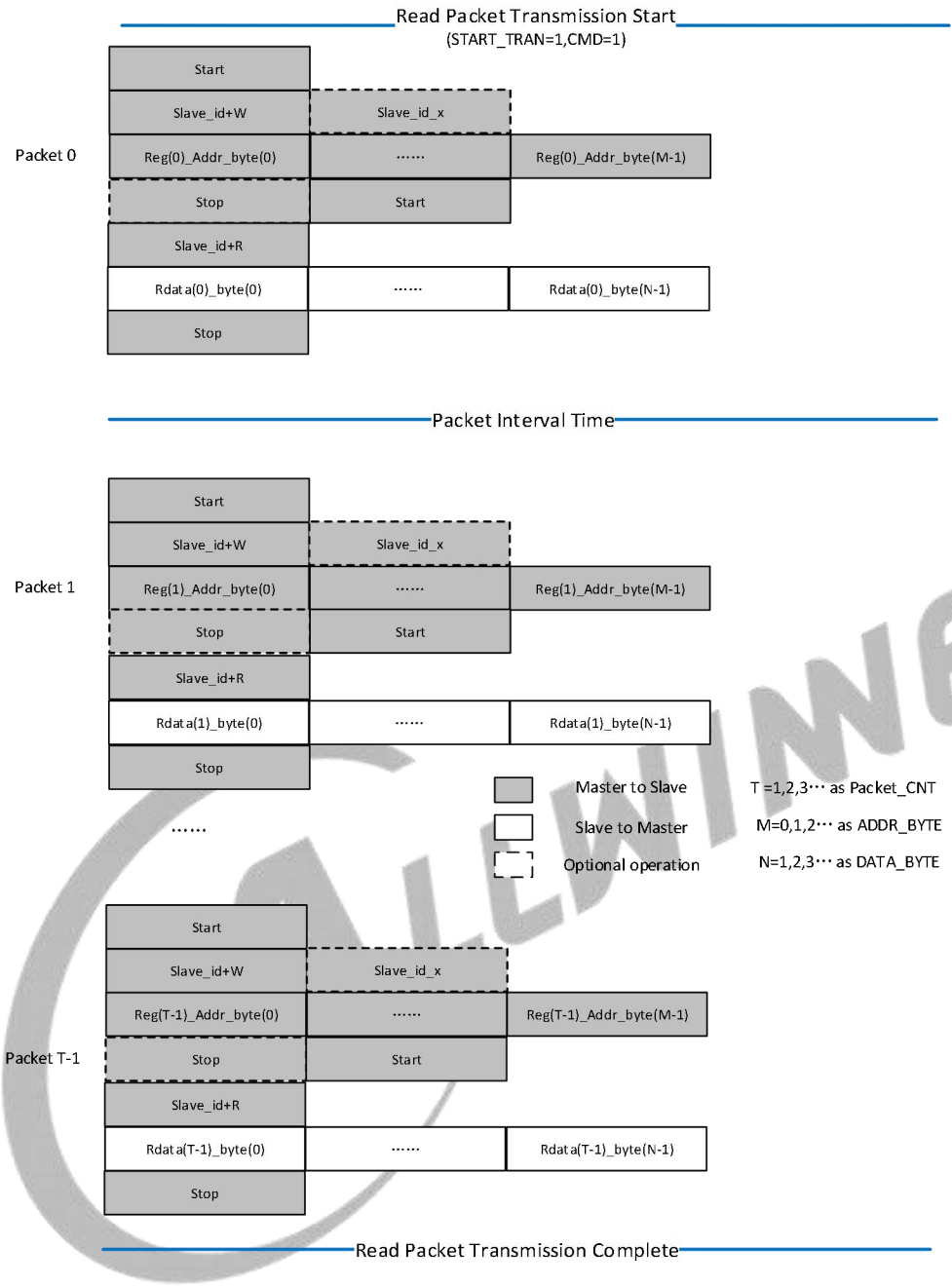


Figure 8-52 TWI Driver Read Packet Transmission



8.13.3.5 Master and Slave Mode of TWI Engine

In Master mode, the CPU host controls the TWI engine by writing command and data to its registers. The TWI engine transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP command is detected. The CPU host can poll the status register if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting TWI_CNTR[M_STA] to high. The TWI engine will assert the INT line and TWI_CNTR[INT_FLAG] to indicate a completion for the START command and each consequent byte transfer. At each interrupt, the CPU host needs to check the current state by the TWI_STAT

register. A transfer must conclude with the STOP command by setting TWI_CNTR[M_STP] to high.

In Slave mode, the TWI engine also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed, and the TWI engine interrupts the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write the TWI_DATA register, and set the TWI_CNTR register. After each byte transfer, a slave device always stops the operation of the remote master by holding the next low pulse on the SCL line until the CPU host responds to the status of the previous byte transfer or START command.

8.13.3.6 Generation of Repeated Start

After the data transfer, if the master still requires the bus, it can signal another Start followed by another slave address without signaling a Stop.

8.13.3.7 Programming State Diagram

Figure 8-53 shows the TWI programming state diagram. For the value between two states, see the TWI_STAT register in section 8.13.6.5.

M_SEND_S: master sends START signal;

M_SEND_ADDR: master sends slave address;

M_SEND_XADD: master sends slave extended address;

M_SEND_SR: master repeated start;

M_SEND_DATA: master sends data;

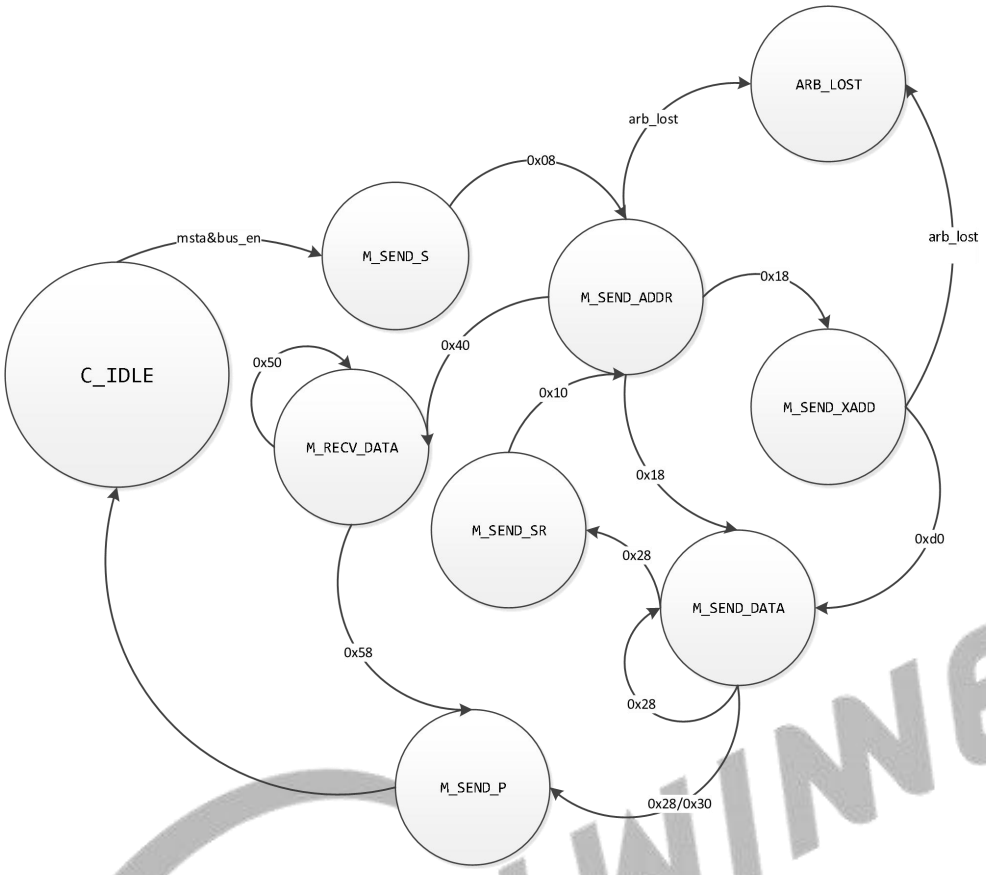
M_SEND_P: master sends STOP signal;

M_RECV_DATA: master receives data;

ARB_LOST: Arbitration lost;

C_IDLE: Idle.

Figure 8-53 TWI Programming State Diagram



8.13.4 Programming Guidelines

The TWI controller operates in an 8-bit data format. The data on the TWI_SDA line is always 8 bits long. At first, the TWI controller sends a start condition. When in the addressing formats of 7-bit, the TWI sends out an 8-bit message which includes 7 MSB slave address and 1 LSB read/write flag. The least significant of the salve address indicates the direction of transmission. When the TWI works in 10-bit slave address mode, the operation will be divided into two steps, for details on the operation, refer to register description in Section 8.13.6.1 and 8.13.6.2.

The following takes the TWI module in the CPUX domain as an example.

8.13.4.1 Initialization for TWI Engine

To initialize the TWI engine, perform the following steps:

Step 1 Configure corresponding GPIO multiplex function as TWI mode.

Step 2 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 0 to close TWIn clock.

Step 3 For TWIn, set TWI_BGR_REG[TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.

Step 4 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 1 to open TWIn clock.

Step 5 Configure TWI_CCR[CLK_M] and TWI_CCR[CLK_N] to get the needed rate (The clock source of TWI is from APB1).

Step 6 Configure TWI_CNTR[BUS_EN] and TWI_CNTR[A_ACK], when using interrupt mode, set TWI_CNTR[INT_EN] to 1, and register the system interrupt through GIC module. In slave mode, configure TWI_ADDR and TWI_XADDR registers to finish TWI initialization configuration.

8.13.4.2 Writing Data Operation for TWI Engine

To write data to the device, perform the following steps:

Step 1 Clear TWI_EFR register, and configure TWI_CNTR[M_STA] to 1 to transmit the START signal.

Step 2 After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step 3 The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).

Step 4 Interrupt is triggered after data address transmission completes, write data to be transmitted to TWI_DATA (For consecutive write data operation, every byte transmission completion triggers interrupt, during interrupt write the next byte data to TWI_DATA).

Step 5 After transmission completes, write TWI_CNTR[M_STP] to 1 to transmit the STOP signal and end this write-operation.

8.13.4.3 Reading Data Operation for TWI Engine

To read data from the device, perform the following steps:

Step 1 Clear TWI_EFR register, and set TWI_CNTR[A_ACK] to 1, and configure TWI_CNTR[M_STA] to 1 to transmit the START signal.

Step 2 After the START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA (For a 10-bit device ID, firstly write the first-byte ID, secondly write the second-byte ID in the next interrupt).

Step 3 The Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA (For a 16-bit address, firstly write the first-byte address, secondly write the second-byte address).

Step 4 The Interrupt is triggered after data address transmission completes, write TWI_CNTR[M_STA] to 1 to transmit new START signal, and after interrupt triggers, write device ID to TWI_DATA to start read-operation.

Step 5 After device address transmission completes, each receive completion will trigger an interrupt, in turn, read TWI_DATA to get data, when receiving the previous interrupt of the last byte data, clear [A_ACK] to stop acknowledge signal of the last byte.

Step 6 Write TWI_CNTR[M_STP] to 1 to transmit the STOP signal and end this read-operation.

8.13.4.4 Initialization for TWI Driver

To initialize the TWI driver, perform the following steps:

Step 1 Configure corresponding GPIO multiplex function as TWI mode.

Step 2 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 0 to close TWIn clock.

Step 3 For TWIn, set TWI_BGR_REG[TWIn_RST] in CCU module to 0, then set to 1 to reset TWIn.

Step 4 For TWIn, set TWI_BGR_REG[TWIn_GATING] in CCU module to 1 to open TWIn clock.

Step 5 Set TWI_DRV_CTRL[TWI_DRV_EN] to 1 to enable the TWI driver.

Step 6 Configure TWI_DRV_BUS_CTRL[CLK_M] and TWI_DRV_BUS_CTRL[CLK_N] to get the needed rate (The clock source of TWI is from APB1).

Step 7 Set TWI_DRV_CTRL[RESTART_MODE] to 0 and [READ_TRAN_MODE] to 1, set TWI_DRV_INT_CTRL[TRAN_COM_INT_EN] to 1.

Step 8 When using DMA for data transmission, set TWI_DRV_DMA_CFG[DMA_RX_EN] and TWI_DRV_DMA_CFG[DMA_TX_EN] to 1, and configure TWI_DRV_DMA_CFG[RX_TRIG] and TWI_DRV_DMA_CFG[TX_TRIG] to set the thresholds of RXFIFO and TXFIFO.

8.13.4.5 Writing Packet Transmission for TWI Driver

To write package to the device, perform the following steps:

Step 1 Configure TWI_DRV_SLV[SLV_ID] to set the device ID, and configure TWI_DRV_SLV[CMD] to 0 to set the write operation.

Step 2 Configure TWI_DRV_FMT[ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT[DATA_BYTE] according to the written data count in a packet.

Step 3 Configure TWI_DRV_CFG[PACKET_CNT] to set the written packet number.

Step 4 Configure DMA channel, including TWI TXFIFO, device register address, and the written data.

Step 5 Set [START_TRAN] to 1 to start TWI Driver transmission.

Step 6 When TWI driver transmission completes, the interrupt is triggered, it indicates that the write packet transmission ends.

8.13.4.6 Reading Packet Transmission for TWI Driver

Step 1 To read package from the device, perform the following steps:

Step 2 Configure TWI_DRV_SLV[SLV_ID] to set the device ID, and configure TWI_DRV_SLV[CMD] to 1 to set the read operation.

Step 3 Configure TWI_DRV_FMT[ADDR_BYTE] according to the address width of the device register, and TWI_DRV_FMT[DATA_BYTE] according to the read data count in a packet.

Step 4 Configure TWI_DRV_CFG[PACKET_CNT] to set the read packet number.

Step 5 Configure DMA channel, including TWI TXFIFO, TWI RXFIFO, device register address and the read data.

Step 6 Set [START_TRAN] to 1 to start TWI Driver transmission.

Step 7 When TWI driver transmission completes, the interrupt is triggered, it indicates that the read packet transmission ends.

8.13.5 Register List

Module Name	Base Address	Comments
TWI0	0x0250 2000	
TWI1	0x0250 2400	TWI1 register is the same with TWI0.
TWI2	0x0250 2800	TWI2 register is the same with TWI0.
TWI3	0x0250 2C00	TWI3 register is the same with TWI0.
TWI4	0x0250 3000	TWI4 register is the same with TWI0.
TWI5	0x0250 3400	TWI5 register is the same with TWI0.
S_TWI0	0x0708 1400	R-TWI0 register is the same with TWI0.
S_TWI1	0x0708 1800	R-TWI1 register is the same with TWI0.
S_TWI2	0x0708 1C00	R-TWI2 register is the same with TWI0.

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address Register
TWI_XADDR	0x0004	TWI Extended Slave Address Register
TWI_DATA	0x0008	TWI Data Byte Register
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset Register
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register

Register Name	Offset	Description
TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register
TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

8.13.6 Register Description

8.13.6.1 0x0000 TWI Slave Address Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address For 7-bit addressing, the bit[7:1] indicates: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 For 10-bit addressing, the bit[7:1] indicates: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with b'11110, the TWI recognizes b'11110 as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (For example, SLAX9 and SLAX8 for the extended address of the device), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

8.13.6.2 0x0004 TWI Extend Address Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

8.13.6.3 0x0008 TWI Data Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

8.13.6.4 0x000C TWI Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
			1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus SDA/SCL is ignored and the TWI controller will not respond to any address on the bus. 1: The TWI will respond to call to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Note: In master operation mode, this bit should be set to '1'.
5	R/WAC	0x0	M_STA Master Mode Start When the M_STA is set to '1', the TWI controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.
4	R/W1C	0x0	M_STP Master Mode Stop If the M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode), then transmit the START condition. The M_STP bit is cleared automatically. Writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag The INT_FLAG is automatically set to '1' when any of the 28 (out of the possible 29) states is entered (see

Offset: 0x000C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
			'STAT Register' below). The state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when INT_FLAG is set to '1'. If the TWI is operating in slave mode, the data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the GCE bit in the ADDR register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1	/	/	/
0	R/W	0x0	CLK_COUNT_MODE 0: scl clock high period count on oscl 1: scl clock high period count on iscl

8.13.6.5 0x0010 TWI Status Register (Default Value: 0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0xF8	STA

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
			Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in the address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in the address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in the address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK

Offset: 0x0010			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
			received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: The Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

8.13.6.6 0x0014 TWI Clock Register (Default Value: 0x0000_0080)

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit [7] takes effect 1: 30%
7	R/W	0x1	CLK_DUTY Setting duty cycle of clock as master 0: 50% 1: 40%
6:3	R/W	0x0	CLK_M The TWI SCL output frequency, in master mode, is F1/10: F1 = F0/(CLK_M + 1) Fscl = F1/10 = Fin/(2^CLK_N * (CLK_M + 1)*10) Specially, Fscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin/2^CLK_N The TWI SCL output frequency, in master mode, is F1/10: F1 = F0/(CLK_M + 1) Fscl = F1/10 = Fin/(2^CLK_N * (CLK_M + 1)*10)

Offset: 0x0014			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
			Specially, Fscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce. For Example: Fin = 24 MHz (APB clock input) For 400 kHz full speed 2-wire, CLK_N = 1, CLK_M = 2 F0 = 24 MHz/2^1 = 12 MHz, F1 = F0/(10*(2+1)) = 0.4 MHz For 100 kHz standard speed 2-wire, CLK_N = 1, CLK_M = 11 F0 = 24 MHz/2^1 = 12 MHz, F1 = F0/(10*(11+1)) = 0.1 MHz

8.13.6.7 0x0018 TWI Soft Reset Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation.

8.13.6.8 0x001C TWI Enhance Feature Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00: No data byte can be written after the read command 01: Only 1-byte data can be written after the read command 10: 2-bytes data can be written after the read command 11: 3-bytes data can be written after the read command

8.13.6.9 0x0020 TWI Line Control Register (Default Value: 0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When the line control mode is enabled (bit[2] is set), this bit decides the output level of TWI_SCL. 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When the line control mode is enabled (bit[0] is set), this bit decides the output level of TWI_SDA. 0: Output low level 1: Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

8.13.6.10 0x0200 TWI_DRV Control Register (Default Value: 0x00F8_1000)

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	START_TRAN

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
			Start transmission 0: Transmission idle 1: Start transmission Automatically cleared to '0' when finished. If the slave is not responding for the expected status over the time defined by TIMEOUT, the current transmission will stop. All setting formats and data will be loaded from registers and FIFO when the transmission starts.
30	/	/	/
29	R/W	0x0	RESTART_MODE Restart mode 0: RESTART 1: STOP+START Define the TWI_DRV action after sending the register address.
28	R/W	0x0	READ_TRAN_MODE Read transition mode 0: Send slave_id+W 1: Not send slave_id+W Setting this bit to 1 if reading from a slave in which the register width is equal to 0.
27:24	R	0x0	TRAN_RESULT Transition result 000: OK 001: FAIL Other: Reserved
23:16	R	0xf8	TWI_STA TWI status 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not

Offset: 0x0200			Register Name: TWI_DRV_CTRL
Bit	Read/Write	Default/Hex	Description
			received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending the 9th SCL clock Other: Reserved
15:8	R/W	0x10	TIMEOUT_N Timeout number When sending the 9th clock, assert fail signal when the slave device does not respond after N*F_{SCL} cycles. And the software must do a reset to the TWI_DRV module and send a stop condition to slave.
7:2	/	/	/
1	R/W	0x0	SOFT_RESET Software reset 0: Normal 1: Reset
0	R/W	0x0	TWI_DRV_EN TWI driver enable 0: Module disable 1: Module enable (only use in TWI Master Mode)

8.13.6.11 0x0204 TWI_DRV Transmission Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0204			Register Name: TWI_DRV_CFG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL F_{SCL} cycles.
15:0	R/W	0x1	PACKET_CNT The FIFO data is transmitted as PACKET_CNT packets in current format.

8.13.6.12 0x0208 TWI_DRV Slave ID Register (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:9	R/W	0x0	SLV_ID

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	Read/Write	Default/Hex	Description
			Slave device ID For 7-bit addressing, the bit[7:1] indicates: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 For 10-bit addressing, the bit[7:1] indicates: 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD R/W operation to slave device 0: Write 1: Read
7:0	R/W	0x0	SLV_ID_X SLAX[7:0] The low 8 bits for slave device ID with 10-bit addressing.

8.13.6.13 0x020C TWI_DRV Packet Format Register (Default Value: 0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE How many bytes be sent as slave device reg address 0-255
15:0	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1-65535

8.13.6.14 0x0210 TWI_DRV Bus Control Register (Default Value: 0x0000_80C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	CLK_DUTY_30_EN Enabling duty cycle 30% of Clock as Master 0: bit [15] takes effect 1: 30%
16	W	0x0	CLK_COUNT_MODE Clock count mode 0: scl clock high period count on oscl 1: scl clock high period count on iscl
15	R/W	0x1	CLK_DUTY

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	Read/Write	Default/Hex	Description
			Setting duty cycle of clock as Master 0: 50% 1: 40%
14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10 Specially, Foscl = F1/11 when CLK_M=0 and CLK_DUTY=40% due to the delay of SCL sample debounce.
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output enable
0	R/W	0x0	SDA_MOE SDA manual output enable

8.13.6.15 0x0214 TWI_DRV Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
19	R/W	0x0	RX_REQ_INT_EN If set, an interrupt is sent when RX_REQ_PD sets.
18	R/W	0x0	TX_REQ_INT_EN If set, an interrupt is sent when TX_REQ_PD sets.
17	R/W	0x0	TRAN_ERR_INT_EN If set, an interrupt is sent when TRAN_ERR_PD sets.
16	R/W	0x0	TRAN_COM_INT_EN If set, an interrupt is sent when TRAN_COM_PD sets.
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD

Offset: 0x0214			Register Name: TWI_DRV_INT_CTRL
Bit	Read/Write	Default/Hex	Description
			Set when the data byte number in RECV_FIFO reaches RX_TRIG.
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO.
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failure pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completion pending

8.13.6.16 0x0218 TWI_DRV DMA Configure Register (Default Value: 0x0010_0010)

Offset: 0x0218			Register Name: TWI_DRV_DMA_CFG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	DMA_RX_EN DMA RX Enable
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG RX trigger When DMA_RX_EN is set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG, or the read transmission is completed, the data of RECV_FIFO does not reach RX_TRIG but as long as the RECV_FIFO is not empty.
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN DMA TX Enable
7:6	/	/	/
5:0	R/W	0x10	TX_TRIG TX trigger When DMA_TX_EN is set, send DMA TX Req when the space of SEND_FIFO (FIFO Level – data volume) reaches TX_TRIG.

8.13.6.17 0x021C TWI_DRV FIFO Content Register (Default Value: 0x0000_0000)

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/

Offset: 0x021C			Register Name: TWI_DRV_FIFO_CON
Bit	Read/Write	Default/Hex	Description
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV_FIFO pointer, and this bit is cleared automatically.
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV_FIFO
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer, and this bit is cleared automatically.
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

8.13.6.18 0x0300 TWI_DRV Send Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TWI_DRV_SEND_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Address of a 32x8 SEND_FIFO, which stores reg address and data sending to the slave device.

8.13.6.19 0x0304 TWI_DRV Receive Data FIFO Access Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: TWI_DRV_RECV_FIFO_ACC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RECV_DATA_FIFO Address of a 32x8 RECV_FIFO, which stores data received from the slave device.

8.14 PWM

8.14.1 Overview

The Pulse Width Modulation (PWM) module can output the configurable PWM waveforms and measure the external input waveforms.

The PWM has the following features:

- Up to 30 PWM channels and 4 PWM controllers: PWM [19:0] in CPUX domain, S-PWM [9:0] in CPUS domain
  - PWM [15:0] for PWMCTRL0 controller
  - PWM [19:16] for PWMCTRL1 controller
  - S-PWM [1:0] for S_PWMCTRL controller
  - S-PWM [9:2] for MCU_PWMCTRL controller
- Maximum 16 independent PWM channels for PWM controller
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz (when the clock source is DCXO24M)
    - 0 to 100 MHz (when the clock source is APB1 clock)
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Maximum 8 complementary pairs output
  - The pairing methods for each controller are as follows. The components are internal PWM channels:
    - Maximum 8 pairs for PWMCTRL0:

      PWM0 + PWM1, PWM2 + PWM3, PWM4 + PWM5, PWM6 + PWM7, PWM8 + PWM9, PWM10 + PWM11, PWM12 + PWM13, PWM14 + PWM15
    - Maximum 2 pairs for PWMCTRL1:

      PWM0+PWM1, PWM2+PWM3
    - Maximum 1 pair for S_PWMCTRL:

      PWM0+PWM1
    - Maximum 4 pairs for MCU_PWMCTRL:

      PWM0+PWM1, PWM2+PWM3, PWM4+PWM5, PWM6+PWM7
  - Supports dead-zone generator, and the dead-zone time is configurable

- Maximum 4 group of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Maximum 16 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

The basic features for four PWM controllers are as follows:

PWM controller	Domain	Channels	Pairs
PWMCTRL0	CPUX	16	8 PWM pairs PWM01 (PWM0+PWM1) PWM23 (PWM2+PWM3) PWM45 (PWM4+PWM5) PWM67 (PWM6+PWM7) PWM89 (PWM8+PWM9) PWMab (PWM10+PWM11) PWMcd (PWM12+PWM13) PWMef (PWM14+PWM15)
PWMCTRL1	CPUX	4	2 PWM pairs PWM01 (PWM0+PWM1) PWM23 (PWM2+PWM3)
S_PWMCTRL	CPUS	2	1 PWM pair PWM01 (PWM0+PWM1)
MCU_PWMCTRL	CPUS	8	4 PWM pair PWM01 (PWM0+PWM1) PWM23 (PWM2+PWM3) PWM45 (PWM4+PWM5) PWM67 (PWM6+PWM7)

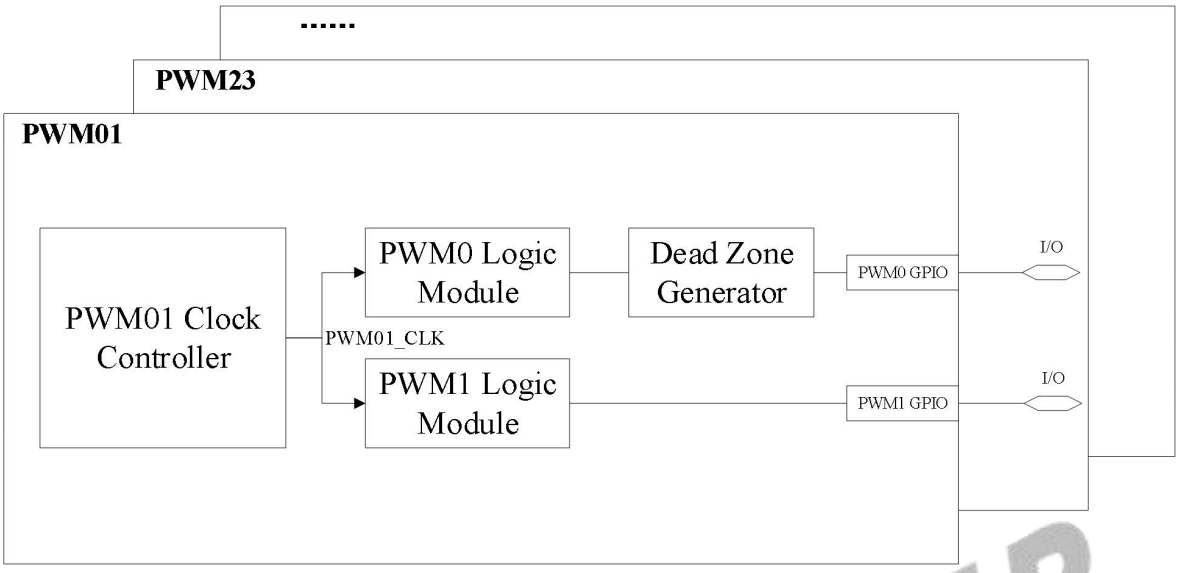
NOTE

For the corresponding relationship between the channels of each PWM controller and the external signals, please refer to section 8.14.3.1 External Signals.

8.14.2 Block Diagram

The PWM includes multi PWM channels. Each channel can generate different PWM waveform by the independent counter and duty-ratio configuration register. Each PWM pair shares one group of clock and dead-zone generator to generate PWM waveform.

Figure 8-54 PWM Block Diagram



Each PWM pair consists of 1 clock module, 2 timer logic module, and 1 programmable dead-zone generator.

8.14.3 Functional Description

8.14.3.1 External Signals

The following table describes the external signals of the PWM.

Table 8-38 PWM External Signals

Signal	Description	Type
PWMCTRL0		
PWM0	PWM channel0 in PWMCTRL0	I/O
PWM1	PWM channel1 in PWMCTRL0	I/O
PWM2	PWM channel2 in PWMCTRL0	I/O
PWM3	PWM channel3 in PWMCTRL0	I/O
PWM4	PWM channel4 in PWMCTRL0	I/O
PWM5	PWM channel5 in PWMCTRL0	I/O
PWM6	PWM channel6 in PWMCTRL0	I/O
PWM7	PWM channel7 in PWMCTRL0	I/O
PWM8	PWM channel8 in PWMCTRL0	I/O
PWM9	PWM channel9 in PWMCTRL0	I/O
PWM10	PWM channel10 in PWMCTRL0	I/O
PWM11	PWM channel11 in PWMCTRL0	I/O
PWM12	PWM channel12 in PWMCTRL0	I/O
PWM13	PWM channel13 in PWMCTRL0	I/O

Signal	Description	Type
PWM14	PWM channel14 in PWMCTRL0	I/O
PWM15	PWM channel15 in PWMCTRL0	I/O
PWMCTRL1		
PWM16	PWM channel0 in PWMCTRL1	I/O
PWM17	PWM channel1 in PWMCTRL1	I/O
PWM18	PWM channel2 in PWMCTRL1	I/O
PWM19	PWM channel3 in PWMCTRL1	I/O
S_PWMCTRL		
S-PWM0	PWM channel0 in S_PWMCTRL	I/O
S-PWM1	PWM channel1 in S_PWMCTRL	I/O
MCU_PWMCTRL		
S-PWM2	PWM channel0 in MCU_PWMCTRL	I/O
S-PWM3	PWM channel1 in MCU_PWMCTRL	I/O
S-PWM4	PWM channel2 in MCU_PWMCTRL	I/O
S-PWM5	PWM channel3 in MCU_PWMCTRL	I/O
S-PWM6	PWM channel4 in MCU_PWMCTRL	I/O
S-PWM7	PWM channel5 in MCU_PWMCTRL	I/O
S-PWM8	PWM channel6 in MCU_PWMCTRL	I/O

8.14.3.2 Clock Sources

The following table describes the clock sources of the PWM controllers.

Table 8-39 PWM clock sources

PWM	Clock Sources	Description	Module
PWMCTRL0 PWMCTRL1	HOSC	24 MHz, external clock.	CCU
	APB1_CLK	24 MHz, PWM bus clock.	
S_PWMCTRL MCU_PWMCTRL	CLK24M	By default, CLK24M is 24 MHz.	PRCM
	CLK32K	By default, CLK32K is 32 kHz.	
	CLK_RC	By default, CLK_RC is 16 MHz.	

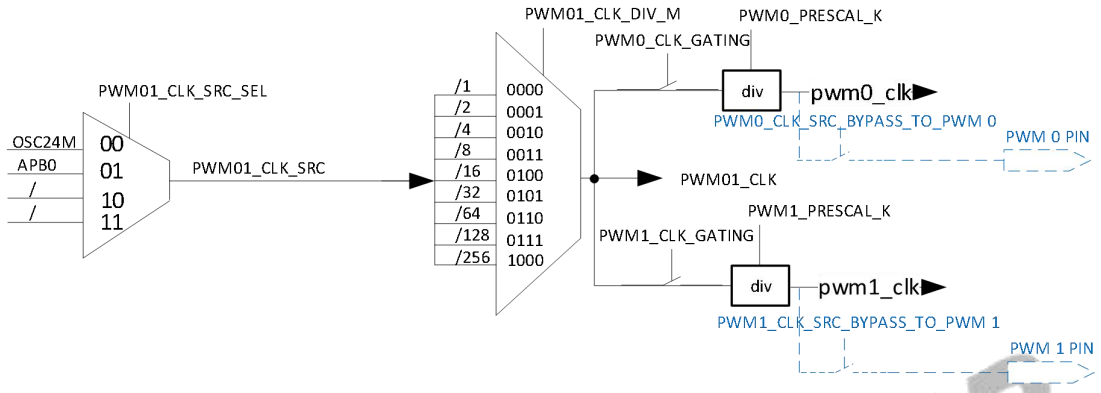
8.14.3.3 Typical Application

- Suitable for display device, such as LCD
- Suitable for electric motor control

8.14.3.4 Clock Controller

Using PWM01 as an example. The other PWM pairs are the same as PWM01.

Figure 8-55 PWM01 Clock Controller Diagram



The clock controller of each PWM pair includes clock source select (PWM01_CLK_SRC), 1-256 scaler (PWM01_CLK_DIV_M). Each PWM channel has the secondary frequency division (PWM_PRESCAL_K), clock source bypass (PWMx_CLK_BYPASS) and clock switch (PWMx_CLK_GATING).

The clock sources have HOSC and APB0. The HOSC comes from the external high-frequency oscillator; the APB0 is APB0 bus clock.

The bypass function of the clock source is that the clock source directly accesses PWM output, the PWM output waveform is the waveform of the clock controller output. The BYPASS gridlines in the above figure indicate the bypass function of the clock source, see Figure 8-56 for the details about implement. At last, the output clock of the clock controller is sent to the PWM logic module.

8.14.3.5 PWM Output

Taking PWM01 as an example, Figure 8-56 indicates the PWM01 output logic diagram. The logic diagrams of other PWM pairs are the same as PWM01.

The timer logic module of PWM consists of one 16-bit up-counter (PCNTR) and three 16-bit parameters (PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE, PWM_COUNTER_START). The PWM_ENTIRE_CYCLE is used to control the PWM cycle, the PWM_ACT_CYCLE is used to control the duty-cycle, the PWM_COUNTER_START is used to control the output phase (multi-channel synchronization work requirements).

The PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE support the cache load, after PWM output is enabled, the register values of the PWM_ENTIRE_CYCLE and the PWM_ACT_CYCLE can be changed anytime, the changed value caches into the cache register. When the PCNTR counter outputs a period of PWM waveform, the value of the cache register can be updated for the PCNTR

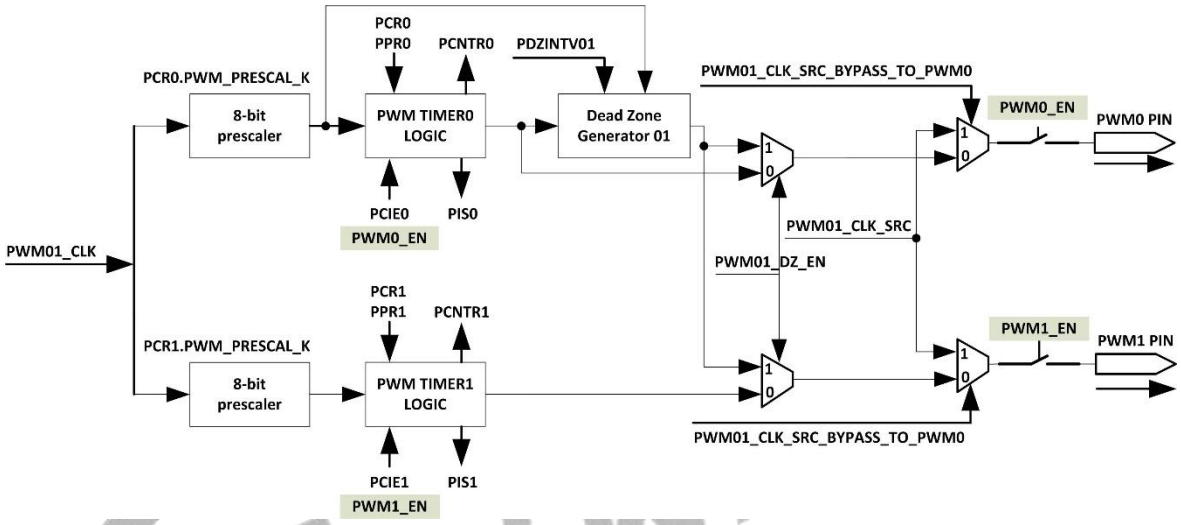
control. The purpose of the cache load is to avoid the unstable PWM output waveform with glitches when updating the values of the PWM_ENTIRE_CYCLE and PWM_ACT_CYCLE.

The PWM supports cycle and pulse waveform output.

Cycle mode: The PWM outputs the setting PWM waveform continually, that is, the output waveform is a continuous PWM square wave.

Pulse mode: After setting the PWM_PUL_NUM parameter, the PWM outputs (PWM_PULNUM+1) periods of PWM waveform, that is, the waveform with several pulses are output.

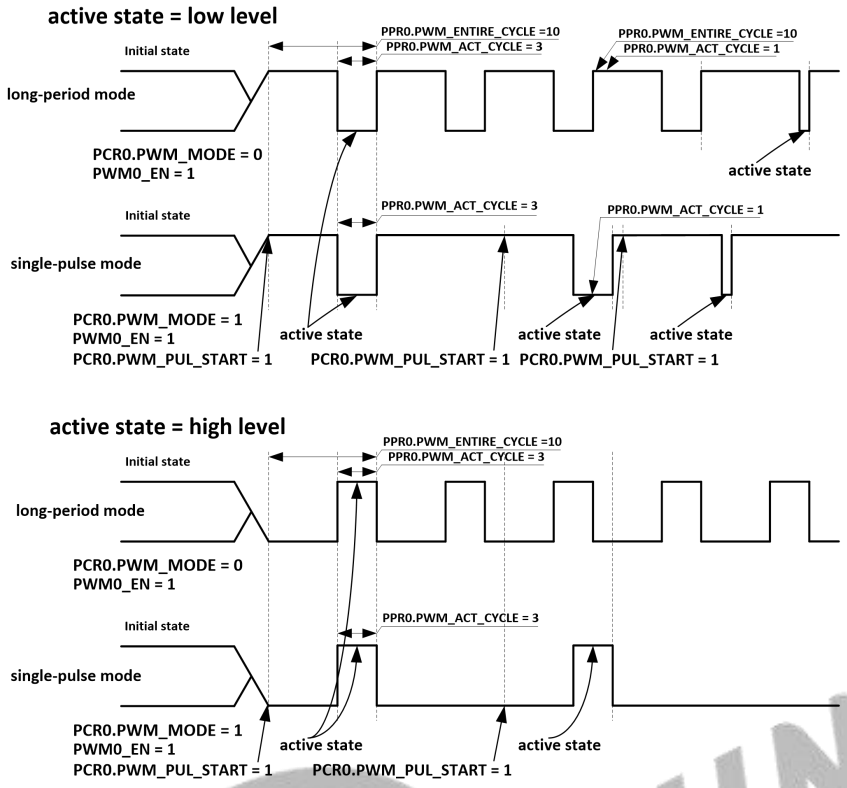
Figure 8-56 PWM01 Output Logic Module Diagram



8.14.3.6 Pulse Mode and Cycle Mode

The PWM output supports pulse mode and cycle mode. PWM in pulse mode outputs PCR[PWM_PUL_NUM] +1 cycles waveform, but PWM in cycle mode outputs continuous waveform. The following figure shows the PWM output waveform in pulse mode and cycle mode.

Figure 8-57 PWM0 Output Waveform in Pulse Mode and Cycle Mode



Each channel of the PWM module supports the PWM output of pulse mode and cycle mode, the active state of the PWM output waveform can be programmed to control.

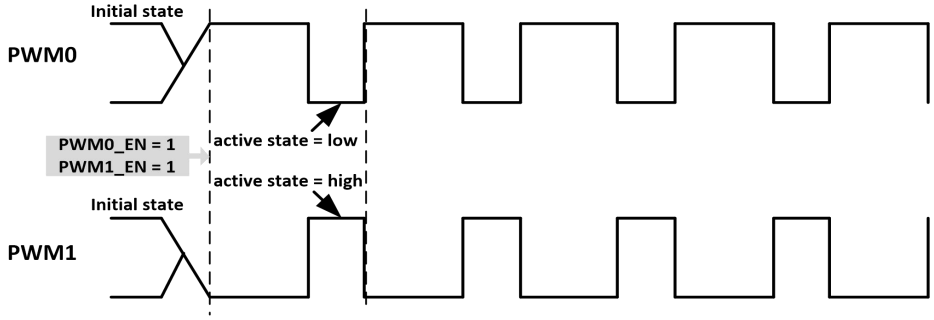
When PCR[PWM_MODE] is 0, the PWM0 outputs in cycle mode. When PCR[PWM_MODE] is 1, the PWM0 outputs in pulse mode.

Specifically, in pulse mode, after the PWM0 channel enabled, PCR[PWM_PUL_START] needs to be set to 1 when the PWM0 needs to output pulse waveform, after completed the output, PCR[PWM_PUL_START] can be cleared to 0 by hardware. The next setting 1 can be operated after PCR[PWM_PUL_START] is cleared.

8.14.3.7 Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time. the following figure shows the complementary pair output of PWM01.

Figure 8-58 PWM01 Complementary Pair Output



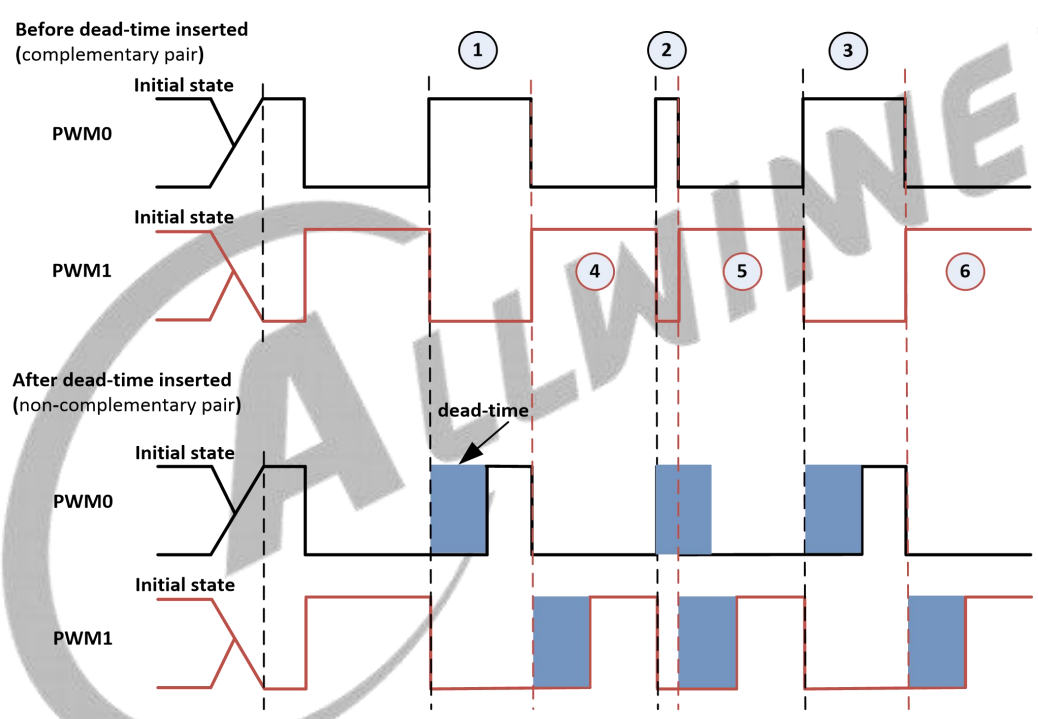
The complementary pair output needs to satisfy the following conditions:

- PWM0 and PWM1 have the same clock divider, frequency, duty-cycle, and phase
- PWM0 and PWM1 have an opposite active state
- Enable the clock gating of PWM0 and PWM1 at the same time
- Enable the waveform output of PWM0 and PWM1 at the same time

8.14.3.8 Dead-time Generator

Every PWM pair has a programmable dead-time generator. When the dead-time function of the PWM pair enabled, the PWM01 output waveform is decided by PWM timer logic and DeadZone Generator. the following figure shows the output waveform.

Figure 8-59 Dead-time Output Waveform



The PWM waveform before the insertion of dead-time indicates a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.

The PWM waveform after the insertion of dead-time indicates a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01. The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.

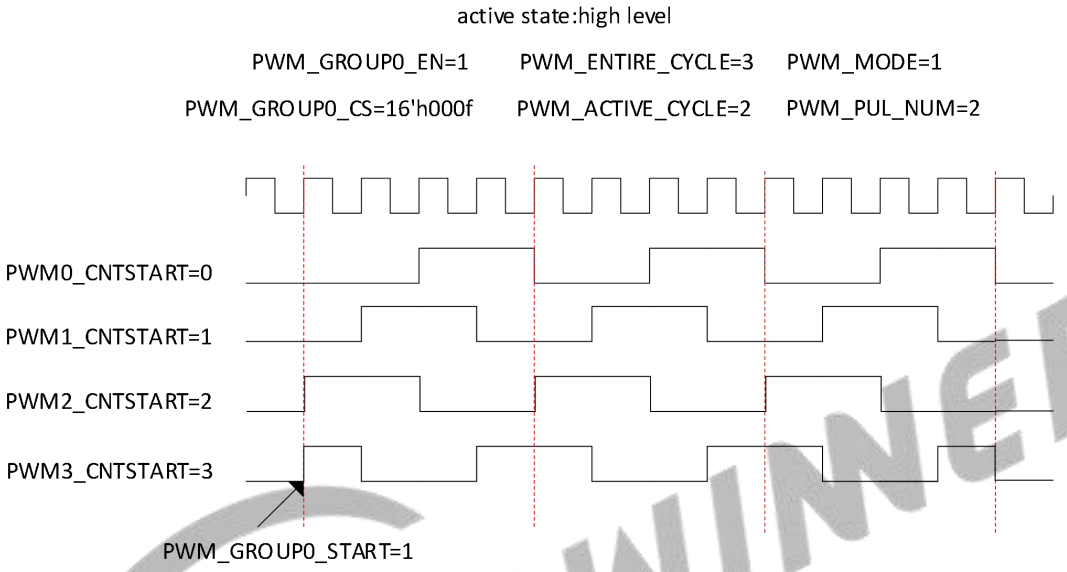
For the complementary pair of Dead Zone Generator 01, the principle of inserting dead-time is that to insert dead-time as soon as the rising edge came. If the high level time for mark② in the above figure is less than dead-time, then dead-time will override the high level. The setting of dead-time needs to consider the period and the duty-cycle of the output waveform. The dead-time formula is defined as follows:

Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PDZINTV01

8.14.3.9 PWM Group Mode

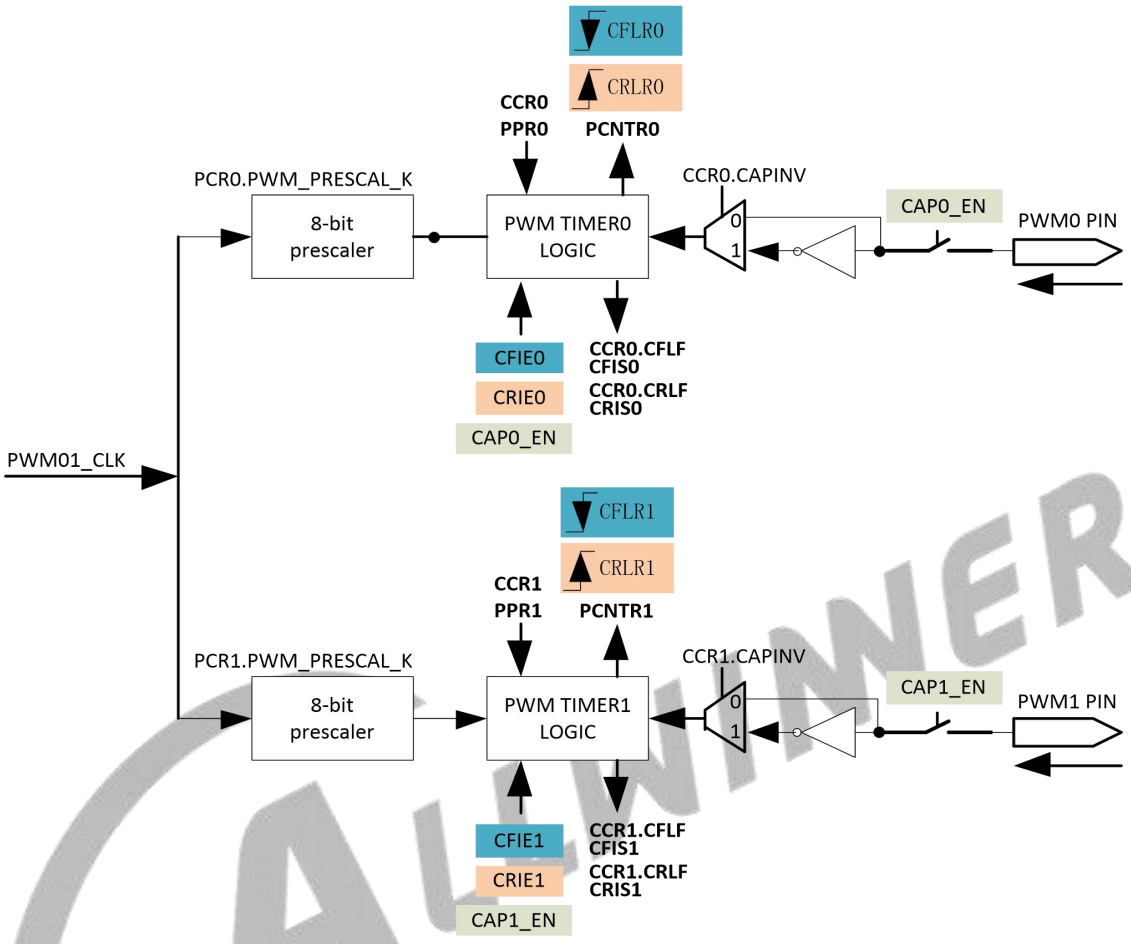
Taking PWM Group0 as an example. The same group of PWM channel is selected to work by PGR0.CS; the same PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE are set by the same clock configuration; the different PWM_COUNTER_START can output PWM group signals with the same duty-cycle and the different phase.

Figure 8-60 Group 0-3 PWM Signal Output



8.14.3.10 Capture Input

Figure 8-61 PWM01 Capture Logic Module Diagram



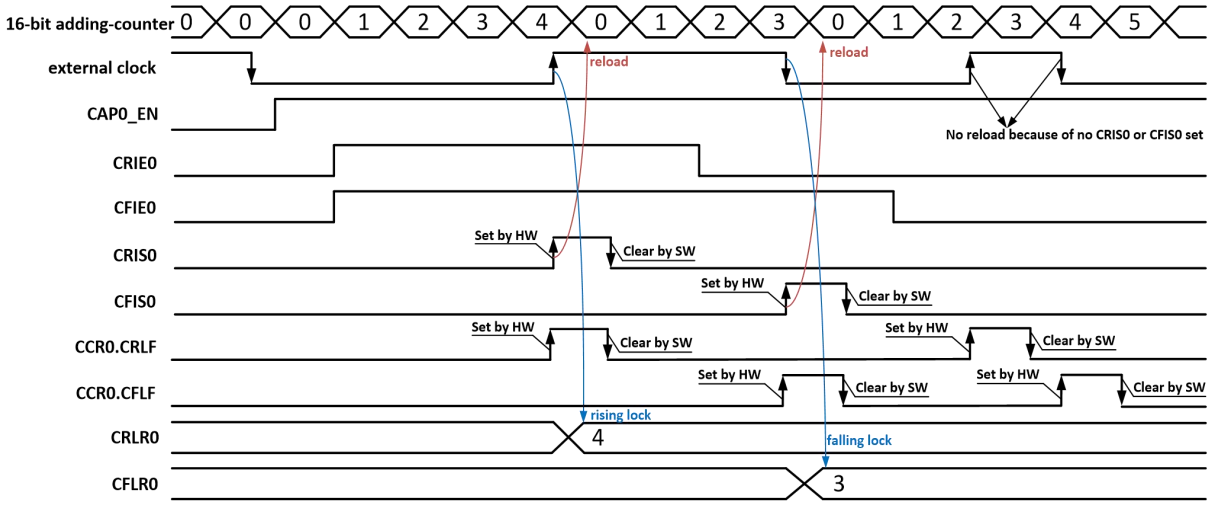
Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture the rising edge and the falling edge of the external clock. Using the PWM0 channel as an example, the PWM0 channel has one CFLR0 and one CRLR0 for capturing up-counter value on the falling edge and rising edge, respectively. You can calculate the period of the external clock by CFLR0 and CRLR0.

Thigh-level = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

Tlow-level = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

Tperiod = Thigh-level + Tlow-level

Figure 8-62 PWM0 Channel Capture Timing



When the capture input function of the PWM0 channel is enabled, the PCNTR of the PWM0 channel starts to work.

When the timer logic module of PWM0 captures a rising edge, the current value of the up-counter is locked to CRLR0 and CCR0[CRLF] is set to 1. If CRIE0 is 1, then CRIS0 is set to 1, the PWM0 channel sends interrupt requests, and the up-counter is loaded to 0 and continues to count. If CRIE0 is 0, the timer logic module of PWM0 captures a rising edge, CRIS0 cannot be set to 1, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of PCNTR is locked to CFLR0 and CCR0[CFLF] is set to 1. If CFIE0 is 1, then CFIS0 is set to 1, the PWM0 channel sends interrupt requests, and the up-counter is loaded to 0 and continues to count. If CFIE0 is 0, the timer logic module of PWM0 captures a falling edge, CFIS0 cannot be set to 1, the up-counter is not loaded to 0.

8.14.4 Programming Guidelines

The following working mode takes PWM01 as an example, other PWM pairs and PWM01 are consistent.

8.14.4.1 Configuring Clock

Step 1 PWM gating: When using PWM, write 1 to PCGR[PWMx_CLK_GATING].

Step 2 PWM clock source select: Set PCCR01[PWM01_CLK_SRC] to select HOSC or APB0 clock.

Step 3 PWM clock divider: Set PCCR01[PWM01_CLK_DIV_M] to select different frequency division coefficient (1/2/4/8/16/32/64/128/256).

Step 4 PWM clock bypass: Set PCGR[PWM_CLK_SRC_BYPASS_TO_PWM] to 1, output the PWM clock after the secondary frequency division to the corresponding PWM output pin.

Step 5 PWM internal clock configuration: Set PCR[PWM_PRESCAL_K] to select any frequency division coefficient from 1 to 256.

NOTE

For the channel of complementary output and group mode, firstly, set the same clock configurations (clock source selects APB0, clock division configures the same division factor); secondly, open clock gating at the same time; thirdly, configure PWM parameters; finally, enable PWM output at the same time to ensure each channel sync.

We suggest that the two channels of the same PWM pair cannot subject to two groups because of they have the same first level clock division and gating. If must allocate based on this way, the first level of clock division of the channel used by all groups needs to set to the same coefficient and open gating at the same time. And the total module needs to be reset when the group mode regroups.

8.14.4.2 Configuring PWM

Step 1 PWM mode: Set PCR[PWM_MODE] to select cycle mode or pulse mode, if pulse mode, PCR[PWM_PUL_NUM] needs to be configured.

Step 2 PWM active level: Set PCR[PWM_ACT_STA] to select a low level or high level.

Step 3 PWM duty-cycle: Configure PPR[PWM_ENTIRE_CYCLE] and PPR[PWM_ACT_CYCLE] after clock gating is opened.

Step 4 PWM starting/stoping phase: Configure PCNTR[PWM_COUNTER_START] after the clock gating is enabled and before the PWM is enabled. You can verify whether the configuration was successful by reading back PCNTR[PWM_COUNTER_STATUS].

Step 5 Enable PWM: Configure PER to select the corresponding PWM enable bit; when selecting pulse mode, PCR[PWM_PUL_START] needs to be enabled.

8.14.4.3 Configuring Deadzone

Step 1 Set initial value: set [PDZINTV01].

Step 2 Enable Deadzone: set [PWM01_DZ_CN].

8.14.4.4 Configuring Capture Input

Step 1 Enable capture: Configure CER to enable the corresponding channel.

Step 2 Capture mode: Configure CCR[CRLF] and CCR[CFLF] to select rising edge capture or falling edge capture, configure CCR[CAPINV] to select whether the input signal does reverse processing.

8.14.5 Register List

Module Name	Base Address
PWMCTRL0	0x0200 0C00
PMWCTRL1	0x0205 1000
S_PWMCTRL	0x0702 0C00
MCU_PWMCTRL	0x0710 3000

Register Name	Offset	Description	PWMCTRL0	PMWCTRL1	S_PWMCTRL	MCU_PWMCTRL
PIER	0x0000	PWM IRQ Enable Register	Yes	Yes	Yes	Yes
PISR	0x0004	PWM IRQ Status Register	Yes	Yes	Yes	Yes
CIER	0x0010	Capture IRQ Enable Register	Yes	Yes	Yes	Yes
CISR	0x0014	Capture IRQ Status Register	Yes	Yes	Yes	Yes
PCCR01	0x0020	PWM01 Clock Configuration Register	Yes	Yes	Yes	Yes
PCCR23	0x0024	PWM23 Clock Configuration Register	Yes	Yes	No	Yes
PCCR45	0x0028	PWM45 Clock Configuration Register	Yes	No	No	Yes
PCCR67	0x002C	PWM67 Clock Configuration Register	Yes	No	No	Yes
PCCR89	0x0030	PWM89 Clock Configuration Register	Yes	No	No	No
PCCRab	0x0034	PWMab Clock Configuration Register	Yes	No	No	No
PCCRcd	0x0038	PWMcd Clock Configuration Register	Yes	No	No	No
PCCRef	0x003C	PWMef Clock Configuration Register	Yes	No	No	No
PCGR	0x0040	PWM Clock Gating Register	Yes	Yes	Yes	Yes
PDZCR01	0x0060	PWM01 Dead Zone Control Register	Yes	Yes	Yes	Yes
PDZCR23	0x0064	PWM23 Dead Zone Control Register	Yes	Yes	No	Yes
PDZCR45	0x0068	PWM45 Dead Zone Control Register	Yes	No	No	Yes
PDZCR67	0x006C	PWM67 Dead Zone Control Register	Yes	No	No	Yes
PDZCR89	0x0070	PWM89 Dead Zone Control Register	Yes	No	No	No
PDZCRab	0x0074	PWMab Dead Zone Control Register	Yes	No	No	No
PDZCRcd	0x0078	PWMcd Dead Zone Control Register	Yes	No	No	No
PDZCRef	0x007C	PWMef Dead Zone Control Register	Yes	No	No	No
PER	0x0080	PWM Enable Register	Yes	Yes	Yes	Yes
PGR0	0x0090	PWM Group0 Register	Yes	Yes	Yes	Yes
PGR1	0x0094	PWM Group1 Register	Yes	Yes	Yes	Yes
PGR2	0x0098	PWM Group2 Register	Yes	Yes	Yes	Yes
PGR3	0x009C	PWM Group3 Register	Yes	Yes	Yes	Yes
CER	0x00c0	Capture Enable Register	Yes	Yes	Yes	Yes
PCR	0x0100+N*0x0020	PWM Control Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
PPR	0x0104+N*0x0020	PWM Period Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
PCNTR	0x0108+N*	PWM Counter Register	N= 0	N= 0 to	N= 0, 1	N= 0 to 7

Register Name	Offset	Description	PWMCTRL0	PMWCTRL1	S_PWMCTRL	MCU_PWMCTRL
	0x0020		to 15	3		
PPCNTR	0x010C+N*0x0020	PWM Pulse Counter Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
CCR	0x0110+N*0x0020	Capture Control Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
CRLR	0x0114+N*0x0020	Capture Rise Lock Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7
CFLR	0x0118+N*0x0020	Capture Fall Lock Register	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

8.14.6 Register Description

8.14.6.1 0x0000 PWM IRQ Enable Register (Default Value: 0x0000_0000)

NOTE

For PWMCTRL1, bit [15:4] are reserved.

For S_PWMCTRL, bit [15:2] are reserved.

For MCU_PWWMCTRL, bit [15:8] are reserved.

Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0x0	PGIE3 PWM group 3 Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	PGIE2 PWM group 2 Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	PGIE1 PWM group 1 Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	PGIE0 PWM group 0 Interrupt Enable 0: Disable 1: Enable

Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
15	R/W	0x0	PCIE15. PWM channel 15 Interrupt Enable. 0: PWM channel 15 Interrupt Disable; 1: PWM channel 15 Interrupt Enable.
14	R/W	0x0	PCIE14. PWM channel 14 Interrupt Enable. 0: PWM channel 14 Interrupt Disable; 1: PWM channel 14 Interrupt Enable.
13	R/W	0x0	PCIE13. PWM channel 13 Interrupt Enable. 0: PWM channel 13 Interrupt Disable; 1: PWM channel 13 Interrupt Enable.
12	R/W	0x0	PCIE12. PWM channel 12 Interrupt Enable. 0: PWM channel 12 Interrupt Disable; 1: PWM channel 12 Interrupt Enable.
11	R/W	0x0	PCIE11. PWM channel 11 Interrupt Enable. 0: PWM channel 11 Interrupt Disable; 1: PWM channel 11 Interrupt Enable.
10	R/W	0x0	PCIE10. PWM channel 10 Interrupt Enable. 0: PWM channel 10 Interrupt Disable; 1: PWM channel 10 Interrupt Enable.
9	R/W	0x0	PCIE9. PWM channel 9 Interrupt Enable. 0: PWM channel 9 Interrupt Disable; 1: PWM channel 9 Interrupt Enable.
8	R/W	0x0	PCIE8. PWM channel 8 Interrupt Enable. 0: PWM channel 8 Interrupt Disable; 1: PWM channel 8 Interrupt Enable.
7	R/W	0x0	PCIE7. PWM channel 7 Interrupt Enable. 0: PWM channel 7 Interrupt Disable; 1: PWM channel 7 Interrupt Enable.
6	R/W	0x0	PCIE6. PWM channel 6 Interrupt Enable. 0: PWM channel 6 Interrupt Disable; 1: PWM channel 6 Interrupt Enable.
5	R/W	0x0	PCIE5.

Offset:0x0000			Register Name: PIER
Bit	Read/Write	Default/Hex	Description
			PWM channel 5 Interrupt Enable. 0: PWM channel 5 Interrupt Disable; 1: PWM channel 5 Interrupt Enable.
4	R/W	0x0	PCIE4. PWM channel 4 Interrupt Enable. 0: PWM channel 4 Interrupt Disable; 1: PWM channel 4 Interrupt Enable.
3	R/W	0x0	PCIE3. PWM channel 3 Interrupt Enable. 0: PWM channel 3 Interrupt Disable; 1: PWM channel 3 Interrupt Enable.
2	R/W	0x0	PCIE2. PWM channel 2 Interrupt Enable. 0: PWM channel 2 Interrupt Disable; 1: PWM channel 2 Interrupt Enable.
1	R/W	0x0	PCIE1. PWM channel 1 Interrupt Enable. 0: PWM channel 1 Interrupt Disable; 1: PWM channel 1 Interrupt Enable.
0	R/W	0x0	PCIE0. PWM channel 0 Interrupt Enable. 0: PWM channel 0 Interrupt Disable; 1: PWM channel 0 Interrupt Enable.

8.14.6.2 0x0004 PWM IRQ Status Register (Default Value: 0x0000_0000)

NOTE

For PWMCTRL1, bit [15:4] are reserved.

For S_PWMCTRL, bit [15:2] are reserved.

For MCU_PWWMCTRL, bit [15:8] are reserved.

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W1C	0x0	PGIS3 PWM group 3 Interrupt Status
18	R/W1C	0x0	PGIS2 PWM group 2 Interrupt Status

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
17	R/W1C	0x0	PGIS1 PWM group 1 Interrupt Status
16	R/W1C	0x0	PGIS0 PWM group 0 Interrupt Status
15	R/W1C	0x0	PIS15. PWM channel 15 Interrupt Status. When PWM channel 15 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 15 interrupt is not pending. 1: PWM channel 15 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 15 interrupt status.
14	R/W1C	0x0	PIS14. PWM channel 14 Interrupt Status. When PWM channel 14 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 14 interrupt is not pending. 1: PWM channel 14 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 14 interrupt status.
13	R/W1C	0x0	PIS13. PWM channel 13 Interrupt Status. When PWM channel 13 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 13 interrupt is not pending. 1: PWM channel 13 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 13 interrupt status.
12	R/W1C	0x0	PIS12. PWM channel 12 Interrupt Status. When PWM channel 12 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 12 interrupt is not pending.

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
			1: PWM channel 12 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 12 interrupt status.
11	R/W1C	0x0	PIS11. PWM channel 11 Interrupt Status. When PWM channel 11 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 11 interrupt is not pending. 1: PWM channel 11 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 11 interrupt status.
10	R/W1C	0x0	PIS10. PWM channel 10 Interrupt Status. When PWM channel 10 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 10 interrupt is not pending. 1: PWM channel 10 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 10 interrupt status.
9	R/W1C	0x0	PIS9. PWM channel 9 Interrupt Status. When PWM channel 9 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 9 interrupt is not pending. 1: PWM channel 9 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 9 interrupt status.
8	R/W1C	0x0	PIS8. PWM channel 8 Interrupt Status. When PWM channel 8 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 8 interrupt is not pending. 1: PWM channel 8 interrupt is pending.

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
			Writes 0: no effect. 1: Clear PWM channel 8 interrupt status.
7	R/W1C	0x0	PIS7. PWM channel 7 Interrupt Status. When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. 1: PWM channel 7 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6. PWM channel 6 Interrupt Status. When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. 1: PWM channel 6 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5. PWM channel 5 Interrupt Status. When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. 1: PWM channel 5 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4. PWM channel 4 Interrupt Status. When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. 1: PWM channel 4 interrupt is pending. Writes 0: no effect.

Offset: 0x0004			Register Name: PISR
Bit	Read/Write	Default/Hex	Description
			1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3. PWM channel 3 Interrupt Status. When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. 1: PWM channel 3 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2. PWM channel 2 Interrupt Status. When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. 1: PWM channel 2 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1. PWM channel 1 Interrupt Status. When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. 1: PWM channel 1 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0. PWM channel 0 Interrupt Status. When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. 1: PWM channel 0 interrupt is pending. Writes 0: no effect. 1: Clear PWM channel 0 interrupt status.

8.14.6.3 0x0010 Capture IRQ Enable Register (Default Value: 0x0000_0000)

NOTE

For PWMCTRL1, bit [31:8] are reserved.

For S_PWMCTRL, bit [31:4] are reserved.

For MCU_PWWMCTRL, bit [31:16] are reserved.

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CFIE15 If this enable bit is set 1, when capture channel 15 captures falling edge, it generates a capture channel 15 pending. 0: Capture channel 15 fall lock Interrupt disable; 1: Capture channel 15 fall lock Interrupt enable.
30	R/W	0x0	CRIE15 If this enable bit is set 1, when capture channel 15 captures rising edge, it generates a capture channel 15 pending. 0: Capture channel 15 rise lock Interrupt disable; 1: Capture channel 15 rise lock Interrupt enable.
29	R/W	0x0	CFIE14 If this enable bit is set 1, when capture channel 14 captures falling edge, it generates a capture channel 14 pending. 0: Capture channel 14 fall lock Interrupt disable; 1: Capture channel 14 fall lock Interrupt enable.
28	R/W	0x0	CRIE14 If this enable bit is set 1, when capture channel 14 captures rising edge, it generates a capture channel 14 pending. 0: Capture channel 14 rise lock Interrupt disable; 1: Capture channel 14 rise lock Interrupt enable.
27	R/W	0x0	CFIE13 If this enable bit is set 1, when capture channel 13 captures falling edge, it generates a capture channel 13 pending. 0: Capture channel 13 fall lock Interrupt disable; 1: Capture channel 13 fall lock Interrupt enable.
26	R/W	0x0	CRIE13 If this enable bit is set 1, when capture channel

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
			13 captures rising edge, it generates a capture channel 13 pending. 0: Capture channel 13 rise lock Interrupt disable; 1: Capture channel 13 rise lock Interrupt enable.
25	R/W	0x0	CFIE12 If this enable bit is set 1, when capture channel 12 captures falling edge, it generates a capture channel 12 pending. 0: Capture channel 12 fall lock Interrupt disable; 1: Capture channel 12 fall lock Interrupt enable.
24	R/W	0x0	CRIE12 If this enable bit is set 1, when capture channel 12 captures rising edge, it generates a capture channel 12 pending. 0: Capture channel 12 rise lock Interrupt disable; 1: Capture channel 12 rise lock Interrupt enable.
23	R/W	0x0	CFIE11 If this enable bit is set 1, when capture channel 11 captures falling edge, it generates a capture channel 11 pending. 0: Capture channel 11 fall lock Interrupt disable; 1: Capture channel 11 fall lock Interrupt enable.
22	R/W	0x0	CRIE11 If this enable bit is set 1, when capture channel 11 captures rising edge, it generates a capture channel 11 pending. 0: Capture channel 11 rise lock Interrupt disable; 1: Capture channel 11 rise lock Interrupt enable.
21	R/W	0x0	CFIE10 If this enable bit is set 1, when capture channel 10 captures falling edge, it generates a capture channel 10 pending. 0: Capture channel 10 fall lock Interrupt disable; 1: Capture channel 10 fall lock Interrupt enable.
20	R/W	0x0	CRIE10 If this enable bit is set 1, when capture channel 10 captures rising edge, it generates a capture channel 10 pending. 0: Capture channel 10 rise lock Interrupt disable; 1: Capture channel 10 rise lock Interrupt enable.
19	R/W	0x0	CFIE9

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
			If this enable bit is set 1, when capture channel 9 captures falling edge, it generates a capture channel 9 pending. 0: Capture channel 9 fall lock Interrupt disable; 1: Capture channel 9 fall lock Interrupt enable.
18	R/W	0x0	CRIE9 If this enable bit is set 1, when capture channel 9 captures rising edge, it generates a capture channel 9 pending. 0: Capture channel 9 rise lock Interrupt disable; 1: Capture channel 9 rise lock Interrupt enable.
17	R/W	0x0	CFIE8 If this enable bit is set 1, when capture channel 8 captures falling edge, it generates a capture channel 8 pending. 0: Capture channel 8 fall lock Interrupt disable; 1: Capture channel 8 fall lock Interrupt enable.
16	R/W	0x0	CRIE8 If this enable bit is set 1, when capture channel 8 captures rising edge, it generates a capture channel 8 pending. 0: Capture channel 8 rise lock Interrupt disable; 1: Capture channel 8 rise lock Interrupt enable.
15	R/W	0x0	CFIE7 If this enable bit is set 1, when capture channel 7 captures falling edge, it generates a capture channel 7 pending. 0: Capture channel 7 fall lock Interrupt disable; 1: Capture channel 7 fall lock Interrupt enable.
14	R/W	0x0	CRIE7 If this enable bit is set 1, when capture channel 7 captures rising edge, it generates a capture channel 7 pending. 0: Capture channel 7 rise lock Interrupt disable; 1: Capture channel 7 rise lock Interrupt enable.
13	R/W	0x0	CFIE6 If this enable bit is set 1, when capture channel 6 captures falling edge, it generates a capture channel 6 pending. 0: Capture channel 6 fall lock Interrupt disable; 1: Capture channel 6 fall lock Interrupt enable.

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
12	R/W	0x0	CRIE6 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
11	R/W	0x0	CFIE5 If this enable bit is set 1, when capture channel 5 captures falling edge, it generates a capture channel 5 pending. 0: Capture channel 5 fall lock Interrupt disable; 1: Capture channel 5 fall lock Interrupt enable.
10	R/W	0x0	CRIE5 If this enable bit is set 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock Interrupt disable; 1: Capture channel 5 rise lock Interrupt enable.
9	R/W	0x0	CFIE4 If this enable bit is set 1, when capture channel 4 captures falling edge, it generates a capture channel 4 pending. 0: Capture channel 4 fall lock Interrupt disable; 1: Capture channel 4 fall lock Interrupt enable.
8	R/W	0x0	CRIE4 If this enable bit is set 1, when capture channel 4 captures rising edge, it generates a capture channel 4 pending. 0: Capture channel 4 rise lock Interrupt disable; 1: Capture channel 4 rise lock Interrupt enable.
7	R/W	0x0	CFIE3 If this enable bit is set 1, when capture channel 3 captures falling edge, it generates a capture channel 3 pending. 0: Capture channel 3 fall lock Interrupt disable; 1: Capture channel 3 fall lock Interrupt enable.
6	R/W	0x0	CRIE3 If this enable bit is set 1, when capture channel 3 captures rising edge, it generates a capture channel 3 pending. 0: Capture channel 3 rise lock Interrupt disable;

Offset: 0x0010			Register Name: CIER
Bit	Read/Write	Default/Hex	Description
			1: Capture channel 3 rise lock Interrupt enable.
5	R/W	0x0	CFIE2 If this enable bit is set 1, when capture channel 2 captures falling edge, it generates a capture channel 2 pending. 0: Capture channel 2 fall lock Interrupt disable; 1: Capture channel 2 fall lock Interrupt enable.
4	R/W	0x0	CRIE2 If this enable bit is set 1, when capture channel 2 captures rising edge, it generates a capture channel 2 pending. 0: Capture channel 2 rise lock Interrupt disable; 1: Capture channel 2 rise lock Interrupt enable.
3	R/W	0x0	CFIE1 If this enable bit is set 1, when capture channel 1 captures falling edge, it generates a capture channel 1 pending. 0: Capture channel 1 fall lock Interrupt disable; 1: Capture channel 1 fall lock Interrupt enable.
2	R/W	0x0	CRIE1 If this enable bit is set 1, when capture channel 1 captures rising edge, it generates a capture channel 1 pending. 0: Capture channel 1 rise lock Interrupt disable; 1: Capture channel 1 rise lock Interrupt enable.
1	R/W	0x0	CFIE0 If this enable bit is set 1, when capture channel 0 captures falling edge, it generates a capture channel 0 pending. 0: Capture channel 0 fall lock Interrupt disable; 1: Capture channel 0 fall lock Interrupt enable.
0	R/W	0x0	CRIE0 If this enable bit is set 1, when capture channel 0 captures rising edge, it generates a capture channel 0 pending 0: Capture channel 0 rise lock Interrupt disable; 1: Capture channel 0 rise lock Interrupt enable.

8.14.6.4 0x0014 Capture IRQ Status Register (Default Value: 0x0000_0000)

NOTE

For PWMCTRL1, bit [31:8] are reserved.

For S_PWMCTRL, bit [31:4] are reserved.

For MCU_PWWMCTRL, bit [31:16] are reserved.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CFIS15 Capture channel 15 falling lock interrupt status. When capture channel 15 captures falling edge, if capture channel 15 fall lock interrupt (CFIE15) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 15 interrupt is not pending. 1: Capture channel 15 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 15 interrupt status.
30	R/W1C	0x0	CRIS15 Capture channel 15 rising lock interrupt status. When capture channel 15 captures rising edge, if capture channel 15 rise lock interrupt (CRIE15) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 15 interrupt is not pending. 1: Capture channel 15 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 15 interrupt status.
29	R/W1C	0x0	CFIS14 Capture channel 14 falling lock interrupt status When capture channel 14 captures falling edge, if capture channel 14 fall lock interrupt (CFIE14) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			Reads 0: Capture channel 14 interrupt is not pending. 1: Capture channel 14 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 14 interrupt status.
28	R/W1C	0x0	CRIS14 Capture channel 14 rising lock interrupt status When capture channel 14 captures rising edge, if capture channel 14 rise lock interrupt (CRIE14) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 14 interrupt is not pending. 1: Capture channel 14 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 14 interrupt status.
27	R/W1C	0x0	CFIS13 Capture channel 13 falling lock interrupt status When capture channel 13 captures falling edge, if capture channel 13 fall lock interrupt (CFIE13) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 13 interrupt is not pending. 1: Capture channel 13 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 13 interrupt status.
26	R/W1C	0x0	CRIS13 Capture channel 13 rising lock interrupt status When capture channel 13 captures rising edge, if capture channel 13 rise lock interrupt (CRIE13) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 13 interrupt is not pending.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			1: Capture channel 13 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 13 interrupt status.
25	R/W1C	0x0	CFIS12 Capture channel 12 falling lock interrupt status When capture channel 12 captures falling edge, if capture channel 12 fall lock interrupt (CFIE12) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 12 interrupt is not pending. 1: Capture channel 12 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 12 interrupt status.
24	R/W1C	0x0	CRIS12 Capture channel 12 rising lock interrupt status When capture channel 12 captures rising edge, if capture channel 12 rise lock interrupt (CRIE12) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 12 interrupt is not pending. 1: Capture channel 12 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 12 interrupt status.
23	R/W1C	0x0	CFIS11 Capture channel 11 falling lock interrupt status When capture channel 11 captures falling edge, if capture channel 11 fall lock interrupt (CFIE11) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 11 interrupt is not pending. 1: Capture channel 11 interrupt is pending.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			Writes 0: no effect. 1: Clear capture channel 11 interrupt status.
22	R/W1C	0x0	CRIS11 Capture channel 11 rising lock interrupt status. When capture channel 11 captures rising edge, if capture channel 11 rise lock interrupt (CRIE11) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 11 interrupt is not pending. 1: Capture channel 11 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 11 interrupt status.
21	R/W1C	0x0	CFIS10 Capture channel 10 falling lock interrupt status When capture channel 10 captures falling edge, if capture channel 10 fall lock interrupt (CFIE10) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 10 interrupt is not pending. 1: Capture channel 10 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 10 interrupt status.
20	R/W1C	0x0	CRIS10 Capture channel 10 rising lock interrupt status When capture channel 10 captures rising edge, if capture channel 10 rise lock interrupt (CRIE10) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 10 interrupt is not pending. 1: Capture channel 10 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 10 interrupt

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			status.
19	R/W1C	0x0	CFIS9 Capture channel 9 falling lock interrupt status When capture channel 9 captures falling edge, if capture channel 9 fall lock interrupt (CFIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 9 interrupt status.
18	R/W1C	0x0	CRIS9 Capture channel 9 rising lock interrupt status When capture channel 9 captures rising edge, if capture channel 9 rise lock interrupt (CRIE9) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. 1: Capture channel 9 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 9 interrupt status.
17	R/W1C	0x0	CFIS8 Capture channel 8 falling lock interrupt status When capture channel 8 captures falling edge, if capture channel 8 fall lock interrupt (CFIE8) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 8 interrupt status.
16	R/W1C	0x0	CRIS8 Capture channel 8 rising lock interrupt status When capture channel 8 captures rising edge, if capture channel 8 rise lock interrupt (CRIE8) is

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. 1: Capture channel 8 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 8 interrupt status.
15	R/W1C	0x0	CFIS7 Capture channel 7 falling lock interrupt status When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (CFIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capture channel 7 rising lock interrupt status When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (CRIE7) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6 Capture channel 6 falling lock interrupt status When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (CFIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
12	R/W1C	0x0	CRIS6 Capture channel 6 rising lock interrupt status When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (CRIE6) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capture channel 5 falling lock interrupt status When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (CFIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
10	R/W1C	0x0	CRIS5 Capture channel 5 rising lock interrupt status When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (CRIE5) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 5 interrupt status.
9	R/W1C	0x0	CFIS4 Capture channel 4 falling lock interrupt status

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (CFIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
8	R/W1C	0x0	CRIS4 Capture channel 4 rising lock interrupt status When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (CRIE4) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (CFIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (CRIE3) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
			pending. 1: Capture channel 3 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (CFIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (CRIE2) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (CFIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 1 interrupt status.

Offset: 0x0014			Register Name: CISR
Bit	Read/Write	Default/Hex	Description
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (CRIE1) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (CFIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (CRIE0) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 0 interrupt status.

8.14.6.5 0x0020 PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCR01	Support	Support	Support	Support

Offset: 0x0020			Register Name: PCCR01
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM01_CLK_SRC Select PWM01 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM01_CLK_DIV_M PWM01 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.6 0x0024 PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCR23	Support	Support	Not Support	Support

Offset: 0x0024			Register Name: PCCR23
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM23_CLK_SRC_SEL Select PWM23 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM23_CLK_DIV_M PWM23 clock divide M 0000: /1 0001: /2

Offset: 0x0024			Register Name: PCCR23
Bit	Read/Write	Default/Hex	Description
			0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.7 0x0028 PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCR45	Support	Not Support	Not Support	Support

Offset: 0x0028			Register Name: PCCR45
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM45_CLK_SRC_SEL Select PWM45 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM45_CLK_DIV_M PWM45 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.8 0x002C PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCR67	Support	Not Support	Not Support	Support

Offset: 0x002C			Register Name: PCCR67
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM67_CLK_SRC_SEL Select PWM67 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM67_CLK_DIV_M PWM67 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.9 0x0030 PWM89 Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCR89	Support	Not Support	Not Support	Not Support

Offset: 0x0030			Register Name: PCCR89
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWM89_CLK_SRC_SEL Select PWM89 clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWM89_CLK_DIV_M PWM89 clock divide M

Offset: 0x0030			Register Name: PCCR89
Bit	Read/Write	Default/Hex	Description
			0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.10 0x0034 PWMab Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCRab	Support	Not Support	Not Support	Not Support

Offset: 0x0034			Register Name: PCCRab
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWMab_CLK_SRC_SEL Select PWMab clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWMab_CLK_DIV_M PWMab clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.11 0x0038 PWMcd Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCRcd	Support	Not Support	Not Support	Not Support

Offset: 0x0038			Register Name: PCCRcd
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWMcd_CLK_SRC_SEL Select PWMcd clock source 00: OSC24M 01: APB1 Others: /
6:4	/	/	/
3:0	R/W	0x0000	PWMcd_CLK_DIV_M PWMcd clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.12 0x003C PWMef Clock Configuration Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCCRef	Support	Not Support	Not Support	Not Support

Offset: 0x003C			Register Name: PCCRef
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:7	R/W	0x00	PWMef_CLK_SRC_SEL Select PWMef clock source 00: DCXO24M 01: APB1 Others: /

Offset: 0x003C			Register Name: PCCRef
Bit	Read/Write	Default/Hex	Description
6:4	/	/	/
3:0	R/W	0x0000	PWMef_CLK_DIV_M PWMef clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

8.14.6.13 0x0040 PWM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PWM15_CLK_BYPASS Bypass clock source (after pre-scale) to PWM15 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
30	R/W	0x0	PWM14_CLK_BYPASS Bypass clock source (after pre-scale) to PWM14 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
29	R/W	0x0	PWM13_CLK_BYPASS Bypass clock source(after pre-scale) to PWM13 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
28	R/W	0x0	PWM12_CLK_BYPASS Bypass clock source (after pre-scale) to PWM12 output 0: not bypass 1: bypass

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
			Note: This bit is only for PWMCTRL0.
27	R/W	0x0	PWM11_CLK_BYPASS Bypass clock source(after pre-scale) to PWM11 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
26	R/W	0x0	PWM10_CLK_BYPASS Bypass clock source(after pre-scale) to PWM10 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
25	R/W	0x0	PWM9_CLK_BYPASS Bypass clock source(after pre-scale) to PWM9 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
24	R/W	0x0	PWM8_CLK_BYPASS Bypass clock source(after pre-scale) to PWM8 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0.**
23	R/W	0x0	PWM7_CLK_BYPASS Bypass clock source(after pre-scale) to PWM7 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
22	R/W	0x0	PWM6_CLK_BYPASS Bypass clock source(after pre-scale) to PWM6 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
21	R/W	0x0	PWM5_CLK_BYPASS Bypass clock source(after pre-scale) to PWM5

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
			output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
20	R/W	0x0	PWM4_CLK_BYPASS Bypass clock source(after pre-scale) to PWM4 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
19	R/W	0x0	PWM3_CLK_BYPASS Bypass clock source(after pre-scale) to PWM3 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0, PWMCTRL1, and MCU_PWMCTRL.**
18	R/W	0x0	PWM2_CLK_BYPASS Bypass clock source(after pre-scale) to PWM2 output 0: not bypass 1: bypass **Note: This bit is only for PWMCTRL0, PWMCTRL1, and MCU_PWMCTRL.**
17	R/W	0x0	PWM1_CLK_BYPASS Bypass clock source(after pre-scale) to PWM1 output 0: not bypass 1: bypass
16	R/W	0x0	PWM0_CLK_BYPASS Bypass clock source (after pre-scale) to PWM0 output 0: not bypass 1: bypass
15	R/W	0x0	PWM15_CLK_GATING Gating clock for PWM15 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
14	R/W	0x0	PWM14_CLK_GATING Gating clock for PWM14 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
13	R/W	0x0	PWM13_CLK_GATING Gating clock for PWM13 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
12	R/W	0x0	PWM12_CLK_GATING Gating clock for PWM12 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
11	R/W	0x0	PWM11_CLK_GATING Gating clock for PWM11 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
10	R/W	0x0	PWM10_CLK_GATING Gating clock for PWM10 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
9	R/W	0x0	PWM9_CLK_GATING Gating clock for PWM9 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
8	R/W	0x0	PWM8_CLK_GATING Gating clock for PWM8 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0.**
7	R/W	0x0	PWM7_CLK_GATING Gating clock for PWM7 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**

Offset: 0x0040			Register Name: PCGR
Bit	Read/Write	Default/Hex	Description
6	R/W	0x0	PWM6_CLK_GATING Gating clock for PWM6 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
5	R/W	0x0	PWM5_CLK_GATING Gating clock for PWM5 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
4	R/W	0x0	PWM4_CLK_GATING Gating clock for PWM4 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0 and MCU_PWMCTRL.**
3	R/W	0x0	PWM3_CLK_GATING Gating clock for PWM3 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0, PWMCTRL1, and MCU_PWMCTRL.**
2	R/W	0x0	PWM2_CLK_GATING Gating clock for PWM2 0: Mask 1: Pass **Note: This bit is only for PWMCTRL0, PWMCTRL1, and MCU_PWMCTRL.**
1	R/W	0x0	PWM1_CLK_GATING Gating clock for PWM1 0: Mask 1: Pass
0	R/W	0x0	PWM0_CLK_GATING Gating clock for PWM0 0: Mask 1: Pass

8.14.6.14 0x0060 PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCR01	Support	Support	Support	Support

Offset: 0x0060			Register Name: PDZCR01
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01 PWM01 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.15 0x0064 PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCR23	Support	Support	Not Support	Support

Offset: 0x0064			Register Name: PDZCR23
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN PWM23 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.16 0x0068 PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCR45	Support	Not Support	Not Support	Support

Offset: 0x0068			Register Name: PDZCR45
Bit	Read/Write	Default/Hex	Description

Offset: 0x0068			Register Name: PDZCR45
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM45_DZ_INTV PWM45 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN PWM45 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.17 0x006C PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCR67	Support	Not Support	Not Support	Support

Offset: 0x006C			Register Name: PDZCR67
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM67_DZ_INTV PWM67 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN PWM67 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.18 0x0070 PWM89 Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCR89	Support	Not Support	Not Support	Not Support

Offset: 0x0070			Register Name: PDZCR89
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM89_DZ_INTV PWM89 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM89_DZ_EN PWM89 Dead Zone enable

Offset: 0x0070			Register Name: PDZCR89
Bit	Read/Write	Default/Hex	Description
			0: Dead Zone disable 1: Dead Zone enable

8.14.6.19 0x0074 PWMab Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCRab	Support	Not Support	Not Support	Not Support

Offset: 0x0074			Register Name: PDZCRab
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWMab_DZ_INTV PWMab Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWMab_DZ_EN PWMab Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.20 0x0078 PWMcd Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCRcd	Support	Not Support	Not Support	Not Support

Offset: 0x0078			Register Name: PDZCRcd
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWMcd_DZ_INTV PWMcd Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWMcd_DZ_EN PWMcd Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.21 0x007C PWMef Dead Zone Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PDZCRef	Support	Not Support	Not Support	Not Support

Offset: 0x007C			Register Name: PDZCRef
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWMef_DZ_INTV PWMef Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWMef_DZ_EN PWMef Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

8.14.6.22 0x0080 PWM Enable Register (Default Value: 0x0000_0000)

NOTE

For PWMCTRL1, bit [15:4] are reserved.

For S_PWMCTRL, bit [15:2] are reserved.

For MCU_PWWMCTRL, bit [15:8] are reserved.

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	PWM15_EN PWM Channel 15 Enable 0: PWM disable 1: PWM enable
14	R/W	0x0	PWM14_EN PWM Channel14 Enable 0: PWM disable 1: PWM enable
13	R/W	0x0	PWM13_EN PWM Channel 13 Enable 0: PWM disable 1: PWM enable
12	R/W	0x0	PWM12_EN

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
			PWM Channel 12 Enable 0: PWM disable 1: PWM enable
11	R/W	0x0	PWM11_EN PWM Channel 11 Enable 0: PWM disable 1: PWM enable
10	R/W	0x0	PWM10_EN PWM Channel 10 Enable 0: PWM disable 1: PWM enable
9	R/W	0x0	PWM9_EN PWM Channel 9 Enable 0: PWM disable 1: PWM enable
8	R/W	0x0	PWM8_EN PWM Channel 8 Enable 0: PWM disable 1: PWM enable
7	R/W	0x0	PWM7_EN PWM Channel 7 Enable 0: PWM disable 1: PWM enable
6	R/W	0x0	PWM6_EN PWM Channel 6 Enable 0: PWM disable 1: PWM enable
5	R/W	0x0	PWM5_EN PWM Channel 5 Enable 0: PWM disable 1: PWM enable
4	R/W	0x0	PWM4_EN PWM Channel 4 Enable 0: PWM disable 1: PWM enable
3	R/W	0x0	PWM3_EN PWM Channel 3 Enable 0: PWM disable 1: PWM enable
2	R/W	0x0	PWM2_EN PWM Channel 2 Enable

Offset: 0x0080			Register Name: PER
Bit	Read/Write	Default/Hex	Description
			0: PWM disable 1: PWM enable
1	R/W	0x0	PWM1_EN PWM Channel 1 Enable 0: PWM disable 1: PWM enable
0	R/W	0x0	PWM0_EN PWM Channel 0 Enable 0: PWM disable 1: PWM enable

8.14.6.23 0x0090 PWM Group0 Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: PGR0
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG0_START PWM channels selected in PWMG0_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG0_EN PWM Group0 Enable
15:0	R/W	0x0	PWMG0_CS If bit[i] is set, PWM i is selected as one channel of PWM Group0

8.14.6.24 0x0094 PWM Group1 Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: PGR1
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG1_START PWM channels selected in PWMG1_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG1_EN PWM Group1 Enable
15:0	R/W	0x0	PWMG1_CS If bit[i] is set, PWM i is selected as one channel of PWM Group1.

8.14.6.25 0x0098 PWM Group2 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: PGR2
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG2_START PWM channels selected in PWMG2_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG2_EN PWM Group2 Enable
15:0	R/W	0x0	PWMG2_CS If bit[i] is set, PWM i is selected as one channel of PWM Group2.

8.14.6.26 0x009C PWM Group3 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PGR3
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/WAC	0x0	PWMG3_START PWM channels selected in PWMG3_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG3_EN PWM Group2 Enable
15:0	R/W	0x0	PWMG3_CS If bit[i] is set, PWM i is selected as one channel of PWM Group3.

8.14.6.27 0x00C0 Capture Enable Register (Default Value: 0x0000_0000)

NOTE

For PWMCTRL1, bit [15:4] are reserved.

For S_PWMCTRL, bit [15:2] are reserved.

For MCU_PWWMCTRL, bit [15:8] are reserved.

Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	CAP15_EN

Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
			When enable capture function, the 16-bit up-counter starts working and capture channel 15 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
14	R/W	0x0	CAP14_EN When enable capture function, the 16-bit up-counter starts working and capture channel 14 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
13	R/W	0x0	CAP13_EN When enable capture function, the 16-bit up-counter starts working and capture channel 13 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
12	R/W	0x0	CAP12_EN When enable capture function, the 16-bit up-counter starts working and capture channel 12 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
11	R/W	0x0	CAP11_EN When enable capture function, the 16-bit up-counter starts working and capture channel 11 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
10	R/W	0x0	CAP10_EN When enable capture function, the 16-bit up-counter starts working and capture channel 10 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
9	R/W	0x0	CAP9_EN When enable capture function, the 16-bit up-counter starts working and capture channel 9 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
8	R/W	0x0	CAP8_EN When enable capture function, the 16-bit up-counter starts working and capture channel 8 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
7	R/W	0x0	CAP7_EN When enable capture function, the 16-bit up-counter starts working and capture channel 7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
6	R/W	0x0	CAP6_EN When enable capture function, the 16-bit up-counter starts working and capture channel 6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
5	R/W	0x0	CAP5_EN When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
4	R/W	0x0	CAP4_EN When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable

Offset: 0x00C0			Register Name: CER
Bit	Read/Write	Default/Hex	Description
			1: Capture enable
3	R/W	0x0	CAP3_EN When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
2	R/W	0x0	CAP2_EN When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
1	R/W	0x0	CAP1_EN When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
0	R/W	0x0	CAP0_EN When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

8.14.6.28 0x0100+N*0x0020 PWM Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x0100+N*0x0020			Register Name: PCR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_PUL_NUM In pulse mode, PWM output pulse for PWM_CYCLE_NUM+1 times and then stop.

Offset: 0x0100+N*0x0020			Register Name: PCR
Bit	Read/Write	Default/Hex	Description
15:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM period register ready 0: PWM period register is ready to write 1: PWM period register is busy.
10	R/WAC	0x0	PWM_PUL_START PWM pulse output start 0: no effect 1: output pulse for PWM_CYCLE_NUM+1 After finishing configuration for outputting pulse, set this bit once and then PWM would output waveform. After the waveform is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM output mode select 0: cycle mode 1: pulse mode
8	R/W	0x0	PWM_ACT_STA PWM active state 0: Low Level 1: High Level
7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1) K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256

8.14.6.29 0x0104+N*0x0020 PWM Period Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PPR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x0104+N*0x0020			Register Name: PPR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock 0 = 1 cycle

Offset: 0x0104+N*0x0020			Register Name: PPR
Bit	Read/Write	Default/Hex	Description
			1 = 2 cycles ..... N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK .
15:0	R/W	0x0	PWM_ACT_CYCLE Number of the active cycles in the PWM clock 0 = 0 cycle 1 = 1 cycles ..... N = N cycles

8.14.6.30 0x0108+N*0x0020 PWM Counter Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PCNTR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x0108+N*0x0020			Register Name: PCNTR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PWM_COUNTER_START PWM counter value is set for phase control.
15:0	R	0x0	PWM_COUNTER_STATUS On PWM output or capture input, reading this register could get the current value of the PWM 16 bit up-counter.

8.14.6.31 0x010C+N*0x0020 PWM Pulse Counter Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
PPCNTR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x010C+N*0x0020			Register Name: PPCNTR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	PWM_PUL_COUNTER_STATUS On PWM output , reading this register could get the current value of the PWM pulse counter.

8.14.6.32 0x0110+N*0x0020 Capture Control Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
CCR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x0110+N*0x0020			Register Name: CCR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/W1C	0x0	CRLF When capture channel captures rising edge, the 16-bit up-counter's current value is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
3	R/W1C	0x0	CFLF When capture channel captures falling edge, the 16-bit up-counter's current value is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
2	R/W	0x0	CRTE Rising edge capture trigger enable
1	R/W	0x0	CFTE Falling edge capture trigger enable
0	R/W	0x0	CAPINV Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: not inverse 1: inverse

8.14.6.33 0x0114+N*0x0020 Capture Rise Lock Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
CRLR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x0114+N*0x0020			Register Name: CRLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CRLR When capture channel captures rising edge, the 16-bit up-counter's current value is latched to this register.

8.14.6.34 0x0118+N*0x0020 Capture Fall Lock Register (Default Value: 0x0000_0000)

Register	PWMCTRL0	PWMCTRL1	S_PWMCTRL	MCU_PWMCTRL
CFLR	N= 0 to 15	N= 0 to 3	N= 0, 1	N= 0 to 7

Offset: 0x0118+N*0x0020			Register Name: CFLR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CFLR When capture channel captures falling edge, the 16-bit up-counter's current value is latched to this register.

8.15 SPI

8.15.1 Overview

The Serial Peripheral Interface (SPI) is a full-duplex, synchronous, four-wire serial communication interface between a CPU and SPI-compliant external devices. The SPI controller contains a 64 x 8 bits receiver buffer (RXFIFO) and a 64 x 8 bits transmit buffer (TXFIFO). It can work in master mode and slave mode.

The SPI has the following features:

- Three SPI interfaces:
  - SPI0 and SPI2 in CPUX Domain
  - S_SPI0 in CPUS Domain
- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmmable serial data frame length of 1 bit to 32 bits
- Maximum clock frequency: 100MHz
- TX/RX DMA slave interface
- 8-bit wide and 64-entry FIFO for both transmitting and receiving data
- 8-bit wide and 4-entry buffer for transmitting
- 8-bit wide and 128-entry buffer for receiving data
- Supports mode0, mode1, mode2, and mode3
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

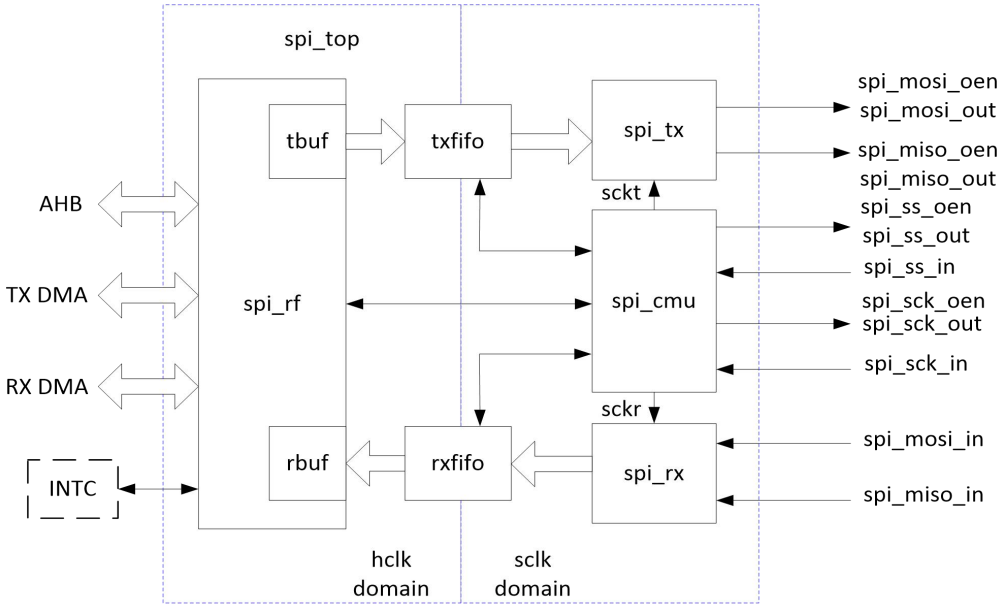
NOTE

This chapter only describes SPI0, SPI2, and S_SPI0. For detailed information of SPI1 (supports SPI mode and DBI mode), please refer to section 8.16 SPI_DBI.

8.15.2 Block Diagram

The following figure shows a block diagram of the SPI.

Figure 8-63 SPI Block Diagram



SPI contains the following sub-blocks:

Table 8-40 SPI Sub-blocks

Sub-block	Description
spi_rf	Responsible for implementing the internal register, interrupt, and DMA Request.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	Responsible for implementing SPI bus clock, chip select, internal sample, and the generation of transfer clock.
spi_tx	Responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	Responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.

8.15.3 Functional Description

8.15.3.1 External Signals

The following table describes the external signals of SPI. The MOSI and MISO are bidirectional I/O, when SPI is as a master device, the CLK and CS are the output pin; when SPI is as a slave device, the CLK and CS are the input pin. When using SPI, the corresponding PADs are selected as SPI function via section 8.5 GPIO.

Table 8-41 SPI External Signals

Signal Name	Description	Type
SPI0-CS[1:0]	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal Provides serial interface timing.	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI0-HOLD	SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI2-CS0	SPI2 Chip Select Signal, Low Active	I/O
SPI2-CLK	SPI2 Clock Signal Provides serial interface timing.	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
S-SPI0-CS0	S-SPI Chip Select Signal, Low Active	I/O
S-SPI0-CLK	S-SPI Clock Signal Provides serial interface timing.	I/O
S-SPI0-MOSI	S-SPI Master Data Out, Slave Data In	I/O
S-SPI0-MISO	S-SPI Master Data In, Slave Data Out	I/O

8.15.3.2 Clock Sources

Every SPI controller gets 5 different clock sources, users can select one of them to make SPI clock source. The following table describes the clock sources for SPI. For more details on the clock setting, configuration, and gating information, see section 2.5 Clock Controller Unit (CCU) and section 2.11 Power Reset Clock Management (PRCM).

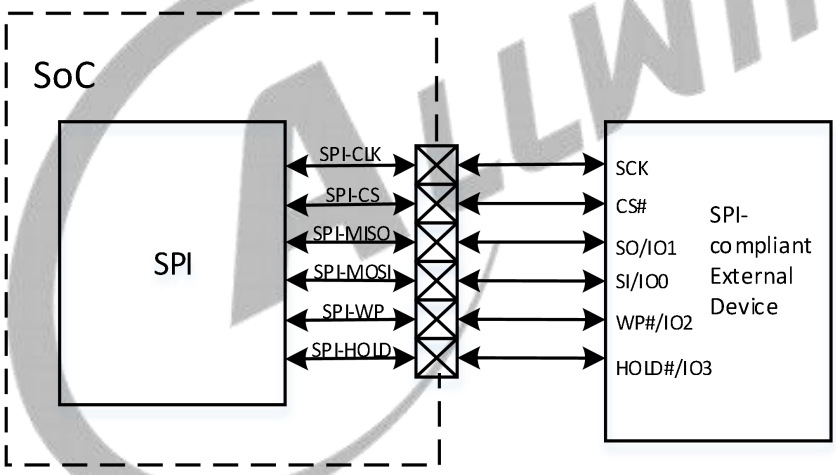
Table 8-42 SPI Clock Sources

SPI	Clock Sources	Description	Clock Module
SPI0, SPI2	HOSC	24 MHz Crystal	CCU
	PERI0_200M	Peripheral Clock, default value is 200 MHz.	
	PERI0_300M	Peripheral Clock, default value is 300 MHz.	
	PERI1_200M	Peripheral Clock, default value is 200 MHz.	
	PERI1_300M	Peripheral Clock, default value is 300 MHz.	
S_SPI0	DCXO24M	24 MHz Crystal	PRCM
	PERIPLL_DIV	Peripheral Clock, default value is 200 MHz.	
	PERI0_300M	Peripheral Clock, default value is 300 MHz.	
	PERI1_300M	Peripheral Clock, default value is 300 MHz.	
	AUDIO1PLL4X	Audio system clock, the defult value is 768 MHz.	

8.15.3.3 Typical Application

The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 8-64 SPI Application Block Diagram



8.15.3.4 SPI Transmit Format

The SPI supports 4 different formats for data transfer. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR (Offset: 0x0008). The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

The CPOL (SPI_TCR [1]) defines the polarity of the clock signal (SPI_SCLK). The SPI_SCLK is a high level when CPOL is '1' and it is a low level when CPOL is '0'. The CPHA (SPI_TCR [0]) decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used

to setup data when CPHA is '1', and sample data when CPHA is '0'. The following table lists the four modes.

Table 8-43 SPI Transmit Format

Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
Mode0	0	0	Sample on the rising edge	Setup on the falling edge
Mode1	0	1	Setup on the rising edge	Sample on the falling edge
Mode2	1	0	Sample on the falling edge	Setup on the rising edge
Mode3	1	1	Setup on the falling edge	Sample on the rising edge

The following figures describe four waveform for SPI_SCLK.

Figure 8-65 SPI Phase 0 Timing Diagram

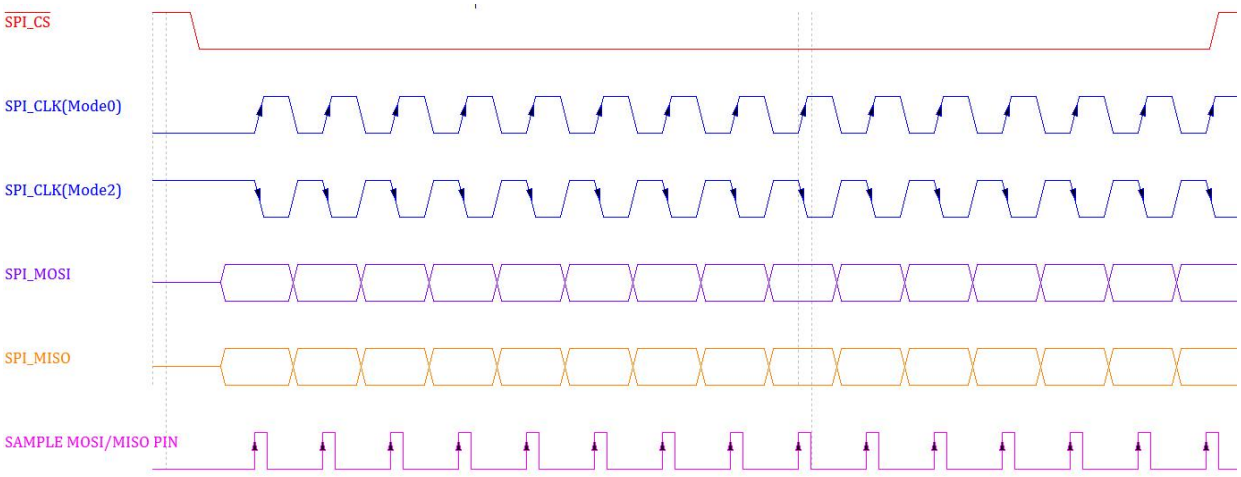
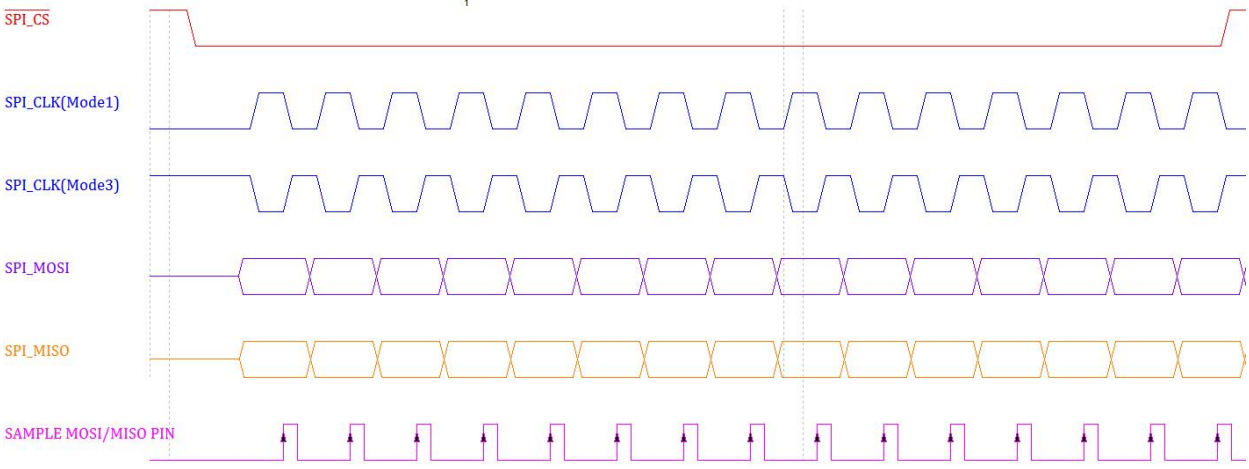


Figure 8-66 SPI Phase 1 Timing Diagram

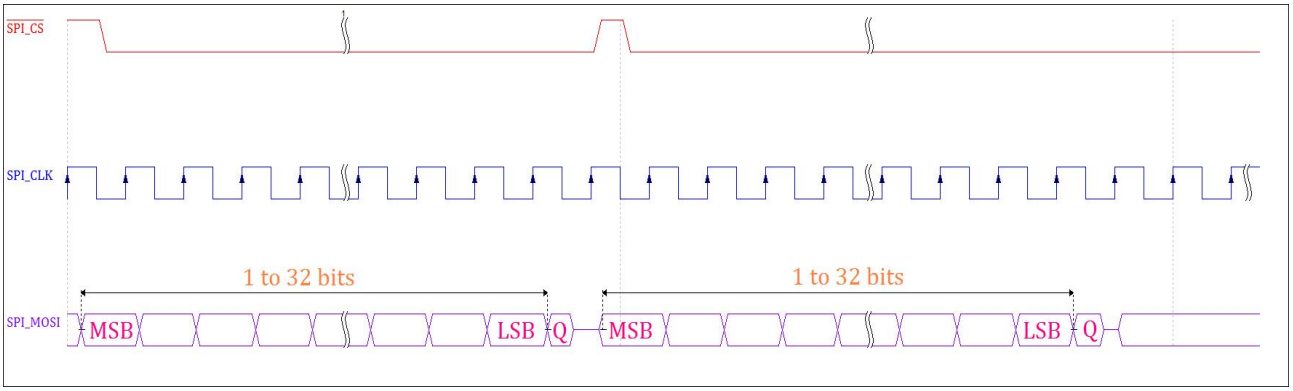


8.15.3.5 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATCR [1:0]) is equal to 0x2. And in the 3-wire mode, the

input data and the output data use the same single data line. The following figure describes the 3-wire mode.

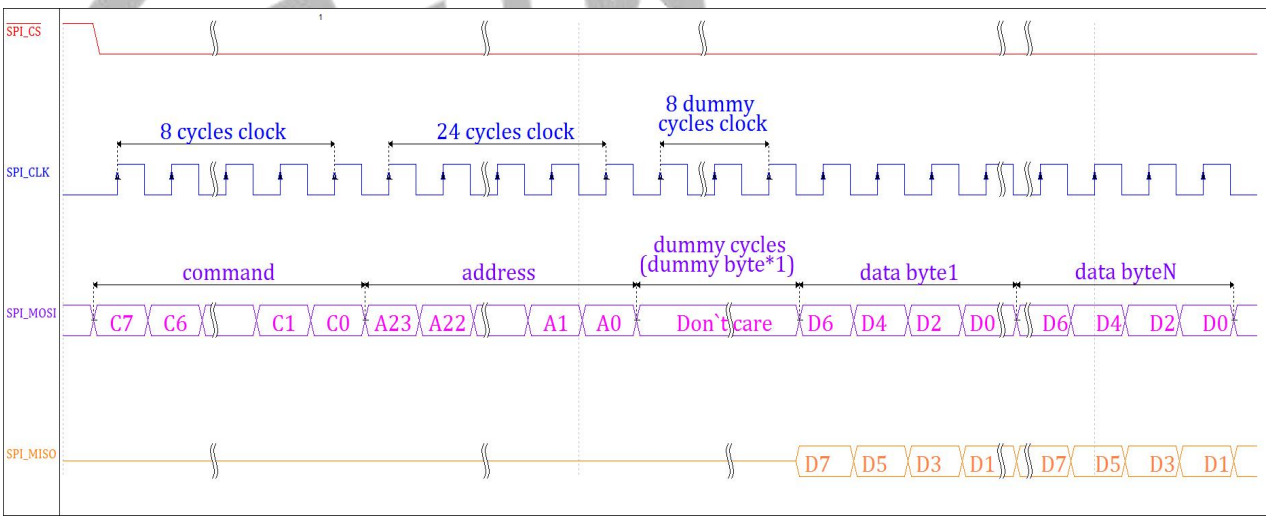
Figure 8-67 SPI 3-Wire Mode



8.15.3.6 SPI Dual-Input/Dual-Output and Dual I/O Mode

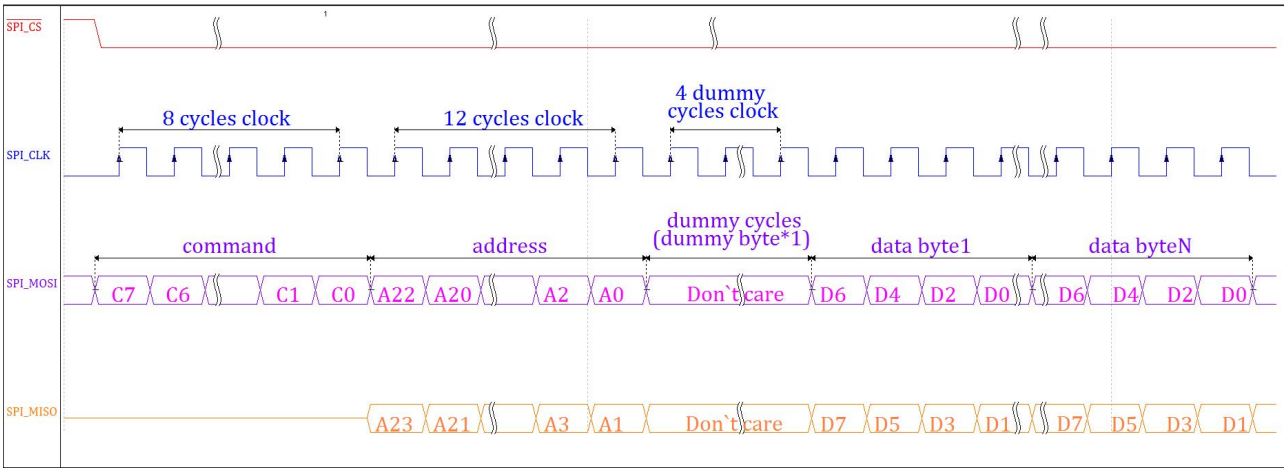
The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC (Offset: 0x0038) [28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI.

Figure 8-68 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 8-69 SPI Dual I/O Mode

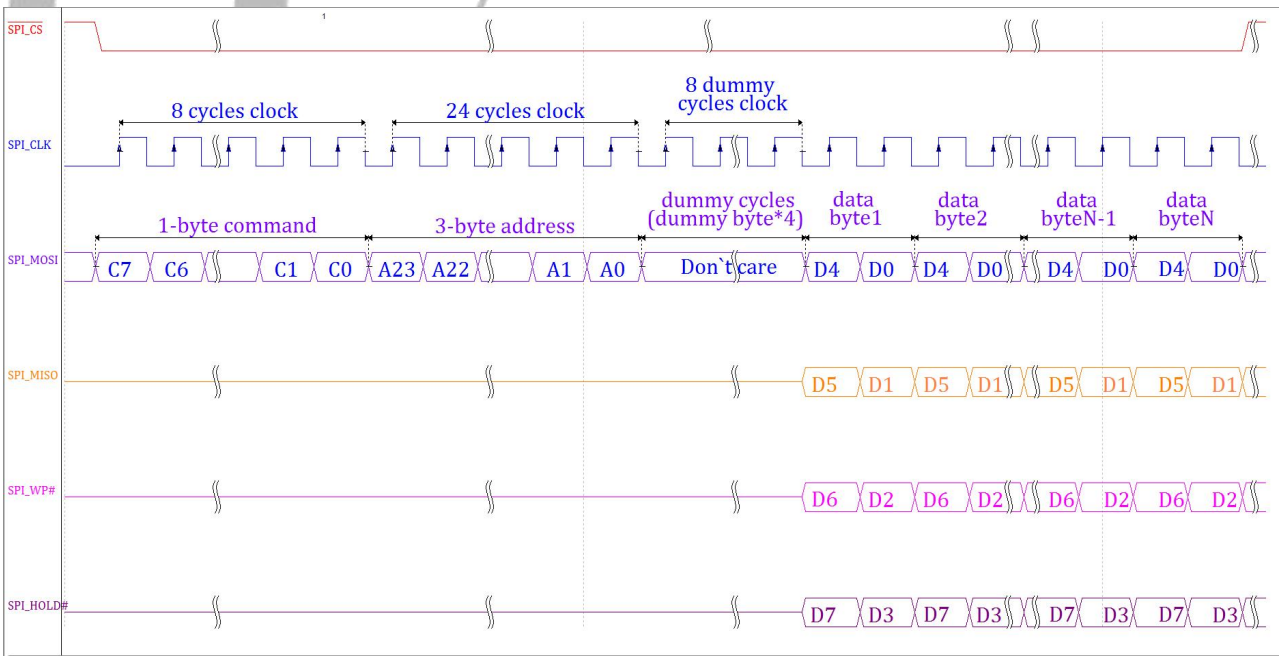


In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

8.15.3.7 SPI Quad-Input/Quad-Output Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC (Offset: 0x0038) [29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#) and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Figure 8-70 SPI Quad-Input/Quad-Output Mode



In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

8.15.3.8 Transmission/Reception Bursts in Master Mode

In SPI master mode, the transmission and reception bursts (byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmission bursts are written in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. The transmission bursts in single mode before automatically sending dummy bursts are written in STC (bit [23:0]) of the SPI Master Burst Control Counter Register. For dummy data, the SPI controller can automatically send before receiving by writing DBC (bit [27:24]) in the SPI Master Burst Control Counter Register. If users do not use the SPI controller to send dummy data automatically, then the dummy bursts are used as the transmission counters to write together in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. In master mode, the total burst numbers are written in MBC (bit [23:0]) of the SPI Master Burst Counter Register. When all transmission and reception bursts are transferred, the SPI controller will send a completed interrupt, at the same time, the SPI controller will clear DBC, MWTC, and MBC.

8.15.3.9 SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz–100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in the master mode. The SPI clock is selected from different clock sources, the SPI must configure different work mode. There are three work modes: normal sample mode, delay half-cycle sample mode, delay one-cycle sample mode. Delay half-cycle sample mode is the default mode of the SPI controller. When the SPI runs at 40 MHz or below 40 MHz, the SPI can work at normal sample mode or delay half-cycle sample mode. When the SPI runs over 80 MHz, setting the SDC bit in the SPI Transfer Control Register to '1' makes the internal read sample point with a half-cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. The following tables show the different configurations of the SPI sample mode.

Table 8-44 SPI Old Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24 MHz
delay half cycle sample	0	0	<=40 MHz
delay one cycle sample	0	1	>=80 MHz

CAUTION

The remaining spectrum is not recommended. Because when the output delay of SPI flash (refer to the datasheet of the manufactures for the specific delay time) is the same with the half-cycle time of SPI working clock, the variable edge of the output data for the device bumps into the clock sampling edge of the controller, so setting 1 cycle of sampling delay would cause stability problem.

Table 8-45 SPI New Sample Mode

SPI Sample Mode	SDM (bit13)	SDC (bit11)	SDC1 (bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

8.15.3.10 SPI Error Conditions

If any error conditions occur, the hardware will set the corresponding status bits in the SPI Interrupt Status Register (Offset: 0x0014) and stop the transfer. For the SPI controller, the following error scenarios can happen.

- TX_FIFO Underrun

The TX_FIFO underrun happens when the CPU/DMA reads data from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- TX_FIFO Overflow

The TX_FIFO overflow happens when the CPU/DMA writes data into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the TF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Underrun

The RX_FIFO underrun happens when the CPU/DMA reads data from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF

bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_UDF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

- RX_FIFO Overflow

The RX_FIFO overflow happens when the CPU/DMA writes data into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the SPI Interrupt Status Register (Offset: 0x0014). The SPI controller will generate an interrupt if interrupts are enabled. The software has to clear the error bit and the RF_OVF bit. To start a new transaction, the software has to reset the FIFO by writing to the SRST (soft reset) bit in the SPI Global Control Register (Offset: 0x0004).

8.15.4 Programming Guidelines

8.15.4.1 Writing/Reading Data Process

The SPI transfers serial data between the processor and the external device. The CPU mode and DMA mode are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX channel and RX channel. The TX channel has the path from TX FIFO to the external device. The RX channel has the path from the external device to RX FIFO.

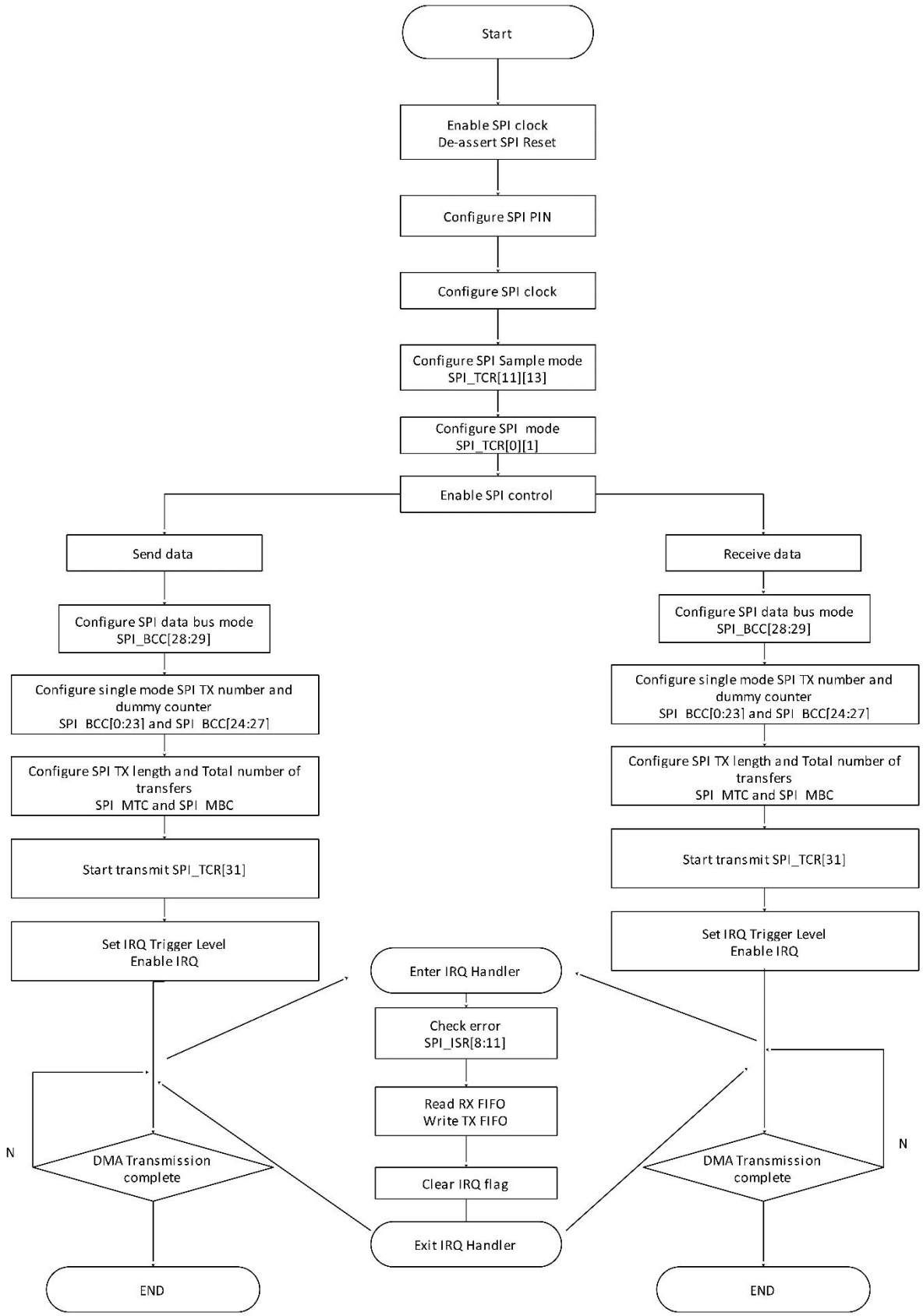
Write Data: The CPU or DMA must write data on the SPI_TXD (Offset: 0x0200), the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, the CPU or DMA must access the SPI_RXD (Offset: 0x0300) and the data are automatically sent to the SPI_RXD (Offset: 0x0300).

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor after each transmission is complete.

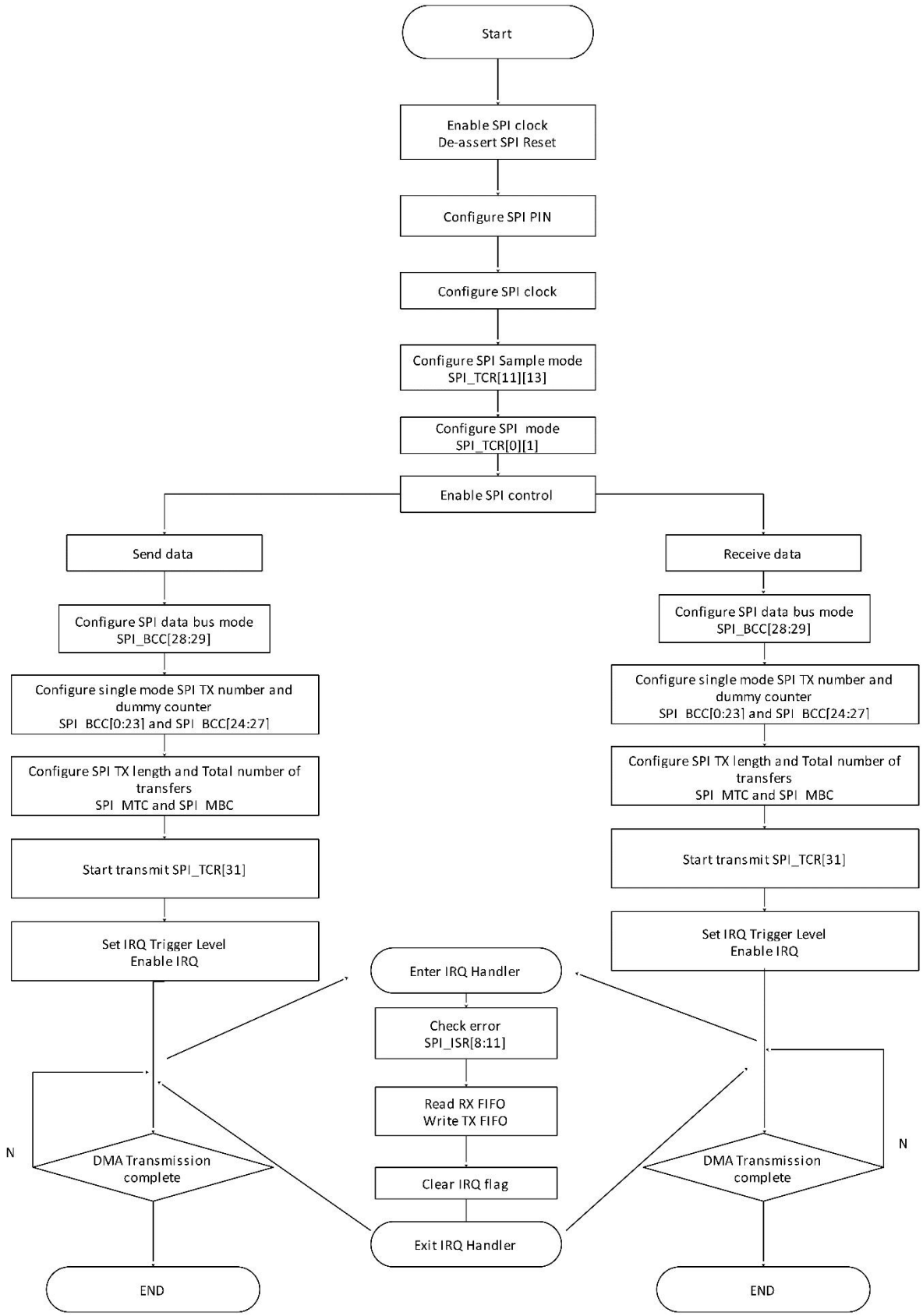
CPU Mode

Figure 8-71 SPI Write/Read Data in CPU Mode



DMA Mode

Figure 8-72SPI Write/Read Data in DMA Mode



8.15.5 Register List

Module Name	Base Address
SPI0	0x0402 5000
SPI2	0x0402 7000
S_SPI0	0x0709 2000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter register
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register
SPI_BSR	0x0400	SPI BUF Status register

8.15.6 Register Description

8.15.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
			In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: stop transmit data when RXFIFO full 0: normal operation, ignore RXFIFO status **Note: This bit cannot be written when XCH=1.**
6:3	/	/	/
2	R/W	0x0	MODE_SEL Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing **Note: This bit cannot be written when XCH=1.**
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode **Note: This bit cannot be written when XCH=1.**
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable **Note: After transforming from bit_mode to byte_mode, it must Enable the SPI Module again.**

8.15.6.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write “1” to SRST will also clear this bit. Write ‘0’ to this bit has no effect. **Note: This bit cannot be written when XCH=1.**
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
			Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point **Note: This bit cannot be written when XCH=1.**
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual I/O mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1 - Normal Sample Mode 0 - Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first **Note：Can't be written when XCH=1.**
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point **Note: This bit can't be written when XCH=1.**

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode Note: Can't be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one **Note: This bit can't be written when XCH=1.**
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. **Note: This bit can't be written when XCH=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: This bit can't be written when XCH=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: This bit can't be written when XCH=1.**
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
			10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: This bit can't be written when XCH=1.**
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts **Note: This bit can't be written when XCH=1.**
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: This bit can't be written when XCH=1.**
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: This bit can't be written when XCH=1.**
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) **Note: This bit can't be written when XCH=1.**

8.15.6.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
11	R/W	0x0	TF_UDR_INT_EN TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
			1: Enable

8.15.6.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, when set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W1C	0x0	TF_UDF TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
			overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL <= RX_TRIG_LEVEL 1: RX_WL > RX_TRIG_LEVEL This bit is set any time if RX_WL > RX_TRIG_LEVEL.

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
			Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.15.6.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, write to ‘0’ has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable In normal mode, TX FIFO can only be read by SPI controller, write ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don’t set in normal operation and don’t set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, write ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write ‘1’ to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don’t set in normal operation and don’t

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
			set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level CAUTION: Whether in CPU mode or in DMA mode, trigger level should be set properly that actual data amount reaches trigger level.

8.15.6.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO ... 64 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO + RX BUFFER 0: 0 byte in RX FIFO & RX BUFFER 1: 1 byte in RX FIFO & RX BUFFER ... 64: 64 bytes in RX FIFO & RX BUFFER ... 192:192bytes in RX FIFO & RX BUFFER other: Reserved

8.15.6.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch waits clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. **Note: This bit can't be written when XCH=1.**
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted Note: 1. Can't be written when XCH=1;

8.15.6.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

8.15.6.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst ... N: N bursts Note: (i) Can't be written when XCH=1; (ii) Total transfer data, include the TXD, RXD and dummy burst.

8.15.6.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

8.15.6.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
			1: Quad mode enable **Note:** • **Can't be written when XCH=1;** • **Quad mode includes Quad-Input and Quad-Output.**
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode **Note:** • **Can't be written when XCH=1;** • **It is only valid when Quad_Mode_EN=0.**
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don't care by the device. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

8.15.6.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
			serial bit's frame, it is only valid when Work Mode Select==0x10/0x11. 0: Idle 1: Initiates transfer. Write "1" to this bit will start to transfer serial bits' frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed **Note: It is only valid when Work Mode Select==0x10/0x11.**
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable **Note: It is only valid when Work Mode Select==0x10/0x11.**
23:22	/	/	/
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
			... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
15:14	/	/	/
13:8	R/W	0x00	TX_FRM_LEN Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: It is only valid when Work Mode Select= =0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
1:0	R/W	0x0	*WMS* *Work Mode Select* 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

8.15.6.13 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. Note: In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

8.15.6.14 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
			serial data frame. Note: In the process of transmission, the LSB is transmitted first. This register is only valid when Work Mode Select==0x10/0x11.

8.15.6.15 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: DMA_active is low 01: DMA_active is high 10: DMA_active is controlled by dma_request(DRQ) 11:DMA_active is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ACK 1: active fall must after detect ACK is high
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to dma_active high

8.15.6.16 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note: This address is writing-only if TF_TEST is '0',**

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
			and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.

8.15.6.17 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

8.15.6.18 0x0400 SPI BUF Status Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
15:8	/	/	/
7:0	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer

8.16 SPI_DBI

8.16.1 Overview

The A523 provides a 3/4 line SPI display bus interface (SPI_DBI) for video data transmission. It supports DBI mode or SPI mode. The DBI mode is compatible with multiple video data formats at the same time. The SPI mode is used for low-cost display schemes.

The SPI mode has the following features:

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
- Maximum clock frequency: 100MHz
- TX/RX DMA slave interface
- 8-bit wide by 64-entry FIFO for both transmitting and receiving data
- Supports mode0, mode1, mode2, and mode3
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

The DBI mode has the following features:

- DBI Type C 3 Line/4 Line Interface Mode
- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

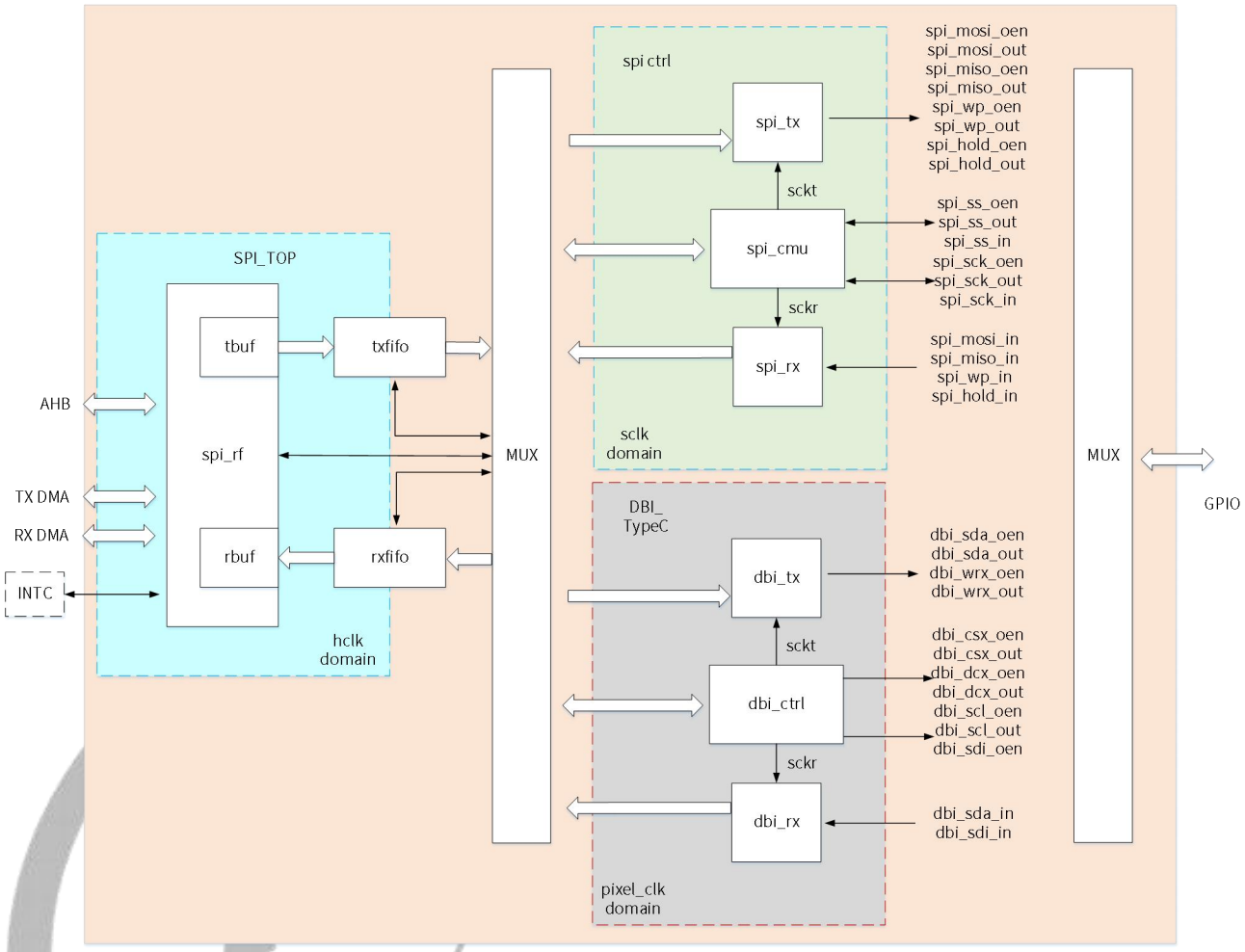
NOTE

This chapter only describes SPI1 (SPI mode and DBI mode). For detailed information of SPI0, SPI2, and S_SPI0, please refer to section 8.15 SPI.

8.16.2 Block Diagram

The following figure shows a block diagram of the SPI_DBI.

Figure 8-73 SPI_DBI Block Diagram



SPI_DBI contains the following sub-blocks:

Table 8-46 SPI_DBI Sub-blocks

Sub-block	Description
spi_rf	Responsible for implementing the internal register, interrupt, and DMA Request.
spi_tbuf	The data length transmitted from AHB to TXFIFO is converted into 8 bits, then the data is written into the RXFIFO.
spi_rbuf	The block is used to convert the RXFIFO data into the reading data length of AHB.
txfifo, rxfifo	The data transmitted from the SPI to the external serial device is written into the TXFIFO; the data received from the external serial device into SPI is pushed into the RXFIFO.
spi_cmu	Responsible for implementing SPI bus clock, chip select, internal sample, and

Sub-block	Description
	the generation of transfer clock.
spi_tx	Responsible for implementing SPI data transfer, the interface of the internal TXFIFO, and status register.
spi_rx	Responsible for implementing SPI data receive, the interface of the internal RXFIFO, and status register.
dbi_ctrl	Responsible for implementing DBI bus clock, chip select, data command select, RGB format reshape.
dbi_tx	Responsible for implementing DBI data transfer, the interface of the internal TXFIFO, and status register.
dbi_rx	Responsible for implementing DBI data receive, the interface of the internal RXFIFO, and status register.

8.16.3 Functional Description

8.16.3.1 External Signals

The following table describes the external signals of SPI_DBI. When using SPI_DBI, the corresponding PADs are selected as SPI_DBI function via section 8.5 GPIO.

Table 8-47 GPIO multiplexing of SPI1 and DBI

DBI	SPI1
DBI-CSX	SPI1-CS0
DBI-SCLK	SPI1-CLK
DBI-SDO	SPI1-MOSI
DBI-SDI/ DBI-TE/ DBI-DCX	SPI1-MISO
DBI-DCX/DBI-WRX	SPI1-HOLD
DBI-TE	SPI1-WP

Table 8-48 SPI_DBI External Signals

Signal Name	Description	Type
SPI Mode		
SPI1-CS0	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal Provides serial interface timing.	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-HOLD	SPI1 Hold Signal	I/O

Signal Name	Description	Type
	Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	
DBI Mode		
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

8.16.3.2 Clock Sources

The SPI_DBI controller gets 5 different clock sources, users can select one of them to make SPI_DBI clock source. The following table describes the clock sources for SPI_DBI. For more details on the clock setting, configuration, and gating information, see section 2.5 Clock Controller Unit (CCU).

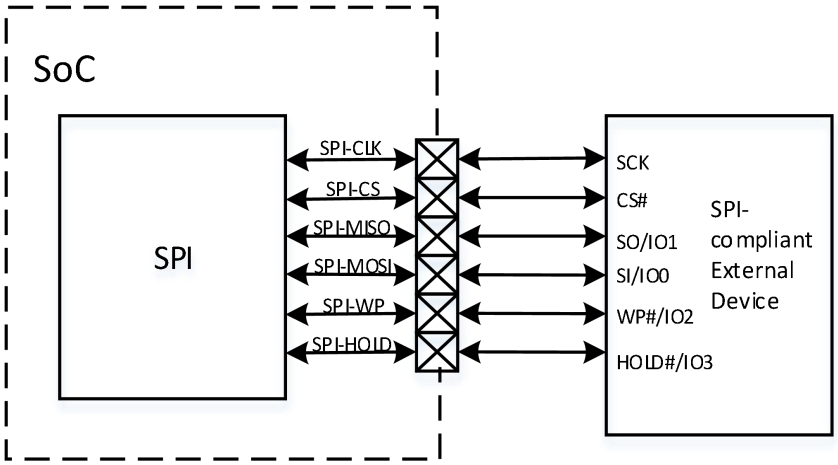
Table 8-49 SPI_DBI Clock Sources

Clock Sources	Description	Clock Module
HOSC	24 MHz Crystal	CCU
PERI0_200M	Peripheral Clock, default value is 200 MHz.	
PERI0_300M	Peripheral Clock, default value is 300 MHz.	
PERI1_200M	Peripheral Clock, default value is 200 MHz.	
PERI1_300M	Peripheral Clock, default value is 300 MHz.	

8.16.3.3 Typical Application

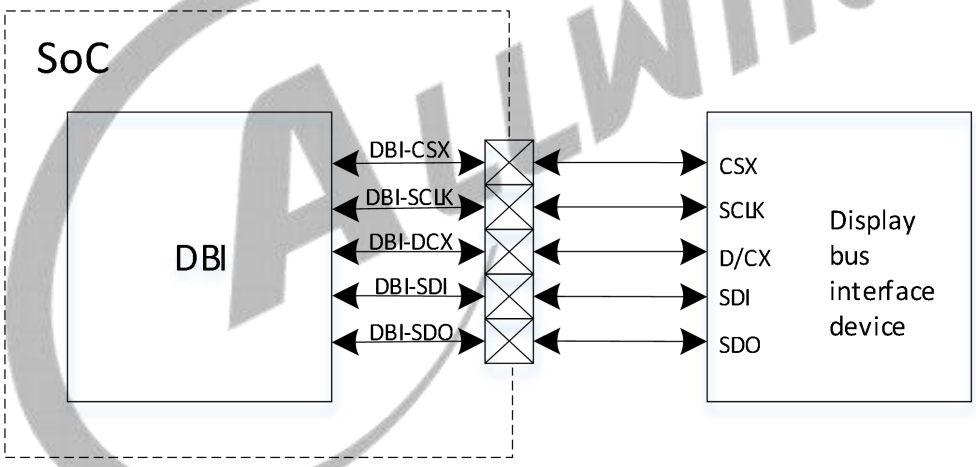
The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 8-74 SPI Application Block Diagram



The following figure shows the application block diagram when the DBI master device is connected to a display bus interface device.

Figure 8-75 DBI Application Block Diagram



8.16.3.4 SPI Transmission Format

The SPI supports 4 different formats for data transmission. The software can select one of the four modes in which the SPI works by setting the bit1 (Polarity) and bit0 (Phase) of SPI_TCR. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

The CPOL (SPI_TCR[1]) defines the polarity of the clock signal (SPI_SCLK). The SPI_SCLK is a high level when CPOL is '1' and it is a low level when CPOL is '0'. The CPHA (SPI_TCR[0]) decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used to setup data when CPHA is '1', and sample data when CPHA is '0'. The following table lists the four modes.

Table 8-50 SPI Transmit Format

SPI Mode	Polarity (CPOL)	Phase (CPHA)	Leading Edge	Trailing Edge
mode0	0	0	Sample on the rising edge	Setup on the falling edge
mode1	0	1	Setup on the rising edge	Sample on the falling edge
mode2	1	0	Sample on the falling edge	Setup on the rising edge
mode3	1	1	Setup on the falling edge	Sample on the rising edge

The following figures describe four waveforms for SPI_SCLK.

Figure 8-76 SPI Phase 0 Timing Diagram

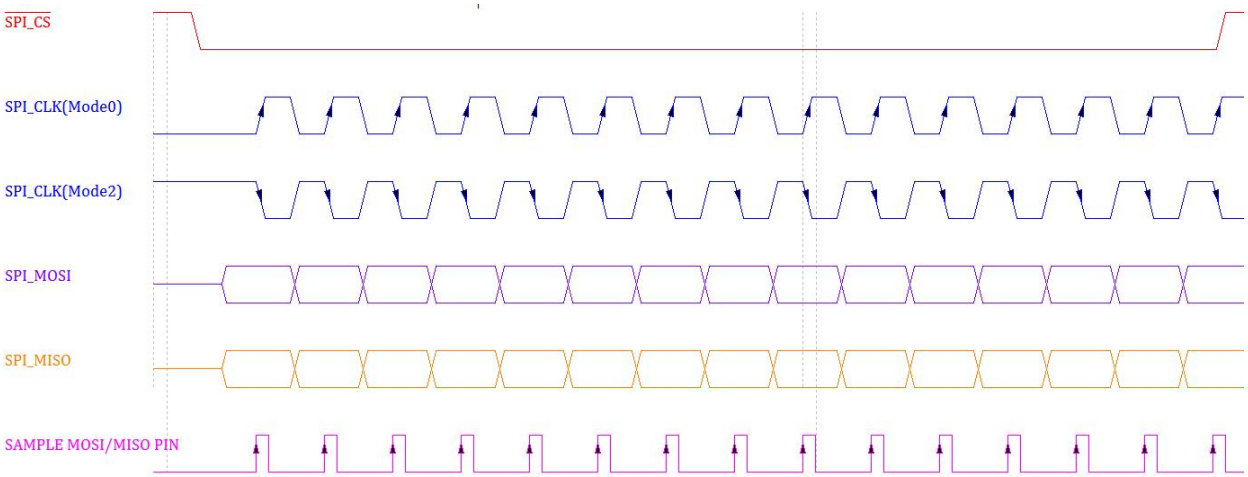
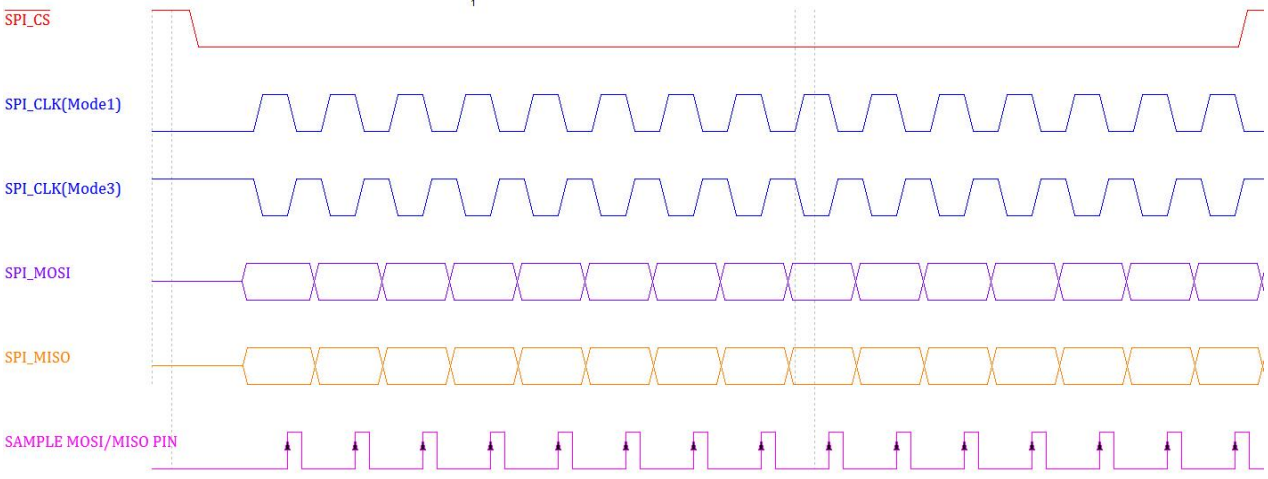


Figure 8-77 SPI Phase 1 Timing Diagram



8.16.3.5 SPI Master and Slave Mode

The SPI controller can be configured to a master or slave device. The master mode is selected by setting the MODE bit (SPI_GCR[1]); the slave mode is selected by clearing the MODE bit.

In master mode, the SPI_CLK is generated and transmitted to the external device, and the data from the TX FIFO is transmitted on the MOSI pin, the data from the slave is received on the MISO pin and sent to RX FIFO. The Chip Select (SPI_SS) is an active low signal, and it must be set low

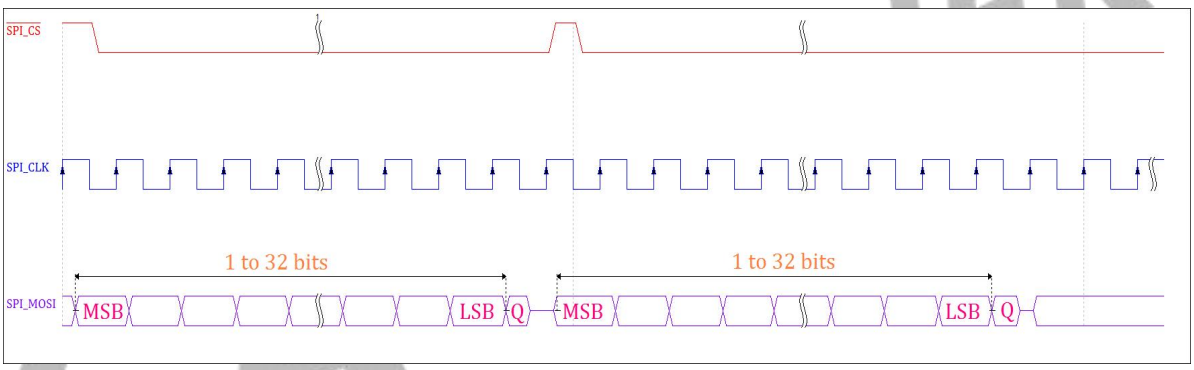
before the data are transmitted or received. The SPI_SS can be selected the auto control mode or the software manual control mode. When using auto control, the SS_OWNER (SPI_TCR[6]) must be cleared (default value is 0); when using manual control, the SS_OWNER must be set. And the level of SPI_SS is controlled by SS_LEVEL (SPI_TCR[7]).

In slave mode, after the software selects the MODE bit (SPI_GCR [1]) to '0', it waits for master initiate a transaction. When the master asserts SPI_SS, and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on the MISO pin, and the data from the MOSI pin is received in RX FIFO.

8.16.3.6 SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the Work Mode Select bit (SPI_BATC [1:0]) is equal to 0x2. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes the 3-wire mode.

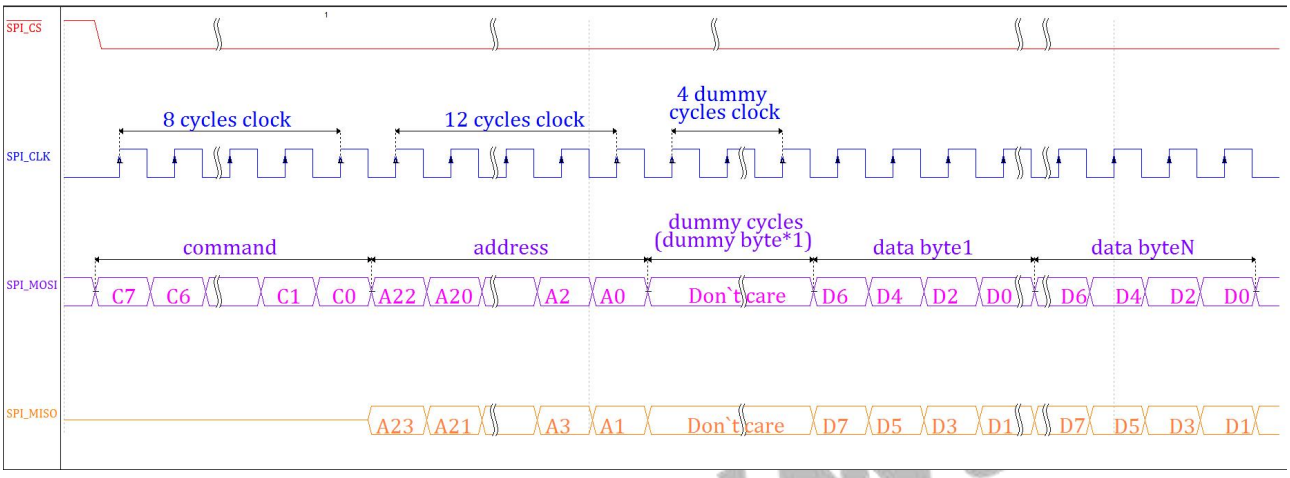
Figure 8-78 SPI 3-Wire Mode



8.16.3.7 SPI Dual-Input/Dual-Output and Dual I/O Mode

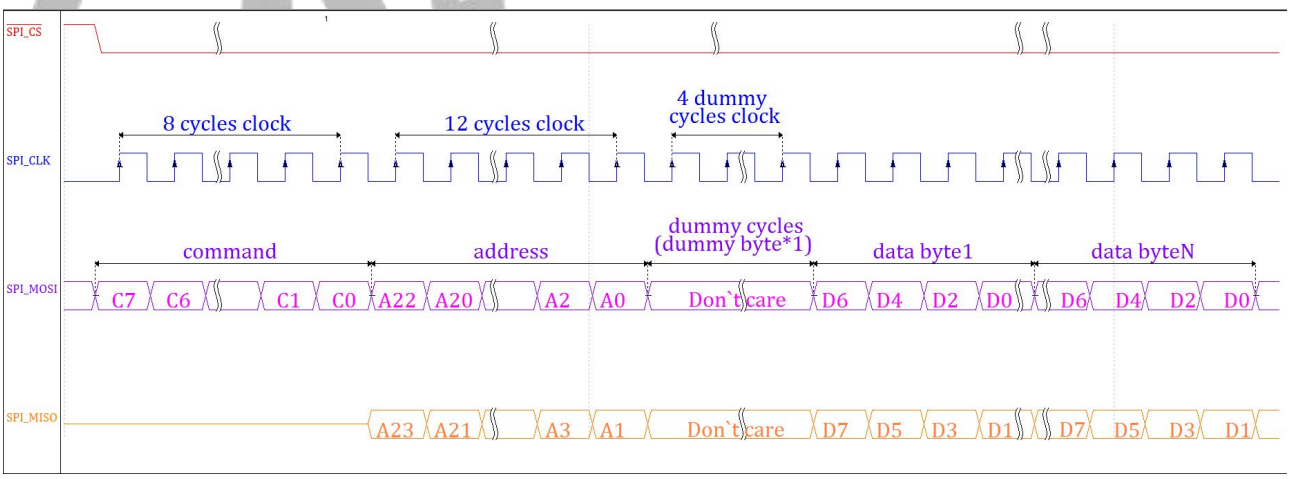
The dual read mode (SPI x2) is selected when the DRM is set in SPI_BCC [28]. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode SPI devices, the data can be read at fast speed using two data bits (MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI and the dual I/O SPI

Figure 8-79 SPI Dual-Input/Dual-Output Mode



In the dual-input/dual-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line, only the data bytes are output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 8-80 SPI Dual I/O Mode

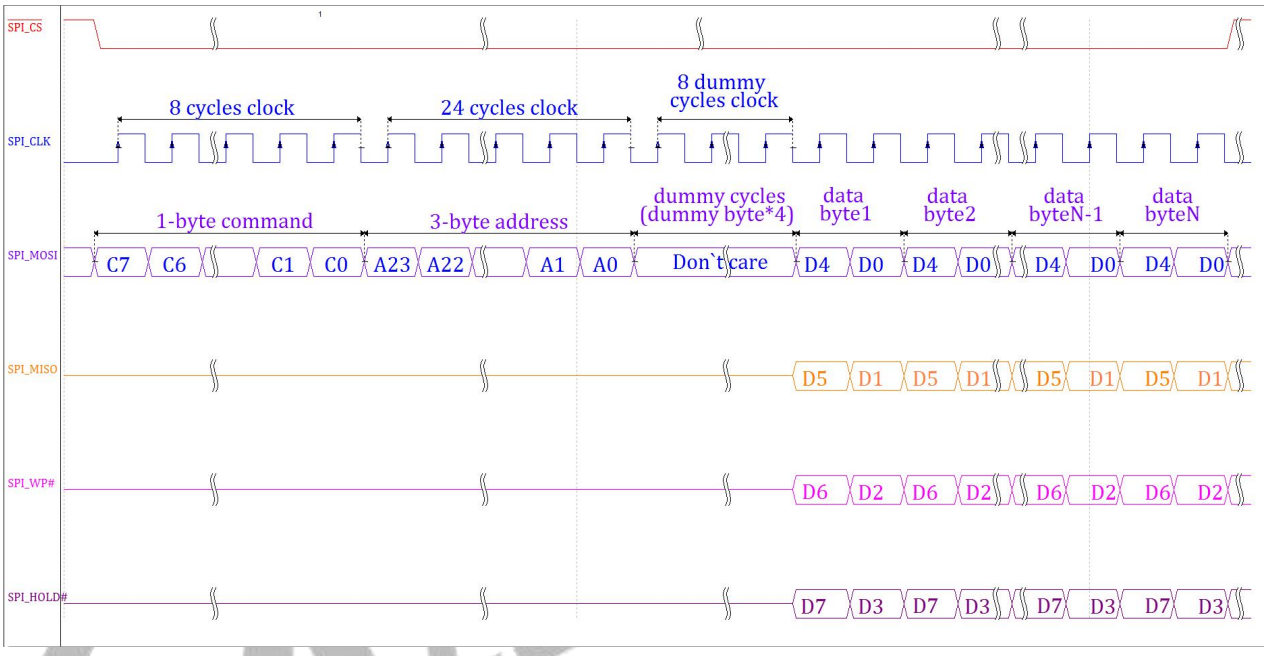


In the dual I/O SPI mode, only the command bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. The address bytes and the dummy bytes output in a unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes output (write) and input (read) in a unit of dual bits through the SPI_MOSI and SPI_MISO.

8.16.3.8 SPI Quad-Input/Quad-Output Mode

The quad read mode (SPI x4) is selected when the Quad_EN is set in SPI_BCC [29]. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, the data can be read at fast speed using four data bits (MOSI, MISO, IO2 (WP#) and IO3 (HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

Figure 8-81 SPI Quad-Input/Quad-Output Mode



In the quad-input/quad-output SPI mode, the command, address, and the dummy bytes output in a unit of a single bit in serial mode through the SPI_MOSI line. Only the data bytes output (write) and input (read) in a unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP#, and SPI_HOLD#.

8.16.3.9 Transmission/Reception Bursts in Master Mode

In SPI master mode, the transmission and reception bursts (byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmission bursts are written in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. The transmission bursts in single mode before automatically sending dummy bursts are written in STC (bit [23:0]) of the SPI Master Burst Control Counter Register. For dummy data, the SPI controller can automatically send before receiving by writing DBC (bit [27:24]) in the SPI Master Burst Control Counter Register. If users do not use the SPI controller to send dummy data automatically, then the dummy bursts are used as the transmission counters to write together in MWTC (bit [23:0]) of the SPI Master Transmit Counter Register. In master mode, the total burst numbers are written in MBC (bit [23:0]) of the SPI Master Burst Counter Register. When all transmission and reception bursts are transferred, the SPI controller will send a completed interrupt, at the same time, the SPI controller will clear DBC, MWTC, and MBC.

8.16.3.10 SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz–100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in the master mode. The SPI clock is selected from different clock sources, the SPI must configure different work mode. There are three work modes: normal sample mode, delay half-cycle sample mode, delay one-cycle sample mode. Delay half-cycle sample mode is the default mode of the SPI controller. When the SPI runs at 40 MHz or below 40 MHz, the SPI can work at normal sample mode or delay half-cycle sample mode. When the SPI runs over 80 MHz, setting the SDC bit in the SPI Transfer Control Register to '1' makes the internal read sample point with a half-cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK between master and slave. The following tables show the different configurations of the SPI sample mode.

Table 8-51 SPI Old Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24 MHz
delay half cycle sample	0	0	<=40 MHz
delay one cycle sample	0	1	>=80 MHz

CAUTION

The remaining spectrum is not recommended. Because when the output delay of SPI flash (refer to the datasheet of the manufactures for the specific delay time) is the same with the half-cycle time of SPI working clock, the variable edge of the output data for the device bumps into the clock sampling edge of the controller, so setting 1 cycle of sampling delay would cause stability problem.

Table 8-52 SPI New Sample Mode

SPI Sample Mode	SDM (bit13)	SDC (bit11)	SDC1 (bit15)
normal sample	1	0	0
delay half cycle sample	0	0	0
delay one cycle sample	0	1	0
delay 1.5 cycle sample	1	1	0
delay 2 cycle sample	1	0	1
delay 2.5 cycle sample	0	0	1
delay 3 cycle sample	0	1	1

8.16.3.11 DBI 3-Line Interface Writing and Reading Timing

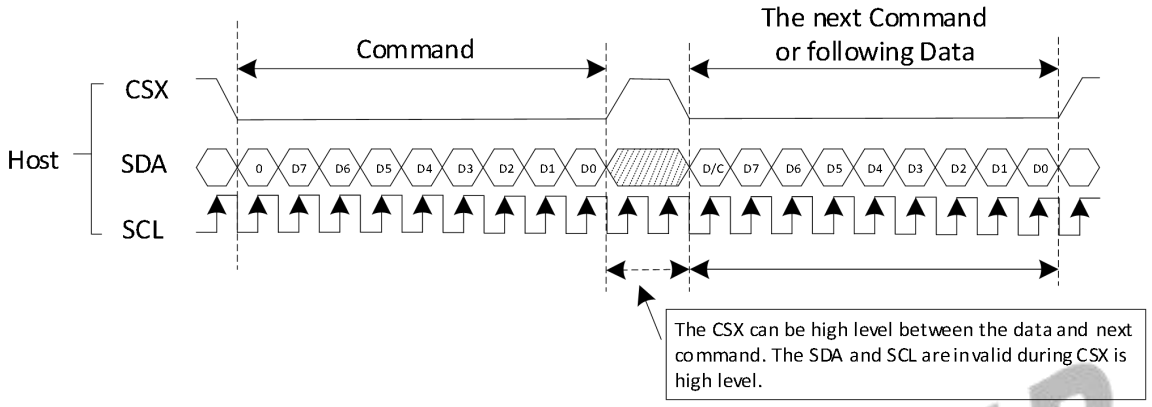
The 3-line DBI Interface I contains CSX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 3-line DBI Interface II contains CSX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

Since the 3-line display bus mode has no Data/Command data line indicating whether Data or Command is currently being transmitted, an extra bit is added to the data-stream before MSB to indicate whether Data or Command is currently being transmitted. (0: Command, 1: Data)

The following figure shows the writing operation format of 3-line DBI Interface I and Interface II.

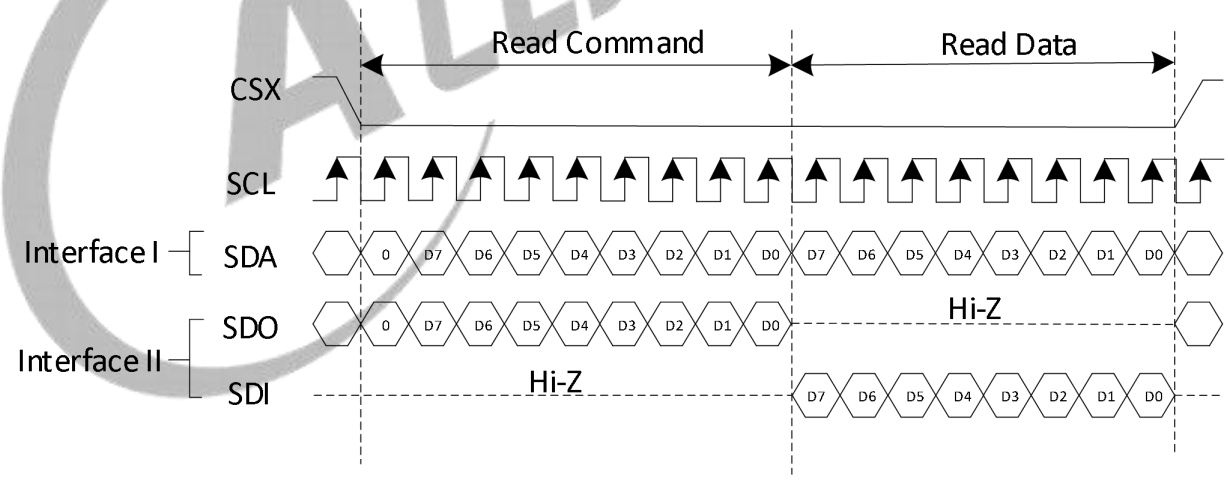
Figure 8-82 DBI 3-Line Display Bus Serial Interface Writing Operation Format



The 3-line DBI Interface I uses the SDA port as bidirectional data input and output port. There are only three cases of data reading volume, 8bits/24bits/32bits, and the first data sampled is high.

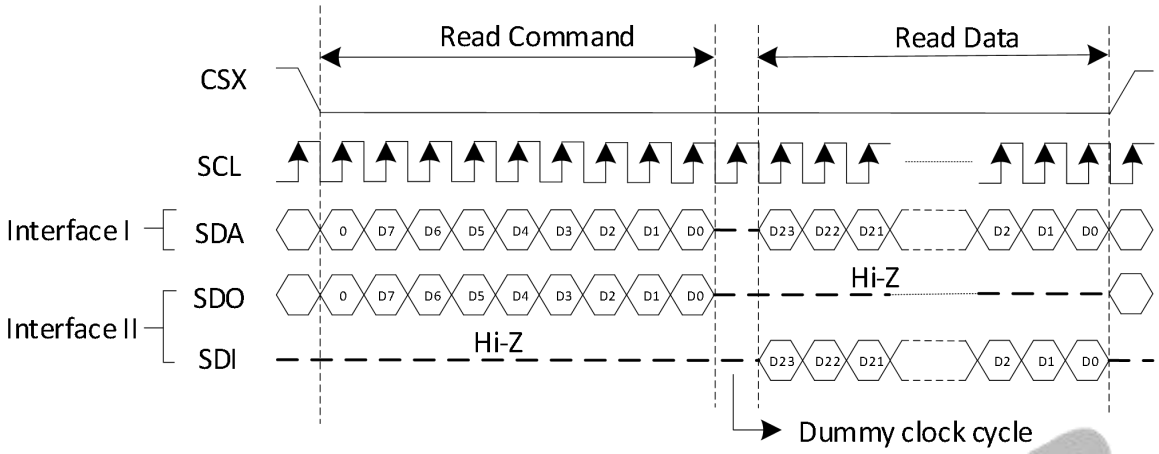
The following figure shows the 8 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read immediately with on dummy period.

Figure 8-83 DBI 3-Line Display Bus Serial Interface 8-bit Reading Operation Format



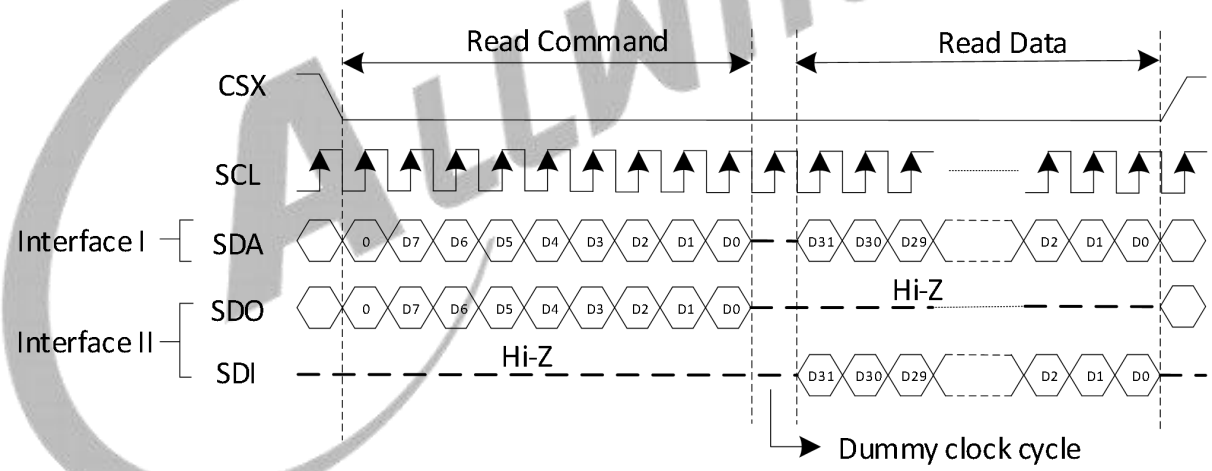
The following figure shows the 24 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read after waiting for the dummy clock cycle.

Figure 8-84 DBI 3-Line Display Bus Serial Interface 24-bit Reading Operation Format



The following figure shows the 32 bits reading operation format of 3-line DBI Interface I and Interface II. After the read command is transmitted, the data is read after waiting for the dummy clock cycle.

Figure 8-85 DBI 3-Line Display Bus Serial Interface 32-bit Reading Operation Format



8.16.3.12 DBI 4-Line Interface Writing and Reading Timing

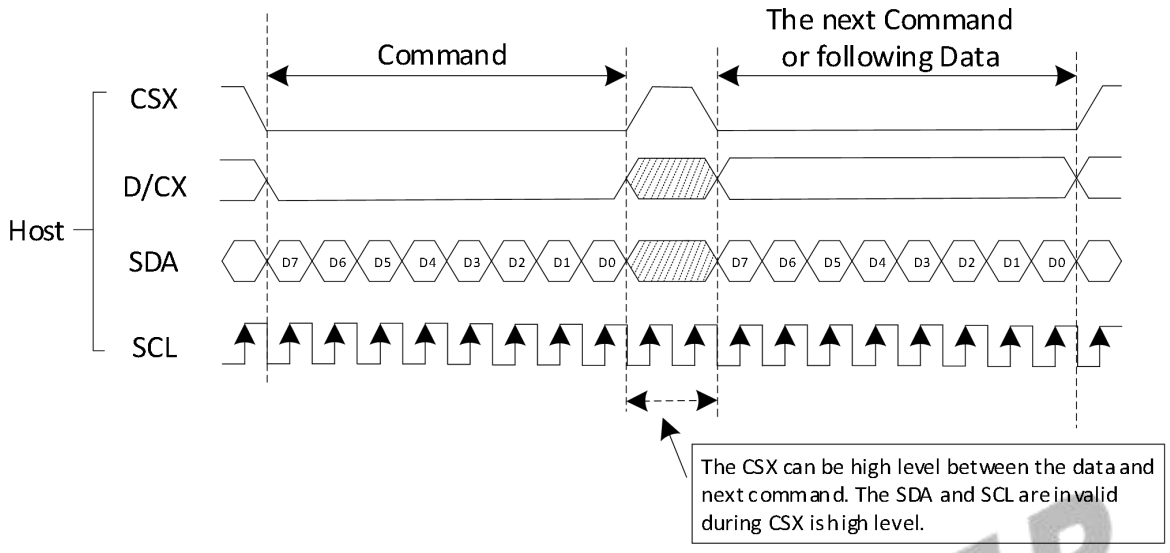
The 4-line DBI Interface I contains CSX, D/CX, SDA, and SCL, where SDA shares this port for bidirectional port data input and output.

The 4-line DBI Interface II contains CSX, D/CX, SDA, SCL, and SDI; Data input and output ports are independent of each other.

Since the 4-line display bus mode has a Data/Command data line indicating whether Data or Command is currently being transmitted (0: Command, 1: Data). So there is no need to add an extra bit to data-stream before MSB like the 3-line DBI.

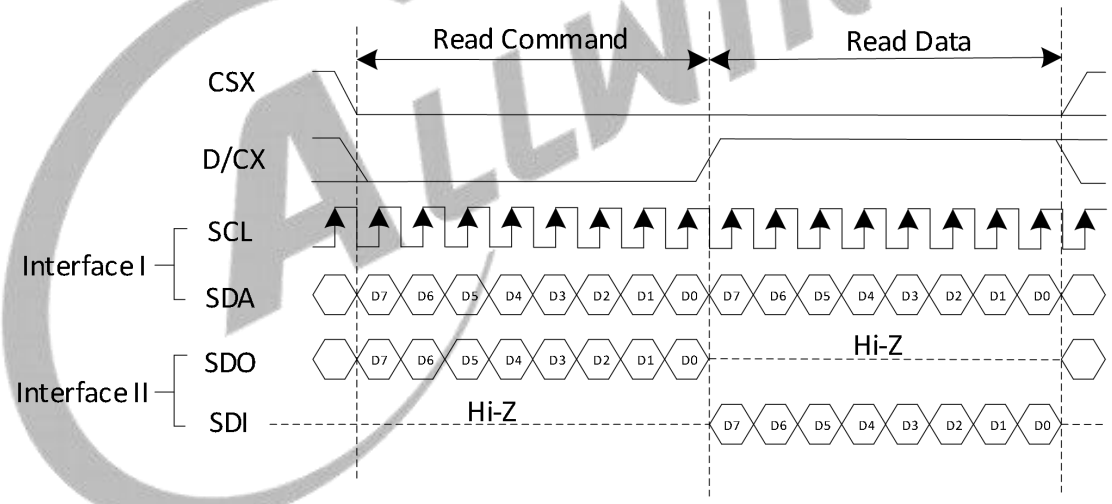
The following figure shows the writing operation format of 4-line DBI Interface I and Interface II.

Figure 8-86 DBI 4-Line Display Bus Serial Interface Writing Operation Format



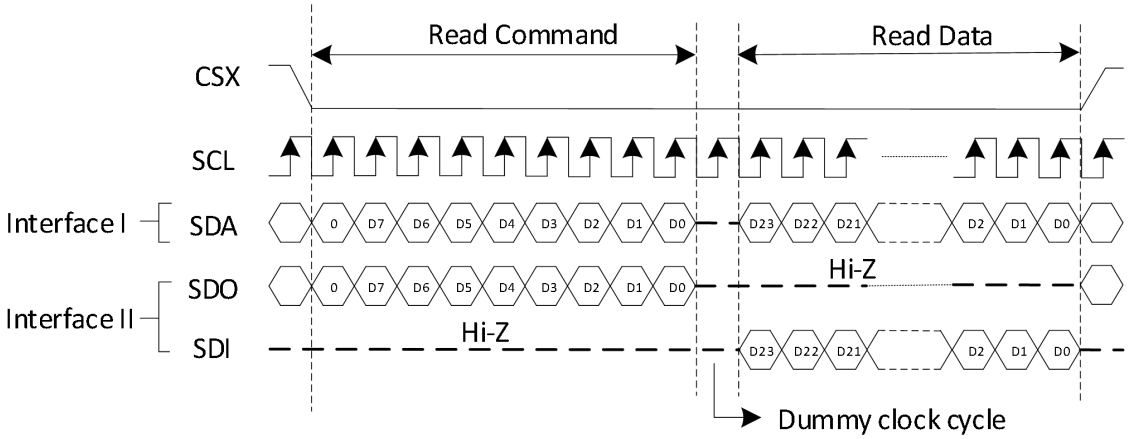
The following figure shows the 8 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 8-87 DBI 4-Line Display Bus Serial Interface 8-bit Reading Operation Format



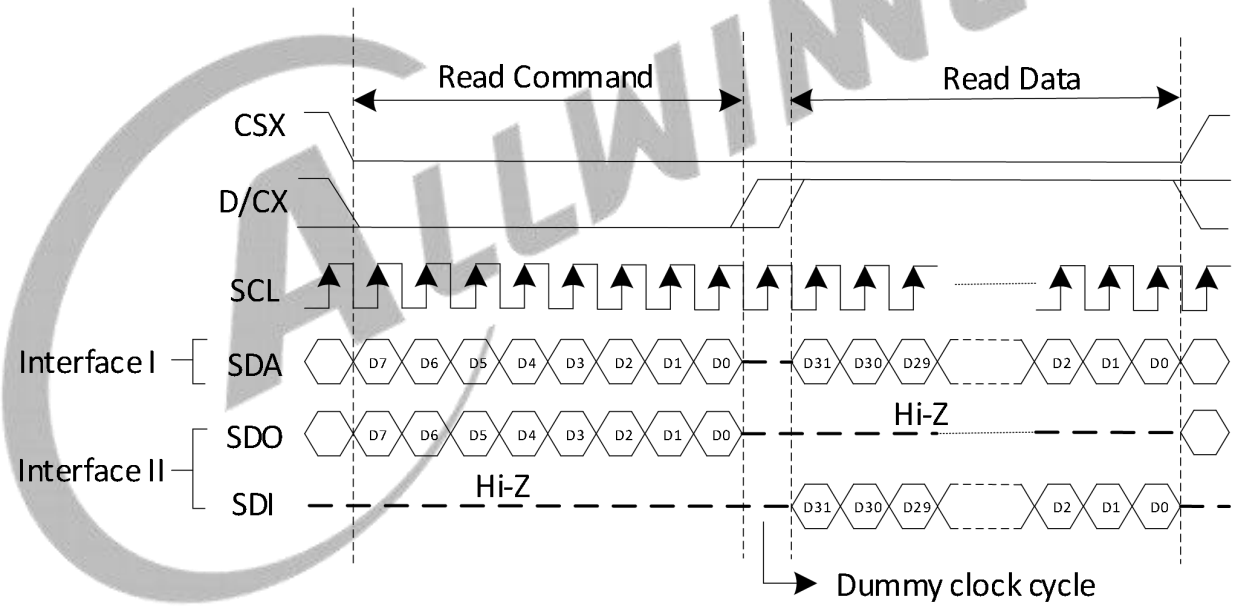
The following figure shows the 24 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 8-88 DBI 4-Line Display Bus Serial Interface 24-bit Reading Operation Format



The following figure shows the 32 bits reading operation format of 4-line DBI Interface I and Interface II.

Figure 8-89 DBI 4-Line Display Bus Serial Interface 32-bit Reading Operation Format



8.16.3.13 DBI 3-Line Interface Transmit Video Format

Figure 8-90 RGB111 3-Line Interface Transmit Video Format

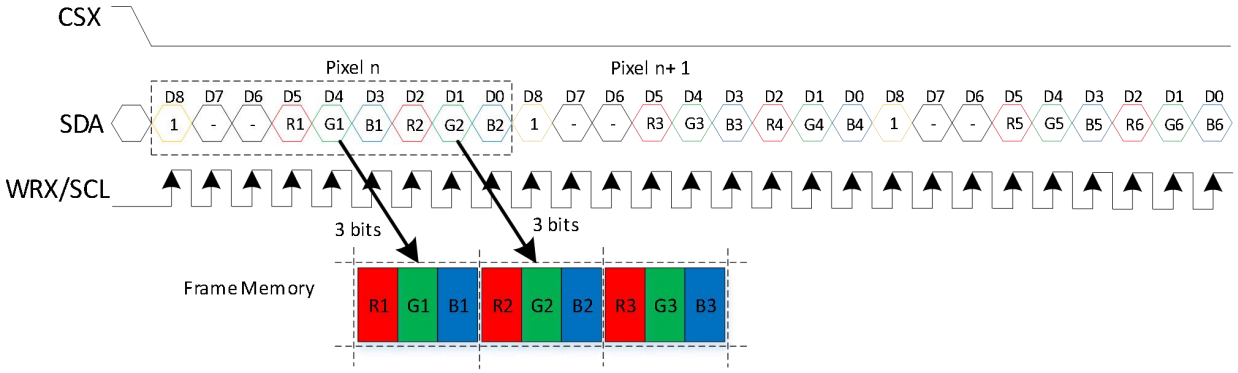
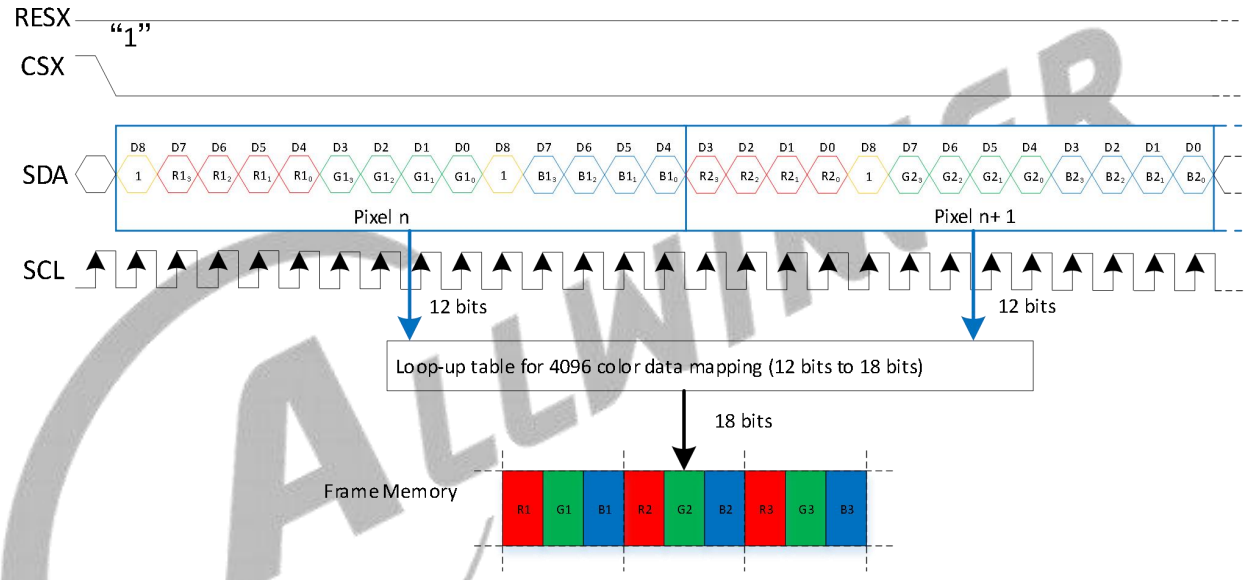
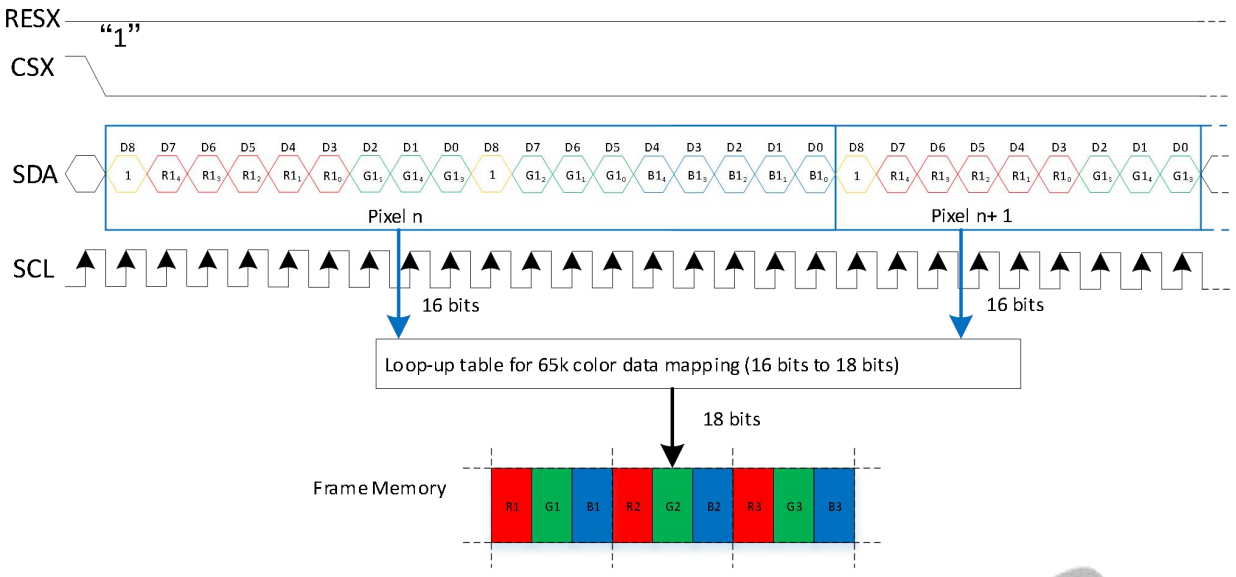


Figure 8-91 RGB444 3-Line Interface Transmit Video Format



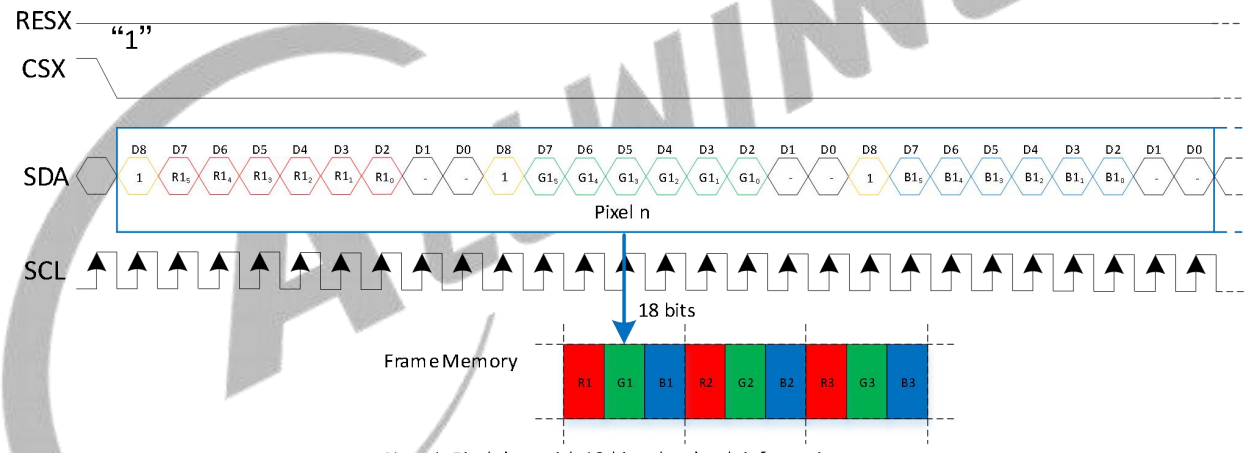
Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-92 RGB565 3-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-93 RGB666 3-Line Interface Transmit Video Format



Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.16.3.14 DBI 4-Line Interface Transmit Video Format

Figure 8-94 RGB111 4-Line Interface Transmit Video Format

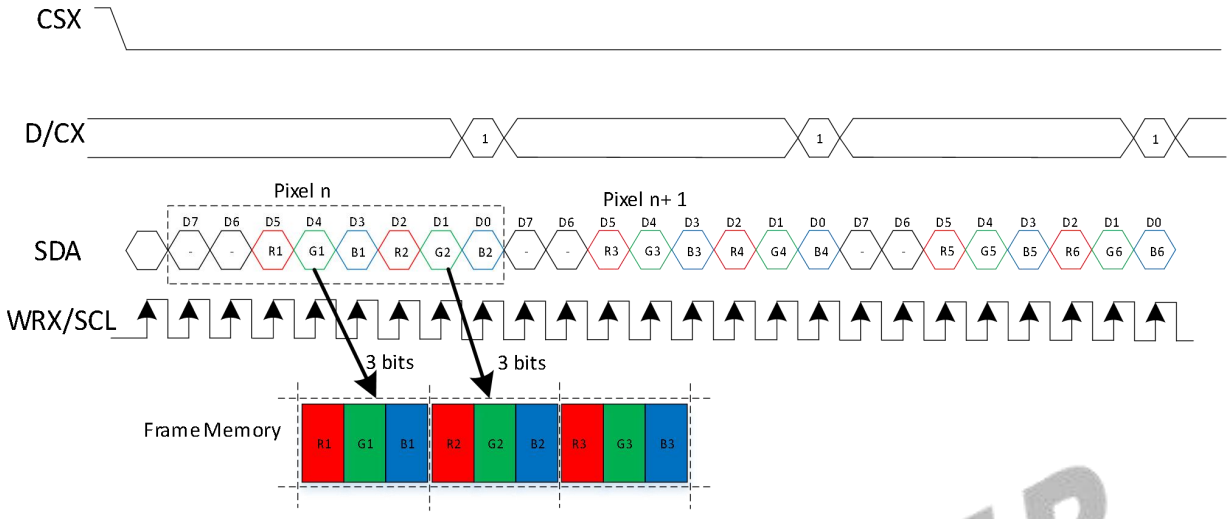
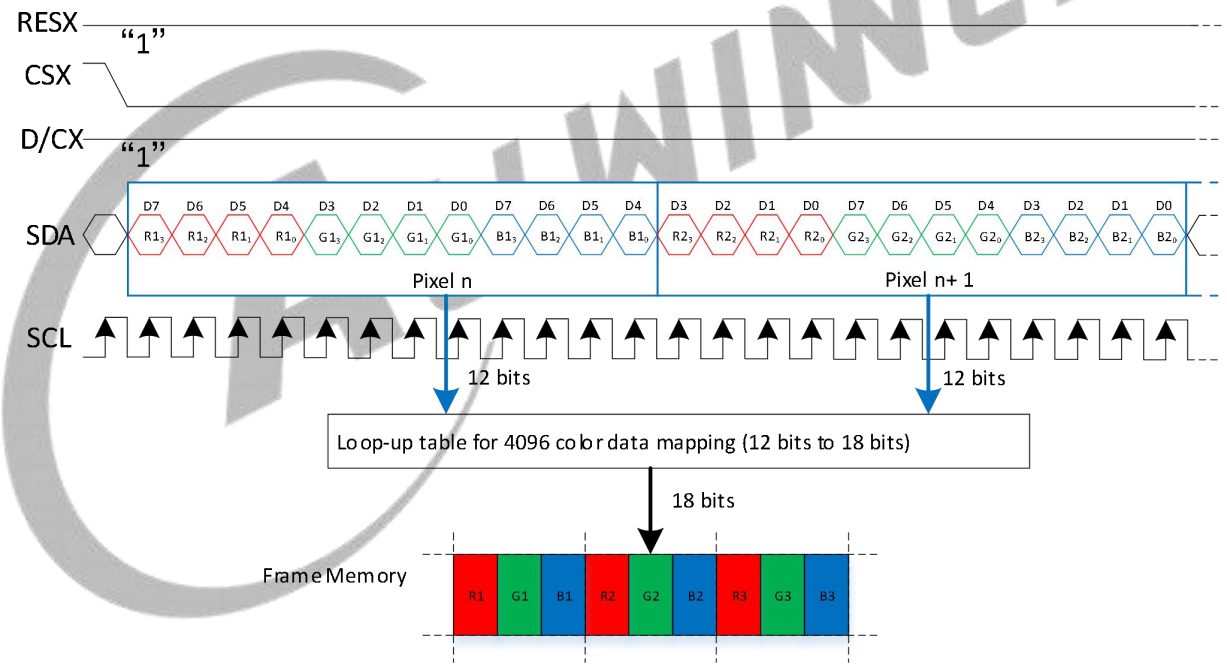
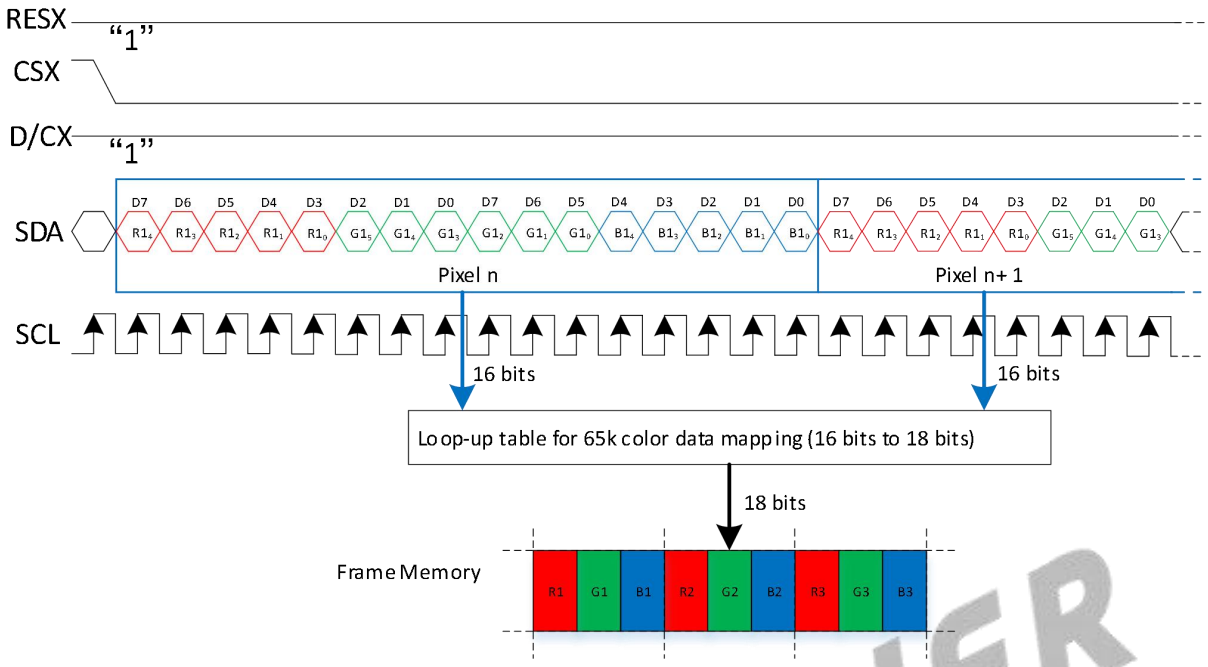


Figure 8-95 RGB444 4-Line Interface Transmit Video Format



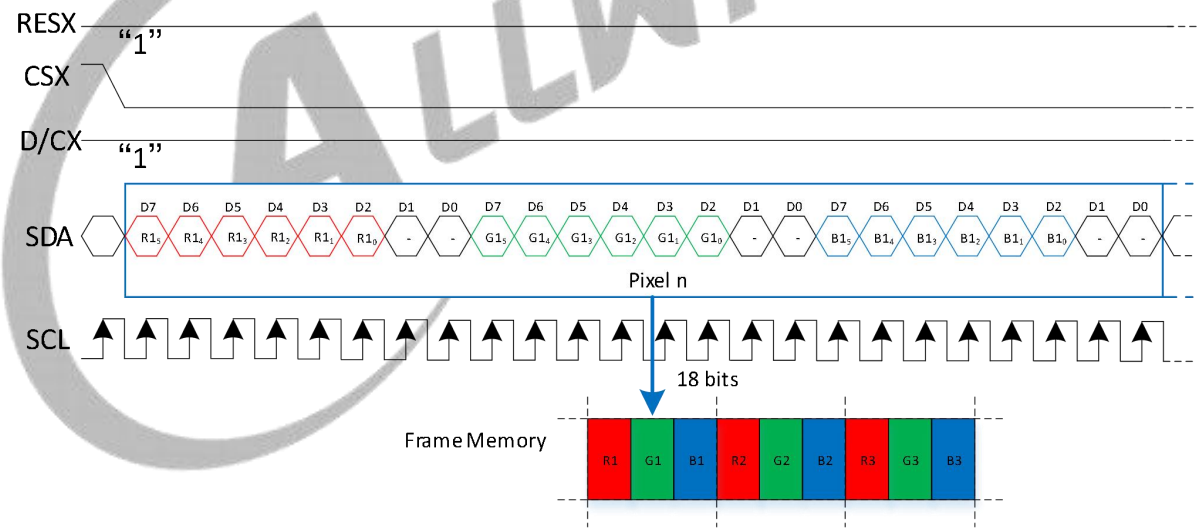
Note 1. Pixel data with 12-bit color depth information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-96 RGB565 4-Line Interface Transmit Video Format



Note 1. Pixel data with 16-bit color depth information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-97 RGB666 4-Line Interface Transmit Video Format

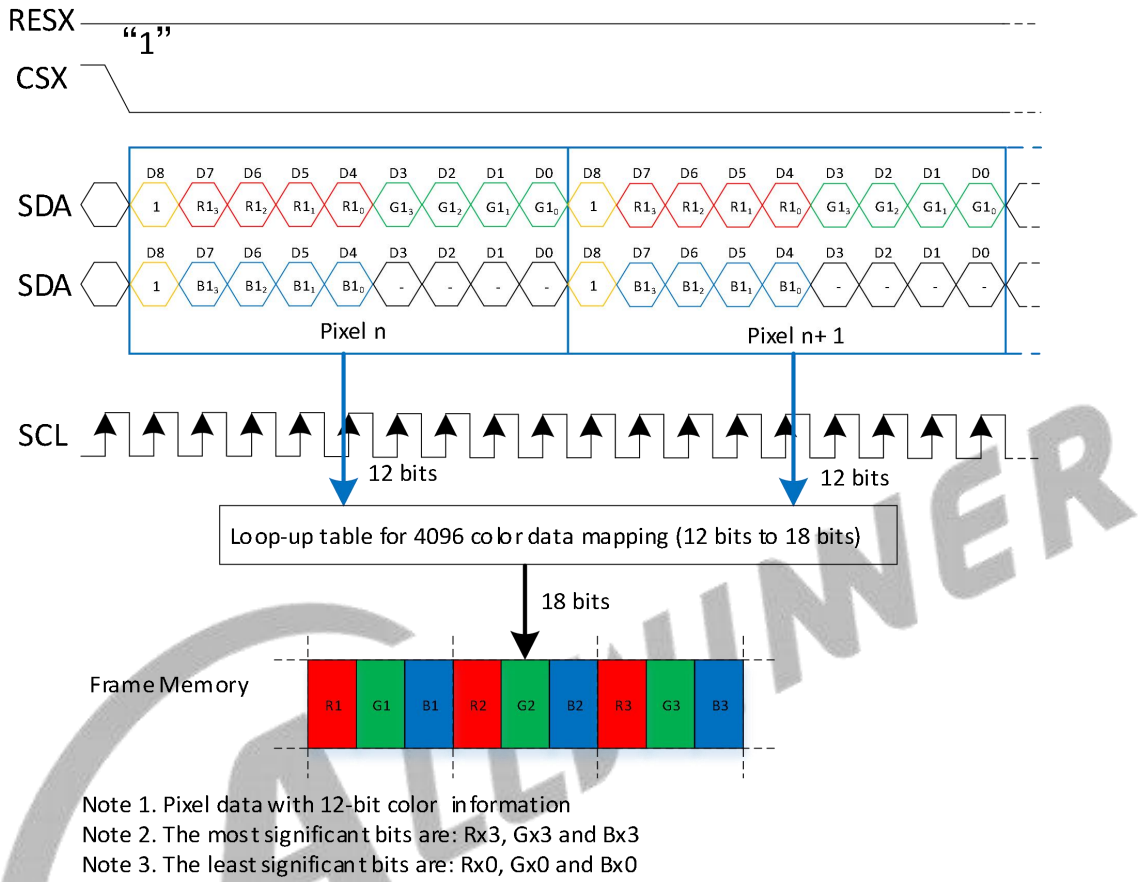


Note 1. Pixel data with 18-bit color depth information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.16.3.15 DBI 2 Data Lane Interface Transmit Video Format

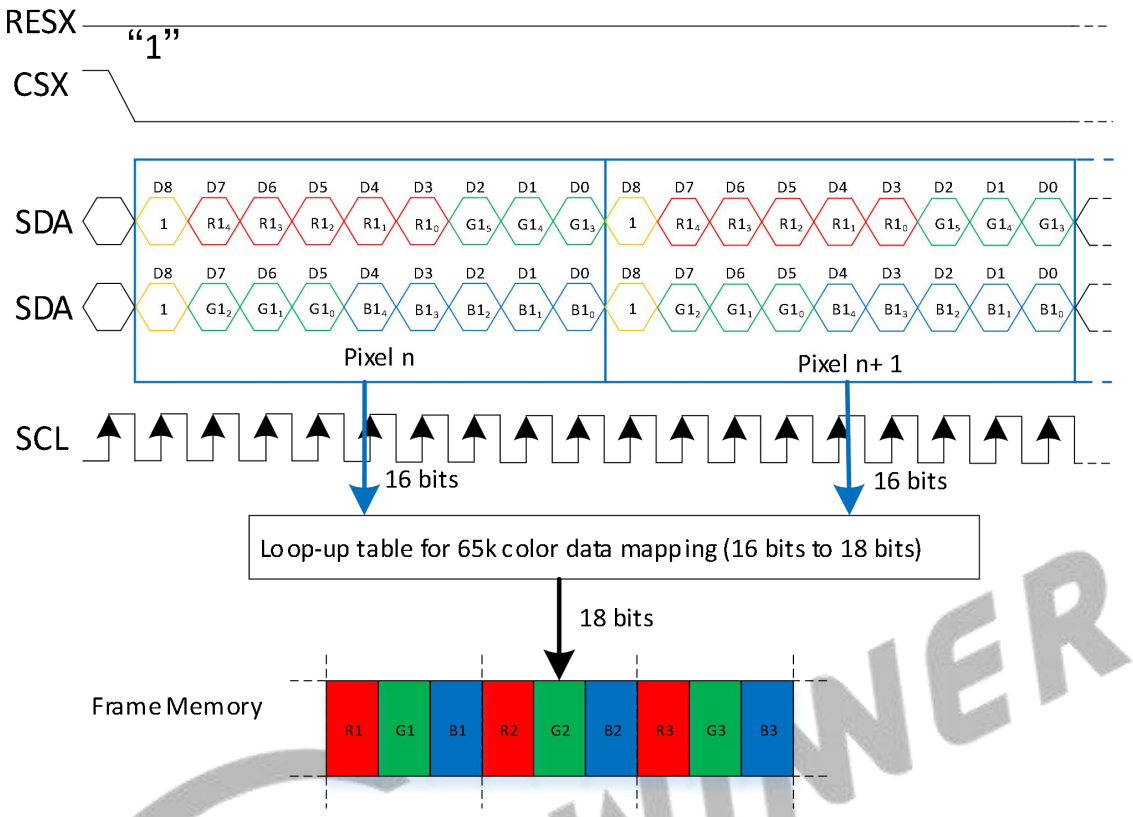
For RGB444:

Figure 8-98 RGB444 2 Data Lane Interface Transmit Video Format



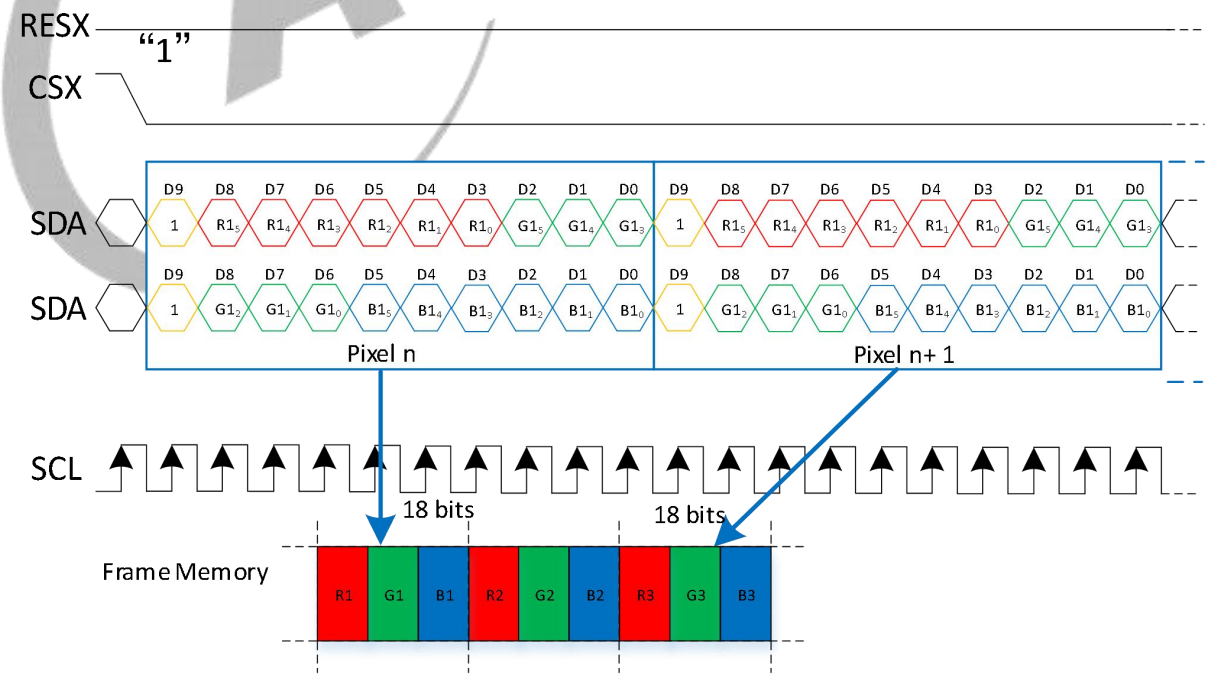
Note 1. Pixel data with 12-bit color information
Note 2. The most significant bits are: Rx3, Gx3 and Bx3
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-99 RGB565 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 16-bit color information
Note 2. The most significant bits are: Rx4, Gx5 and Bx4
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-100 RGB666 2 Data Lane Interface Transmit Video Format 0



Note 1. Pixel data with 18-bit color information
Note 2. The most significant bits are: Rx5, Gx5 and Bx5
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

Figure 8-101 RGB666 2 Data Lane Interface Transmit Video Format 1 (ilitek)

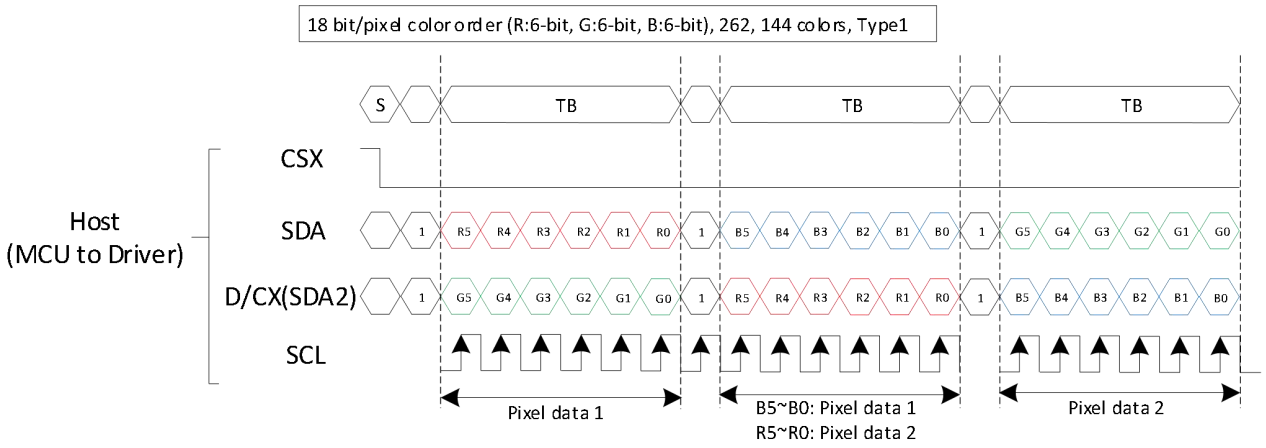


Figure 8-102 RGB666 2 Data Lane Interface Transmit Video Format 2 (New vision)

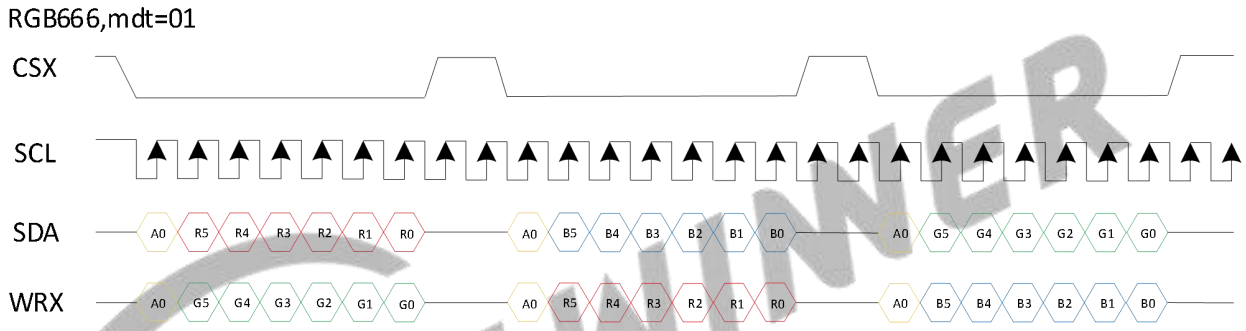
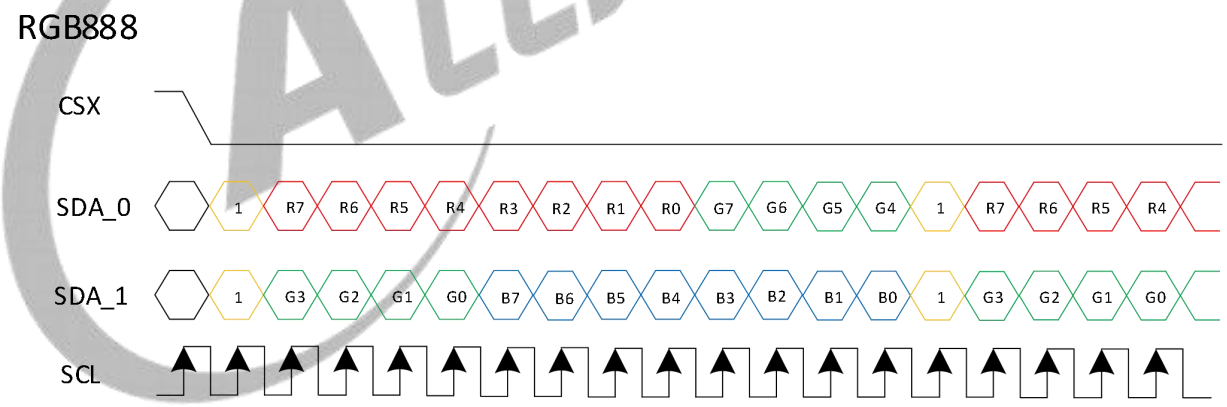


Figure 8-103 RGB888 2 Data Lane Interface Transmit Video Format



Note 1. Pixel data with 24-bit color information
Note 2. The most significant bits are: R7, G7 and B7
Note 3. The least significant bits are: R0, G0 and B0

8.16.4 Programming Guidelines

8.16.4.1 Writing/Reading Data Process Using SPI Mode

The SPI transfers serial data between the processor and the external device. CPU and DMA are the two main operational modes for SPI. For each SPI, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI has 2 channels, including the TX

channel and RX channel. The TX channel has the path from TX FIFO to the external device. The RX channel has the path from the external device to RX FIFO.

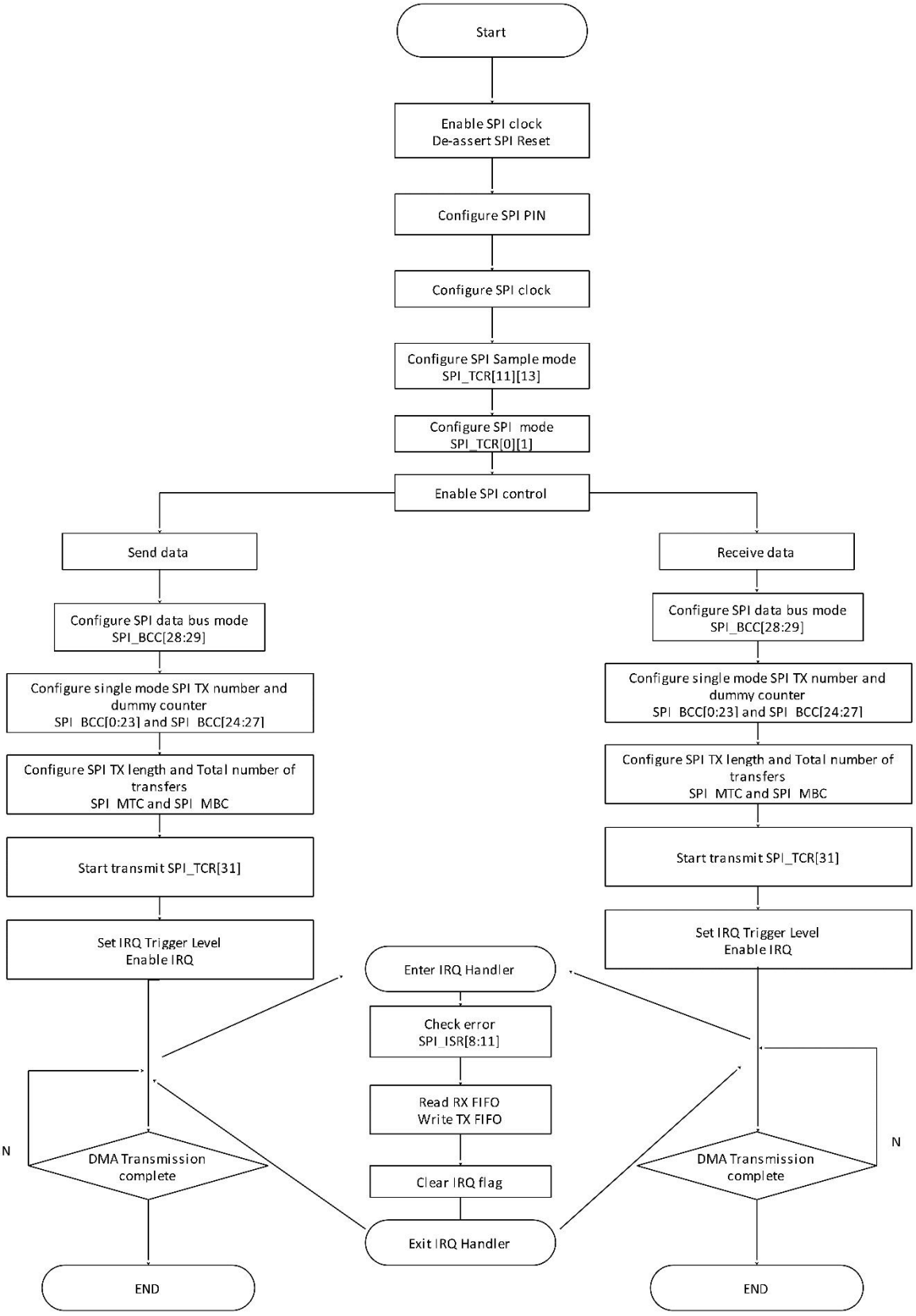
Write Data: CPU or DMA must write data on the SPI_TXD register, the data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends a completed interrupt (SPI_ISR[TC]) to the processor at the end of each transfer.

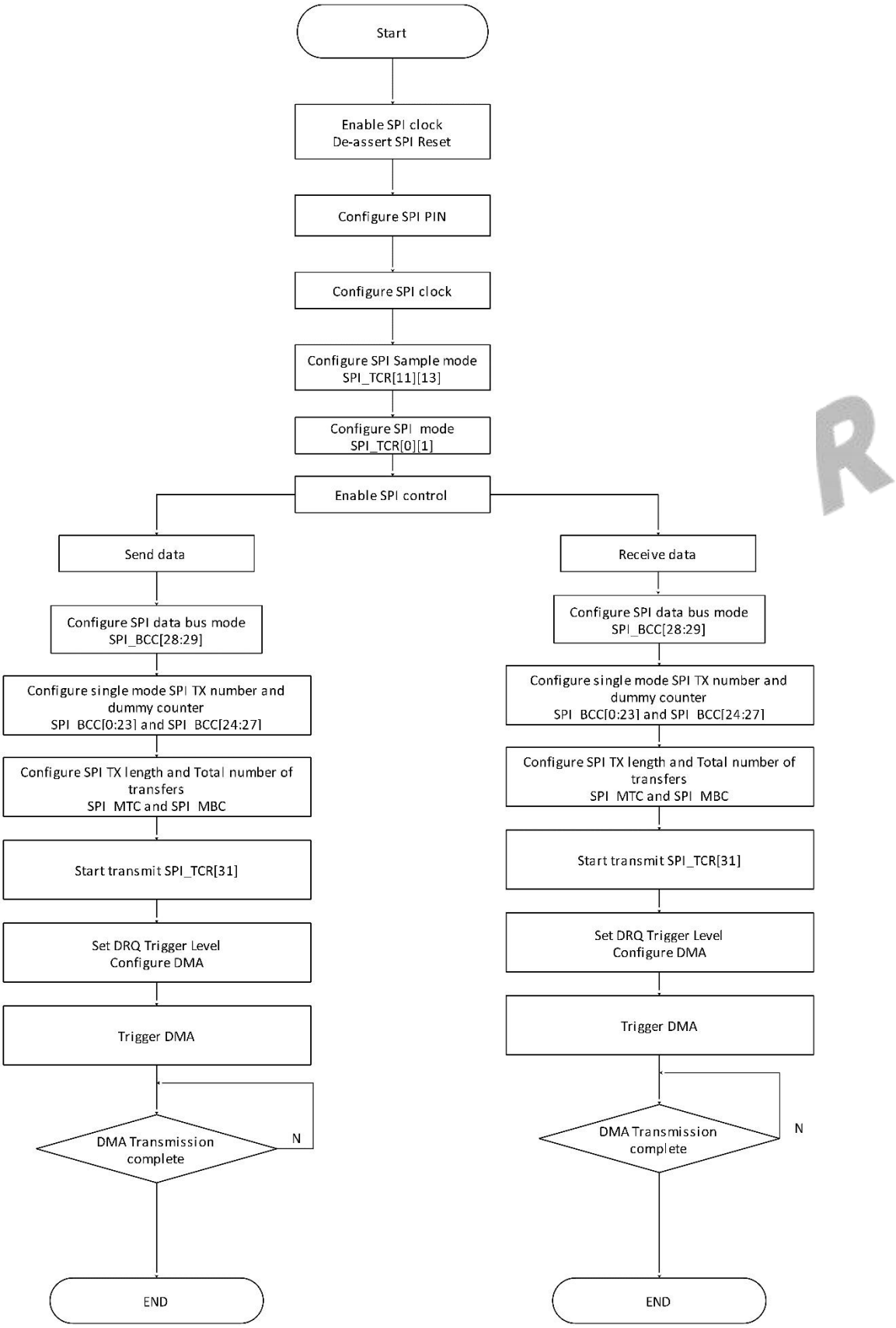
CPU Mode

Figure 8-104 SPI Write/Read Data in CPU Mode



DMA Mode

Figure 8-105 SPI Write/Read Data in DMA Mode



8.16.4.2 Transmitting Write Command Using DBI Mode

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.

Step 3 Configure the DBI_CTL_0 (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

b) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.

Step 7 Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

8.16.4.3 Transmitting Parameter Using DBI Mode

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0 to select the trigger mode of DBI.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to configure the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0 to transmit the command.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 1 to send the parameter.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[TF_DRQ_EN] (bit24) to 1 to enable TXFIFO DMA.

b) Set SPI_FCR[TX_TRIG_LEVEL] (bit[23:16]) to 255. It indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 255.

CPU Path: Write the command to be sent to the 0x200 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting the command.

Step 7 Wait until the TX FIFO underrun interrupt (SPI_ISR[TF_UDF]) is 1. It indicates that the command written to the TX FIFO is transmitted completely.

8.16.4.4 Transmitting Video Using DBI Mode

Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

If the data is from the CPU path, the controller writes the command to be sent to the 0x0200 address by the AHB bus.

If the data is from the DMA path, configure DBI_CTL_1[DBI_FIFO_DRQ_EN] (bit15) to 1 and DBI_CTL_1[TX_TRIG_LEVEL] (bit[14:8]) to 64, which indicates the controller requests data from DMA if the remaining space of TX FIFO is greater than 64.

Software Trigger Mode

The software enables DBI_en_trigger when the edge interrupt of TE is detected.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt and stops transmitting data.

Wait for the edge interrupt of TE, the software needs to enable DBI_en_trigger, in circulation.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 1 to select the software trigger mode.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111//444/565/666/888.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x110) according to the sent image size.

Step 6 Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

Step 7 Detect the TE interrupt of the DBI_INT (0x0120) register.

Step 8 Configure DBI_CTL_1[DBI_soft_trigger] to 1.

Timer Trigger Mode

The software configures timer_en to enable timer counting, and when the counter reaches the specified value, the DBI_EN automatically can be enabled to start transmitting data.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt, and stops transmitting data.

The timer starts counting again. When the counter reaches the specified value, the controller automatically enables DBI_EN, and in circulation until the software turns off the timer_en.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 2 to select the timer trigger mode.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

b) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

c) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

d) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

e) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

f) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

g) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Set DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x110) to transmit the image size.

Step 6 Configure the related parameter of DBI_Timer (0x10C).

TE Trigger Mode

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN automatically can be enabled to start transmitting data.

After transmitting each frame image, the controller clears automatically the line_cnt, pixel_cnt, and stops transmitting data.

When the edge changes of the TE are detected (The rising and falling edges are optional), the DBI_EN automatically can be enabled to start transmitting data until the software shuts down TE_EN or the screen no longer sends TE signals.

The operation process is as follows.

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit30:29) of DBI_CTL_1 (0x0104) to 3 to select the TE Configure the DBI_CTL_0 register (0x0100).

Step 3 Set DBI_CTL_0[Command Type] (bit31) to 0 to set the writing command.

a) Set DBI_CTL_0[Write Command Dummy Cycles] (bit[30:20]) to configure the number of dummy cycles between commands.

b) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

c) Set DBI_CTL_0[Transmit Mode] (bit15) to 1 to select the image path.

d) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to select RGB111/444/565/666/888.

e) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

f) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the image data.

Step 5 Configure DBI_Video_Size (0x0110) to transmit the image size.

Step 6 Configure DBI_CTL_2 (0x0108) to set the TE-related parameter.

8.16.4.5 Transmitting Read Command and Read Data Using DBI Mode

Step 1 Set the SPI_DBI_MODE_SEL (bit3) of SPI_GCR (0x0004) to 1 to select DBI mode.

Step 2 Set the DBI EN MODE SEL (bit[30:29]) of DBI_CTL_1 (0x0104) to 0.

Step 3 Configure the DBI_CTL_0 register (0x0100).

a) Set DBI_CTL_0[Command Type] (bit31) to 0 to set the reading command.

b) Set DBI_CTL_0[Output Data Sequence] (bit19) to select the MSB or LSB.

c) Set DBI_CTL_0[Transmit Mode] (bit15) to 0 to select the command path.

d) Set DBI_CTL_0[Output Data Format] (bit[14:12]) to 0.

e) Set DBI_CTL_0[DBI interface Select] (bit[10:8]) to select the DBI interface type.

f) The remaining values of the DBI_CTL_0 register remain the default value.

Step 4 Configure the DBI_CTL_1 register (0x0104).

a) Configure DBI_CTL_1[DCX_DATA] (bit22) to 0 to send the command.

b) Configure DBI_CTL_1[Read_MSB_First] (bit20) to select whether the first bit of the read data is the highest or lowest bit of data.

c) Configure DBI_CTL_1[Read Data Number of Bytes] to set the byte number to be read.

d) Configure DBI_CTL_1[Read Command Dummy Cycles] to set the dummy cycle between the read command and the read data, when the dummy cycle is complete, the data starts to be sampled.

Step 5 DMA Path: Configure the SPI_FCR register (0x0018).

a) Set SPI_FCR[RF_DRQ_EN] (bit8) to 1 to enable RXFIFO DMA.

b) Set SPI_FCR[RX_TRIG_LEVEL] (bit[7:0]) to 32, which indicates the controller requests receiving data from DMA if the data of the RX FIFO is greater than 64.

CPU Path: Read data in RX FIFO from the 0x0300 address.

Step 6 Set SPI_GCR[DBI_EN] (bit4) to 1 to start transmitting command.

Step 7 Wait until DBI_INT[RD_DONE_INT] is 1. It indicates that the data is read completely.

8.16.5 Register List

Module Name	Base Address
SPI1	0x0402 6000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control register
SPI_IER	0x0010	SPI Interrupt Control register
SPI_ISR	0x0014	SPI Interrupt Status register
SPI_FCR	0x0018	SPI FIFO Control register
SPI_FSR	0x001C	SPI FIFO Status register
SPI_WCR	0x0020	SPI Wait Clock Counter register
SPI_SAMP_DL	0x0028	SPI Sample Delay Control Register
SPI_MBC	0x0030	SPI Master Burst Counter register

Register Name	Offset	Description
SPI_MTC	0x0034	SPI Master Transmit Counter Register
SPI_BCC	0x0038	SPI Master Burst Control Counter register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
DBI_CTL_0	0x0100	DBI Control Register 0
DBI_CTL_1	0x0104	DBI Control Register 1
DBI_CTL_2	0x0108	DBI Control Register 2
DBI_TIMER	0x010C	DBI Timer Control Register
DBI_VIDEO_SIZE	0x0110	DBI Video Size Register
DBI_INT	0x0120	DBI Interrupt Register
DBI_DEBUG_0	0x0124	DBI DEBUG Register 0
DBI_DEBUG_1	0x0128	DBI DEBUG Register 1
SPI_TXD	0x0200	SPI TX Data register
SPI_RXD	0x0300	SPI RX Data register
SPI_BSR	0x0400	SPI BUF Status register

8.16.6 Register Description

8.16.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0s	SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1: Stop transmitting data when RXFIFO is full. 0: Normal operation, ignore RXFIFO status. **Note: Can't be written when XCH=1.**
6:5	/	/	/
4	R/W	0x0	DBI_EN DBI Module Enable Control

Offset: 0x0004			Register Name: SPI_GCR
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
3	R/W	0x0	SPI_DBI_MODE_SEL SDBISPI_DBI Working Mode Select 0: SPI MODE 1: DBI MODE
2	R/W	0x0	MODE_SELEC Sample Timing Mode Select 0: Old mode of Sample Timing 1: New mode of Sample Timing **Note: Can't be written when XCH=1.**
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode **Note: Can't be written when XCH=1.**
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable **Note: After transforming from bit_mode to byte_mode, it must Enable the SPI Module again.**

8.16.6.2 0x0008 SPI Transfer Control Register (Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write "1" to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write "1" to SRST will also clear this bit. Write '0' to this bit has no effect. **Note: Can't be written when XCH=1.**
30:16	/	/	/
15	R/W	0x0	SDC1 Master Sample Data Control register1 Set this bit to '1' to make the internal read sample

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
			point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: normal operation, do not delay internal read sample point 1: delay internal read sample point **Note：Can't be written when XCH=1.**
14	R/W	0x0	SDDM Sending Data Delay Mode 0:normal sending 1:delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual io mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 1: Normal Sample Mode 0: Delay Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first **Note: Can't be written when XCH=1.**
11	R/W	0x0	SDC Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: normal operation, do not delay internal read sample point 1: delay internal read sample point **Note: Can't be written when XCH=1.**
10	R/W	0x0	RPSM

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
			Rapids mode select Select Rapids mode for high speed write. 0: normal write mode 1: rapids write mode **Note: Can't be written when XCH=1.**
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one **Note: Can't be written when XCH=1.**
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. **Note: Can't be written when XCH=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: Can't be written when XCH=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: Can't be written when XCH=1.**
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted

Offset: 0x0008			Register Name: SPI_TCR
Bit	Read/Write	Default/Hex	Description
			11: SPI_SS3 will be asserted **Note: Can't be written when XCH=1.**
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts **Note: Can't be written when XCH=1.**
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: Can't be written when XCH=1.**
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: Can't be written when XCH=1.**
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) **Note: Can't be written when XCH=1.**

8.16.6.3 0x0010 SPI Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN

Offset: 0x0010			Register Name: SPI_IER
Bit	Read/Write	Default/Hex	Description
			TXFIFO under run Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO under run Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

8.16.6.4 0x0014 SPI Interrupt Status Register (Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
11	R/W1C	0x0	TF_UDF TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/

Offset: 0x0014			Register Name: SPI_ISR
Bit	Read/Write	Default/Hex	Description
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL <= RX_TRIG_LEVEL 1: RX_WL > RX_TRIG_LEVEL This bit is set any time if RX_WL > RX_TRIG_LEVEL. Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.16.6.5 0x0018 SPI FIFO Control Register (Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Write '1' to this bit will reset the control portion of the TX FIFO and auto clear to '0' when completing reset operation, write to '0' has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: disable 1: enable In normal mode, TX FIFO can only be read by SPI controller, write '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable

Offset: 0x0018			Register Name: SPI_FCR
Bit	Read/Write	Default/Hex	Description
			1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

8.16.6.6 0x001C SPI FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	Read/Write	Default/Hex	Description
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO ... 64 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO ... 64: 64 bytes in RX FIFO other: Reserved

8.16.6.7 0x0020 SPI Wait Clock Counter Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted

Offset: 0x0020			Register Name: SPI_WCR
Bit	Read/Write	Default/Hex	Description
			n: n SPI_SCLK wait states inserted These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. **Note：Can't be written when XCH=1.**
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted **Note: Can't be written when XCH=1.**

8.16.6.8 0x0028 SPI Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0028			Register Name: SPI_SAMP_DL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

8.16.6.9 0x0030 SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MBC

Offset: 0x0030			Register Name: SPI_MBC
Bit	Read/Write	Default/Hex	Description
			Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst ... N: N bursts **Note:** • **Can't be written when XCH=1;** • **Total transfer data, include the TXD, RXD and dummy burst.**

8.16.6.10 0x0034 SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst ... N: N bursts **Note: Can't be written when XCH=1.**

8.16.6.11 0x0038 SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31: 30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable **Note:**

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
			• Can't be written when XCH=1; • Quad mode includes Quad-Input and Quad-Output.
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Note: • Can't be written when XCH=1. • It is only valid when Quad_Mode_EN=0.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don't care by the device. 0: 0 burst 1: 1 burst ... N: N bursts Note: Can't be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst ... N: N bursts Note: Can't be written when XCH=1.

8.16.6.12 0x0040 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bits frame, it is only valid when Work Mode Select==0x10/0x11.

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
			0: Idle 1: Initiates transfer. Write "1" to this bit will start to transfer serial bits frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Standard Sample Mode 1: Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode. In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register(or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed **Note: It is only valid when Work Mode Select==0x10/0x11.**
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable **Note: It is only valid when Work Mode Select==0x10/0x11.**
23:22	/	/	/
21:16	R/W	0x00	RX_FEM_LEN Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit ... 100000: 32bits

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
			Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
15:14	/	/	/
13:8	R/W	0x00	TX_FEM_LEN Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
4	/	/	/
3:2	R/W	0x0	SS_SEL

Offset: 0x0040			Register Name: SPI_BATCR
Bit	Read/Write	Default/Hex	Description
			SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: It is only valid when Work Mode Select= =0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
1:0	R/W	0x0	WMS Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

8.16.6.13 0x0048 SPI TX Bit Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first. **Note: This register is only valid when Work Mode Select==0x10/0x11.**

8.16.6.14 0x004C SPI RX Bit Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first. **Note: This register is only valid when Work Mode**

Offset: 0x004C			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
			Select==0x10/0x11.

8.16.6.15 0x0088 SPI Normal DMA Mode Control Register (Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0x3	SPI_ACT_M SPI NDMA Active Mode 00: DMA_ACTIVE is low 01: DMA_ACTIVE is high 10: DMA_ACTIVE is controlled by DMA_REQUEST(DRQ) 11: DMA_ACTIVE is controlled by controller
5	R/W	0x1	SPI_ACK_M SPI NDMA Acknowledge Mode 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	SPI_DMA_WAIT The counts of hold cycles from DMA last signal high to DMA_ACTIVE high。

8.16.6.16 0x0100 DBI Control Register 0 (Default Value: 0x0010_0000)

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CMDT Command Type 0: Write Command 1: Read Command
30:20	R/W	0x1	WCDC Write Command Dummy Cycles Controls dummy cycles between two write commands Range 1-255 Default Condition: there is a dbi_clk cycle between each command or parameter.
19	R/W	0x0	DAT_SEQ Output Data Sequence 0: MSB First

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
			1: LSB First
18:16	R/W	0x0	RGB_SEQ Output RGB Sequence 0：RGB 1：RBG 2：GRB 3：GBR 4：BRG 5：BGR 6-7 Reserve
15	R/W	0x0	TRAN_MOD Transmit Mode 0：Command / Parameter 1：Video
14:12	R/W	0x0	DAT_FMT Output Data Format 0 : RGB111 1 : RGB444 2 : RGB565 3 : RGB666 4 : RGB888 (only for 2 Data Lane Interface) 5-7 Reserve
11	/	/	/
10:8	R/W	0x0	DBI_INTF DBI Interface 0: 3 Line Interface I 1: 3 Line Interface II 2: 4 Line Interface I 3: 4 Line Interface II 4: 2 Data Lane Interface
7:4	R/W	0x0	RGB_FMT RGB_Source_Format When Video Source_Type is RGB32 0：RGB 1：RBG 2：GRB 3：GBR 4：BRG 5：BGR Other:Reserve

Offset: 0x0100			Register Name: DBI_CTL_0
Bit	Read/Write	Default/Hex	Description
			When Video Source_Type is RGB16 0：RGB 1-4:reserve 5：BGR 6：GRBG_0:{G[5:3] R[4:0] B[4:0] G[2:0]} 7：GBRG_0:{G[5:3] B[4:0] R[4:0] G[2:0]} 8：GRBG_1:{G[2:0] R[4:0] B[4:0] G[5:3]} 9：GBRG_1:{G[2:0] B[4:0] R[4:0] G[5:3]} Other:Reserve
3	R/W	0x0	DUM_VAL Dummy Cycle Value Output Value During Dummy Cycle
2	R/W	0x0	RGB_BO RGB Bit Order 0: Remain the sequence of RGB data 1: Swap the higher bit and the lower bit for each component of DRAM RGB
1	R/W	0x0	ELEMENT_A_POS Element A Position Only for RGB32 Data Format 0: A component is in the bit [31:24] of data source 1: A component is in the bit [7:0] of data source
0	R/W	0x0	VI_SRC_TYPE RGB Source Type 0: RGB32 1: RGB16

8.16.6.17 0x0104 DBI Control Register 1 (Default Value: 0x0000_0001)

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	DBI_SOFT_TRG It is only available for software trigger mode. Write '1' to this bit will start DBI TX module and auto clear to '0' when completing start operation, write to '0' has no effect.
30:29	R/W	0x0	DBI_EN_MOD_SEL DBI Enable Mode Select 0: always on mode 1: software trigger mode 2: timer trigger mode

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
			3: te trigger mode
28	/	/	/
27:26	R/W	0x0	RGB666_FMT 2 Data Lane RGB666 Format 00: Normal Format 01: Special Format for ILITEK 10: Special Format for New Vision
25	R/W	0x0	DBI_RXCLK_INV DBI rx clock inverse 0: Sample data by using the positive edge of the output clock 1: Sample data by using the negative edge of the output clock
24	R/W	0x0	DBI_CLKO_MOD DBI output clock mode 0: DBI clock always on(DCX Setup/hold equals one clock cycle) 1: DBI clock auto gating(DCX Setup/hold equals to a half clock cycle)
23	R/W	0x0	DBI_CLKO_INV DBI clock output inverse When the bit24 (DBI output clock mode) is 0. 0: The falling edge releases the CSX signal, and the falling edge releases data 1: The rising edge releases the CSX signal, and the rising edge releases data When the bit24 (DBI output clock mode) is 1. 0: The rising edge releases the CSX signal, and the falling edge releases data 1: The falling edge releases the CSX signal, and the rising edge releases data
22	R/W	0x0	DCX_DATA DCX Data Value 0：DCX Value equal to 0 1：DCX Value equal to 1
21	R/W	0x0	RGB 16 Data Source Select RGB 16 Data Source Select 0: Pixel1 is stored in the higher bit of address, and Pixel0 is stored in the lower bit of address 1: Pixel0 is stored in the higher bit of address, and Pixel1 is stored in the lower bit of address

Offset: 0x0104			Register Name: DBI_CTL_1
Bit	Read/Write	Default/Hex	Description
20	R/W	0x0	RDAT_LSB Bit Order of Read Data 0: A reading data is the higher bit 1: A reading data is the lower bit
19:16	/	/	/
15:8	R/W	0x0	RCDC Read Command Dummy Cycles The dummy cycle between the read command and read data Reading 1-byte (8 bits) data has not dummy cycle.
7:0	R/W	0x1	RDBN Read Data Number of Bytes Sample Bytes data based on configuration.

8.16.6.18 0x0108 DBI Control Register 2 (Default Value: 0x0000_4000)

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	DBI_FIFO_DRQ_EN DBI FIFO DMA Request Enable 0: Disable 1: Enable
14:8	R/W	0x40	DBI_TRIG_LEVEL DBI FIFO Empty Request Trigger Level
7	/	/	/
6	R/W	0x0	DBI_SDI_OUT_SEL DBI SDI PIN Output Select The signal is used with the DBI SDI PIN Function Sel bit. 0: Output WRX (When DBI DCX PIN Function Sel = 0, the SDI pin outputs data) 1: Output DCX
5	R/W	0x0	DBI_DCX_SEL DBI DCX PIN Function Sel 0: DBI DCX Function 1:WRX(2 Data Lane Interface)
4:3	R/W	0x0	DBI_SDI_SEL DBI SDI PIN Function sel 0: DBI_SDI (Interface II) , WRX(2 Data Lane Interface)

Offset: 0x0108			Register Name: DBI_CTL_2
Bit	Read/Write	Default/Hex	Description
			1: DBI_TE 2: DBI_DCX Reserve
2	R/W	0x0	TE_DBC_SEL TE debounce function select 0: debounce 1: no-debounce
1	R/W	0x0	TE_TRIG_SEL TE edge trigger select 0: TE rising edge 1: TE falling edge
0	R/W	0x0	TE_EN TE enable 0: TE Disable 1: TE Enable

8.16.6.19 0x010C DBI Timer Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: DBI_TIMER
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DBI_TM_EN DBI Timer enable 0: enable 1: disable
30:0	R/W	0x0	DBI Timer Value It sets the time interval between sending data twice, which is frame blanking. It is used to set the time at which the interrupt of the DBI Timer is triggered. When the Timer_EN is 1, the timer starts to count (the clock of the counting is SCLK), and the counter reaches the target value to trigger the Timer_INT of DBI, the data will start to send in series. **Note: Do not count when sending the series data.**

8.16.6.20 0x0110 DBI Video Size Register (Default Value: 0x01e0_0140)

Offset: 0x0110			Register Name: DBI_VIDEO_SIZE
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/

Offset: 0x0110			Register Name: DBI_VIDEO_SIZE
Bit	Read/Write	Default/Hex	Description
26:16	R/W	0x1e0	V_SIZE It is used to generate the Frame int.
15:11	/	/	/
10:0	R/W	0x140	H_SIZE It is used to generate the Line int.

8.16.6.21 0x0120 DBI Interrupt Register (Default Value: 0x0000_4000)

Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W1C	0x1	DBI_FIFO_EMPTY_INT DBI FIFO Empty Interrupt Status 0: DBI_FIFO is not empty 1: DBI_FIFO is empty
13	R/W1C	0x0	DBI_FIFO_FULL_INT DBI FIFO Full Interrupt Status 0: DBI_FIFO is not full 1: DBI_FIFO is full
12	R/W1C	0x0	TIMER_INT it indicates that timer has been count sclk cycles to the value of DBI_Timer Register[30:0] . Writing 1 to this bit clears it. 0: Timer has no been achieve objective 1: Timer has been achieve objective
11	R/W1C	0x0	RD_DONE_INT it indicates that the number of byte setting in DBI_Control Register 1 [19:8] has been read . Writing 1 to this bit clears it. 0: all of data has been not read 1: all of data has been read
10	R/W1C	0x0	TE_INT it indicates that TE signal has been changed. Writing 1 to this bit clears it. 0: TE signal is no changed 1: TE signal has been changed
9	R/W1C	0x0	FRAM_DONE_INT it indicates that a frame video data has been send. Writing 1 to this bit clears it. 0: a frame video has not been send 1: a frame video has been send

Offset: 0x0120			Register Name: DBI_INT
Bit	Read/Write	Default/Hex	Description
8	R/W1C	0x0	LINE_DONE_INT it indicates that a line of video data has been send. Writing 1 to this bit clears it. 0: a line of video data has not been send 1: a line of video data has been send
7	/	/	/
6	R/W	0x0	DBI_FIFO_EMPTY_INT_EN DBI FIFO Empty Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DBI_FIFO_FULL_INT_EN DBI FIFO Full Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TIMER_INT_EN Timer Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RD_DONE_INT_EN Read Done Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	TE_INT_EN TE Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	FRAM_DONE_INT_EN Frame Done Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	LINE_DONE_INT_EN Line Done Interrupt Enable 0: Disable 1: Enable

8.16.6.22 0x0124 DBI Debug Register 0 (Default Value: 0x007F_0000)

Offset: 0x0124			Register Name: DBI_DEBUG_0
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:16	R	0x7F	DBI_FIFO_AVAIL

Offset: 0x0124			Register Name: DBI_DEBUG_0
Bit	Read/Write	Default/Hex	Description
			DBI FIFO ROOM VALID 0-127 Words
15:13	/	/	/
12	R	0x0	TE_VAL TE input value 0 : TE not Trigger 1 : TE Trigger
11:8	R	0x0	DBI_RXCS FSM for DBI Receive RX_BS0 - RX_BS6 , Gray - Code
7:4	R	0x0	SH_CS FSM for shifter 0-11 : SH0-SH11
3:2	R	0x0	DBI_TXCS FSM for DBI Transmit 0: IDLE 1: SHIF 2: DUMY 3: READ
1:0	R	0x0	MEM_CS FSM for DBI Memory 0: IDLE_FRM 1: FRM_POS 2: FRM_RDY

8.16.6.23 0x0128 DBI Debug Register 1 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: DBI_DEBUG_1
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R	0x0	LCNT Line counter The number of pixel lines that are currently sent
15:12	/	/	/
11:0	R	0x0	CCNT Component counter The number of RGB components that are currently sent The field is equal to pixel_cnt *3.

8.16.6.24 0x0200 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **Note: This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

8.16.6.25 0x0300 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

8.16.6.26 0x0400 SPI BUF Status Register (Default Value: 0x0000_0000)

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:16	R	0x0	TB_CNT

Offset: 0x0400			Register Name: SPI_BSR
Bit	Read/Write	Default/Hex	Description
			TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
15:8	/	/	/
7:0	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer

8.17 SPI Flash controller (SPIFC)

8.17.1 Overview

The SPI Flash Controller (SPIFC) is a synchronous, serial communication interface which allows rapid data communication with fewer software interrupts. Different from SPI, this IP is typically designed for higher speed Flash devices and it only works at Master mode.

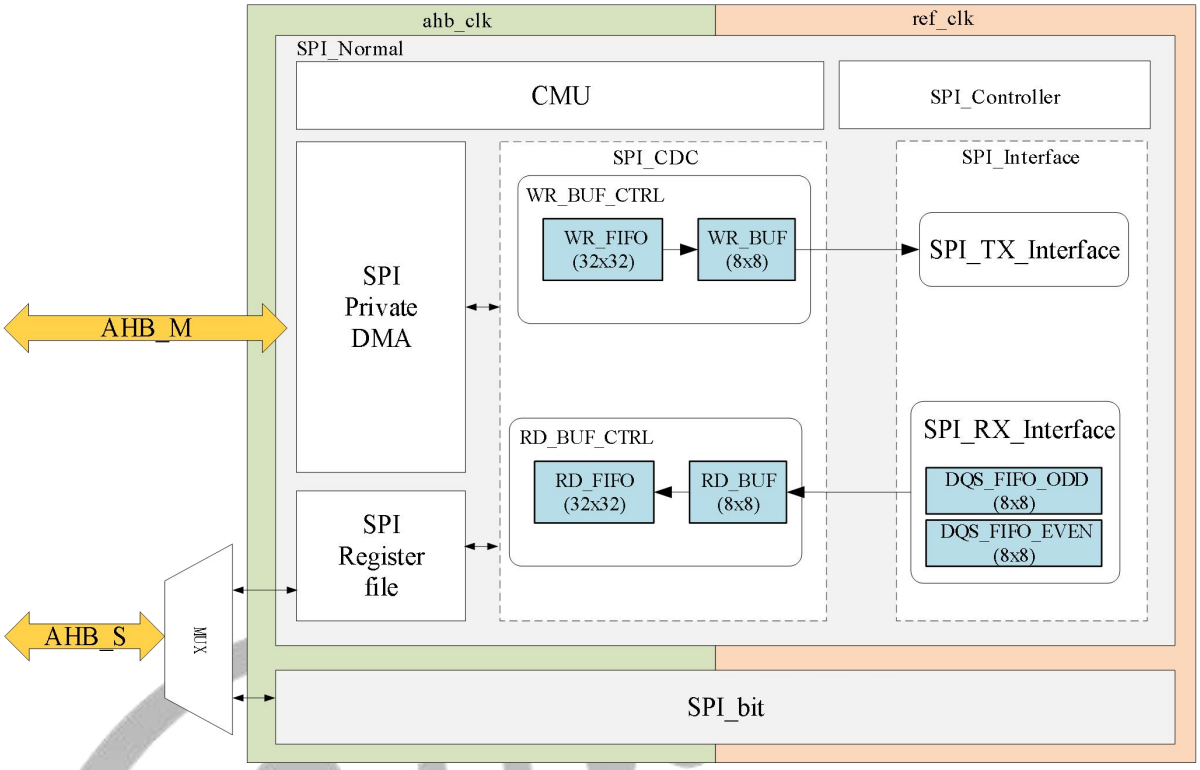
The SPI Flash Controller has the following features:

- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports STR mode and DTR mode, and DTR mode supports DQS signal
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Software Write Protection
  - Write protection for all/portion of memory via software
  - Top/Bottom Block protection
- Programmable delay between transactions
- Supports Mode0, Mode1, Mode2 and Mode3
- Supports control signal configuration
  - Up to four chip selects to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

8.17.2 Block Diagram

The following figure shows a block diagram of the SPI Flash Controller.

Figure 8-106 SPI_Flash Block Diagram



SPI Flash Controller contains the following sub-blocks:

Table 8-53 SPI Flash Controller Sub-blocks

Sub-block	Description
SPI_Register_File	Responsible for implementing registers configuration through AHB1 bus.
SPI_Private_DMA	Private DMA for SPI, which contains AHB master and supports TXFIFO(WR_FIFO) and RXFIFO(RD_FIFO).
CMU	Responsible for generating internal clock; Implementing sckr delay, clock sourcess selection, clock gating, and scan; supporting synchronous release of asynchronous reset and scan.
SPI_CDC	SPI cross-clock module, in which bit width transition finishes. (TX: 32bit->8bit; RX: 8bit->32bit) WR_BUF: Cache the write SPI data of AHB, and write them to WR_FIFO. RD_BUF: Cache the read SPI data of RD_FIFO to AHB. WR_FIFO: SPI write data FIFO (SRAM 32x32) RD_FIFO: SPI read data FIFO (SRAM 32x32) in the normal mode.
SPI_Controller	SPI controlling center. It generates TX/RX controlling signal in the course of SPI communication.
SPI_Interface	Standard SPI interface. It is responsible for receiving and transmitting data with Devices.

Sub-block	Description
SPI_bit	the processing module in SPI 3-wire mode.

8.17.3 Functional Description

8.17.3.1 External Signals

The following table describes the external signals of SPI Flash Controller. When using SPI Flash Controller, the corresponding PADs are selected as SPI Flash Controller function via section 8.5 GPIO.

Table 8-54 SPI Flash Controller External Signals

Signal Name	Description	Type
SPIF-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF-CLK	SPI Master Mode Clock Output	O
SPIF-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF-DQS	Data Strobe Signal	I
SPIF-D[7:4]	SPI Master Mode Data in Octal Mode	I/O
SPIF-WP	SPI Write Protect, Low Active	I/O
SPIF-HOLD	SPI Hold Signal	I/O

8.17.3.2 Clock Sources

The SPI_Flash controller gets 5 different clock sources and users can select one of them to make SPI Flash Controller clock source. The following table describes the clock sources for SPI Flash Controller. For more details on the clock setting, configuration, and gating information, see section 2.5 Clock Controller Unit (CCU).

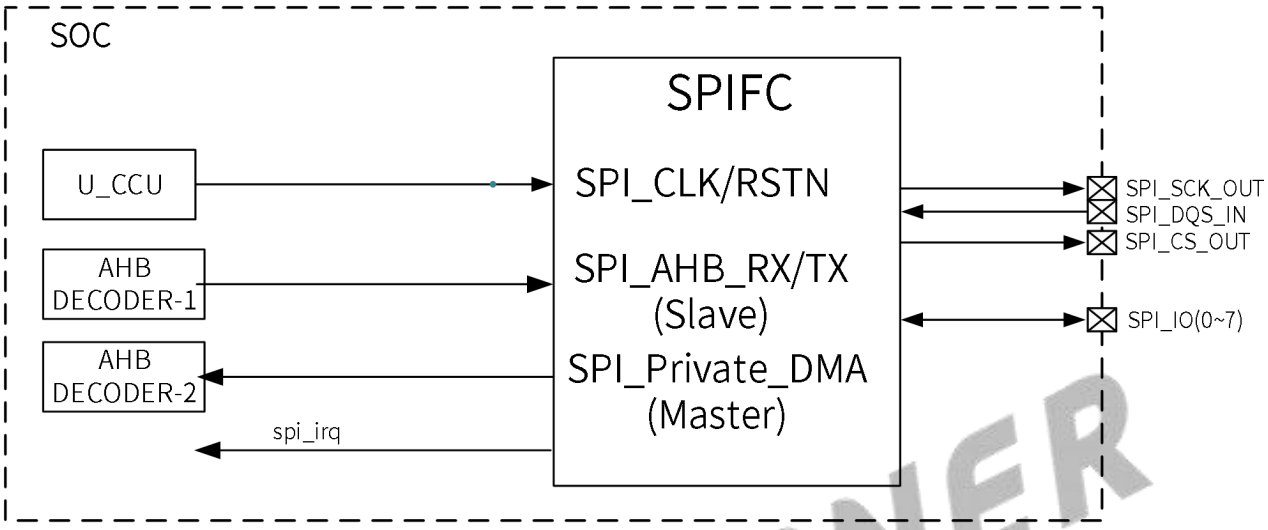
Table 8-55 SPI Flash Controller Clock Sources

Clock sources	Description	Clock module
HOSC	24 MHz Crystal	CCU
PERI0_400M	Peripheral Clock, default value is 400 MHz.	
PERI0_300M	Peripheral Clock, default value is 300 MHz.	
PERI1_400M	Peripheral Clock, default value is 400 MHz.	
PERI1_300M	Peripheral Clock, default value is 300 MHz.	

8.17.3.3 Typical Application

The following figure shows the application block diagram when the SPI master device is connected to a slave device.

Figure 8-107 Typical Application



The SPI Flash Controller is running in Master device. SPI_SCK is generated and transmitted to external device. The data from the TX FIFO is routed to the MOSI pin. The data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_CS) signal is active in low level. SPI_CS must be set to low before data are transmitted or received.

8.17.3.4 SPI Flash Controller feature list

Table 8-56 SPI Flash Controller Feature List

SPI mode		Feature List					
		STR	DTR	DTR-RX-DQS	SCK_MODE	Address Size	Description
Bit Mode	3-wire 4-wire	√	×	×	mode0	×	/
Standard SPI	1-1-1-1	√	√	√	• mode 0/1/2/3 (STR) • mode0 (DTR)	24bit/32bit	• 1-1-1-1: cmd-addr-mode-data. • mode is optional and can be turned

SPI mode		Feature List					
		STR	DTR	DTR-RX-DQS	SCK_MODE	Address Size	Description
							off.
Dual SPI	1-1-1-2	√	√	√			
	1-1-2-2						
	1-2-2-2						
	2-2-2-2						
Quad SPI	1-1-1-4	√	√	√			
	1-1-4-4						
	1-4-4-4						
	4-4-4-4						
Octal SPI	1-1-1-8	√	√	√			8-wire DTR only supports the following: ADDR-24+MODE ADDR-32
	1-1-8-8						
	1-8-8-8						
	8-8-8-8						

8.17.3.5 SPI Flash Controller Clock

SPI includes two clock domains: ahb_clk and spi_clk:

- The functions in ahb_clk: parameter analysis (ahb_register) and DMA.
- The functions in spi_clk: cross domain clock, main control unit, the communication between SPI-TX/RX and external devices.

The clock management unit (CMU) divides the external SPI reference clock and gets the o_spi_clk as the internal clock. Based on the clock properties configured by the CPU, the sckt/sckr is gotten to be used as communication clocks for the SPI_TX_INTERFACE/SPI_RX_INTERFACE.

The clock properties include:

- SPI Clock Mode
- DQS EN
- STR or DTR

When the SPI runs at a higher clock frequency, sckr may sample the wrong data because of lane delay. Thus, before sampling, the sckr should be processed by the receive clock latency.

SPI Flash Controller Clock Mode

The SPI Flash controller supports 4 different modes for data transfer. Software can select one of the four modes in which the SPI works by setting the bit5(SPI_CPOL) and bit4(SPI_CPHA) of SPI Global Control Register[0x0004].

The SPI_CPOL defines the signal polarity when SPI_SCLK is in the idle state. The SPI_SCLK is high level when POL is '1 'and it is low level when POL is '0'. The SPI_CPHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kind of modes are listed Table:

Table 8-57 SPIFC Modes with Clock Polarity and Phase

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

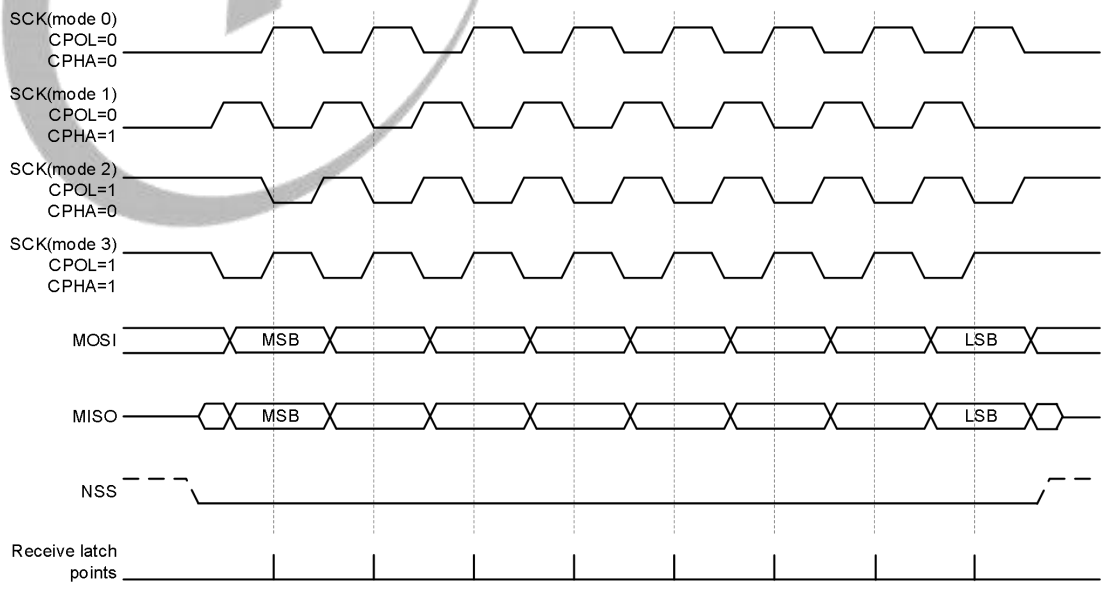
During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges and is shifted in on falling edges.

SPI Bit Mode only supports Phase 0, Polarity 0 operation; the most significant bit (MSB) of data is transmitted first which is not configurable.

The following figure describe four waveforms for SPI_SCLK.

Figure 8-108 SPI Transfer Mode

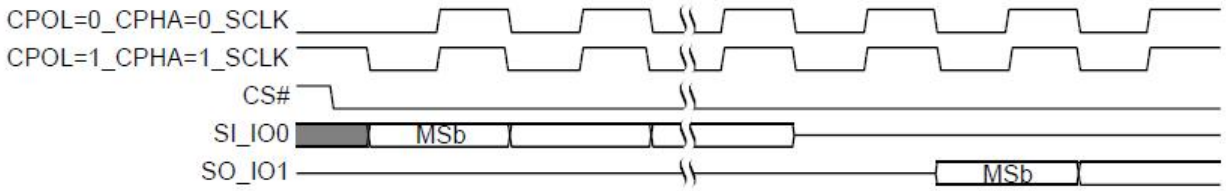


For MSB first

Single Transfer Rate (STR)

In mode 0 and mode 3, the input data of devices will be latched at the rising edge of SCK, and the output data will be used at the falling edge of SCK.

Figure 8-109 SPI STR Transfer



Double Transfer Rate (DTR)

As with the STR command, the instruction bit is latched at the rising edge of the clock in the DTR command, but the address and input data are latched at the dual edge. After the instruction bit is latched at the falling edge of SCK, the first address bit will be latched at the next rising edge of SCK. The first output data bit will be sent at the falling edge of the last access latency period.

As with the STR command, the SCK period is the cycle between two adjacent SCK falling edges. In mode 0, the SCK is already at a low level when some command starts to be executed, thus the first SCK period during the command execution indicates the cycle from the falling edge of CS# to the first falling edge of SCK.

Figure 8-110 SPI DTR Transfer Example, 1-4-4

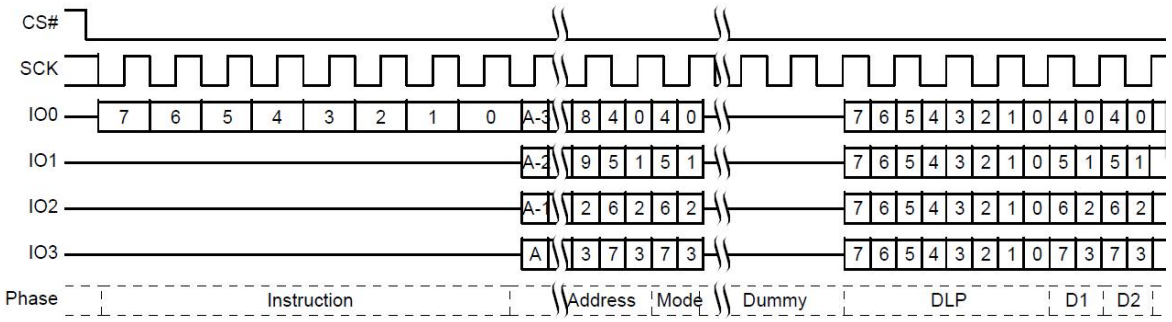
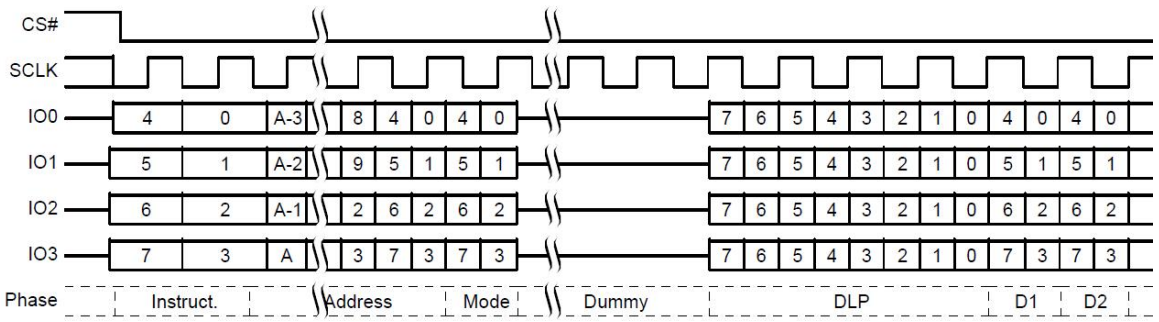


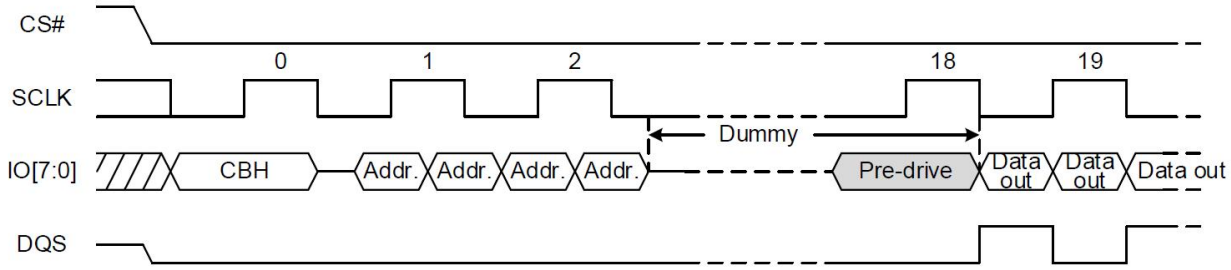
Figure 8-111 SPI DTR Transfer Example, 4-4-4



DQS

DQS (DATA Strobe Signal) signal indicates input/output data valid for DTR modes and is required to support high-speed data. When data strobe function is enabled, DQS signal is driven to ground once CS# goes LOW till the device is driving output data, in which case DQS toggles to synchronize data output. When data strobe function is not enabled, DQS signal will not be driven.

Figure 8-112 SPI DTR Transfer with DQS Input Clock Signal



8.17.3.6 SPI Run Clock and Sample Mode

SCKR Delay through Digital Adjustment

To realize the SCKR delay, connect the clk_gate and clk_xor in series to control the opening time of the EN terminal of clk_gate and the polarity of the EN terminal of clk_xor. The specific steps are as follows:

Step 1 Enable the EN terminal delay of the first-level clk_gate module to realize a delay of 1 sclk. (the effective range is 0-3 sclk)

Step 2 Make the EN terminal of the second-level clk_xor module differ in polarity to realize a delay of 0.5 sclk. (the effective values are 0 sclk and 0.5 sclk)

SCKR Delay through Analog Adjustment

There are delay chains in SPI, used to generate delay to make proper timing between internal SPI clock signal and data signals. Delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

Take RX delay chain as an example: the steps to calibrate delay chain are as follows:

Step 1 Configure a proper clock for the SPI Flash Controller. Calibration delay chain is based on the clock for SPI FLASH CONTROLLER from Clock Controller Unit (CCU)

Step 2 Set proper initial delay value to (SPI Timing Configure Register, 0x000C). Write 0x60 to this register to set initial delay value 0x20 to delay chain. Then write 0x0 to delay control register to clear this value.

Step 3 Write 0x80 to SPI Timing Configure Register to start calibrate delay chain.

Step 4 Wait until the flag (Bit7 in SPI Timing Delay State Register 0x0010) of calibration done is set. The number of delay cells is shown at Bit5-Bit0 in SPI Timing Delay State Register. The delay time generated by these delay cells is equal to the cycle of SPI FLASH CONTROLLER's clock nearly. This value is the result of calibration.

Step 5 Calculate the delay time of one delay cell according to the cycle of SPI FLASH CONTROLLER's clock and the result of calibration.

8.17.3.7 SPI Transfer Mode

SPI supports multiple transfer modes such as SPI Bit Mode, SPI Standard Mode, SPI Dual Mode, SPI Quad Mode, and SPI Octal Mode. Their main differences are the number of wires. Even in the same transfer mode, the detail modes will be derived based on the number of wires used to data transfer. The number of data lines used by Command-Address-Data is indicated on the subdivision pattern heading, expressed as (x-x-x). For example, Command uses one Data line, Address and data both use two data lines, identified by (1-2-2).

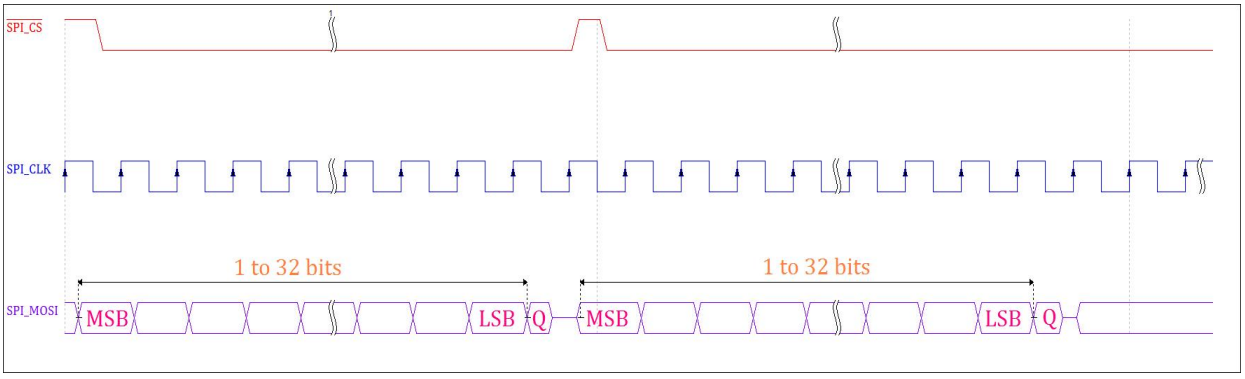
SPI Bit Mode (3-Wire/4-Wire)

For some specific scenarios, some devices such as the sensor use the SPI interfaces as the communication protocol. Generally, their data size is relatively small, and some devices support three wires, so the bit mode is added and 3-wire mode and 4-wire mode are subdivided, which includes SPI_CS, SPI_SCK, and 1/2 wires. The transmission length ranges from 1-32bit.

The 4-Wire Mode is selected when the Work Mode Select(bit[1:0]) is equal to 0x3 in the SPI Bit-Aligned Transfer Configure Register. In SPI 4-Wire Mode, the input data and output data use the independent two data line. The MISO is used for input data, and the MOSI is used for output data.

The SPI 3-Wire Mode is only valid when the SPI controller work as Master Device, and selected when the Work Mode Select(bit[1:0]) is equal to 0x2 in the SPI Bit-Aligned Transfer Configure Register. and in the 3-Wire mode, the input data and the output data use the same single data line. The following figure describe this mode.

Figure 8-113 SPI 3-Wire Mode



SPI Standard Mode (4-Wire)

Signal Wire: CS#, SCK, IO0, and IO1.

Figure 8-114 SPI CMD with Single IO

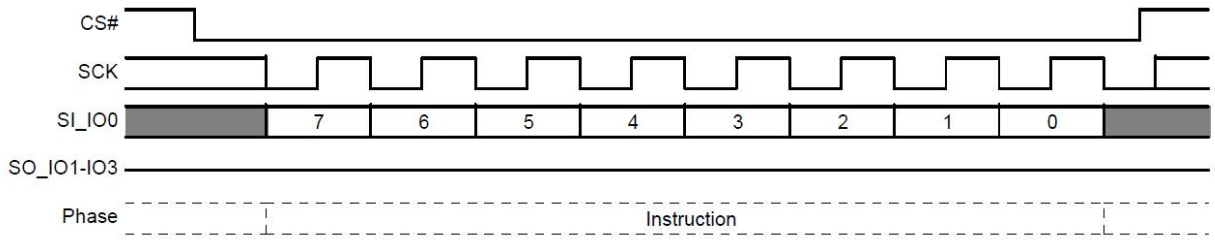


Figure 8-115 SPI Write CMD and DATA with One Wire

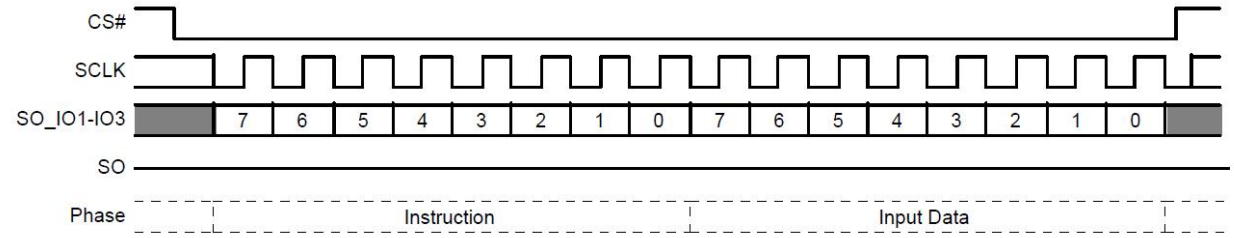


Figure 8-116 SPI Write CMD and Read DATA with One Wire (No Dummy)

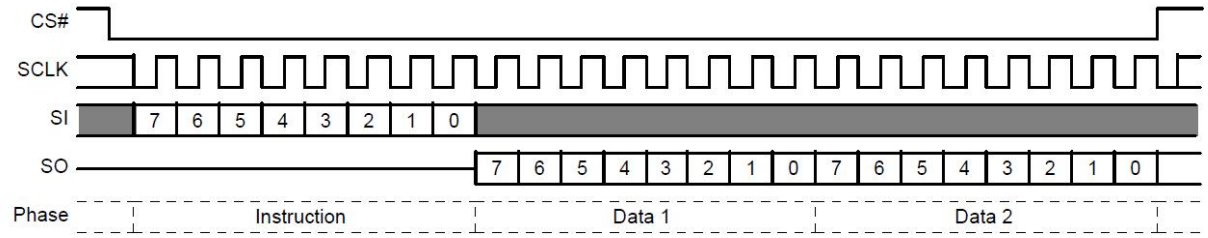
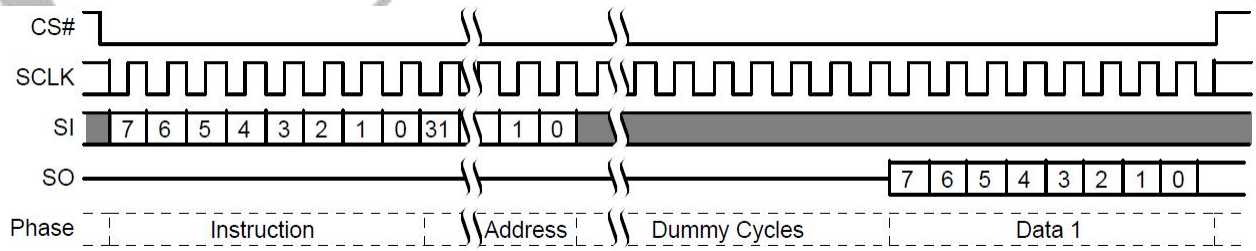


Figure 8-117 SPI Write CMD and Read DATA with One Wire (with Dummy)



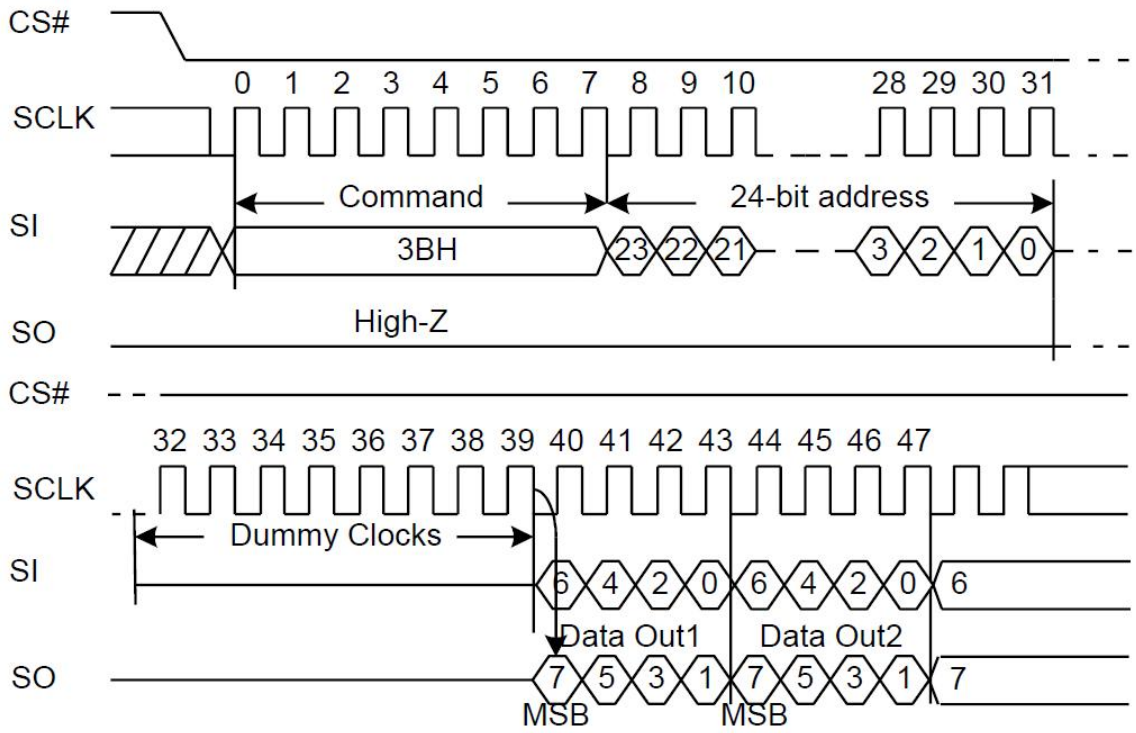
SPI Dual Mode

Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices. Data can be read at a faster speed using two data bits (MOSI and MISO) at a time. The following describe the Dual Input/Dual Output SPI (1-1-2), the Dual IO SPI (1-2-2), and the (2-2-2) SPI Mode.

- SPI Dual Input/dual Output Mode (1-1-2)

In the dual Input/dual Output SPI, the command, address, and the dummy bytes are output in the unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output (write) and input (read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

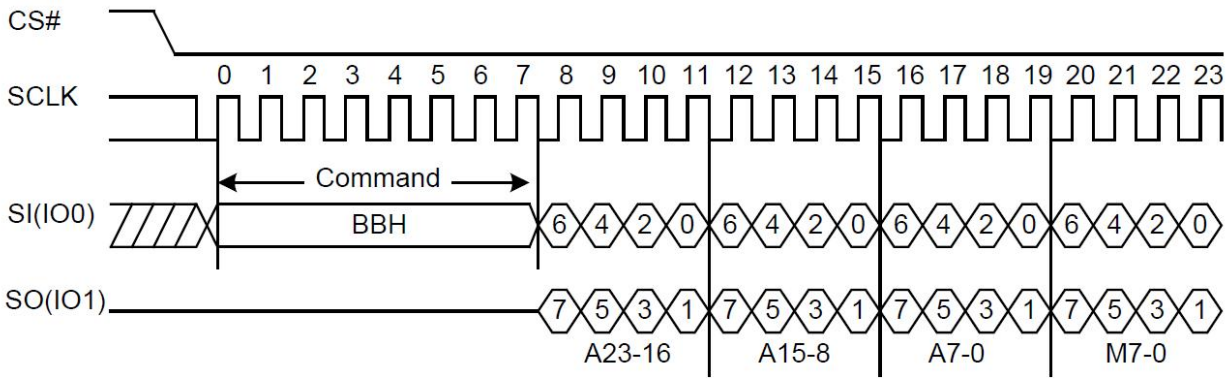
Figure 8-118 SPI Dual Input/Dual Output Mode（1-1-2）



- SPI Dual IO Mode (1-2-2)

In the Dual IO SPI, only the command bytes are output in the unit of a single bit in serial mode through SPI_MOSI line. The address bytes and the dummy bytes are output in the unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes are output (write) and input (read) in the unit of dual bits through the SPI_MOSI and SPI_MISO.

Figure 8-119 SPI Dual Input/Dual Output Mode (1-2-2)



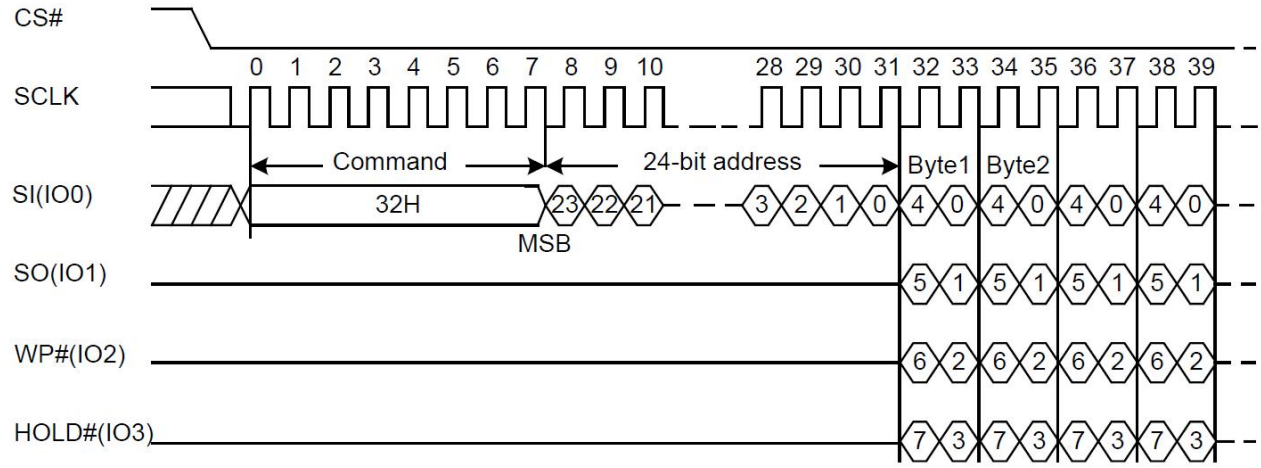
SPI Quad Mode

Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits (MOSI, MISO, IO2(WP#) and IO3(HOLD#)) at the same time. The following describe the Quad Input/Quad Output SPI (1-1-4), 1-4-4 mode, and 4-4-4 mode.

- Quad Input/Quad Output SPI (1-1-4)

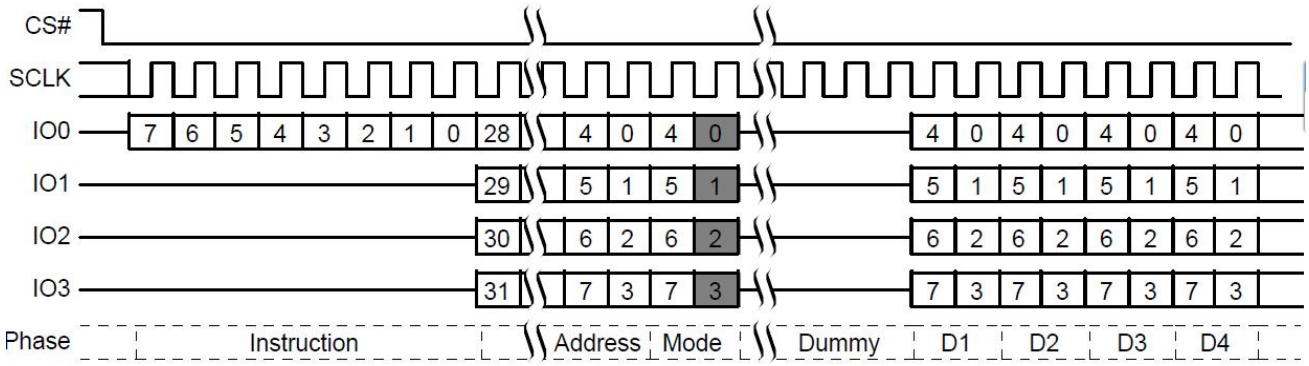
In the Quad Input/Quad Output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output (write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

Figure 8-120 SPI Quad Input/Dual Output Mode (1-1-4)



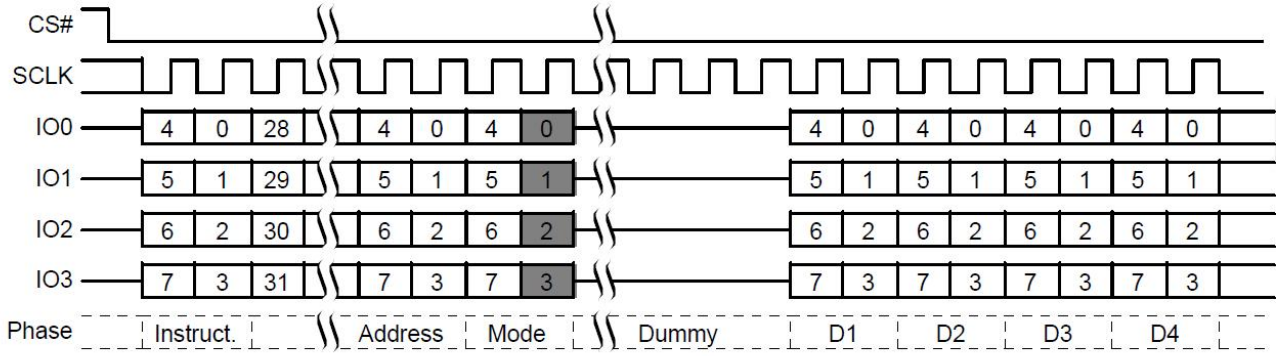
- 1-4-4 Mode

Figure 8-121 SPI Quad Input/Dual Output Mode (1-4-4)



- 4-4-4 Mode

Figure 8-122 SPI Quad Input/Dual Output Mode (4-4-4)

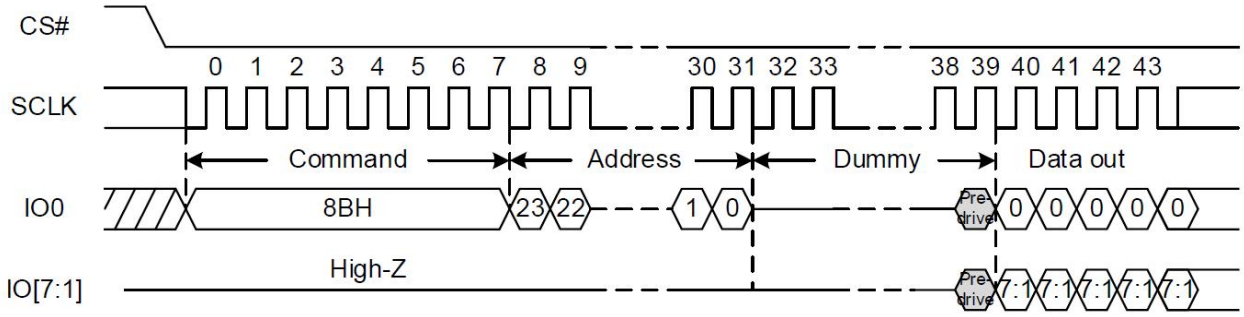


SPI Octal Mode

The Octal SPI Mode allow data to be transferred to or from the device at eight times the rate of the standard SPI. When using the Octal SPI, there are 8 data wires.

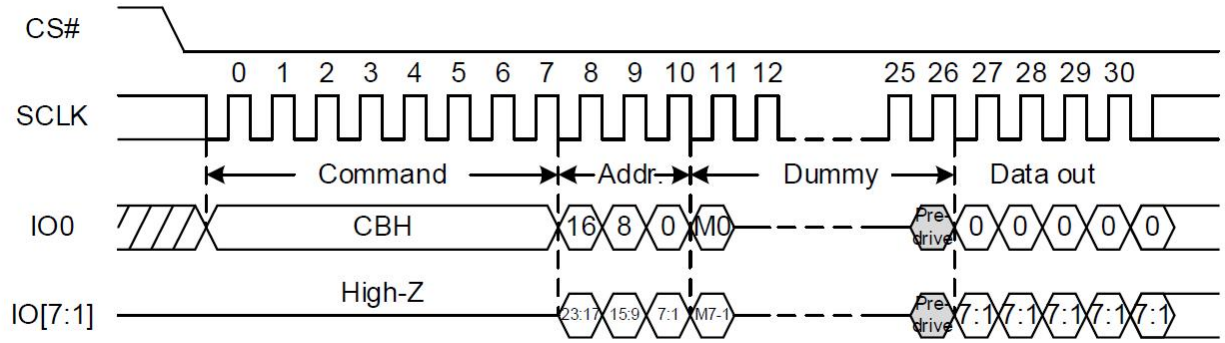
- SPI Octal 1-1-8

Figure 8-123 SPI Octal Input/Dual Output Mode (1-1-8)



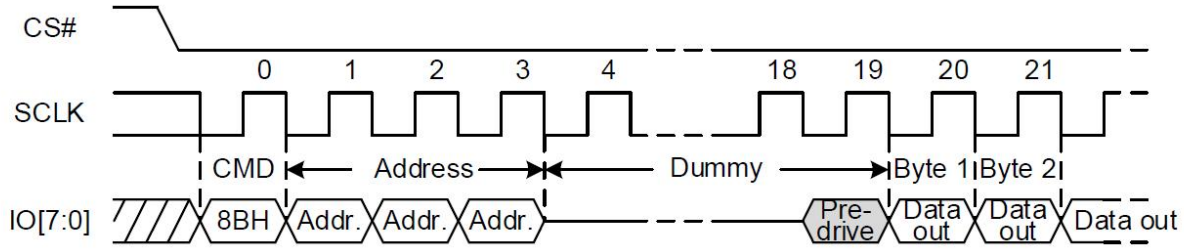
- SPI Octal 1-8-8

Figure 8-124 SPI Octal Input/Dual Output Mode (1-8-8)



- SPI Octal 8-8-8

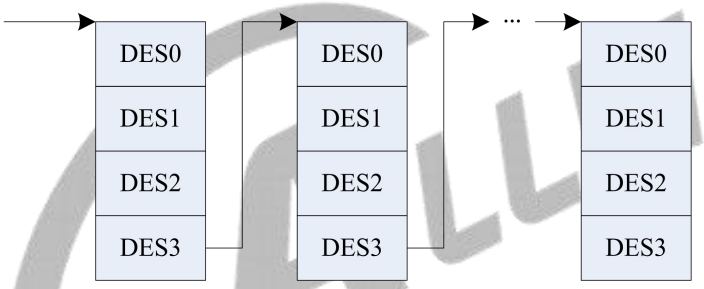
Figure 8-125 SPI Octal Input/dual Output Mode (8-8-8)



8.17.3.8 SPIFC Private DMA

The private DMA adopts the chained descriptor structure. The address and size of the first descriptor are configured by registers. After getting the first descriptor, the hardware will obtain the data from the address recorded in the descriptors. When the current transfer finishes, the hardware will continue to obtain descriptors based on the address of the next descriptor given by the previous descriptor until the terminal character is found. Then, a DMA transfer ends.

Figure 8-126 Descriptor Structure Diagram



The private DMA also supports SPI parameter configuration. The SPI transfer can be configured by the parameters of the descriptors 4-7.

Descriptor0 Definition

Bits	Descriptor
31:7	Reserved
6:4	HBURST_TYPE indicate hburst len 000: SINGLE, hburst_len = 1 011: INCR4, hburst_len = 4 101: INCR8, hburst_len = 8 111: INCR16, hburst_len = 16
3:2	/
1	DMA_DIR

Bits	Descriptor
	DMA Write Process or Read Process 0: Read 1:Write
0	DMA_FINISH_FLAG DMA Finish Flag

Descriptor1 Definition

Bits	Descriptor
31:24	DMA_BLK_LEN DMA Block Len Mode 0: 8Byte 1: 16Byte 2: 32Byte 3: 64Byte Recommended Configuration： The data volume of DMA_BLK_LEN is greater than or equal to that of HBURST_TYPE.
23:17	/
16:0	DMA_DATA_LEN Indicate the data byte number of current DMA operation.

Descriptor2 Definition

Bits	Descriptor
31:0	DMA_Buffer_ SADDR The real address is as below The word address is needed, namely, the byte address abandons the low 2 bits.

Descriptor3 Definition

Bits	Descriptor
31:0	NEXT_DESCRIPTOR_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present, which are word (4byte) address (The lower two bits are deleted from the byte address).

Descriptor4 Definition

Bit	Description
31:30	/
29	CMD_DTR CMD DTR Control

Bit	Description
	1: CMD DTR 0: CMD not DTR CAUTION: When CMD DTR, DTR must be on and CMD2 is required.
28	COMMAND_TRANS_EN Set to '1' if command data need trans to device SPI Controller FSM Phase Enable 1: Enable 0:Disable
27:25	/
24	ADDRESS_TRANS_EN Set to '1' if address need trans to device SPI Controller FSM Phase Enable 1: Enable 0:Disable
23:21	/
20	MODE_BIT_TRANS_EN Set to '1' if Mode bit need trans after address SPI Controller FSM Phase Enable 1: Enable 0:Disable
19:17	/
16	DUMMY_BIT_TRANS_EN Dummy Bit State Enable SPI Controller FSM Phase Enable 1: Enable 0:Disable
15:13	/
12	TX_DATA_EN Set to '1' if Data Need Trans SPI Controller FSM Phase Enable 1: Enable 0:Disable
11:9	/
8	RX_DATA_EN Set to '1' if Data Need Receive SPI Controller FSM Phase Enable 1: Enable 0:Disable
7:0	/

Descriptor5 Definition

Bit	Description

Bit	Description
31:0	ADDR_OPCODE Address Content Trans Through SPI

Descriptor6 Definition

This register should be setup while the controller is idle.

Bit	Description
31:24	CMD_OPCODE Command Content Trans Through SPI
23:16	MODE_OPCODE Mode Content Trans Through SPI
15:8	CMD_OPCODE2 Command2 Content Trans Through SPI
7:6	CMD_TRANS_TYPE Command Transfer Type 00: Command can be Shifted to the device on DQ0 01: Command can be Shifted to the device on DQ0 and DQ1 10: Command can be Shifted to the device on DQ0- DQ3 11 : Command can be Shifted to the device on DQ0-DQ7
5:4	ADDR_TRANS_TYPE Address Transfer Type 00: Address can be Shifted to the device on DQ0 01: Address can be Shifted to the device on DQ0 and DQ1 10: Address can be Shifted to the device on DQ0- DQ3 11: Address can be Shifted to the device on DQ0-DQ7
3:2	MODE_BIT_TRANS_TYPE Mode Bit Transfer Type 00: Mode Bit can be Shifted to the device on DQ0 01: Mode Bit can be Shifted to the device on DQ0 and DQ1 10: Mode Bit can be Shifted to the device on DQ0- DQ3 11: Mode Bit can be Shifted to the device on DQ0-DQ7
1:0	DATA_TRANS_TYPE Data Transfer Type 00: Opcode can be Shifted to the device on DQ0 only 01: Opcode can be Shifted to the device on DQ0 and DQ1 only 10: Opcode can be Shifted to the device on DQ0- DQ3 11: Opcode can be Shifted to the device on DQ0-DQ7

Descriptor7 Definition

Bit	Description
31	DATA_TRANS_NUM[16]
30:29	

Bit	Description
28	SPI_NORMAL_EN if dma config spi, this bit start SPI FSM.
27:25	/
24	ADDR_SIZE_MODE Address Size Mode 0: Address Size 24bit. 1: Address Size 32bit.
23:16	DUMMY_TRANS_NUM Number of Dummy Cycles A value of 0 = 1 Cycle A value of 1 = 1 Cycle ... A value of N = N Cycle
15:0	DATA_TRANS_NUM Num of Data Trans Through SPI(Byte) 0: Non-Write. 1: Write 1 Byte. 2: Write 2 Bytes. 3: Write 3 Bytes. ..... 65535: Write 65535 Bytes. **Note: These Bits Indicate number of data bytes in a CHIP SELECT period. Notice the difference between DATA_TRANS_NUM here and DMA_DATA_LEN in Descriptor1.**

8.17.4 Programming Guidelines

8.17.4.1 DMA Transfer

The software operation of the SPI DMA transfer is divided into 5 steps. 5 steps are described in detail in the following sections.

Step 1 System Setup

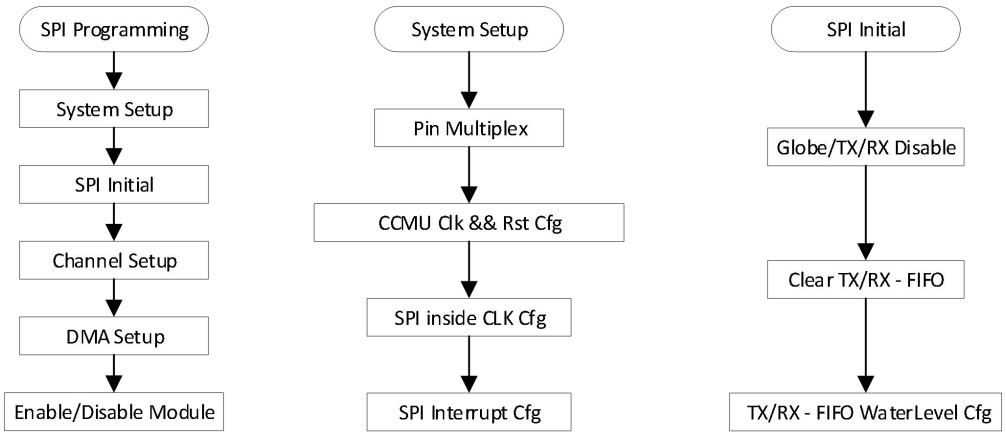
Step 2 SPI Initialization

Step 3 Channel Setup

Step 4 DMA Setup

Step 5 Enable SPI

Figure 8-127 SPI Programming flow



8.17.4.2 System Setup

Step 1 Configure SPI Pin

Programming the GPIO.

Step 2 Configure SPI Clock and Reset in CCU

Configure SPI ref clock, AHB Clock, De-assert SPI ref Reset, and AHB reset in Clock Controller Unit (CCU).

Step 3 Configure SPI Internal Working Clock

a) Configure clock source (SPI_TIMING_CFG[0x000C])

- STR Mode

  Write 0 to the CLK_SPI_SRC_SEL bit (bit [24]), the CLK_SCK_SRC_SEL bit (bit [25]) bit, and the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit.

- DTR Mode

  Write 0 to the CLK_SPI_SRC_SEL bit (bit [24]) and the CLK_SCK_SRC_SEL bit (bit [25]) bit.

  Write 1 to the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit.

NOTE

When the value of the CLK_SCKOUT_SRC_SEL bit (bit [26]) bit is 1, the real output clock frequency of SPIF-CLK signal is the SPIFC clock frequency divided by 2.

b) Generate the sckr of SPI data receiving

- Configure SCKR delay mode (SPI_TIMING_CFG[0x000C]). Refer to the section SPI Run Clock and Sample Mode for more details.

SCKR_DLY_MODE_SEL (bit [20]): Select delay mode. Writing 0 is the digital delay, and writing 1 is the digital and analog delay.

- Configure the digital delay of SCKR

  SPI_TIMING_CFG[0x000C], DIGITAL_SCKR_DELAY_CFG (bit[18:16]): digital delay volume. (step length: 0.5 clock)

- Configure the analog delay of SCKR

  SPI_TIMING_CFG[0x000C], ANALOG_SAMP_DL_SW_VALUE (bit[5:0])

c) Generate SPI output clock

- Select SPI working mode (SPI_MODE). Refer to the section SPI Flash Controller Clock Mode for more details.
- Configure SPI_GLOBAL_CTRL[0x0004]:

  SPI_CPOL (bit [5]): Clock Polarity

  SPI_CPHA (bit [4]): Clock Phase

- DTR switch (SPI_GLOBAL_CTRL[0x0004])

  DTR_EN (bit [16]): It is closed by default.

Step 4 Configure SPI Interrupt

Configure the SPI_INT_EN (0x0014[31:0]) as 0.

8.17.4.3 SPI Initialization

After the system setup, the registers of SPI can be setup. At first, the SPI needs to be initialized.

Step 1 Disable the SPI_GLOBAL_CTRL.

SPI_NMODE_EN (bit [2]): Write 0.

Step 2 Reset TX/RX FIFO (SPI_GLOBAL_CTRL_ADD[0x0008])

Reset the CDC-BUF/FIFO of TX channel: Write 1 to CDC_WF_SRST to reset the WR_BUFF and WR_FIFO in SPI_WR_BUF_CTRL and the SWF in SPI_TX_INTERFACE.

Reset the CDC-BUF/FIFO of RX channel: Write 1 to CDC_RF_SRST.

Step 3 Water Lever

Configure the water level of FIFO.

SPI_CDC_FIFO_TRIG_LEVEL[0x004C]

8.17.4.4 Channel Setup

Select SPI Channel Parameter Resource

- SPI channel parameter resources:

- CPU is configured by AHB.
- The private DMA fetches descriptors and parses the descriptors 4-7.

- Configure SPI channel parameter sources: SPI_GLOBAL_CTRL[0x0004] and SPI_CFG_MODE(bit[0])
  - 0: Source from CPU
  - 1: Source from DMA descriptor

NOTE

If the parameters source from CPU, configure in reference to all the guidelines in the section Channel Setup. If the parameters source from DMA, configure in reference to the first two guidelines in the section 8.17.4.4 Channel Setup.

SPI Interface Configuration—Public Configuration

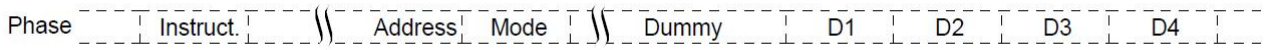
Step 1 CS Delay Configuration：SPI_CS_DELAY[0x001C]

- CSDA (bit [23:16]): The intervals of two adjacent CS enable. The minimum interval is 1sclk. The actual value is CSDA+1.
- CSEOT (bit [15:8]): After the SCLK_OUT is invalid, the CS signal will be de-asserted after CSEOT SCLK. The minimum interval is 1sclk. The actual value is CSEOT+1.
- CSSOT (bit [7:0]): After the SCLK_OUT is valid, the CS signal will be asserted after CSSOT SCLK. The minimum interval is 1sclk. The actual value is CSSOT+1.

Step 2 Activate SPI Trans Phase (SPI_TRANS_PHA_CFG[0x0020])

In a transmission of the SPI interface, the transferring content of I/O wire is as follows. Enable the corresponding Trans Phase based on the content to be transferred.

Figure 8-128 SPI Transfer Phase Flow Diagram



- COMMAND_TRANS_EN (bit [28]): Command (Instruct) Transfer Enable
- ADDRESS_TRANS_EN (bit [24]): Address Transfer Enable
- MODE_BIT_TRANS_EN (bit [20]): Mode Transfer Enable
- DUMMY_BIT_TRANS_EN (bit [16]): Dummy Transfer Enable
- TX_DATA_EN (bit [12]): Enable TX data transfer.
- RX_DATA_EN (bit [8]): Enable RX data transfer.

NOTE

RX_DATA_EN and TX_DATA_EN cannot be activated at the same time.

Step 3 Configure the number of I/O used by TransPhase. (SPI_TRANS_CFG2[0x0028])

- CMD_TRANS_TYPE (bit [13:12])
- ADDR_TRANS_TYPE (bit [9:8])
- MODE_BIT_TRANS_TYPE (bit [5:4])
- DATA_BIT_TRANS_TYPE (bit [1:0])

Step 4 Configure the transferring number of TransPhase (SPI_TRANS_NUM[0x002C])

SPI Interface Configuration—Normal Mode

Configure the contents of all TransPhase

- ADDR: SPI_TRANS_CFG1[0x0024], ADDR_OPCODE (bit [31:0])
- CMD: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[31:24])
- MODE: SPI_TRANS_CFG2[0x0028], CMD_OPCODE (bit[23:16])

SPI Interface Configuration—BIT Mode

Refer to the functions of SPI Bit Mode (3-Wire/4-Wire).

8.17.4.5 DMA Setup

DMA Configuration Registers

Step 1 Configure the descriptor size and starting address of the first descriptor.

- SPI_DMA_CTRL[0x0040]: DMA_DESCRIPTOR_LEN（bit[11:4]）
- SPI_DESCRIPTOR_SADDR[0x0044]

Step 2 Initiate DMA

SPI_DMA_CTRL[0x0040]，CFG_DMA_START（bit[0]）

DMA Configuration

Step 1 In the DMA register, configure the size and the starting address of storage location for the first descriptor.

Step 2 Configure the first DMA descriptor and store the corresponding address in the step 1.

- Descriptor0
  - AHB Master Burst Configuration

HBURST_TYPE (bit [6:4]): Support SINGLE/INCR4/INCR8/INCR16 mode.

- DMA Handling Direction Configuration

  DMA_DIR (bit [1]): Read by DMA, or Write by DMA.

- DMA Finish Flag

  DMA_FINISH_FLAG (bit [0]): Currently the memory space allocated by the CPU to DMA may be a part of the total data volume to be transferred. For instance, the 256 Byte memory space is allocated to transfer 1 MB data. In this situation, a DMA descriptor points to the allocated 256 Byte data location and the next descriptor to fetch data. When the data of the last descriptor is fetched by DMA, the stop bit should be pulled up to terminate a DMA handling.

➢ Descriptor1

- DMA_BLK_LEN ([31:16])

  DMA BLK length. It indicates the size of each DMA packet, with multiples of 8 Byte aligned to achieve the optimized rate when accessing storage.

- DMA_DATA_LEN (bit [15:0])

  It indicates the data volume indicated by the current descriptor of DMA

➢ Descriptor2

It indicates the data storage location of current descriptor.

➢ Descriptor3

It indicates the storage location of the next descriptor.

➢ Descriptor4-7

The SPI configuration parameters. When setting parameters with DMA for SPI, the content of descriptors is configured to SPI.

8.17.4.6 Enable SPI

Normal Mode

SPI_GLOBAL_CTRL[0x0004]，SPI_NMODE_EN (bit[2])

Write 1 to the SPI_NMODE_EN, then it will be auto pulled down.

8.17.4.7 CPU Transfer

The software operation of CPU transfer is almost the same as DMA transfer. There are still two main differences. One difference is that when CPU transfer, channel parameter cannot come from DMA descriptors. SPI_GLOBAL_CTRL[0x0004], SPI_CFG_MODE(bit[0]) must be set 0. All parameters should come from REGISTER FILE.

SPI_GLOBAL_CTRL[0x0004], SPI_CPU_MODE_EN(bit[20]) is used to start CPU transfer (Different from descriptor and SPI_GLOBAL_CTRL[0x0004], SPI_NMODE_EN(bit[2])).

Another difference is that when reading data from Register [0x0210], it is recommended to read SPI_CDC_FIFO_STA[0x0050], RF_CNT([bit5-0]), especially when total read number is not integer multiple of trigger level. When writing data to Register [0x0220], it is always ready as long as trigger level is not reached.

NOTE

Register [0x0040] and [0x0044] are not used in CPU transfer.

8.17.4.8 Status Reading

The software operation of STATUS READING is almost the same as CPU transfer. CMD_TRANS_EN and RX_DATA_EN must be set high because RX data path is used for status reading. MODE_BIT_TRANS_EN and DUMMY_BIT_TRANS_EN should be set accordingly. But STATUS OPCODE will not go through READ_FIFO and READ_BUFFER. Meanwhile, I/O Pins used should be set accordingly. SPI_STATUS_READ[0x0068] and SPI_STATUS_READ_2[0x006C] are used for STATUS READING. And to avoid endless reading and dead lock, CPU should tell the maximum reading times. Then, to start STATUS READING, SPI_READ_STATUS_MODE_EN should be set. In this mode, DATA_TRANS_NUM (002C, [15:0]) is suggested to be 1 and DTR_EN [0x0004, bit 16] is suggested to be 0.

8.17.5 Register List

Module Name	Base Address
SPIFC	0x047F 0000

Register Name	Offset	Description
SPI_GLOBAL_CTRL	0x0004	SPI Global Control Register
SPI_GLOBAL_CTRL_ADD	0x0008	SPI Global Control Additional Register
SPI_TIMING_CFG	0x000C	SPI Timing Configure Register
SPI_TIMING_DLY_STA	0x0010	SPI Timing Delay State Register
SPI_INT_EN	0x0014	SPI Interrupt Enable Register
SPI_INT_STA	0x0018	SPI Interrupt Status Register
SPI_CS_DELAY	0x001C	SPI Chipselect Delay Register
SPI_TRANS_PHA_CFG	0x0020	SPI Trans Phase Configure Register
SPI_TRANS_CFG1	0x0024	SPI Trans Configure1 Register
SPI_TRANS_CFG2	0x0028	SPI Trans Configure2 Register
SPI_TRANS_NUM	0x002C	SPI Trans Number Register
SPI_DMA_CTRL	0x0040	SPI DMA Control Register
SPI_DESCRIPTOR_SADDR	0x0044	SPI DMA Descriptor Start Address Register
SPI_CDC_FIFO_TRIG_LEVEL	0x004C	SPI CDC FIFO Trigger Level Register
SPI_CDC_FIFO_STA	0x0050	SPI CDC FIFO Status Register

Register Name	Offset	Description
SPI_BATC	0x0054	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0058	SPI Bit-Aligned CLOCK Configuration Register
SPI_TBR	0x005C	SPI TX Bit Register
SPI_RBR	0x0060	SPI RX Bit Register
SPI_STATUS	0x0064	SPI Status Register
SPI_STATUS_READ	0x0068	SPI READ Status Register
SPI_STATUS_READ2	0x006C	SPI READ Status Register_2
SPI_RX_DATA	0x0210	SPI RX Data Register
SPI_TX_DATA	0x0220	SPI TX Data Register

8.17.6 Register Description

8.17.6.1 0x0004 SPI Global Control Register (Default Value: 0x0000_0100)

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22	R/W	0x0	START_MODE 0：old start mode 1：new start mode
21	R/WAC	0x0	SPI_READ_STATUS_MODE_EN SPI READ STATUS Mode Enable 0: Disable 1: Enable This bit is not used for data transfer. It is used for status confirm. And when this operation ends, the last returned byte value is sent to 0x0064[31:24].
20	R/WAC	0x0	SPI_CPU_MODE_EN SPI CPU Mode Enable 0: Disable 1: Enable CPU transfer mode.
19	R/W	0x0	SPI_CLK_OUTPUT 0: Disable 1: Enable when the SPI_CLK_OUTPUT is enabled, the SPI FLASH CONTROLLER will convey the sclk from CCU to the spi_sck_out pin. This bit cannot be enabled in the process of data transmission to avoid anomaly.
18	R/W	0x0	SPI_TX_CFG_FBS Transmit Interface First Transmit Bit Select. 0: MSB First

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
			1: LSB First
17	R/W	0x0	SPI_RX_CFG_FBS Receive Interface First Transmit Bit Select. 0: MSB First 1: LSB First
16	R/W	0x0	DTR_EN Double Trans Rate Enable 0: Disable 1: Enable
15	R/W	0x0	SPI_WP_EN 0: Disable 1: Enable In Standard SPI or Dual SPI, SPI PIN Write Protect Function can be Open In the open status, SPI_WP_IO2_OUT is enabled. The exact polarity is decided by the configuration of SPI_WP_POL. In the closed status, SPI_WP_IO2_OUT is controlled by hardware. The exact polarity is decided by the controller.
14	R/W	0x0	SPI_WP_POL SPI PIN Write Protect Polar 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
13	R/W	0x0	SPI_HOLD_EN 0: Disable 1: Enable In Standard SPI or Dual SPI, SPI PIN HOLD Function can be Open In the open status, SPI_HOLD_IO3_OUT is enabled. The exact polarity is decided by the configuration of SPI_HOLD_POL. In the closed status, SPI_HOLD_IO3_OUT is controlled by hardware. The exact polarity is decided by the controller.
12	R/W	0x0	SPI_HOLD_POL SPI PIN HOLD Polar 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
11	/	/	/
10	R/W	0x0	DQS_RX_EN

Offset: 0x0004			Register Name: SPI_GLOBAL_CTRL
Bit	Read/Write	Default/Hex	Description
			Receive DQS Signal Enable 0: Disable 1: Enable
9	R/W	0x0	DUMMY_BIT_POL Dummy Bit Trans Value 0: Dummy bit Trans 0 1: Dummy bit Trans 1
8	R/W	0x1	SPI_CS_POL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
7:6	R/W	0x0	SPI_CS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted
5	R/W	0x0	SPI_CPOL SPI Clock Polarity Control 0: Active High Polarity. 1: Active Low Polarity.
4	R/W	0x0	SPI_CPHA SPI Clock/Data Phase Control 0: Phase 0(Leading Edge for Sample Data) 1: Phase 1(Leading Edge For Setup Data)
3	/	/	/
2	R/WAC	0x0	SPI_NMODE_EN SPI Normal Mode Enable 0: Disable 1: Enable DMA transfer mode.
1	/	/	/
0	R/W	0x0	SPI_CFG_MODE SPI Parameter Config Source in normal(DMA) mode. Set to 0 When CPU Transfer. 0: From REGISTER 1: From DMA Descriptor

8.17.6.2 0x0008 SPI Global Control Additional Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: SPI_GLOBAL_CTRL_ADD
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R/WAC	0x0	SPI_FLASH_DMA_END Terminate the DMA Chain after the present BLK is done. After the DMA chain terminates, set 1 to this bit to stop DMA transmission after the DMA module finishes the BLK whether the current chain completes or the finish_flag is set to 1. DMA_END and SPI_SRST should be used together: Enable the DMA_END first, and then enable the SPI_FLASH_SRST after DMA_END is cleared.
3	R/WAC	0x0	SPI_FLASH_SRST Reset All the Logic in SPI Flash (DMA chain is not included)
2	/	/	/
1	R/WAC	0x0	CDC_WF_SRST Transfer FIFO Software Reset, In SPI_WR_BUF_CTRL Module 0: Auto Clear to 0. 1: Reset Transfer FIFO. Writing 1 to this bit will reset the control portion of the transfer FIFO, and auto clear to 0 when completing reset operation. Writing 0 to this bit has no effect.
0	R/WAC	0x0	CDC_RF_SRST Receiver FIFO Software Reset, In SPI_RD_BUF_CTRL Module 0: Auto Clear to 0. 1: Reset Receiver FIFO. Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.

8.17.6.3 0x000C SPI Timing Configure Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26	R/W	0x0	CLK_SCKOUT_SRC_SEL SPI Output Clk Select

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
			Select the rate of SPI output clock (SCK_OUT). 0: Original Clock 1: Two-frequency Clock
25	R/W	0x0	CLK_SCK_SRC_SEL SPI Interface Clock Select 0: Original Clock 1: Two-frequency Clock
24	R/W	0x0	CLK_SPI_SRC_SEL SPI Inter Process Clock Select 0: Original Clock 1: Two-frequency
23:22	/	/	/
21	R/W	0x0	SCKT_DELAY_MODE_SEL SCKT Delay Mode Select 0: Select the SCKT without delay 1: Select the SCKT after the analog delay chain adjustment
20	R/W	0x0	SCKR_DELAY_MODE_SEL SCKR Delay Mode Select 0: digital delay 1: digital delay + analog delay
19	/	/	/
18:16	R/W	0x0	DIGITAL_SCKR_DELAY_CFG Digital SCKR Delay Value Config, Step 0.5 spi_clk 000: delay 0 clk 001: delay 0.5 clk 010: delay 1 clk 011: delay 1.5 clk 100: delay 2 clk 101: delay 2.5 clk 110: delay 3 clk 111: delay 3.5 clk
15	R/W	0x0	ANALOG_SAMP_DL_CAL_START_TX Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R/W	0x0	ANALOG_SAMP_DL_SW_EN_TX Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
13:8	R/W	0x0	ANALOG_SAMP_DL_SW_VALUE_TX Sample Delay Software Value

Offset: 0x000C			Register Name: SPI_TIMING_CFG
Bit	Read/Write	Default/Hex	Description
			The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.
7	R/W	0x0	ANALOG_SAMP_DL_CAL_START_RX Sample Delay Calibration Start When set, start sample delay chain calibration.
6	R/W	0x0	ANALOG_SAMP_DL_SW_EN_RX Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
5:0	R/W	0x0	ANALOG_SAMP_DL_SW_VALUE_RX Sample Delay Software Value The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

8.17.6.4 0x0010 SPI Timing Delay State Register (Default Value: 0x0000_2020)

Offset: 0x0010			Register Name: SPI_TIMING_DLY_STA
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ANALOG_SAMP_DL_CAL_DONE_TX Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
14	/	/	/
13:8	R	0x20	ANALOG_SAMP_DL_TX Sample Delay Value It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.

Offset: 0x0010			Register Name: SPI_TIMING_DLY_STA
Bit	Read/Write	Default/Hex	Description
7	R	0x0	ANALOG_SAMP_DL_CAL_DONE_RX Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
6	/	/	/
5:0	R	0x20	ANALOG_SAMP_DL_RX Sample Delay Value It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.

8.17.6.5 0x0014 SPI Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0014			Name: SPI_INT_EN
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	READ_STATUS_DONE_INT_EN 0: Disable. 1: Enable.
27	R/W	0x0	READ_STATUS_TIME_OUT_INT_EN 0: Disable. 1: Enable.
26	R/W	0x0	SPI_TRANS_DONE_INT_EN SPI Transmit Finish Interrupt Enable 0: Disable. 1: Enable.
25	/	/	/
24	R/W	0x0	DMA_TRANS_DONE_INT_EN DMA Chain Transmit Finish Interrupt Enable 0: Disable. 1: Enable.
23	R/W	0x0	DQS_RF_ODD_UDF_INT_EN DQS Receive FIFO Underflow Interrupt Enable 0: Disable.

Offset: 0x0014			Name: SPI_INT_EN
Bit	Read/Write	Default/Hex	Description
			1: Enable.
22	R/W	0x0	DQS_RF_ODD_OVF_INT_EN DQS Receive FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
21	R/W	0x0	DQS_RF_EVEN_UDF_INT_EN DQS Receive FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
20	R/W	0x0	DQS_RF_EVEN_OVF_INT_EN DQS Receive FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
19:12	/	/	/
11	R/W	0x0	WF_UDF_INT_EN Write FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
10	R/W	0x0	WF_OVF_INT_EN Write FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
9	R/W	0x0	RF_UDF_INT_EN Read FIFO Underflow Interrupt Enable 0: Disable. 1: Enable.
8	R/W	0x0	RF_OVF_INT_EN Read FIFO Overflow Interrupt Enable 0: Disable. 1: Enable.
7:5	/	/	/
4	R/W	0x0	WF_RDY_INT_EN Write FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.
3:1	/	/	/
0	R/W	0x0	RF_RDY_INT_EN Read FIFO Ready Request Interrupt Enable 0: Disable. 1: Enable.

8.17.6.6 0x0018 SPI Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W1C	0x0	READ_STATUS_DONE_INT READ_STATUS MODE Done Interrupt. When set, this bit indicates that at least one wanted bit has got expected value.
27	R/W1C	0x0	READ_STATUS_TIME_OUT_INT READ_STATUS MODE TIME OUT Interrupt. When set, this bit indicates that READ_STATUS MODE ends and in the written period, no wanted bit gets expected value.
26	R/W1C	0x0	SPI_TRANS_DONE_INT SPI Transmit Finish Interrupt
25	/	/	/
24	R/W1C	0x0	DMA_TRANS_DONE_INT DMA Chain Transmit Finish Interrupt Note: When set, this bit indicates that Write FIFO has underflow. Writing “1” to this bit clears it.
23	R/W1C	0x0	DQS_RF_ODD_UDF_INT DQS Receive FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing “1” to this bit clears it.
22	R/W1C	0x0	DQS_RF_ODD_OVF_INT DQS Receive FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing “1” to this bit clears it.
21	R/W1C	0x0	DQS_RF_EVEN_UDF_INT DQS Receive FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing “1” to this bit clears it.
20	R/W1C	0x0	DQS_RF_EVEN_OVF_INT DQS Receive FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing “1” to this bit clears it.
19:12	/	/	/
11	R/W1C	0x0	WF_UDF_INT Write FIFO underflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has underflow. Writing “1” to this bit clears it.
10	R/W1C	0x0	WF_OVF_INT

Offset: 0x0018			Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
			Write FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Write FIFO has overflowed. Writing “1” to this bit clears it.
9	R/W1C	0x0	RF_UDF_INT Read FIFO Underflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has underflow. Writing “1” to this bit clears it.
8	R/W1C	0x0	RF_OVF_INT Read FIFO Overflow Interrupt Flag Note: When set, this bit indicates that Read FIFO has overflowed. Writing “1” to this bit clears it.
7:5	/	/	/
4	R/W1C	0x1	WF_RDY_INT Write FIFO Ready Request Interrupt Flag 0: WF_WL > WF_EMPTY_TRIG_LEVEL. 1: WF_WL <= WF_EMPTY_TRIG_LEVEL. This bit is set any time if WF_WL <= WF_EMPTY_TRIG_LEVEL. Writing “1” to this bit clears it.
3:1	/	/	/
0	R/W1C	0x0	RF_RDY_INT Read FIFO Ready Request Interrupt Flag 0: RF_WL < RX_EMPTY_TRIG_LEVEL and rest total RX data byte number is larger than RX_EMPTY_TRIG_LEVEL. 1: RF_WL >= RX_EMPTY_TRIG_LEVEL, or rest total RX data byte number is smaller than RX_EMPTY_TRIG_LEVEL meanwhile RF_WL >= 1. This bit is set any time if condition is reached. Writing “1” to this bit clears it.

8.17.6.7 0x001C SPI Chipselect Delay Register (Default Value: 0x0000_0606)

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	DBG_SEL 0: The high 8 bits of debug signal are io*_oen, and the low 8 bits are 0. 1: The high 8 bits are WF_CNT, and the low 8 bits are RF_CNT. 2: The high 8 bits are WB_CNT, and the low 8 bits are

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
			RB_CNT. 3: The high 8 bits are DMA state machine, and the low 8 bits are SPI state machine. 4: Debug signal are read DRQ and write DRQ. 2'b0: dqs_rfifo_even water level; 4'b0: dqs_rfifo_odd water level.
23:16	R/W	0x0	CSDA Chip Select De-Assert The interval of two adjacent CS signal enable, namely, the interval of two SPI scheduling. The unit is the i_clk_spi_ref. The minimum interval A (CSDA=0) is 4 clk (used for ending SPI functions) The maximum A (CSDA=FB) is FF clk (used for ending SPI functions) When CSDA is X, the actual interval is X+A.
15:8	R/W	0x6	CSEOT Chip Select End of Transfer The interval between the rising edge of last output clock signal (SPI_CLK_OUT) and the CS signal disable. The unit is the reference clock The minimum interval B (CSEOT=0) is: DTR-TX: 3 clk DTR-RX: 5 clk STR-TX, CPOL=0: 3 clk STR-RX, CPOL=0: 4 clk STR-TX, CPOL=1: 2.5 clk STR-RX, CPOL=1: 3.5 clk When CSEOT is X, the actual interval is X+B. When using delay, the length of CSEOT should be larger than that of delay, or the data will be lost.
7:0	R/W	0x6	CSSOT Chip Select Start of Transfer The interval between the CS signal enable and the rising edge of the first output clock signal (SPI_CLK_OUT). The unit is the reference clock. The minimum interval C (CSSOT=0) is: CPOL=0: 1 clk CPOL=1: 1.5 clk When CSSOT is X, the actual interval is X+C. The minimum interval is recommended to be 6, or the

Offset: 0x001C			Register Name: SPI_CS_DELAY
Bit	Read/Write	Default/Hex	Description
			anomaly will occur in some special conditions.。 The minimum interval should be larger than 6 in NEW_START_MODE.

8.17.6.8 0x0020 SPI Transfer Phase Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_TRANS_PHA_CFG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	CMD_DTR CMD DTR Control 1: CMD DTR 0: CMD not DTR CAUTION: When CMD DTR, DTR_EN must be on and CMD2 is required.
28	R/W	0x0	COMMAND_TRANS_EN Set to 1 if command data need trans to device SPI Controller FSM Phase Enable 1: Enable 0:Disable
27:25	/	/	/
24	R/W	0x0	ADDRESS_TRANS_EN Set to 1 if address need trans to device SPI Controller FSM Phase Enable 1: Enable 0: Disable
23:21	/	/	/
20	R/W	0x0	MODE_BIT_TRANS_EN Set to 1 if Mode bit need trans after address SPI Controller FSM Phase Enable 1: Enable 0:Disable
19:17	/	/	/
16	R/W	0x0	DUMMY_BIT_TRANS_EN Dummy Bit State Enable SPI Controller FSM Phase Enable 1: Enable 0:Disable
15:13	/	/	/
12	R/W	0x0	TX_DATA_EN

Offset: 0x0020			Register Name: SPI_TRANS_PHA_CFG
Bit	Read/Write	Default/Hex	Description
			Set to 1 if Data Need Trans SPI Controller FSM Phase Enable 1: Enable 0: Disable The CPU channels should be configured before writing to this bit out of protection requirements.
11:9	/	/	/
8	R/W	0x0	RX_DATA_EN Set to '1' if Data Need Receive SPI Controller FSM Phase Enable 1: Enable 0: Disable The CPU channels should be configured before reading from this bit out of protection requirements.
7:0	/	/	/

8.17.6.9 0x0024 SPI Trans Configure1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SPI_TRANS_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	ADDR_OPCODE Address Content Trans Through SPI When the length of ADDR is configured as 24bit. To configure MSB first, use the low 24 bits of ADDR_OPCODE. Namely, the sending sequence is from bit23 to bit0 in ADDR_OPCODE [23:0]. To configure LSB first, use the high 24bits of ADDR_OPCODE. Namely, the sending sequence is from bit8 to bit31 in ADDR_OPCODE[31:8].

8.17.6.10 0x0028 SPI Trans Configure2 Register (Default Value: 0x0000_0000)

NOTE

This register should be setup while the controller is idle.

Offset: 0x0028			Register Name: SPI_TRANS_CFG2
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	CMD_OPCODE

Offset: 0x0028			Register Name: SPI_TRANS_CFG2
Bit	Read/Write	Default/Hex	Description
			Command Content Trans Through SPI
23:16	R/W	0x0	MODE_OPCODE Mode Content Trans Through SPI
15:8	R/W	0x0	CMD_OPCODE2 Command2 Content Trans Through SPI
7:6	R/W	0x0	CMD_TRANS_TYPE Command Transfer Type 00: Command can be Shifted to the device on DQ0 01: Command can be Shifted to the device on DQ0 and DQ1 10: Command can be Shifted to the device on DQ0- DQ3 11: Command can be Shifted to the device on DQ0-DQ7
5:4	R/W	0x0	ADDR_TRANS_TYPE Address Transfer Type 00: Address can be Shifted to the device on DQ0 01: Address can be Shifted to the device on DQ0 and DQ1 10: Address can be Shifted to the device on DQ0- DQ3 11 : Address can be Shifted to the device on DQ0-DQ7
3:2	R/W	0x0	MODE_BIT_TRANS_TYPE Mode Bit Transfer Type 00: Mode Bit can be Shifted to the device on DQ0 01: Mode Bit can be Shifted to the device on DQ0 and DQ1 10: Mode Bit can be Shifted to the device on DQ0- DQ3 11 : Mode Bit can be Shifted to the device on DQ0-DQ7
1:0	R/W	0x0	DATA_TRANS_TYPE Data Transfer Type 00: Opcode can be Shifted to the device on DQ0 only 01: Opcode can be Shifted to the device on DQ0 and DQ1 only 10: Opcode can be Shifted to the device on DQ0- DQ3 11 : Opcode can be Shifted to the device on DQ0-DQ7

8.17.6.11 0x002C SPI Trans Number Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SPI_TRANS_NUM
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DATA_TRANS_NUM[16]

Offset: 0x002C			Register Name: SPI_TRANS_NUM
Bit	Read/Write	Default/Hex	Description
30:25	/	/	/
24	R/W	0x0	ADDR_SIZE_MODE Address Size Mode 0: Address Size 24bit. 1: Address Size 32bit.
23:16	R/W	0x0	DUMMY_TRANS_NUM Number of Dummy Cycles A value of 0 = 1 Cycle A value of 1 = 1 Cycle ... A value of N = N Cycle
15:0	R/W	0x0	DATA_TRANS_NUM Num of Data Trans Through SPI(Byte) 0: Non-Write. 1: Write 1 Byte. 2: Write 2 Bytes. 3: Write 3 Bytes. ..... 65535: Write 65535 Bytes. Note: These Bits Indicate Current Operation is Write Data To Flash.

8.17.6.12 0x0040 SPI DMA Control Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: SPI_DMA_CTRL
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:4	R/W	0x0	DMA_DESCRIPTOR_LEN DMA Descriptor Length In the initial design, there are eight DMA descriptors and the length of each descriptor is 4 Byte. In this bit, the length of descriptor is set to 32=8*4Byte.
3:1	/	/	/
0	R/WAC	0x0	CFG_DMA_START Config DMA Start Signal When all the DMA parameters are configured well, pull up a pulse of this signal to enable DMA chain.

8.17.6.13 0x0044 SPI DMA Descriptor Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SPI_DESCRIPTOR_SADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	FIRST_DESCRIPTOR_SADDR First Descriptor Start Address The WORD address is needed.

8.17.6.14 0x004C SPI CDC FIFO Trigger Level Register (Default Value: 0x1001_1a10)

Offset: 0x004C			Name: SPI_CDC_FIFO_TRIG_LEVEL
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:24	R/W	0x10	WF_DMA_TRIG_LEVEL Write FIFO DMA Request Trigger Level (WORD) In the case of DMA conveying, WF_DMA_TRIG_LEVEL should be set to be less than or equal to 16 to avoid the efficiency reduction.
23:22	/	/	/
21:16	R/W	0x01	WF_CPU_TRIG_LEVEL Write FIFO CPU Request Trigger Level (WORD) In the case of DMA conveying, when WF_CNT is less than WF_CPU_TRIG_LEVEL, WF_RDY interrupts will be sent out.
15:14	/	/	/
13:8	R/W	0x1a	RF_FULL_TRIG_LEVEL Read FIFO Full Request Trigger Level (WORD) RF_FULL_TRIG_LEVEL is recommended to be less than or equal to 26 to avoid FIFO anomaly. RF_FULL_TRIG_LEVEL only decides the volume of RX_FIFO, not influencing the RX_RDY_INT.
7:6	/	/	/
5:0	R/W	0x10	RF_RDY_TRIG_LEVEL Read FIFO RDY Request Trigger Level (WORD). In the case of CPU reading data, when the rest data volume is larger than RF_RDY_TRIG_LEVEL, and RF_CN is greater than RF_RDY_TRIG_LEVEL; or the rest data volume is less than RF_RDY_TRIG_LEVEL, and RF_CNT is larger than 1, the RF_RDY_INT will be sent out.

8.17.6.15 0x0050 SPI CDC FIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0050			Name: SPI_CDC_FIFO_STA
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:26	R	0x0	Flash Controller State Debug Reg.
25	R	0x0	WB_WR Write Buffer Could or Not Write.
24:21	R	0x0	WB_CNT Write Buffer Counter(Byte) These Bits Indicate Number of Bytes in Write Buffer.
20	R	0x0	RB_RD_RDY_STATE Read Buffer Could or Not Read
19:16	R	0x0	RB_CNT Read Buffer Counter(Byte) These Bits Indicate Number of Bytes in Read Buffer.
15:14	/	/	/
13:8	R	0x0	WF_CNT Write FIFO Counter (Level) These Bits Indicate Water Level in Write FIFO. 0: 0 level in Write FIFO. 1: 1 level in Write FIFO. ... 32: 32 level in Write FIFO.
7:6	/	/	/
5:0	R	0x0	RF_CNT Read FIFO Counter (Level) These Bits Indicate Water Level in Read FIFO. 0: 0 level in Read FIFO. 1: 1 level in Read FIFO. ... 32: 32 level in Read FIFO.

8.17.6.16 0x0054 SPI Bit-Aligned Transfer Configure Register (Default Value: 0x0000_00A0)

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start t1o transfer the serial bit's frame, it is only valid when Work Mode Select==0x10/0x11.

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
			0: Idle 1: Initiates transfer. Write "1" to this bit will start to transfer serial bits' frame (the value comes from the SPI TX Bit Register or SPI RX Bit Register), and will auto clear after the bursts transfer completely. Write '0' to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0 - Standard Sample Mode 1 - Delay Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in SPI TX Bit Register (or SPI RX Bit Register) has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed Note: It is only valid when Work Mode Select==0x10/0x11.
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable Note: It is only valid when Work Mode Select==0x10/0x11.
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
			Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.
15:14	/	/	/
13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit ... 100000: 32bits Other values: reserved **Note: It is only valid when Work Mode Select==0x10/0x11, and can't be written when TCE=1.**
7	R/W	0x1	SS_LEVEL When control SS signal manually, set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) **Note: It is only valid when Work Mode Select==0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices

Offset: 0x0054			Register Name: SPI_BATC
Bit	Read/Write	Default/Hex	Description
			00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted **Note: It is only valid when Work Mode Select= =0x10/0x11, and only work in Mode0, can't be written when TCE=1.**
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in Standard SPI, Dual-Output/Dual Input SPI, Dual IO SPI and Quad-Output/Quad-Input SPI. 01: Reserve 10: Data frame is bit aligned in 3-Wire SPI 11: Data frame is bit aligned in Standard SPI

8.17.6.17 0x0058 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select==0x10/0x11.

Offset: 0x0058			Register Name: SPI_BA_CCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)).

8.17.6.18 0x005C SPI TX Bit Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select==0x10/0x11.

Offset: 0x005C			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description

Offset: 0x005C			Register Name: SPI_TBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. Note: In the process of transmission, the LSB is transmitted first.

8.17.6.19 0x0060 SPI RX Bit Register (Default Value: 0x0000_0000)

NOTE

This register is only valid when Work Mode Select==0x10/0x11.

Offset: 0x0060			Register Name: SPI_RBR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. Note: In the process of transmission, the LSB is transmitted first.

8.17.6.20 0x0064 SPI STATUS Register (Default Value: 0x0000_0885)

Offset: 0x0064			Register Name: SPI_STATUS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	READ_STATUS_RESULT
23:12	/	/	/
11:8	R	0x8	DQS_RF_ODD_WL Rest of space.
7：4	R	0x8	DQS_RF_EVEN_WL Rest of space.
3	R	0x0	WF_FULL Write FIFO Full Interrupt Flag 0: Write FIFO is Not Full. 1: Write FIFO is Full. Note: This bit is set when the Write FIFO is full.
2	R	0x1	WF_EMPTY Write FIFO Empty Request Interrupt Flag

Offset: 0x0064			Register Name: SPI_STATUS
Bit	Read/Write	Default/Hex	Description
			0: Write FIFO always contains one or more bytes. 1: Write FIFO has been empty. Note: This bit is set if the Write FIFO is empty.
1	R	0x0	RF_FULL Read FIFO Full Interrupt Flag 0: Not Full. 1: Read FIFO has been Full. Note: This bit is set when Read FIFO is full.
0	R	0x1	RF_EMPTY Read FIFO Empty Interrupt Flag 0: Not Empty. 1: Read FIFO has been Empty. Note: This bit is set if the Read FIFO is empty.

8.17.6.21 0x0068 SPI STATUS READ Register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: SPI_STATUS_READ
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	SPI_READ_STATUS_DETECTED_BIT_POSITION These 8 bits are used to distinguish the wanted bit in a STATUS BYTE. For every bit that CPU cares, put a high level in the corresponding bit position.
15:8	/	/	/
7:0	R/W	0x0	SPI_READ_STATUS_DETECTED_BIT_VALUE These 8 bits are used to distinguish the wanted bit in a STATUS BYTE. For every bit that CPU cares, put the level that CPU wants in the corresponding bit position. And when one bit is detected the same value, READ_STATUS_MODE shall stop and return a DONE interrupt. Then CPU shall check the exact result in 0x0068[31:24].

8.17.6.22 0x006C SPI STATUS READ Register_2(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: SPI_STATUS_READ2
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x0	MAXIMUM_STATUS_READ_TIME These 14 bits are used to tell the module that when

Offset: 0x006C			Register Name: SPI_STATUS_READ2
Bit	Read/Write	Default/Hex	Description
			reading FLASH status, how many times it should read before it stops reading and instead return a TIME_OUT INTERRUPT to avoid dead lock. NOTE：Suggested minimum value is 1.
15:14	/	/	/
13:0	R/W	0x0	READ_STATUS_INTERVAL The INTERVAL is counted with 32KHz clock. These 14 bits are used to tell that when READING STATUS, after how many rising edge of the 32K clock should the module start a READ STATUS visit to the connected FLASH. NOTE：Suggested minimum value is 1.

8.17.6.23 0x0210 SPI RX Data Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: SPI_RX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_RX_DATA SPI RX Data.Non read when DMA transfer.

8.17.6.24 0x0220 SPI TX Data Register (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: SPI_TX_DATA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	SPI_TX_DATA SPI TX Data. Non write when DMA transfer.

8.18 UART

8.18.1 Overview

The universal asynchronous receiver transmitter (UART) provides an asynchronous serial communication with external devices, modem (data carrier equipment, DCE). It performs serial-to-parallel conversion on the data received from peripherals and transmits the converted data to the internal bus. It also performs parallel-to-serial conversion on the data that is transmitted to peripherals.

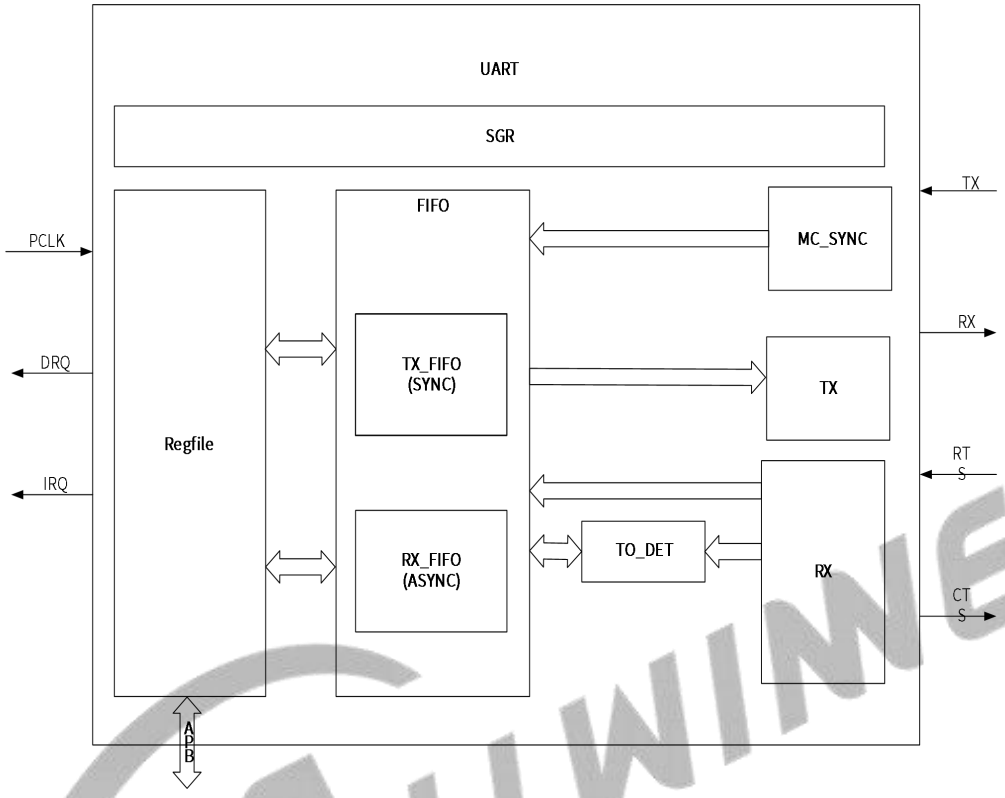
The UART has the following features:

- Up to 10 UART controllers
  - 8 UART controllers in CPUX domain: UART0, UART1, UART2, UART3, UART4, UART5, UART6, and UART7
  - 2 UART controllers in CPUS domain: S_UART0 and S_UART1
- Compatible with industry-standard 16450/16550 UARTs
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes for UART0, S_UART0, and S_UART1
  - Each of them is 128 bytes for UART1, UART2, UART3, UART4, UART5, UART6, and UART7
- The working reference clock is from the APB bus clock
  - Speed up to 10 Mbit/s with 160 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 5 Mbit/s with 80 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 3.75 Mbit/s with 60 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 characters, or 9 bits RS-485 format
- 1, 1.5 or 2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports IrDA-compatible slow infrared (SIR) format
- Supports auto-flow by using CTS & RTS (excluding UART0, S_UART0, and S_UART1)

8.18.2 Block Diagram

The following figure shows a block diagram of the UART.

Figure 8-129 UART Block Diagram



8.18.3 Functional Description

8.18.3.1 External Signals

The following table describes the external signals of UART.

Table 8-58 UART External Signals

Signal Name	Description	Type
UART0-TX	UART0 Data Transmitter	O
UART0-RX	UART0 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART1-CTS	UART1 Data Clear to Send	I
UART1-RTS	UART1 Data Request to Send	O
UART2-TX	UART2 Data Transmitter	O
UART2-RX	UART2 Data Receiver	I
UART2-CTS	UART2 Data Clear to Send	I
UART2-RTS	UART2 Data Request to Send	O
UART3-TX	UART3 Data Transmitter	O
UART3-RX	UART3 Data Receiver	I

Signal Name	Description	Type
UART3-CTS	UART3 Data Clear to Send	I
UART3-RTS	UART3 Data Request to Send	O
UART4-TX	UART4 Data Transmitter	O
UART4-RX	UART4 Data Receiver	I
UART4-CTS	UART4 Data Clear to Send	I
UART4-RTS	UART4 Data Request to Send	O
UART5-TX	UART5 Data Transmitter	O
UART5-RX	UART5 Data Receiver	I
UART5-CTS	UART5 Data Clear to Send	I
UART5-RTS	UART5 Data Request to Send	O
UART6-TX	UART6 Data Transmitter	O
UART6-RX	UART6 Data Receiver	I
UART6-CTS	UART6 Data Clear to Send	I
UART6-RTS	UART6 Data Request to Send	O
UART7-TX	UART7 Data Transmitter	O
UART7-RX	UART7 Data Receiver	I
UART7-CTS	UART7 Data Clear to Send	I
UART7-RTS	UART7 Data Request to Send	O
S-UART0-TX	S-UART0 Data Transmitter	O
S-UART0-RX	S-UART0 Data Receiver	I
S-UART1-TX	S-UART1 Data Transmitter	O
S-UART1-RX	S-UART1 Data Receiver	I

8.18.3.2 Clock Sources

The following table describes the clock sources of UART.

Table 8-59 UART Clock Sources

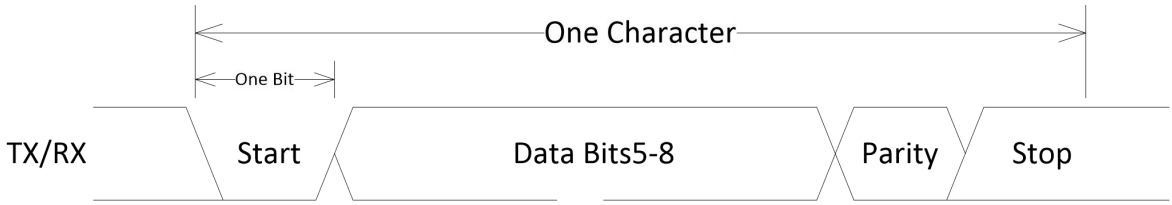
UART Interfaces	Clock Source	Description	Clock Module
UART0 to UART7	APB1 Bus	UART clock source. Refer to CCU for details on APB1.	CCU
S_UART0, S_UART1	APBS1 Bus	S_UART clock source. Refer to PRCM for details on APB1.	PRCM

8.18.3.3 Typical Applications and Timing Diagram

UART Serial Data Format

The following figure shows the UART serial data format. The start bit, data bit, parity bit, and stop bit can be configured.

Figure 8-130 UART Serial Data Format



Using UART for RTS/CTS Autoflow Control

Figure 8-131 shows the typical application diagram for RTS/CTS autoflow control. Figure 8-132 shows the data format of the RTS/CTS autoflow control.

Figure 8-131 Application Diagram for RTS/CTS Autoflow Control

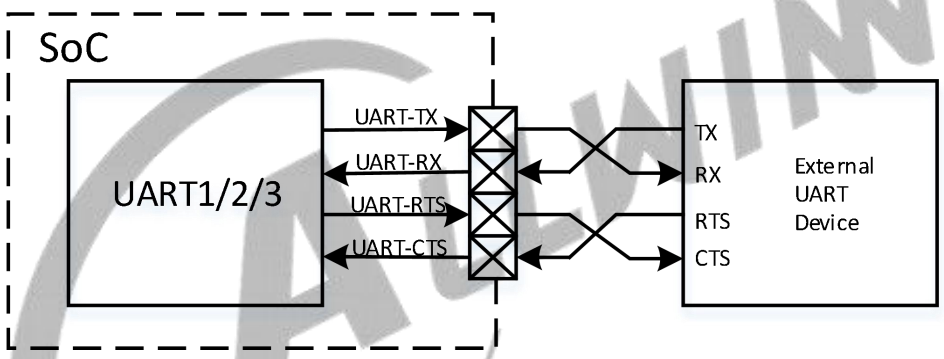
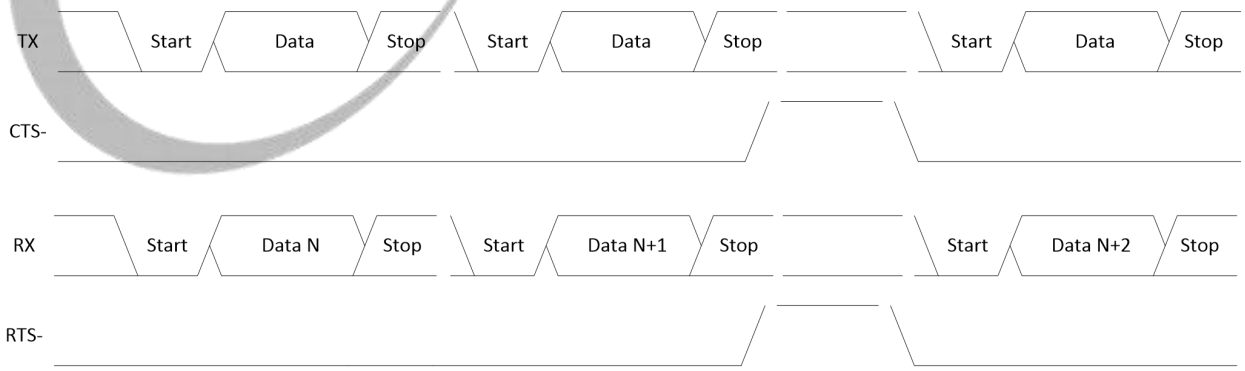


Figure 8-132 RTS/CTS Autoflow Control Data Format



Using UART for Serial IrDA

Figure 8-133 shows the application diagram for the IrDA transceiver. Figure 8-134 shows the data format of the serial IrDA.

Figure 8-133 Application Diagram for IrDA Transceiver

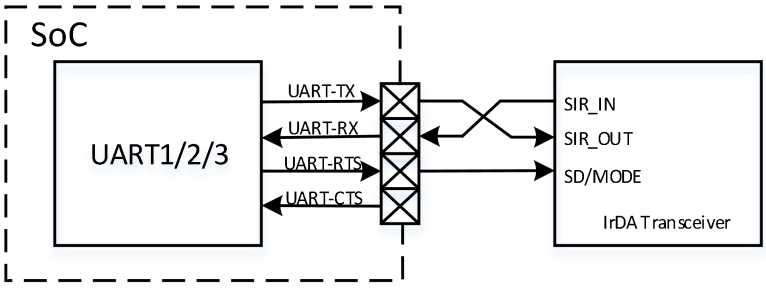
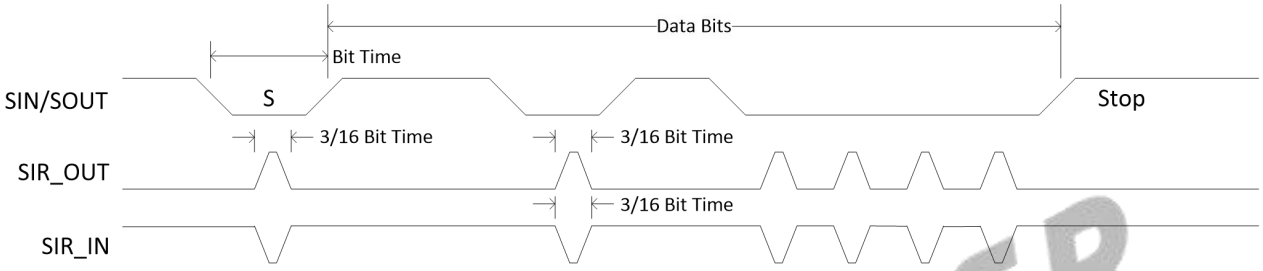


Figure 8-134 Serial IrDA Data Format



Using UART for RS-485

Figure 8-135 shows the application diagram for the RS-485 transceiver. Figure 8-136 shows the data format of the RS-485.

Figure 8-135 Application Diagram for RS-485 Transceiver

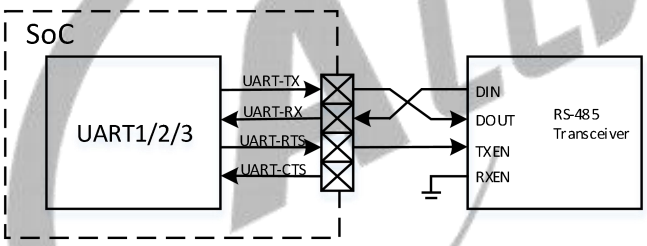
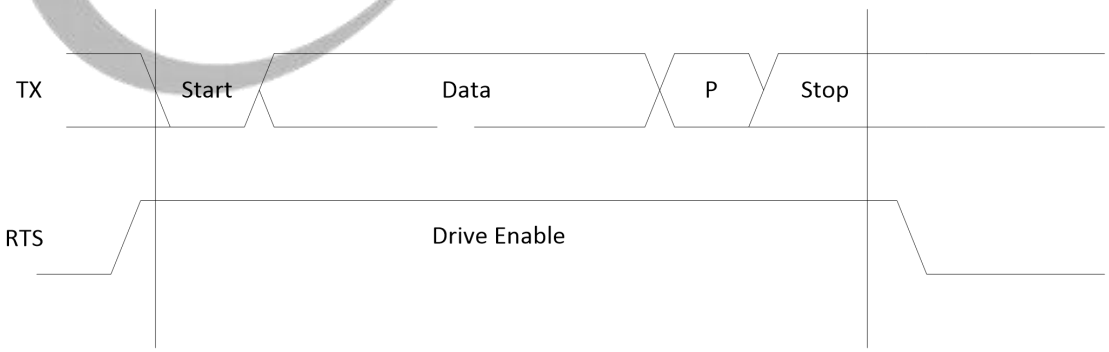


Figure 8-136 RS-485 Data Format



8.18.3.4 UART Operating Mode

Data Frame Format

The UART_LCR register can set the basic parameter of a data frame: data width (5 to 8 bits), stop bit number (1/1.5/2), parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit, and stop signal. The LSB is transmitted first.

- Start signal (start bit): It is the start flag of a data frame. According to the UART protocol, the low level of the TXD signal indicates the start of a data frame. When the UART transmits data, the level needs to hold high.
- Data signal (data bit): The data bit width can be configured as 5-bit, 6-bit, 7-bit, and 8-bit through different applications. If RS-485 mode is enabled, th data bit width is 8-bit.
- Parity bit: It is a 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the UART_LCR register. If RS-485 mode is enabled, the parity bit must be keep enabled.
- Stop Signal (stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit, 1.5-bit, and 2-bit by the UART_LCR register. The high level of the TXD signal indicates the end of a data frame.

Baud and Error Rates

The baud rate is calculated as follows: Baud rate = SCLK/(16 * divisor).

The SCLK is usually APB1 and can be set in section 2.5 Clock Controller Unit (CCU).

The divisor is frequency divider of UART. The frequency divider has 16-bit, the low 8-bit is in the UART_DLL register, the high 8-bit is in the UART_DLH register.

The relationship between the different UART mode and the error rate is as follows.

Table 8-60 UART Mode Baud and Error Rates

Clock Source	Divisor	Baud Rate	Over Sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
60000000	1	3750000	16	0

Clock Source	Divisor	Baud Rate	Over Sampling	Error(%)
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
80000000	1	5000000	16	0
160000000	1	10000000	16	0

Table 8-61 IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 8-62 RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
60000000	1	3750000	16	0
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
80000000	1	5000000	16	0
160000000	1	10000000	16	0

DLAB Definition

The DLAB control bit (UART_LCR[7]) is the access control bit of the divisor Latch register.

If DLAB is 0, then the 0x00 offset address is the UART_RBR/UART_THR (RX/TX FIFO) register, and the 0x04 offset address is the UART_IER register.

If DLAB is 1, then the 0x00 offset address is the UART_DLL register, and the 0x04 offset address is the UART_DLH register.

When the UART initials, the divisor needs to be set. That is, writing 1 to DLAB can access the UART_DLL and UART_DLH register, after finished the configuration, writing 0 to DLAB can access the UART_RBR/UART_THR register.

CHCFG_AT_BUSY Definition

The function of the CHCFG_AT_BUSY (UART_HALT [1]) and CHANGE_UPDATE (UART_HALT[2]) are as follows.

CHCFG_AT_BUSY: Enable the bit, the software can also set the UART controller when UART is busy, such as the UART_LCR, UART_DLH, UART_DLL register.

CHANGE_UPDATE: If CHCFG_AT_BUSY is enabled, and CHANGE_UPDATE is written to 1, the configuration of the UART controller can be updated. After completed the update, the bit is cleared to 0 automatically.

Setting divisor performs the following steps:

Write 1 to CHCFG_AT_BUSY to enable “configure at busy”.

Write 1 to DLAB (UART_LCR[7]) and set the UART_DLH and UART_DLL registers.

Write 1 to CHANGE_UPDATE to update the configuration. The bit is cleared to 0 automatically after completing the update.

UART Busy Flag

The UART_USR [0] is a busy flag of the UART controller.

When the TX transmits data, or the RX receives data, or the TX FIFO is not empty, or the RX FIFO is not empty, then the busy flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

8.18.4 Programming Guidelines

The following takes the UART module in the CPUX domain as an example.

8.18.4.1 Initialization

Step 1 System Initialization

- Configure APB1_CLK_REG in the CCU module to set the APB1 bus clock (The clock is 24MHz by default).

- Set UART_BGR_REG[UARTx_GATING] to 1 to enable the module clock, and set UART_BGR_REG[UARTx_RST] to 1 to de-assert the module.

Step 2 UART Controller Initialization

- IO configuration: Configure GPIO multiplex as UART function, and set UART pins to internal pull-up mode (For detail, see the description in section 8.5 GPIO).
- Baud-rate configuration:
  - Set UART baud-rate (refer to section 8.18.3.4);
  - Write UART_FCR[FIFOE] to 1 to enable TX/RX FIFO;
  - Write UART_HALT[HALT_TX] to 1 to disable TX transfer;
  - Set UART_LCR[DLAB] to 1, remain default configuration for other bits; set 0x00 offset address to the UART_DLL register, set 0x04 offset address to the UART_DLH register;
  - Write the high 8-bit of divisor to the UART_DLH register, and write the low 8-bit of divisor to the UART_DLL register;
  - Set UART_LCR[DLAB] to 0, remain default configuration for other bits; set 0x00 offset address to the UART_RBR/UART_THR register, set 0x04 offset address to the UART_IER register;
  - Set UART_HALT[HALT_TX] to 0 to enable TX transfer.

Step 3 Controller Parameter Configuration

- Set data width, stop bits, and even/odd parity type by writing the UART_LCR register.
- Reset, enable FIFO and set FIFO trigger condition by writing the UART_FCR register.
- Set the flow control parameter by writing the UART_MCR register.

Step 4 Interrupt Configuration

- Configure UART interrupt vector number to request UART interrupt (Refer to section 2.7 Generic Interrupt Controller (GIC) for interrupt vector number).
- In DMA mode, write UART_IER to 0 to disable interrupt; write UART_HSK[Handshake configuration] to 0xE5 to set DMA handshake mode; write UART_FCR[DMAM] to 1 to set DMA transmission/reception mode; set DMA parameter and request DMA interrupt according to DMA configuration process.
- In Interrupt mode, configure UART_IER to enable the corresponding interrupt according to requirements: such as transmit (TX) interrupt, receive (RX) interrupt, receive line status interrupt, RS48 interrupt, etc. (Here TX/RX interrupt is usually used).

8.18.4.2 Transferring/Receiving Data in DMA Mode

Step 1 Initialize UART model. Refer to section 8.18.4.1 Initialization for initialization steps.

Step 2 Configure UART_TFL and UART_RFL to set DRQ trigger level for DMA.

Step 3 Configure UART_HALT to set PTE and DMA_PTE_RX.

Step 4 DMA data channel, including the transfer source address, the transfer destination address, the number of data to be transferred, and the transfer type, and so on. For details, see section 2.6 DMA Controller (DMAC).

Step 5 Enable the DMA transfer or receive function of the UART by setting the register of the DMA module.

Step 6 Determine whether UART data is transferred or received completely based on the DMA status. If all data is transferred or received completely, disable the DMA transfer or receive function of the UART.

8.18.4.3 Transferring/Receiving Data in Interrupt Mode

- Data transfer

Step 1 Initialize UART model. Refer to section 8.18.4.1 for initialization steps.

Step 2 Configure UART_TFL and UART_RFL to set DRQ trigger level for DMA.

Step 3 Configure UART_HALT to set PTE and DMA_PTE_RX.

Step 4 Set UART_IER[ETBEI] to 1 to enable the UART transmission interrupt.

Step 5 Write the data to be transmitted to UART_THR.

Step 6 When the data of TX_FIFO meets trigger condition (such as FIFO/2, FIFO/4), the UART transfer interrupt is generated.

Step 7 Check UART_USR[TFE] and determine whether TX_FIFO is empty. If UART_USR[TFE] is 1, it indicates that the data in TX_FIFO is transmitted completely.

Step 8 Clear UART_IER[ETBEI] to 0 to disable transfer interrupt.

- Data receive

Step 1 Initialize UART model. Refer to section 8.18.4.1 for initialization steps.

Step 2 Configure UART_TFL and UART_RFL to set DRQ trigger level for DMA.

Step 3 Configure UART_HALT to set PTE and DMA_PTE_RX.

Step 4 Set UART_IER[ERBFI] to 1 to enable the UART reception interrupt.

Step 5 When the received data from RX_FIFO meets trigger condition (such as FIFO/2, FIFO/4), the UART receive interrupt is generated.

Step 6 Read data from UART_RBR.

Step 7 Check RX_FIFO status by reading UART_USR[RFNE] and determine whether to read data. If the bit is 1, continue to read data from UART_RBR until UART_USR[RFNE] is cleared to 0, which indicates data is received completely.

8.18.4.4 Transferring/Receiving Data in RS485 Mode

Step 1 Initialize UART model. Refer to section 8.18.4.1 for initialization steps.

Step 2 Configure UART_485_CTL [1:0] to select UART RS485 receive data format.

Step 3 If AAD receive data mode is choosed, configure UART_RS485_ADDR_MATCH register to set receive address in AAD mode.

Step 4 If DMA mode is selected, perform Step2 to Step6 in section 8.18.4.2. Otherwise, perform Step2 to Step7 in section 8.18.4.3.

8.18.5 Register List

Module Name	Base Address
UART0	0x02500000
UART1	0x02500400
UART2	0x02500800
UART3	0x02500C00
UART4	0x02501000
UART5	0x02501400
UART6	0x02501800
UART7	0x02501C00
S_UART0	0x07080000
S_UART1	0x07080400

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register

Register Name	Offset	Description
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_DMA_REQ_EN	0x008C	UART DMA Request Enable Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control Configure and Status Register
UART_RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHECK	0x00C8	BUS IDLE CHECK Register
TX_DELAY	0x00CC	TX_DELAY Register
UART_FCC	0x00F0	UART FIFO Clock Control Register

8.18.6 Register Description

8.18.6.1 0x0000 UART Receiver Buffer Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

8.18.6.2 0x0000 UART Transmit Holding Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

8.18.6.3 0x0000 UART Divisor Latch Low Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.18.6.4 0x0004 UART Divisor Latch High Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.18.6.5 0x0004 UART Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest

Offset: 0x0004			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
			priority interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

8.18.6.6 0x0008 UART Interrupt Identity Register (Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID

Offset: 0x0008			Register Name: UART_IIR
Bit	Read/Write	Default/Hex	Description
			This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt（pending by UART_485_CTL[6:5]） 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
		empty	threshold (Program THRE Mode enabled)	XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

8.18.6.7 0x0008 UART FIFO Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
			dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0	DMAM DMA Mode 0: Mode 0 In this mode, when PTE is high and TX FIFO is enable, the TX DMA request will be set when TFL is less than or equal to FIFO Trigger Level(otherwise it will be cleared). When PTE is high and TX FIFO is disabled, the TX DMA request will be set only if THR is empty. If PTE is low, the TX DMA request will be set only if the TX FIFO(TX FIFO Enabled) or THR(TX FIFO Disabled) is empty. When dma_pte_rx is high and RX FIFO is enabled, the rx drq will be set only if RFL is equal to or more than FIFO Trigger Level, otherwise it will be cleared. 1: Mode 1 In this mode, TX FIFO should be enable. If the PTE is high, the TX DMA request will be set when TFL is less than or equal to FIFO Trigger Level; If PTE is low, the TX DMA request will be set when TX FIFO is empty. Once the request is set, it is cleared only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level or there is a character timeout , the rx drq will be set; Once the rx drq is set, it is cleared only when RX FIFO(RX FIFO enabled) or RBR(RX FIFO disabled) is empty.
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO

Offset: 0x0008			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
			and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

8.18.6.8 0x000C UART Line Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0	EPS Even Parity Select

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
			It is writable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 0, indicates that this is a data byte. 10:9th bit = 1, indicates that this is an address byte. Note: When use this function, PEN(LCR[3]) must set to 1.
3	R/W	0	PEN Parity Enable It is writable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits It is writable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0	DLS Data Length Select It is writable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the

Offset: 0x000C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description
			number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

8.18.6.9 0x0010 UART Modem Control Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W	0	UART_FUNCTION Select IrDA or RS485 0:UART Mode 1:IrDA SIR Mode 2:RS485 Mode 3:Reverse
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled

Offset: 0x0010			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
			AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	/	/	/
2	/	/	/
1	R/W	0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n。 0：dtr_n de-asserted (logic 1) 1：dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

8.18.6.10 0x0014 UART Line Status Register (Default Value: 0x0000_0060)

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
			the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	RC	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.

Offset: 0x0014			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
1	RC	0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

8.18.6.11 0x0018 UART Modem Status Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0	RI Line State of Ring Indicator

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
			This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: Ff the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is

Offset: 0x0018			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
			removed if the dcd_n signal remains asserted.
2	RC	0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RC	0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

8.18.6.12 0x001C UART Scratch Register (Default Value: 0x0000_0000)

Offset: 0x001C	Register Name: UART_SCH

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

8.18.6.13 0x007C UART Status Register (Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY

Offset: 0x007C			Register Name: UART_USR
Bit	Read/Write	Default/Hex	Description
			UART Busy Bit 0: Idle or inactive 1: Busy

8.18.6.14 0x0080 UART Transmit FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

8.18.6.15 0x0084 UART Receive FIFO Level Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8:0	R	0	RFL Receive FIFO Level This indicates the number of data entries in the receive FIFO.

8.18.6.16 0x0088 UART DMA Handshake Configuration Register (Default Value: 0x0000_00A5)

Offset: 0x0088			Register Name: UART_HSK
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xA5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

8.18.6.17 0x008C UART DMA Request Enable Register (Default Value: 0x0000_0003)

Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0	DMA Timeout Enable

Offset: 0x008C			Register Name: UART_DMA_REQ_EN
Bit	Read/Write	Default/Hex	Description
			0: disable 1: enable
1	R/W	1	DMA TX REQ Enable 0: disable 1: enable
0	R/W	1	DMA RX REQ Enable 0: disable 1: enable

8.18.6.18 0x00A4 UART Halt TX Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, when DMA_PTE_RX = 1 and FIFO on, if RFL is more than or equal to trig, send DRQ, else DRQ is cleared. In other cases, once the receive data is valid, send DRQ.
6	R/W	0	PTE The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set 1, when TFL is less than or equal to trig, send the DMA request. If PTE is set 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set 1 and FIFO on, when TFL is less than or equal to trig, send DMA request. If PTE is set 1 and FIFO off, when THR is empty, send DMA request. If PTE is set 0, when FIFO(FIFO Enable) or THR(FIFO Enable) is empty, send DMA request. Otherwise, DMA request is cleared.
5	R/W	0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert

Offset: 0x00A4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
			0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0	CHANGE_UPDATE After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1). 1: Enable change when busy
0	R/W	0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled Note: If FIFOs are not enabled, the setting has no effect on operation.

8.18.6.19 0x00B0 UART DBG DLL Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: UART_DBG_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0	DEBUG DLL

8.18.6.20 0x00B4 UART DBG DLH Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: UART_DBG_DLH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0	DEBUG DLH

8.18.6.21 0x00C0 UART RS485 Control Configure and Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: UART_485_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	Add_bit_polarity Address bit polarity 0: The address bit is 1 representative the data is address 1: The address bit is 0 representative the data is address
6	R/W1C	0	AAD_ADDR_Detecte AAD Mode Receive address detecte 0:Receive address is different with set 1:Receive address is same with set
5	R/W1C	0	Address_detected RS485 Address detect 0: No address detected 1: address detected
4:2	/	/	/
1:0	R/W	0	RCM RS485 Receive mode This is used to chose the RS485 Receive mode 00: RS_9BITM 01: AAD

8.18.6.22 0x00C4 UART RS485 Address Match Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: UART_RS485_ADDR_MATCH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	AAD_Receive _ADDR AAD Mode Receive address

8.18.6.23 0x00C8 UART RS485 Bus idle Check Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: BUS_IDLE_CHECK
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	BUS_IDLE_CHK_EN 1: Enable bus idle check function 0: Disable bus idle check function

Offset: 0x00C8			Register Name: BUS_IDLE_CHECK
Bit	Read/Write	Default/Hex	Description
6	R	0	BUS_STATUS The flag of bus status 1:busy 0:idle
5:0	R	0	ADJ_TIME How long the bus is idle.The unit is 8*16*Tclk

8.18.6.24 0x00CC UART TX Delay(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: TX_DELAY
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLY The delay time between the last stop bit and the next start bit. The uint is 16*Tclk. It is use to control the space between tow bytes in TX.

8.18.6.25 0x00F0 UART FIFO Clock Control Register (Default Value: 0x0000_0003)

Offset: 0x00F0			Register Name: UART_FCC
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	FIFO Depth Indicates the depth of TX/RX FIFO
7:3	/	/	/
2	R/W	0	RXFIFO Clock Mode 0: Sync mode, R/W clocks use apb clock 1:Sync mode, write clock uses apb clock, read clock uses ahb clock
1	R/W	1	TX FIFO Clock Enable 0: clock disable 1: clock enable
0	R/W	1	RX FIFO Clock Enable 0: clock disable 1: clock enable

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9 Security System

9.1 Crypto Engine (CE)

9.1.1 Overview

The Crypto Engine (CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RBG algorithms. There are two software interfaces for secure and non-secure world each. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world and 4 different types of algorithms simultaneously. This module also has an internal DMA controller to transfer data between CE and memory. It supports parallel running for symmetric, HASH, asymmetric algorithms.

The CE has the following features:

- Symmetrical algorithm:
  - AES symmetrical algorithm
    - Key size: 28/192/256 bits
    - CFB mode includes: CFB1, CFB8, CFB64, and CFB128
    - CTR mode includes: CTR16, CTR32, CTR64, and CTR128
    - Supports ECB, CBC, CTS, OFB, CBC-MAC, and GCM modes
  - DES symmetrical algorithm
    - CTR mode, includes: CTR16, CTR32, and CTR64
    - Supports ECB, CBC, and CBC-MAC mode
  - Supports 3DES
  - SM4 symmetrical algorithm supports ECB and CBC mode
- Hash algorithms
  - Support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
  - Support HMAC-SHA1, HMAC-SHA256
  - Support multi-package[1] mode for these ones
  - Support hardware padding
- Random bit generator algorithms
  - Support PRNG, 175 bits seed width, and output with multiple of 5 words

[1] If not last package, input should aligned with computation block, namely 512bits or 1024bit

- Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words
- Support Instantiate/Reseed/Generate/Uninstantiate 4 process
- Support prediction resistance requests
- Support 8 separate suits of Internal State
- Maxim 2^32 BYTE length of Entropy input, Nonce, Personalization, Additional input. And length is multiple of word

- Public key algorithms
  - Supports RSA public key algorithms: 512/1024/2048/3072/4096-bit width
  - Supports ECC public key algorithms: 160/224/256/384/521-bit width
  - Supports SM2 algorithms
- Security Strategy and System Feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time.
  - Support task chain mode for each request. Task or task chain are executed at request order.
  - multi- scatter group(sg) are supported for both input and output data
  - Support secure and non-secure interfaces respectively, each world issues task request through its own interface, don't know each other's existence.
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other.
  - Supports byte-aligned address for all configurations

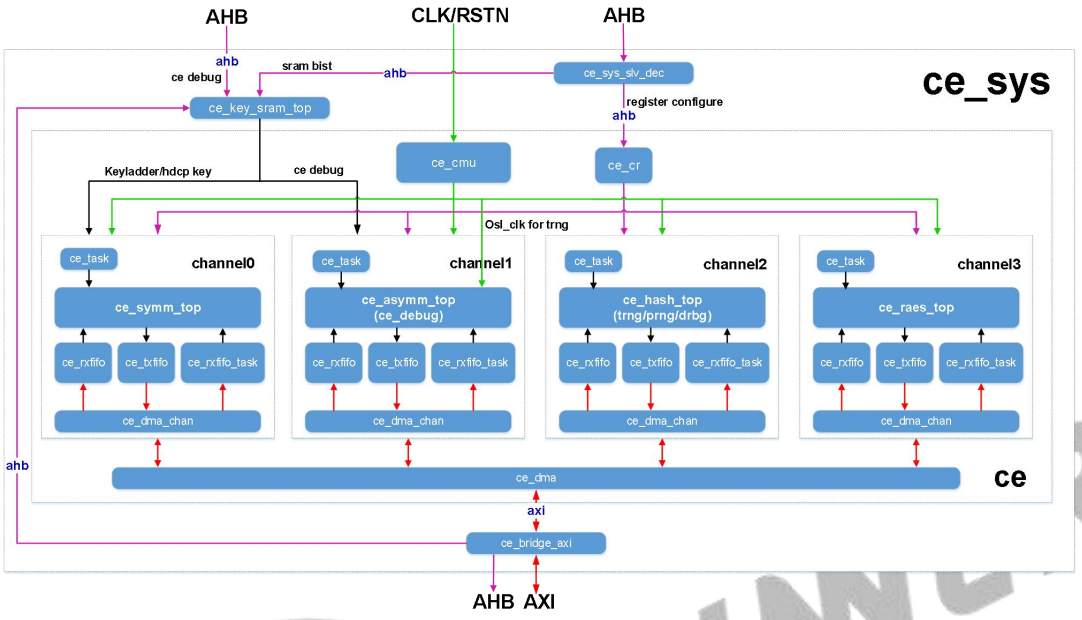
NOTE

The total length of data_length in the CBC and ECB modes of the symmetric channels needs to be aligned according to the algotithm granularity. For example, in the AES-128 algorithm, the total length of data_length needs to be an integer multiple of 128 bits

9.1.2 Block Diagram

The following figure shows a block diagram of CE.

Figure 9-1 CE Block Diagram

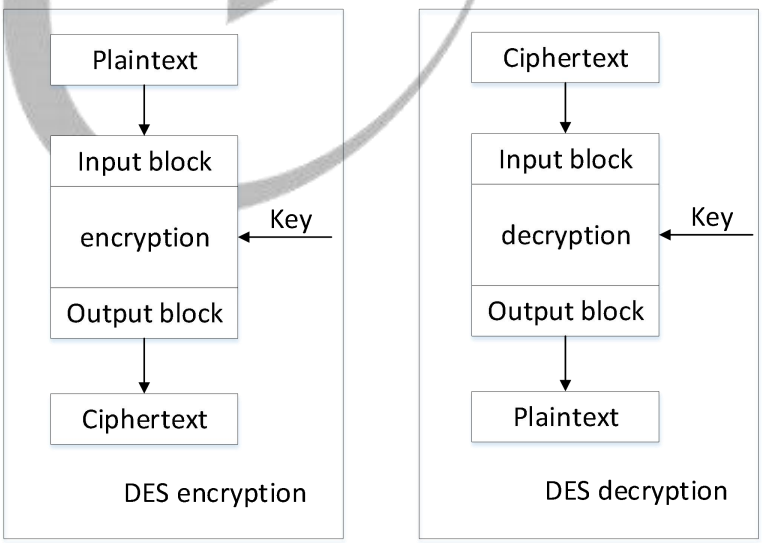


9.1.3 Functional Description

9.1.3.1 DES Algorithm

The following figure shows the DES encryption and decryption operation.

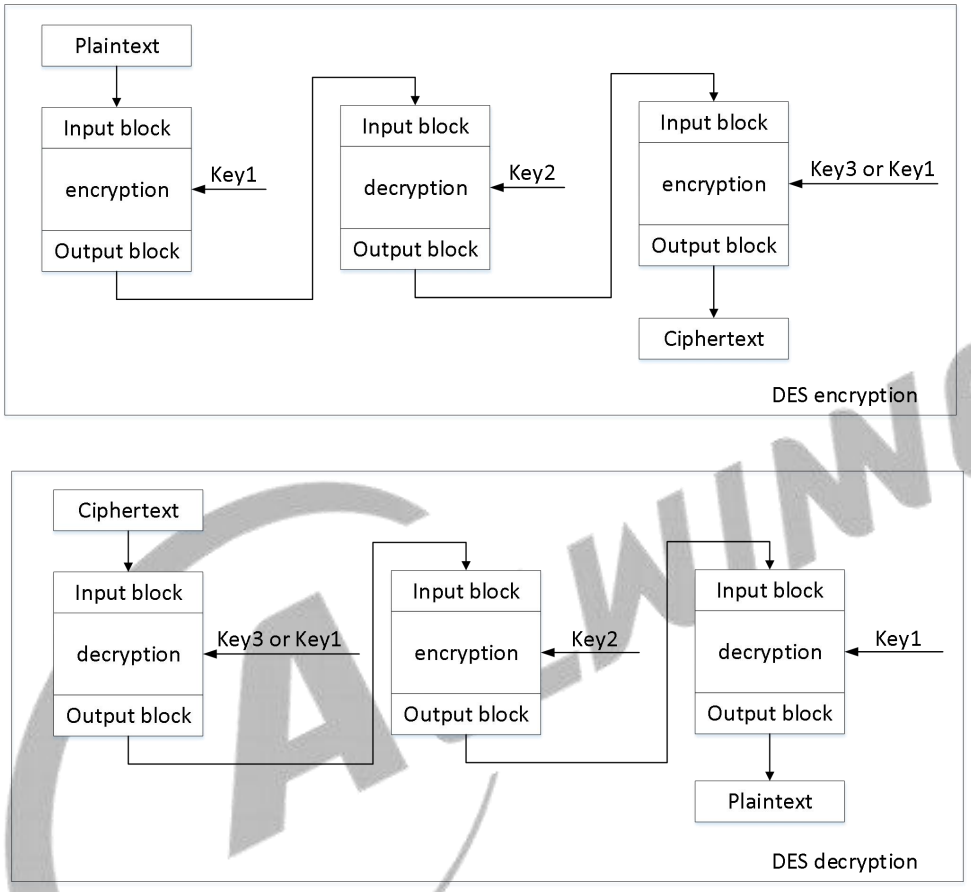
Figure 9-2 DES Encryption and Decryption



9.1.3.2 3DES Algorithm

The 3DES algorithm supports both 3-key and 2-key operations. A 2-key operation can be regarded as a simplified 3-key operation. To be specific, key 3 is represented by key 1 in a 2-key operation. The following figure shows the 3DES encryption and decryption operation of a 3-key operation and a 2-key operation.

Figure 9-3 3DES Encryption and Decryption of a 3-key Operation and a 2-key Operation

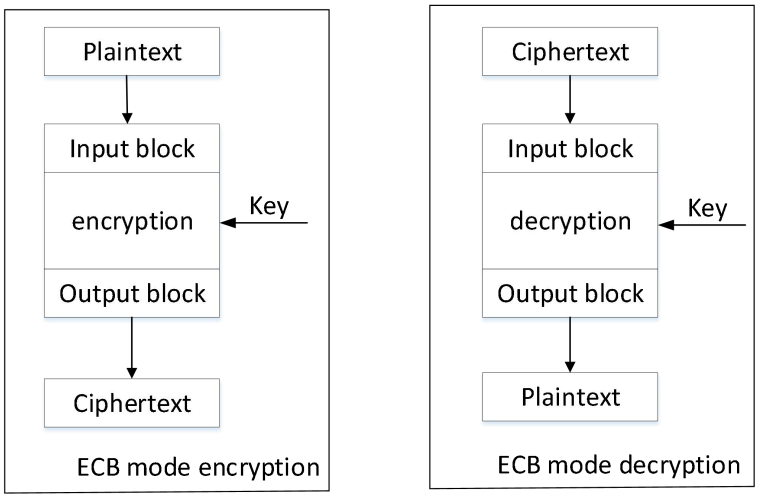


9.1.3.3 ECB Mode

The ECB mode is a confidentiality mode that features, for a given key, the assignment of a fixed ciphertext block to each plaintext block, analogous to the assignment of code words in a codebook.

In ECB mode, encryption and decryption algorithms are directly applied to the block data. The operation of each block is independent, so the plaintext encryption and ciphertext decryption can be performed concurrently.

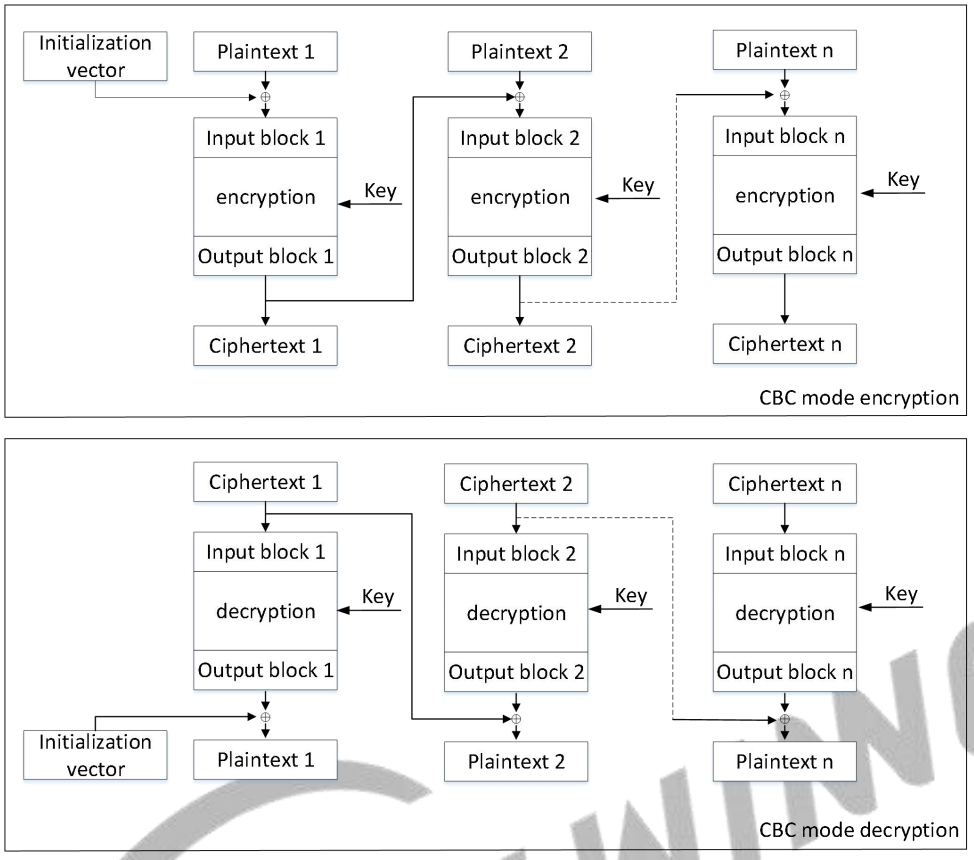
Figure 9-4 ECB Mode Encryption and Decryption



9.1.3.4 CBC Mode

The CBC mode is a confidentiality mode whose encryption process features the combining of the plaintext blocks with the previous ciphertext blocks. The CBC mode requires an initialization vector (IV) to combine with the first plaintext block. The encryption process of each plaintext block is related to the block processing result of the previous ciphertext blocks, so encryption operations cannot be concurrently performed in CBC mode. The decryption operation is independent of output plain text of the previous block, so decryption operations can be performed concurrently.

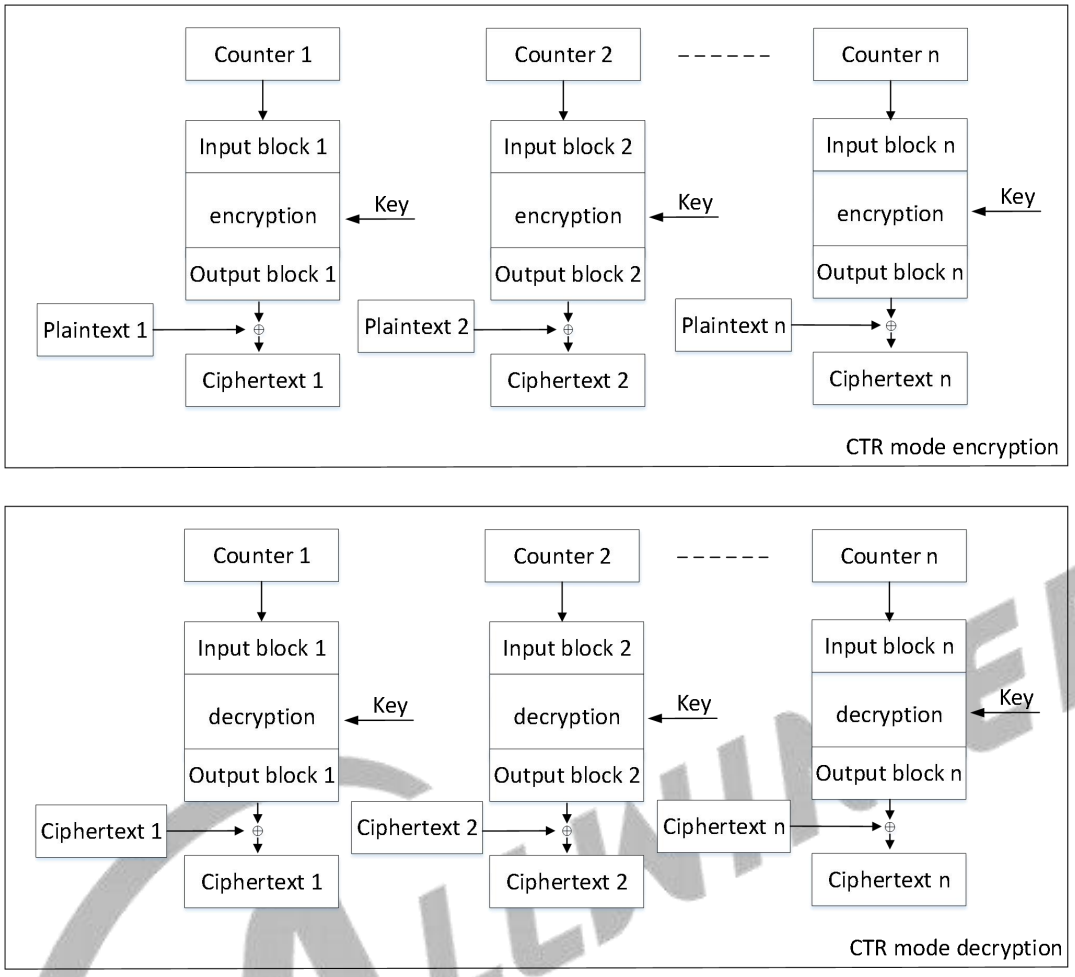
Figure 9-5 CBC Mode Encryption and Decryption



9.1.3.5 CTR Mode

The CTR mode is a confidentiality mode that features the application of the forward cipher to a set of input blocks, called counters, to produce a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. All of the counters must be distinct.

Figure 9-6 CTR Mode Encryption and Decryption

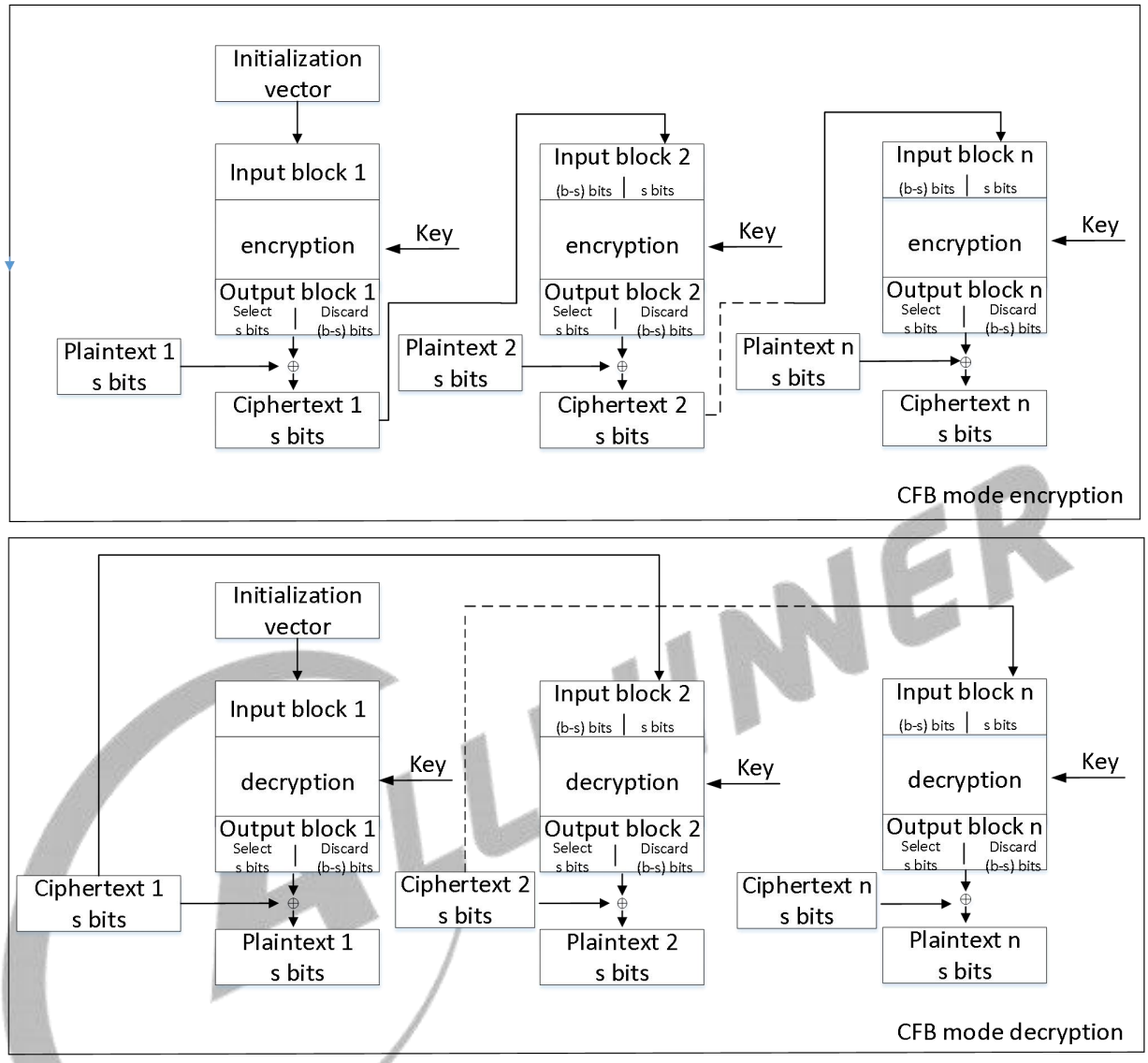


9.1.3.6 CFB Mode

The CFB mode is a confidentiality mode that features the feedback of successive ciphertext segments into the input blocks of the forward cipher to generate output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. The CFB mode requires an IV as the initial input block, and the forward cipher operation is applied to the IV to produce the first output block. The first ciphertext segment is produced by exclusive-ORing the first plaintext segment with the s most significant bits of the first output block. The value of s is 1 bit, 8 bits, 64 bits, or 128 bits.

The following figure shows the s-bit CFB mode of the AES algorithms.

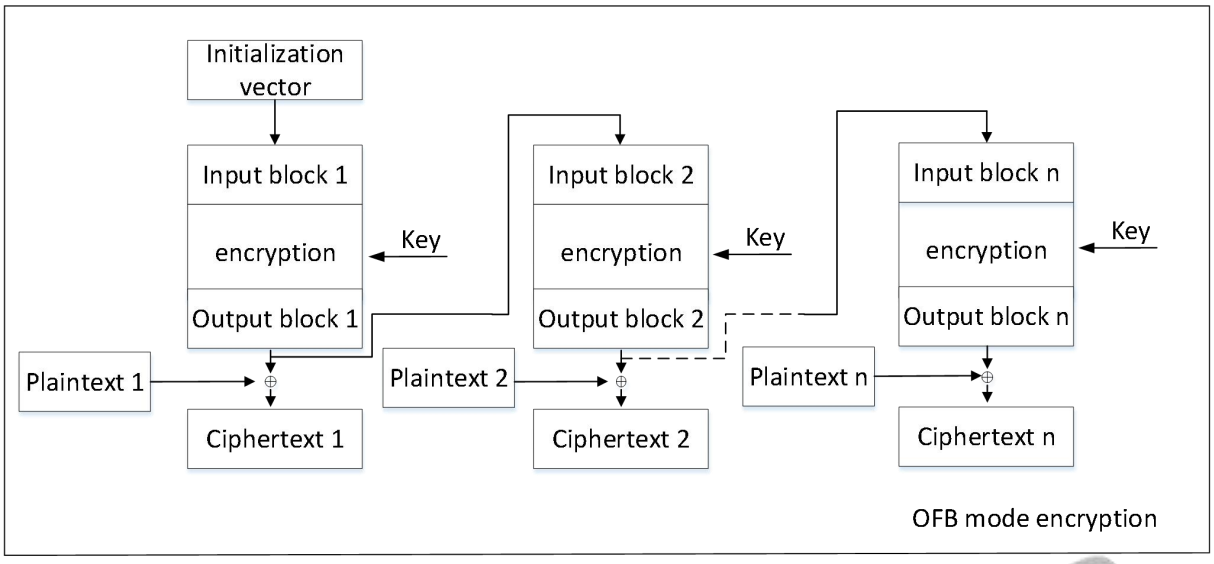
Figure 9-7 CFB Mode Encryption and Decryption

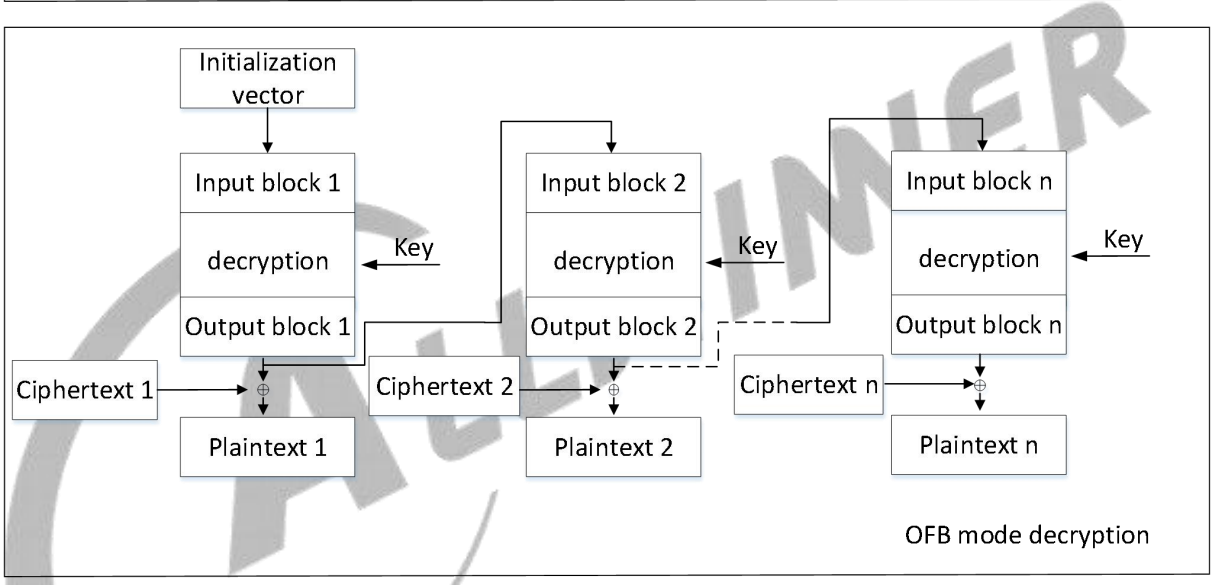


9.1.3.7 OFB Mode

The OFB mode is a confidentiality mode that features the iteration of the forward cipher on an IV to generate a sequence of output blocks that are exclusive-ORed with the plaintext to produce the ciphertext, and vice versa. If a same key is used, different IVs must be used to ensure operation security.

Figure 9-8 OFB Mode Encryption and Decryption

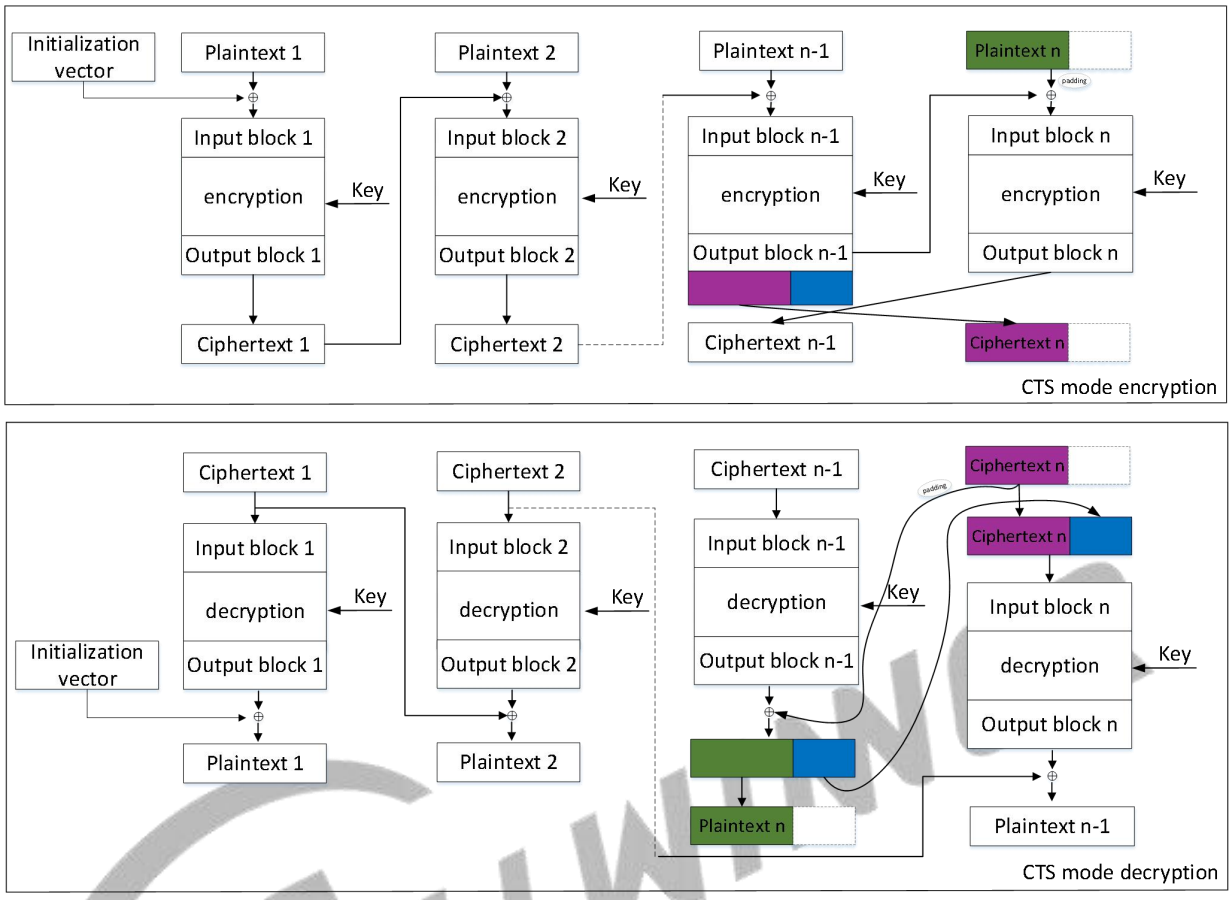




9.1.3.8 CTS Mode

The CTS mode is a confidentiality mode that accepts any plaintext input whose bit length is greater than or equal to the block size but not necessarily a multiple of the block size. Below are the diagrams for CTS encryption and decryption.

Figure 9-9 CTS Mode Encryption and Decryption



9.1.3.9 HASH Algorithm

The hash algorithms support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC-SHA1, and HMAC-SHA256. All algorithms are iterative, one-way hash functions that can process a message to produce a condensed representation called a message digest. When a message is received, the message digest can be used to verify whether the data has changed, that is, to verify its integrity.

The hash algorithm of the CE supports block-aligned total length of the input data (padded by software), that is, a multiple of 64 bytes. The message length after padding by software is used as the configured data length for the hash algorithm.

9.1.3.10 RSA Algorithm

The RSA is a public key encryption/decryption algorithm implemented through the modular exponentiation operation.

The ciphertext is obtained as follows: C = ME mod N. The plaintext is obtained as follows: M = CD mod N.

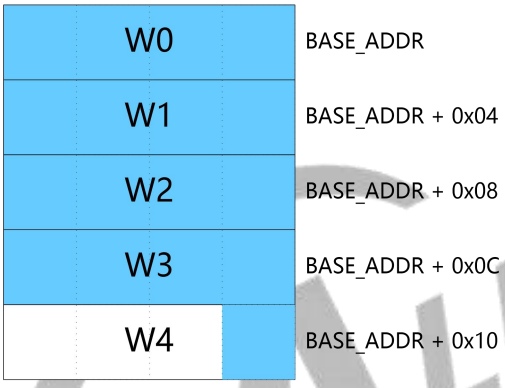
M indicates the plaintext, C indicates the ciphertext, (N, E) indicates the public key, and (N, D) indicates the private key.

9.1.3.11 Storing Message

In the application, a message may not be stored contiguously in the memory, but divided into multiple segments. Or a piece of continuously stored messages can be artificially split into multiple pieces as needs. Then each segment corresponds to a set of the source address and source length in the descriptor. Multiple segments correspond to groups 0-7 source address/source length in sequence.

Each task supports up to 8 message segments, and the data volume of each message segment supports up to 4 GWord (AES-CTS is 1 GByte). The total amount of all segments in a task (that is a package) supports up to 4 GWord (AES-CTS is 1 GByte). If a message is divided into multiple packages, all others are required to be whole words; when the last package of AES-CTS is less than one word, 0 needs to be padded, and those less than one word are counted as one word. The following figure shows the address order structure.

Figure 9-10 Word Address of Message



Byte order: low byte first, high byte last. When the data is less than one word, the low byte is filled first. The following figure shows the byte order structure (blue means it is filled by the message).

Figure 9-11 Byte Order

Bit order: high bit first, low bit last. When the data is less than one Byte, the high bit is filled first. The following figure shows the bit order structure.

Figure 9-12 Bit Order

9.1.3.12 Storing Key

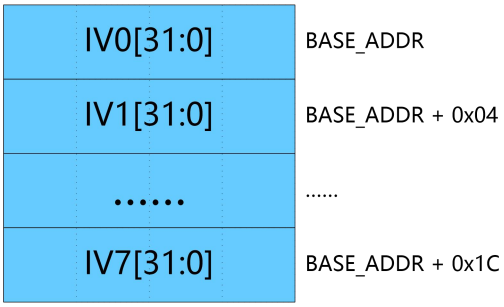
The length of KEY must be an integer multiple of word.

9.1.3.13 Storing IV

For different algorithms, the length of IV is different. But they are integer multiples of word. To keep the byte order of IV and HASH digest output consistent, the byte order of IV is different from that of the message. For the multi-packet operation, the first address of the digest output result of the previous HASH can be directly configured to the first address of the next IV, and the software does not need to do any processing on the digest.

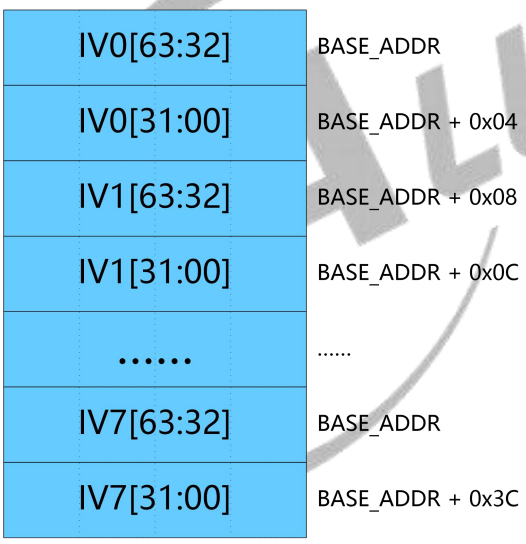
The following figure shows the storage method of 32-bit IV value.

Figure 9-13 The Storage Method of 32-bit IV



The following figure shows the storage method of 64-bit IV value.

Figure 9-14 The Storage Method of 64-bit IV



9.1.3.14 Task Descriptor of Hash Algorithms and RBG Algorithms

The task descriptor is data written by software to a contiguous space in memory. The data describes the various properties of a task, such as algorithm type, mode, subcommand, key address, data source address, the data size read from data source, abstract destination address, the written destination data size, and the information of other tasks. First, we configure the task descriptor by software; then we operates the registers of CE to start this task. After the task starts, CE will read task descriptor based on the address of the task descriptor configured in register, and perform the task one time based on the described properties.

In applications, the “NEXT TASK ADDR” field can be configured as the starting address of the next task descriptor, to concatenate multi task descriptors into a task chain. After starting the first task, CE will perform every task in order until the “NEXT TASK ADDR” field is invalid (that is 0).

The HASH/RBG algorithms and Symmetrical/Asymmetrical algorithms use the different descriptor structure, separately.

Figure 9-15 Task Chaining of Hash Algorithms and Random Bit Generator Algorithms

The detail structures are as follows.

No.	Descriptor	Name	Width	Description
0	CTRL	CHN	[1:0]	Channel ID
		IVE	[8]	IV mode enable, active high
		LPKG	[12]	1: Multi-SG enable. This bit needs to be fixed as 1.
		DLAV	[13]	Data length valid For last package, the bit needs be configured. For non last package, the bit needs not be configured. (Please configure it as 0 in PRNG/TRNG) 1: DLA means the WORD address where data total length (by bits) is saved. 0: DLA means the value of message total length (by bits).
		IE	[16]	Interrupt enable for current task, active high
1	CMD	HASH SEL	[3:0]	Hash algorithms select 0: MD5 1: SHA1 2: SHA224 3: SHA256 4: SHA384 5: SHA512 6: SM3 Other: Reserved
		HME	[4]	HMAC mode enable, active high
		RGB SEL	[11:8]	RGB algorithms select 0: No RGB use 1: PRNG 2: TRNG Other: Reserved
		SUB CMD	[31:16]	Sub-command in a specific algorithms When using PRNG, sub_cmd[15] means PRNG seed reload； sub_cmd[14:0] means PRNG linearly shifted seed
2	DLA	DLA	[31:0]	Data length OR its address. For last package, the field needs be configured. For non last package, the field needs not be configured. (Not used in PRNG/TRNG) When DLAV=1, here is the WORD address where data total length (by bits) is saved.

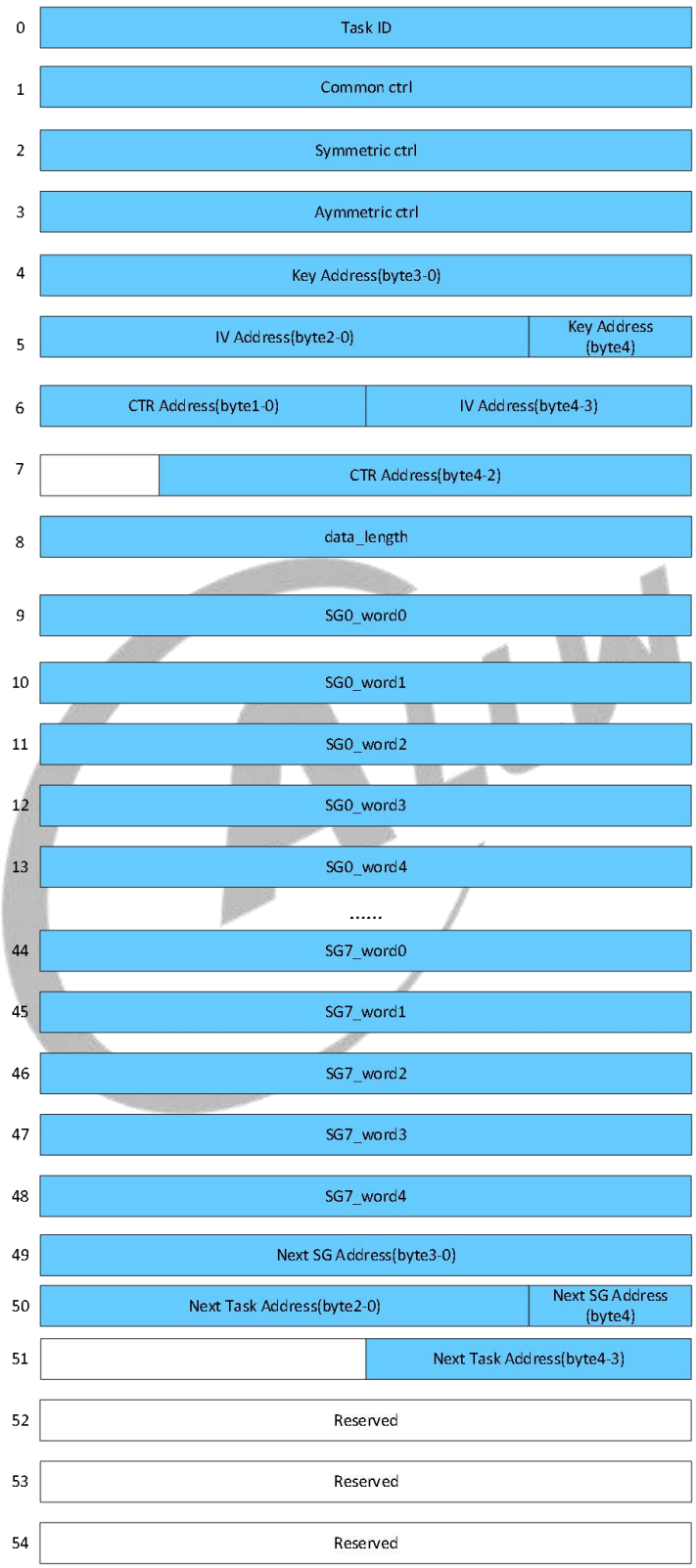
No.	Descriptor	Name	Width	Description
				When DLAV=0, here is the value of message total length (by bits)
3	DLA	DLA	[7:0]	When DLAV=1, here is the byte address bit[39:32] where data total length (by bits) is saved.
	KA	KA	[31:8]	KEY Address: The byte address bit[23:0].where HMAC KEY or PRNG KEY is saved.
4	KA	KA	[15:0]	KEY Address: The byte address bit[39:24].where HMAC KEY or PRNG KEY is saved.
	IVA	IVA	[31:16]	IV Address: The byte address bit[15:0] where IV is saved.
5	IVA	IVA	[23:0]	IV Address: The byte address bit[39:16] where IV is saved.
	Reversed	Reversed	[31:24]	/
6+5*x	SGx_W0	SGx_WORD0	[31:0]	Source Data Address x: The byte address bit[31:0] where Source Datax is saved.
7+5*x	SGx_W1	SGx_WORD1	[7:0]	Source Data Address x: The byte address bit[39:32] where Source Datax is saved.
			[31:8]	Output Data Address x: The byte address bit[23:0]where Output Datax to be saved.
8+5*x	SGx_W2	SGx_WORD2	[15:0]	Output Data Address x: The byte address bit[39:24]where Output Datax to be saved.
	Reversed	Reversed	[31:16]	/
9+5*x	SGx_W3	SGx_WORD3	[31:0]	Source Data length x: The Length (by bytes) of Source Datax.
10+5*x	SGx_W4	SGx_WORD4	[31:0]	Output Data length x: The Length (by bytes) of output Datax.
46	NSA	NSA	[31:0]	Next SG Address: The byte address bit[31:0].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 32'h0.
47	NSA	NSA	[7:0]	Next SG Address:

No.	Descriptor	Name	Width	Description
				The byte address bit[39:32].where the descriptor of the next 8 sg in a task is saved. If this is the only one group sg or the last group of a task, NSA must be 8'h0. The [38] indicate whether the next set of source sg exists.[39] bit indicate whether the next set of output（dst）sg exists.
	NTA	NTA	[31:8]	Next task Address: The byte address bit[23:0] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 24'h0.
48	NTA	NTA	[7:0]	Next task Address: The byte address bit[39:24] where the descriptor of the next task in a task-chain is saved. If this is the only task or the last task of a task-chain, NTA must be 16'h0.
	Reversed	Reversed	[31:8]	/
49	Reversed	Reversed	/	/
50	Reversed	Reversed	/	/
51	Reversed	Reversed	/	/

9.1.3.15 Other Algorithms Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination sg address and size, etc. The task descriptor is as follows.

Figure 9-16 Task Chaining of Other Algorithms



Channel id supports 0-3 for each world.

- Common ctrl

Bit	Read/Write	Default	Description
31	R/W	0	interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:25	/	/	/
24:17	R/W	0	cbc_mac_len the outcome bit length of CBC-MAC when in CBC-MAC mode. The part also be used as gcm/ocb mode tag_len.
16:9	/	/	/
8	R/W	0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0	Algorithm type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x3： SM4 others: reserved 0x20: RSA 0x21: ECC 0x22: SM2 others: reserved 0x30: RAES Others: reserved

- Symmetric ctrl

Bit	Read/Write	Default	Description
31:30	/	/	/
29:28	R/W	0	SCK_SEL 0: use sck0/maskkey0 1: use sck1/maskkey1 2: use sck2/maskkey2 3: reserved
27:24	/	/	/
23:20	R/W	0	KEY Select key select for AES/SM4/TDES（TDES only configured as

Bit	Read/Write	Default	Description
			0/8-15) 0: Select input CE_KEYx (Normal Mode) 1: Select {SSK} 2: Select {HUK} 3: Select {RSSK}, used for decrypt EK, BSSK 4-7: Reserved 8-15: Select internal Key n (n from 0 to 7)
19:18	R/W	0	cfb_width For AES-CFB width 0: CFB1 1: CFB8 2: CFB64 3: CFB128
17	/	/	/
16	R/W	0	AES CTS last package flag When set to ‘1’, it means this is the last package for AES-CTS mode(the size of the last package >128bit). The part also be used as gcm/ocb mode gcm_last/ocb_last .
15:12	/	/	/
11:8	R/W	0	AES/DES/3DES/RAES modes. DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC operation mode for symmetric 0: Electronic Code Book (ECB) mode 1: Cipher Block Chaining (CBC) mode 2: Counter (CTR) mode 3: CipherText Stealing (CTS) mode 4: Output feedback (OFB)mode 5: Cipher feedback (CFB)mode 6: CBC-MAC mode 7: OCB mode 8: GCM mode 9: Reserved Other: reserved
7:6	/	/	/
5:4	R/W	0	gcm_iv_mode[1:0] gcm_iv_mode[0]:value 1 show the last req for iv calculate gcm_iv_mode[1]: 0 :no GHASH calculate mode 1: GHASH calculate mode gcm_iv_mode[1:0]: 00: IDLE state ,this calculate do not have the process from iv to J0.

Bit	Read/Write	Default	Description
			01: by iv padding generating J0. On the mode ,iv padding is 96 bits, so iv_length will be 96bits. 10: by GHASH calculate for iv generating J0, and this is not the last req for iv calculate. 11: by GHASH calculate for iv generating J0, and this is the last req for iv calculate
3:2	R/W	0	CTR Width Counter Width for CTR Mode 0: 16-bits Counter 1: 32-bits Counter, gcm mode always use this setting without software 2: 64-bits Counter 3: 128-bits Counter
1:0	R/W	0	AES Key Size 0: 128-bits 1: 192-bits 2: 256-bits 3: Reserved

- Asymmetric ctrl

Bit	Read/Write	Default	Description
31:21	/	/	/
20:16	R/W	0	PKC algorithm mode. For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved For SM2： 00000: encryption

Bit	Read/Write	Default	Description
			00001: decryption 00010: sign 00011: sign verify 00100: key exchange
15:8	/	/	/
7:0	R/W	0	Asymmetric algorithms operation width field. It indicates how much width this request apply, as words.

key addr field is address for each algorithm's key, also for extension feature micro codes address. (By byte)

ctr addr is address for next block's IV. (By byte)

src/dst sgX addr field indicate 40bits address for source and destination data. (By byte)

src/dst sgX size field indicates size for each sg respectively(by byte)

For SG, the detail as flow:

byte3	byte2	byte1	byte0	
SRC_ADDR0 [B3]	SRC_ADDR0 [B2]	SRC_ADDR0 [B1]	SRC_ADDR0 [B0]	SG_WORD0
DST_ADDR0 [B2]	DST_ADDR0 [B1]	DST_ADDR0 [B0]	SRC_ADDR0 [B4]	SG_WORD1
		DST_ADDR0 [B4]	DST_ADDR0 [B3]	SG_WORD2
SRC_SIZE0 [B3]	SRC_SIZE0 [B2]	SRC_SIZE0 [B1]	SRC_SIZE0 [B0]	SG_WORD3
DST_SIZE0 [B3]	DST_SIZE0 [B2]	DST_SIZE0 [B1]	DST_SIZE0 [B0]	SG_WORD4

1 group SG has 8 sg, each sg has 5 words, the ADDR is 40 bits and byte-addr; the SIZE is 32bits nad byte-unit. We will support unlimited SG number,but the 1860 just use for test. This can has many group SG in a task, using the next_sg_addr to create the new SG information in the task.

Next sg field should be set to 0 when no next group sg, else set to next sg's descriptor.

next task field should be set to 0 when no next task, else set to next task's descriptor.

9.1.3.16 PKC Microcode

PKC module supports RSA, ECC, SM2 algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC/SM2 encryption, decryption, sign, verify are implemented with these microcode.

Asymmetric algorithms RSA/ECC/SM2 are implemented as microcode in PKC module. The encryption, decryption, sign, verify operations of asymmetric algorithms are composed with certain fixed microcode with hardware.

9.1.3.17 PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.

For RSA, parameters should be at the order of key, modulus, plaintext.

For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.

For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.

For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.

For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.

For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.

For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

9.1.3.18 Error Check

After CE reads the task descriptor, CE can monitor error during algorithm operation. When the error is monitored, CE will do the following operations:

The task will pause immediately

Generates interrupt

The corresponding channel of the task status register is Fail

The corresponding channel bit of error status register can be read error number

The error number has the following types.

Code	Name	Description	Algorithms Type
0x01	algorithm not support	The algorithm type is not supported.	All
0x11	KEYSRAM access error	In AES decryption task, RSSK is used as plaintext, the DST address is not in	AES decryption

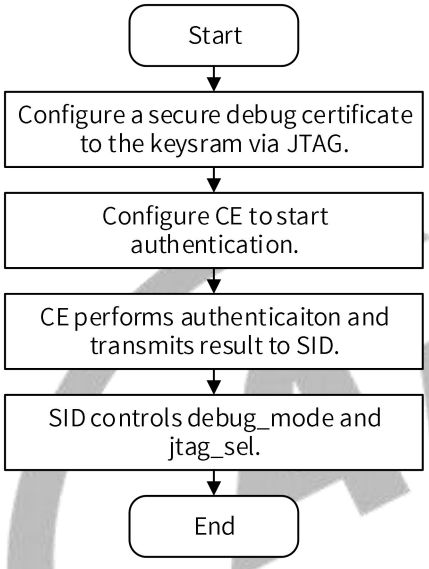
Code	Name	Description	Algorithms Type
		KEYSRAM space.	
0x21	key ladder configuration error	/	KL
0x31	data length error	Input size or output size configuration size error.	All

9.1.4 Programming Guidelines

9.1.4.1 Processing Secure Debug

The following figure shows the secure debug process.

Figure 9-17 Secure Debug Process



In secure debug process, CE mainly performs the following operatioins:

- Signature authentication
- Comparision of hash values of public key and chip_id
- Transmission of debug mode and transmission of authentification result

9.1.5 Register List

There are tree groups of registers in

Module Name	Base Address	Comments
CE_NS	0x03040000	Non-Security CE
CE_S	0x03040800	Security CE
SECURE_DEBUG_CFG	0x03042000	Secure Debug Configuration

9.1.5.1 CE_NS Register List

Module Name	Base Address	Comments
CE_NS	0x03040000	Non-Security CE

Register Name	Offset	Description
CE_TDA0_NS	0x0000	Non-Security CE Task Descriptor Address0 Register
CE_TDA1_NS	0x0004	Non-Security CE Task Descriptor Address1 Register
CE_ICR_NS	0x0008	Non-Security CE Interrupt Control Register
CE_ISR_NS	0x000C	Non-Security CE Interrupt Status Register
CE_TLR_NS	0x0010	Non-Security CE Task Load Register
CE_TSR_NS	0x0014	Non-Security CE Task Status Register
CE_ESR_NS	0x0018	Non-Security CE Error Status Register

9.1.5.2 CE_S Register List

Module Name	Base Address	Comments
CE_S	0x03040800	Security CE

Register Name	Offset	Description
CE_TDA0_S	0x0000	Security CE Task Descriptor Address0 Register
CE_TDA1_S	0x0004	Security CE Task Descriptor Address1 Register
CE_ICR_S	0x0008	Security CE Interrupt Control Register
CE_ISR_S	0x000C	Security CE Interrupt Status Register
CE_TLR_S	0x0010	Security CE Task Load Register
CE_TSR_S	0x0014	Security CE Task Status Register
CE_ESR_S	0x0018	Security CE Error Status Register
CE_SCSA0_S	0x0020	Security CE Symmetric algorithm DMA Current Source Address0 Register
CE_SCSA1_S	0x0024	Security CE Symmetric algorithm DMA Current Source Address1 Register
CE_SCDA0_S	0x0028	Security CE Symmetric algorithm DMA Current Destination Address0 Register
CE_SCDA1_S	0x002C	Security CE Symmetric algorithm DMA Current Destination Address1 Register
CE_ACSA0_S	0x0030	Security CE Asymmetric algorithm DMA Current Source Address0 Register
CE_ACSA1_S	0x0034	Security CE Asymmetric algorithm DMA Current Source Address1 Register
CE_ACDA0_S	0x0038	Security CE Asymmetric algorithm DMA Current Destination

Register Name	Offset	Description
		Address0 Register
CE_ACDA1_S	0x003C	Security CE Asymmetric algorithm DMA Current Destination Address1 Register
CE_HCSA0_S	0x0040	Security CE HASH algorithm DMA Current Source Address0 Register
CE_HCSA1_S	0x0044	Security CE HASH algorithm DMA Current Source Address1 Register
CE_HCDA0_S	0x0048	Security CE HASH algorithm DMA Current Destination Address0 Register
CE_HCDA1_S	0x004C	Security CE HASH algorithm DMA Current Destination Address1 Register
CE_XCSA0_S	0x0050	Security CE RAES algorithm DMA Current Source Address0 Register
CE_XCSA1_S	0x0054	Security CE RAES algorithm DMA Current Source Address1 Register
CE_XCDA0_S	0x0058	Security CE RAES algorithm DMA Current Destination Address0 Register
CE_XCDA1_S	0x005C	Security CE RAES algorithm DMA Current Destination Address1 Register

9.1.5.3 SECURE_DEBUG_CFG Register List

Module Name	Base Address	Comments
SECURE_DEBUG_CFG	0x03042000	Secure Debug Configuration

Register Name	Offset	Description
DEBUG_CTRL_AUTH	0x0000	Debug Authentication control Register

9.1.6 CE_NS Register Descrption

9.1.6.1 0x0000 Non-Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_NS
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_Address0 Task Descriptor Address0 is bit[31:0] (byte addr)

9.1.6.2 0x0004 Non-Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_Address1 Task Descriptor Address is bit[39:32] (byte addr)

9.1.6.3 0x0008 Non-Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_NS
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	/	/	HASH_PADDING 0: Hardware padding, perform one hash operation within a task. 1: Software padding, perform one hash operation in multiple tasks.
4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

9.1.6.4 0x000C Non-Security CE Interrupt Status Register (Default Value: 0x0000_0000)

NOTE

The tasks of 4 channels can be calculated in parallel. Therefore, 4 types of interrupts can be pulled high at the same time.

Offset: 0x000C			Register Name: CE_ISR_NS
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

9.1.6.5 0x0010 Non-Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_NS
Bit	Read/Write	Default	Description
31	R	0	TASK3_F_FULL task FIFO is not full. 0：channel 3 is ready to load task. 1：channel 3 is busy, can not load task.
30	R	0	TASK2_F_FULL task FIFO is not full. 0：channel 2 is ready to load task.

Offset: 0x0010			Register Name: CE_TLR_NS
Bit	Read/Write	Default	Description
			1：channel 2 is busy, can not load task.
29	R	0	TASK1_F_FULL task FIFO is not full. 0：channel 1 is ready to load task. 1：channel 1 is busy, can not load task.
28	R	0	TASK0_F_FULL task FIFO is not full. 0：channel 0 is ready to load task. 1：channel 0 is busy, can not load task.
27:20	/	/	/
19:16	R/W	0	Channel Task Load enable When set, channel load task . 0001：channel 0 load task enable 0010：channel 1 load task enable 0100：channel 2 load task enable 1000：channel 3 load task enable **Note: only when the corresponding bit is enabled, the task load signal can be loaded into the channel.**
15	R/W	0	TASK_LOAD_RAES When set, channel 3 can load the descriptor. 1：load ares task 0：no effect
14:11	/	/	/
10	R/W	0	TASK_LOAD_HASH When set, channel 2 can load the descriptor of task. 1：load hash task 0：no effect
9:6	/	/	/
5	R/W	0	TASK_LOAD_ASYMM When set, channel 1 can load the descriptor of task. 1：load asymm task 0：no effect
4:1	/	/	/
0	R/W	0	TASK_LOAD_SYMM When set, channel 0 can load the descriptor of task. 1：load symm task 0：no effect

9.1.6.6 0x0014 Non-Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014	Register Name: CE_TSR_NS

Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R	0x0	TASK_CHAN_RAES indicate which channel in run for RAES. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
23:19	/	/	/
18:16	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
15:11	/	/	/
10:8	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
7:3	/	/	/
2:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

9.1.6.7 0x0018 Non-Security CE Error Status Register (Default Value: 0x0000_0000)

NOTE

If data length error occurs, CE needs to be reset. Because, in this case, the computation has already started. In order to ensure that the data FIFO and algorithm state machine are cleared after the error stauts is cleared, CE needs to be reset to ensure the normal calculation of the next task.

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE

Offset: 0x0018			Register Name: CE_ESR_NS
Bit	Read/Write	Default/Hex	Description
			Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved

9.1.7 CE_S Register Descrption

9.1.7.1 0x0000 Security CE Task Descriptor Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TASK_DES_ADDR0 Task Descriptor Address is bit[31:0] (byte addr)

9.1.7.2 0x0004 Security CE Task Descriptor Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_TDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	TASK_DES_ADDR1 Task Descriptor Address is bit[39:32] (byte addr)

9.1.7.3 0x0008 Security CE Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR_S
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	HASH_PADDING 0: Hardware padding, perform one hash operation within a task. 1: Software padding, perform one hash operation in multiple tasks.
4	/	/	/
3	R/W	0x0	TASK_CHAN3_INT_EN Channel 3 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
2	R/W	0x0	TASK_CHAN2_INT_EN Channel 2 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
1	R/W	0x0	TASK_CHAN1_INT_EN Channel 1 Task Interrupt Enable 0: interrupt disable 1: interrupt enable
0	R/W	0x0	TASK_CHAN0_INT_EN Channel 0 Task Interrupt Enable 0: interrupt disable 1: interrupt enable

9.1.7.4 0x000C Security CE Interrupt Status Register (Default Value: 0x0000_0000)

NOTE

The tasks of 4 channels can be calculated in parallel. Therefore, 4 types of interrupts can be pulled high at the same time.

Offset: 0x000C			Register Name: CE_ISR_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R/W1C	0x0	TASK_CHAN3_STA Channel 3 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
5:4	R/W1C	0x0	TASK_CHAN2_STA Channel 2 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
3:2	R/W1C	0x0	TASK_CHAN1_STA Channel 1 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.
1:0	R/W1C	0x0	TASK_CHAN0_STA Channel 0 task Status : Read 0x1: task completed successfully Read 0x2: task fail and stop Write 0x3 to clear it.

9.1.7.5 0x0010 Security CE Task Load Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR_S
Bit	Read/Write	Default	Description
31	R	0	CHANNEL3_F_FULL task FIFO is not full. 0：channel 3 is ready to load task. 1：channel 3 is busy，can not load task.
30	R	0	CHANNEL2_F_FULL task FIFO is not full. 0：channel 2 is ready to load task.

Offset: 0x0010			Register Name: CE_TLR_S
Bit	Read/Write	Default	Description
			1：channel 2 is busy，can not load task.
29	R	0	CHANNEL1_F_FULL task FIFO is not full. 0：channel 1 is ready to load task. 1：channel 1 is busy，can not load task.
28	R	0	CHANNEL0_F_FULL task FIFO is not full. 0：channel 0 is ready to load task. 1：channel 0 is busy，can not load task.
27:20	/	/	/
19:16	R/W	0	Channel Task Load enable When set, channel load task . 0001：channel 0 load task enable 0010：channel 1 load task enable 0100：channel 2 load task enable 1000：channel 3 load task enable **Note: only when the corresponding bit is enabled, the task load signal can be loaded into the channel.**
15	R/W	0	TASK_LOAD_RAES When set, ares can load the descriptor. 1：load ares task 0：no effect
14:11	/	/	/
10	R/W	0	TASK_LOAD_HASH When set, hash can load the descriptor of task. 1：load hash task 0：no effect
9:6	/	/	/
5	R/W	0	TASK_LOAD_ASYMM When set, asymm can load the descriptor of task. 1：load asymm task 0：no effect
4:1	/	/	/
0	R/W	0	TASK_LOAD_SYMM When set, symm can load the descriptor of task. 1：load symm task 0：no effect

9.1.7.6 0x0014 Security CE Task Status Register (Default Value: 0x0000_0000)

Offset: 0x0014	Register Name: CE_TSR_S

Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:24	R	0x0	TASK_CHAN_RAES indicate which channel in run for RAES. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
23:19	/	/	/
18:16	R	0x0	TASK_CHAN_DIG indicate which channel in run for digest. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
15:11	/	/	/
10:8	R	0x0	TASK_CHAN_ASYMM indicate which channel in run for asymmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3
7:3	/	/	/
2:0	R	0x0	TASK_CHAN_SYMM indicate which channel in run for symmetric. 0: task channel0 1: task channel1 2: task channel2 3: task channel3

9.1.7.7 0x0018 Security CE Error Status Register (Default Value: 0x0000_0000)

NOTE

If data length error occurs, CE needs to be reset. Because, in this case, the computation has already started. In order to ensure that the data FIFO and algorithm state machine are cleared after the error stauts is cleared, CE needs to be reset to ensure the normal calculation of the next task.

Offset: 0x0018	Register Name: CE_ESR_S

Bit	Read/Write	Default/Hex	Description
31:24	R	0x0	CHAN3_ERR_STATE Error code for task channel 3 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
23:16	R	0x0	CHAN2_ERR_STATE Error code for task channel 2 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
15:8	R	0x0	CHAN1_ERR_STATE Error code for task channel 1 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved
7:0	R	0x0	CHAN0_ERR_STATE Error code for task channel 0 0x00: No error 0x01: algorithm not support 0x11: KEYSRAM access error 0x21: key ladder configuration error 0x31: data length error other: reserved

9.1.7.8 0x0020 Security CE Symmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CE_SCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_SRC_ADDR0 Symmetric algorithm current source address DMA reads. Bit[31:0], byte addr.

9.1.7.9 0x0024 Security CE Symmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_SRC_ADDR1 Symmetric algorithm current source address DMA reads. Bit[39:32], byte addr.

9.1.7.10 0x0028 Security CE Symmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	SYMM_CUR_DST_ADDR0 Symmetric algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.11 0x002C Security CE Symmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_SCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	SYMM_CUR_DST_ADDR1 Symmetric algorithm current destination address DMA writes. Bit[39:32], byte addr.

9.1.7.12 0x0030 Security CE Asymmetric algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CE_ACSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_SRC_ADDR0 Asymmetric algorithm current source address DMA reads. Bit[31:0], byte addr.

9.1.7.13 0x0034 Security CE Asymmetric algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_ACSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_SRC_ADDR1 Asymmetric algorithm current source address DMA reads. Bit[39:32], byte addr.

9.1.7.14 0x0038 Security CE Asymmetric algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_ACDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ASYMM_CUR_DST_ADDR0 Asymmetric algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.15 0x003C Security CE Asymmetric algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: CE_ACDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	ASYMM_CUR_DST_ADDR1 Asymmetric algorithm current destination address DMA writes. Bit[39:32], byte addr.

9.1.7.16 0x0040 Security CE HASH algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CE_HCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_SRC_ADDR0 HASH algorithm current source address DMA reads. Bit[31:0], byte addr.

9.1.7.17 0x0044 Security CE HASH algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_HCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_SRC_ADDR1 HASH algorithm current source address DMA reads. Bit[39:32], byte addr.

9.1.7.18 0x0048 Security CE HASH algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_HCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH_CUR_DST_ADDR0 HASH algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.19 0x004C Security CE HASH algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CE_HCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	HASH_CUR_DST_ADDR1 HASH algorithm current destination address DMA writes. Bit[39:32], byte addr.

9.1.7.20 0x0050 Security CE RAES algorithm DMA Current Source Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CE_XCSA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RAES_CUR_CUR_ADDR0 RAES algorithm current source address DMA reads.

9.1.7.21 0x0054 Security CE RAES algorithm DMA Current Source Address1 Register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RAES_CUR_CUR_ADDR1 RAES algorithm current source address DMA reads.

9.1.7.22 0x0058 Security CE RAES algorithm DMA Current Destination Address0 Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA0_S
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RAES_CUR_DST_ADDR0 RAES algorithm current destination address DMA writes. Bit[31:0], byte addr.

9.1.7.23 0x005C Security CE RAES algorithm DMA Current Destination Address1 Register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: CE_XCDA1_S
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RAES_CUR_DST_ADDR1 RAES algorithm current destination address DMA writes. Bit[39:32], byte addr.

Appendix: Glossary

The following table contains acronyms and abbreviations used in this document.

Term	Meaning
A	
ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Synchronization
AWB	Automatic White Balance
B	
BROM	Boot ROM
C	
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
D	
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
E	
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
F	
FEL	Fireware Exchange Launch

Term	Meaning
FIFO	First In First Out
G	
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
I	
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor
J	
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
L	
LCD	Liquid-Crystal Display
LRADC	Low Rate Analog to Digital Converter
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
M	
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N	
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
O	
OHCI	Open Host Controller Interface
OTP	One Time Programmable
OWA	One Wire Audio
P	
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
PPU	Power Policy Unit
POR	Power-On Reset
PRCM	Power Reset Clock Management

Term	Meaning
PWM	Pulse Width Modulation
R	
R	Read only/non-Write
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
S	
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
T	
TDES	Triple Data Encryption Standard
TWI	Two Wire Interface
U	
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB DRD	Universal Serial Bus Dual Role Device
UTMI	USB2.0 Transceiver Macrocell Interface

Allwinner Technology Co., Ltd.

No.9 Technology Road 2, High-Tech Zone,

Zhuhai, Guangdong Province, China

Contact US:

Service@allwinnertech.com

www.allwinnertech.com