XR806 Datasheet

Wi-Fi + BLE5.0 Combo MCU

for Internet of Things Applications

Revision 1.1

October 27, 2020

Revision History

Revision	Date	Author	Description
1.0	October 12, 2020	AWA1091	Initial version
1.1	October 27, 2020	AWA1091	1. Modify chapter 4.5, add chapter 4.5.2； 2. Modify Figure 3-1、 Figure 3-6 and Table 5-1; 3. Modify some details description;

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1 About This Document

1.1 Purpose and Scope

This document is XR806's technical specification. It provides the system features, power management, module functions, package specification and other information about XR806.

1.2 Intended Audience

The intended audience about this document are technical engineers, application engineers and FAE, etc.

1.3 Conventions and Terminology

1.3.1 Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	Indicates potential risk of injury or death exists if the instructions are not obeyed.
CAUTION	Indicates potential risk of equipment damage, data loss, performance degradation, or unexpected results exists if the instructions are not obeyed.
NOTE	Provides additional information to emphasize or supplement important points of the main text.
TIP	Indicates a tip that may help you solve a problem or save time.

1.3.2 Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

1.3.3 Reset Value Conventions

In the register definition tables:

If other column value in a bit or multiple bits row is “/”, that this bit or these multiple bits are unused.

If the default value of a bit or multiple bits is “UDF”, that the default value is undefined.

1.3.4 Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear. Writing 1 has no effect
R/W1C	Read/Write 1 to Clear. Writing 0 has no effect
R/W1S	Read/Write 1 to Set. Writing 0 has no effect
W	Write Only

1.3.5 Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1 K	1024
	1 M	1,048,576
	1 G	1,073,741,824
Frequency, data rate	1 k	1000
	1 M	1,000,000
	1 G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200, 0x79	Address or data in hexadecimal
0b	0b010, 0b00 000 111	Data or sequence in binary (register description is excluded.)
X	00X, XX1	In data expression, X indicates 0 or 1. For example, 00X indicates 000 or 001 and XX1 indicates 001, 011, 101 or 111.

2 Overview

2.1 General Description

XR806 is a highly integrated low-power Wi-Fi and Bluetooth Low Energy(BLE) Micro-controller System-on-Chip (SoC) solution designed for Internet of Things (IoT), Machine-to-Machine (M2M), Smart Home, Cloud Connectivity and Smart Energy applications.

The XR806 application subsystem is powered by an ARMv8-M architecture MCU with Trustzone-M (named AR800A) that operates up to 160MHz. It supports an integrated 320KB SRAM and 160KB ROM, a SQPI interface to SIP up to 16MB Flash. Integrated CACHE enables Execute In Place (XIP) from flash and PSRAM. It also includes many peripherals, including UART, TWI, SPI, PWM, IrDA (T/R), and GPADC.

The Wi-Fi subsystem contains the 802.11b/g/n baseband, MAC and radio with integrated PA, LNA, Switch and harmonic filter, which is design to meet both the low power, high integration and high performance network application. A novel digital RF transmitter is design using XRADIOTECH's MPD™ technology to deliver higher output power and maintain higher efficiency, and also to keep the chip not sensitive to antenna mismatch but always have good EVM at different VSWR.

The Bluetooth subsystem contains full feature bluetooth5.0 standard, including RF, modem, baseband and profiles. Which is optimized for long range and low power application, especially smart home mesh connections. High performance and larger SRAM allow for simple mesh gateway design with integrated Wi-Fi system to connected to internet directly.

The SoC is designed for networked low-power embedded applications. It has an integrated network processor with a large set of TCP/IP with IPv4/IPv6 based services. These services can be accessed via a serial UART/SPI link connected to an external host CPU.

2.2 Features

2.2.1 General System Features

Table 2- 1 XR806 Features

Chip List	Description	XR806AF2L	XR806BF2L	XR806BM2I
Package	Trays and tape-in-reel	4x4mm^2	5x5mm^2	5x5mm^2
		QFN32	QFN40	QFN40
Supply voltage	Power supply from system	1.8~5.5V		
	5V IO	Yes		
PMU	LDO for external device (EXT LDO)	Yes		
Clock	External HOSC	24/26/32/40MHz		
	External LOSC	32.768KHz		
	Internal RCOSC	30~60KHz		
	Internal RCOSC Calibration	YES		
MCU Core	Core Type	Cortex M33 Star (Armv8-M Architecture)		
	Core clock maximum frequency	160MHz	160MHz	up to 240MHz
Memory	Internal ROM	160KB		
	Internal RAM	up to 320KB		
	Internal Flash with XIP	2MB	2MB	-
	External Flash with XIP	Max. 16MB		
	Internal PSRAM	-	-	2MB
Backup register	Backup register for power save	16B		
Secure boot	-	Yes		
Trustzone-M	Default size: 28KB	Yes		
Crypto Engine	AES, DES, 3DES, SHA-1, MD5, TRNG, CRC32/16, SHA256	Yes		
TRNG	Provide random number seed	Yes		
WDG reset protection	Protect specified peripherals been reset by watchdog reset	Yes		
BOR	BOR Detection	Yes		
Wi-Fi	802.11 b/g/n	Yes		
Bluetooth	BLE 5.0	Yes		
	BLE Configure	Yes		

Chip List	Description		XR806AF2L	XR806BF2L	XR806BM2I
	BLE Mesh		Yes	Yes	Yes
Peripheral	1.8/3.3/5V GPIO	General Purpose	4	4	4
	1.8/3.3 GPIO	General Purpose	14	22	22
	WAKEUP IO	From RTC wake-up	8	10	10
	UART	Max.3Mbps	3	3	3
	SPI	Master and slave	1	1	1
	I2C	Max.400Kbps	2	2	2
	IR	TX and RX	1	1	1
	DAudio	IIS/PCM	1	1	1
	Audio PWM	Playback Channel	1	1	1
	PWM	Output Channel	8	8	8
	KEYSCAN	8*16	-	YES	YES
	Smart Card	ISO7816	1	1	1
	GPADC	VBAT channel	1	1	1
		Normal channel	3	7	7
	NDMA	8 Channel	YES	YES	YES
	SDMA	2 Channel	YES	YES	YES
	Timer	RTC timer	1	1	1
		Watchdog timer	1	1	1
		Normal timer	2	2	2
		Wakeup timer	1	1	1

2.2.2 Wi-Fi Subsystem Features

- IEEE 802.11b/g/n, 1x1 SISO 2.4GHz
- Integrated MAC, BB, RF and Embedded TCP/IP Stack
- Integrated T/R switch, harmonic filter, PA and LNA
- Antenna diversity
- Station, AP Modes
- Smart-Configure Technology for Autonomous and Fast Wi-Fi Connections
- Security Supports for WEP, WPA/WPA2/WPA3 personal, WPS2.0
- Industry-Standard BSD Socket Application Programming Interfaces (APIs)

2.2.3 Bluetooth5.0 Subsystem Features

- Bluetooth5.0 Radio, Protocol stack and application profiles
- Backwards-compatible to v4.0/4.1/4.2 devices
- Supports Central and Peripherals Roles
- Supports secure connections
- Supports data packet length extension
- Supports LE 2M PHY with Bluetooth 5 Compatibility

2.2.4 Power Management

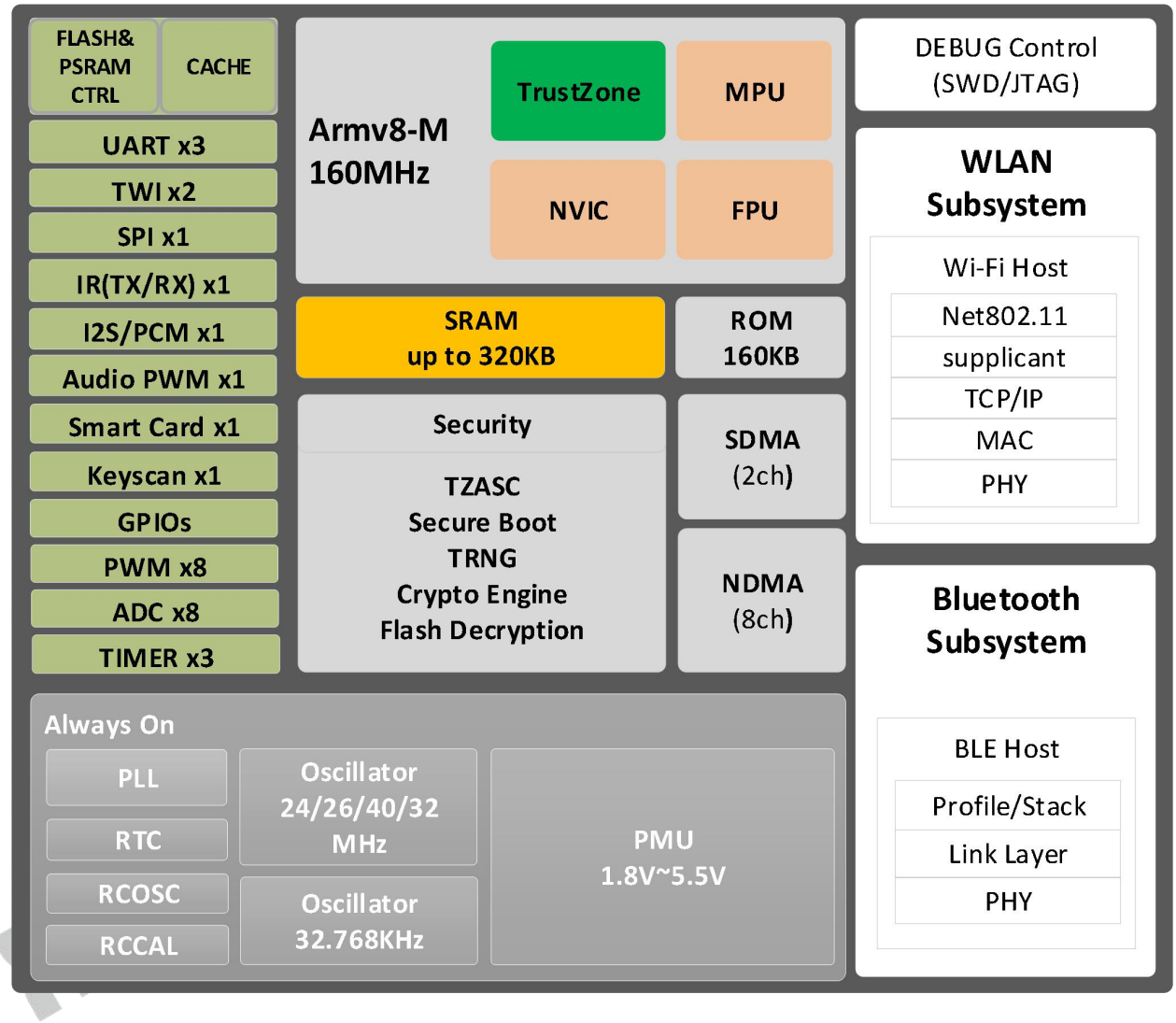
- Integrate highly flexibility power management unit by several LDOs and internal DC-DC controller
- Wide range power supply: 1.8~5.5V
- Industry leading Low-Power Wi-Fi mode (at DC-DC mode)
- Integrates 1Kbit eFuse to store device specific information and RF calibration data

2.3 Applications

- Security Systems
- Smart Energy
- Internet Gateway
- Smart Home
- Access Control
- Cloud Connectivity
- Industrial Control
- IP Network Sensor Nodes

2.4 Block Diagram

Figure 2- 1 XR806 Functional Block Diagram



3 Function Description

3.1 System Overview

3.1.1 Power Management

A single 1.8~5.5V power supply is required for the XR806. It could be from an AC-DC converter, USB to supply to 5V or a DC-DC converter to convert higher voltage supply to 3.3V or even lower. It could be from a battery directly too, no matter it is lithium, single 3V button or 2 serial NI-MH battery.

The Power Management Unit (PMU) contains a DC-DC, several Low Drop-out Regulators (LDOs), and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, load regulation, high ripple rejection, and low output noise. The PMU integrates several LDOs for different circuits: EXT LDO, DIG LDO, RTC LDO, DC-DC, TOP LDO, as shown in Figure 3-1. They have different operating conditions and features:

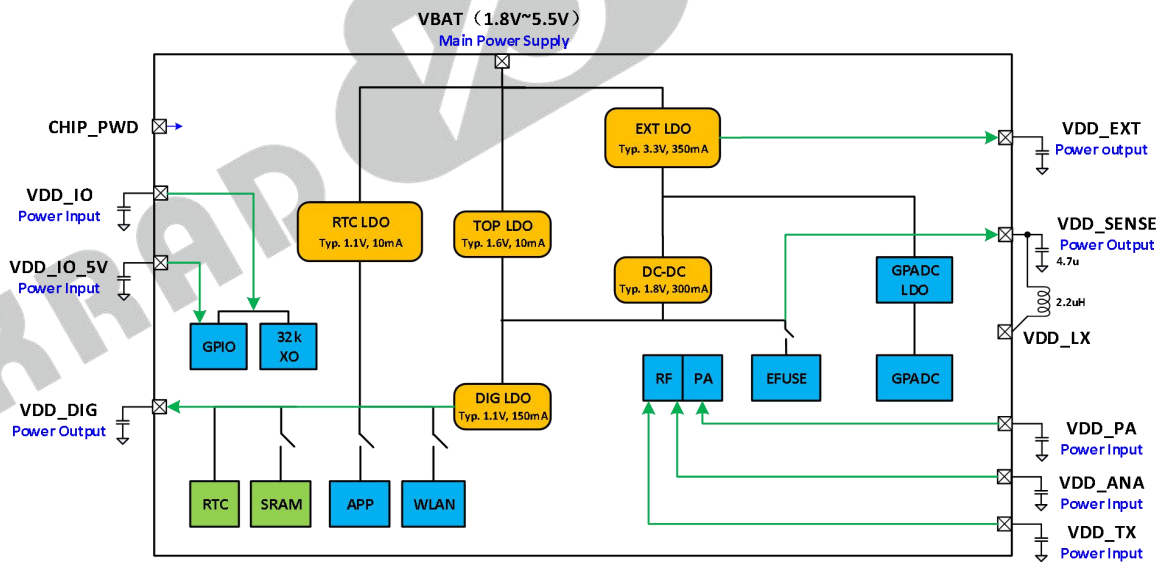
- **EXT LDO** is a main power supply for external device in application, and also can be provide to VDDIO, GPADC. It has maximum 150mA load current. The output voltage is limited to 3.3/3.1/2.8/2.5V (by register configure setting), when VBAT is lower than the value, it will automatically switch to bypass mode to let output voltage follow VBAT.
- **DIG LDO** is the main supply for whole chip digital circuit with programmable voltage from 0.6V to 1.35V to let DVFS operate effectively.
- **RTC LDO** is the main supply only for RTC domain to optimize power consumption at HIBERNATION state.
- **DC-DC** provide programmable voltage from 1.0V to 2.5V with maximum 300mA load current, for DIG LDO、EFUSE program、VDD_ANA(RFIP).
- **TOP LDO** provide programmable voltage from 0.9V to 2.4V with maximum 10mA load current, for STANDBY and HIBERNATION state, also DIG LDO input at STANDBY state. Normally, make sure VBAT voltage is higher than this programmable output voltage setting.

There are four power domains in the system: RTC domain, OA domain, Digital Core domain and Wi-Fi domain. They mainly used for different scenario to maintain ultra-low power application. We define XR806 into **ACTIVE, STANDBY, HIBERNATION** and **SHUTDOWN** power management states, as shown in Table 3-1.

Table 3- 1 Power Management States

POWER MODE	APP CPU	Wi-Fi	EXT LDO	RTC LDO	TOP LDO	DIG LDO	DCXO /DPLL	Description
ACTIVE	ACTIVE	ACTIVE	ON	ON	ON	ON	ON	All CPU active
	ACTIVE	OFF	ON	ON	ON	ON	ON/OFF	APP CPU active
STANDBY	SLEEP	ACTIVE	ON	ON	ON	ON	ON	APP CPU goes to sleep, Wi-Fi DTIMx state
	SLEEP	SLEEP	ON	ON	LP	LP	OFF	
	SLEEP	OFF	ON	ON	LP	LP	OFF	APP CPU goes to sleep, Wi-Fi power off
HIBERNATE	OFF	OFF	ON/OFF	ON	OFF /LP	OFF	OFF	Only RTC on, waiting for timer or wake-up IO to interrupt
SHUTDOWN	OFF	OFF	OFF	OFF	OFF	OFF	OFF	CHIP_PWD pin keep low level

Figure 3- 1 XR806 Power Architecture



NOTE

The green arrow indicates the power supply from the chip to the pin or from the pin to the chip;

3.1.2 Power State and Power Sequence

Figure 3- 2 Power-on Sequence

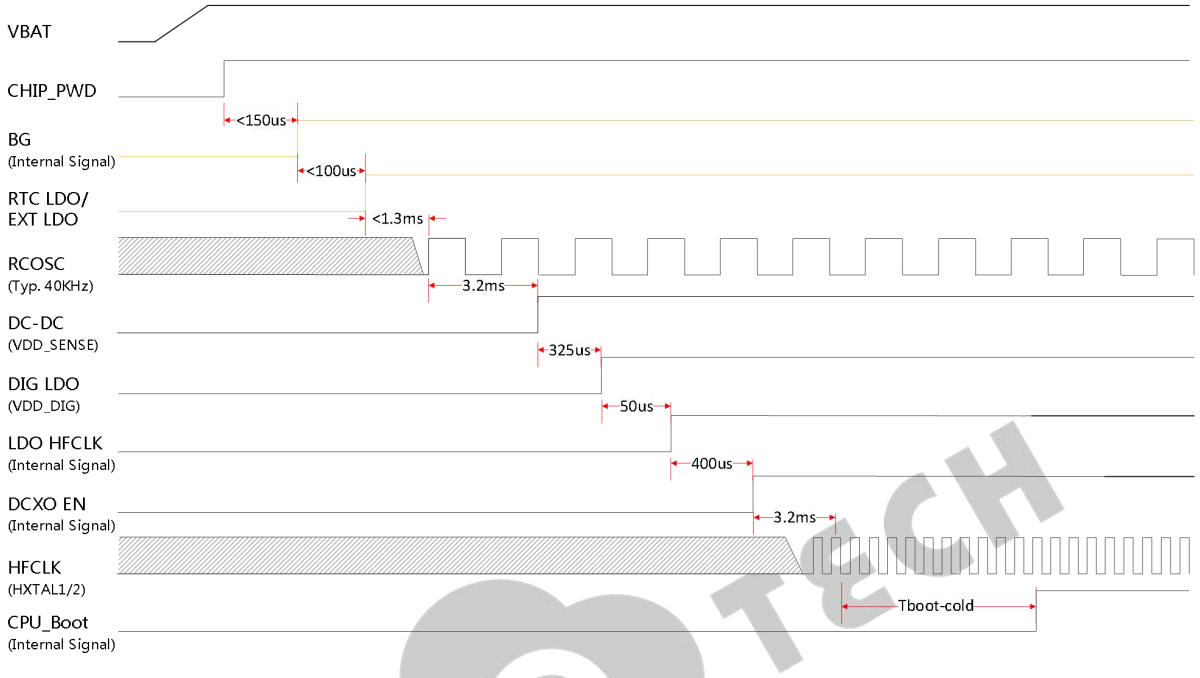


Figure 3- 3 Wakeup from Standby

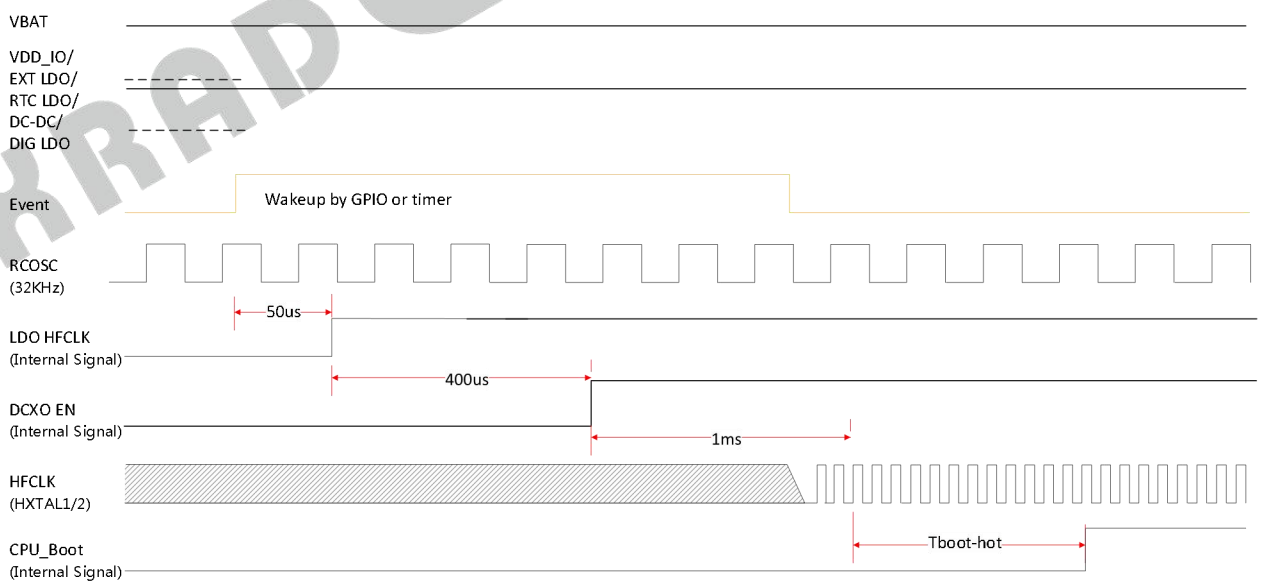


Figure 3- 4 Wakeup from Hibernation

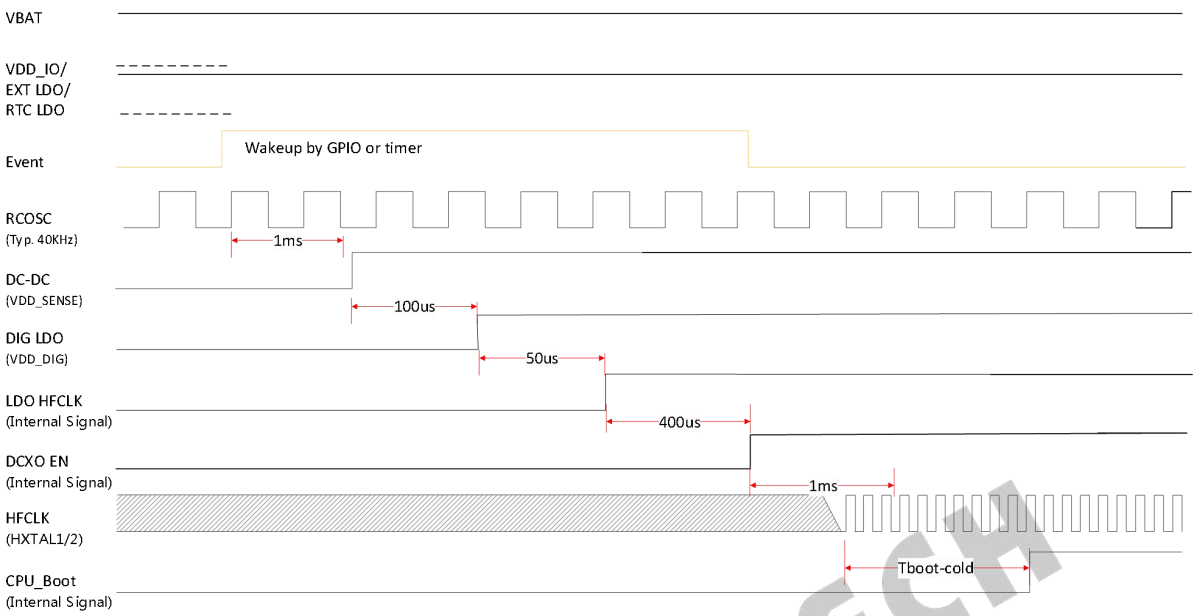
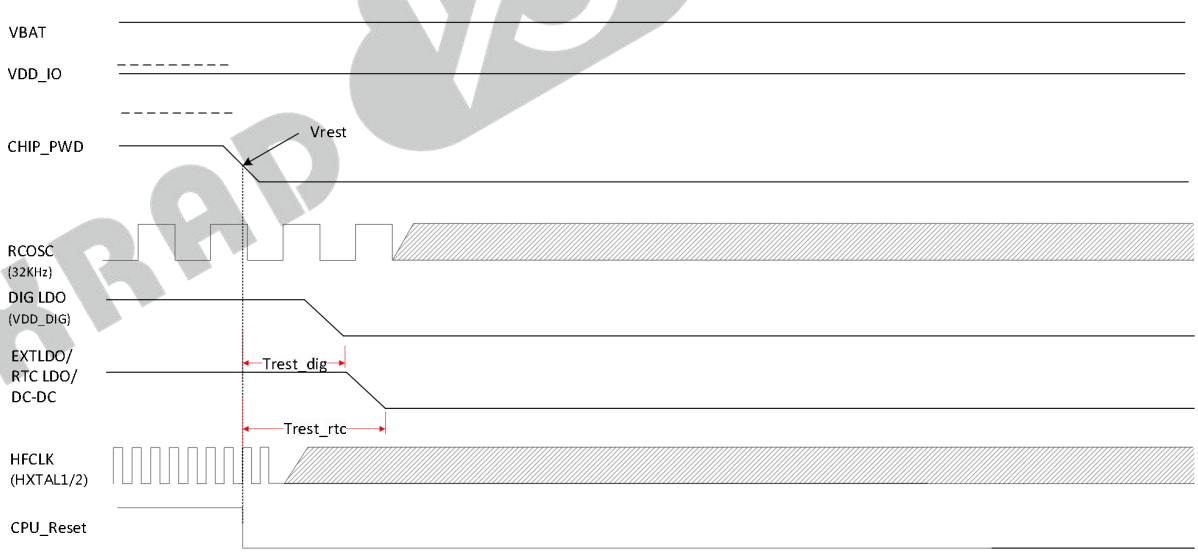


Figure 3- 5 Shutdown Sequence



3.1.3 Clock

The clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based up a module's individual requirements. The system depends on, and generates two different clocks: a high frequency clock *HFCLK* and a low frequency clock *LFCLK.*

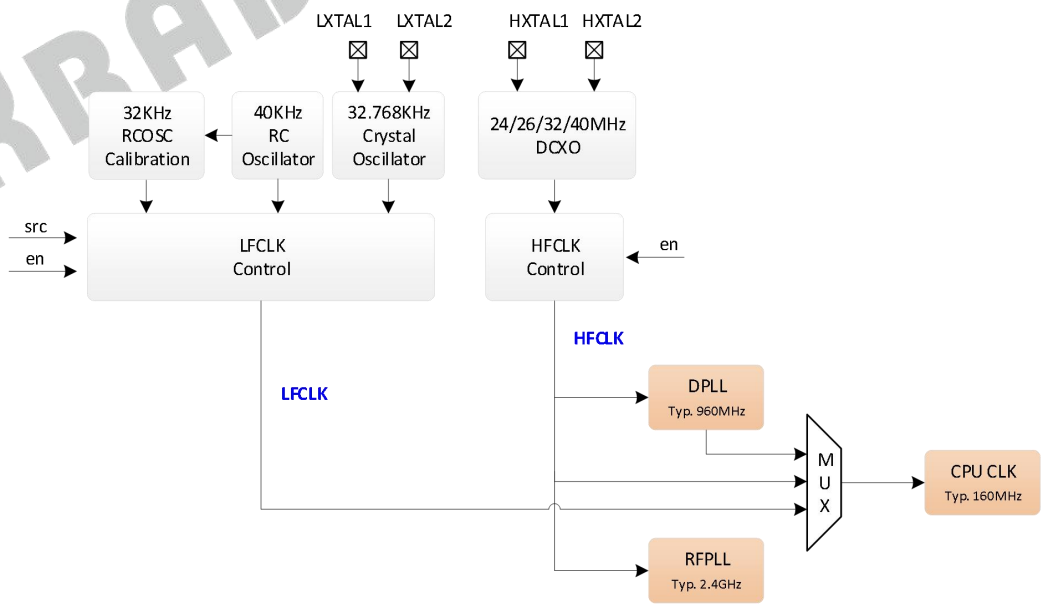
The system supports three LFCLK clock sources, the 32.768 KHz crystal oscillator, the 30~60KHz RC oscillator and the RC oscillator calibration. The 32.768 KHz crystal oscillator requires an external AT-cut quartz crystal to be connected to the LXTAL1 and LXTAL2 pins. The LFCLK clock and all of the available LFCLK sources are switched off by default when the system is powered up. The LFCLK clock can be started by selecting the preferred clock source in PRCM register. It is used for each subsystem to achieve lower current consumption for different running mode. In addition, the LFCLK is also used in RTC circuit to achieve accuracy timing.

There is only one clock source for HFCLK, the 24MHz, 26Mhz, 40MHz, 32MHz crystal oscillator. The HFCLK is enabled automatically when the system is powered up and can be switched off when all subsystems won't use it anymore in some low power modes.

The HFCLK is used to generate the clock source for Digital PLL, which is used to generate the clock sources for Cortex-AR800A core, Wi-Fi and peripherals.

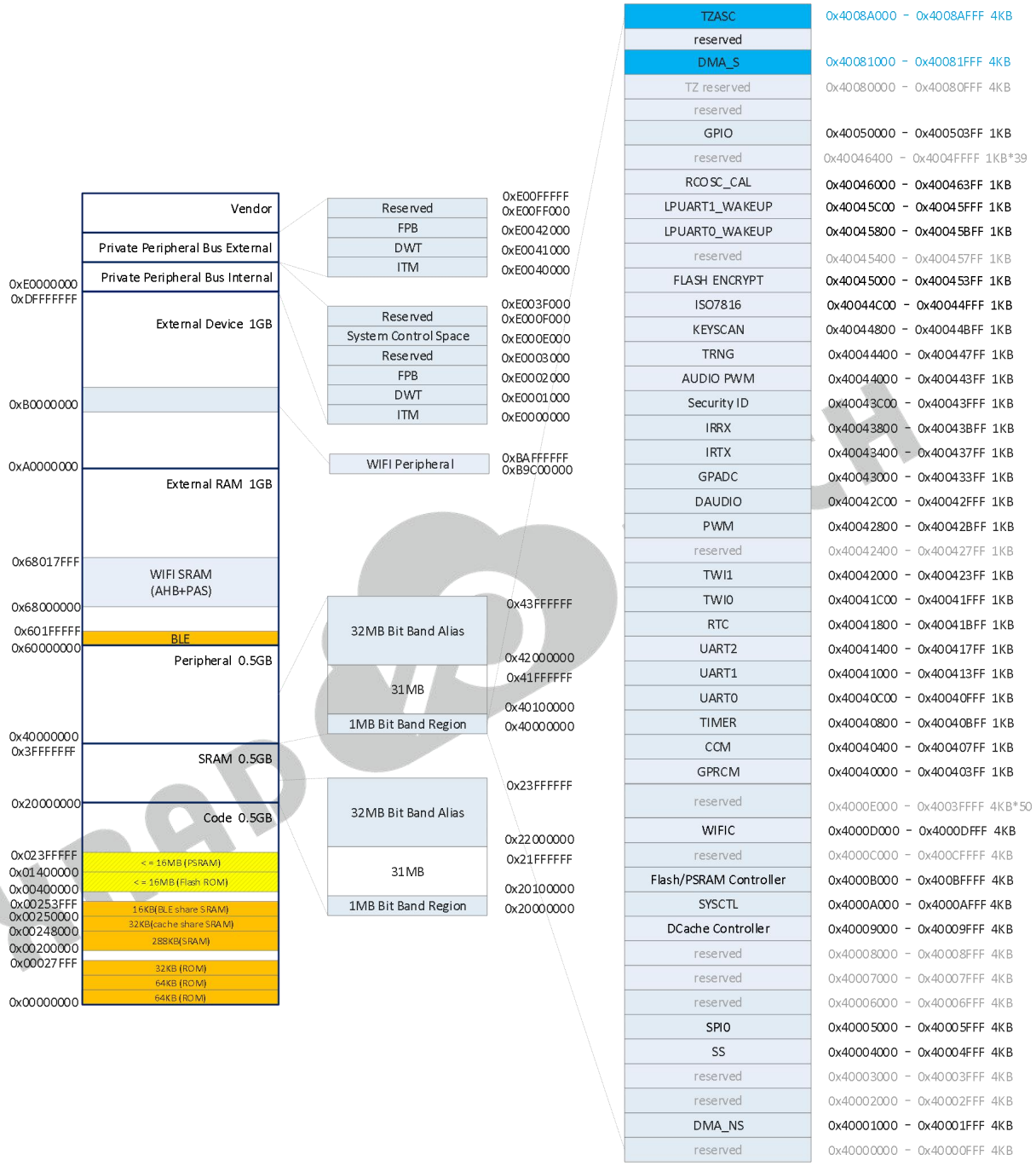
The following figure shows the clock control block diagram.

Figure 3- 6 Clock Control



3.1.4 Memory Mapping

Figure 3- 7 XR806 Memory Mapping



3.1.5 CPU

XR806 features an ARM Cortex M33 Star processor, which is the most energy efficient ARM processor available. It supports the clock rates from 32KHz up to 160MHz. The processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption.

The Cortex M33 Star core has low-latency interrupt processing with the following features:

- Mainline profile of Armv8-M including the 16 and 32-bit Thumb instruction set
- Supports for the Armv8-M Security Extension
- FPv5 hardware single precision floating Point Unit (FPU) to support DSP related function
- DSP Extension instruction set
- NVIC supporting up to 64 external interrupts with up to 256 priority levels
- MPU supporting up to 16 regions for secure and non-secure applications
- SAU supporting up to 8 memory regions as secure or non-secure
- Harvard 32-bit AMBA 5 AHB bus architecture supporting exclusive transactions and security state
- Bit-band support for memory and select peripheral that include atomic bit-band write and read operations
- Wake-up Interrupt Controller (WIC) providing ultra-low power sleep mode Supports

3.1.6 NDMA

There are 8 AHB DMA channels for this NDMA controller. Only one channel can be active and the sequence is according to the priority level.

The NDMA controller can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned. Although the increase mode of NDMA should be address aligned, but its byte counter should not be multiple. The DMA Source Address, Destination Address, Byte Counter Registers can be modified even if the DMA is started.

3.1.7 SDMA

There are 2 AHB DMA channels for this SDMA controller. Only one channel can be active and the sequence is according to the priority level.

The SDMA controller can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned. Although the increase mode of SDMA should be address aligned, but its byte counter should not be multiple. The SDMA Source Address, Destination Address, Byte Counter Registers can be modified even if the SDMA is started.

3.1.8 Crypto Engine

The Crypto Engine (CE) is one encrypt/decrypt algorithms accelerator. It is suitable for a variety of applications.

Features:

- Supports AES, DES, 3DES, SHA-1, MD5, CRC32/16, SHA256, TRNG
- Supports ECB, CBC, CTR modes for AES/DES/3DES
- Supports 128-bits, 192-bits and 256-bit key size for AES
- Supports 160-bits hardware PRNG with 192-bits seed
- 32-word RX FIFO and 32-word TX FIFO for high speed applications
- CPU mode and DMA mode are supported

The TRNG(True Random Number Generator) generates random numbers from the ring oscillator (RCO) outputs. Various types of RCOs are adopted, including Hybrid Fibonacci Ring Oscillator (H-FIRO), Hybrid Ring Oscillator (H-RO) and Hybrid Galois Ring Oscillator (H-GARO). IRQ will be issued once the random data is successfully generated.

3.1.9 Timer

Timer 0 and 1 can take their inputs from internal RC oscillator, external 32768Hz crystal or OSC. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode.

The watch-dog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds. It can generate a general reset or an interrupt request.

3.1.10 RTC

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator.

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wake-up are activated. In power-off mode, the power management wake-up signal is activated. In this section, there are two kinds of alarm. Alarm 0 is a general alarm; its counter is based on second. Alarm 1 is a weekly alarm; its counter is based on the real time.

3.2 Peripherals

3.2.1 GPIO

The XR806 GPIO unit provides as many as 26 GPIO (General Purpose IO) pins. All ports are brought out of the device using alternate function multiplexing. The GPIO function can be multiplexed on a multi-function I/O pin by selecting the GPIO alternate function in the GPIO Controller registers.

There are two types of GPIO designs in XR806: GPIO and AGPIO. Each GPIO can be configured with the following options:

- Input / Output / Floating(Hi-Z) mode
- Input mode: Pull-up or Pull-down
- Output mode: Active driving
- Pull-up/down control: the pull-up and pull-down resistance is 90KΩ with ±30% variation over PVT condition
- External Interrupt IO with 5 trigger modes: high-level, low-level, rising edge, falling edge, double edge
- 14 WAKEUP IOs can be set to wake system by external interrupt at HIBERNATION state (RTC on only)
- All IOs can be set to wake system by external interrupt at STANDBY mode (RTC and AO domain on)

The digital IO AGPIO function is equivalent to GPIO as shown above. A dedicated internal control signal is used to select between the digital and analog functions. These IOs are multiplexed with 8 channels ADC (channel 8 is internal connected to measure VBAT voltage).

GPIO PA23 has a special function which is used to enter test mode at first pup when it is high at start up. So we need to keep it without pull high (floating or tie low) to have whole chip power up correctly.

Table 3- 2 XR806B GPIO Multiplexing

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC8	FUNC9
PA00	FEM_CTRL1	AUDIO_PWMP	TWI1_SCL	IR_RX	KEY_Y0	PWM5/ECT5
PA01	FEM_CTRL2	AUDIO_PWMN	TWI1_SDA	FLASH_CS1	KEY_Y1	PWM6/ECT6
PA10/WUPIO0	ADC_CH0	SPI0_MOSI	-	UART1_RX	KEY_Y2	IR_TX
PA11/WUPIO1	ADC_CH1	SPI0_MISO	I2S_MCLK	UART1_TX	KEY_Y3	IR_RX
PA12/WUPIO2	ADC_CH2	PWM4/ECT4	I2S_BCLK	IR_TX	KEY_Y4	TWI0_SCL
PA13/WUPIO3	ADC_CH3	PWM5/ECT5	I2S_DI	UART2_TX	KEY_Y5	TWI0_SDA
PA14/WUPIO4	ADC_CH4	PWM6/ECT6	I2S_DO	UART2_RX	KEY_Y6	-
PA15/WUPIO5	ADC_CH5	SPI0_CS0	I2S_LRCLK	UART2_CTS	KEY_Y7	TWI1_SCL
PA16/WUPIO6	ADC_CH6	SPI0_CLK	-	UART2_RTS	KEY_X0	TWI1_SDA
PA17/WUPIO7	TWI0_SCL	AUDIO_PWMP	32KOSCO	IR_TX	KEY_X1	-
PA18/WUPIO8	TWI0_SDA	AUDIO_PWMN	FEM_CTRL2	FLASH_CS1	KEY_X2	-
PA19/WUPIO9	UART2_RTS	CARD_DATA	PWM0/ECT0	SPI0_MOSI	KEY_X3	AUDIO_PWMP
PA20/WUPIO10	UART2_CTS	CARD_CLK	PWM1/ECT1	SPI0_MISO	KEY_X4	AUDIO_PWMN
PA21/WUPIO11	UART2_RX	CARD_RST	PWM2/ECT2	SPI0_CS0	KEY_X5	I2S_DO
PA22/WUPIO12	UART2_TX	CARD_DETECT	PWM3/ECT3	SPI0_CLK	KEY_X6	I2S_LRCLK
PA23/WUPIO13/TEST	DCXO_PUP_OUT	IR_RX	FEM_CTRL1	FEM_CTRL2	KEY_X7	I2S_MCLK
PB00[1]	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	KEY_Y8	-
PB01[1]	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	KEY_Y9	-
PB02	UART0_CTS	JTAG_TDO	PWM6/ECT6	FLASH_WP/IO2	KEY_Y1	SWD_TMS
PB03	UART0_RTS	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO3	KEY_Y1	SWD_TCK
PB04	SPI0_MOSI	PWM0/ECT0	UART1_RTS	FLASH_MOSI/IO0	KEY_Y1	I2S_BCLK
PB05	SPI0_MISO	PWM1/ECT1	UART1_CTS	FLASH_MISO/IO1	KEY_Y1	I2S_DI
PB06	SPI0_CS0	PWM2/ECT2	UART1_RX	FLASH_CS0	KEY_Y1	I2S_DO
PB07	SPI0_CLK	PWM3/ECT3	UART1_TX	FLASH_CLK	KEY_Y1	I2S_LRCLK
PB14[1]	UART1_TX	UART2_TX	TWI1_SCL	UART0_CTS	KEY_Y0	PWM5/ECT5
PB15[1]	UART1_RX	UART2_RX	TWI1_SDA	UART0_RTS	KEY_Y1	PWM6/ECT6

NOTE

1. Supports 1.8V/3.3V/5V IO type; Others only support 1.8V/3.3V IO type;
2. refer to document of 'XR806 PIN MUX.pdf' for other functions;

Table 3- 3 XR806AF2L GPIO Multiplexing

GPIO	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
PA11/WUPIO1	ADC_CH1	SPI0_MISO	I2S_MCLK	UART1_TX	EINTA11
PA12/WUPIO2	ADC_CH2	PWM4/ECT4	I2S_BCLK	IR_TX	EINTA12
PA13/WUPIO3	ADC_CH3	PWM5/ECT5	I2S_DI	UART2_TX	EINTA13
PA19/WUPIO9	UART2_RTS	CARD_DATA	PWM0/ECT0	SPI0_MOSI	EINTA19
PA20/WUPIO10	UART2_CTS	CARD_CLK	PWM1/ECT1	SPI0_MISO	EINTA20
PA21/WUPIO11	UART2_RX	CARD_RST	PWM2/ECT2	SPI0_CS0	EINTA21
PA22/WUPIO12	UART2_TX	CARD_DETECT	PWM3/ECT3	SPI0_CLK	EINTA22
PA23/WUPIO13/TES	DCXO_PUP_O	IR_RX	FEM_CTRL1	FEM_CTRL2	EINTA23
PB00[1]	UART0_TX	JTAG_TMS	PWM4/ECT4	SWD_TMS	EINTB0
PB01[1]	UART0_RX	JTAG_TCK	PWM5/ECT5	SWD_TCK	EINTB1
PB02	UART0_CTS	JTAG_TDO	PWM6/ECT6	FLASH_WP/IO2	EINTB2
PB03	UART0_RTS	JTAG_TDI	PWM7/ECT7	FLASH_HOLD/IO3	EINTB3
PB04	SPI0_MOSI	PWM0/ECT0	UART1_RTS	FLASH_MOSI/IO0	EINTB4
PB05	SPI0_MISO	PWM1/ECT1	UART1_CTS	FLASH_MISO/IO1	EINTB5
PB06	SPI0_CS0	PWM2/ECT2	UART1_RX	FLASH_CS0	EINTB6
PB07	SPI0_CLK	PWM3/ECT3	UART1_TX	FLASH_CLK	EINTB7
PB14[1]	UART1_TX	UART2_TX	TWI1_SCL	UART0_CTS	EINTB14
PB15[1]	UART1_RX	UART2_RX	TWI1_SDA	UART0_RTS	EINTB15

NOTE

1. Supports 1.8V/3.3V/5V IO type; Others only support 1.8V/3.3V IO type;
2. refer to Table 3-2 or document of 'XR806 PIN MUX.pdf' for other functions;

3.2.2 UART

The XR806 provides 3 UART controllers: one is used for debug and two with auto-flow control are used for communication with external devices. The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

Features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- Supports DMA controller interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR

- Supports RS-485 mode
- Supports configurable baud rate from 9600, 19200, 38400, 115200 and 921600 etc.
- Supports baud rate detection

3.2.3 SPI

The XR806 features one SPI controller which can be configured to a SPI master or a SPI slave. It is used as an extension interface to control the peripheral devices. And it supports two options of clock polarity (CPOL) and two options of initial clock phase (CPHA).

Figure 3- 8 SPI Phase 0 Transfer Format

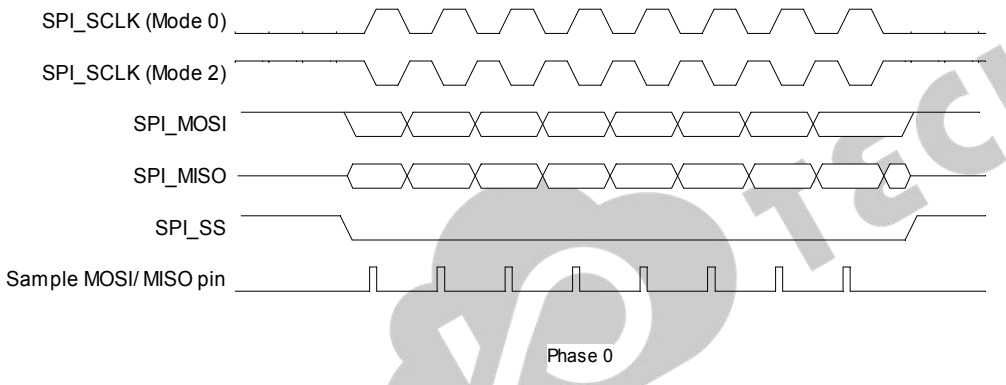
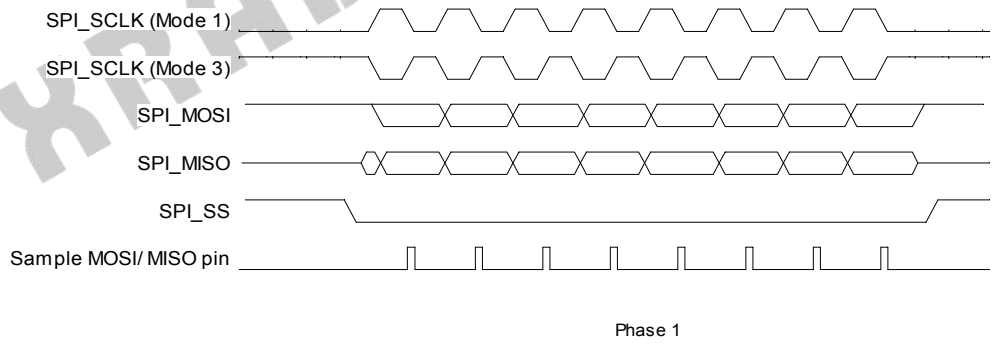


Figure 3- 9 SPI Phase 1 Transfer Format



3.2.4 TWI

The XR806 features two TWI serial interfaces. They can be configured as master and salve mode. Each TWI controller supports three IO mapping. The TWI controllers can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400Kbps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

Features:

- Compatible with IIC protocol and SCCB protocol
- Software-programmable for Slave or Master
- Supports Repeated START signal
- Multi-master systems are supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

3.2.5 PWM

XR806 features 8 PWMs to generate pulse sequences with programmable frequency a duration for LCD, vibrators and other devices. The PWM controller provides 8 PWM channels, which are divided into four pairs of PWM pair, each is composed of three parts: a clock controller, two timer modules, a programmable dead-zone generator. The PWM channel logic can be configured as input capture function. The capturer detects the rising edge and the falling edge of the signal and calculates the high-level and the low-level duration with a 16-bit counter.

Features:

- 8 PWM channels, divided into 4 PWM pairs
- Supports pulse, period and complementary pair outputs
- Supports input capture
- Programmable dead-zone generator
- Configurable output frequency, 0%-100% duty adjustable

3.2.6 Audio PWM

XR806 features a Digital Differential PWM driver to drive external Class-D audio amplifier. The DPWM driver works by up-sampling and modulating a PCM input to a differential signal drive the AUDIO_PWMP and AUDIO_PWMN pins. The output amplitude of the DPWM driver is controlled by VDD_IO voltage.

Features:

- One Mono Digital Audio PWM Driver

- SNR ≥ 95dB (A-Weighting).
- THD+N ≤ -80dB (A-Weighting).
- Supports playback sample rates from 8KHz to 48KHz.

- One 64x18-bits FIFO for playback data transmit.
- Programmable FIFO thresholds.
- DMA and Interrupt support.

3.2.7 CIR

XR806 features an infrared remote transmitter and a receiver controller. Through the process control pulse waveform, the remote controller can support a variety of infrared protocol.

The IR receiver controller features:

- Full physical layer implementation
- Supports IR for remote control
- 64x8 bits FIFO for data buffer

The IR transmitter controller features:

- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Interrupt and DMA support

3.2.8 GPADC

XR806 features one GPADC function. The ADC function contains a 8-channel analog switch, a single end input asynchronous 12-bit SAR (Successive Approximation Register) ADC. The channels 0 to 6 are used to detect the voltage of the external input and the channel 8 is dedicated to detect the voltage of the VBAT.

Features:

- 12-bit Resolution and 10-bit effective SAR type A/D converter
- 8-channel multiplexer, 7 normal channel and 1 VBAT voltage detection channel
- 64 FIFO depth of data register
- DMA supports
- Power supply 1.8~3.6V, internal analog circuit generate 1.4V or 2.5V to Vref

- Maximum Sampling frequency: 1 MHz
- Supports wake-up from standby mode
- Supports self-calibration
- Supports data compare and interrupt
- Supports operation mode: Continuous conversion mode, Outbreak conversion mode

3.2.9 I2S

XR806 features one DAI(Digital Audio Interface) Controller function. The controller supports standard I2S format, Left-justified Mode format, Right-justified Mode format, PCM Mode format and TDM Mode format.

Features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Supports full-duplex synchronous work mode
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Supports Master / Slave mode
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Supports up to 8 slots which has adjustable width from 8-bit to 32-bit
- Supports sample rate from 8KHz to 192KHz
- Supports 8-bits u-law and 8-bits A-law companding sample
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)

3.2.10 Smart Card

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation. Cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

Feature:

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:

- Card activation and deactivation
- Cold/warm reset
- Answer to Reset (ATR) response reception
- Data transfers to and from the card

- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- 128bits FIFO for data transmit & receive.
- Supports FIFOs for receive and transmit buffers (up to 128 bits) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

3.3 Wi-Fi Subsystem

3.3.1 Wi-Fi MAC

Supports MAC enhancements including:

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11h - Transmit power control dynamic and frequency selection
- 802.11i - Security including WPA2 compliance
- 802.11r - Roaming

3.3.2 Wi-Fi Baseband

Features:

- Compatible with IEEE 802.11 b/g/n standard
- 802.11n MCS0-7 with data rate up to 72.2Mbps (BPSK, r=1/2 through 64QAM, r=5/6)
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Short Guard Interval
- Long Guard Interval
- RX antenna Diversity

3.3.3 Wi-Fi Radio

Features:

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network and harmonic filter allow chip to connect to antenna directly
- High Power Amplifier with 1.4~3.3V full range directly Supports XRADIOTECH's MPD™ technology ensure linearity tracking automatically to always keep EVM and mask within specifications
- Special Architecture and Device design to keep the reliability of PA up to 3.3V high voltage and also deliver high output power (>25dBm)

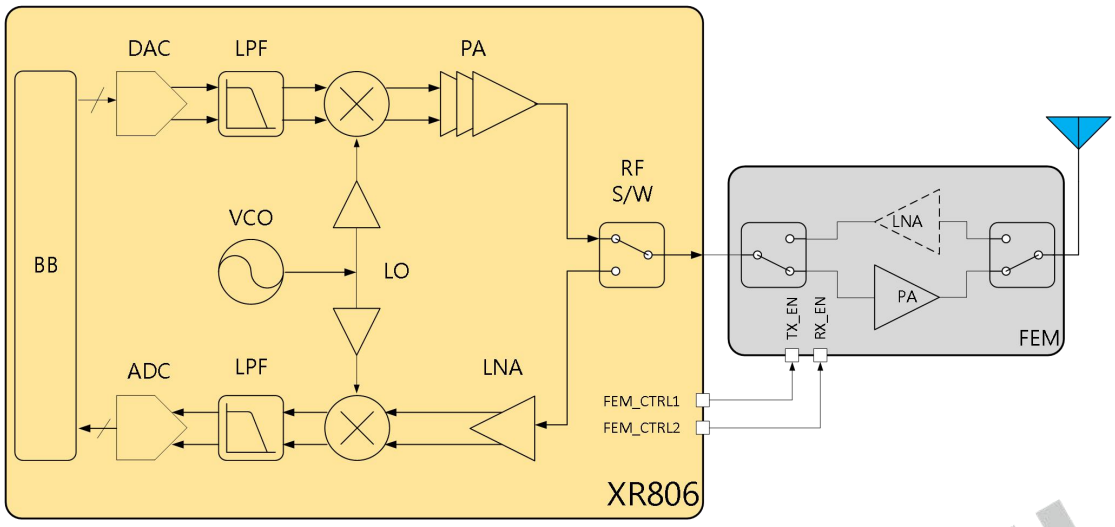
3.3.4 Front End Module Control

For applications that use external front-end components, the XR806 provides the ability to control them with two antenna switch control outputs named:

- FEM_CTRL1: TX_EN
- FEM_CTRL2: RX_EN

FEM_CTRL1 and FEM_CTRL2 are used to control TX and RX signal path separately. It is very useful when customer want to use XR806 to extend range coverage by add addition high output power RF PA. The typical extend application is below:

Figure 3- 10 FEM Control Application Diagram



3.4 Bluetooth Subsystem

Features:

- Complies with Bluetooth V5.0 LE features
- Data rates support: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- Long range feature supports
- TRNG generator
- AES-128 data encryption with ECB and CCM mode
- Advertising Extension supports
- Packet Assembly and Disassembly
- Data Whitening and De-whitening
- Data CRC generation and checking
- Packet filtering based on filter policies (white and resolving lists)
- Private address generation and Accelerate address resolution
- Access address generation and matching
- Frequency hopping and channel mapping
- RSSI Reporting to host

4 Electrical Characteristics

4.1 Absolute Maximum Rating

Table 4- 1 Absolute Maximum Rating

Symbol	Parameter	Maximum rating	Unit
I/O	In/Out current for input and output	-35 to 35	mA
VBAT	1.8~5.5V Power supply	-0.3 to 6.0	V
CHIP_PWD	RESET pin for chip	-0.3 to 6.0	V
VDD_TX	Power supply	-0.3 to 3.0	V
VDD_DIG	Power supply	-0.3 to 1.5	V
VDD_EXT	Power supply	-0.3 to 4.0	V
VDD_IO	Power supply	-0.3 to 4.0	V
VDD_IO_5V	Power supply	-0.3 to 6.0	V
T_{opr}	Operating Temperature	-40 to 105	°C
$T_{junction}$	Junction Temperature	-40 to 125	°C
T_{stg}	Storage Temperature	-55 to 125	°C
VESD	HBM	-2000/+2000	V
VESD	CDM	-500/+500	V

4.2 Recommended Operating Conditions

Table 4- 2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_a	Ambient Operating Temperature	-40	-	105	°C
VBAT	Power supply of chip input	1.8	3.3	5.5	V
CHIP_PWD	RESET	1.8	3.3	5.5	V
VDD_ANA	Power supply of analog/RF input	1.4	1.6	2.5	V
VDD_PA	Power supply of PA	1.4	3.3	3.6	V
VDD_DIG	Power supply of digital input	0.6	1.1	1.35	V
VDD_EXT	Power supply of external device input	2.5	3.3	3.5	V
VDD_IO	Power supply of GPIO input	1.8	3.3	3.6	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_IO_5V	Power supply of GPIO 5V input	1.8	3.3	5.5	V

4.3 Digital IO Characteristics

Table 4- 3 DC Characteristics of VDD_IO=3.3V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO=3.3V	-0.3	1.32	V
V_{IH}	Input High Voltage	VDD_IO=3.3V	2.06	3.6	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 7.5~50 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 7.5~50 mA	2.9	3.6	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	35	95	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	35	95	KΩ

Table 4- 4 DC Characteristics of VDD_IO=1.8V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO=1.8V	-0.3	0.65	V
V_{IH}	Input High Voltage	VDD_IO=1.8V	1.18	1.98	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 2.25~15 mA	-0.3	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 2.25~15 mA	1.44	2.0	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	63	190	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	63	190	KΩ

Table 4- 5 DC Characteristics of VDD_IO_5V=5V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VDD_IO_5V=5V	-0.3	0.81	V
V_{IH}	Input High Voltage	VDD_IO_5V=5V	1.3	5.5	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 5~47 mA	-0.3	0.5	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 5~47 mA	4.5	5.0	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	63	150	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	63	150	KΩ

4.4 Bootstrap Modes and Pins

Table 4- 6 Bootstrap pins

Symbol	Bootstrap Function Name	Value	Description
PA23	Test Mode	0	Normal operation mode
		1	Enter into test/debug mode when releasing CHIP_PWD
PB02	Boot Mode	0	when releasing CHIP_PWD will cause the system going to firmware update mode.
		1	Internal normal boot

4.5 Frequency Reference Clock

4.5.1 High Frequency Reference Clock

Table 4- 7 External Reference Clock Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{IN}	Clock input frequency list using an external clock source	-	24,26,32,40	-	MHz
	Clock input frequency list using a XTAL and the built-in oscillator	-	24,26,32,40	-	MHz
F_{INTOL}	Tolerance on input frequency without trimming	-20	-	+20	ppm
T_{stable}	Clock stabilization time	-	-	10	ms
I_{LEAK}	Input leakage current, both for analog and digital	-	-	1	uA

4.5.1.1 Clock Source Detection

An integrated automatic detection mechanism detects the clock source from the connections of the HXTAL1 and HXTAL2 pins:

- When an external reference clock source is used, the clock input pin is HXTAL2. The XR806 supports both an analog and digital source. An analog source shall be AC coupled to HXTAL2 while a digital source shall be DC coupled to HXTAL2. In both cases, HXTAL1 shall be DC grounded.
- When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to HXTAL1 and HXTAL2.

4.5.1.2 External Clock Source

Table 4- 8 External Clock Requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit
AC coupled signal					
F_{IN}	Frequency	-	24,26,32,40	-	MHz
V_{PP}	Peak-to-peak voltage range of the AC coupled analog input	0.6	1.0	1.5	V
N_H	Total harmonic content of the input signal	-	-	-25	dBc
DC coupled signal					
V_{IL}	input low voltage on HXTAL2	0	-	0.3*1.5	V
V_{IH}	input high voltage on HXTAL2	0.7*1.5	-	1.5	V
Tr/T_f	10%-90% rise and fall time	-	-	5	ns
Duty Cycle	Cycle-to-cycle	40	50	60	%
Both analog and digital signals					
Phase Noise	Ref clock @ 24 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	 -123 -133 -138 -138	dBc/Hz

4.5.1.3 External XTAL and Built-in Oscillator

Table 4- 9 External High Frequency Crystal Characteristics Requirements

Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		-	24,26,32,40	-	MHz
ESR		-	-	60	Ω
Cin_xtal[1]	Single-ended	0	3.5	15	pF
Load Capacitance[1]		-	16	27	pF
Oscillator Tuning Range[2]		+/-20	+/-50	+/-70	ppm
Crystal Frequency Accuracy at Nominal Temp.	25 °C	-10	-	+10	ppm
Crystal Drift Due to Temperature	-20 to +85 °C	-10	-	+10	ppm
Crystal Pull Ability		10	-	150	ppm/pF

Symbol	Conditions	Min.	Typ.	Max.	Unit

NOTE

1. The load capacitance value (C_{load}) and shunt capacitance value(C_{shunt}) depends on XTAL model, XTAL1 and XTAL2 pin have inside capacitance (C_{in_xtal}), so external added load capacitance value (PCB Welding Capacitance) $C_{load\_ext} = C_{load} * 2 - C_{in\_xtal} - C_{pcb} - C_{shunt} * 2$, C_{pcb} is PCB parasitic capacitance(single-ended). C_{in_xtal} has tuning range about 25.4pF, which is controlled by software.

2. Tuning range depends on XTAL load capacitance requirement, typical case is based on 24MHz XTAL, 16pF Cload.

4.5.2 Low Frequency Reference Clock

XR806 use low frequency reference clock, it can either use an external low frequency crystal and a built-in oscillator, or internal RCOSC. The external crystal and a built-in oscillator is used during power save modes.

4.5.2.1 External XTAL and Built-in Oscillator

Table 4- 10 External Low Frequency Crystal Characteristics Requirements

Symbol	Conditions	Min.	Typ.	Max.	Unit
Nominal Frequency	-	-	32.768	-	KHz
Load Capacitance[1]	-	-	-	-	pF
C_{shunt}[1]	-	-	2	-	pF

NOTE

1. The load capacitance value (C_{load}) and shunt capacitance value(C_{shunt}) depends on LXTAL model, external added load capacitance value (PCB Welding Capacitance) $C_{load\_ext} = C_{load} * 2 - C_{pcb} - C_{shunt} * 2$, C_{pcb} is PCB parasitic capacitance(single-ended).

4.5.2.2 Internal RCOSC Reference Clock Source

XR806 have an integrated RC oscillator low frequency reference clock source inside. This clock is calibrated by CPU clock source from high frequency reference. RCOSC takes effect automatically when there is no external crystal.

4.6 Wi-Fi 2.4G RF Receiver Specifications

Table 4- 11 RF Receiver Specifications

Condition: VBAT=3.3V, VDD_ANA=1.5V, Temperature=25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412	-	2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS	-96.8	-98.8	-	dBm
	2Mbps DSSS	-93.7	-95.7	-	dBm
	5.5Mbps CCK	-92.0	-94.0	-	dBm
	11Mbps CCK	-89.0	-91.0	-	dBm
RX Sensitivity (802.11g)	6Mbps OFDM	-91.8	-93.8	-	dBm
	9Mbps OFDM	-91.0	-93.0	-	dBm
	12Mbps OFDM	-90.0	-92.0	-	dBm
	18Mbps OFDM	-87.0	-89.0	-	dBm
	24Mbps OFDM	-84.5	-86.5	-	dBm
	36Mbps OFDM	-81.0	-83.0	-	dBm
	48Mbps OFDM	-77.0	-79.0	-	dBm
	54Mbps OFDM	-75.3	-77.3	-	dBm
RX Sensitivity (802.11n, 20MHz)	MCS 0	-91.0	-93.0	-	dBm
	MCS 1	-88.0	-90.0	-	dBm
	MCS 2	-86.0	-88.0	-	dBm
	MCS 3	-83.0	-85.0	-	dBm
	MCS 4	-79.7	-81.7	-	dBm
	MCS 5	-75.5	-77.5	-	dBm
	MCS 6	-73.8	-75.8	-	dBm
	MCS 7	-72.0	-74.0	-	dBm
Maximum Receive Level	6 Mbps OFDM	-10.0	5.0	-	dBm
	54 Mbps OFDM	-10.0	-5.0	-	dBm
	MCS0	-10.0	5.0	-	dBm
	MCS7	-20.0	-6.7	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	40.0	-	-	dBc
	11 Mbps CCK	35.0	-	-	dBc

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
	BPSK rate 1/2, 6 Mbps OFDM	30.2	-	-	dBc
	64QAM rate 3/4, 54 Mbps OFDM	12.7	-	-	dBc
	HT20, MCS 0, BPSK rate 1/2	27.3	-	-	dBc
	HT20, MCS 7, 64QAM rate 5/6	8.2	-	-	dBc

NOTE

The minimum limit considers the variation of process, voltage and temperature.

4.7 Wi-Fi 2.4G RF Transmitter Specifications

Table 4- 12 RF Transmitter Specifications

Condition1: VBAT=3.3V, VDD_PA=3.3V, VDD_ANA=1.5V, Temperature=25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412	-	2484	MHz
TX output Power with mask and EVM compliance[1]	1Mbps DSSS	-	19.5	-	dBm
	11Mbps CCK	-	19.6	-	dBm
	6Mbps OFDM	-	16.1	-	dBm
	54Mbps OFDM	-	15.9	-	dBm
	HT20, MCS 0	-	16.1	-	dBm
	HT20, MCS 7	-	15.1	-	dBm
TX EVM	1Mbps DSSS	-	-17.0	-9.1	dB
	11Mbps CCK	-	-16.5	-9.1	dB
	6Mbps OFDM	-	-30.7	-5.0	dB
	54Mbps OFDM	-	-29.6	-25.0	dB
	HT20, MCS 0	-	-30.5	-5.0	dB
	HT20, MCS 7	-	-31.8	-28.0	dB
Carrier Suppression		-	-	-30.0	dBc
Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5	-	1.5	dB

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Harmonic Output Power	2nd Harmonic	-	-	-30.0	dBm/MHz
	3rd Harmonic	-	-	-30.0	dBm/MHz

NOTE

1. Refer to IEEE 802.11 specification for Tx spectrum limits:

- 802.11b mask (18.4.7.3)

- 802.11g mask (19.5.4)

- 802.11g EVM (17.3.9.6.3)

- 802.11n HT20 mask (20.3.21.1)

- 802.11n HT20 EVM (20.3.21.7.3)

2. The minimum limit considers the variation of process, voltage and temperature.

4.8 Bluetooth RF Receiver Specifications

Table 4- 13 RF Receiver Specifications

Condition: VBAT=3.3V, VDD_ANA=1.5V, Temperature=25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2400	-	2484	MHz
RX Sensitivity	BLE Sensitivity at 1Mbps, PER≤30.8%	-	TBD	-	dBm
	BLE Sensitivity at 2Mbps, PER≤30.8%	-	TBD	-	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%, S=2	-	TBD	-	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%, S=8	-	TBD	-	dBm
Maximum Receiving Power	-	-	TBD	-	dBm
BLE Selectivity (1Mbps)	Co-channel	-	TBD	-	dB
	1MHz offset	-	TBD	-	dB

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
	2MHz offset	-	TBD	-	dB
	>=3MHz offset	-	TBD	-	dB
	Image	-	TBD	-	dB
	Image +/-1MHz	-	TBD	-	dB
BLE Selectivity (2Mbps)	Co-channel	-	TBD	-	dB
	1MHz offset	-	TBD	-	dB
	2MHz offset	-	TBD	-	dB
	>=3MHz offset	-	TBD	-	dB
	Image	-	TBD	-	dB
	Image +/-1MHz	-	TBD	-	dB
Intermodulation Power	Tested as per BLE standard requirements	-	TBD	-	dBm
Blockers (1Mbps)	30MHz-2000MHz	-	TBD	-	dBm
	2003MHz-2399MHz	-	TBD	-	dBm
	2.484GHz-2.997GHz	-	TBD	-	dBm
	3.0GHz-12.75GHz	-	TBD	-	dBm

NOTE

The minimum limit considers the variation of process, voltage and temperature.

4.9 Bluetooth RF Transmitter Specifications

Table 4- 14 RF Transmitter Specifications

Condition1: VBAT=3.3V, VDD_PA=3.3V, VDD_ANA=1.5V, Temperature=25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2400	-	2484	MHz
FSK Data Rate	-	-	1.0	-	Mbps
Modulation Deviation	BLE@1Mbps	225	250	275	KHz
	BLE@2Mbps	450	500	550	KHz
Output Power	LP mode	-20	-	13	dBm

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Range	HP mode	10	-	20	dBm
TX RF Output Steps	-	-	2	-	dB
TX Power Variation vs. Temp	-40~125oC	-	+/-1	-	dB
TX Power Variation vs. Frequency	-40~125oC	-	+/-1	-	dB
In Band Spurious Emissions (1Mbps)	Frequency offset=2MHz	-	-38.5	-	dBm
	Frequency offset=3MHz	-	-39.8	-	dBm
In Band Spurious Emissions (2Mbps)	Frequency offset=4MHz	-	-45.2	-	dBm
	Frequency offset=5MHz	-	-45.6	-	dBm
	Frequency offset=6MHz	-	-46.9	-	dBm
Out of Band Spurious Emissions (at 6dBm)	Frequencies<2.4GHz	-	-	-50	dBm
Out of Band Spurious Emissions (at 20dBm)	2.48-12GHz, including harmonics	-	-	-40	dBm

NOTE

The minimum limit considers the variation of process, voltage and temperature.

4.10 Power Consumptions with Wi-Fi

Table 4- 15 Power Consumption 1

Temp=25°C, VBAT=3.3V, VDD_ANA=1.5V, internal DC-DC 90% efficiency, MCU 160MHz

Symbol	MCU State	Wi-Fi State	TX/ RX	Test Condition （Signaling Mode）		Performance			
						Min.	Typ.	Max.	Unit
ACTIVE	ACTIVE	ACTIVE	TX[1]	1M DSSS	17dBm	-	189.0	-	mA
				11M CCK	17dBm	-	190.0	-	mA
				6M OFDM	16dBm	-	188.0	-	mA
				54M OFDM	16dBm	-	192.0	-	mA
				HT20, MCS0	16dBm	-	188.0	-	mA
				HT20, MCS7	15dBm	-	181.0	-	mA

Symbol	MCU State	Wi-Fi State	TX/ RX	Test Condition （Signaling Mode）		Performance			
						Min.	Typ.	Max.	Unit
			RX	1M DSSS	-	-	38.5	-	mA
				11M CCK	-	-	39.0	-	mA
				6M OFDM	-	-	40.0	-	mA
				54M OFDM	-	-	41.5	-	mA
				HT20, MCS0	-	-	40.0	-	mA
				HT20, MCS7	-	-	41.0	-	mA
STANDBY	SLEEP	ACTIVE	TX[1]	1M DSSS, null frame	17dBm	-	189.0	-	mA
			RX	RX listen	-	-	34.1	-	mA
				1M DSSS	-	-	29.4	-	mA
		PS Mode[2]	RX	DTIM1	-	-	838.0	-	uA
				DTIM3	-	-	372.0	-	uA
				DTIM8	-	-	179.0	-	uA
				DTIM10	-	-	161.0	-	uA
		OFF	-	-	-	-	54.0	-	uA
HIBERNATION[3]	OFF	OFF	-	-	-	-	5.8	-	uA
SHUTDOWN[4]	OFF	OFF	-	-	-	-	0.3	-	uA

NOTE

1. Data is captured at TX continues mode on the duration of transmitting;
2. Use XR806 by external 32K XTAL, Beacon length 1.8ms；
3. RTC and wake up timer on only;
4. CHIP_PWD keeps at low level;

Table 4- 16 Power Consumption 2

Temp=25°C, VBAT=3.3V, VDD_ANA=1.5V, LDO supply, MCU 160MHz

Symbol	MCU State	Wi-Fi State	TX/ RX	Test Condition （Signaling Mode）		Performance			
						Min.	Typ.	Max.	Unit
ACTIVE	ACTIVE	ACTIVE	TX[1]	1M DSSS	17dBm	-	236.0	-	mA
				11M CCK	17dBm	-	238.0	-	mA
				6M OFDM	16dBm	-	260.0	-	mA
				54M OFDM	16dBm	-	267.0	-	mA

Symbol	MCU State	Wi-Fi State	TX/ RX	Test Condition （Signaling Mode）		Performance			
						Min.	Typ.	Max.	Unit
				HT20, MCS0	16dBm	-	261.0	-	mA
				HT20, MCS7	15dBm	-	252.0	-	mA
			RX	1M DSSS	-	-	73.0	-	mA
				11M CCK	-	-	74.0	-	mA
				6M OFDM	-	-	77.0	-	mA
				54M OFDM	-	-	78.0	-	mA
				HT20, MCS0	-	-	77.0	-	mA
				HT20, MCS7	-	-	79.0	-	mA
STANDBY	SLEEP	ACTIVE	TX[1]	1M DSSS, null frame	19dBm	-	236.0	-	mA
			RX	RX listen	-	-	66.0	-	mA
				1M DSSS	-	-	54.0	-	mA
		PS Mode[2]	RX	DTIM1	-	-	1330.0	-	uA
				DTIM3	-	-	584.0	-	uA
				DTIM8	-	-	356.0	-	uA
				DTIM10	-	-	258.0	-	uA
		OFF	-	-	-	-	55.0	-	uA
HIBERNATION[3]	OFF	OFF	-	-	-	-	6.0	-	uA
SHUTDOWN[4]	OFF	OFF	-	-	-	-	0.3	-	uA

NOTE

1. Data is captured at TX continues mode on the duration of transmitting;
2. Use XR806 by RCOSC, Beacon length 1.8ms；
3. RTC and wake up timer on only;
4. CHIP_PWD keeps at low level;

4.11 Power Consumptions with Bluetooth only

Table 4- 17 Power Consumption with Bluetooth

Temp=25°C, VBAT=3.3V, VDD_ANA=1.5V, external DC-DC 90% efficiency, MCU 160MHz

Symbol	MCU State	Wi-Fi State	TX/ RX	Test Condition	Performance			
					Min.	Typ.	Max.	Unit
ACTIVE	ACTIVE	ACTIVE	TX[1]	0dBm	-	TBD	-	mA
				6dBm	-	TBD	-	mA
				10dBm	-	TBD	-	mA
				20dBm	-	TBD	-	mA
			RX	Low Power	-	TBD	-	mA
				High Performance	-	TBD	-	mA
HIBERNATION[2]	OFF	OFF	-	-	-	TBD	-	uA
SHUTDOWN[3]	OFF	OFF	-	-	-	TBD	-	uA

NOTE

1. Data is captured at TX continues mode on the duration of transmitting;
2. RTC and wake up timer on only;
3. CHIP_PWD keeps at low level;

5 Package Specifications

5.1 Pin Layout

XR806 uses 5mm x 5mm QFN40 package and 4mm x 4mm QFN32 package for different feature lists.

Figure 5- 1 XR806BF2L Pin Layout

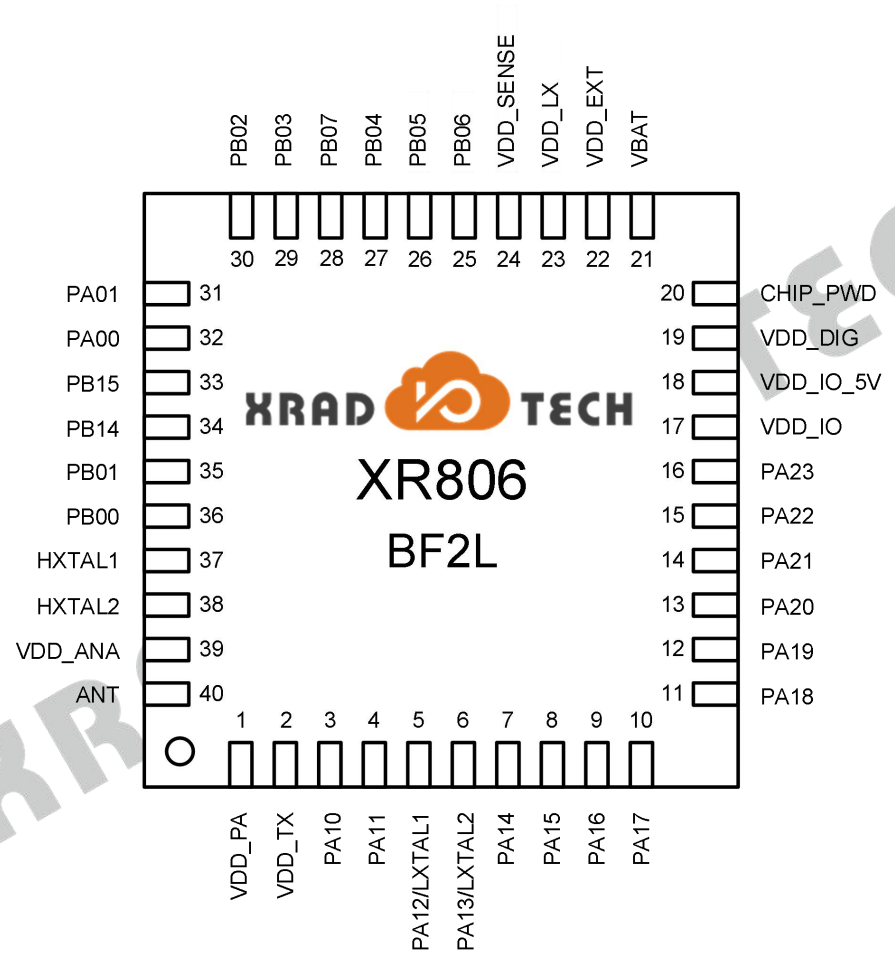


Figure 5- 2 XR806BM2I Pin Layout

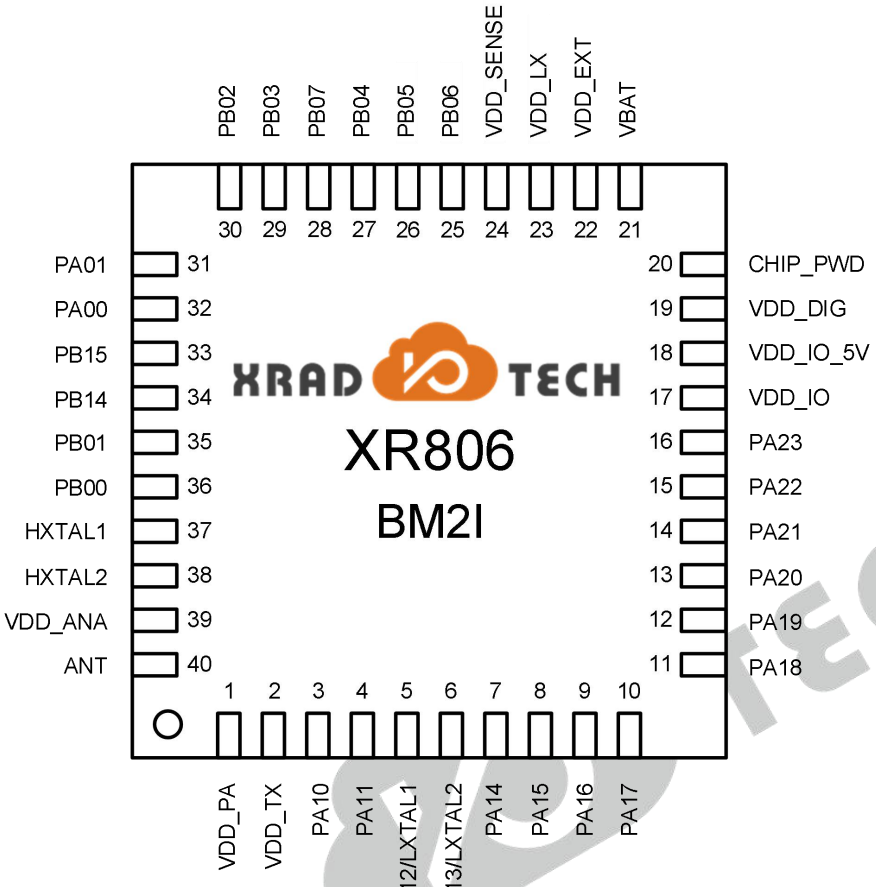
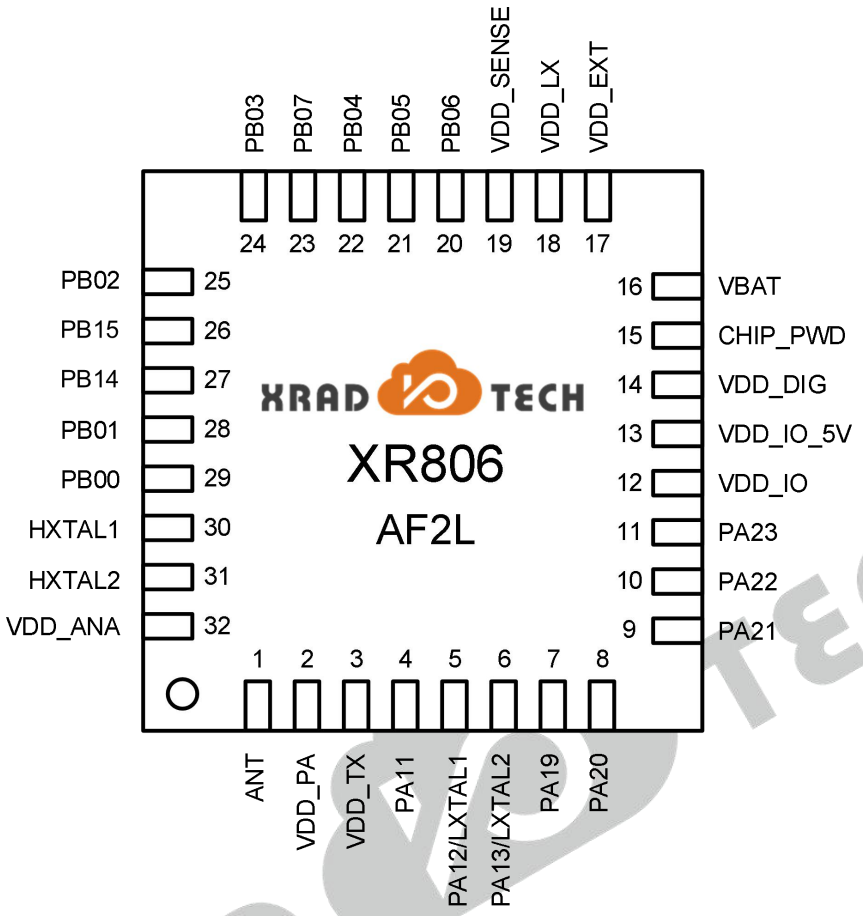


Figure 5- 3 XR806AF2L Pin Layout



5.2 Pin Descriptions

Table 5- 1 Pin Description

Pin Name	I/O	XR806B	XR806A	Pin Description
Power, Reset and Clocks				
VDD_PA	Input	1	2	PA power supply
VDD_TX	Input	2	3	RF power supply
LXTAL1	Analog	5[1]	5[1]	32KHz crystal
LXTAL2	Analog	6[2]	6[2]	32KHz crystal
VDD_IO	Input	17	12	GPIO 3.3V/1.8V power supply
VDD_IO_5V	Input	18	13	GPIO 5V/3.3V/1.8V power supply
VDD_DIG	Output	19	14	Dig Core 1.1V power supply
CHIP_PWD	Input	20	15	Chip Power Down/System Reset
VBAT	Input	21	16	1.8~5.5V power supply
VDD_EXT	output	22	17	external device power supply
VDD_LX	Input	23	18	BUCK power supply
VDD_SENSE	Output	24	19	BUCK output

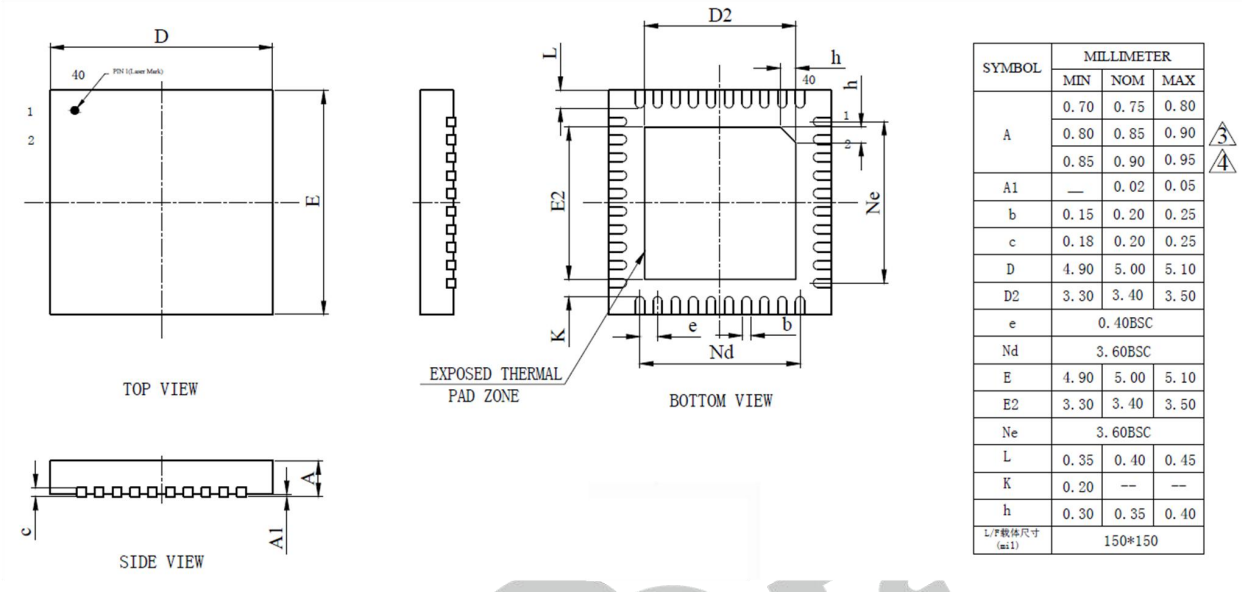
Pin Name	I/O	XR806B	XR806A	Pin Description
HXTAL1	Analog	37	30	24/26/32/40MHz crystal
HXTAL2	Analog	38	31	24/26/32/40MHz crystal
VDD_ANA	Input	39	32	Analog power supply
Programmable I/O				
PA10	In/Out	3	-	Programmable input/output, wakeup io, gpadc in
PA11	In/Out	4	4	Programmable input/output, wakeup io, gpadc in
PA14	In/Out	7	-	Programmable input/output, wakeup io, gpadc in
PA15	In/Out	8	-	Programmable input/output, wakeup io, gpadc in
PA16	In/Out	9	-	Programmable input/output, wakeup io, gpadc in
PA17	In/Out	10	-	Programmable input/output, wakeup io, gpadc in
PA18	In/Out	11	-	Programmable input/output, wakeup io, gpadc in
PA19	In/Out	12	7	Programmable input/output, wakeup io
PA20	In/Out	13	8	Programmable input/output, wakeup io
PA21	In/Out	14	9	Programmable input/output, wakeup io
PA22	In/Out	15	10	Programmable input/output, wakeup io
PA23	In/Out	16	11	Programmable input/output, wakeup io, test strap pin
PB06	In/Out	25	20	Programmable input/output
PB05	In/Out	26	21	Programmable input/output
PB04	In/Out	27	22	Programmable input/output
PB07	In/Out	28	23	Programmable input/output
PB03	In/Out	29	24	Programmable input/output
PB02	In/Out	30	25	Programmable input/output
PA01	In/Out	31	-	Programmable input/output
PA00	In/Out	32	-	Programmable input/output
PB15	In/Out	33	26	Programmable input/output
PB14	In/Out	34	27	Programmable input/output
PB01	In/Out	35	28	Programmable input/output
PB00	In/Out	36	29	Programmable input/output
Wi-Fi Radio Interface				
ANT	Analog	40	1	RF Antenna

NOTE

1. LXTAL1 is reused as PA12 which is a programble input/output IO ,wakeup io or gpadc in;
2. LXTAL2 is reused as PA13 which is a programble input/output IO ,wakeup io or gpadc in;

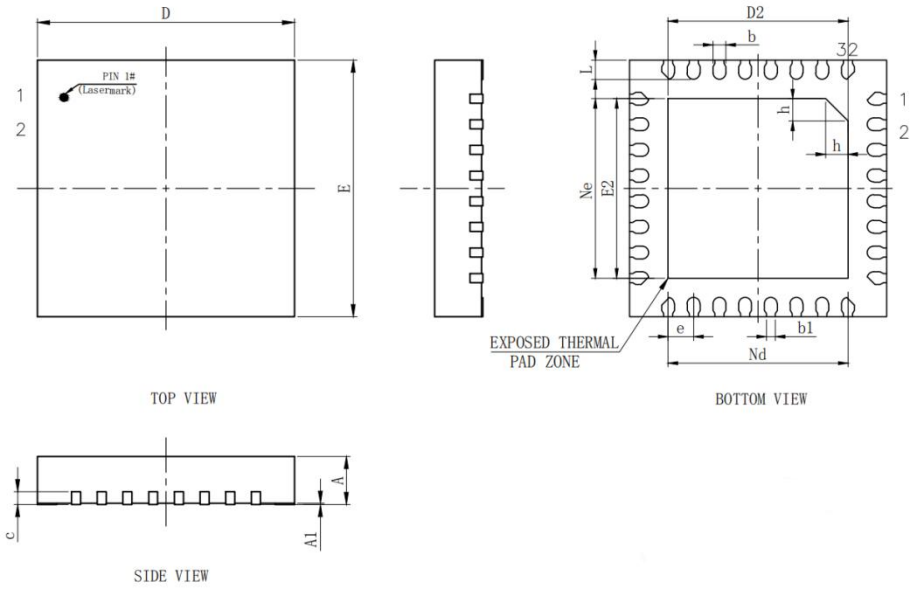
5.3 Package Information

Figure 5- 4 QFN40 Package Outline Drawing



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	3
	0.85	0.90	0.95	4
A1	—	0.02	0.05	
b	0.15	0.20	0.25	
c	0.18	0.20	0.25	
D	4.90	5.00	5.10	
D2	3.30	3.40	3.50	
e	0.40BSC			
Nd	3.60BSC			
E	4.90	5.00	5.10	
E2	3.30	3.40	3.50	
Ne	3.60BSC			
L	0.35	0.40	0.45	
K	0.20	--	--	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	150*150			

Figure 5- 5 QFN32 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122X122		

5.4 Package Thermal Characteristics

Table 5- 2 QFN40 Package Thermal Characteristics

Symbol	Parameter	Conditions	Typ.	Unit
Θ_{JA}	Junction-to-Ambient	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	28	°C /W
Θ_{JB}	Junction-to-Board	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	8.5	°C /W
Θ_{JC}	Junction-to-Case	JESD51	9.2	°C /W

Symbol	Parameter	Conditions	Typ.	Unit
		76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow		

Table 5- 3 QFN32 Package Thermal Characteristics

Symbol	Parameter	Conditions	Typ.	Unit
Θ_{JA}	Junction-to-Ambient	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	32.1	°C /W
Θ_{JB}	Junction-to-Board	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	10.0	°C /W
Θ_{JC}	Junction-to-Case	JESD51 76.2 x 114.3mm, 4-layer(2s2p) PCB No air flow	12.5	°C /W

6 Carrier Information

Table 6- 1 Reel Carrier Information

Item	Color	Size
Reel	Blue	13 inches
Aluminum foil bags	Silvery white	450mm x 375mm x 0.14mm
Inside Box	White	336mm x 336mm x 48mm
Outside Box	White	423mm x 358mm x 365mm

Figure 6- 1 Tape Dimension Drawing

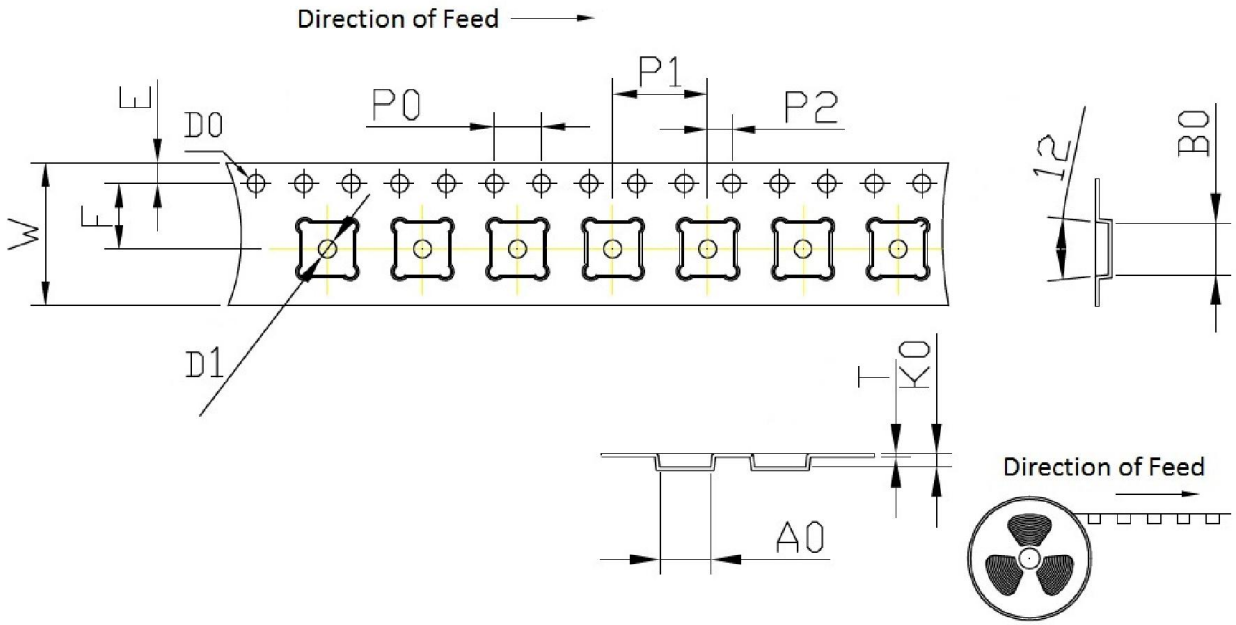


Table 6- 2 Reel Carrier Information

Device	W(mm)	A0(mm)	B0(mm)	K0(mm)	P0(mm)	P1(mm)
XR806B	12±0.30	5.30±0.1	5.30±0.1	$0.85^{+0.01}_{-0.05}$	4.0±0.1	8.00±0.1
XR806A	12±0.30	4.30±0.1	4.30±0.1	$1.10^{+0.05}_{-0.00}$	4.0±0.1	8.00±0.1
Device	**P2(mm)**	**F(mm)**	**E(mm)**	**D0(mm)**	**D1(mm)**	**T(mm)**
XR806B	2.0±0.1	7.5±0.1	1.75±0.1	$1.5^{+0.10}_{-0.00}$	$1.5^{+0.10}_{-0.00}$	0.3±0.05
XR806A	2.0±0.1	5.5±0.1	1.75±0.1	$1.5^{+0.10}_{-0.00}$	$1.5^{+0.10}_{-0.00}$	0.3±0.05

Table 6- 3 Packing Quantity Information

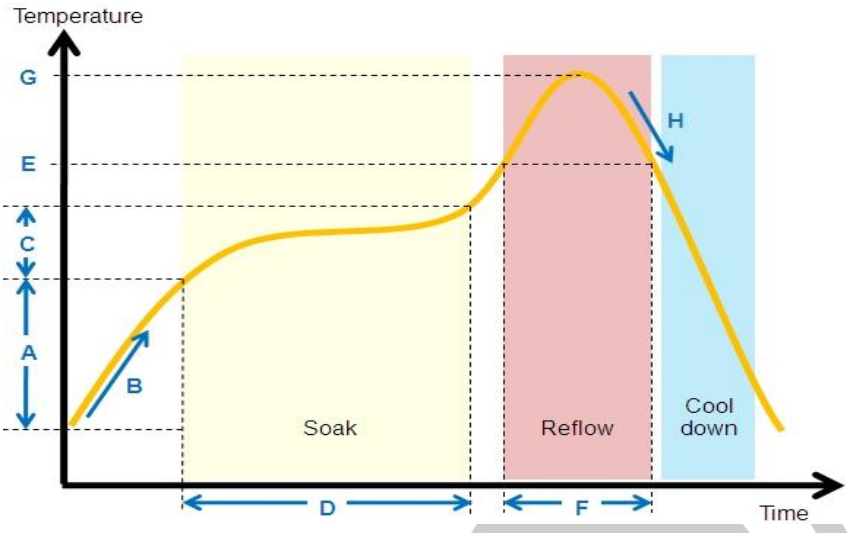
Type	Quantity	Part Number
Tape Reel	3000pcs	XR806B
Tape Reel	3000pcs	XR806A

7 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

Figure 7-1 shows the typical reflow profile of XR806 device sample.

Figure 7- 1 Typical Reflow Profile



Reflow profile conditions of XR806 device sample is given in Table 7-1.

Table 7- 1 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C-> 150 °C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150 °C-> 190 °C
D	Soak time	80~110 sec
E	Liquidus temperature	217 °C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250 °C
H	Cool down temperature rate	≤ 4 °C/sec

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