AXP717 Single Cell NVDC PMU with E-gauge

1 Features

- 3.9V–5.5V Input Operating Range and Support single Cell Battery
- Battery fuel gauge: E-gauge 3.0
- Support TWSI(Two Wire Serial Interface) and RSB(Reduced Serial Bus)
- 3A switch charger, CV accuracy +/-0.5%
- Support USB BC1.2& type C CC input
- High battery discharge efficiency with 30 mΩ
- High integration includes all MOSFETS, current sensing and loop compensation
- Power off current <35uA (BATFET off, RTCLDO output on)
- Ultra low power mode(Green mode)support
- 4 DCDC(DCDC4 is not available in charger mode)
  DCDC1:0.5~1.54V, IMAX=4A
  DCDC2: 0.5~3.4V, IMAX=3A
  DCDC3: 0.5~1.84V, IMAX=1.5A
  DCDC4: 1.0~3.7V, IMAX=3A
- 14 LDOS
  RTCLDO: 1.8V/2.5V/3V/3.3V, 30mA; Support supplied by backup battery (button battery)
  A/B/CLDO: 0.5~3.5V, 0.1V/step
  ALDO2, BLDO1/3, CLDO1/3/4: IMAX=500mA
  ALDO1/4, BLDO4, CLDO2: IMAX=400mA
  ALDO3, BLDO2: IMAX=200mA
  CPUSLDO: for CPUs, 0.5~1.4V, IMAX=30mA, Supplied by DCDC3
- Startup sequence and default voltage of DCDC/LDO setting
- Sleep/Wake up/Fast Wake up support
- Charging LED with breathing function
- Protection
  Input Over-Voltage Protection
  Battery Thermal Sense Hot/Cold Charge Suspend
  Programmable Safety Timer for Charger
  Die Thermal regulation for Charger
  Thermal Shutdown
  DCDC Over-Voltage/Under-Voltage Protection
  LDO Current Limit Protection

2 Applications

- Tablets, E-ink , Smart speaker, Vacuum

3 Description

AXP717 is a highly integrated power management IC (PMIC) targeting at single cell Li-battery(Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

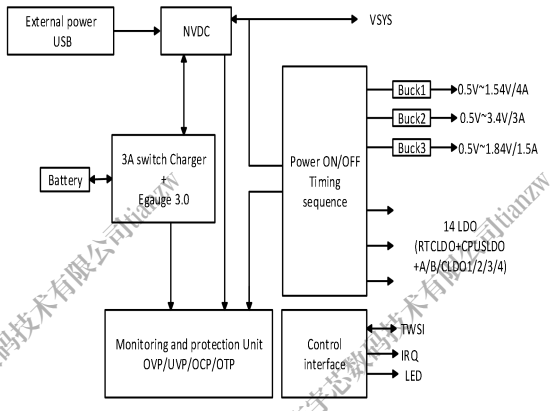
AXP717 supports NVDC switch charge. Besides, it supports 17 channel power outputs which include 3 channels DC-DC and 14 channels LDO. To ensure the security and stability of the system, AXP717 provides multiple channels 14-bit ADC for voltage/temperature monitor and integrates protection circuits such as over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP). Moreover, AXP717 features a unique E-Gauge™ (Fuel Gauge) system, making power gauge easy and exact.

AXP717 supports TWSI and RSB for system to dynamically adjust output voltages, charge current and configure interrupt condition

Device Information

Part Number	Package	Body Size
AXP717	QFN-52	6mm * 6mm

Simplified Application Diagram



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Revision History

Revision	Date	Author	Description
1.0	May 13, 2021	AWA 1017	Initial version
1.1	Jan. 11, 2022	AWA 1017	Update IMAX of ALDO2/ BLDO1/BLDO3/CLDO1/CLDO3/CLDO4

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4 Pin Configuration and Functions

Figure 4-1 Pin Map

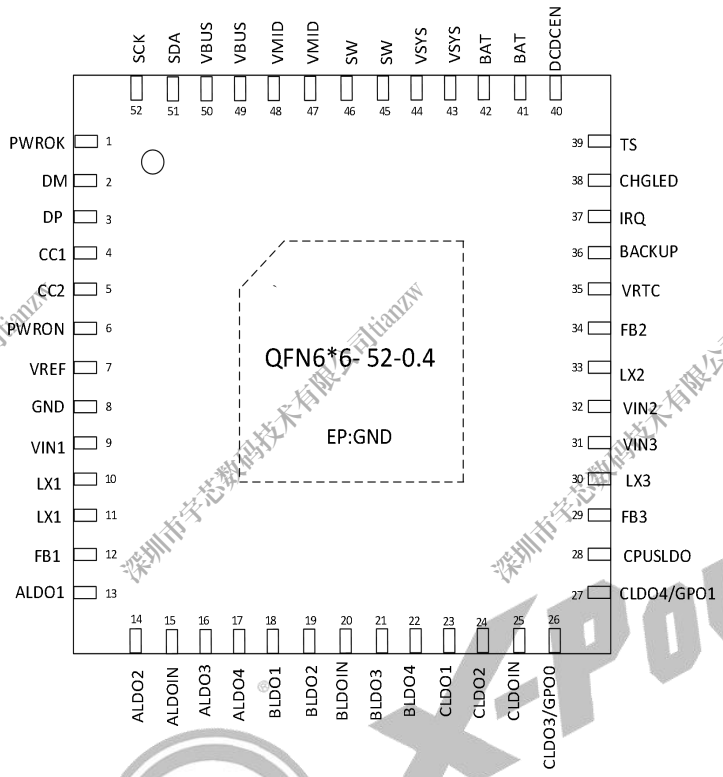

Table 4-1 Pin Description

NO.	Pin Name	I/O(1)	Description
1	PWROK	DIO	Power good indication output
2	DM	DIO	BC1.2 detection, connect to DM of USB connector
3	DP	DIO	BC1.2 detection, connect to DP of USB connector
4	CC1	DIO	Type-C cc logic, connect to CC1 of USB connector
5	CC2	DIO	Type-C cc logic, connect to CC2 of USB connector
6	PWRON	DIO	Power On-Off key input, Internal pulled up.
7	VREF	P	Internal reference voltage
8	GND	G	GND for internal analog circuit
9	VIN1	PI	DCDC1 input source
10/11	LX1	PIO	Inductor pin for DCDC1
12	FB1	AI	DCDC1 feedback pin

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13	ALDO1	PO	Output pin of ALDO1
14	ALDO2	PO	Output pin of ALDO2
15	ALDOIN	PI	ALDO input source, connected to VSYS
16	ALDO3	PO	Output pin of ALDO3
17	ALDO4	PO	Output pin of ALDO4
18	BLDO1	PO	Output pin of BLDO1
19	BLDO2	PO	Output pin of BLDO2
20	BLDOIN	PI	BLDO input source, connected to VSYS or DCDC output
21	BLDO3	PO	Output pin of BLDO3
22	BLDO4	PO	Output pin of BLDO4
23	CLDO1	PO	Output pin of CLDO1
24	CLDO2	PO	Output pin of CLDO2
25	CLDOIN	PI	CLDO input source, connected to VSYS or DCDC output
26	CLDO3/GPO0	PO	Output pin of CLDO3 or GPO0(open drain)
27	CLDO4/GPO1	PO	Output pin of CLDO4 or GPO1(push pull)
28	CPUSLDO	PO	Output pin of CPUSLDO
29	FB3	AI	DCDC3 feedback pin
30	LX3	PIO	Inductor pin for DCDC3
31	VIN3	PI	DCDC3 input source
32	VIN2	PI	DCDC2 input source
33	LX2	PIO	Inductor pin for DCDC2
34	FB2	AI	DCDC2 feedback pin
35	VRTC	PO	RTC power output
36	BACKUP	P	Input pin of backup battery.
37	IRQ	DIO	IRQ output. Connect the IRQ to a logic rail via a resistor. The IRQ pin sends a low level signal to host to report device status and fault.
38	CHGLED	DO	Charge status output to indicate various charger operation. In no battery mode, CHGLED pin can be the feedback pin of DCDC4
39	TS	AI	Battery Temperature Sensor Input
40	DCDCEN	DO	Be connected to external DCDC enable pin. The start-up sequence of DCDCEN is the same as that of CLDO2. High level available, internal pulled up to RTCLDO.

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41/42	BAT	P	Battery connection point
43/44	VSYS	P	System connection point
45/46	SW	P	Switching node connecting to output inductor
47/48	VMID	P	VMID Power output
49/50	VBUS	P	VBUS input
51	SDA	DIO	Data pin for serial interface.
52	SCK	DI	Clock pin for serial interface.

(1)**O** for output, **I** for input, **IO** for input/output, **D** for digital, **A** for analog, **P** for power, and **G** for ground.

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5 Specifications

5.1 Absolute Maximum Ratings (1)

Over operating free-air temperature range (unless otherwise noted)

Table 5-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBUS	Voltage range(with respect to GND)	-0.3	12	V
Others pin (exp VBUS,EP, GND)		-0.3	7	V
		-0.3	7	V
EP to GND		-0.3	0.3	V
T_a	Operating Temperature Range	-40	85	℃
T_J	Junction Temperature Range	-40	125	℃
T_s	Storage Temperature Range	-40	150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)		300	℃

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

Table 5-2 ESD Ratings

		VALUE	UNIT
VESD	Human body model(HBM)(1)	±2000	V
	Charged device model(CDM)(2)	±750	V

(1) Reference: ESDA/JEDEC JS-001-2017.

(2) Reference: ESDA/JEDEC JS-002-2018.

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5.3 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN	Input voltage(VBUS)	3.9	5.5	V
VBAT	Battery voltage		4.4	V

5.4 Thermal Information

Table 5-4 Thermal Information

Thermal Metric(1)		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	24.43	°C/W
θ_{JB}	Junction-to-board thermal resistance	3.26	
θ_{JC}	Junction-to-case(top) thermal resistance	11.91	

(1)Thermal metrics are calculated refer to JEDEC document JESD51.

5.5 Electrical Characteristics

Table 5-5 Electrical Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current in different cases.	no VBUS, BATFET Disabled, with only RTCLDO on;		35		uA
		no VBUS, BATFET enabled, PMIC is power on, all DCDC/ ALDO/ BLDO/ CLDO is off		300		uA
		no VBUS, PMIC is work in green mode.		100		uA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		5.5	V
V_{VBUS_UVLOZ}	VBUS under voltage threshold		3.5		3.9	V

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V_{SLEEPZ}	Sleep mode rising threshold(VBUS-VBAT)			150		mV
V_{VBUS_OV}	VBUS over-voltage rising threshold			7		V
V_{BAT_UVLO}	VBAT under voltage threshold			2.3		V
V_{BAT_UVLOZ}	VBAT under voltage hysteresis			2.45		V
V_{OFF}	VSYS power off threshold		2.6		3.3	V
V_{OFF_HYST}	VSYS power off hysteresis			0.3		V
V_{SYS_OVP}	VSYS over-voltage turn-off		5.8		6	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature rising		145		℃
T_{SHUT_HYS}	Thermal Shutdown Hysteresis	Temperature falling		20		℃
Battery Charger						
V_{BATREG_RANGE}	Typical Charge voltage range	V_{BATREG}=4.0/4.1/4.2/4.35/4.4V	4		4.4	V
V_{BATREG}	Charge voltage resolution accuracy	V_{BAT} = 4.2V, TJ = 25℃	-0.50%		0.50%	
$I_{CHG\_REG\_RANGE}$	Typical Fast charge current regulation range		0		3072	mA
$I_{CHG\_REG\_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.2V or 3.8V, I_{CHG}=1024mA,T_J = 25℃	-20%		20%	
$V_{BATLOWV}$	Battery low voltage threshold	Fast charge to precharge		3		V
I_{PRECHG_RANGE}	Precharge current range		64		1024	mA
I_{PRECHG_ACC}	Precharge current accuracy	V_{BAT}=2.5V, I_{PRECHG} = 256mA, T_J = 25℃	-30%		30%	
I_{TERM_RANGE}	Termination current range		64		1024	mA
V_{TRICHG}	Battery trickle charge threshold	V_{BAT} falling		2		V
I_{TRICHG}	Battery trickle charge current	V_{BAT} < 2 V		10		mA
V_{RECHG}	Recharge Threshold below VBATREG	V_{BAT} falling		100		mV

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FSW	PWM Switching Frequency			1.5		MHz
POWER-PATH MANAGEMENT						
V_{SYS}	Typical system regulation voltage	Isys = 0A, V_{BAT}> VS_{YS_MIN}, BATFET Disabled		V_{BAT}+ 50mV		V
		Isys= 0A, V_{BAT}<V_{SYS_MIN}, BATFET Disabled		V_{SYS_MIN}+ 150mV		V
V_{SYS_MIN}	Minimum DC System Voltage Output	V_{BAT}< V_{SYS_MIN}, SYS_MIN = 3.5V , ISYS= 0A		3.65		V
Input Voltage / Current Regulation						
V_{INDPM_RANGE}	Typical Input voltage regulation range		3.88		5.08	V
V_{INDPM_ACC}	Input voltage regulation accuracy	V_{INDPM}=4.36V	-3%		3%	
I_{INDPM_RANGE}	Input current regulation range		100		3250	mA
I_{INDPM_ACC}	Input current regulation accuracy	I_{INLIM} =500mA	450		550	mA
BAT OVER-VOLTAGE						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104%* V_{BAT_REG}		V
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
DCDC						
DCDC1/2/3						
V_{IN}	Input Voltage		2.6		5.5	V
UVP				85%		
OVP				130%		
FSW	Switching Frequency			3		MHz
Accuracy	Output Accuracy	Accuracy, PWM mode, V_{OUT}<1V	-30		30	mV
		Accuracy, PWM mode, V_{OUT}>1V	-3.00%		3.00%	
DCDC1						
V_{OUT}	Output Voltage	Output Range	0.5		1.54	V

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		Step Size, V_{OUT}=0.5V~1.2V		10		mV
		Step Size, V_{OUT}=1.22V~1.54V		20		mV
I_{OUT}	Output Load Current			4		A
DCDC2						
V_{OUT}	Output Voltage	Output Range	0.5		3.4	V
		Step Size, V_{OUT}=0.5V~1.2V		10		mV
		Step Size, V_{OUT}=1.22V~1.54V		20		mV
		Step Size, V_{OUT}=1.6~3.4V		100		mV
I_{OUT}	Output Load Current			3		A
DCDC3						
V_{OUT}	Output Voltage	Output Range	0.5		1.84	V
		Step Size, V_{OUT}=0.5V~1.2V		10		mV
		Step Size, V_{OUT}=1.22V~1.84V		20		mV
I_{OUT}	Output Load Current			1.5		A
DCDC4						
V_{OUT}	Output Voltage	Output Range	1.0		3.7	V
		Step Size		100		mV
I_{OUT}	Output Load Current			3		A
LDO						
RTCLDO						
V_{OUT}	Output Voltage		1.8		3.3	V
	Output voltage accuracy		-10%		+10%	
I_{OUT}	Output Load Current			30		mA
CPUSLDO						
VIN	Input Voltage	Input is DCDC3	0.8		1.84	V
V_{OUT}	Output Voltage	Output Range	0.5		1.4	V
		Step size		50		mV
		Accuracy,VIN=0.8V~1.84V, V_{OUT}<1V, I_{load}=10mA	-30		30	mV
		Accuracy,VIN=0.8V~1.84V,	-3%		3%	

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		V_{OUT}>1V, I_{load}=10mA				
I_{OUT}	Output Load Current			30		mA
ILIM	Current Limit			300		mA
ALDO/BLDO/CLDO 1~4						
VIN	Input Voltage		2.6		5.5	V
V_{Drop}	Dropout	V_{OUT}=3.3V		200		mV
V_{OUT}	Output Voltage	Output Range	0.5		3.5	V
		Step size		100		mV
		Accuracy, ALDOIN=2.6V~5.5V, V_{OUT}<1V, I_{load}=10mA only for ALDO3/4	-20		20	mV
		Accuracy, ALDOIN=2.6V~5.5V, V_{OUT}>1V, I_{load}=10mA only for ALDO3/4	-2%		2%	
		Accuracy, xLDOIN=2.6V~5.5V, V_{OUT}<1V, I_{load}=10mA	-30		30	mV
		Accuracy,xLDOIN=2.6V~5.5V, V_{OUT}>1V, I_{load}=10mA	-3%		3%	
I_{OUT}	Output Load Current	ALDO2, BLDO1/3, CLDO1/3/4		500		mA
		ALDO1/4, BLDO4, CLDO2		400		mA
		ALDO3, BLDO2		200		mA
ILIM	Current Limit			500		mA
BOOST						
$V_{BST\_REG\_RANGE}$	Typical Boost mode regulation voltage range		4.55		5.51	V
$V_{BST\_REG\_STEP}$	Typical Boost Mode Regulation voltage step			64		mV
$V_{BST\_REG\_ACC}$	Boost mode regulation voltage accuracy	V_{BST}=5.126V	-3%		3%	
$V_{BST\_BAT\_LOWV}$	Battery voltage exiting boost mode	BAT falling	2.4	2.6	3.0	V
I_{BST}	Boost mode output current range				1.5	A

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V_{BST_OVP}	Boost mode over-voltage threshold	Rising threshold	5.8		6.4	V
$V_{BST\_OVP\_HYS}$	Boost mode over-voltage threshold hysteresis	Falling threshold	100		300	mV
FSW	PWM Switching Frequency, and digital clock	Oscillator frequency		1.5		MHz
TWI&IO						
TWI INTERFACE (SCL, SDA)						
VIH	Input high threshold level, SCL and SDA	Pull-up rail 1.8V	1.3			V
VIL	Input low threshold level	Pull-up rail 1.8V			0.8	V
VOL	Output low threshold level	Sink Current = 5mA, sink current			0.4	V
Logic I/O pin Characteristics (IRQ/PWRON/PWROK)						
VIH	Input high threshold level		1.3			V
VIL	Input low threshold level				0.8	V

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6 Detail Description

6.1 Overview

AXP717 is a highly integrated power management IC(PMIC) targeting at single cell Li-battery (Li-ion or Li-polymer) applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

AXP717 supports 3A switch charger. Besides, it supports 17 channel power outputs which include 3 channel DCDCs and 14 channel LDOs. To ensure the security and stability of the system, AXP717 provides multiple channels 14-bit ADC for voltage/temperature monitor and integrates protection circuits such as over-voltage protection(OVP), over-current protection(OCP) and over-temperature protection(OTP). Moreover, AXP717 features a unique E-Gauge™ (Fuel Gauge) system, making power gauge easy and exact.

AXP717 supports TWSI and RSB for system to dynamically adjust output voltages, charge current and configure interrupt condition.

AXP717 is available in 6mm x 6mm 52-pin QFN package.

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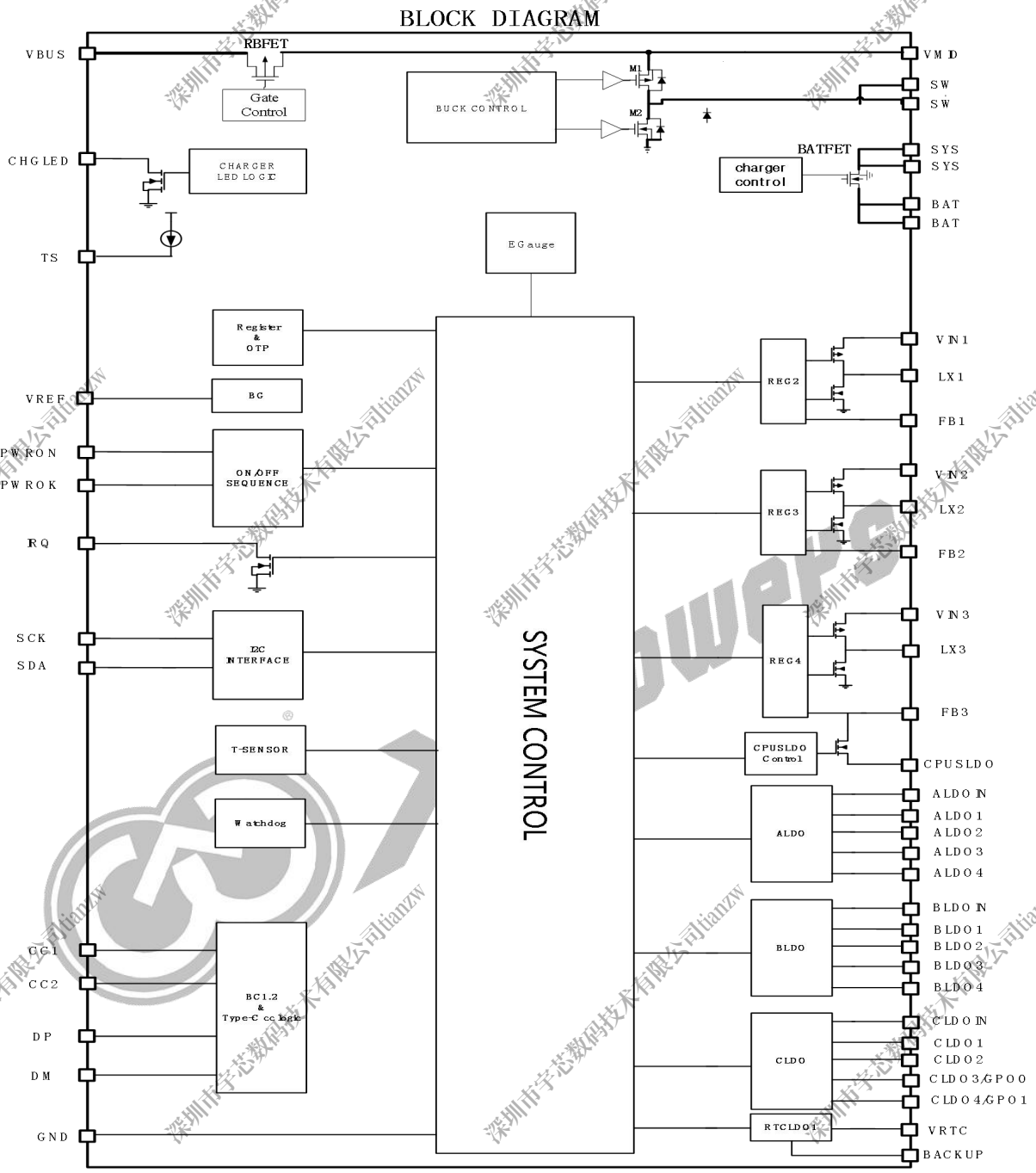
6.2 Function Block Diagram



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6.3 Serial Interface Communication

AXP717 supports TWSI protocol and performs as a TWSI slave device with default address 0x68/0x69(8 bits). When AXP717 powers on, SCK/SDA pin of TWSI will be pulled up to IO Power and then Host can adjust and monitor AXP717 with rich feedback information.

Besides, AXP717 supports RSB for Allwinner platform with address 0x01D1 or 0x0273 by customer.

Note: “Host” here refers to processor.

6.4 Power Path

VBUS as the charger input, connecting to VSYS pin through a switch charger, provides power to system and charges battery through BATFET. Charge current can be adjusted automatically according to the feedback current which is detected with an internal resistor.

The device provides automatic power path selection for system from VBUS, battery or both. When battery voltage is above VSYS, BATFET is turned on and AXP717 enters supplement mode. If an adapter is not inserted, system current is provided only by battery. At this time, BATFET is at fully on state.

6.5 Power On/Off and reset

6.5.1 Power on reset(POR)

AXP717 is powered from the higher voltage between VBUS and BAT. When VBUS voltage(V_{VBUS}) is higher than V_{VBUS_UVLOZ} or BAT voltage(V_{BAT}) is higher than V_{BAT_UVLOZ}, the device is POR, and all registers are reset to the default value.

6.5.2 Power up from BAT

If only battery is present and V_{BAT} is higher than UVLO threshold , BATFET(connecting battery to system) is off by default and need to be turned on by pressing the PWRON key or inserting an adapter. Serial Interface communication is not available before power on.

6.5.3 Power up from VBUS

When VBUS is inserted and V_{VBUS} is higher than V_{VBUS_UVLOZ}, the VBUS insertion IRQ is sent and the register bit reg49H[7] is set to 1 to indicate VBUS is inserted. Then PMU detects the input source whether it is good or not. If VBUS is good, the RBFET is open and VSYS is working.

6.5.3.1 Good source condition

PMU needs to check the power capability of the input source. Only when the input source meets the following requirements can it start the buck converter.

a. VBUS voltage is lower than V_{ACOV}(typical 7V)

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b. VBUS voltage is higher than $V_{VBUSUVLO}$ when pulling I_{BADBUS}(typical 15mA)

Once the input source meets the requirements above, the register bit reg00H[5](VBUS_GD) is set to 1 to indicate the input source is good.

6.5.3.2 Set input voltage limit(VINDPM)

AXP717 supports wide range of input voltage(3.9V~5.5V). V_{INDPM} can be set through reg16H[3:0]. The range of V_{INDPM} is from 3.88V to 5.08V and the step is 80mV.

When VBUS voltage reaches V_{INDPM}, the charge current will decrease automatically until the current is zero. If I_{SYS} is over the input power supply capability, VSYS will drop. If V_{BAT} is above VSYS, PMU will enter the supplement mode.

6.5.3.3 Set input current limit(IINDPM)

AXP717 supports input current limit to avoid adaptor overload. I_{INDPM} can be set through reg17H[5:0]. The range of I_{INDPM} is from 100mA to 3.25A and the step is 100mA.

When input current reaches I_{INDPM}, the charge current will decrease automatically until the current is zero. If I_{SYS} is over the input power supply capability, VSYS will drop. If V_{BAT} is above VSYS, PMU will enter the supplement mode.

6.5.4 System power on/off management

PMU has power off and power on status. When at off state, all voltage outputs are turned off except RTCLDO.

6.5.4.1 Power on-off Key (POK)

EN/PWRON pin can be customized as PWRON pin or EN pin. The default is PWRON pin. The Power on-off Key (POK) can be connected between PWRON pin and GND of AXP717. AXP717 can automatically identify the four status (Long-press, Short-press, Negative edge, Positive edge) and then correspond respectively.

6.5.4.2 Power on

1.When EN/PWRON pin is customized as PWRON pin, power on sources include:

(1). POK. AXP717 can be powered on by pressing and holding POK for a period of time that longer than “ONLEVEL”.

(2). VBUS low to high. The function can be configured by customization.

(3). VBAT low to high. The function can be configured by customization.

(4). IRQ Low level. IRQ pin is low level for more than 16ms, AXP717 will be powered on.The function can be configured by customization.

(5). Battery is charged to normal(VBAT>3.3V and is charging). The function can be configured by customization.

2.When EN/PWRON pin is customized as EN pin, AXP717 can be powered on by EN pin from low to high(0.6V).

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After power on, DCDCs and LDOs will be soft booted in preset timing sequence. If IRQ low level is the power on source, AXP717 can be configured for fast power on by REG2FH [5], and the DCDCs/LDOs start sequence can be configured by REG2BH~REG2FH.

6.5.4.3 Power Off

1.When EN/PWRON pin is customized as PWRON pin, power off sources include:

(1). POK. AXP717 can be powered off by pressing and holding POK for a period of time that longer than "OFFLEVEL". The function can be configured by REG22H [1] and REG22H [0] decides whether the PMU auto turns on or not when it shuts down after OFFLEVEL POK.

(2). Write "1" to REG27H [0].

(3). VSYSGOOD high to low. When VSYS<VOFF or VBUS>7V, AXP717 will be powered off. The default of VOFF is 2.6V which can be configured by REG24H [6:4].

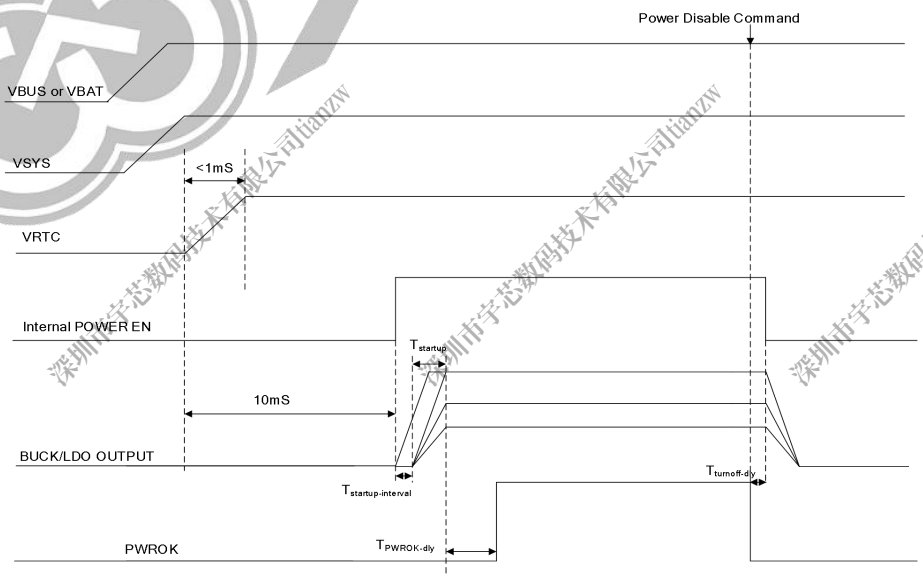
(4). The output voltage of DCDC is 15% lower than the setting value. The function can be configured by REG23H [3:0].

(5). The output voltage of DCDC is much larger than their setting(130%). The function can be configured by REG23H [4].

(6). Die temperature is over the warning level2(145℃). The function can be configured by REG22H [2].

(7). LDO over current(typical 500mA for ALDO/BLDO/CLDO). The function can be configured by REG22H [3].

Figure 6-1 System power up and shut down sequence



6.5.4.4 Sleep and wakeup

When the running system needs to enter Sleep mode, maybe one or several power outputs should be disabled or changed to other voltage. Wakeup can be initiated by the following sources:

1. Software wakeup (REG25H [1] is set to 1)

2. IRQ pin wakeup (REG 25H [5] =1 and IRQ pin is low level for more than 4ms)

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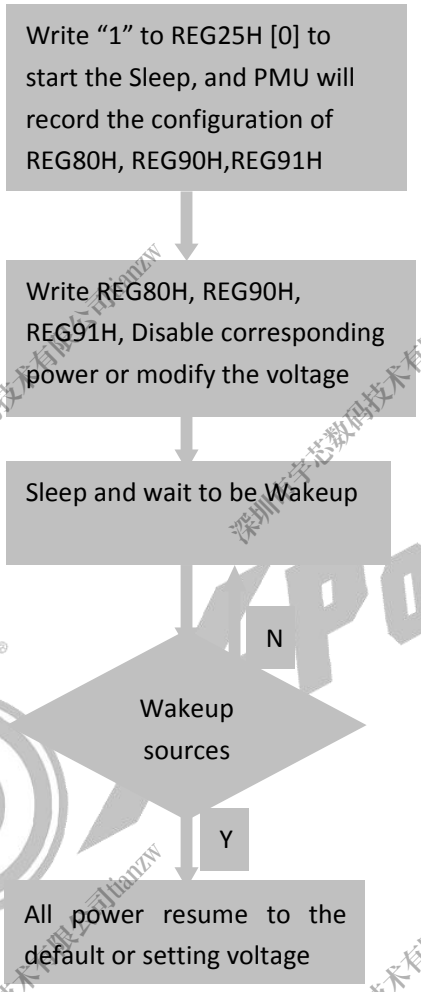
These sources will make all the power outputs resume to the default voltage or the setting voltage, which is configured by REG25H[2], and all shutdown powers will resume by the startup sequence.

The control process under sleep and wakeup modes is as below.

Figure 6-2 Sleep and Wakeup



6.5.4.5 System Reset

System reset means the related registers will be reset when PMU is power off. The system will power off and then power on. VRTC will not be off during restart. Restart can be initiated by the following sources:

(1). PWROK drive low.

The PWROK pin can be used as the reset signal of application system. During AXP717 startup, PWROK outputs low level, which will be pulled up to startup the system after output voltage reaches the regulated value.

When application system works normally, if the PWROK pin is driven low for 128us, the PMU will be restarted. The function can be configured by REG27H [3].

(2). Write “1” to REG27H [1] to restart the PMU.

(3). Watchdog timeout. The function can be configured by REG19H [0] and REG1AH [5:4].

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6.5.4.6 POR

Power on reset means all the registers will be reset when PMU is power down. All voltage outputs are turned off including RTCLDO and VREF. Pressing and holding POK for more than 16s can force POR.

6.5.4.7 Fast power on/Fast Wake up

If fast power on and fast wake up function is enabled by REG3FH, all voltage outputs are turned on based on the timing sequence set by REG28H~REG2BH. The startup interval is 0.4ms.

6.5.4.8 Green mode

AXP717 has ultra-low power mode(Green mode) to support the application such as Elink.

There are two ways to let AXP717 enter to green mode.

(1) Disable all the power rails, and only enable CPUSLDO/DCDC3/BLDO2, then set REG1DH[0] to enable green mode. To exit green mode, host needs to clear REG1D[0].

(2) Set REG25H[0] to enter sleep mode, and configure the power rails on/off in sleep mode. Then set REG2AH[1] and REG25H[6] to let the device enter to both sleep and green mode automatically. In this way, there is a delay time before sleep and green mode taking effect.

In Green mode, the quiescent power consumption is much lower than normal status. However, the voltage output accuracy and capacity is worse. The following table shows the capacity and accuracy of the voltage output.

Table 6-1 The capacity and accuracy in Green mode

Output Path	Accuracy	Load Capacity(Max)
CPUSLDO	+-5%	10mA
RTCLDO	+-5%	5mA
DCDC3	+-5%	10mA
BLDO2	+-5%	5mA

6.6 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP717.

Table 6-2 Multi-Power Outputs

Output Path	Type	Default Voltage	Startup Sequence	Application Suggestion	Load Capacity
DCDC1	BUCK	Customization	Customization	CPU	4000mA
DCDC2	BUCK			VSYS/VDD-USB/DRAM	3000mA
DCDC3	BUCK			VCC-DRAM	1500mA

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DCDC4	BUCK			Not available in charger mode	3000mA
ALDO1	LDO			AVDD-CSI	400mA
ALDO2	LDO			IO/AF-CSI VCC-PE	200mA
ALDO3	LDO			VCC-USB/VCC-PL	200mA
ALDO4	LDO			AVCC/PLL/DRAM	400mA
BLDO1	LDO			WIFI	400mA
BLDO2	LDO			LPDDR	200mA
BLDO3	LDO			MOTOR	200mA
BLDO4	LDO			DVDD-CSI	400mA
CLDO1	LDO			MIPI/LVDS.etc	400mA
CLDO2	LDO			CTP	400mA
CLDO3	LDO			VCC-SENSOR/NAND.etc	400mA
CLDO4	LDO			LCD	400mA
VCPUS	LDO			CPUs	30mA
VRTC	LDO		Always on	RTC	30mA

AXP717 includes 4 synchronous step-down DCDCs and 14 LDOs. The work frequency of DC-DC 1/2/3 is 3MHz and DCDC4 is 1.5MHz. External small inductors and capacitors can be connected. In addition, DCDC 1/2/3 can be set in fixed PWM mode or auto mode (automatically switchable according to the load). See register REG81H.

DCDC1/2/3 has DVM enable option. In DVM mode, when there is a change in the output voltage, DCDC will change to the new targeted value step by step. It supports two kinds of DVM slope: 1 step/15.625us and 1step/31.250us. The slope can be chosen by REG82H [0].

AXP717 can configure the default voltage, the startup sequence and other control of all power output.

Startup sequence: The startup sequence has eight levels from 0 to 7. When the sequence is 0, it means the output is booted at the first step. When the sequence code is 1, it means the output is booted at the second step. When the sequence is 7, it means the output is not booted.

Default voltage setting: The default voltage of each channel can be set to each step within the output range.

6.7 Multi-Function Pin Description

EN/PWRON

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EN/PWRON can be customized as EN pin or PWRON PIN. When it is configured as PWRON pin, a Power on-off Key (POK) can be connected between PWRON pin and GND. When it is configured as EN pin, it can be used for dial switch.

CLDO4/GPO1

It can be customized as LDO or GPO. When customized as GPO, it is push-pull. GPO1 output is configured by REG1CH [4].

CLDO3/GPO0

It can be customized as LDO or GPO. When customized as GPO, it is open-drain. GPO0 output is configured by REG1CH [0].

6.8 Charger

6.8.1 Characteristics

- Range of input voltage:3.9V~5.5V, switch charger, supports single cell Li-battery
- Pre-charge current settable ($I_{PRE-CHG}$, reg61H [3:0]), default:128mA, range: 0mA~960mA, step:64mA
- Fast charge current settable (I_{CHG}, reg62H[5:0]), default:1024mA, range: 0mA~3072mA, step:64mA
- Target charge voltage settable (V_{REG}, reg64H[2:0]), default:4.2V, range: 4.0v/4.1v/4.2v/4.35v/4.4v/5.0v
- Termination current settable(Iterm,reg63H[3:0]),default:384mA,range:64~1024,step:64mA
- Accuracy of target voltage:±0.5%(testing ambient temperature:25℃, target voltage:4.2V)

6.8.2 Charging condition

- VBUS is present and available, $V_{VBUS}>V_{BAT}+V_{SLEEPZ}$
- Input source detection finishes (reg00H [5] =1)
- Charging is enabled (reg19H [1] =1)
- Die temperature is lower than T_{SHUT}
- When TS pin is used to detect battery temperature, battery temperature is within the chargeable range
- V_{BAT} is lower than V_{BAT_OVP} and Battery is present
- No charger safety timer fault

6.8.3 Charging process

When PMU meets all charging conditions, it can complete the whole charging process without the participation of Host. The charging status can be known from the register bits reg01H[2:0]. The default values of charging parameters are shown as following. Host can modify registers to optimize the values through TWSI.

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Table 6-3 Default values of charging parameters

Parameter	Default value
Charging voltage	4.2V
Charging current	1.024A
Pre-charging current	128mA
Termination current	320mA
Temperature profile	Cold/hot
Safety timer in fast-charge	12hours

6.8.3.1 Pre-charge

When V_{BAT} is lower than $V_{BATLOWV}$(3V), the charger is under pre-charge mode where charging current is limited to a value of $I_{PRE-CHG}$. Safety time in pre-charge is 50 minutes. If pre-charge process times out, PMU will stop charging and send a corresponding IRQ to Host. The function of safety timer can be disabled through reg67H [2].

6.8.3.2 Constant current charge

Once V_{BAT} is higher than $V_{BATLOWV}$ and lower than V_{REG}, the charger is under constant current charge mode. It will charge with constant current I_{CHG}.

6.8.3.3 Constant voltage charge

When V_{BAT} reaches target voltage (V_{REG}), the charger enters constant voltage charge mode. In this stage, the charger keeps the output voltage constant and step down charging current gradually, in order to fully charge battery.

When V_{BAT} is above V_{RECHG} and the charging current reduces under termination current (I_{TERM}), AXP717 reports charger done, stops charging (charger enable bit is still 1) and turns off BATFET. Meanwhile, IRQ is sent to Host.

When AXP717 is in regulation of input current(IDPM), input voltage(VDPM) or temperature(thermal regulation), the function of charging termination configured through reg63 H[4] is temporarily disabled and the speed of safety timer slows down. Whether to set safety timer during DPM or thermal regulation depends on reg67H [7].

6.8.3.4 Re-charge

After charge done, if V_{BAT} falls below V_{RECHG}, PMU will automatically enable charger without reinserting adapter.

No matter whether V_{BAT} is above V_{RECHG} or not, the charger is enabled when an adapter is inserted.

6.8.3.5 Battery detection

As long as an AC adapter is present and usable, battery detection will be enabled to detect whether battery is connected. Battery detection function is enabled by default and can be disabled through reg68H [0]. If the function is disabled, PMU considers that battery is always present. The detection result is saved in reg00H [3]

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6.8.4 Charging protection

6.8.4.1 charger safety timer

Once starting pre-charge mode, PMU will enable timer1. If PMU cannot enter constant current charge mode from pre-charge within 50 minutes, PMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

When the charger enters into constant current charge mode, PMU will enable timer2. If PMU cannot finish the whole charge cycle within 12 hours, PMU will enter battery safe mode and send IRQ to indicate the battery may be damaged.

6.8.4.2 Battery safe mode

In battery safe mode, the charger always charges with 10mA current. PMU can quit battery safe mode with one of the following methods:

- $V_{BAT}>V_{RECHG}$
- Adapter removal
- Charger enable bit (reg18H [1]) is reset to 1
- Safety timer1 enable bit(reg67H [2]) or safety timer2 enable bit(reg67H [6]) is reset to 1

6.8.4.3 PMU die temperature protection

AXP717 has built-in temperature protection function through ADC to monitor internal temperature.

Under charging mode, the temperature point of thermal regulation can be set through reg65H[1:0]. When die temperature rises up to the setting point, the charging current will be decreased to decrease heat. When thermal regulation works, actual charge current is lower than the setting value and thermal regulation status(reg00H [1]) is set to 1. If die temperature rises up to T_{SHUT} (145℃), IRQ is sent and PMU is power off. When die temperature falls below hysteretic threshold (120℃), PMU is not power on automatically.

6.8.4.4 Battery temperature protection

AXP717 can monitor battery temperature, when TS pin is used to detect battery temperature and parallel with charger(reg50H[4]=0). The battery temperature sensitive resistor is connected between TS pin and GND. The suggestion resistance should be 10Kohm at 25℃ ambient temperature. Through TS pin, PMU outputs constant current which can set through reg50H [1:0] to adapt different resistance. When the resistance is 10Kohm, the current should be set to 50uA. The enable bit of TS current source is configured through reg50H [3:2]. When current passes through the temperature sensitive resistor, PMU gets a detected voltage and calculates its value through ADC circuit. Take for example, TH11-3H103F temperature sensitive resistor of Mitsubishi Company. Using 50uA current source, the relationship among temperature, equivalent resistance, detected voltage and ADC data is as following.

Table 6-4 Relationship among temperature, equivalent resistance, detected voltage and ADC data

Temperature	equivalent resistance	detected voltage	ADC DATA

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-20℃	63.00Kohm	3.150V	189Ch
-15℃	50.15Hohm	2.508V	1398h
-10℃	40.26Kohm	2.013V	FBAh
-5℃	32.55Kohm	1.628V	CB8h
0℃	26.49Kohm	1.325V	A5Ah
5℃	21.68Kohm	1.084V	878h
10℃	17.78Kohm	0.889V	6F2h
15℃	14.63Kohm	0.732V	5B8h
20℃	12.07Kohm	0.604V	4B8h
25℃	10.00Kohm	0.500V	3E8h
30℃	8.320Kohm	0.416V	340h
35℃	6.954Kohm	0.348V	2B8h
40℃	5.839Kohm	0.292V	248h
45℃	4.924Kohm	0.246V	1ECh
50℃	4.171Kohm	0.209V	1A2h
55℃	3.549Kohm	0.177V	162h
60℃	3.032Kohm	0.152V	130h

During battery charging process, if TS pin voltage is lower than VHTF-CHG or higher than VLTF-CHG (VHTF-CHG and VLTF-CHG can be set through reg55H and reg54H. The default value of VLTF-CHG is set around 0℃ and VHTF-CHG around 45℃), which indicates battery temperature is too high or too low, then the charger is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the charger will recovery automatically.

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During battery discharging mode, if TS pin voltage is lower than VHTF-WORK or higher than VLTF-WORK (VHTF-WORK and VLTF-WORK can be set through reg57H and reg56H. The default value of VLTF-WORK is set around -10℃ and VHTF-WORK around 55℃), which indicates battery temperature is too high or too low, then the boost is paused and IRQ is sent to notify Host. When battery temperature is back to the normal range, the boost will recovery automatically.

High temperature protection threshold hysteresis for VHTF-CHG and VHTF-WORK can be set through reg53H. Low temperature protection threshold hysteresis for VLTF-CHG and VLTF-WORK can be set through reg52H. The range of temperature detection can be expanded by adding more resistors.

Some battery may have no temperature sensitive resistor. Under this situation, TS pin can be pulled down to GND with a 10Kohm resistor externally or set as external input of ADC through register.

6.8.5 Charging indication

CHGLED pin uses open-drain/push-pull output method. It is internally pulled up to LDO. Its output drive capability is above 10mA. Detail function control is shown as the following table.

Table 6-5 CHGLED function

REG70H [2:0] = 000 (Type A CHGLED) Open Drain	Hi-Z	No charging(conditions are not met or battery charged)
	25% 1Hz pull low/Hi-Z jump	Charger internal abnormal alarm(including timer out、die temperature over temperature、battery temperature out of charging range)
	25% 4Hz pull low/Hi-Z jump	Input source or battery over voltage
	Pull low	Charging
REG70H [2:0] = 001 (Type B CHGLED) Open Drain	Hi-Z	No VBUS, and power supply by battery
	25% 1Hz pull low/Hi-Z jump	Charging
	25% 4Hz pull low/Hi-Z jump	Alarm, including input source or battery over voltage, battery temperature out of charging range, timer out ,die temperature over temperature
	Pull low	No battery or charge finished, and power supply by VBUS
REG70H[2:0]=010 Breathing LED	Breathing LED controlled by charger(Breathing LED on in charging status)	
REG70H[2:0]=011	Breathing LED controlled by REG70H[6]	

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Breathing LED	
REG70H[2:0]=110 CFG CHGLED	The output status is controlled by REG70H[5:4]

Note: 1. LED is on when CHGLED pin is low. 2.Breathing LED display behavior controlled by REG72H~REG78H

6.8.6 DCDC4 mode

AXP717 works in charger mode by default to support single-cell applicaiton. If it is used in multi-cell or non-battery application, the charger module can be used as DCDC4. In DCDC4 mode, charger module works as a common buck, and CHGLED pin works as the feedback of DCDC4. In order to support multi-cell gauge, gauge will measure the battery voltage by external resistor divider from DP pin instead of VBAT pin. In DCDC4 mode, charging indication/battery detection/USB typeC/BC1.2 function is not available. User can select DCDC4 or charger mode by customization.

6.9 BOOST

AXP717 supports boost converter operation to deliver battery power to VBUS or VMID. The maximum output current support 1.5A. If below conditions are valid, boost will be enabled,

(1)V_{BAT} is higher than boost mode disable threshold(REG1EH[3:2], default is 2.6V)

(2)VBUS voltage is lower than VBAT+V_{SLEEP}

(3)Boost mode is enabled(REG19H[4]=1)

(4)Voltage at TS pin is within working range (REG56H/57H)

6.10 BATFET

BATFET connects system and battery. The on-resistance is low to 30mohm. The minimum system voltage is set by REG15H[2:0]. When battery voltage is below minimum system voltage, the BATFET operates in linear mode and system voltage is regulated at minimum system voltage setting. As the battery voltage rises, the BATFET can turn to full on.

If only battery is present , BATFET is off when the system is power off and can be turned on again by pressing the PWRON key or inserting an adapter.

6.11 RBFET

RBFET connects VMID and VBUS. The on-resistance is low to 100mOhm. It supports input and output current limit function. In boost mode, the output current limit value of RBFET is set through reg1EH [1:0].

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6.12 ADC

AXP717 has a low speed 14 Bits SAR ADC for measuring BAT voltage, VBUS voltage, VSYS voltage, TS voltage and die temperature.

Table 6-6 ADC channel

No.	Channel function	000H	001H	002H	…	FFFH
0	BAT voltage	0mV	1mV	2mV	…	8.192V
1	VBUS voltage	0mV	1mV	2mV	…	8.192V
2	VSYS voltage	0mV	1mV	2mV	…	8.192V
3	TS voltage	0mV	0.5mV	1mV	…	4.096V
4	die temperature	0mV	0.1mV	2mV	…	0.8192V

Note: ADC data is 14 bits. In order to get the complete data, TWSI must read the high 6 bits firstly and then the low 8 bits.

6.13 E-Gauge

The Fuel Gauge system is able to export information about battery capacity percentage (regA4H) and Battery Voltage (regC4H, regC5H). The Fuel Gauge can be enabled or disabled through reg0BH[2]. The Battery low warning level can be set through reg1BH, and IRQ will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set through reg1BH.

Once a default battery is selected for a particular design, it is highly recommended to program the battery module to achieve better Fuel Gauge accuracy. Once the battery module data are available, user can write these information to battery parameter (REGA1H) after brom is enabled on each boot. Additionally, the Fuel Gauge system is capable to learn the battery characteristic automatically.

6.14 IRQ /BACKUP

6.14.1 IRQ

AXP717 has an IRQ pin which is used to indicate whether there interrupt events occur.

PMU Interrupt Controller monitors the trigger events such as over voltage, over current, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enabled bits are set to 1 (Refer to registers

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reg40H~44H), corresponding IRQ status will be set to 1 (Refer to registers reg48H~4CH), and IRQ pin will be pulled down. When Host detects triggered IRQ signal, Host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing “1” to status bit.

6.14.2 BACKUP

AXP717 has a backup pin which is used to connect backup battery. It is the source of RTCLDO when PMU has only backup battery.

When PMU is power on, the backup battery also can be charged by configuring reg19H[3]. The charger is working under linear mode with 100uA charge current and the termination voltage can be configured by reg6AH in range from 2.6V to 3.3V (default 2.9V).

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6.15 Register

6.15.1 Register List

Address	Description	R/W
0X00	PMU status1	R
0X01	PMU status2	R
0X05	BC_detect	R
0X06	ILIM type	R
0X08	PMU fault	RW1C
0X0B	module enable control1	RW
0X10	DCDC/LDO Discharge_configure	RW
0X14	Tshut configure	RW
0X15	Minimum system voltage control	RW
0X16	Input voltage limit control	RW
0X17	Input current limit control	RW
0X18	Reset the fuel gauge	RW
0X19	module enable control2	RW
0X1A	Watch dog control	RW
0X1B	Low Battery warning threshold setting	RW
0X1C	GPO configure	RW
0X1D	Low power configure	RW
0X1E	Boost configure	RW
0X20	PWRON status	R
0X21	PWROFF status	R
0X22	PWROFF_EN	RW
0X23	PWROFF of DCDC OVP/UVP control	RW
0X24	VSYS voltage for PWROFF threshold setting	RW
0X25	Sleep and Wakeup configure	RW
0X26	IRQLEVEL/OFFLEVEL/ONLEVEL setting	RW
0X27	Soft Poweroff configure	RW
0X28	Auto Sleep map0	RW

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Address	Description	R/W
0X29	Auto Sleep map1	RW
0X2A	Auto Sleep map2	RW
0X2B	Fast pwron setting 0	RW
0X2C	Fast pwron setting 1	RW
0X2D	Fast pwron setting 2	RW
0X2E	Fast pwron setting 3	RW
0X2F	Fast pwron setting 4	RW
0X3E	TWI/RSB configure	RW
0X40-0X44	IRQ Enable	RW
0X48-0X4C	IRQ Status	RW
0X50	TS pin configure	RW
0X52	TS_HYSL2H setting	RW
0X53	TS_HYSH2L setting	RW
0X54	VLTF_CHG setting	RW
0X55	VHTF_CHG setting	RW
0X56	VLTF_WORK setting	RW
0X57	VHTF_WORK setting	RW
0X58	JIETA standard Enable control	RW
0x59-0X5B	JIETA standard setting	RW
0X61	Iprechg charger setting	RW
0X62	ICC charger setting	RW
0X63	Iterm charger setting and control	RW
0X64	CV charger voltage setting	RW
0X65	Thermal regulation threshold setting	RW
0X67	Charger timeout setting and control	RW
0X68	Battery detection control	RW
0X69	IR compensation	RW
0X6A	Button battery charge termination voltage setting	RW
0X70	CHGLED setting and control	RW
0X80-0X82	DCDC configure0/1/2	RW
0X83-0X86	DCDC1/2/3/4 voltage setting	RW

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Address	Description	R/W
0X90-0X91	LDOS ON/OFF control	RW
0X93-0X9F	LDOS voltage setting	RW
0XA1	Battery parameter	RW
0XA2	Fuel gauge control	RW
0XA4	Battery percentage data	R
0XC0	ADC Channel enable control	RW
0XC4-0XCB	VBAT/VBUS/VSYS/ICHG ADC data	R
0XCD	ADC_data select	RW
0XCE/0XCF	adc_data	R
0XE1	Type-C CC Audio Accessory enable	RW
0XE3	Type-C CC mode control	RW
0XE7	Type-C CC status	R

6.15.2 Register Description

6.15.2.1 REG 00: PMU status1

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	VBUS good indication 0: not good 1: good	RO	POR	0
4	BATFET state 0: close 1: open	RO	POR	0
3	Battery present state 0: absent 1: present	RO	POR	0
2	Battery in Active Mode 0: in Normal 1: in Active Mode	RO	POR	0
1	Thermal regulation status 0: normal 1: in thermal regulation	RO	POR	0
0	Current Limit state 0: not in current limit state 1: in current limit state	RO	POR	0

6.15.2.2 REG 01: PMU status2

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0

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6:5	Battery Current Direction 00: Standby 01: charge 10: discharge 11: Reserved	RO	POR	0
4	System status indication 0: System is power off. 1: System is power on.	RO	POR	0
3	VINDPM status 0: not in VINDPM 1: VINDPM	RO	POR	0
2:0	charging status 000: tri_charge 001: pre_charge 010: constant charge(CC) 011: constant voltage(CV) 100: charge done 101: not charging 11X: Reserved	RO	POR	0

6.15.2.3 REG 05: BC_detect

Bit	Description	R/W	Reset	Default
7:5	000:Reserved 001:SDP 010:CDP 011:DCP 1XX:	RO	POR	000b
4:0	Reserved	RO	/	0

6.15.2.4 REG 06: ILIM type

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2:0	001:power on default 010:VBUS remove default 011: TypeC CC 100:BC 1.2 101: ACL 110:TWI register configure	R0	POR	000b

6.15.2.5 REG 08: PMU fault

Bit	Description	R/W	Reset	Default
7:6	Reserved	/	/	00b
5	VBUS Over Voltage 0:VBUS<=7V 1:VBUS>7V	RW1C	POR	0b
4	DCDC Over Voltage 0: DCDC Voltage <= 130% 1: DCDC Voltage > 130%	RW1C	POR	0b
3	VSYS Over Voltage of 5V 0: VSYS < 5V 1: VSYS >= 5V	RW1C	POR	0b

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2	VBAT UVLO(2.5V) 0: VBAT >= UVLO(2.5V) 1: VBAT < UVLO(2.5V)	RW1C	POR	0b
1	Battery Over Temperature in Work mode 0: TS voltage<= Tvhtf_work 1: TS voltage> Tvhtf_work	RW1C	POR	0b
0	Battery Under Temperature in Work mode 0: TS voltage>= Tvltf_work 1: TS voltage< Tvltf_work	RW1C	POR	0b

6.15.2.6 REG 0B: module enable control1

Bit	Description	R/W	Reset	Default
7:5	Reserved	RW	/	0b
4	BC1.2 detect enable 0:disable 1:enable	RW	POR	EFUSE 0b
3	Type-C CC detect enable 0:disable 1:enable	RW	POR	EFUSE 0b
2	Gauge enable 0:disable 1:enable	RW	POR	1b
1	Reserved	RW	/	0b
0	Watchdog enable 0:disable 1:enable	RWAC	POR	0b

6.15.2.7 REG 10: DCDC/LDO Discharge_configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RW	/	00100b
2	Internal off-discharge enable for DCDC & LDO 0:disable 1:enable	RW	POR	1b
1:0	Reserved	RW	/	10b

6.15.2.8 REG 14: Tshut configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2:1	DIE Over Temperature Protection Level1 Configuration 00: 115deg 01: 125deg 10: 135deg 11: Reserved	RW	POR	01b
0	DIE Temperature Detect Enable	RW	POR	1b

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	0: disable 1: enable			

6.15.2.9 REG 15: Minimum system voltage control

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	00000b
2:0	Minimun system voltage limit 3.0+N*0.1 V 000: 3.0V 001: 3.1V 010: 3.2V 011: 3.3V 100: 3.4V 101: 3.5V 110: 3.6V 111: 3.7V	RW	POR	101b

6.15.2.10 REG 16: Input voltage limit control

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	
3:0	VINDPM configuration: 3.88+N*0.08 V 0000: 3.88V 0001: 3.96V 0010: 4.04V 0011: 4.12V 0100: 4.20V 0101: 4.28V 0110: 4.36V 0111: 4.44V 1000: 4.52V 1001: 4.60V 1010: 4.68V 1011: 4.76V 1100: 4.84V 1101: 4.92V 1110: 5.00V 1111: 5.08V	RW	POR	EFUSE 0110b

6.15.2.11 REG 17: Input current limit control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	
5:0	Input current limit: 100+N*50mA 000000: 100mA 000001: 150mA 000010: 200mA …… 111110: 3200mA 111111: 3250mA	RW	POR	EFUSE 001000b

6.15.2.12 REG 18: Reset the fuel gauge

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	reset the gauge(includes registers) 0: normal 1: reset	RWAC	POR	0b
2	reset the gauge besides registers 0: normal 1: reset	RW	POR	0b
1:0	Reserved	RO	/	0

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6.15.2.13 REG 19: module enable control2

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	Boost enable 0: disable 1: enable	RW	System Reset	0b
3	Button Battery charge enable 0: disable 1: enable	RW	System Reset	0b
2	Battery charge led enable 0: disable 1: enable	RW	POR	1b
1	Battery charge enable 0: disable 1: enable	RW	System Reset	1b
0	Watchdog Module enable 0: disable 1: enable	RW	System Reset	0b

6.15.2.14 REG 1A: Watchdog control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:4	Watchdog Reset Configuration 00: IRQ only 01: IRQ and System Reset 10: System Reset and Pull down PWROK 1s 11: System Restart(PWROFF & PWRON)and Pull down PWROK 1s	RW	POR	0b
3	watchdog clear signal 0: normal 1: clear	RWAC	POR	0b
2:0	TWSI watchdog timer configuration 000: 1s 001: 2s 010: 4s 011: 8s 100: 16s 101: 32s 110: 64s 111: 128s	RW	POR	110b

6.15.2.15 REG 1B: Gauge low battery warning threshold setting

Bit	Description	R/W	Reset	Default
7:4	low battery warning threshold 5-20%, 1% per step 0000: 5% 0001: 6% …… 1111: 20%	RW	POR	1010b
3:0	low battery shutdown threshold 0-15%, 1% per step	RW	POR	0001b

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	0000: 0% 0001: 1% …… 1111: 15%			

6.15.2.16 REG 1C: GPO configure

Bit	Description	R/W	Reset	Default
7:5	Reserved	RW	POR	000b
4	GPO1 Output Configure 0: Low 1: High	RW	POR	0b
3:1	Reserved	RW	POR	000b
0	GPO0 Output Configure 0: Low 1: High	RW	POR	0b

6.15.2.17 REG 1D: Low power configure

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	POR	0000111b
0	Green mode enable 0: disable 1: enable	RW	System Reset	0b

6.15.2.18 REG 1E: Boost configure

Bit	Description	R/W	Reset	Default
7:4	Boost voltage regulation 4.55+0.064*N V 0000:4.550V 0001:4.614V 0010:4.678V …… 1110:5.446V 1111:5.510V	RW	System Reset	1001b
3:2	Boost Disable threshold 00:2.4V 01:2.6V 10:2.8V 11:3.0V	RW	POR	01b
1:0	Boost Output current limit 00: 500mA 01:900mA 10:1500mA 11:Disable current limit	RW	System Reset	00b

6.15.2.19 REG 20: PWRON status

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	POWERON always high when EN Mode as POWERON Source 0: no 1: yes	RO	System Reset	0b

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4	Battery Insert and Good as POWERON Source 0: no 1: yes	RO	System Reset	0b
3	Battery Voltage > 3.3V when Charged as Source 0: no 1: yes	RO	System Reset	0b
2	VBUS Insert and Good as POWERON Source 0: no 1: yes	RO	System Reset	0b
1	IRQ PIN Pull-down as POWERON Source 0: no 1: yes	RO	System Reset	0b
0	POWERON low for on level when POWERON Mode as POWERON Source 0: no 1: yes	RO	System Reset	0b

6.15.2.20 REG 21: PWROFF status

Bit	Description	R/W	Reset	Default
7	Die Over Temperature as POWEROFF Source 0: no 1: yes	RO	POR	0b
6	DCDC Over Voltage as POWEROFF Source 0: no 1: yes	RO	POR	0b
5	DCDC Under Voltage as POWEROFF Source 0: no 1: yes	RO	POR	0b
4	LDO over current as POWEROFF Source 0: no 1: yes	RO	POR	0b
3	VSYS Under Voltage as POWEROFF Source 0: no 1: yes	RO	POR	0b
2	POWERON always low when EN Mode as POWEROFF Source 0: no 1: yes	RO	POR	0b
1	Software configuration as POWEROFF Source 0: no 1: yes	RO	POR	0b
0	POWERON Pull down for off level when POWERON Mode as POWEROFF Source 0: no 1: yes	RO	POR	0b

6.15.2.21 REG 22: PWROFF_EN

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0000b
3	LDO Over-Current as POWEROFF Source enable 0: disable 1: enable	RW	POR	EFUSE 0b

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2	Reserved	RO	/	1b
1	PWRON > OFFLEVEL as POWEROFF Source enable 0: disable 1: enable	RW	POR	EFUSE 0b
0	Function Select when REG22[2]=1 and button event occur 0: Power-off 1: Restart	RW	POR	EFUSE 0b

6.15.2.22 REG 23: PWROFF of DCDC OVP/UVP control

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	DCDC 120%(130%) high voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b
3	DCDC4 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	0b
2	DCDC3 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b
1	DCDC2 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b
0	DCDC1 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1b

6.15.2.23 REG 24: VSYS voltage for PWROFF threshold setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:4	Battery Voltage for POWEROFF 2.6~3.3V,0.1V/step,8steps 000: 2.6V 001: 2.7V …… 111: 3.3V	RW	POR	EFUSE 000b
3	Reserved	RO	/	0
2	Check the PWROK Pin enable after all dcdc/ldo output valid 128ms 0: disable 1: enable	RW	POR	1b
1	POWEROFF Delay 4ms after PWROK disable 0: disable 1: enable	RW	POR	1b
0	POWEROFF Sequence Control 0: At the same time 1: the reverse of the startup	RW	POR	0b

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6.15.2.24 REG 25: Sleep and Wakeup configure

Bit	Description	R/W	Reset	Default
7	Reserved	R0	/	0
6	Auto sleep enable 0: disable 1: enable	RWAC	System Reset	0b
5	IRQ Pin low to Wakeup 0: disable 1: enable	RW	POR	0b
4:3	Reserved	RO	POR	00b
2	DCDC/LDO Voltage Select when Wakeup 0: The Default 1: The voltage before wakeup	RW	POR	0b
1	Wake Up enable 0: disable 1: enable	RWLC	System Reset	0b
0	SLEEP enable 0: disable 1: enable	RWLC	System Reset	0b

6.15.2.25 REG 26: IRQLEVEL/OFFLEVEL/ONLEVEL setting

Bit	Description	R/W	Reset	Default
7:6	Reserved	R0	/	0
5:4	IRQLEVEL configuration 00: 1s 01: 1.5s 10: 2s 11: 2.5s	RW	POR	01b
3:2	OFFLEVEL configuration 00: 4s 01: 6s 10: 8s 11: 10s	RW	POR	01b
1:0	ONLEVEL configuration 00: 128ms 01: 512ms 10: 1s 11: 2s	RW	POR	EFUSE 10b

6.15.2.26 REG 27: Soft Poweroff configure

Bit	Description	R/W	Reset	Default
7:4	Reserved	R0	POR	0000b
3	PWROK PIN pull low to Restart the System 0: disable 1: enable	RW	POR	0b
2	PWRON 16s to shutdown the PMIC enable 0: disable 1: enable	RW	POR	1b
1	Restart the System, POWOFF/POWON and reset the related	RWAC	POR	0b

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	registers 0: normal 1: reset			
0	Soft PWROFF 0: Normal 1: PWROFF Configure	RWAC	POR	0b

6.15.2.27 REG 28: Auto Sleep map0

Bit	Description	R/W	Reset	Default
7	ALDO4 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
6	ALDO3 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
5	ALDO2 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
4	ALDO1 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
3	DCDC4 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
2	DCDC3 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
1	DCDC2 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
0	DCDC1 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b

6.15.2.28 REG 29: Auto Sleep map1

Bit	Description	R/W	Reset	Default
7	CLDO4 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
6	CLDO3 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
5	CLDO2 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
4	CLDO1 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
3	BLDO4 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b

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2	BLDO3 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
1	BLDO2 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
0	BLDO1 PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b

6.15.2.29 REG 2A: Auto Sleep map2

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	POR	0b
1	GREEN MODE enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b
0	CPUSLDO PWROFF enable when auto_sleep configure 0: disable 1: enable	RW	POR	0b

6.15.2.30 REG 2B: Fast pwron setting 0

Bit	Description	R/W	Reset	Default
7:6	DCDC4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	DCDC3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	DCDC2 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
1:0	DCDC1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

6.15.2.31 REG 2C: Fast pwron setting 1

Bit	Description	R/W	Reset	Default
7:6	ALDO4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	ALDO3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	ALDO2 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
1:0	ALDO1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

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6.15.2.32 REG 2D: Fast pwron setting 2

Bit	Description	R/W	Reset	Default
7:6	BLDO4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	BLDO3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	BLDO2 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
1:0	BLDO1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

6.15.2.33 REG 2E: Fast pwron setting 3

Bit	Description	R/W	Reset	Default
7:6	CLDO4 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
5:4	CLDO3 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
3:2	CLDO2 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b
1:0	CLDO1 Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

6.15.2.34 REG 2F: Fast pwron setting 4

Bit	Description	R/W	Reset	Default
7	Reserved	RO	POR	0b
5	Fast Power On Enable 0: disable 1: enable	RW	POR	0b
4	Fast Wake up Enable 0: disable 1: enable	RW	POR	0b
3:2	Reserved	RO	POR	00b
1:0	CPUSLDO Fast Power On Start Sequence 00~10: Start Sequence Code 11: disable	RW	POR	0b

6.15.2.35 REG 3E: TWI/RSB configure

Bit	Description	R/W	Reset	Default
7:0	BUS Mode Select: 7Ch : RSB others: TWI	RW	POR	00h

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6.15.2.36 REG 40: IRQ Enable 0

Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level2 IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	SOC drop to Warning Level1 IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Reserved	RO	/	1b
4	Gauge New SOC IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Reserved	RO	/	0b
2	BOOST Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	0b
1	VBUS Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	VBUS Fault IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.15.2.37 REG 41: IRQ Enable 1

Bit	Description	R/W	Reset	Default
7	VBUS Insert IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	VBUS Remove IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Battery Insert IRQ enable 0: disable 1: enable	RW	System Reset	1b
4	Battery Remove IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	POWERON Short PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	POWERON Long PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	POWERON Negative Edge IRQ enable 0: disable 1: enable	RW	System Reset	0b
0	POWERON Positive Edge IRQ enable 0: disable 1: enable	RW	System Reset	0b

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6.15.2.38 REG 42: IRQ Enable 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ enable 0: disable 1: enable	RW	System Reset	0b
6	LDO Over Current IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	BATFET Over Current Protection IRQ enable 0: disable 1: enable	RW	System Reset	0b
4	Battery charge done IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Charger start IRQ(chgst_irq) enable 0: disable 1: enable	RW	System Reset	1b
2	DIE Over Temperature level1 IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	Charger Safety Timer1/2 expire IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	Battery Over Voltage Protection IRQ enable 0: disable 1: enable	RW	System Reset	1b

6.15.2.39 REG 43: IRQ Enable 3

Bit	Description	R/W	Reset	Default
7	BC1.2 detect finished IRQ enable 0: disable 1: enable	RW	System Reset	1b
6	BC1.2 detect result change IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Reserved	RO	POR	0b
4	Battery Over Temperature Quit IRQ enable 0: disable 1: enable	RW	System Reset	1b
3	Battery Over Temperature in Charge mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
2	Battery Under Temperature in Charge mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
1	Battery Over Temperature in Work mode IRQ enable 0: disable 1: enable	RW	System Reset	1b
0	Battery Under Temperature in Work mode IRQ enable 0: disable 1: enable	RW	System Reset	1b

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6.15.2.40 REG 44: IRQ Enable 4

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0b
6	Type-C device removed (unattached) IRQ enable 0: disable 1: enable	RW	System Reset	1b
5	Type-C device insert and detection finished IRQ enable 0: disable 1: enable	RW	System Reset	1b
4:0	Reserved	RO	/	00011b

6.15.2.41 REG 48: IRQ Status 0

Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level IRQ 0: no irq 1: irq when SOC >= Warning Level or SOC < shutdown Level to clear it	RW1C	POR	0b
6	SOC drop to Shutdown Level IRQ 0: no irq 1: irq when SOC >= Shutdown Level to clear it	RW1C	System Reset	0b
5	Reserved	RO	POR	0b
4	Gauge New SOC IRQ 0: no irq 1: irq	RW1C	System Reset	0b
3	Reserved	RO	System Reset	0b
2	BOOST OverVoltage IRQ 0: no irq 1: irq	RW1C	System Reset	0b
1	VBUS OverVoltage IRQ 0: no irq 1: irq	RW1C	System Reset	0b
0	VBUS Fault IRQ 0: no irq 1: irq	RW1C	System Reset	0b

6.15.2.42 REG 49: IRQ Status 1

Bit	Description	R/W	Reset	Default
7	VBUS Insert IRQ 0: no irq 1: irq VBUS Remove to clear it	RW1C	System Reset	0b
6	VBUS Remove IRQ 0: no irq 1: irq	RW1C	System Reset	0b

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	VBUS Insert to clear it			
5	Battery Insert IRQ 0: no irq 1: irq Battery Remove to clear it	RW1C	System Reset	0b
4	Battery Remove IRQ 0: no irq 1: irq Battery Insert to clear it	RW1C	System Reset	0b
3	POWERON Short PRESS IRQ 0: no irq 1: irq	RW1C	System Reset	0b
2	POWERON Long PRESS IRQ 0: no irq 1: irq	RW1C	System Reset	0b
1	POWERON Negative Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0b
0	POWERON Positive Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0b

6.15.2.43 REG 4A: IRQ Status 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ 0: no irq 1: irq	RW1C	System Reset	0b
6	LDO Over Current IRQ 0: no irq 1: irq LDO Current to normal to clear it	RW1C	System Reset	0b
5	BATFET Over Current Protection IRQ 0: no irq 1: irq	RW1C	System Reset	0b
4	Battery charge done IRQ 0: no irq 1: irq Battery charge start to clear it	RW1C	System Reset	0b
3	Battery charge start IRQ 0: no irq 1: irq Battery charge done to clear it	RW1C	System Reset	0b
2	DIE Over Temperature level1 IRQ 0: no irq 1: irq DIE Temperature to normal to clear it	RW1C	System Reset	0b
1	Charger Safety Timer1/2 expire IRQ 0: no irq 1: irq	RW1C	System Reset	0b
0	Battery Over Voltage Protection IRQ	RW1C	System	0b

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	0: no irq 1: irq Battery Voltage to normal to clear it		Reset	

6.15.2.44 REG 4B: IRQ Status 3

Bit	Description	R/W	Reset	Default
7	BC1.2 detect finished IRQ. 0: no irq 1: irq VBUS remove, bc1.2 detect again will clear it.	RW1C	System Reset	0b
6	BC1.2 detect result change IRQ 0: no irq 1: irq VBUS remove will clear it	RW1C	System Reset	0b
5	Reserved	RO	System Reset	0b
4	Battery Over Temperature Quit in Charge mode IRQ 0: no irq 1: irq bcot_irq to clear it	RW1C	System Reset	0b
3	Battery Over Temperature in Charge mode IRQ 0: no irq 1: irq bcotq_irq to clear it	RW1C	System Reset	0b
2	Battery Under Temperature in Charge mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b
1	Battery Over Temperature in Work mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b
0	Battery Under Temperature in Work mode IRQ 0: no irq 1: irq Battery Temperature to normal to clear it	RW1C	System Reset	0b

6.15.2.45 REG 4C: IRQ Status 4

Bit	Description	R/W	Reset	Default
7	Reserved	RO	System Reset	0b
6	Type-C device removed (unattached) IRQ status: 0: no irq 1: irq insert_irq to clear it	RW1C	System Reset	0b
5	Type-C device insert and detection finished IRQ status: 0: no irq 1: irq	RW1C	System Reset	0b

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	remove irq to clear it			
4:0	Reserved	RO	System Reset	00000b

6.15.2.46 REG 50: TS pin configure

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	TS PIN function select: 0: TS pin is the battery temperature sensor input and will affect the charger 1: TS pin is the external fixed input and doesn't affect the charger	RW	POR	EFUSE 0b
3:2	TS current source on/off enable 00: off 01/10: on when TS channel of ADC is enabled 11: always on	RW	POR	EFUSE 01b
1:0	current source to TS pin configuration 00: 20uA 01: 40uA 10: 50uA 11: 60uA	RW	POR	10b

6.15.2.47 REG 52: TS_HYSL2H setting

Bit	Description	R/W	Reset	Default
7:0	hysteresis for TS from low go to normal Thys = N*16mV (default 32mV)	RW	POR	2h

6.15.2.48 REG 53: TS_HYSH2L setting

Bit	Description	R/W	Reset	Default
7:0	hysteresis for TS from high go to normal Thys = N*4mV (default 4mV)	RW	POR	1h

6.15.2.49 REG 54: VLTFCHG setting

Bit	Description	R/W	Reset	Default
7:0	VLTF in voltage of charge configuration VLTF = N*32 mV (default is about 0deg) This is also T1 of JEITA	RW	POR	29h

6.15.2.50 REG 55: VHTFCHG setting

Bit	Description	R/W	Reset	Default
7:0	VHTF in voltage of charge configuration	RW	POR	58h

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	VHTF = N*2 mV (default is about 55deg) This is also T4 of JEITA			

6.15.2.51 REG 56: VLTFWORK setting

Bit	Description	R/W	Reset	Default
7:0	VLTF in voltage of work configuration VLTF = N*32 mV (default is about -10deg)	RW	POR	3Eh

6.15.2.52 REG 57: VHTFWORK setting

Bit	Description	R/W	Reset	Default
7:0	VHTF in voltage of work configuration VHTF = N*2 mV (default is about 60deg)	RW	POR	4Ch

6.15.2.53 REG 58: JIETA standard Enable control

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	JEITA Standard Enable 0: disable 1: enable	RW	POR	EFUSE 0b

6.15.2.54 REG 59: JEITA CV configuration

Bit	Description	R/W	Reset	Default
7:6	Current fall of Warm in JEITA Standard 00: 100% 01: 50% 10:25% 11:Reserved	RW	POR	00b
5:4	Current fall of Cool in JEITA Standard 00: 100% 01: 50% 10:25% 11:Reserved	RW	POR	01b
3:2	Reserved	RO	/	01b
1:0	Reserved	RO	/	00b

6.15.2.55 REG 5A: JIETA Cool configuration

Bit	Description	R/W	Reset	Default
7:0	Cool Temperature(T2) in voltage of charge configuration VHTF = N*16 mV (default is about 10deg)	RW	POR	37h

6.15.2.56 REG 5B: JIETA Warm configuration

Bit	Description	R/W	Reset	Default
7:0	Warm Temperature(T3) in voltage of charge configuration VHTF = N*8 mV (default is about 45deg)	RW	POR	1Eh

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6.15.2.57 REG 61: Iprechg charger setting

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3:0	Precharge current limit: 64*N mA 0000: 0mA 0001: 64mA 0010: 128mA …… 0100: 896mA 0101: 960mA	RW	POR	0010b

6.15.2.58 REG 62: ICC charger setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
5:0	constant current charge current limit: 64*N mA if N<=48 000000: 0mA 000001: 64mA 000010: 128mA …… 101110: 2944mA 101111: 3008mA 110000~111111: Reserved	RW	POR	010000b

6.15.2.59 REG 63: Iterm charger setting and control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	DPM to disbale charger terminal 0: enable charger terminal 1: disable charger terminal	RW	POR	0b
4	Charging termination of current enable 0: disable 1: enable	RW	System Reset	1b
3:0	Termination current limit: 64*N mA 0000: 0mA 0001: 64mA 0010: 128mA …… 0111: 896mA 1000: 960mA	RW	POR	0101b

6.15.2.60 REG 64: CV charger voltage setting

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2:0	Charge voltage limit 000: 4.0V 001: 4.1V 010: 4.2V	RW	POR	010b

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	011: 4.35V 100: 4.4V 111: 5.0V 101~110: Reserved			

6.15.2.61 REG 65: Thermal regulation threshold setting

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	/	0
1:0	Thermal regulation threshold 00: 60deg 01: 80deg 10: 100deg 11: 120deg	RW	System Reset	10b

6.15.2.62 REG 67: Charger timeout setting and control

Bit	Description	R/W	Reset	Default
7	safety timer1/2 setting during DPM or thermal regulation 0: safety timer not slowed during input DPM or thermal regulation 1: safety timer slowed during input DPM or thermal regulation	RW	POR	1b
6	Fast charge safe timer enable 0: disable 1: enable	RW	POR	1b
5:4	Fast charge safety timer configuration 00: 5hours 01: 8hours 10: 12hours 11: 20hours	RW	POR	10b
3	Reserved	RO	/	0
2	pre-charge safe timer enable 0: disable 1: enable	RW	POR	1b
1:0	pre-charge safe timer configuration 00: 40mins 01: 50mins 10: 60mins 11: 70mins	RW	POR	10b

6.15.2.63 REG 68: Battery detection control

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	battery detection enable 0: disable 1: enable	RW	POR	1b

6.15.2.64 REG 69: IR compensation

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	IR Compensation Enable	RW	POR	0b

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	0: disable 1: enable			

6.15.2.65 REG 6A: Button battery charge termination voltage setting

Bit	Description	R/W	Reset	Default
7:3		RO	/	0
2:0	Button Battery charge termination voltage 2.6~3.3V，100mV/step，8steps 000: 2.6V 001: 2.7V 010: 2.8V 011: 2.9V 100: 3.0V 101: 3.1V 110: 3.2V 111: 3.3V	RW	POR	011b

6.15.2.66 REG 70: CHGLED setting and control

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6	CHGLED pin output breath enable when REG70[2:0]=011b 0: disable; 1: enable;	RW	System Reset	0b
5:4	CHGLED pin output when REG70[2:0]=110b 00: Hiz; 01: Low/Hiz 25%/75% duty 1Hz; 10: Low/Hiz 25%/75% duty 4Hz; 11: drive low;	RW	System Reset	00b
3	Reserved	RO	/	0
2:0	CHGLED pin display function configuration 000: display with type A function 001: display with type B function 010: display with breath function controlled by charger 011: display with breath function controlled by REG70<6> 110: output controlled by the register REG70[5:4] 100/101/111: Reserved	RW	POR	EFUSE 000b

6.15.2.67 REG 80: DCDC configure0

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0b
3	DCDC4 enable 0: disable 1: enable	RW	System Reset	EFUSE
2	DCDC3 enable	RW	System	EFUSE

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	0: disable 1: enable		Reset	
1	DCDC2 enable 0: disable 1: enable	RW	System Reset	EFUSE
0	DCDC1 enable 0: disable 1: enable	RW	System Reset	EFUSE

6.15.2.68 REG 81: DCDC configure1

Bit	Description	R/W	Reset	Default
7	DCDC frequency spread enable 0: disable 1: enable	RW	System Reset	0b
6	DCDC frequency spread range control 0: 50KHz 1: 100kHz	RW	System Reset	0b
5	Reserved	RO	/	0b
4	DCDC3 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
3	DCDC2 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
2	DCDC1 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0b
1:0	DCDC UVP debounce time configuration 00: 60us 01: 120us 10: 180us 11: 240us	RW	POR	00b

6.15.2.69 REG 82: DCDC configure2

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	DVM voltage ramp control 0: 15.625 us/step 1: 31.250 us/step	RW	System Reset	0b

6.15.2.70 REG 83: DCDC1 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC1 DVM enable control 0: disable 1: enable	RW	System Reset	1b
6:0	DCDC1 output voltage config 0.5~1.2V,10mV/step,71steps 1.22~1.54V,20mV/step,17steps	RW	System Reset	EFUSE

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	0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1010111: 1.54V 1011000~1111111: Reserved			

6.15.2.71 REG 84: DCDC2 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC2 DVM enable control 0: disable 1: enable	RW	System Reset	1b
6:0	DCDC2 output voltage config 0.5~1.2V,10mV/step,71steps 1.22~1.54V,20mV/step,17steps 1.6~3.4V,100mV/step,19steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1010111: 1.54V 1011000: 1.60V 1011001: 1.70V …… 1101011: 3.40V 1101100~1111111: Reserved	RW	System Reset	EFUSE

6.15.2.72 REG 85: DCDC3 voltage setting

Bit	Description	R/W	Reset	Default

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7	DCDC3 DVM enable control 0: disable 1: enable	RW	System Reset	1b
6:0	DCDC3 output voltage config 0.5~1.2V,10mV/step,71steps 1.22~1.84V,20mV/step,32steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1100110: 1.84V 1100111~1101000: Reserved	RW	System Reset	EFUSE

6.15.2.73 REG 86: DCDC4 voltage setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:0	DCDC4 output voltage config 1.0~3.7V,100mV/step,24steps 00000: 1.0V 00001: 1.1V …… 11011: 3.7V 11100~11111: Reserved	RW	System Reset	EFUSE

6.15.2.74 REG 90: LDOS ON/OFF control 0

Bit	Description	R/W	Reset	Default
7	bldo4 enable 0: disable 1: enable	RW	System Reset	EFUSE
6	bldo3 enable 0: disable 1: enable	RW	System Reset	EFUSE
5	bldo2 enable 0: disable 1: enable	RW	System Reset	EFUSE
4	bldo1 enable	RW	System	EFUSE

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	0: disable 1: enable		Reset	
3	aldo4 enable 0: disable 1: enable	RW	System Reset	EFUSE
2	aldo3 enable 0: disable 1: enable	RW	System Reset	EFUSE
1	aldo2 enable 0: disable 1: enable	RW	System Reset	EFUSE
0	aldo1 enable 0: disable 1: enable	RW	System Reset	EFUSE

6.15.2.75 REG 91: LDOS ON/OFF control 1

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	cpusldo enable 0: disable 1: enable	RW	System Reset	EFUSE
3	cldo4 enable 0: disable 1: enable	RW	System Reset	EFUSE
2	cldo3 enable 0: disable 1: enable	RW	System Reset	EFUSE
1	cldo2 enable 0: disable 1: enable	RW	System Reset	EFUSE
0	cldo1 enable 0: disable 1: enable	RW	System Reset	EFUSE

6.15.2.76 REG 93: ALDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.77 REG 94: ALDO2 voltage setting

Bit	Description	R/W	Reset	Default

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7:5		RO	/	0
4:0	aldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.78 REG 95: ALDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.79 REG 96: ALDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	aldo4 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.80 REG 97: BLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	bldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V	RW	System Reset	EFUSE

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	00001: 0.6V …… 11110: 3.5V 11111: Reserved			

6.15.2.81 REG 98: BLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	bldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.82 REG 99: BLDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	bldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.83 REG 9A: BLDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	bldo4 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

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6.15.2.84 REG 9B: CLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.85 REG 9C: CLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.86 REG 9D: CLDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	EFUSE

6.15.2.87 REG 9E: CLDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cldo4 output voltage configuration	RW	System	EFUSE

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	0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved		Reset	

6.15.2.88 REG 9F: CPUSLDO voltage setting

Bit	Description	R/W	Reset	Default
7:5		RO	/	0
4:0	cpusldo output voltage configuration 0.5~1.4V，50mV/step，20steps 00000: 0.50V 00001: 0.55V …… 10011: 1.40V 10100~11111: Reserved	RW	System Reset	EFUSE

6.15.2.89 REG A1: Battery parameter

Bit	Description	R/W	Reset	Default
7:0	Battery parameter ROM	RO	POR	xx

6.15.2.90 REG A2: Fuel gauge control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5	Reserved	RW	POR	0b
4	ROM or SRAM select 1: select sram; 0: select rom;	RW	POR	0b
3:1	Reserved	RO	/	0b
0	brom writer control 1:enable 0:disable	RW	POR	0b

6.15.2.91 REG A4: Battery percentage data

Bit	Description	R/W	Reset	Default
7:0	battery percentage	RO	POR	00h

6.15.2.92 REG C0: ADC Channel enable control

Bit	Description	R/W	Reset	Default

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7	batton battery(backup battery) voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0b
6	VMID voltage measure ADC channel 0 enable 0: disable 1: enable	RW	POR	0b
5	charger current ADC channel enable 0: disable 1: enable	RW	POR	0b
4	die temperature measure ADC channel enable 0: disable 1: enable	RW	POR	0b
3	system voltage voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0b
2	VBUS voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0b
1	TS pin measure ADC channel enable 0: disable 1: enable	RW	POR	1b
0	battery voltage measure ADC channel enable 0: disable 1: enable	RW	POR	1b

6.15.2.93 REG C4: vbat_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	vbat[13:8]	RO	POR	0b

6.15.2.94 REG C5: vbat_l

Bit	Description	R/W	Reset	Default
7:0	vbat[7:0]	RO	POR	0b

6.15.2.95 REG C6: VBUS_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	VBUS[13:8]	RO	POR	0b

6.15.2.96 REG C7: VBUS_l

Bit	Description	R/W	Reset	Default
7:0	VBUS[7:0]	RO	POR	0b

6.15.2.97 REG C8: VSYS_h

Bit	Description	R/W	Reset	Default

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7:6	Reserved	RO	/	0b
5:0	VSYS[13:8]	RO	POR	0b

6.15.2.98 REG C9: VSYS_l

Bit	Description	R/W	Reset	Default
7:0	VSYS[7:0]	RO	POR	0b

6.15.2.99 REG CA: ICHG_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	ichg_h[13:8]	RO	POR	0b

6.15.2.100 REG CB: ICHG_l

Bit	Description	R/W	Reset	Default
7:0	ichg_l[7:0]	RO	POR	0b

6.15.2.101 REG CD: ADC_data select

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	/	0
1:0	adc_data_h/adc_data_l select configure: 00: TS 01:TDIE 10:VMID 11:VBACKUP	RW	POR	0b

6.15.2.102 REG CE: adc_data_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0b
5:0	adc_data_h[13:8]	RO	POR	0b

6.15.2.103 REG CF: adc_data_l

Bit	Description	R/W	Reset	Default
7:0	adc_data_l[7:0]	RO	POR	0b

6.15.2.104 REG E1: Type-C CC Audio Accessory enable

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	Audio Accessory Enable. 0: disable 1: enable	RW	POR	0
4:0	Reserved	RO	/	0

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6.15.2.105 REG E3: Type-C CC mode control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	DRP port prefer to be SRC. 0: unactive 1: active	RW	POR	0b
4	DRP port prefer to be SNK. 0: unactive 1: active	RW	POR	1b
3:2	The Current Mode Control. 0x: Default Mode 10: 1.5A Mode 11: 3.0A Mode	RW	POR	00b
1:0	The Port Mode Control. 00: Disable 01: SINK 10: SOURCE 11: DRP	RW	POR	01b

6.15.2.106 REG E7: Type-C CC status

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:4	The Power State of Source of CC Logic in HW mode 00: POWER IDLE 01: POWER_DEF 10: POWER_1P5A 11: POWER_3P0A	RO	POR	00b
3:0	The State of CC Logic in HW mode 0000: DISABLE 0001: UNATTACH_SNK 0010: ATTACHWAIT_SNK 0011: ATTACH_SNK 0100: UNATTACH_SRC 0101: ATTACHWAIT 0110: ATTACH_SRC 0111: AUDIO_ACSY 1000: Reserved 1001: TRY_SRC 1010: TRYWAIT_SNK 1011: TRY_SNK 1100: TRYWAIT_SRC 1101: Reserved 1110: ERROR_RECOVERY	RO	POR	0000b

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	1111: Reserved			

Note:

Default value below “EFUSE” is the default efuse value. If different EFUSE configuration is needed, please contact FAE/SD for support.

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7 Application Information

7.1 Typical Application

Figure 7-1 Charger Mode Application

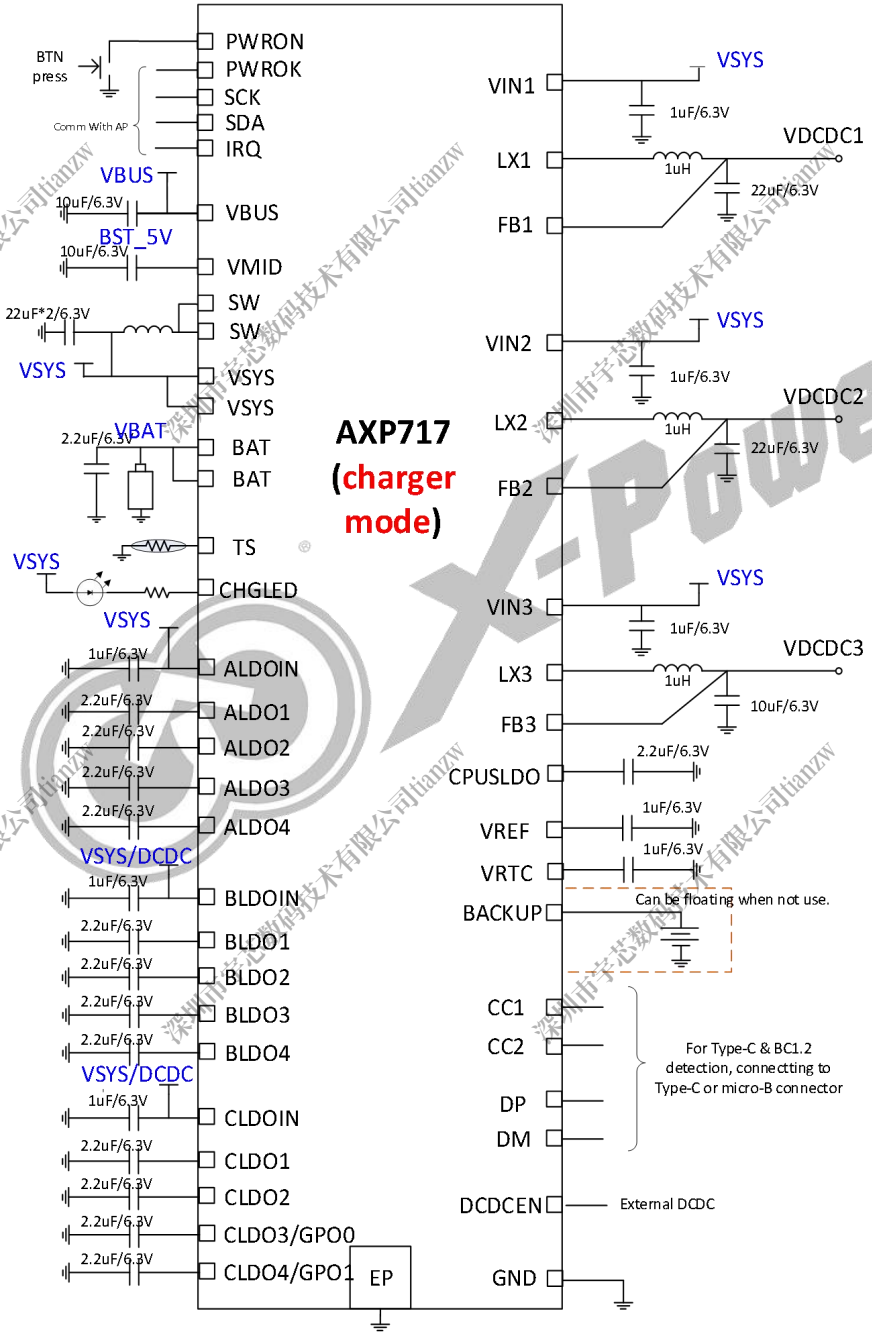

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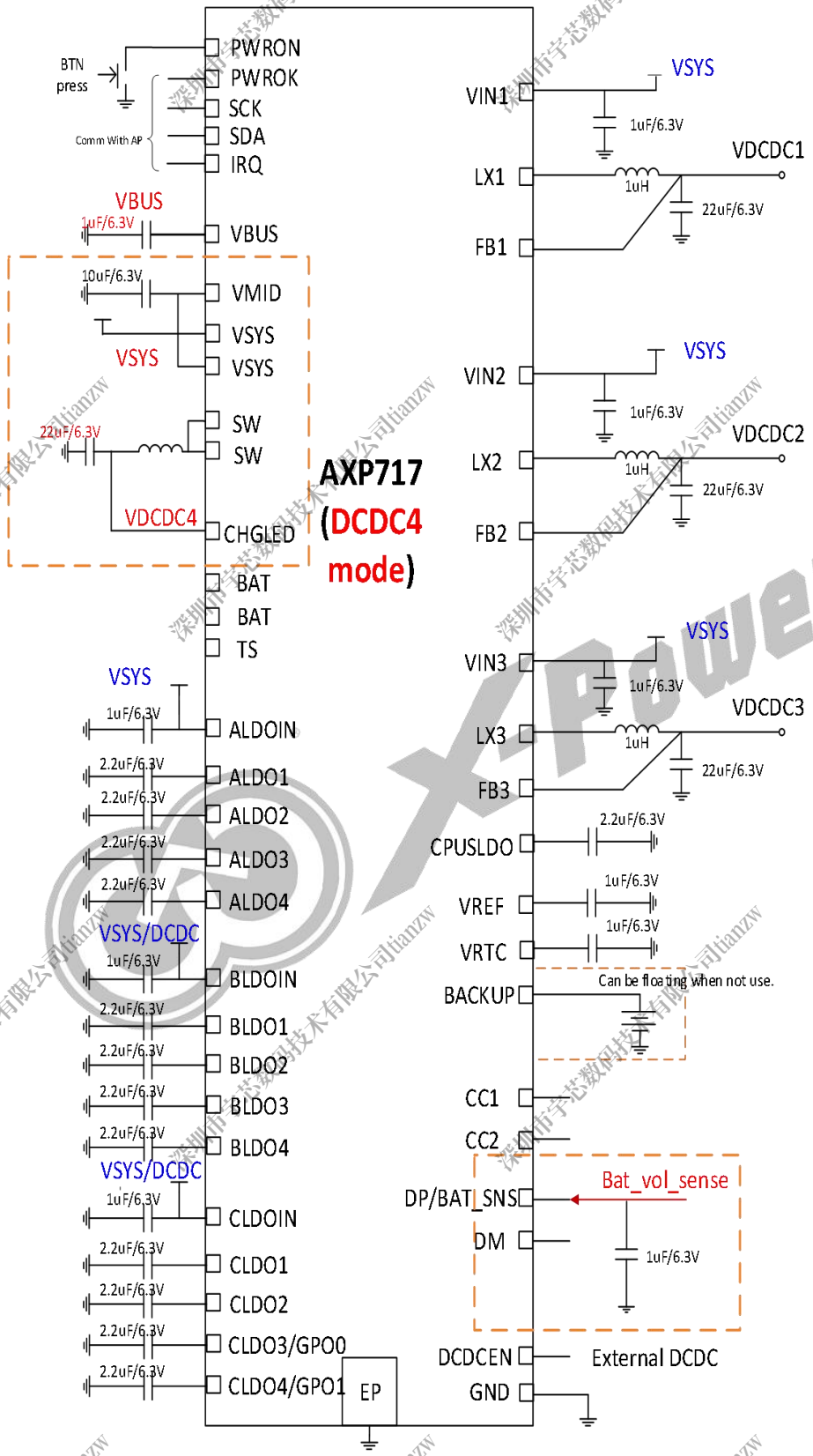
Figure 7-2 DCDC Mode Application



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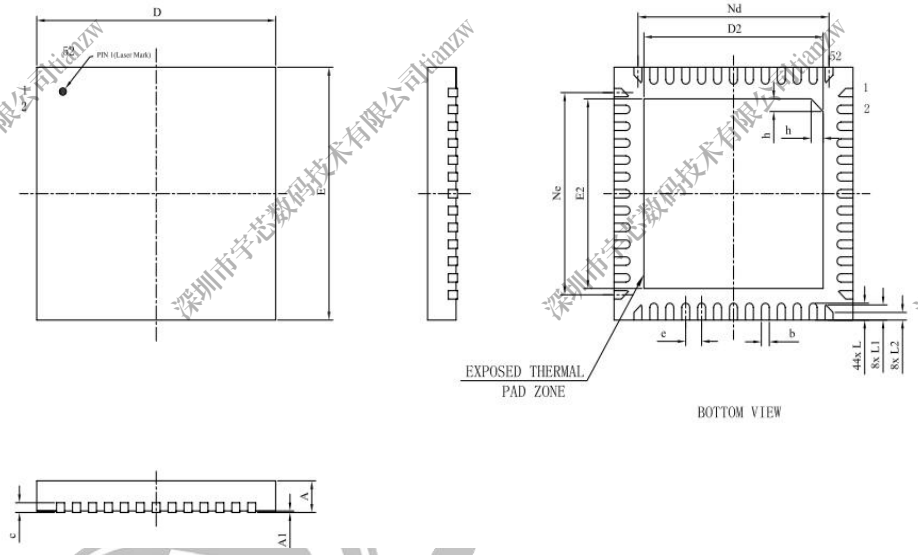
8 Package, Carrier, Storage and Baking Information

8.1 Package

AXP717 package is QFN6*6, 52-pin. Figure 8-1 shows AXP717 package.

Figure 8-1 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 8-2 AXP717 Marking

Table 8-1 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP717	Product name	Fixed
2	LLLLLBA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

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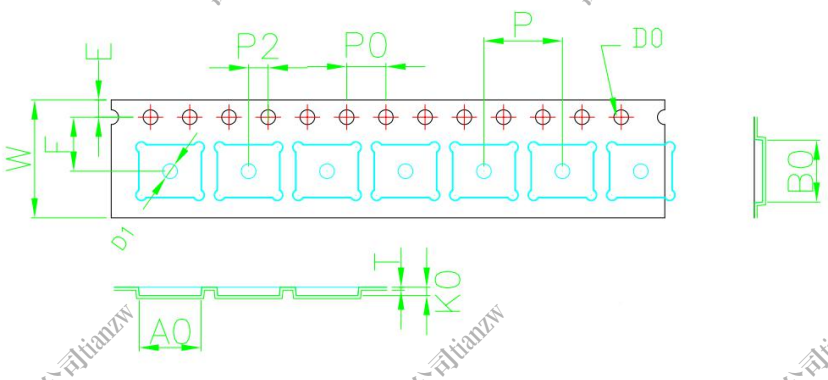
8.2 Carrier

Figure 8-3 AXP717 Tape Dimension Drawing



W	16.00±0.30	P	8.00±0.10	A0	6.30±0.10	B0	6.30±0.10
S	0.00±0.10	P0	4.00±0.10	A1		B1	
E	1.75±0.10	P2	2.00±0.10			B2	
F	7.50±0.10	D0	ø1.50 +0.10 0	K0	0.85 +0.10 −0.05	K1	
T	0.30±0.05	D1	ø1.50 +0.10 0.10				

Table 8-2 AXP717 Packing Quantity Information

Type	Quantity	Part Number
Tape	3000pcs/Tape	AXP717

8.3 Storage

8.3.1 Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in the following table.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30℃/85%RH
2	1 year	≤30℃/60%RH
2a	4 weeks	≤30℃/60%RH
3	168 hours	≤30℃/60%RH
4	72 hours	≤30℃/60%RH
5	48 hours	≤30℃/60%RH

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5a	24 hours	≤30℃/60%RH
6	Time on Label(TOL)	≤30℃/60%RH

AXP717 device samples are classified as MSL3.

8.3.2 Bagged Storage Conditions

The shelf life of AXP717 are defined in the following table.

Table 8-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Shelf life	6 months

8.3.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP717 is as follows.

Table 8-5 Out-of-bag Duration

Storage temperature	20℃~26℃
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

8.4 Baking

It is not necessary to bake AXP717 if the conditions specified in Section 8.4.2 and Section 8.4.3 have not been exceeded. It is necessary to bake AXP717 if any condition specified in Section 8.4.2 and Section 8.4.3 have been exceeded.

Table 8-6 Baking Conditions

Surrounding	Condition	Note
Nitrogen	Tray: 125℃/8 hours Tape: 60℃/72 hours	Recommended condition. It is recommended to bake once, no more than three times.

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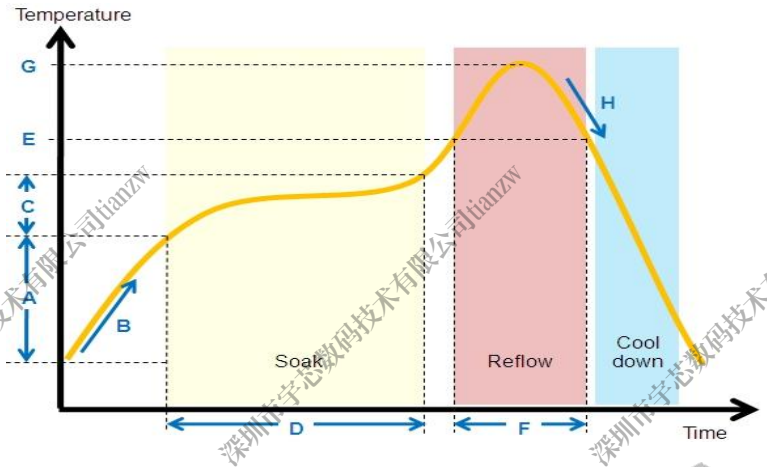
9 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

The following figure shows the typical reflow profile of AXP717 device sample.

Figure 9-1 AXP717 Typical Reflow Profile



Reflow profile conditions of AXP717 device sample is given in the following table.

Table 9-1 AXP717 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25℃ -> 150℃
B	Preheat ramp up rate	1.5~2.5 ℃ /sec
C	Soak temperature range	150℃ -> 190℃
D	Soak time	80~110 sec
E	Liquidus temperature	217℃
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250℃
H	Cool down temperature rate	≤4℃ /sec

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