V3X Datasheet

Single-Core Application Processor

Version 1.0

July 19, 2021

Revision History

Version	Date	Description
V1.0	2021-07-19	Initial release version

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1. Overview

The V3X integrates a single ARM Cortex™-A7 CPU that operates at speed up to 1GHz with supporting peripherals. A 128MB DDR3 is highly integrated in the V3X. The processor has optimized external memory interfaces to SPI NAND/ Nor flash, SD/MMC.

Dedicated video engine and audio subsystem are included to provide an advanced multimedia applications and services. Video Engine supports multi-format such as H.264 encoder by 1080p@60fps, H.264 decoder by 1080p@60fps, JPEG/MJPEG decoder by 1080p@30fps. Audio subsystem includes audio codec with dedicated hardware. To enrich camera feature, V3X equips an 8M HawkView™ ISP with advanced features like spatial de-noise, chrominance de-noise, zone-based AE/AF/AWB statistics, black level correction, lens shading correction, color correction and anti-flick detection statistics.

To reduce total system cost and enhance overall functionality, V3X has a broad range of hardware peripherals such as DMA, Timers, GPIO, UART, SPI, USB HS/FS OTG , TWI, EMAC etc.

2. Feature

2.1. CPU Architecture

- Single-Core ARM Cortex™ –A7 processor
- Thumb-2 Technology
- Support NEON Advanced SIMD(single instruction multiple data)instruction for acceleration of media and signal processing functions
- Support Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- 32KB L1 Instruction cache and 32KB L1 Data cache
- 128KB L2 cache

2.2. Memory Subsystem

Boot ROM

- On -chip memory
- Size:32KB
- Support system boot from the following device:
  - SPI Nor flash
  - SPI Nand flash
  - SD/TF card
  - eMMC flash
- Support system code download through USB OTG

SDRAM

- SIP 128MB DDR3

SD/MMC Interface

- Up to three SD/MMC controllers
- 1/4/8-bit SD,SDIO,MMC mode
- Complies with eMMC standard specification V4.41, SD physical layer specification V2.0, SDIO card specification V2.0
- Support hardware CRC generation and error detection
- Support block size from 1 to 65535 bytes

2.3. System Peripherals

Timer

- Three on-chip timers with interrupt-based operation
- One watchdogs to generate reset signal or interrupts
- 33 bits Audio/Video Sync(AVS) Counter
- 24MHz or Internal OSC clock input

High Speed Timer

- Up to two high speed timers

- Counters up to 56 bits
- Clock source is synchronized with AHB1 clock, much more accurate than other timers

RTC

- Time, calendar
- Counters second, minutes, hours, day, week, month and year with leap year generator
- Alarm: general alarm and weekly alarm
- One 32KHz fanout

GIC

- Support 16 SGIs(Software Generated Interrupt), 16 PPIs(Private Peripheral Interrupt) and 125 SPIs(Shared Peripheral Interrupts)

DMA

- Up to 8-channel DMA
- Flexible data width of 8/16/32 bits
- Support linear and IO address modes
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

CCU

- 9 PLLs
- One on-chip RC oscillator
- One 24MHz oscillator
- One 32.768KHz external oscillator
- Clock management: clock gating ,clock enabling to the device modules, clock reset, clock generation, clock division

PWM

- Up to two PWM channels
- Support outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency

LRADC

- 6-bit resolution
- 1x channel
- Support hold key and continuous key
- Support single key, normal key and continuous key

Security Engine

- Crypto engine
  - Support AES 128/192/256-bits with ECB,CBC,CTS,CTR mode
  - Support DES/TDES with ECB,CBC,CTR mode
  - Support SHA1 and MD5
  - 160-bits hardware PRNG with 175-bits seed
- 256-bits EFUSE

2.4. Display Subsystem

DE2.0

- Output size up to 1024x1024
- Support three alpha blending channel for main display
- Support four overlay layers in each channel, and has a independent scale
- Support potter-duff compatible blending operation
- Support input format YUV422/ YUV420/ YUV411/ ARGB8888/ XRGB8888/ RGB888/ ARGB4444/ ARGB1555/ RGB 565

Display Output

- Support LVDS interface with single link, up to 1024x768@60fps
- Support RGB interface with DE/SYNC mode, up to 1024x768@60fps
- Support serial RGB/dummy RGB/CCIR656 interface, up to 800x480@60fps
- Support i80 interface with 18/16/9/8 bit, support TE, up to 800x480@60fps
- Support pixel format: RGB888, RGB666 and RGB565
- Dither function from RGB666/RGB565 to RGB888
- Gamma correction with R/G/B channel independence

2.5. Video Engine

Video Decoding

- Support video decoder for H.264 and JPEG/MJPEG
- Support H.264 BP/MP/HP up to 1080p@60fps
- Support H.264 output formats :NV21,NV12,YU12,YV12
- Support JPEG/MJPEG up to 1080p@30fps

Video Encoding

- Support H.264 video encoding up to 1080p@60fps, 720p@120fps
- JPEG baseline: picture size up to 8192x8192
- Support input picture size up to 4800x4800
- Support input formats: YU12/YV12/NV12/NV21/YUYV/YVYU/UYVY/VYUY
- Support Alpha blending
- Support thumb generation
- Support 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Support rotated input

2.6. Image Subsystem

Image Input

- Support 8/10/12-bits CMOS sensor parallel interface
- Support 8bit CCIR656 protocol for NTSC and PAL
- Support ITU-R BT 1120 protocol for HD-CIF system
- Support 16bit interface with separate syncs
- Support Format:
  - YUV422-8/10 bit
  - RAW-8/10/12bit

- Performance:
  - Still capture resolution up to 5M with parallel interface
  - Video capture resolution up to 1080p@30fps with parallel interface

ISP

- Support input formats:8/10-bits RAW RGB,8-bits YCbCr
- Support output formats: YCbCr420 semi-planar,YCrCb420 semi-planar, YCbCr422 semi-planar,YCrCb422 semi-planar,YUV420 planar,YUV422 planar
- Support image mirror flip and rotation
- Support two output channels
- Speed up to 8MPixels@24fps
- Defect pixel correction
- Super lens shading correction
- Anisotropic non-linear Bayer interpolation with false color suppression
- Programmable color correction
- Advanced contrast enhance and sharping
- Advanced saturation adjust
- Advanced spatial(2D) de-noise filter
- Advanced chrominance noise reduction
- Zone-based AE/AF/AWB statistics
- Anti-flick detection statistics
- Histogram statistics

2.7. Audio Subsystem

Audio Codec

- Two audio digital-to-analog(DAC) channels
- Support analog/digital volume control
- Support Dynamic Range Controller adjusting the DAC playback output(DRC)
- Stereo Headphone output

2.8. External Peripherals

USB

- One USB 2.0 OTG controller with PHY
- Complies with USB2.0 Specification
- Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps) in host mode
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0,and the Open Host Controller Interface(OHCI) Specification,Version 1.0a for host mode
- Up to 8 User-Configurable Endpoints in device mode
- Support point-to-point and point-to-multipoint transfer in both host and peripheral mode

Ethernet

- Integrated an internal 10/100M PHY
- Support 10/100Mbps data transfer rate

- Support full-duplex and half-duplex operation
- Support linked-list descriptor list structure
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Support a variety of flexible address filtering modes

UART

- Up to three UART controllers
- 64-Bytes Transmit and receive data FIFOs for all UART
- Compliant with industry-standard 16550 UARTs
- Support Infrared Data Association (IrDA) 1.0 SIR

SPI

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Mode0~3 supported for both transmit and receive operations
- Support single and dual read mode
- Two 64-Bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation
- SPI Clock (SPI_CLK) configurable

TWI

- Up to Two Wire Interface (TWI)controllers
- Support Standard mode (up to 100K bps) and Fast mode(up to 400K bps)
- Master/Slave configurable
- Allows 10-bit addressing transactions

2.9. Package

- eLQFP128，16mm*16mm，0.4mm Pitch

3. Block Diagram

The following figure shows the block diagram of V3X processor.

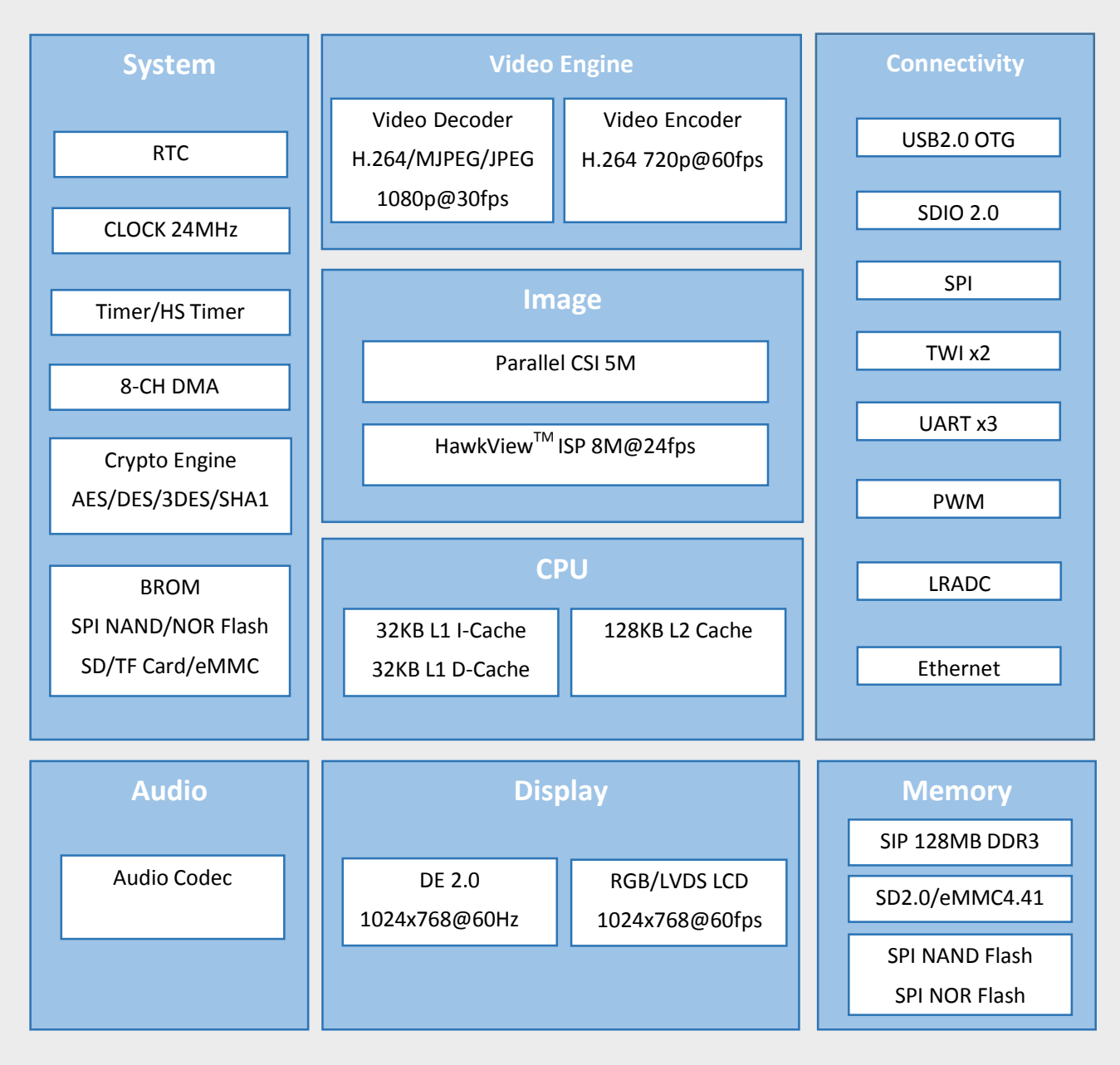


Figure 3-1. V3X Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of V3X Pins from seven aspects.

[1].Pin#: Package pin numbers associated with each signals.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

[4].Pin Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled by software.

[6].Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.

[7].Power Supply: The voltage supply for the terminal's IO buffers.

Table 4-1. Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
DRAM						
75	ZQ	AI	Z	NA	NA	VCC-DRAM
71	SVREF	AI	Z	NA	NA	VCC-DRAM
67	DVREF	AI	Z	NA	NA	VCC-DRAM
68,69,70,72,73,74	VCC-DRAM	P	NA	NA	NA	NA
GPIO B						
42	PB0	I/O	Z	PU/PD	20	VCC-IO
43	PB1	I/O	Z	PU/PD	20	VCC-IO
44	PB4	I/O	Z	PU/PD	20	VCC-IO
45	PB5	I/O	Z	PU/PD	20	VCC-IO
46	PB6	I/O	Z	PU/PD	20	VCC-IO
47	PB7	I/O	Z	PU/PD	20	VCC-IO
48	PB8	I/O	Z	PU/PD	20	VCC-IO
49	PB9	I/O	Z	PU/PD	20	VCC-IO

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
GPIO C						
52	PC0	I/O	Z	PU/PD	20	VCC-IO
53	PC1	I/O	Z	PU/PD	20	VCC-IO
54	PC2	I/O	Z	PU/PD	20	VCC-IO
55	PC3	I/O	Z	PU/PD	20	VCC-IO
56	PC4	I/O	Z	PU/PD	20	VCC-IO
57	PC5	I/O	Z	PU/PD	20	VCC-IO
59	PC6	I/O	Z	PU/PD	20	VCC-IO
60	PC7	I/O	Z	PU/PD	20	VCC-IO
61	PC8	I/O	Z	PU/PD	20	VCC-IO
62	PC9	I/O	Z	PU/PD	20	VCC-IO
63	PC10	I/O	Z	PU/PD	20	VCC-IO
GPIO D						
16	PD12	I/O	Z	PU/PD	20	VCC-IO
15	PD13	I/O	Z	PU/PD	20	VCC-IO
18	PD14	I/O	Z	PU/PD	20	VCC-IO
17	PD15	I/O	Z	PU/PD	20	VCC-IO
21	PD16	I/O	Z	PU/PD	20	VCC-IO
20	PD17	I/O	Z	PU/PD	20	VCC-IO
23	PD18	I/O	Z	PU/PD	20	VCC-IO
22	PD19	I/O	Z	PU/PD	20	VCC-IO
25	PD20	I/O	Z	PU/PD	20	VCC-IO
24	PD21	I/O	Z	PU/PD	20	VCC-IO
GPIO E						
41	PE0	I/O	Z	PU/PD	20	VCC-IO
40	PE1	I/O	Z	PU/PD	20	VCC-IO
39	PE2	I/O	Z	PU/PD	20	VCC-IO
38	PE3	I/O	Z	PU/PD	20	VCC-IO
37	PE4	I/O	Z	PU/PD	20	VCC-IO
36	PE5	I/O	Z	PU/PD	20	VCC-IO
35	PE6	I/O	Z	PU/PD	20	VCC-IO
34	PE7	I/O	Z	PU/PD	20	VCC-IO
33	PE8	I/O	Z	PU/PD	20	VCC-IO
32	PE9	I/O	Z	PU/PD	20	VCC-IO
29	PE10	I/O	Z	PU/PD	20	VCC-IO
28	PE11	I/O	Z	PU/PD	20	VCC-IO
27	PE12	I/O	Z	PU/PD	20	VCC-IO
13	PE13	I/O	Z	PU/PD	20	VCC-IO
12	PE14	I/O	Z	PU/PD	20	VCC-IO
11	PE15	I/O	Z	PU/PD	20	VCC-IO
10	PE16	I/O	Z	PU/PD	20	VCC-IO
9	PE17	I/O	Z	PU/PD	20	VCC-IO

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
8	PE18	I/O	Z	PU/PD	20	VCC-IO
6	PE19	I/O	Z	PU/PD	20	VCC-IO
5	PE20	I/O	Z	PU/PD	20	VCC-IO
4	PE21	I/O	Z	PU/PD	20	VCC-IO
3	PE22	I/O	Z	PU/PD	20	VCC-IO
2	PE23	I/O	Z	PU/PD	20	VCC-IO
1	PE24	I/O	Z	PU/PD	20	VCC-IO
GPIO F						
102	PF0	I/O	Z	PU/PD	20	VCC-IO
101	PF1	I/O	Z	PU/PD	20	VCC-IO
100	PF2	I/O	Z	PU/PD	20	VCC-IO
98	PF3	I/O	Z	PU/PD	20	VCC-IO
97	PF4	I/O	Z	PU/PD	20	VCC-IO
96	PF5	I/O	Z	PU/PD	20	VCC-IO
95	PF6	I/O	Z	PU/PD	20	VCC-IO
GPIO G						
128	PG0	I/O	Z	PU/PD	20	VCC-IO
127	PG1	I/O	Z	PU/PD	20	VCC-IO
126	PG2	I/O	Z	PU/PD	20	VCC-IO
125	PG3	I/O	Z	PU/PD	20	VCC-IO
124	PG4	I/O	Z	PU/PD	20	VCC-IO
123	PG5	I/O	Z	PU/PD	20	VCC-IO
122	PG6	I/O	Z	PU/PD	20	VCC-IO
121	PG7	I/O	Z	PU/PD	20	VCC-IO
120	PG8	I/O	Z	PU/PD	20	VCC-IO
119	PG9	I/O	Z	PU/PD	20	VCC-IO
RTC&PLL						
92	RTC-VIO	P	-	-	-	-
91	X32KIN	A	-	-	-	-
90	X32KOUT	A	-	-	-	-
93	VCC-RTC	P	-	-	-	-
78	VCC-PLL	P	-	-	-	-
System Control						
94	RESET	I	-	-	-	-
77	X24MIN	A	-	-	-	-
76	X24MOUT	A	-	-	-	-
USB						
106	VCC-USB	P	-	-	-	-
104	USB-DM	A	-	-	-	-
105	USB-DP	A	-	-	-	-
Audio Codec						
108	AVCC	P	-	-	-	-

Pin#[1]	Pin Name[2]	Type[3]	Pin Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
109	AGND	G	-	-	-	-
110	VRA1	A	-	-	-	-
111	VRA2	A	-	-	-	-
112	HPOUTR	A	-	-	-	-
113	HPOUTL	A	-	-	-	-
114	HPVCCIN	P	-	-	-	-
115	HPVCCBP	A	-	-	-	-
116	HPCOM	A	-	-	-	-
EPHY						
79	EPHY-LINK-LED	O	-	-	-	-
80	EPHY-SPD-LED	O	-	-	-	-
83	VDD-EPHY	P	-	-	-	-
84	EPHY-RXN	A	-	-	-	-
85	EPHY-RXP	A	-	-	-	-
86	EPHY-TXN	A	-	-	-	-
87	EPHY-TXP	A	-	-	-	-
88	VCC- EPHY	P	-	-	-	-
89	EPHY-RTX	A	-	-	-	-
LRADC						
107	LRADC0	A	-	-	-	-
Power						
7, 19, 31, 50, 64, 99, 118	VCC-IO	P	-	-	-	-
14, 65, 66, 82, 103, 117	VDD-SYS	P	-	-	-	-
26, 30, 51, 58	VDD-CPU	P	-	-	-	-
EPAD	GND	P				
TEST						
TEST	TEST	A	-	-	-	-

4.2. GPIO Multiplexing Functions

The following table provides a description of the V3X GPIO multiplexing functions.

Table 4-2. Multiplexing Functions

Pin Name	GPIO Group	IO Type	Function 2	Function3	Function 4	Function 5	Function 6
PB0	GPIOB	I/O	UART2_TX				PB_EINT0
PB1		I/O	UART2_RX				PB_EINT1
PB4		I/O	PWM0				PB_EINT4
PB5		I/O	PWM1				PB_EINT5
PB6		I/O	TWI0_SCK				PB_EINT6
PB7		I/O	TWI0_SDA				PB_EINT7
PB8		I/O	TWI1_SCK	UART0_TX			PB_EINT8
PB9		I/O	TWI1_SDA	UART0_RX			PB_EINT9
PC0	GPIOC	I/O	SDC2_CLK	SPI0_MISO			
PC1		I/O	SDC2_CMD	SPI0_CLK			
PC2		I/O	SDC2_RST	SPI0_CS			
PC3		I/O	SDC2_D0	SPI0_MOSI			
PC4		I/O	SDC2_D1				
PC5		I/O	SDC2_D2				
PC6		I/O	SDC2_D3				
PC7		I/O	SDC2_D4				
PC8		I/O	SDC2_D5				
PC9		I/O	SDC2_D6				
PC10		I/O	SDC2_D7				
PD12	GPIOD	I/O		LVDS_VP0			
PD13		I/O		LVDS_VN0			
PD14		I/O		LVDS_VP1			
PD15		I/O		LVDS_VN1			
PD16		I/O		LVDS_VP2			
PD17		I/O		LVDS_VN2			
PD18		I/O		LVDS_VPC			
PD19		I/O		LVDS_VNC			
PD20		I/O		LVDS_VP3			
PD21		I/O		LVDS_VN3			
PE0	GPIOE	I/O	CSI_PCLK	LCD_CLK			
PE1		I/O	CSI_MCLK	LCD_DE			
PE2		I/O	CSI_HSYNC	LCD_HSYNC			
PE3		I/O	CSI_VSYNC	LCD_VSYNC			
PE4		I/O	CSI_D0	LCD_D2			
PE5		I/O	CSI_D1	LCD_D3			
PE6		I/O	CSI_D2	LCD_D4			
PE7		I/O	CSI_D3	LCD_D5			
PE8		I/O	CSI_D4	LCD_D6			

Pin Name	GPIO Group	IO Type	Function 2	Function3	Function 4	Function 5	Function 6
PE9		I/O	CSI_D5	LCD_D7			
PE10		I/O	CSI_D6	LCD_D10			
PE11		I/O	CSI_D7	LCD_D11			
PE12		I/O	CSI_D8	LCD_D12			
PE13		I/O	CSI_D9	LCD_D13			
PE14		I/O	CSI_D10	LCD_D14			
PE15		I/O	CSI_D11	LCD_D15			
PE16		I/O	CSI_D12	LCD_D18			
PE17		I/O	CSI_D13	LCD_D19			
PE18		I/O	CSI_D14	LCD_D20			
PE19		I/O	CSI_D15	LCD_D21			
PE20		I/O	CSI_FIELD				
PE21		I/O	CSI_SCK	TWI1_SCK	UART1_TX		
PE22		I/O	CSI_SDA	TWI1_SDA	UART1_RX		
PE23				LCD_D22	UART1_RTS		
PE24				LCD_D23	UART1_CTS		
PF0	GPIOF	I/O	SDC0_D1				
PF1		I/O	SDC0_D0				
PF2		I/O	SDC0_CLK	UART0_TX			
PF3		I/O	SDC0_CMD				
PF4		I/O	SDC0_D3	UART0_RX			
PF5		I/O	SDC0_D2				
PF6		I/O					
PG0	GPIOG	I/O	SDC1_CLK				PG_EINT0
PG1		I/O	SDC1_CMD				PG_EINT1
PG2		I/O	SDC1_D0				PG_EINT2
PG3		I/O	SDC1_D1				PG_EINT3
PG4		I/O	SDC1_D2				PG_EINT4
PG5		I/O	SDC1_D3				PG_EINT5
PG6		I/O	UART1_TX				PG_EINT6
PG7		I/O	UART1_RX				PG_EINT7
PG8		I/O	UART1_RTS				PG_EINT8
PG9		I/O	UART1_CTS				PG_EINT9

4.3. Detailed Pin/Signal Description

Table 4-3 shows the detailed function of every pin/signal based on the different interface.

Table 4-3.Detailed Pin Description

Pin/Signal Name	Description	Type
DRAM		
ZQ	DDR calibrated resistor	AI

Pin/Signal Name	Description	Type
SVREF	DRAM Reference Voltage Input	AI
DVREF	DRAM Reference Voltage Input	AI
VCC-DRAM	DRAM Power Supply	P
System Control		
RESET	RESET Signal	I
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
RTC		
RTC-VIO	Internal LDO Output Bypass	P
X32KIN	Clock input of 32768Hz Crystal	AI
X32KOUT	Clock output of 32768Hz Crystal	AO
VCC-RTC	RTC Power Supply	P
VCC-PLL	PLL Power Supply	P
USB		
VCC-USB	USB Power Supply	P
USB-DM	USB data signal DM	AI/O
USB-DP	USB data signal DP	AI/O
LRADC		
LRADC0	ADC input for key0	AI
Audio Codec		
AVCC	Power Supply for Analog Part	P
AGND	Ground for Analog Part	G
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
HPOUTR	Headphone Output Right Channel	AO
HPOUTL	Headphone Left Right Channel	AO
HPVCCIN	Headphone VCC Input	P
HPVCCBP	Headphone VCC Bypass	AO
HPCOM	Headphone Common Reference Output	AO
EPHY		
EPHY-LINK-LED	EPHY LINK Up/Down Indicator LED	AI/O
EPHY-SPD-LED	EPHY 10M/100M Indicator LED	AI/O
VDD-EPHY	Analog Power Supply for EPHY	P
EPHY-RXN	Transceiver Negative Output/Input	AI/O
EPHY-RXP	Transceiver Positive Output/Input	AI/O
EPHY-TXN	Transceiver Negative Output/Input	AI/O
EPHY-TXP	Transceiver Positive Output/Input	AI/O
VCC- EPHY	Analog Power Supply for EPHY	P
EPHY-RTX	EPHY External Resistance to Ground	AI
SD/MMC		
SDC0_CMD	Command Signal for SD/TF Card	I/O
SDC0_CLK	Clock for SD/TF Card	O
SDC0_D[3:0]	Data Input and Output for SD/TF Card	I/O

Pin/Signal Name	Description	Type
SDC1_CMD	Command Signal for SD/TF Card / SDIO	I/O
SDC1_CLK	Clock for SD/TF Card / SDIO	O
SDC1_D[3:0]	Data Input and Output for SD/TF Card / SDIO	I/O
SDC2_CMD	Command Signal for SD/TF Card / EMMC	I/O
SDC2_CLK	Clock for SD/TF Card / EMMC	O
SDC2_D[7:0]	Data Input and Output for SD/TF Card / EMMC	I/O
Interrupt		
PB_EINT[1:0]\[9:4]	GPIO B Interrupt	I
PG_EINT[24:0]	GPIO G Interrupt	I
PWM		
PWM0	Pulse Width Modulation output channel0	O
PWM1	Pulse Width Modulation output channel1	O
LCD		
LCD_D[23:0]	LCD Data Output	O
LCD_CLK	LCD Clock Signal	O
LCD_DE	LCD Data Enable	O
LCD_HSYNC	LCD Horizontal SYNC	O
LCD_VSYNC	LCD Vertical SYNC	O
LVDS		
LVDS_VP[3:0]	LVDS Data Positive Signal Output	AO
LVDS_VN[3:0]	LVDS Data Negative Signal Output	AO
LVDS_VPC	LVDS Clock Positive Signal Output	AO
LVDS_VNC	LVDS Clock Negative Signal Output	AO
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[15:0]	CSI Data Input	I
CSI_SCK	CSI Command Serial Clock Signal	I/O
CSI_SDA	CSI Command Serial Data Signal	I/O
CSI_FIELD	CSI Field Signal	I/O
SPI		
SPI0_CS	SPI Chip Select signal, low active	I/O
SPI0_CLK	SPI Clock signal	I/O
SPI0_MOSI	SPI Master data Out, Slave data In	I/O
SPI0_MISO	SPI Master data In, Slave data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I

Pin/Signal Name	Description	Type
UART1_CTS	UART1 Data Clear To Send	I
UART1_RTS	UART1 Data Request To Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear To Send	I
UART2_RTS	UART2 Data Request To Send	O
TWI		
TWI0_SCK	TWI0 Serial Clock Signal	I/O
TWI0_SDA	TWI0 Serial Data Signal	I/O
TWI1_SCK	TWI1 Serial Clock Signal	I/O
TWI1_SDA	TWI1 Serial Data Signal	I/O
Power		
VCC-IO	IO Power	P
VDD-SYS	System Power	P
VDD-CPU	CPU Power	P
GND	Ground for Power and Signals	P
TEST		
TEST	Connect to Ground	-

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Functional operation of the device at these or any other conditions beyond the absolute maximum ratings listed in Table 5-1 can cause permanent damage to the device.

Table 5-1.Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage Temperature	-40	125	°C
AVCC	Power Supply for Analog part	-0.3	3.6	V
EPHY-VCC	Power Supply for EPHY	-0.3	3.6	V
EPHY-VDD	Power Supply for EPHY	-0.3	1.4	V
HPVCCIN	Power Supply for Headphone	-0.3	3.6	V
VCC-IO	Power Supply for IO	-0.3	3.6	V
VCC-PLL	Power Supply for PLL	-0.3	3.6	V
VCC-RTC	Power Supply for RTC	-0.3	3.6	V
VCC-USB	Power Supply for USB	-0.3	3.6	V
VCC-DRAM	Power Supply for DDR3 DRAM	-0.3	1.65	V
VCC-CPU	Power Supply for CPU	-0.3	1.4	V
VCC-SYS	Power Supply for System	-0.3	1.4	V
$I_{I/O}$	In/Out current for input and output	-40	40	mA

5.2. Recommended Operating Conditions

All V3X modules are used under the operating Conditions contained in Table 5-2.

Table 5-2.Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_a	Ambient Temperature	-20	-	85	°C
AVCC	Power Supply for Analog part	2.8	3.0	3.3	V
EPHY-VCC	Power Supply for EPHY	2.8	3.3	3.6	V
EPHY-VDD	Power Supply for EPHY	1.0	1.1	1.2	V
HPVCCIN	Power Supply for Headphone	3.0	3.3	3.6	V
VCC-IO	Power Supply for IO	1.7	1.8~3.3	3.6	V
VCC-PLL	Power Supply for PLL	2.7	3.0	3.3	V
VCC-RTC	Power Supply for RTC	3.0	3.3	3.6	V
VCC-USB	Power Supply for USB	3.0	3.3	3.45	V
VCC-DRAM	Power Supply for DRAM	1.425	1.5	1.575	V
VCC-CPU	Power Supply for CPU	-	1.2	-	V
VCC-SYS	Power Supply for System	-	1.2	-	V

5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of V3X.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7*VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3*VCC-IO	V
R_{PU}	Input Pull-up Resistance	50	100	150	KΩ
R_{PD}	Input Pull-down Resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. Oscillator Electrical Characteristics

The V3X contains two oscillators:a 24MHz oscillator and a 32768Hz oscillator.Each oscillator requires a specific crystal.The V3X device operation requires the following two input clocks:
The 32.768kHz frequency is used for low frequency operation.
The 24.000MHz frequency is used to generate the main source clock of the V3X device.

Table 5-4. 24MHz Oscillator Characteristics

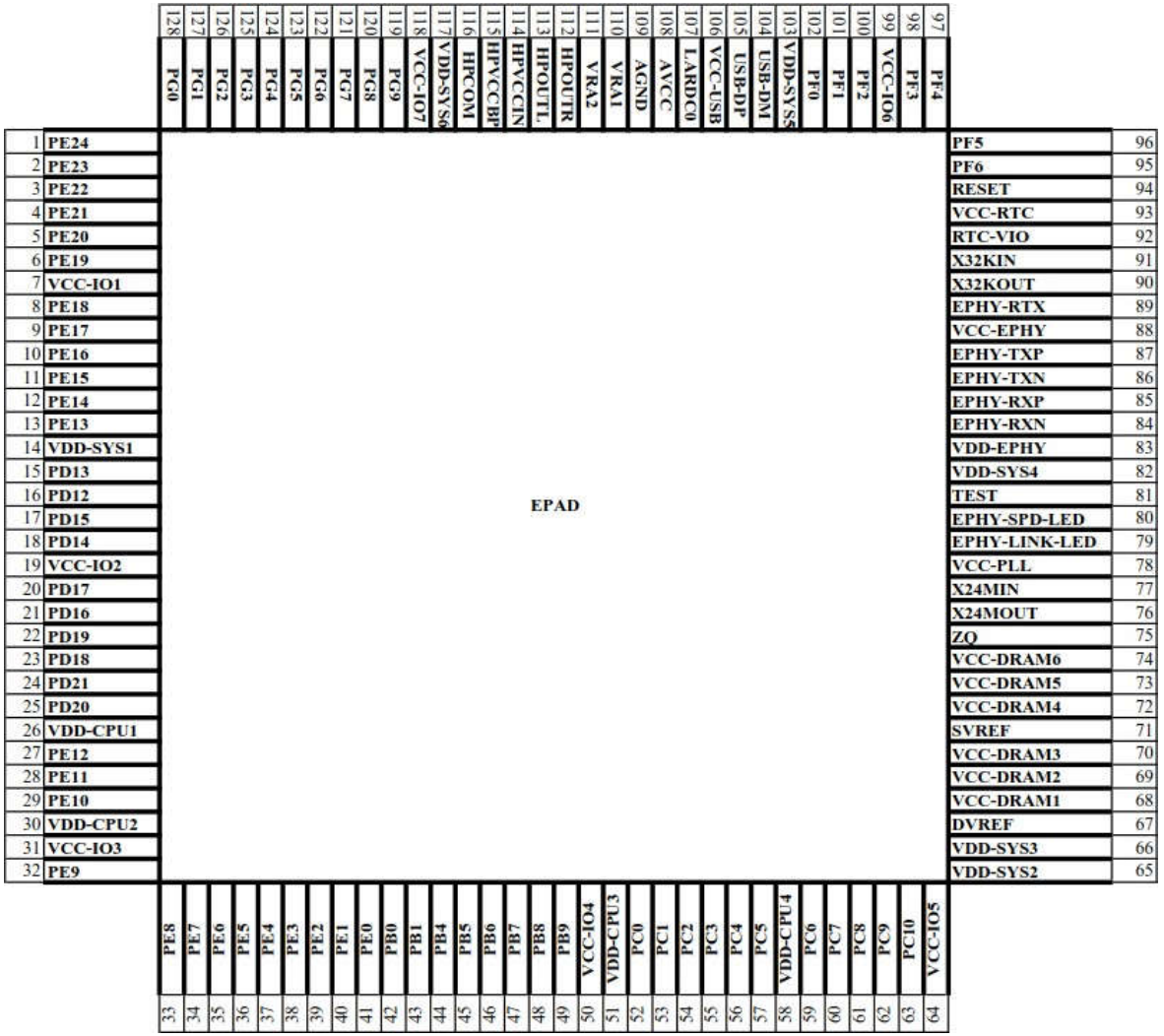
Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–

Table 5-5. 32.768kHz Oscillator Characteristics

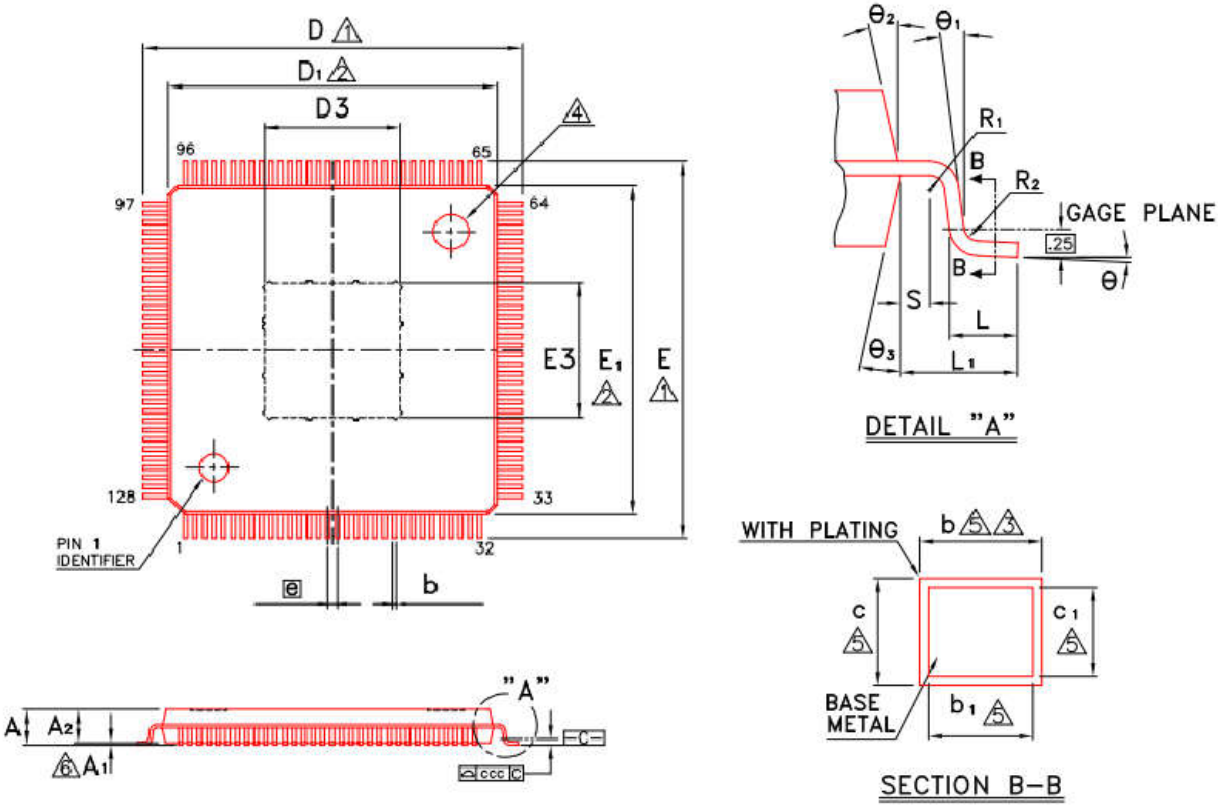
Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	32768	–	Hz
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–

6. Pin Assignment

6.1. Pin Map



6.2. Package Outline Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		
ccc	0.08			0.003		