T7 User Manual

Revision 1.0

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Revision History

Revision	Date	Description
1.0	May.11, 2018	Initial release version

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Chapter 1 About This Document

1.1. Purpose

This document describes the features,logical structures,functions,operating modes,and related registers of each module about T7. For details about the interface timings and related parameters ,the pins, pin usages, performance parameters, and package dimension ,please refer to the ***Allwinner T7 Datasheet***.

1.2. Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Programmers in writing code or modifying the Allwinner provided code

1.3. Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

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1.4. Notes

1.4.1. Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete. Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

1.4.2. Reset Value Conventions

In the register definition tables:

If other column value in a bit or multiple bits row is "/" , that this bit or these multiple bits are unused.

If the default value of a bit or multiple bits is "UDF", that the default value is undefined.

1.4.3. Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency,data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register

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		description is excluded.)
X	00X,XX1	In data expression,X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

1.5. Acronyms and Abbreviations

The following table contains acronyms and abbreviations used in this document.

ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
AWB	Automatic White Balance
BROM	Boot ROM
CIR	Consumer Infrared
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array

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FEL	Fireware Exchange Launch
FIFO	First In First Out
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HiSPI	High-Speed Serial Pixel Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LRADC	Analog to Digital Converter for Key
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OSD	On-Screen Display
OTP	One Time Programmable
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
R	Read only/non-Write
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface

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ROM	Read Only Memory
RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Sychronous Dynamic Random Access Memory
SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TFBGA	Thin Fine Ball Grid Array
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

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Chapter 2 Product Description

2.1. Overview

The T7 processor represents Allwinner's latest achievement in smart automotive processors. The processor is ideal for applications that require 3D graphics, advanced video processing, rich user interfaces, lower power consumption and higher system integration. It will bring the advanced consumer electronics experiences into the vehicles of the future, and achieve a good balance of high performance, drive safety, drive video record and device connectivity.

The T7 processor has some very exciting features:

- **CPU**: T7 is based on Hexa-core Cortex™-A7 CPU architecture with 1024KB L2 cache.
- **CPUS**: CPUS is a heterogeneous processor independent of ARM. It is mainly used for standby management, including power management, IO control, peripheral status monitoring and so on. And it is low power consumption.
- **GPU**: T7 adopts the extensively implemented and technically mature Mali400 MP4. It is applied to identify the real-time traffic, and provides possibilities for automatic drive.
- **Video Engine**: High-definition H.265 decoder is up to 1080p@60fps and H.265 encoder is up to 1080p@60fps.
- **Camera**: Supports 2 individual parallel CSI interfaces, 4-channel TVIN and 2 individual MIPI-CSI, which can easily finish multi-channel video recording.
- **EVE**: Integrated Embedded Visual Engine(EVE) can detect vehicle, lane, pedestrian, traffic sign, and traffic signals. Detection speed is up to 30fps for VGA images.
- **ISP**: T7 equips two 4M ISP with advanced features like better 2D/3D de-noise, contrast enhancement, AE/AF/AWB statistics, color correction, gamma correction, sharpening, and anti-flick detection statistics, etc.
- **Display**: Content can be displayed on 4-lane MIPI DSI displays, or RGB panel, or LVDS panel.TV-out interface for TV encoder is also supported.
- **Audio**: Integrated analog audio codec supports 2-ch high-quality stereo playback DAC, one stereo line-out output, and one differential phone-out output; 3-ch high-quality stereo recording ADC, three differential microphone inputs, and one stereo line-in input. Digital audio interfaces support I2S/PCM for connecting to an external audio codec, OWA for connecting to external amplifier, and DMIC for digital audio recording.
- **Memory**: Supports external memory interfaces to NAND Flash, SD/eMMC, Nor Flash and SDRAM port. SDRAM port can be configured to support DDR3, DDR3L, LPDDR2, LPDDR3.
- **Peripherals**: To reduce total system cost, T7 has a broad range of hardware peripherals to meet the flexible peripheral configuration requirements such as UART, SPI, CIR_RX, USB2.0 OTG, USB2.0 HOST, TWI, etc.
- **Reliability**: Pass the AEC-Q100 Grade3 Certification test.

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2.2. Features

2.2.1. CPU

- Hexa-core ARM Cortex™-A7 Processor
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- Large Physical Address Extensions(LPAE)
- 32KB L1 Instruction cache and 32KB L1 Data cache for per CPU
- 1024KB L2 cache shared

2.2.2. GPU

- Mali400 MP4, up to 400MHz
- Embedded four pixel processors capable of processing 1600M pix/sec
- Built-in MMU for each processor and L2 cache with 128KB size
- Supports OpenGL ES1.1/2.0 and OpenVG1.1 3D graphics standard

2.2.3. Internal Memory

2.2.3.1. Boot ROM

- Supports eMMC, SD card, Nand flash, SPI Nor flash and SPI Nand flash
- Supports mandatory upgrade process through SMHC0 and USB
- Supports normal Boot and secure Boot
- Boot select pin(FEL) is used to select boot process: jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process
- Supports super standby wakeup process
- Supports Pin Boot select
- Supports eFuse Boot select

2.2.4. External Memory Interfaces

2.2.4.1. SDRAM

- Compatible with JEDEC standard DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- DDR3/DDR3L interface with the maximum frequency of 800MHz
- LPDDR3 interface with the maximum frequency of 672MHz

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- LPDDR2 interface with the maximum frequency of 533MHz
- Up to 3GB memory capacity
- 32-bit data bus width
- Supports Memory Dynamic Frequency Scale(MDFS)

2.2.4.2. NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 2 ready_busy signals
- Supports SLC/MLC/TLC flash and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

2.2.4.3. SMHC

- Up to four SMHC controllers(SDC0,SDC1,SDC2,SDC3)
- Compatible with eMMC standard specification V5.0, SD physical layer specification V2.0 ,SDIO card specification V3.0
- 1-/4-/8-bit bus width, only SDC2 supports up to 8-bit,shared with NAND flash pins
- Embedded special DMA to do data transfer
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.2.5. Video Engine

2.2.5.1. Video Decoder

- Supports video decoding up to 1080p@60fps
- Supports multi-formats:
  - H.265 MP/L4.1: 1080p@60fps
  - H.264 BP/MP/HP Level4.2: 1080p@45fps
  - H.263 BP: 1080p@45fps
  - MPEG4 SP/ASP L5: 1080p@45fps
  - MPEG2 MP/HL: 1080p@45fps
  - MPEG1 MP/HL: 1080p@45fps
  - xvid: 1080p@45fps
  - Sorenson Spark: 1080p@45fps
  - VP8: 1080p@45fps
  - AVS/AVS+: 1080p@45fps
  - WMV9/VC1: 1080p@30fps

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- JPEG: 16384 x 16384@45Mbps

2.2.5.2. Video Encoder

- Supports H.265 MP video encoding up to 1080p@60fps
- Supports H.264 MP video encoding up to 1080p@60fps
- Supports input formats: titled(128x32)/YU12/YV12/NU12/NV12/ARGB/YUYV
- Supports Alpha blending
- Supports Thumb generation
- Supports 4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

2.2.5.3. Display Engine(DE)

- Output size up to 2048x2048
- Four alpha blending channels for main display, two channels for aux display
- Four overlay layers in each channel, and has a independent scaler
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports write back for high efficient dual display and miracast

2.2.5.4. De-interlacer

- Off-line processing mode
- Supports NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined data format
- Input video resolution from 32 x 32 to 2048 x 2048 pixel
- Supports weave/pixel-motion-adaptive de-interlacer method
- Noise reduction function

2.2.5.5. G2D

- Layer size up to 2048 x 2048 pixels
- Horizontal and vertical flip, clockwise 0/90/180/270 degree rotate
- Multiple formats convert function
- Alpha blending, Window clip, BitBlit, and MaskBlit

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2.2.6. Embedded Visual Engine(EVE)

- Detection speed: 30fps for VGA images (working frequency: 300MHz)
- Supports classic HAAR and LBP feature, total feature up to 4000 and 1000 respectively
- Supports 4K input and built-in zoom, extract ROI
- Supports 4 channel integral image, processes 130 million features per second
- Supports up to 3 channel feature calculation
- The minimum resolution of target object in single image detection is 20 x 20

2.2.7. Video Output Interfaces

2.2.7.1. MIPI DSI

- Supports 4 lanes MIPI DSI up to 1920 x 1200@60fps
- 1/2/3/4 data lanes configuration and up to 1Gbit/s per lane
- Supports video mode with sync pulse/sync event, burst mode/command mode
- Pixel format: RGB888, RGB666, RGB666 packed, and RGB565

2.2.7.2. LVDS

- Supports LVDS interface up to 1920 x 1200@60fps
- Dual link LVDS mode output, up to 1920 x 1200@60fps
- Single link LVDS mode output, up to 1366 x 768@60fps
- Multiplex pin with RGB interface

2.2.7.3. RGB

- Supports 18-bit RGB interface with DE/SYNC mode
- Up to 1366 x 768@60fps
- Supports BT656 output
- Supports RGB666 and RGB565 with dither function

2.2.7.4. TVOUT

- Supports 1-ch TV CVBS output
- Supports NTSC and PAL mode
- Plug status auto detecting

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2.2.8. ISP

- Supports 2 individual image signal processor(ISP)
- Adjustable 3A functions, including automatic exposure(AE), automatic white balance(AWB) and automatic focus (AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D/3D denoising
- Sensor build-in WDR, 2F-line base WDR, local tone mapping
- 1/64 to 1x scaling output for 4 channels
- Graphics mirror and flip
- ISP tuning tools for the PC
- Maximum frame rate of 30fps for the 1920 x 2688 resolution

2.2.9. Video Input Interfaces

2.2.9.1. Parallel CSI

- Two individual parallel CSI interfaces, with 16-bit data wide per interface
- Supports 8-,10-,12-,16-bit digital camera(DC) interface
- Supports DDR sample mode
- Supports CCIR656 protocol for NTSC and PAL
- Supports ITU-R BT.656/BT.1120 time-multiplexed format
- Supports 16-bit interface with separate syncs
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution to 1080p@30fps
- Maximum pixel clock for parallel to 148.5MHz

2.2.9.2. MIPI CSI

- Two individual MIPI CSI camera control interfaces
- Supports MIPI-DPHY v1.0 and MIPI-CSI2 v1.0
- Supports virtual channel
- Supports formats: YUV422-8bit/10bit, YUV420-8bit/10bit, RAW-8, RAW-10, RAW-12, RGB888, RGB565
- 1/2/3/4 data lanes configuration and up to 1Gbit/s per lane
- Maximum video capture resolution up to 8M@30fps

2.2.9.3. TVIN

- 4 channel CVBS input or 1 channel YPbPr with 1 channel CVBS
- Supports YPbPr input, 576p/480p/576i/480i
- Supports CVBS input, NTSC and PAL mode
- Supports YUV422, YUV420 format writeback

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- One channel 3D comb filter
- Detection for signal locked and 625 lines
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

2.2.10. Audio Interfaces

2.2.10.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
  - Up to 100±2dB SNR during DAC playback
  - Supports DAC sample rate from 8 kHz to 192 kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Three audio analog-to-digital(ADC) channels
  - Up to 92±2dB SNR during ADC recording
  - Supports ADC sample rate from 8 kHz to 48 kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Two audio analog outputs:
  - One stereo line-out output (LINEOUTL and LINEOUTR)
  - One differential phone-out output (PHONEOUTP and PHONEOUTN)
- Four audio inputs:
  - Three differential microphone inputs (MICIN1P and MICIN1N,MICIN2P and MICIN2N, MICIN3P and MICIN3N)
  - One stereo line-in input (LINEINL and LINEINR)
- Supports analog/digital volume control
- One low-noise analog microphone bias output
- Supports dynamic range controller adjusting the DAC playback and ADC recording

2.2.10.2. I2S/PCM

- Up to three I2S/PCM interfaces
- Compliant with standard Philips Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master and slave mode configured
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 kHz to 192 kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- Supports programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)

2.2.10.3. One Wire Audio (OWA)

- IEC-60958 transmitter and receiver functionality

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- Compatible with S/PDIF protocol
- Supports channel status insertion for the transmitter
- Supports channel status capture on the receiver
- Hardware parity generation on the transmitter
- Hardware parity checking on the receiver

2.2.10.4. DMIC

- Supports up to 8 channels
- Supports sample rate from 8 kHz to 48 kHz

2.2.11. Security Engine

- Encryption and decryption algorithms implemented by using hardware, including AES,DES and 3DES
- Signature and verification algorithms implemented by using hardware, including RSA512,RSA1024,RSA2048
- HASH tamper proofing algorithms implemented by using hardware, including SHA1,SHA256, SHA384, SHA512, HMAC_SHA1 and HMAC_SHA256
- True hardware random number(TRNG) generator and pseudo hardware random number(PRNG) generator
- Integrated 2.5 Kbits efuse storage space

2.2.12. External Peripherals

2.2.12.1. USB

- One USB 2.0 OTG(USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) and Low-Speed(LS,1.5 Mbit/s) in host mode
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) in device mode
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 10 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
  - Supports (8KB+64Bytes) FIFO for EPs(including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- Three USB 2.0 Host(USB1,USB2,USB3), with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) and Low-Speed(LS,1.5 Mbit/s) device
- One USB HSIC, share USB3 controller with one USB 2.0 analog PHY

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2.2.12.2. EMAC

- Compliant with IEEE 802.3-2002 standard
- Supports 10/100/1000 Mbit/s data transfer rates
- Supports MII/RMII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 Kbytes
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 Kbytes of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 Kbytes TXFIFO for transmission packets and 16 Kbytes RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.2.12.3. TWI

- Up to 10 TWIs(7 in CPUX domain, 3 in CPUS domain)
- Software-programmable for Slave or Master
- Supports Repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Supports speeds up to 400 kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

2.2.12.4. UART

- Up to 10 UART controllers(5 in CPUX domain, 5 in CPUS domain)
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 5 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

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2.2.12.5. SPI

- Full-duplex synchronous serial interface
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports mode0, mode1, mode2 and mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 0 bit to 32 bits
- Supports the SPI NAND flash and SPI NOR flash
- Supports standard SPI,dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI

2.2.12.6. CIR_RX

- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.2.12.7. LRADC

- One LRADC controller with 2 input channels
- 6-bit resolution
- Sample rate up to 250Hz
- Supports hold Key and general Key
- Supports normal,continue and single work mode
- Voltage input range between 0 to 2.0V
- Power supply voltage:3.0V, reference voltage:2.0V

2.2.12.8. GPADC

- One general purpose ADC(GPADC) controller with 6 input channels
- 12-bit resolution
- 8-bit effective SAR type A/D converter
- Power supply voltage: 3.0V
- Analog input range: 0 V to 3.0 V
- Maximum sampling frequency: 1 MHz
- Supports data compare and interrupt
- Supports three operation modes
  - Single conversion mode

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- Continuous conversion mode
- Burst conversion mode

2.2.12.9. PWM

- 8 PWM channels(4 PWM pairs)
- Supports pulse,cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform,pulse waveform and complementary pair
- Output frequency range: 0~ 24MHz/100MHz
- Various duty-cycle: 0% ~100%
- Minimum resolution: 1⁄65536
- Interrupt generation of PWM output and capture input

2.2.12.10. TSC

- Supports SPI/SSI interface,interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Supports multiple transport stream packet (188, 192, 204) format
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

2.2.12.11. SCR

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:

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  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

2.2.12.12. RSB™

- Designed and implemented by the Allwinner Technology
- Up to 20MHz speed with ultra low power
- Supports push-pull bus
- Supports host mode and multi-devices
- Programmable output delay of CD signal
- Supports parity check for address and data transmission

2.2.13. Package

- PBGA 547 balls, 0.8mm ball pitch, 21mmx21mm

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2.3. Block Diagram

Figure 2-1 shows the block diagram of the T7 processor.

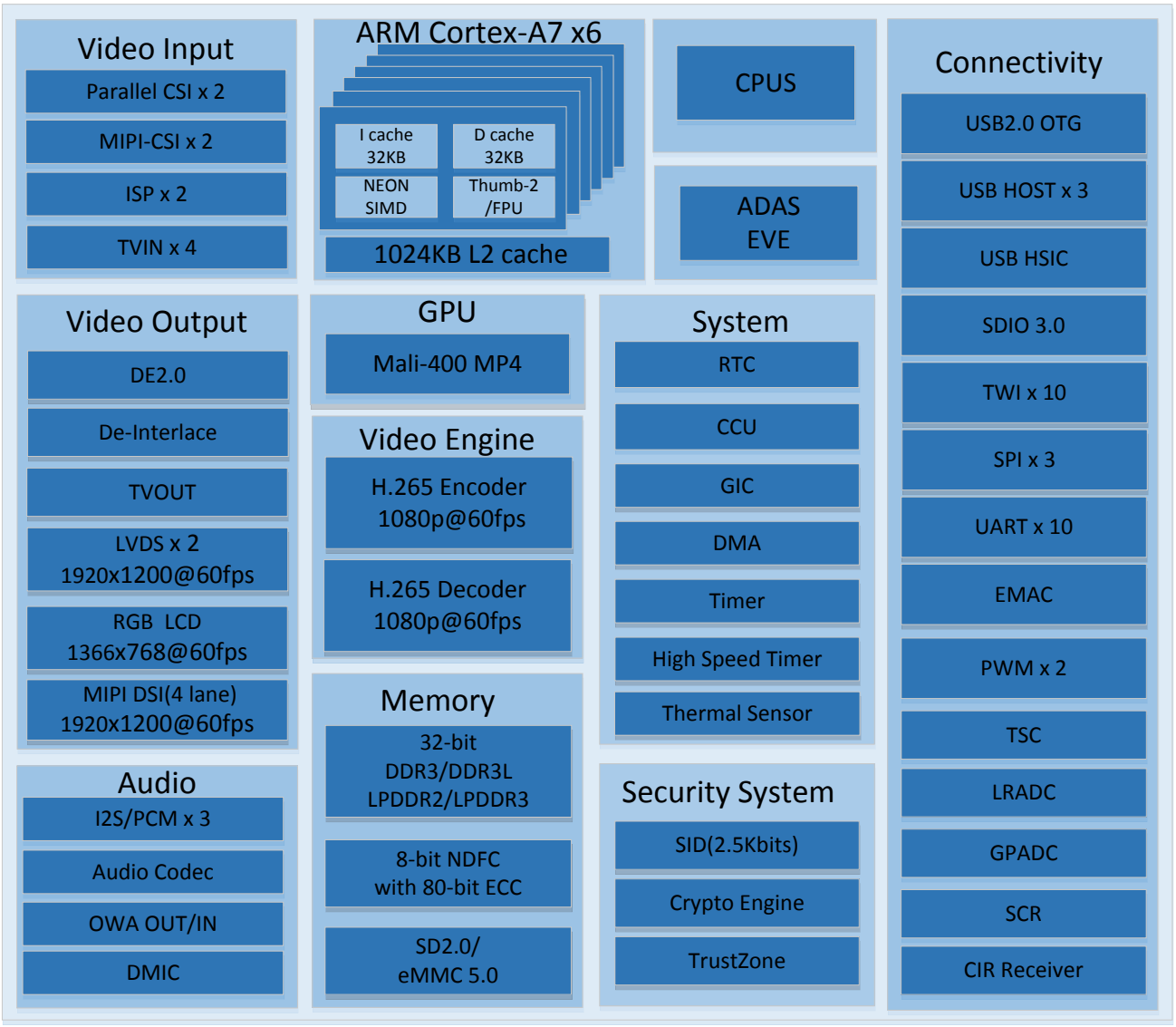

Figure 2- 1. T7 Block Diagram

The typical application diagram is shown in Figure 2-2.

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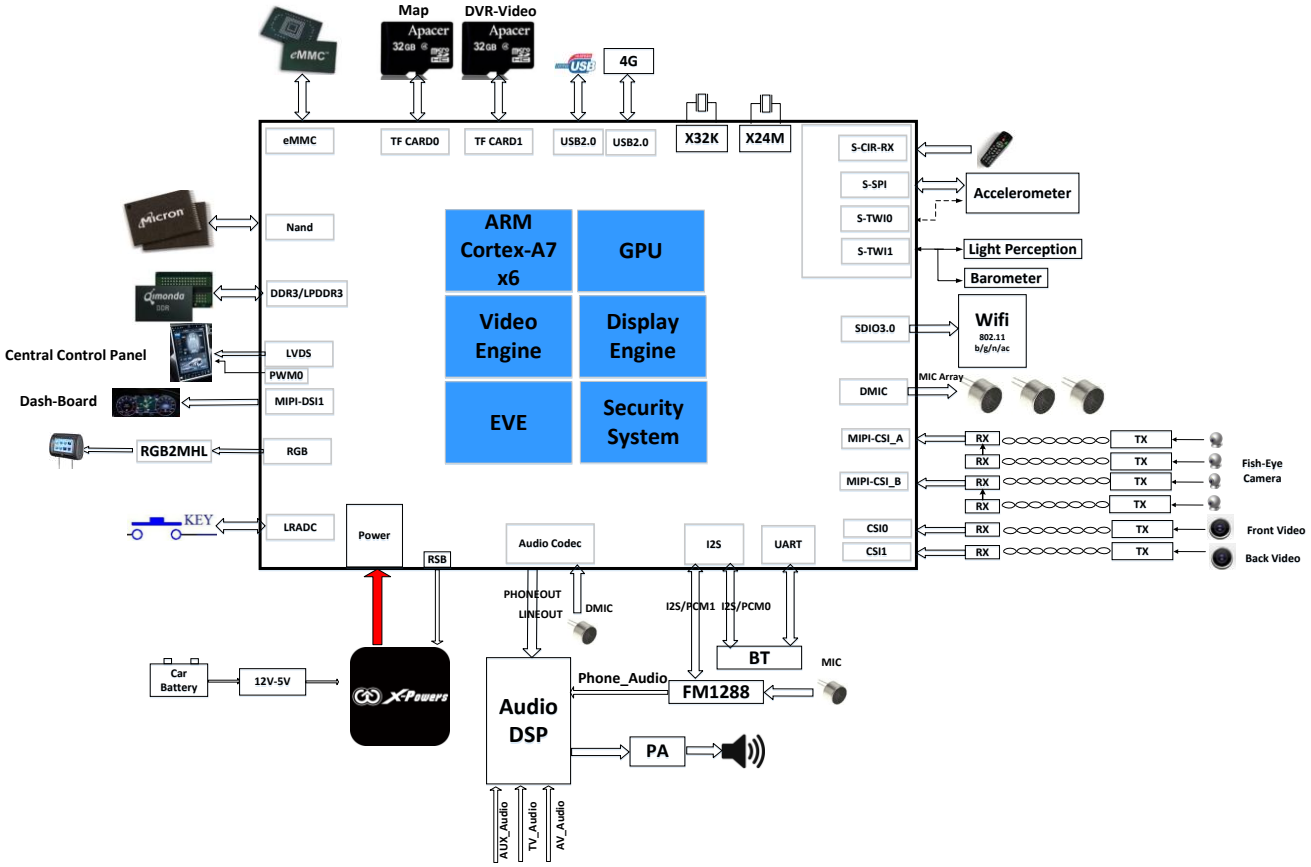

Figure 2- 2. T7 Typical Application Diagram

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Chapter 3 System

3.1. Memory Mapping

Module	Address(It is for Cluster CPU)	Size(Bytes)
N-BROM	0x0000 0000—0x0000 BFFF	48K
S-BROM	0x0000 0000—0x0000 FFFF	64K
SRAM A1	0x0002 0000---0x0002 7FFF	32K
SRAM C	0x0002 8000---0x0004 FFFF (VE:0x0002 8000---0x0004 2FFF DE:0x0004 3000---0x0004 FFFF)	160K
SRAM A2	0x0010 0000---0x0010 3FFF	16K
	0x0010 4000---0x0011 FFFF	112K
DE	0x0100 0000---0x013F FFFF	4M
DI	0x0142 0000---0x0143 FFFF	128K
G2D	0x0148 0000---0x014B FFFF	256K
EVE	0x0150 0000---0x0150 0FFF	4K
EVE_SRAM	0x0150 1000---0x0158 0FFF	512K
GPU	0x0180 0000---0x0180 FFFF	64K
CE_NS	0x0190 4000---0x0190 47FF	2K
CE_S	0x0190 4800---0x0190 4FFF	2K
CE_KEY_SRAM	0x0190 8000---0x0190 8FFF	4K
VE SRAM	0x01A0 0000---0x01BF FFFF	2M
VE	0x01C0 E000---0x01C0 EFFF	4K
ISP_SRAM	0x01D0 0000---0x020F FFFF	4M
ISP	0x0210 0000---0x0210 2FFF	12K
SYS_CFG	0x0300 0000---0x0300 0FFF	4K
CCU	0x0300 1000---0x0300 1FFF	4K
DMA	0x0300 2000---0x0300 2FFF	4K
MSGBOX	0x0300 3000---0x0300 3FFF	4K
SPINLOCK	0x0300 4000---0x0300 4FFF	4K
HSTIMER	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 67FF	2K
TIMER	0x0300 9000---0x0300 93FF	1K
PWM	0x0300 A000---0x0300 A3FF	1K
GPIO	0x0300 B000---0x0300 B3FF	1K

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PSI	0x0300 C000---0x0300 C3FF	1K
DCU	0x0301 0000---0x0301 FFFF	64K
GIC	0x0302 0000---0x0302 FFFF	64K
CCI-400	0x030D 0000---0x030E FFFF	128K
DRAM_CTRL	0x0400 2000---0x0400 5FFF	16K
NAND	0x0401 1000---0x0401 1FFF	4K
SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
SMHC3	0x0402 3000---0x0402 3FFF	4K
UART0	0x0500 0000---0x0500 03FF	1K
UART1	0x0500 0400---0x0500 07FF	1K
UART2	0x0500 0800---0x0500 0BFF	1K
UART3	0x0500 0C00---0x0500 0FFF	1K
UART4	0x0500 1000---0x0500 13FF	1K
TWI0	0x0500 2000---0x0500 23FF	1K
TWI1	0x0500 2400---0x0500 27FF	1K
TWI2	0x0500 2800---0x0500 2BFF	1K
TWI3	0x0500 2C00---0x0500 2FFF	1K
TWI4	0x0500 3000---0x0500 33FF	1K
TWI5	0x0500 3400---0x0500 37FF	1K
TWI6	0x0500 3800---0x0500 3BFF	1K
SCR	0x0500 5000---0x0500 53FF	1K
SPI0	0x0501 0000---0x0501 0FFF	4K
SPI1	0x0501 1000---0x0501 1FFF	4K
EMAC	0x0502 0000---0x0502 FFFF	64K
TS	0x0506 0000---0x0506 0FFF	4K
GPADC	0x0507 0000---0x0507 03FF	1K
I2S/PCM0	0x0509 0000---0x0509 0FFF	4K
I2S/PCM1	0x0509 1000---0x0509 1FFF	4K
I2S/PCM2	0x0509 2000---0x0509 2FFF	4K
OWA	0x0509 3000---0x0509 33FF	1K
DMIC	0x0509 5000---0x0509 53FF	1K
Audio Codec	0x0509 6000---0x0509 67FF	2K
USB0(USB2.0_OTG)	0x0510 0000---0x051F FFFF	1M
USB1(USB2.0_HOST1)	0x0520 0000---0x052F FFFF	1M
USB2(USB2.0_HOST2)	0x0531 0000---0x0531 0FFF	4K
USB3(USB2.0_HOST3)	0x0531 1000---0x0531 1FFF	4K
MIPI_DSI	0x0650 4000---0x0650 5FFF	8K
DISP_IF_TOP	0x0651 0000---0x0651 0FFF	4K
TCON_LCD0	0x0651 1000---0x0651 1FFF	4K
TCON_LCD1	0x0651 2000---0x0651 2FFF	4K
TCON_TV0	0x0651 5000---0x0651 5FFF	4K
TVE_TOP	0x0652 0000---0x0652 3FFF	16K

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TVE	0x0652 4000---0x0652 7FFF	16K
TVD_TOP	0x0653 0000---0x0653 0FFF	4K
TVD0	0x0653 1000---0x0653 1FFF	4K
TVD1	0x0653 2000---0x0653 2FFF	4K
TVD2	0x0653 3000---0x0653 3FFF	4K
TVD3	0x0653 4000---0x0653 4FFF	4K
CSI	0x0660 0000---0x0661 FFFF	128K
CSI_SRAM	0x0662 0000---0x0669 FFFF	512K
RTC	0x0700 0000---0x0700 03FF	1K
R_CPUS_CFG	0x0700 0400---0x0700 0BFF	2K
R_PRCM	0x0701 0000---0x0701 03FF	1K
R_SPI	0x0701 3000---0x0701 3FFF	4K
R_TIMER	0x0702 0000---0x0702 03FF	1K
R_WDOG	0x0702 0400---0x0702 07FF	1K
R_TWDOG	0x0702 0800---0x0702 0BFF	1K
R_PWM	0x0702 0C00---0x0702 0FFF	1K
R_INTC	0x0702 1000---0x0702 13FF	1K
R_GPIO	0x0702 2000---0x0702 23FF	1K
R_VM	0x0703 0000---0x0703 03FF	1K
R_THS	0x0703 0400---0x0703 07FF	1K
R_LRADC	0x0703 0800---0x0703 0BFF	1K
R_CIR_RX	0x0704 0000---0x0704 03FF	1K
R_UART0	0x0708 0000---0x0708 03FF	1K
R_UART1	0x0708 0400---0x0708 07FF	1K
R_UART2	0x0708 0800---0x0708 0BFF	1K
R_UART3	0x0708 0C00---0x0708 0FFF	1K
R_UART4	0x0708 1000---0x0708 13FF	1K
R_TWI0	0x0708 1400---0x0708 17FF	1K
R_TWI1	0x0708 1800---0x0708 1BFF	1K
R_TWI2	0x0708 1C00---0x0708 1FFF	1K
R_RSB	0x0708 3000---0x0708 33FF	1K
CPU_SUBSYS_CFG	0x0810 0000---0x0810 03FF	1K
TIMESTAMP_STU	0x0811 0000---0x0811 0FFF	4K
TIMESTAMP_CTRL	0x0812 0000---0x0812 0FFF	4K
C0_CPUX_CFG	0x0901 0000---0x0901 0FFF	4K
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K
C1_CPUX_CFG	0x0981 0000---0x0981 0FFF	4K
C1_CPUX_MBIST	0x0982 0000---0x0982 0FFF	4K
DRAM SPACE	0x4000 0000---0xFFFF FFFF	3G

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3.2. CPUX Configuration

3.2.1. Overview

The CPUX Configuration(CPUX_CFG) module is used to configure cluster control, including power on,reset, cache, debug, and check the status of CPU. It will be used when you want to disable/enable the CPU, cluster switch, CPU status check, and debug, etc.
The CPUX_CFG module includes C0_CPUX_CFG, C1_CPUX_CFG and CPU_SUBSYS_CTRL.
The C0_CPUX_CFG module is used for configuring cluster0, such as reset, control, cache, debug, CPU status.
The C1_CPUX_CFG module is used for configuring cluster1, such as reset, control, cache, debug, CPU status.
The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as CCI-400,GIC-400,JTAG.

The CPUX_CFG includes the following features.

- CPU reset system: core reset,debug circuit reset and other reset function
- CPU related control: interface control, CP15 control, power on and power down control
- CPU status check: idle status, SMP status, interrupt status and so on
- CPU debug related register for control and status

3.2.2. Operations and Functional Descriptions

3.2.2.1. Signal Description

For the detail of CPUX signal, please refer to ***ARM Cortex-A7 TRM***.

3.2.2.2. L2 Idle Mode

When the L2 of Cluster needs to enter WFI mode, firstly make sure the CPU0/1/2 of Cluster enter WFI mode, which can be checked through the bit[18:16] of **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing 1 to the bit0 of **Cluster Control Register1** , and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Note that set the **ACINACTM** to low when exiting the L2 idle mode.

3.2.2.3. CPUX Reset System

The CPUX reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**. The description of all reset signal in CPUX reset system is as follows.

Table 3- 1. Reset Signal Description

Reset Signal	Description

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CORE_RST	This is the primary reset signal which resets the corresponding core logic that includes NEON and VFP, Debug, ETM, breakpoint and watchpoint logic. This maps to a warm reset that covers reset of the processor logic.
PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. This maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Reset all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/C0_CPUX_CFG/C1_CPUX_CFG.
CPU_SUBSYS_RST	Including C0_H_RST/C1_H_RST/CCI-400/GIC-400/CPU_SUBSYS_CTRL.

3.2.2.4. CPUX Power Block Diagram

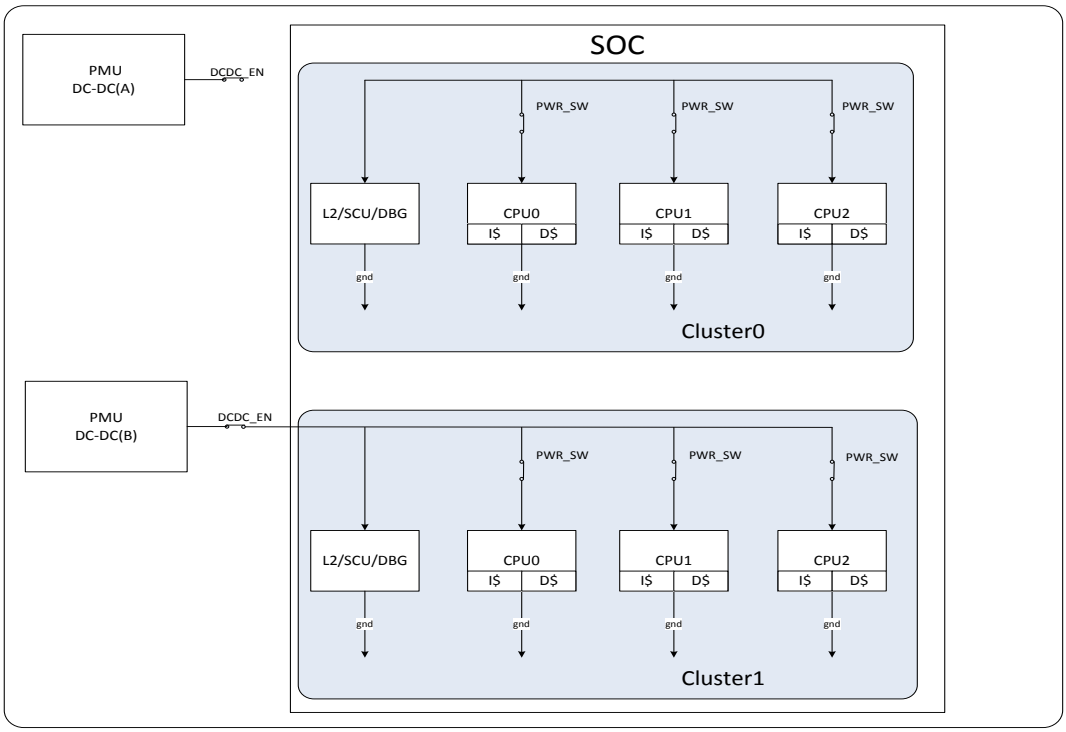

Figure 3- 1. CPUX Power Domain Block Diagram

Figure 3-1 above lists the power domain of cluster in default. For cluster0, the power switch of all CPU core are power-on, the pwron_rst of all CPU core are de-asserted, the core reset of CPU0 is de-asserted, the core reset of CPU [2:1] is asserted. For cluster1, the power switch of all CPU core are power-on, the pwron_rst of all CPU core are de-asserted, the core reset of all CPU are asserted.

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Since each CPU core and its appended circuits have the same power domain, the processor and related L1 cache, neon and vfp should be taken as a whole core.

C0_CPUX_CFG and cluster0 belong to the same power domain, within opening and closing cluster0 process, when cluster0 starts to power on again from power-off state, C0_CPUX_CFG holds in default state, at this time software need initial C0_CPUX_CFG after C0_H_RST is de-asserted.

C1_CPUX_CFG and cluster1 belong to the same power domain, within opening and closing cluster1, when cluster1 starts to power on again from power-off state, C1_CPUX_CFG holds in default state, at this time software need initial C1_CPUX_CFG after C1_H_RST is de-asserted.

CPU_SUBSYS_CTRL belongs to system power domain.The power domains of CPU related module are as follows.

Power Domain	Modules	Description
Cluster0	Cluster0/C0_CPUX_CFG/C0_MBIST	Cluster0 circuit, C0_CPUX_CFG module and CPU reset/power/mbist
Cluster1	Cluster1/C1_CPUX_CFG/C1_MBIST	Cluster1 circuit, C1_CPUX_CFG module and CPU reset/power/mbist
System	Timestamp/GIC/CCI-400/CPU_SUBSYS_CTRL/Clock	Provide system source of CPU sub-system
CPUS	CPUS_CFG	Power on/power off control of core or cluster.Note that when SoC has no CPUS, CPUS_CFG belongs to system power domain.

3.2.2.5. Operation Principle

The CPU-related operations(such as open/close core, cluster switch, status query) need proper configuration of Cx_CPUX_CFG module, as well as related system control resource including BUS, clock.

3.2.3. Programming Guidelines

For CPU core and cluster operation,please see the ***T7_CPU_AP_Note***.

3.2.4. Cluster 0 Configuration Register List

Module Name	Base Address
C0_CPUX_CFG	0x09010000

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1

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C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
C0_ADB400_PWRDNREQN_REG	0x0030	Cluster 0 ADB400 Power Down Request Register
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	Cluster 0 L2 Status Register
DBG_REG0	0x00C0	Cluster 0 Debug Control Register0
DBG_REG1	0x00C4	Cluster 0 Debug Control Register1

3.2.5. Cluster 0 Configuration Register Description

3.2.5.1. Cluster 0 Reset Control Register(Default Value: 0x13FF_0101)

Offset: 0x0000			**Register Name: C0_RST_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: Assert 1: De-assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal for test. 0: Assert 1: De-assert
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: Assert 1: De-assert
23	R/W	0x1	Reserved
22:20	R/W	0x7	ETM_RST Cluster ETM Reset Assert 0: Assert 1: De-assert
19	R/W	0x1	Reserved
18:16	R/W	0x7	DBG_RST Cluster Debug Reset Assert 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: Assert 1: De-assert

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7:3	/	/	/
2:0	R/W	0x1	CORE_RESET Cluster CPU[2:0] Reset Assert 0: Assert 1: De-assert

3.2.5.2. Cluster 0 Control Register0(Default Value:0x6000_0000)

Offset: 0x0010			Register Name: C0_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus 0: Barriers are broadcast onto system bus,this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus.This is compatible with an AXI3 interconnect.
30	R/W	0x1	BROADCAST_INNER Enable broadcasting of inner shareable transactions 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.
29	R/W	0x1	BROADCAST_OUTER Enable broadcasting of outer shareable transactions 0: Outer Shareable transactions are not broadcasted externally. 0: Outer Shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:11	/	/	/
10:8	R/W	0x0	CP15S_DISABLE Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset. 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3	/	/	/
2:0	R/W	0x0	L1_RST_DISABLE Disable automatic Cluster CPU[2:0] L1 cache invalidate at reset. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

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3.2.5.3. Cluster 0 Control Register1(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: C0_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepting requests. 0: Snoop interface is active 1: Snoop interface is inactive

3.2.5.4. Cluster 0 Control Register2(Default Value:0x0000_0010)

Offset: 0x0018			Register Name: C0_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state. This bit must remain high for at least one clock cycle to be visible by the cores.
23	/	/	/
22:20	R/W	0x0	EXM_CLR[2:0] Clear the status of interface.
19:17	/	/	/
16	R/W	0x0	CLREXMONREQ Clearing of the external global exclusive monitor request. When this bit is asserted, it acts as a WFE wake-up event to all the cores in the MPCore device.
15	/	/	/
14:12	R/W	0x0	CRYPTODISABLE Disable the Cryptography Extensions.
11:9	/	/	/
8	R/W	0x0	L2FLUSHREQ L2 hardware flush request.
7:5	/	/	/
4	R/W	0x1	GICCDISABLE. Globally disables the CPU interface logic and routes the "External" signals directly to the processor. 0: Enable the GIC CPU interface logic. 1: Disable the GIC CPU interface logic.
3:0	/	/	/

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3.2.5.5. Cluster 0 ADB400 PWRDNREQN Register(Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: C0_ADB400_PWRDNREQN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	ADB400_PWRDNREQN

3.2.5.6. Cluster0 CPU Status Register(Default Value: 0x000E_0000)

Offset: 0x0080			Register Name: C0_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R	0x0	SMP_AMP CPU[2:0] is in symmetric multiprocessing mode or asymmetric multiprocessing mode. 0: AMP mode 1: SMP mode
23:19	/	0x1	/
18:16	R	0x6	STANDBYWFI Indicates if Cluster CPU[2:0] is in WFI standby mode. 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:11	/	/	/
10:8	R	0x0	STANDBYWFE Indicates if Cluster CPU[2:0] is in the WFE standby mode. 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2 Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

3.2.5.7. L2 Status Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R	0x0	L2FLUSHDONE L2 hardware flush complete
9	R	0x0	EVENTO Event output

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			This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8	R	0x0	CLREXMONACK Clearing of the external global exclusive monitor acknowledge.
7:0	/	/	/

3.2.5.8. Cluster 0 Debug Control Register0(Default Value:0x0000_000F)

Offset: 0x00C0			Register Name: DBG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGL1RSTDISABLE Disable L1 data cache automatic invalidate on reset functionality. 0: Enable automatic invalidation of L1 data cache on reset 1: Disable automatic invalidation of L1 data cache on reset
15:11	/	/	/
10:8	R/W	0x0	DBGRESTART[2:0] External restart requests.
7:3	/	0x1	/
2:0	R/W	0x7	C_DBGPWRDUP Cluster Powered-up 0: Core is powered down 1: Core is powered up

3.2.5.9. Cluster 0 Debug Control Register1(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: DBG_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x0	DBGRESTARTED[2:0] Handshake for DBGRESTART.
11:8	R	0x0	C_DBGRSTREQ Warm reset request.
7	/	/	/
6:4	R	0x0	C_DBGNOPWRDWN Debugger No power-down request[2:0] Debugger has requested that processor is not powered down.
3	/	/	/
2:0	R	0x0	C_DBGPWRUPREQ Debugger power-up request[2:0] 0: Do not request that the core is powered up 1: Request that the core is powered up

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3.2.6. Cluster 1 Configuration Register List

Module Name	Base Address
C1_CPUX_CFG	0x09810000

Register Name	Offset	Description
C1_RST_CTRL	0x0000	Cluster 1 Reset Control Register
C1_CTRL_REG0	0x0010	Cluster 1 Control Register0
C1_CTRL_REG1	0x0014	Cluster 1 Control Register1
C1_CTRL_REG2	0x0018	Cluster 1 Control Register2
C1_ADB400_PWRDNREQN_REG	0x0030	Cluster 1 ADB400 Power Down Request Register
C1_CPU_STATUS	0x0080	Cluster 1 CPU Status Register
L2_STATUS_REG	0x0084	Cluster 1 L2 Status Register
DBG_REG0	0x00C0	Cluster 1 Debug Control Register0
DBG_REG1	0x00C4	Cluster 1 Debug Control Register1

3.2.7. Cluster 1 Configuration Register Description

3.2.7.1. Cluster 1 Reset Control Register(Default Value: 0x13FF_0100)

Offset: 0x0000			Register Name: C1_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: Assert 1: De-assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal for test. 0: Assert 1: De-assert
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: Assert 1: De-assert
23	R/W	0x1	Reserved
22:20	R/W	0x7	ETM_RST Cluster ETM Reset Assert

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			0: Assert 1: De-assert
19	R/W	0x1	Reserved
18:16	R/W	0x7	DBG_RST Cluster Debug Reset Assert 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: Assert 1: De-assert
7:3	/	/	/
2:0	R/W	0x0	CORE_RESET Cluster CPU[2:0] Reset Assert 0: Assert 1: De-assert

3.2.7.2. Cluster 1 Control Register0(Default Value:0x6000_0000)

Offset: 0x0010			**Register Name: C1_CTRL_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus 0: Barriers are broadcast onto system bus,this requires an AMBA4 interconnect. 1: Barriers are not broadcast onto the system bus.This is compatible with an AXI3 interconnect.
30	R/W	0x1	BROADCAST_INNER Enable broadcasting of inner shareable transactions 0: Inner shareable transactions are not broadcasted externally. 1: Inner shareable transactions are broadcasted externally.
29	R/W	0x1	BROADCAST_OUTER Enable broadcasting of outer shareable transactions 0: Outer shareable transactions are not broadcasted externally. 0: Outer shareable transactions are broadcasted externally.
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches. 1: Cache maintenance operations are broadcasted to downstream caches.
27:11	/	/	/

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10:8	R/W	0x0	CP15S_DISABLE Disable write access to some secure CP15 register.
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset. 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3	/	/	/
2:0	R/W	0x0	L1_RST_DISABLE Disable automatic Cluster CPU[2:0] L1 cache invalidate at reset. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.2.7.3. Cluster 1 Control Register1(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: C1_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepting requests. 0: Snoop interface is active 1: Snoop interface is inactive

3.2.7.4. Cluster 1 Control Register2(Default Value:0x0000_0010)

Offset: 0x0018			Register Name: C1_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state. This bit must remain high for at least one clock cycle to be visible by the cores.
23	/	/	/
22:20	R/W	0x0	EXM_CLR[2:0] Clear the status of interface.
19:17	/	/	/
16	R/W	0x0	CLREXMONREQ Clearing of the external global exclusive monitor request. When this bit is asserted, it acts as a WFE wake-up event to all the cores in the MPCore device.
15	/	/	/
14:12	R/W	0x0	CRYPTODISABLE Disable the Cryptography Extensions.

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11:9	/	/	/
8	R/W	0x0	L2FLUSHREQ L2 hardware flush request.
7:5	/	/	/
4	R/W	0x1	GICCDISABLE. Globally disables the CPU interface logic and routes the "External" signals directly to the processor. 0: Enable the GIC CPU interface logic. 1: Disable the GIC CPU interface logic.
3:0	/	/	/

3.2.7.5. Cluster 1 ADB400 PWRDNREQN Register(Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: C1_ADB400_PWRDNREQN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	ADB400_PWRDNREQN

3.2.7.6. Cluster 1 CPU Status Register(Default Value: 0x000E_0000)

Offset: 0x0080			Register Name: C1_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R	0x0	SMP_AMP CPU[2:0] is in symmetric multiprocessing mode or asymmetric multiprocessing mode. 0: AMP mode 1: SMP mode
23:19	/	0x1	/
18:16	R	0x6	STANDBYWFI Indicates if Cluster CPU[2:0] is in WFI standby mode. 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:11	/	/	/
10:8	R	0x0	STANDBYWFE Indicates if Cluster CPU[2:0] is in the WFE standby mode. 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
7:1	/	/	/
0	R	0x0	STANDBYWFIL2 Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode

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			1: Cluster L2 in WFI standby mode

3.2.7.7. L2 Status Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R	0x0	L2FLUSHDONE L2 hardware flush complete
9	R	0x0	EVENTO Event output This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8	R	0x0	CLREXMONACK Clearing of the external global exclusive monitor acknowledge.
7:0	/	/	/

3.2.7.8. Cluster 1 Debug Control Register0(Default Value:0x0000_000F)

Offset: 0x00C0			Register Name: DBG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGL1RSTDISABLE Disable L1 data cache automatic invalidate on reset functionality. 0: Enable automatic invalidation of L1 data cache on reset 1: Disable automatic invalidation of L1 data cache on reset
15:11	/	/	/
10:8	R/W	0x0	DBGRESTART[2:0] External restart requests.
7:3	/	0x1	/
2:0	R/W	0x7	C_DBGPWRDUP Cluster Powered-up 0: Core is powered down 1: Core is powered up

3.2.7.9. Cluster 1 Debug Control Register1(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: DBG_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x0	DBGRESTARTED[2:0]

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			Handshake for DBGRESTART
11:8	R	0x0	C_DBGRSTREQ Warm reset request
7	/	/	/
6:4	R	0x0	C_DBGNOPWRDWN No power-down request Debugger has requested that processor is not powered down. Debug no power down[2:0].
3	/	/	/
2:0	R	0x0	C_DBGPWRUPREQ Power up request Debug power up request[2:0] 0: Do not request that the core is powered up 1: Request that the core is powered up

3.2.8. CPU Subsystem Control Register List

Module Name	Base Address
CPU_SUBSYS_CTRL	0x08100000

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GENER_CTRL_REG1	0x0004	General Control Register1
EVENT_CNT_ STATUS	0x0008	CCI-400 Event Counter Status Register
GIC_JTAG_RST_CTRL	0x000C	GIC and Jtag Reset Control Register
C01_INT_EN	0x0010	Cluster0 and Cluster1 Interrupt Enable Control Register
IRQ_FIQ_STATUS	0x0014	GIC IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2

3.2.9. CPU Subsystem Control Register Description

3.2.9.1. General Control Register0(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GENER_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	GIC_CFGSDISABLE Disables write access to some secure GIC registers.

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3.2.9.2. General Control Register1(Default Value: 0x0000_000E)

Offset: 0x0004			Register Name: GENER_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	QOSOVERRIDE If HIGH, internally generated values override the **ARQOS** and **AWQOS** inputs. One bit exists for each slave interface.
3:2	R/W	0x3	ACCHANNELEN If LOW, then AC requests are not issued on the corresponding slave interface. One bit exists for each slave interface.
1	R/W	0x1	CCI_CLK_ON Setting 1 means CCI Clock always on.
0	R/W	0x0	CCI_CLK_OFF Setting 1 means CCI Clock always off. **NOTE** **When CCI_CLK_OFF and CCI_CLK_ON are valid at the same time ,CCI_CLK_OFF has the higher priority than CCI_CLK_ON.**

3.2.9.3. CCI-400 Event Counter Status Register(Default Value: 0x001F_0000)

Offset: 0x0008			Register Name: EVENT_CNT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:16	R	0x1F	EVENT_CNT_OF Event counter over flag[4:0]. The CCI-400 counters: The CCNT overflow is bit 4,event counters on bits[3:0]. 0: Counter has overflowed 1: Counter has not overflowed
15:2	/	/	/
1	R/W	0x0	C1_ADB400_CACTIVES_SYNC2 Cluster 1 CACTIVE bit.
0	R/W	0x0	C0_ADB400_CACTIVES_SYNC2 Cluster 0 CACTIVE bit.

3.2.9.4. GIC and Jtag Reset Control Register(Default Value: 0x0000_0F01)

Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:16	R/W	0x0	EXM_CLR[2:0]

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			Clear the status of interface, for debug
15:12	/	/	/
11	R/W	0x1	CS_RST CoreSight reset 0: Assert 1: De-assert
10	R/W	0x1	DAP_RST DAP reset 0: Assert 1: De-assert
9	R/W	0x1	PORTRST Jtag portrst 0: Assert 1: De-assert
8	R/W	0x1	TRST Jtag trst 0: Assert 1: De-assert
7:1	/	/	/
0	R/W	0x1	GIC_RESET GIC_reset_cpu_reg 0: Assert 1: De-assert

3.2.9.5. Cluster 0 and Cluster 1 Interrupt Enable Register(Default Value: 0x0000_FFFF)

Offset: 0x0010			**Register Name: C0_INT_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	C0_1_GIC_EN Interrupt enable control register. Mask irq_out/firq_out to system domain.

3.2.9.6. GIC IRQ/FIQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: IRQ_FIQ_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0000	FIQ_OUT[15:0]
15:0	R/W	0x0000	IRQ_OUT[15:0]

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3.2.9.7. General Control Register2(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GENER_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CDBGRSTACK Debug Reset ACK
15:2	/	/	/
1	R/W	0x0	C1_TSCLKCHANGE Cluster 1 Time Stamp change bit
0	R/W	0x0	C0_TSCLKCHANGE Cluster 0 Time Stamp change bit

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3.3. CCU

3.3.1. Overview

The CCU controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 16 PLLs
- Bus source and divisions
- Clock output control
- PLL bias control
- PLL tuning control
- PLL pattern control
- Configuring modules clock
- Bus clock gating
- Bus software reset
- PLL lock control

3.3.2. Operations and Functional Descriptions

3.3.2.1. System Bus Tree

Figure 3-2 shows a block diagram of the System Bus Tree.

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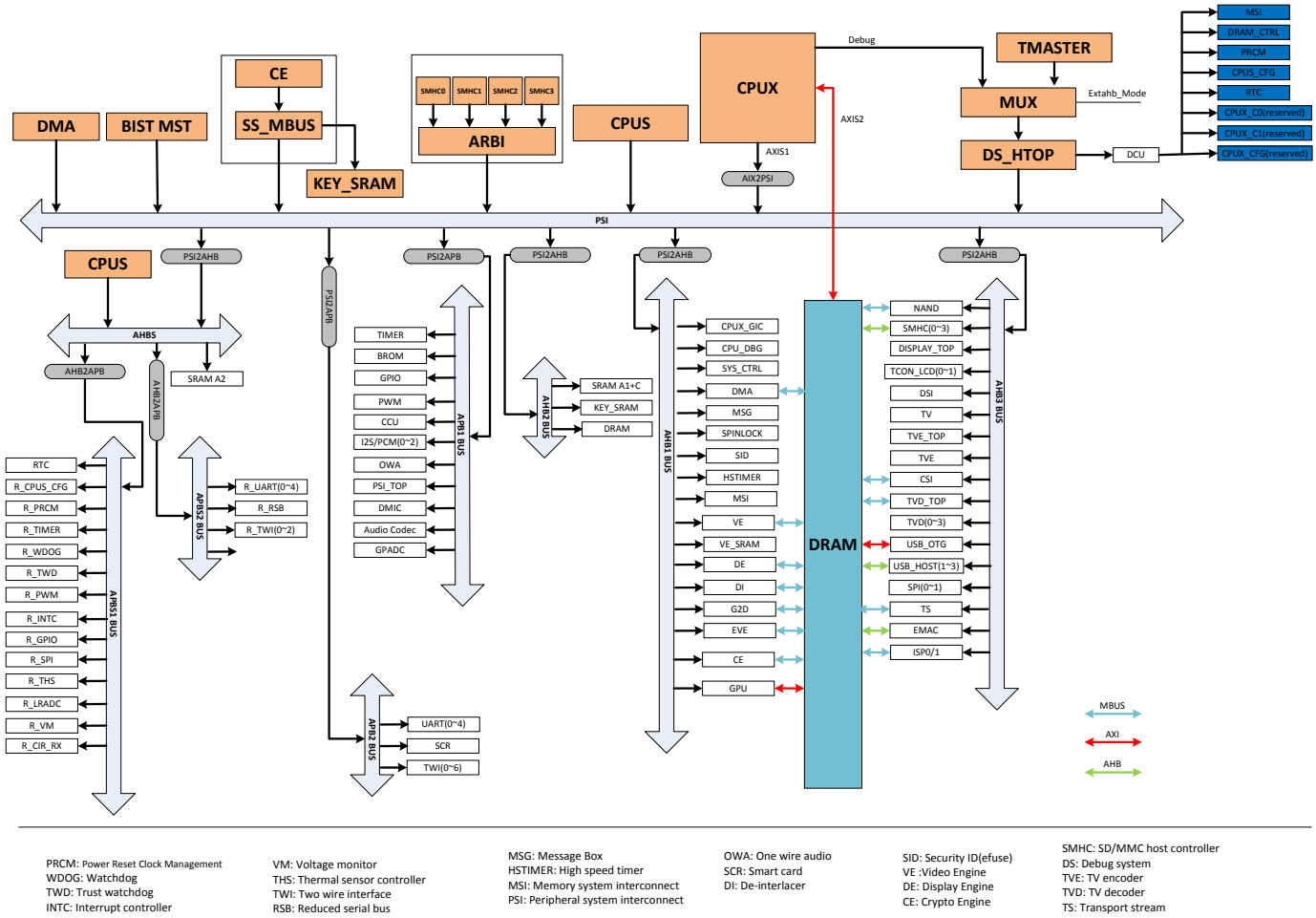

Figure 3- 2. System Bus Tree

The above system bus tree is used to introduce bus interface of every module. These modules can divide into two types: bus master, slave. But a part of these modules can be not only used as bus master, but also as slave. DMA, BIST_MST(Built-in Self Test Master), CE, SMHC0/1/2/3, CPUS,CPUX and DS are as bus master that can access corresponding register of every slave through bus. Every slave hangs in corresponding bus.

For example, CPU accesses to RTC module, the process is as follows: CPU instruction firstly passes AXI bus, then goes to PSI bus through AXI2PSI bridge, then goes to AHBS bus through PSI2AHB bridge, and goes to APBS2 through AHB2APB, finally RTC is operated based on relevant bus protocol . The access time from CPU to RTC , is relevant with the CPU clock , AXI bus clock, PSI bus clock, AHBS bus clock and APBS2 bus clock. Any lower bus clock will lead to access time very long.

DRAM supports 3 bus types, DRAM can interact directly with some modules through different bus without using CPU. Red arrow indicates that those modules (CPU,GPU,USB_OTG) access DRAM through AXI bus. Green arrow indicates that those modules (USB_HOST,SMHC0/1/2/3,EMAC) access DRAM through AHB bus. Blue arrow indicates that those modules(such as DE,CE,VE,DMA,NAND,CSI) access DRAM through MBUS .

In above module, the clocks of these modules(such as TWI and UART) to be hung on APB2/APBS2 are from their respective bus clock , however the clocks of most other modules are from related CLK register , such as DE_CLK_REG.

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Each module clock requirement can refer to their module.

3.3.2.2. Bus Clock Tree

Figure 3-3 shows a block diagram of the Bus Clock Tree.

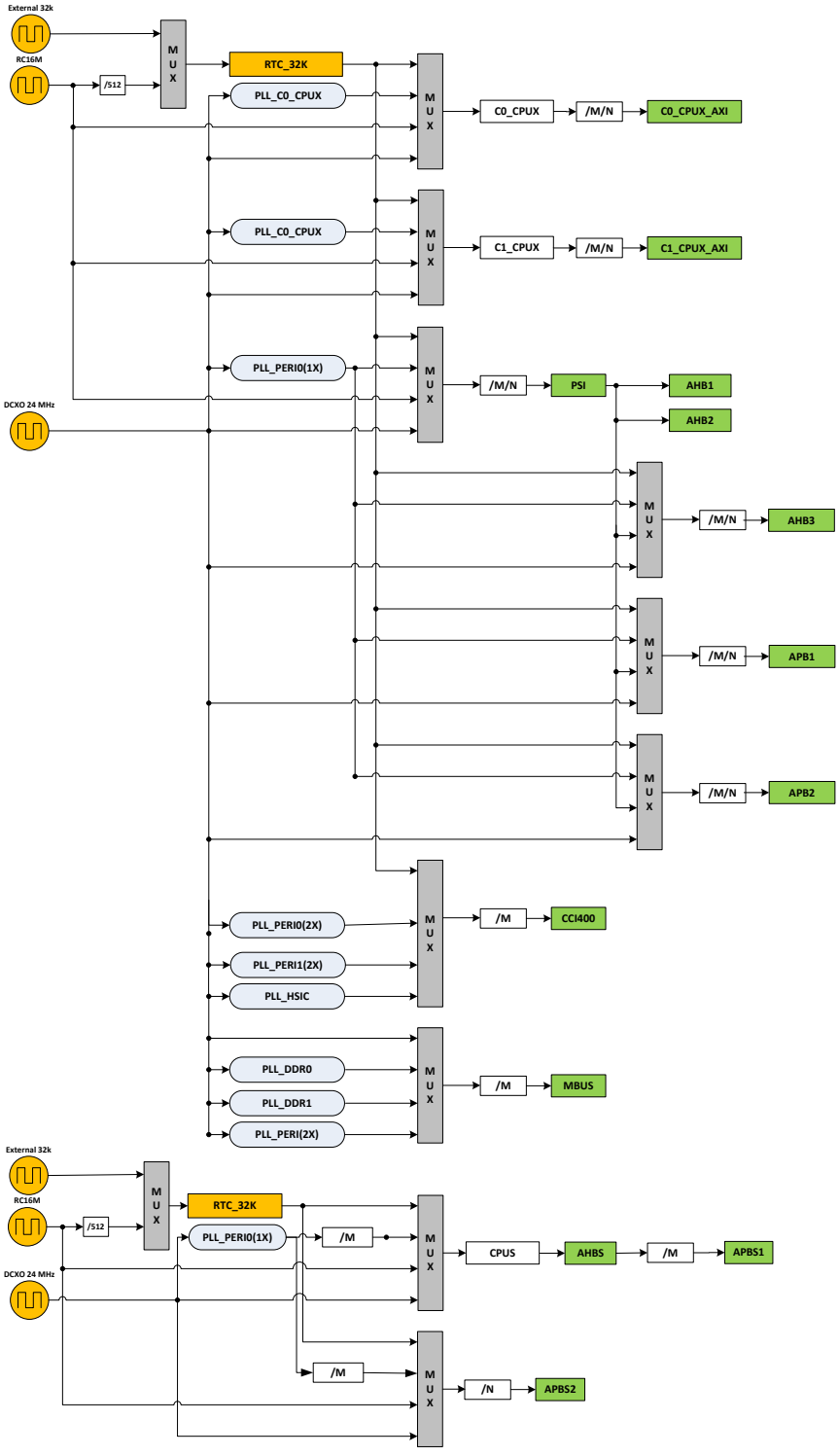

Figure 3- 3. Bus Clock Tree

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3.3.2.3. Module Clock Tree

Figure 3-4 shows the block diagram of the Module Clock Tree.

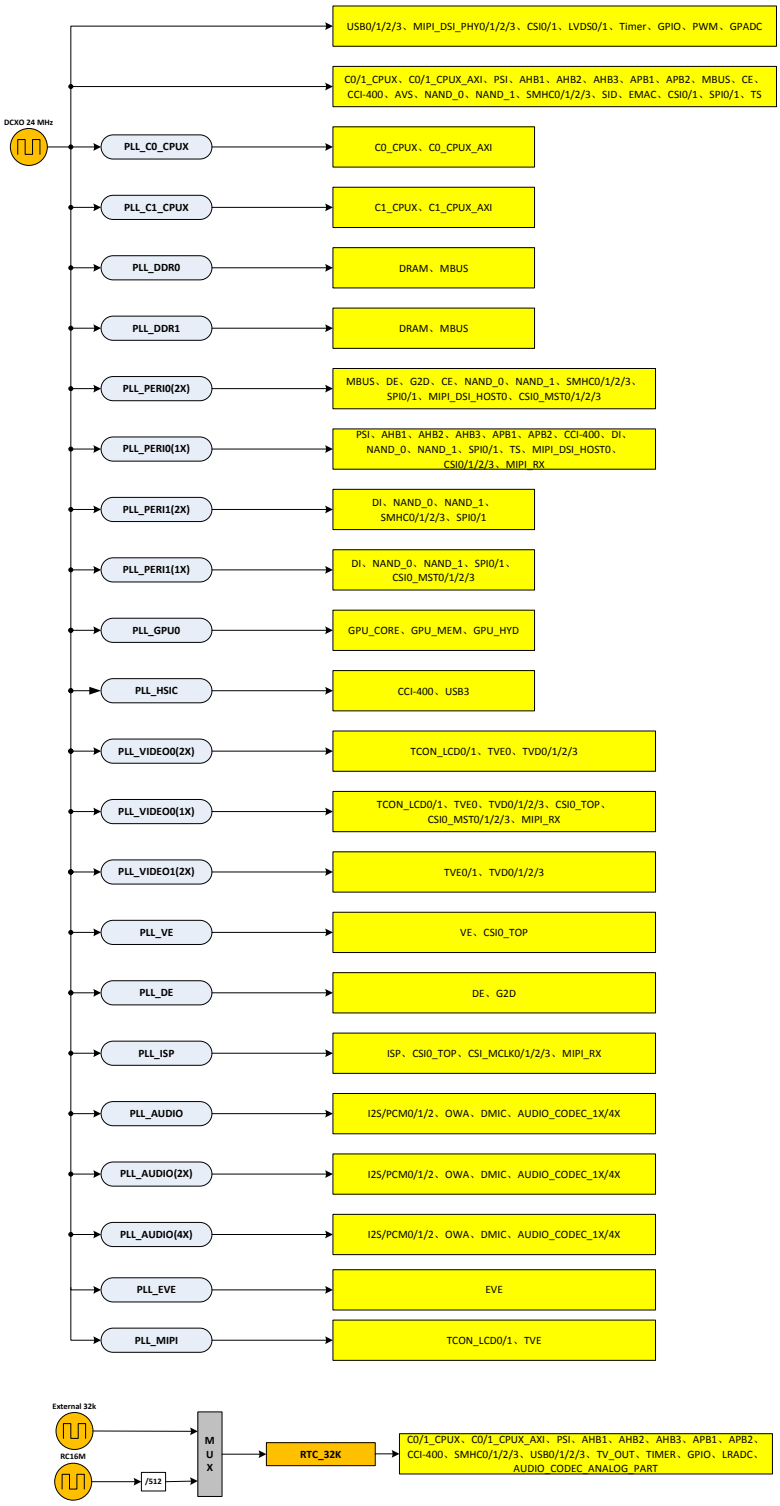

Figure 3- 4. Module Clock Tree

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3.3.2.4. Typical Applications

PLL applications: use the available clock sources to generate clock roots to various parts of the chip.

Table 3- 2. PLL Typical Applications

PLLs	Typical Applications	Description
PLL_C0_CPUX	C0_CPUX, C0_CPUX_AXI	Support DFS
PLL_C1_CPUX	C1_CPUX, C1_CPUX_AXI	Support DFS
PLL_DDR0	MBUS,DRAM	Not Support spread spectrum
PLL_DDR1	MBUS,DRAM	Not Support spread spectrum Support linear frequency scaling
PLL_PERI0(2X)	MBUS, DE,G2D,CE,NAND_0,NAND_1,SMHC0/1/2/3, SPI0/1, MIPI_DSI_HOST0,CSI0_MST0/1/2/3	Not Support DFS
PLL_PERI0(1X)	PSI,AHB1,AHB2,AHB3,APB1,APB2,CCI-400,DI,NAND_0, NAND_1,SPI0/1,TS,MIPI_DSI_HOST0,CSI0/1/2/3,MIPI_RX	Not Support DFS
PLL_PERI1(2X)	DI,NAND_0,NAND_1,SMHC0/1/2/3,SPI0/1	Not Support DFS
PLL_PERI1(1X)	DI,NAND_0,NAND_1,SPI0/1,CSI0_MST0/1/2/3	Not Support DFS
PLL_GPU	GPU_CORE,GPU_MEM,GPU_HYD	Support DFS
PLL_HSIC	CCI-400,USB3	Not Support DFS
PLL_VIDEO0(2X)	TCON_LCD0/1,TVE,TVD0/1/2/3	Not Support DFS
PLL_VIDEO0(1X)	TCON_LCD0/1,TVE, TVD0/1/2/3,CSI0_TOP,CSI0_MST0/1/2/3, MIPI_RX	Not Support DFS
PLL_VIDEO1(2X)	TVE0/1,TVD0/1/2/3	Not Support DFS
PLL_VE	VE,CSI0_TOP	Not Support DFS
PLL_DE	DE,G2D	Not Support DFS
PLL_ISP	ISP,CSI0_TOP,CSI_MCLK0/1/2/3,MIPI_RX	Not Support DFS
PLL_AUDIO	I2S/PCM0,I2S/PCM1,I2S/PCM2,OWA,DMIC,AUDIO_CODEC	Not Support DFS
PLL_AUDIO(2X)	I2S/PCM0,I2S/PCM1,I2S/PCM2,OWA,DMIC,AUDIO_CODEC	Not Support DFS
PLL_AUDIO(4X)	I2S/PCM0,I2S/PCM1,I2S/PCM2,OWA,DMIC,AUDIO_CODEC	Not Support DFS
PLL_EVE	EVE	Not Support DFS
PLL_MIPI	TVE,TCON_LCD0/1	Not Support DFS

DFS: dynamic frequency scaling.

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3.3.2.5. PLL Features

Table 3- 3. PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Lock Time
PLL_C0CPUX	60MHz~2.1GHz	60MHz~1GHz	Yes	No	No	<200ps	3ms
PLL_C1CPUX	60MHz~2.1GHz	60MHz~1GHz	Yes	No	No	<200ps	3ms
PLL_AUDIO	24.576MHz, 22.5792MHz	24.576MHz, 22.5792MHz, (24.576 * 8) MHz, (22.5792 * 8) MHz	Yes	No	No	<1500ps	100us
PLL_PERI0(2X)	504MHz~1.4GHz	1.2GHz	No	No	No	<200ps	100us
PLL_PERI1(2X)	504MHz~1.4GHz	1.2GHz	Yes	No	No	<200ps	100us
PLL_DDR0	192MHz~1.6GHz	240MHz~1.6GHz	No	No	No	200MHz~800MHz(<200ps) 800MHz~1.3GHz(<140ps) 1.3GHz~1.8GHz(<100ps)	1ms
PLL_DDR1	192MHz~1.6GHz	240MHz~1.6GHz	No	Yes	Yes	200MHz~800MHz(<200ps) 800MHz~1.3GHz(<140ps) 1.3GHz~1.8GHz(<100ps)	1ms
PLL_VIDEO0(2X)	384MHz~1.2GHz	324MHz~1.2GHz	Yes	No	No	<200ps	100us
PLL_VIDEO0(1X)	192MHz~600MHz	192MHz~600MHz	Yes	No	No	<200ps	100us
PLL_VIDEO1(2X)	384MHz~1.2GHz	324MHz~1.2GHz	Yes	No	No	<200ps	100us
PLL_VIDEO1(1X)	192MHz~600MHz	192MHz~600MHz	Yes	No	No	<200ps	100us
PLL_VE	192MHz~600MHz	210MHz~500MHz	Yes	No	No	<200ps	100us
PLL_GPU	144MHz~1000MHz	144MHz~600MHz	Yes	No	No	<200ps	100us
PLL_DE	192MHz~600MHz	192MHz~600MHz	Yes	No	No	<200ps	100us
PLL_HSIC	192MHz~600MHz	480MHz	Yes	No	No	<200ps	100us
PLL_MIPI	500MHz~1.4GHz	500MHz~1.4GHz	Yes	No	No	<200ps	5ms

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3.3.3. Programming Guidelines

3.3.3.1. PLL

(1) In practical application, other PLLs do not support dynamic frequency scaling except for PLL_C0_CPUX, PLL_C1_CPUX and PLL_GPU.

(2) The user guide of PLL Lock(using PLL_C0_CPUX as an example)

(a).PLL_C0_CPUX from close to open:

- Write 0 to the bit29 of **PLL_C0_CPUX_CTRL_REG**.
- Configure the parameters **(N,M,K,P)** of **PLL_C0_CPUX_CTRL_REG**.
- Write 1 to the bit31 of **PLL_C0_CPUX_CTRL_REG**.
- Write 1 to the bit29 of **PLL_C0_CPUX_CTRL_REG**.
- Read the bit28 of **PLL_C0_CPUX_CTRL_REG**, when it is 1, then Cluster0 CPUX PLL is locked.
- Delay 20us.

(b).PLL_C0_CPUX frequency conversion:

- Write 0 to the bit29 of **PLL_C0_CPUX_CTRL_REG**.
- Configure the parameters **(N,M,K,P)** of **PLL_C0_CPUX_CTRL_REG**.
- Write 1 to the bit29 of **PLL_C0_CPUX_CTRL_REG**.
- Read the bit28 of **PLL_C0_CPUX_CTRL_REG**, when it is 1, then Cluster0 CPUX PLL is locked.
- Delay 20us.

(c).PLL_C0_CPUX from open to close:

- Write 0 to the bit31 of **PLL_C0_CPUX_CTRL_REG**.
- Write 0 to the bit29 of **PLL_C0_CPUX_CTRL_REG**.

3.3.3.2. BUS

(1) When setting the BUS clock , you should set the division factor firstly, and after the division factor becomes valid, switch the clock source. The clock source will be switched after at least three clock cycles.

(2) The BUS clock should not be dynamically changed in most applications.

3.3.3.3. Clock Switch

Make sure that the clock source output is valid before the clock source switch, and then set a proper divide ratio; after the division factor becomes valid, switch the clock source.

3.3.3.4. Gating and Reset

Make sure that the reset signal has been released before the release of module clock gating.

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3.3.3.5. Spread Spectrum Function

The configuration of spread spectrum follows the following steps.

Step1: Configure PLL_CTRL Register

- According to PLL frequency and PLL frequency formula f = [(N+1)/(M0+1)/(M1+1)+X] * 24MHz, suppose the value of divisor M0 and divisor M1, calculate factor N and decimal value X, and write M0、M1、N and PLL frequency to the PLL_CTRL register.
- Configure the SDM_Enable bit of the PLL_CTRL register to 1 to enable spread spectrum function.

NOTE

Having different PLL calculate formula for different PLL, please refer to each PLL_CTRL register.

Step 2: Configure PLL_PAT Register

- According to decimal value X and spread spectrum frequency(the bit[18:17] of the PLL_PAT register), calculate WAVE_BOT (= 2^{17} * X1) and WAVE_STEP (= 2^{17} * (X2-X1) / (24MHz/PREQ) * 2).
- Configure spread spectrum mode(SPR_FREQ_MODE) to 2. If for PLL_DDR0/1, set SPR_FREQ_MODE to 3.
- Configure the spread spectrum clock source select bit(SDM_CLK_SEL) to 0 by default. But if the PLL_INPUT_DIV_M1 bit of the PLL_CTRL register is 1, the bit should set to 1.
- Write WAVE_BOT、WAVE_STEP、PREQ、SPR_FREQ_MODE and SDM_CLK_SEL to the PLL_PAT register, and configure SIG_DELT_PAT_EN to 1.

Step 3: Delay 20us

3.3.4. Register List

Module Name	Base Address
CCU	0x03001000

Register Name	Offset	Description
PLL_C0_CPUX_CTRL_REG	0x0000	PLL_C0_CPUX Control Register
PLL_C1_CPUX_CTRL_REG	0x0008	PLL_C1_CPUX Control Register
PLL_DDR0_CTRL_REG	0x0010	PLL_DDR0 Control Register
PLL_DDR1_CTRL_REG	0x0018	PLL_DDR1 Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register
PLL_PERI1_CTRL_REG	0x0028	PLL_PERI1 Control Register
PLL_GPU_CTRL_REG	0x0030	PLL_GPU Control Register
PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_VIDEO1_CTRL_REG	0x0048	PLL_VIDEO1 Control Register
PLL_VE_CTRL_REG	0x0058	PLL_VE Control Register
PLL_DE_CTRL_REG	0x0060	PLL_DE Control Register
PLL_ISP_CTRL_REG	0x0068	PLL_ISP Control Register
PLL_HSIC_CTRL_REG	0x0070	PLL_HSIC Control Register

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PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_MIPI_CTRL_REG	0x0080	PLL_MIPI Control Register
PLL_EVE_CTRL_REG	0x00C0	PLL_EVE Control Register
PLL_C0_CPUX_PATTERN_REG	0x0100	PLL_C0_CPUX Pattern Register
PLL_C1_CPUX_PATTERN_REG	0x0108	PLL_C1_CPUX Pattern Register
PLL_DDR0_PATTERN_REG	0x0110	PLL_DDR0 Pattern Register
PLL_DDR1_PATTERN_REG	0x0118	PLL_DDR1 Pattern Register
PLL_PERI1_PATTERN_REG	0x0128	PLL_PERI1 Pattern Register
PLL_GPU_PATTERN_REG	0x0130	PLL_GPU Pattern Register
PLL_VIDEO0_PATTERN_REG	0x0140	PLL_VIDEO0 Pattern Register
PLL_VIDEO1_PATTERN_REG	0x0148	PLL_VIDEO1 Pattern Register
PLL_VE_PATTERN_REG	0x0158	PLL_VE Pattern Register
PLL_DE_PATTERN_REG	0x0160	PLL_DE Pattern Register
PLL_ISP_PATTERN_REG	0x0168	PLL_ISP Pattern Register
PLL_HSIC_PATTERN_REG	0x0170	PLL_HSIC Pattern Register
PLL_AUDIO_PATTERN_REG	0x0178	PLL_AUDIO Pattern Register
PLL_MIPI_PATTERN_REG	0x0180	PLL_MIPI Pattern Register
PLL_EVE_PATTERN_REG	0x01C0	PLL_EVE Pattern Register
PLL_DDR1_SSC_LIN_REG	0x0218	PLL_DDR1 SSC Linear Register
PLL_C0_CPUX_BIAS_REG	0x0300	PLL_C0_CPUX Bias Register
PLL_C1_CPUX_BIAS_REG	0x0308	PLL_C1_CPUX Bias Register
PLL_DDR0_BIAS_REG	0x0310	PLL_DDR0 Bias Register
PLL_DDR1_BIAS_REG	0x0318	PLL_DDR1 Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_PERI1_BIAS_REG	0x0328	PLL_PERI1 Bias Register
PLL_GPU_BIAS_REG	0x0330	PLL_GPU Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_VIDEO1_BIAS_REG	0x0348	PLL_VIDEO1 Bias Register
PLL_VE_BIAS_REG	0x0358	PLL_VE Bias Register
PLL_DE_BIAS_REG	0x0360	PLL_DE Bias Register
PLL_ISP_BIAS_REG	0x0368	PLL_ISP Bias Register
PLL_HSIC_BIAS_REG	0x0370	PLL_HSIC Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_MIPI_BIAS_REG	0x0380	PLL_MIPI Bias Register
PLL_EVE_BIAS_REG	0x03C0	PLL_EVE Bias Register
PLL_C0_CPUX_TUN_REG	0x0400	PLL_C0_CPUX Tuning Register
PLL_C1_CPUX_TUN_REG	0x0408	PLL_C1_CPUX Tuning Register
PLL_MIPI_TUN_REG	0x0480	PLL_MIPI Tuning Register
C0_CPUX_AXI_CFG_REG	0x0500	C0_CPUX AXI Configuration Register
C1_CPUX_AXI_CFG_REG	0x0504	C1_CPUX AXI Configuration Register
PSI_CFG_REG	0x0510	PSI Configuration Register
AHB3_CFG_REG	0x051C	AHB3 Configuration Register
APB1_CFG_REG	0x0520	APB1 Configuration Register

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APB2_CFG_REG	0x0524	APB2 Configuration Register
CCI400_CFG_REG	0x0530	CCI400 Configuration Register
MBUS_CFG_REG	0x0540	MBUS Configuration Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register
DI_CLK_REG	0x0620	DI Clock Register
DI_BGR_REG	0x062C	DI Bus Gating Reset Register
G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
EVE_CLK_REG	0x0650	EVE Clock Register
EVE_BGR_REG	0x065C	EVE Bus Gating Reset Register
GPU_CLK_REG	0x0670	GPU Clock Register
GPU_BGR_REG	0x067C	GPU Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
MSGBOX_BGR_REG	0x071C	Message-Box Bus Gating Reset Register
SPINLOCK_BGR_REG	0x072C	Spin-Lock Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HS-Timer Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PSI_BGR_REG	0x079C	PSI Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MST_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
PLL_DDR_AUX_REG	0x0808	PLL_DDR Auxiliary Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
NAND_CLK0_REG	0x0810	NAND Clock0 Register
NAND_CLK1_REG	0x0814	NAND Clock1 Register
NAND_BGR_REG	0x082C	NAND Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC3_CLK_REG	0x083C	SMHC3 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SCR_BGR_REG	0x093C	SCR Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register

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EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
TS_CLK_REG	0x09B0	TS Clock Register
TS_BGR_REG	0x09BC	TS Bus Gating Reset Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
I2S/PCM0_CLK_REG	0x0A10	I2S/PCM0 Clock Register
I2S/PCM1_CLK_REG	0x0A14	I2S/PCM1 Clock Register
I2S/PCM2_CLK_REG	0x0A18	I2S/PCM2 Clock Register
I2S/PCM_BGR_REG	0x0A1C	I2S/PCM Bus Gating Reset Register
OWA_CLK_REG	0x0A20	OWA Clock Register
OWA_BGR_REG	0x0A2C	OWA Bus Gating Reset Register
DMIC_CLK_REG	0x0A40	DMIC Clock Register
DMIC_BGR_REG	0x0A4C	DMIC Bus Gating Reset Register
AUDIO_CODEC_1X_CLK_REG	0x0A50	Audio Codec 1X Clock Register
AUDIO_CODEC_4X_CLK_REG	0x0A54	Audio Codec 4X Clock Register
AUDIO_CODEC_BGR_REG	0x0A5C	Audio Codec Bus Gating Reset Register
USB2.0_OTG_CLK_REG	0x0A70	USB2.0_OTG Clock Register
USB2.0_HOST1_CLK_REG	0x0A74	USB2.0_HOST1 Clock Register
USB2.0_HOST2_CLK_REG	0x0A78	USB2.0_HOST2 Clock Register
USB2.0_HOST3_CLK_REG	0x0A7C	USB2.0_HOST3 Clock Register
USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
MIPI_DSI_HOST_CLK_REG	0x0B24	MIPI DSI Host Clock Register
MIPI_DSI_BGR_REG	0x0B4C	MIPI DSI Bus Gating Reset Register
DISPLAY_IF_TOP_BGR_REG	0x0B5C	DISPLAY_IF_TOP Bus Gating Reset Register
TCON_LCD0_CLK_REG	0x0B60	TCON_LCD0 Clock Register
TCON_LCD1_CLK_REG	0x0B64	TCON_LCD1 Clock Register
TCON_LCD_BGR_REG	0x0B7C	TCON_LCD Bus Gating Reset Register
TCON_TV_BGR_REG	0x0B9C	TCON_TV Bus Gating Reset Register
LVDS_BGR_REG	0x0BAC	LVDS Bus Gating Reset Register
TVE_CLK_REG	0x0BB0	TVE Clock Register
TVE_BGR_REG	0x0BBC	TVE Bus Gating Reset Register
TVD0_CLK_REG	0x0BC0	TVD0 Clock Register
TVD1_CLK_REG	0x0BC4	TVD1 Clock Register
TVD2_CLK_REG	0x0BC8	TVD2 Clock Register
TVD3_CLK_REG	0x0BCC	TVD3 Clock Register
TVD_BGR_REG	0x0BDC	TVD Bus Gating Reset Register
CSI_MISC_CLK_REG	0x0C00	CSI MISC Clock Register
CSI_TOP_CLK_REG	0x0C04	CSI TOP Clock Register
CSI_MCLK0_REG	0x0C08	CSI Master Clock0 Register
CSI_MCLK1_REG	0x0C0C	CSI Master Clock1 Register
CSI_MCLK2_REG	0x0C10	CSI Master Clock2 Register
CSI_MCLK3_REG	0x0C14	CSI Master Clock3 Register
CSI_BGR_REG	0x0C2C	CSI Bus Gating Reset Register
MIPI_RX_CLK_REG	0x0C30	MIPI RX Clock Register

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CCU_SEC_SWITCH_REG	0x0F00	CCU Security Switch Register
PLL_LOCK_CTRL_REG	0x0F04	PLL Lock Control Register
FRE_DET_CTRL_REG	0x0F08	Frequence Detect Control Register
FRE_UP_LIM_REG	0x0F0C	Frequence Up Limit Register
FRE_DOWN_LIM_REG	0x0F10	Frequence Down Limit Register
24M_CLK_OUTPUT_REG	0x0F20	24M Clock Output Register

3.3.5. Register Description

3.3.5.1. PLL_C0_CPUX Control Register (Default Value: 0x0000_1000)

Offset: 0x0000			Register Name: PLL_C0_CPUX_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_C0_CPUX= (24MHz*N*K)/(M*P) PLL_C0_CPUX is 408MHz by default. **NOTE** **10 ≤ N*K ≤ 88. When the frequency is less than 240MHz, P factor is used. 24MHz*N*K must be in the range from 240MHz to 2.1GHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_DIV_P PLL Output External Divider P 00: 1 01: 2 10: 4 11: / When output clock is less than 240MHz,clock frequency is output by dividing P.

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15:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 31.
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K PLL Factor K K=PLL_FACTOR_K + 1 PLL_FACTOR_K is from 0 to 3.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3.

3.3.5.2. PLL_C1_CPUX Control Register (Default Value: 0x0000_1000)

Offset: 0x0008			Register Name: PLL_C1_CPUX_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_C1_CPUX= (24MHz*N*K)/(M*P) PLL_C1_CPUX is 408MHz by default. **NOTE** **10 ≤ N*K ≤ 88. When the frequency is less than 240MHz, P factor is used.** **24MHz*N*K must be in the range from 240MHz to 2.1GHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_DIV_P

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			PLL Output External Divider P 00: 1 01: 2 10: 4 11: / When output clock is less than 240MHz,clock frequency is output by dividing P.
15:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 31.
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K PLL Factor K K=PLL_FACTOR_K + 1 PLL_FACTOR_K is from 0 to 3.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3.

3.3.5.3. PLL_DDR0 Control Register (Default Value: 0x0000_1800)

Offset: 0x0010			**Register Name: PLL_DDR0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_DDR0 = 24MHz*N/M. PLL_DDR0 is 600MHz by default. **NOTE** **16≤ N ≤ 75.** **24MHz*N/M must be in the range from 192MHz to 1.6GHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)

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27	R/W	0x0	Avoid Mistake 0: Avoid 1: Not Avoid Avoid N=0 by mistake
26:15	/	/	/
14:8	R/W	0x18	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M=PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3.

3.3.5.4. PLL_DDR1 Control Register (Default Value: 0x0000_1800)

Offset: 0x0018			**Register Name: PLL_DDR1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_DDR1 = 24MHz*N/M. PLL_DDR1 is 600 MHz by default.  **NOTE** **16≤N≤75.** **24MHz*N/M must be in the range of 192MHz~1.6GHz.**
30	R/WAC	0x0	PLL_CFG_UPD PLL Configuration Update When PLL_DDR1 has changed, this bit should be set to 1 to validate the PLL, otherwise the change is invalid. It will be auto cleared after the PLL is valid. 0: No effect 1: Update
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	Avoid Mistake 0: Avoid 1: Not Avoid

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			Avoid N=0 by mistake
26:15	/	/	/
14:8	R/W	0x18	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M=PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3.

3.3.5.5. PLL_PERI0 Control Register (Default Value: 0x0000_1811)

Offset: 0x0020			Register Name: PLL_PERI0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI0(1X) = 24MHz*N*K/2. PLL_PERI0(2X) = 24MHz*N*K. **NOTE** **21≤N*K≤58(give priority to K≥2)** The PLL_PERI0(2X) should be fixed to 1.2GHz, it is not recommended to vary this value arbitrarily. 24MHz*N*K clock must be in the range from 504MHz to 1.4GHz. PLL_PERI0(2X) is 1.2GHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 31.
7:6	/	/	/

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5:4	R/W	0x1	PLL_FACTOR_K PLL Factor K K= PLL_FACTOR_K+1 PLL_Factor_K is from 0 to 3.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_D PLL Factor D D = PLL_FACTOR_D + 1 D is only for test. The PLL_PERI0(2X) back door clock output is 24MHz*N*K/D. PLL_FACTOR_D is from 0 to 3.

3.3.5.6. PLL_PERI1 Control Register (Default Value: 0x0000_1811)

Offset: 0x0028			Register Name: PLL_PERI1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI1(1X) = 24MHz*N*K/2. PLL_PERI1(2X) = 24MHz*N*K. **NOTE** **21≤N*K≤58(give priority to K≥2)** The PLL_PERI1(2X) should be fixed to 1.2GHz, it is not recommended to vary this value arbitrarily. 24MHz*N*K clock must be in the range from 504MHz to 1.4GHz. PLL_PERI1(2X) is 1.2GHz by default.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N PLL Factor N

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			N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 31.
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K PLL Factor K K= PLL_FACTOR_K+1 PLL_FACTOR_K is from 0 to 3.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_D PLL Factor D D = PLL_FACTOR_D + 1 D is only for test. The back door clock output of the PLL_PERI0(2X) is 24MHz*N*K/D. PLL_FACTOR_D is from 0 to 3.

3.3.5.7. PLL_GPU Control Register (Default Value: 0x0600_6207)

Offset: 0x0030			**Register Name: PLL_GPU_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_GPU = (24MHz*N)/M. In the fractional mode, the PLL output is selected by bit 25. PLL_GPU is 297MHz by default.  **NOTE** **8≤N/M≤25.** **PLL_GPU must be in the range from 192MHz to 600MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set

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			to 0); no meaning when PLL_MODE_SEL =1. 0: PLL output=270MHz 1: PLL output=297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.8. PLL_VIDEO0 Control Register (Default Value: 0x0600_6207)

Offset: 0x0040			**Register Name: PLL_VIDEO0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_VIDEO0(1X) = (24MHz*N)/M. PLL_VIDEO0(2X) =((24MHz*N)/M)*2. In the fractional mode, the PLL output is selected by bit 25. PLL_VIDEO0(1X) is 297MHz by default. **NOTE** **8≤N/M≤25** **(24MHz*N)/M must be in the range from 192MHz to 600MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK_STATUS 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional Mode

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			1: Integer Mode When in Fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLL_VIDEO0(1X) =270MHz 1: PLL_VIDEO0(1X) =297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.9. PLL_VIDEO1 Control Register (Default Value: 0x0600_6207)

Offset: 0x0048			**Register Name: PLL_VIDEO1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_VIDEO1(1X) = (24MHz*N)/M. PLL_VIDEO1(2X) =((24MHz*N)/M)*2. In the fractional mode, the PLL output is selected by bit 25. PLL_VIDEO1(1X) is 297MHz by default. **NOTE** **8≤N/M≤25** **(24MHz*N)/M must be in the range from 192MHz to 600MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked

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			1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); No meaning when PLL_MODE_SEL =1. 0: PLL_VIDEO1(1X) =270MHz 1: PLL_VIDEO1(1X) =297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.10. PLL_VE Control Register (Default Value: 0x0600_6207)

Offset: 0x0058			**Register Name: PLL_VE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_VE = (24MHz*N)/M. In the fractional mode, the PLL output is selected by bit 25. PLL_VE is 297MHz by default. **NOTE** **8≤N/M ≤25** **PLL_VE must be in the range from 192MHz to 600MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable

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28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output=297MHz.
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.11. PLL_DE Control Register (Default Value: 0x0600_6207)

Offset: 0x0060			**Register Name: PLL_DE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_DE = (24MHz*N)/M. In the fractional mode, the PLL output is selected by bit 25. PLL_DE is 297MHz by default. **NOTE** **8≤N/M≤25** **PLL_DE must be in the range from 30MHz to 600MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable

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			0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional Mode 1: Integer Mode When in Fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output=297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.12. PLL_ISP Control Register (Default Value: 0x0600_6207)

Offset: 0x0068			**Register Name: PLL_ISP_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_ISP = (24MHz*N)/M. In the fractional mode, the PLL output is selected by bit 25. PLL_ISP is 297MHz by default. **NOTE** **8≤N/M≤25.** **PLL_ISP must be in the range from 30MHz to 600MHz.**
30	/	/	/

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29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional mode 1: Integer mode When in fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output=297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.13. PLL_HSIC Control Register (Default Value: 0x0600_1300)

Offset: 0x0070			**Register Name: PLL_HSIC_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_HSIC = (24MHz*N)/M. In the fractional mode, the PLL output is selected by bit 25. PLL_HSIC is 480MHz by default. **NOTE** **8≤N/M≤25.**

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			PLL_HSIC must be in the range from 192MHz to 600MHz.
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional mode 1: Integer mode When in fractional mode, the Per Divider M should be set to 0.
25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output=297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x13	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x0	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.14. PLL_AUDIO Control Register (Default Value: 0x0003_5514)

Offset: 0x0078			**Register Name: PLL_AUDIO_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable The PLL is for Audio. PLL_AUDIO= (24MHz*N)/(M*P). PLL_AUDIO(8X) = (24MHz*N*2)/M

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			PLL_AUDIO(4X) = PLL_AUDIO(8X) /2 PLL_AUDIO(2X) = PLL_AUDIO(4X) /2 PLL_AUDIO is 24.571MHz by default. **NOTE** **3≤N/P≤21.** **PLL_AUDIO must be in the range from 20MHz to 200MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:20	/	/	/
19:16	R/W	0x3	PLL_FACTOR_P PLL Factor P P= PLL_FACTOR_P +1 PLL_Factor_P is from 0 to 15.
15	/	/	/
14:8	R/W	0x55	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:5	/	/	/
4:0	R/W	0x14	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 31.

3.3.5.15. PLL_MIPI Control Register (Default Value: 0x0000_0515)

Offset: 0x0080			**Register Name: PLL_MIPI_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_MIPI= (PLL_VIDEO0(1X)*N*K)/M .

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			PLL_MIPI is 594MHz by default. **NOTE** **K ≥2.** **PLL_MIPI must be in the range from 60MHz to 1.4GHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	SINT_FRAC When VFB_SEL=1, PLL mode control, otherwise no meaning. 0: Integer Mode 1: Fractional Mode
26	R/W	0x0	SDIV2 PLL clock output when VFB_SEL=1; no meaning when VFB_SEL =0 0: PLL Output 1: PLL Output X2
25	R/W	0x0	S6P25_7P5 PLL Output is selected by this bit when VFB_SEL=1 and SINT_FRAC=1, otherwise no meaning. 0: PLL Output=PLL Input*6.25 1: PLL Output= PLL Input *7.5
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23	R/W	0x0	LDO1_EN On-chip LDO1 Enable
22	R/W	0x0	LDO2_EN On-chip LDO2 Enable
21	R/W	0	PLL_SRC PLL Source Select 0: PLL_VIDEO0(1X) 1: PLL_VIDEO1(1X)
20:18	/	/	/
17	R/W	0x0	PLL_FEEDBACK_DIV PLL feed-back divider control. PLL clock output when VFB_SEL=1; no meaning when VFB_SEL =0 0: Divided by 5 1: Divided by 7
16	R/W	0x0	VFB_SEL 0: MIPI Mode(N, K, M valid)

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			1:HDMI Mode(sint_frac,sdiv2,s6p25_7p5 , pll_feedback_div valid)
15:12	/	/	/
11:8	R/W	0x5	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 15.
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K PLL Factor K K= PLL_FACTOR_K +1 PLL_FACTOR_K is from 0 to 3.
3:0	R/W	0x5	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.16. PLL_EVE Control Register (Default Value: 0x0600_6207)

Offset: 0x00C0			**Register Name: PLL_EVE_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable In the integer mode, PLL_EVE = (24MHz*N)/M. In the fractional mode, the PLL output is selected by bit 25. PLL_EVE is 297MHz by default. **NOTE** **8≤N/M≤25.** **PLL_EVE must be in the range from 192MHz to 600MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	/	/	/
26	R/W	0x1	PLL_MODE_SEL 0: Fractional Mode 1: Integer Mode When in fractional mode, the Per Divider M should be set to 0.

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25	R/W	0x1	FRAC_CLK_OUT PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1. 0: PLL Output=270MHz 1: PLL Output=297MHz
24	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable
23:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 127.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_M PLL Per-div M M=PLL_PRE_M+ 1 PLL_PRE_M is from 0 to 15.

3.3.5.17. PLL_C0_CPUX Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: PLL_C0_CPUX_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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3.3.5.18. PLL_C1_CPUX Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PLL_C1_CPUX_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.19. PLL_DDR0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: PLL_DDR0_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz

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			10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.20. PLL_DDR0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: PLL_DDR0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.21. PLL_DDR1 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PLL_DDR1_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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3.3.5.22. PLL_DDR1 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PLL_DDR1_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.23. PLL_PERI1 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: PLL_PERI1_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.24. PLL_GPU Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PLL_GPU_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE

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			Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.25. PLL_VIDEO0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO0_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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3.3.5.26. PLL_VIDEO1 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: PLL_VIDEO1_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.27. PLL_VE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: PLL_VE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz

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			10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.28. PLL_DE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PLL_DE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.29. PLL_ISP Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: PLL_ISP_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP

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			Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.30. PLL_HSIC Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: PLL_HSIC_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.31. PLL_AUDIO Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE

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			Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.32. PLL_MIPI Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: PLL_MIPI_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

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3.3.5.33. PLL_EVE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: PLL_EVE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular 11: Triangular
28:20	R/W	0x0	WAVE_STEP Wave Step
19	/	/	/
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.34. PLL_DDR1 SSC Linear Configuration Register (Default Value: 0x0CCC_A000)

Offset: 0x0218			Register Name: PLL_DDR1_SSC_LIN_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_DDR1_MODE 0: Normal mode 1: Continuously frequency scale
30:29	/	/	/
28:12	R/W	0xCCCA	PLL_SSC The amplitude of SSC must be an integral multiple of (2^Step). Spread spectrum amplitude =(SSC amplitude+2^Step)*24/(2^17). The unit is MHz.
11:7	/	/	/
6:4	R/W	0x0	PLL_DDR1_PHASE_COMPENSATE The value of bit[6:4] is based on 24MHz clock, then the default PLL_C0_CPUX phase compensate is (3/24000000) s.
3:0	R/W	0x0	PLL_DDR1_STEP 0000: 0.00439MHz/us (576/2^17) 0001: 0.00879MHz/us (576/2^16)

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			0010: 0.01758MHz/us (576/2^15) 0011: 0.03516MHz/us (576/2^14) 0100: 0.07031MHz/us (576/2^13) 0101: 0.14062MHz/us (576/2^12) 0110: 0.28125MHz/us (576/2^11) 0111: 0.56250MHz/us (576/2^10) 1000: 1.12500MHz/us (576/2^9) 1001: 2.25000MHz/us (576/2^8) 1010: 4.50000MHz/us (576/2^7) 1011: 9.00000MHz/us (576/2^6) Others: 0.00439MHz/us (576/2^17)

3.3.5.35. PLL_C0_CPUX Bias Register (Default Value: 0x0810_0200)

Offset: 0x0300			Register Name: PLL_C0_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VCO_RST VCO reset in
30:29	/	/	/
28	R/W	0x0	EXG_MODE Exchange Mode CPU PLL source will select PLL_PERIPH instead of PLL_CPU.
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[3:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL PLL Lock Time Control[2:0]
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[3:0]

3.3.5.36. PLL_C1_CPUX Bias Register (Default Value: 0x0810_0200)

Offset: 0x0308			Register Name: PLL_C1_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VCO_RST VCO reset in
30:29	/	/	/
28	R/W	0x0	EXG_MODE

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			Exchange Mode CPU PLL source will select PLL_PERIPH instead of PLL_CPU.
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[3:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL PLL Lock Time Control[2:0]
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[3:0]

3.3.5.37. PLL_DDR0 Bias Register (Default Value: 0x1001_0000)

Offset: 0x0310			Register Name: PLL_DDR0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x01	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:0	/	/	/

3.3.5.38. PLL_DDR1 Bias Register (Default Value: 0x1001_0000)

Offset: 0x0318			Register Name: PLL_DDR1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x01	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:0	/	/	/

3.3.5.39. PLL_PERI0 Bias Register (Default Value: 0x1010_0010)

Offset: 0x0320	Register Name: PLL_PERI0_BIAS_REG

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Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL PLL Band Width Control 0: Narrow 1: Wide
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[1:0]

3.3.5.40. PLL_PERI1 Bias Register (Default Value: 0x1010_0010)

Offset: 0x0328			Register Name: PLL_PERI1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL PLL Band Width Control 0: Narrow 1: Wide
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[1:0]

3.3.5.41. PLL_GPU Bias Register (Default Value: 0x1010_0000)

Offset: 0x0330			Register Name: PLL_GPU_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]

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23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.42. PLL_VIDEO0 Bias Register (Default Value: 0x1010_0000)

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/.
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.43. PLL_VIDEO1 Bias Register (Default Value: 0x1010_0000)

Offset: 0x0348			Register Name: PLL_VIDEO1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.44. PLL_VE Bias Register (Default Value: 0x1010_0000)

Offset: 0x0358			Register Name: PLL_VE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL

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			PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.45. PLL_DE Bias Register (Default Value: 0x1010_0000)

Offset: 0x0360			Register Name: PLL_DE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.46. PLL_ISP Bias Register (Default Value: 0x1010_0000)

Offset: 0x0368			Register Name: PLL_ISP_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.47. PLL_HSIC Bias Register (Default Value: 0x1010_0000)

Offset: 0x0370			Register Name: PLL_HSIC_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

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28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.48. PLL_AUDIO Bias Register (Default Value: 0x1010_0000)

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:0	/	/	/

3.3.5.49. PLL_MIPI Bias Register (Default Value: 0xF810_0400)

Offset: 0x0380			Register Name: PLL_MIPI_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST VCO Reset In
30:28	R/W	0x7	PLLVDD_LDO_OUT_CTRL PLLVDD LDO Output Control PLL_IN_POWER_SEL=1 PLL_IN_POWER_SEL=0 000:1.00V 000:1.20V 001:1.02V 001:1.225V 010:1.04V 010:1.25V 011:1.06V 011:1.275V 100: 1.08V 100:1.30V 101:1.10V 101:1.325V 110:1.12V 110:1.35V 111:1.14V 111:1.375V The PLL_IN_PWR_SEL is in the PLL_MIPI Tuning Register.
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL PLL VCO Bias Control [3:0]
23:21	/	/	/

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20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:11	/	/	/
10:8	R/W	0x4	PLL_LOCK_CTRL PLL Lock Time Control[2:0]
7:1	/	/	/
0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control

3.3.5.50. PLL_EVE Bias Register (Default Value: 0x1010_0000)

Offset: 0x03C0			Register Name: PLL_EVE_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL PLL VCO Bias Control[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL PLL Current Bias Control[4:0]
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL PLL Damping Factor Control[2:0]

3.3.5.51. PLL_C0_CPUX Tuning Register (Default Value: 0x0A10_1000)

Offset: 0x0400			Register Name: PLL_C0_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	PLL_BAND_WID_CTRL PLL Band Width Control 0: Narrow 1: Wide
26	R/W	0x0	VCO_GAIN_CTRL_EN VCO Gain Control Enable 0: Disable 1: Enable
25:23	R/W	0x4	VCO_GAIN_CTRL VCO Gain Control Bits[2:0]
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL PLL Initial Frequency Control[6:0]
15	R/W	0x0	C_OD C-Reg-Od For Verify

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14:8	R/W	0x10	C_B_IN C-B-In[6:0] For Verify
7	R/W	0x0	C_OD1 C-Reg-Od1 For Verify
6:0	R	0x0	C_B_OUT C-B-Out[6:0] For Verify

3.3.5.52. PLL_C1_CPUX Tuning Register (Default Value: 0x0A10_1000)

Offset: 0x0408			Register Name: PLL_C1_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	PLL_BAND_WID_CTRL PLL Band Width Control 0: Narrow 1: Wide
26	R/W	0x0	VCO_GAIN_CTRL_EN VCO Gain Control Enable 0: Disable 1: Enable
25:23	R/W	0x4	VCO_GAIN_CTRL VCO Gain Control Bits[2:0]
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL PLL Initial Frequency Control[6:0]
15	R/W	0x0	C_OD C-Reg-Od For Verify
14:8	R/W	0x10	C_B_IN C-B-In[6:0] For Verify
7	R/W	0x0	C_OD1 C-Reg-Od1 For Verify
6:0	R	0x0	C_B_OUT C-B-Out[6:0] For Verify

3.3.5.53. PLL_MIPI Tuning Register (Default Value: 0x8A10_2000)

Offset: 0x0480			Register Name: PLL_MIPI_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	PLL_INPUT_POWER_SEL 0:2.5V 1:3.0V
30	/	/	/
29:28	R/W	0x0	VREG_OUT_EN

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			For Verify
27	R/W	0x1	PLL_BAND_WID_CTRL PLL Band Width Control 0: Narrow 1: Wide
26	R/W	0x0	VCO_GAIN_CTRL_EN VCO Gain Control Enable 0: Disable 1: Enable
25:23	R/W	0x4	VCO_GAIN_CTRL VCO Gain Control Bits[2:0]
22	/	/	/
21:16	R/W	0x0	CNT_INT For Verify[5:0]
15	R/W	0x0	C_OD C-Reg-Od For Verify
14	/	/	/
13:8	R/W	0x20	C_B_IN C-B-In[5:0] For Verify
7	R/W	0x0	C_OD1 C-Reg-Od1 For Verify
6	/	/	/
5:0	R	0x0	C_B_OUT C-B-Out[5:0] For Verify

3.3.5.54. C0_CPUX AXI Configuration Register (Default Value: 0x0000_0301)

Offset: 0x0500			**Register Name: C0_CPUX_AXI_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: CCU_32K 10: RC16M 11: PLL_C0_CPUX C0_CPUX Clock = Clock Source C0_CPUX_AXI Clock = Clock Source/M C0_CPUX _APB Clock = Clock Source/N
23:10	/	/	/
9:8	R/W	0x3	CPUX_APB_FACTOR_N Factor N (N = FACTOR_N +1) The range of N is from 1 to 4.

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7:2	/	/	/
1:0	R/W	0x1	FACTOR_M Factor M (M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.55. C1_CPUX AXI Configuration Register (Default Value: 0x0000_0301)

Offset: 0x0504			Register Name: C1_CPUX_AXI_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: CCU_32K 10: RC16M 11: PLL_C1_CPUX C1_CPUX Clock = Clock Source C1_CPUX_AXI Clock = Clock Source/M C1_CPUX _APB Clock = Clock Source/N
23:10	/	/	/
9:8	R/W	0x3	CPUX _APB_FACTOR_N Factor N (N = FACTOR_N +1) The range of N is from 1 to 4.
7:2	/	/	/
1:0	R/W	0x1	FACTOR_M Factor M (M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.56. PSI_AHB1_AHB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: PSI_AHB1_AHB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: CCU_32K 10: RC16M 11: PLL_PERI0(1X) PSI_AHB1_AHB2 CLK = Clock Source/M/N
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N

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			Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.57. AHB3 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x051C			Register Name: AHB3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: CCU_32K 10: PSI 11: PLL_PERI0(1X) AHB3 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.58. APB1 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x520			Register Name: APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M

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			01: CCU_32K 10: PSI 11: PLL_PERI0(1X) APB1 CLK = Clock Source/M/N
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.59. APB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x524			Register Name: APB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: CCU_32K 10: PSI 11: PLL_PERI0(1X) APB2 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

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3.3.5.60. CCI400 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x530			Register Name: CCI400_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: CCU_32K 010: PLL_PERI0(2X) 011: PLL_PERI1(2X) 100: PLL_HSIC Others:/ CLK = Clock Source/M.
23:2	/	/	/
1:0	R/W	0x0	FACTOR_ M Factor M.(M= FACTOR_ M +1) The range of M is from 1 to 4.

3.3.5.61. MBUS Configuration Register (Default Value: 0xC000_0000)

Offset: 0x540			Register Name: MBUS_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON MBUS CLK = Clock Source/M.
30	R/W	0x1	MBUS_RST MBUS Reset 0: Assert 1: De-assert
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_DDR0 11: PLL_DDR1
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 8.

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3.3.5.62. DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_DE 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.63. DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DE_RST DE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DE_GATING Gating Clock For DE 0: Mask 1: Pass

3.3.5.64. DI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0620			Register Name: DI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

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			SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_PERI0(1X) 1: PLL_PERI1(1X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.65. DI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x062C			Register Name: DI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DI_RST DI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DI_GATING Gating Clock For DI 0: Mask 1: Pass

3.3.5.66. G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_DE 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M

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			Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.67. G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	G2D_RST G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING Gating Clock for G2D 0: Mask 1: Pass

3.3.5.68. EVE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0650			Register Name: EVE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_EVE 1: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1)

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			The range of M is from 1 to 16.

3.3.5.69. EVE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x065C			Register Name: EVE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EVE_RST EVE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EVE_GATING Gating Clock for EVE 0: Mask 1: Pass

3.3.5.70. GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x0670			Register Name: GPU_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_GPU 1: /
23:3	/	/	/
2:0	R/W	0x0	FACTOR_ M Factor M.(M= FACTOR_ M +1) The range of M is from 1 to 8.

3.3.5.71. GPU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x067C			Register Name: GPU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/

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16	R/W	0x0	GPU_RST GPU Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPU_GATING Gating Clock for GPU 0: Mask 1: Pass

3.3.5.72. CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: OSC24M 1: PLL_PERI0(2X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.73. CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CE_RST

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			CE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CE_GATING Gating Clock for CE 0: Mask 1: Pass

3.3.5.74. VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_VE 1: /
23:3	/	/	/
2:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 8.

3.3.5.75. VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VE_RST VE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING Gating Clock For VE 0: Mask 1: Pass

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3.3.5.76. DMA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMA_RST DMA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING Gating Clock for DMA 0: Mask 1: Pass

3.3.5.77. MSGBOX Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x071C			Register Name: MSGBOX_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MSGBOX_RST MSGBOX Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MSGBOX_GATING Gating Clock for MSGBOX 0: Mask 1: Pass

3.3.5.78. SPINLOCK Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x072C			Register Name: SPINLOCK_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SPINLOCK_RST SPINLOCK Reset 0: Assert 1: De-assert
15:1	/	/	/

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0	R/W	0x0	SPINLOCK_GATING Gating Clock for SPINLOCK 0: Mask 1: Pass

3.3.5.79. HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST HSTIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HSTIMER_GATING Gating Clock for HSTIMER 0: Mask 1: Pass

3.3.5.80. AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.5.81. DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST DBGSYS Reset 0: Assert 1: De-assert
15:1	/	/	/

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0	R/W	0x0	DBGSYS_GATING Gating Clock for DBGSYS 0: Mask 1: Pass

3.3.5.82. PSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x079C			Register Name: PSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PSI_RST PSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PSI_GATING Gating Clock for PSI 0: Mask 1: Pass

3.3.5.83. PWM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			Register Name: PWM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PWM_RST PWM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING Gating Clock for PWM 0: Mask 1: Pass

3.3.5.84. DRAM Clock Register (Default Value: 0x0100_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	MODULE_RST

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			Module Reset 0: Assert 1: De-assert SCLK = Clock Source/M.
29:28	/	/	/
27	R/WAC	0x0	SDRCLK_UPD SDRCLK Configuration 0 Update 0:Invalid 1:Valid **NOTE** **Setting this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid.**
26	/	/	/
25:24	R/W	0x1	CLK_SRC_SEL Clock Source Select 00: PLL_DDR0 01: PLL_DDR1 Others: /
23:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 4.

3.3.5.85. MBUS Master Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	EVE_MCLK_GATING Gating MBUS Clock for EVE 0: Mask 1: Pass
20	R/W	0x0	ISP_MCLK_GATING Gating MBUS Clock for ISP 0: Mask 1: Pass
19:14	/	/	/
11	R/W	0x0	DI_MCLK_GATING Gating MBUS Clock for DI 0: Mask 1: Pass
10	R/W	0x0	G2D_MCLK_GATING

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			Gating MBUS Clock for G2D 0: Mask 1: Pass
9	/	/	/
8	R/W	0x0	CSI_MCLK_GATING Gating MBUS Clock for CSI 0: Mask 1: Pass
7	R/W	0x0	TVD_MCLK_GATING Gating MBUS Clock for TVD 0: Mask 1: Pass
6	/	/	/
5	R/W	0x0	NAND_MCLK_GATING Gating MBUS Clock for NAND 0: Mask 1: Pass
4	/	/	/
3	R/W	0x0	TS_MCLK_GATING Gating MBUS Clock for TS 0: Mask 1: Pass
2	R/W	0x0	CE_MCLK_GATING Gating MBUS Clock for CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_GATING Gating MBUS Clock for VE 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_GATING Gating MBUS Clock for DMA 0: Mask 1: Pass

3.3.5.86. PLL_DDR Auxiliary Register (Default Value: 0x0000_0001)

Offset: 0x0808			Register Name: PLL_DDR_AUX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
4	R/W	0x0	PLL_DDR1 Register Clock1 Option 0: 24M_SYS 1: 24M_PLL_DDR1

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3:2	/	/	/
1	R/W	0x0	PLL_DDR1 Register Clock2 Option 0: 24M_SYS 1: 24M_PLL_DDR1
0	R/W	0x1	PLL_DDR1 RST PLL_DDR1 Reset 0: Assert 1: De-assert

3.3.5.87. DRAM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DRAM_RST DRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DRAM_GATING Gating Clock for DRAM 0: Mask 1: Pass

3.3.5.88. NAND Clock0 Register (Default Value: 0x0000_0000)

Offset: 0x0810			Register Name: NAND_CLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/

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23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.89. NAND Clock1 Register (Default Value: 0x0000_0000)

Offset: 0x0814			Register Name: NAND_CLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

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3.3.5.90. NAND Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x082C			Register Name: NAND_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NAND_RST NAND Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NAND_GATING Gating Clock for NAND 0: Mask 1: Pass

3.3.5.91. SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830			Register Name: SMHC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

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3.3.5.92. SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16

3.3.5.93. SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /

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23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.94. SMHC3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x083C			Register Name: SMHC3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(2X) 010: PLL_PERI1(2X) 011: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

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3.3.5.95. SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	SMHC3_RST SMHC3 Reset 0: Assert 1: De-assert
18	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST SMHC1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST SMHC0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	SMHC3_GATING Gating Clock for SMHC3 0: Mask 1: Pass
2	R/W	0x0	SMHC2_GATING Gating Clock for SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING Gating Clock for SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING Gating Clock for SMHC0 0: Mask 1: Pass

3.3.5.96. UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:21	/	/	/
20	R/W	0x0	UART4_RST UART4 Reset 0: Assert 1: De-assert
19	R/W	0x0	UART3_RST UART3 Reset 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST UART2 Reset 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST UART1 Reset 0: Assert 1: De-assert
16	R/W	0x0	UART0_RST UART0 Reset 0: Assert 1: De-assert
15:5	/	/	/
4	R/W	0x0	UART4_GATING Gating Clock for UART4 0: Mask 1: Pass
3	R/W	0x0	UART3_GATING Gating Clock for UART3 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING Gating Clock for UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING Gating Clock for UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING Gating Clock for UART0 0: Mask 1: Pass

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3.3.5.97. TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	TWI6_RST TWI6 Reset 0: Assert 1: De-assert
21	R/W	0x0	TWI5_RST TWI5 Reset 0: Assert 1: De-assert
20	R/W	0x0	TWI4_RST TWI4 Reset 0: Assert 1: De-assert
19	R/W	0x0	TWI3_RST TWI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST TWI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TWI0_RST TWI0 Reset 0: Assert 1: De-assert
15:7	/	/	/
6	R/W	0x0	TWI6_GATING Gating Clock for TWI6 0: Mask 1: Pass
5	R/W	0x0	TWI5_GATING Gating Clock for TWI5 0: Mask 1: Pass
4	R/W	0x0	TWI4_GATING Gating Clock for TWI4 0: Mask

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			1: Pass
3	R/W	0x0	TWI3_GATING Gating Clock for TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING Gating Clock for TWI2 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING Gating Clock for TWI1 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING Gating Clock for TWI0 0: Mask 1: Pass

3.3.5.98. SCR Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x093C			Register Name: SCR_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SCR_RST SCR Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	SCR_GATING Gating Clock for SCR 0: Mask 1: Pass

3.3.5.99. SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.

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30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.100. SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			**Register Name: SPI1_CLK_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_PERI1(1X) 011: PLL_PERI0(2X) 100: PLL_PERI1(2X) 1XX:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2

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			10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.101. SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	SPI1_RST SPI1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SPI0_RST SPI0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	SPI1_GATING Gating Clock for SPI1 0: Mask 1: Pass
0	R/W	0x0	SPI0_GATING Gating Clock for SPI0 0: Mask 1: Pass

3.3.5.102. EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EMAC_RST EMAC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EMAC_GATING Gating Clock for EMAC

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			0: Mask 1: Pass

3.3.5.103. TS Clock Register (Default Value: 0x0000_0000)

Offset: 0x09B0			Register Name: TS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: OSC24M 1: PLL_PERI0(1X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_ M Factor M.(M= FACTOR_ M +1) The range of M is from 1 to 16.

3.3.5.104. TS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09BC			Register Name: TS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TS_RST TS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TS_GATING Gating Clock for TS 0: Mask

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			1: Pass

3.3.5.105. GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			Register Name: GPADC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GPADC_RST GPADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC_GATING Gating Clock for GPADC 0: Mask 1: Pass

3.3.5.106. I2S/PCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A10			Register Name: I2S/PCM0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

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3.3.5.107. I2S/PCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A14			Register Name: I2S/PCM1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.108. I2S/PCM2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A18			Register Name: I2S/PCM2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N

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			Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.109. I2S/PCM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A1C			Register Name: I2S/PCM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	I2S/PCM2_RST I2S/PCM2 Reset 0: Assert 1: De-assert
17	R/W	0x0	I2S/PCM1_RST I2S/PCM1 Reset 0: Assert 1: De-assert
16	R/W	0x0	I2S/PCM0_RST I2S/PCM0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	I2S/PCM2_GATING Gating Clock for I2S/PCM2 0: Mask 1: Pass
1	R/W	0x0	I2S/PCM1_GATING Gating Clock for I2S/PCM1 0: Mask 1: Pass
0	R/W	0x0	I2S/PCM0_GATING Gating Clock for I2S/PCM0 0: Mask 1: Pass

3.3.5.110. OWA Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A20			Register Name: OWA_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.111. OWA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A2C			Register Name: OWA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	OWA_RST OWA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	OWA_GATING Gating Clock For OWA 0: Mask 1: Pass

3.3.5.112. DMIC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A40			Register Name: DMIC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock

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			0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.113. DMIC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A4C			Register Name: DMIC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMIC_RST DMIC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMIC_GATING Gating Clock for DMIC 0: Mask 1: Pass

3.3.5.114. AUDIO CODEC 1X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A50			Register Name: AUDIO_CODEC_1X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

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			SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The factor of M is from 1 to 16.

3.3.5.115. AUDIO CODEC 4X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A54			Register Name: AUDIO_CODEC_4X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: PLL_AUDIO(8X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The factor of M is from 1 to 16.

3.3.5.116. AUDIO CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A5C			Register Name: AUDIO_CODEC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST AUDIO_CODEC Reset 0: Assert

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			1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING Gating Clock For AUDIO_CODEC 0: Mask 1: Pass

3.3.5.117. USB2.0_OTG Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USB2.0_OTG_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_USB2.0_OTG_OHCI Gating Special Clock for USB2.0_OTG_OHCI 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB2.0_OTG_PHY_RST USB2.0_OTG PHY Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USB2.0_OTG_PHY Gating Special Clock for USB2.0_OTG PHY 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M
28:26	/	/	/
25:24	R/W	0x0	USB2.0_OTG_OHCI_12M_SRC_SEL USB2.0_OTG_OHCI 12M Source Select 00: 12MHz divided from 48MHz 01: 12MHz divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.118. USB2.0_HOST1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A74			Register Name: USB2.0_HOST1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_USB2.0_HOST1_OHCI Gating Special Clock for USB2.0_HOST1_OHCI 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB2.0_HOST1_PHY_RST

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			USB2.0_HOST1 PHY Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USB2.0_HOST1_PHY Gating Special Clock for USB2.0_HOST1 PHY 0: Clock is OFF 1: Clock is ON
28:26	/	/	/
25:24	R/W	0x0	USB2.0_HOST1_OHCI_12M_SRC_SEL USB2.0_HOST1_OHCI 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.119. USB2.0_HOST2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A78			Register Name: USB2.0_HOST2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_USB2.0_HOST2_OHCI Gating Special Clock for USB2.0_HOST2_OHCI 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB2.0_HOST2_PHY_RST USB2.0_HOST2 PHY Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USB2.0_HOST2_PHY Gating Special Clock for USB2.0_HOST2 PHY 0: Clock is OFF 1: Clock is ON
28:26	/	/	/
25:24	R/W	0x0	USB2.0_HOST2_OHCI_12M_SRC_SEL USB2.0_HOST2_OHCI 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

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3.3.5.120. USB2.0_HOST3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A7C			Register Name: USB2.0_HOST3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_USB2.0_HOST3_OHCI Gating Special Clock for USB2.0_HOST3_OHCI 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USB2.0_HOST3_PHY_RST USB2.0_HOST3 PHY Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USB2.0_HOST3_PHY Gating Special Clock for USB2.0_HOST3 PHY 0: Clock is OFF 1: Clock is ON
28	R/W	0x0	USBHSIC_RST USB HSIC Reset 0: Assert 1: De-assert
27	R/W	0x0	SCLK_GATING_12M_HSIC Gating Special 12M Clock for HSIC 0: Clock is OFF 1: Clock is ON SCLK is OSC24M/2
26	R/W	0x0	SCK_GATING_HSIC Gating Special Clock for HSIC 0: Clock is OFF 1: Clock is ON The special clock is from PLL_HSIC
25:24	R/W	0x0	USB2.0_HOST3_OHCI_12M_SRC_SEL USB2.0_HOST3_OHCI 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.121. USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	USB2.0_OTG_RST

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			USB2.0_OTG Reset 0: Assert 1: De-assert
23	R/W	0x0	USB2.0_HOST3_EHCI_RST USB2.0_HOST3_EHCI Reset 0: Assert 1: De-assert
22	R/W	0x0	USB2.0_HOST2_EHCI_RST USB2.0_HOST2_EHCI Reset 0: Assert 1: De-assert
21	R/W	0x0	USB2.0_HOST1_EHCI_RST USB2.0_HOST1_EHCI Reset 0: Assert 1: De-assert
20	R/W	0x0	USB2.0_OTG_EHCI_RST USB2.0_OTG_EHCI Reset 0: Assert 1: De-assert
19	R/W	0x0	USB2.0_HOST3_OHCI_RST USB2.0_HOST3_OHCI Reset 0: Assert 1: De-assert
18	R/W	0x0	USB2.0_HOST2_OHCI_RST USB2.0_HOST2_OHCI Reset 0: Assert 1: De-assert
17	R/W	0x0	USB2.0_HOST1_OHCI_RST USB2.0_HOST1_OHCI Reset 0: Assert 1: De-assert
16	R/W	0x0	USB2.0_OTG_OHCI_RST USB2.0_OTG_OHCI Reset 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USB2.0_OTG_GATING Gating Clock For USB2.0_OTG 0: Mask 1: Pass
7	R/W	0x0	USB2.0_HOST3_EHCI_GATING Gating Clock For USB2.0_HOST3_EHCI 0: Mask 1: Pass
6	R/W	0x0	USB2.0_HOST2_EHCI_GATING

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			Gating Clock For USB2.0_HOST2_EHCI 0: Mask 1: Pass
5	R/W	0x0	USB2.0_HOST1_EHCI_GATING Gating Clock For USB2.0_HOST1_EHCI 0: Mask 1: Pass
4	R/W	0x0	USB2.0_OTG_EHCI_GATING Gating Clock For USB2.0_OTG_EHCI 0: Mask 1: Pass
3	R/W	0x0	USB2.0_HOST3_OHCI_GATING Gating Clock For USB2.0_HOST3_OHCI 0: Mask 1: Pass
2	R/W	0x0	USB2.0_HOST2_OHCI_GATING Gating Clock For USB2.0_HOST2_OHCI 0: Mask 1: Pass
1	R/W	0x0	USB2.0_HOST1_OHCI_GATING Gating Clock For USB2.0_HOST1_OHCI 0: Mask 1: Pass
0	R/W	0x0	USB2.0_OTG_OHCI_GATING Gating Clock For USB2.0_OTG_OHCI 0: Mask 1: Pass

3.3.5.122. MIPI DSI Host Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: MIPI_DSI_HOST_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: PLL_PERI0(1X) 1: PLL_PERI0(2X)
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M

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			Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.123. MIPI DSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: MIPI_DSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MIPI_DSI_RST MIPI_DSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MIPI_DSI_GATING Gating Clock For MIPI_DSI 0: Mask 1: Pass

3.3.5.124. DISPLAY_IF_TOP Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B5C			Register Name: DISPLAY_IF_TOP_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DISPLAY_IF_TOP_RST DISPLAY_IF_TOP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DISPLAY_IF_TOP_GATING Gating Clock For DISPLAY_IF_TOP 0: Mask 1: Pass

3.3.5.125. TCON LCD0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCON_LCD0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON

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			SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others:/
23:0	/	/	/

3.3.5.126. TCON LCD1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B64			Register Name: TCON_LCD1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others:/
23:0	/	/	/

3.3.5.127. TCON LCD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCON_LCD_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	TCON_LCD1_RST TCON_LCD1 Reset 0: Assert 1: De-assert
16	R/W	0x0	TCON_LCD0_RST

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			TCON_LCD0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	TCON_LCD1_GATING Gating Clock for TCON_LCD1 0: Mask 1: Pass
0	R/W	0x0	TCON_LCD0_GATING Gating Clock for TCON_LCD0 0: Mask 1: Pass

3.3.5.128. TCON TV Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0B9C			Register Name: TCON_TV_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TCON_TV_RST TCON_TV Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_TV_GATING Gating Clock for TCON_TV 0: Mask 1: Pass

3.3.5.129. LVDS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BAC			Register Name: LVDS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	LVDS_RST LVDS Reset 0: Assert 1: De-assert
15:1	/	/	/

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3.3.5.130. TVE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BB0			Register Name: TVE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) 110: PLL_MIPI Others:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The value of M is from 1 to 16.

3.3.5.131. TVE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BBC			Register Name: TVE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	TVE_RST TVE Reset 0: Assert 1: De-assert
16	R/W	0x0	TVE_TOP_RST TVE_TOP Reset 0: Assert 1: De-assert

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15:2	/	/	/
1	R/W	0x0	TVE_GATING Gating Clock for TVE 0: Mask 1: Pass
0	R/W	0x0	TVE_TOP_GATING Gating Clock for TVE_TOP 0: Mask 1: Pass

3.3.5.132. TVD0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BC0			Register Name: TVD0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_ M Factor M.(M= FACTOR_ M +1) The range of M is from 1 to 16.

3.3.5.133. TVD1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BC4	Register Name: TVD1_CLK_REG

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_ M Factor M.(M= FACTOR_ M +1) The range of M is from 1 to 16.

3.3.5.134. TVD2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BC8			Register Name: TVD2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) Others: /
23:10	/	/	/

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9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.135. TVD3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0BCC			Register Name: TVD3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(2X) 010: PLL_VIDEO1(1X) 011: PLL_VIDEO1(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.136. TVD Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0BDC	Register Name: TVD_BGR_REG

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Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	TVD3_RST TVD3 Reset 0: Assert 1: De-assert
19	R/W	0x0	TVD2_RST TVD2 Reset 0: Assert 1: De-assert
18	R/W	0x0	TVD1_RST TVD1 Reset 0: Assert 1: De-assert
17	R/W	0x0	TVD0_RST TVD0 Reset 0: Assert 1: De-assert
16	R/W	0x0	TVD_TOP_RST TVD_TOP Reset 0: Assert 1: De-assert
15:6	/	/	/
4	R/W	0x0	TVD3_GATING Gating Clock for TVD3 0: Mask 1: Pass
3	R/W	0x0	TVD2_GATING Gating Clock for TVD2 0: Mask 1: Pass
2	R/W	0x0	TVD1_GATING Gating Clock for TVD1 0: Mask 1: Pass
1	R/W	0x0	TVD0_GATING Gating Clock for TVD0 0: Mask 1: Pass
0	R/W	0x0	TVD_TOP_GATING Gating Clock for TVD_TOP 0: Mask 1: Pass

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3.3.5.137. CSI MISC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C00			Register Name: CSI_MISC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	CSI_CCI2_CCI3_CLK_GATING Gating CCI2 and CCI3 Special Clock Clock source is OSC24M. 0: Clock is OFF 1: Clock is ON
1	/	/	/
0	R/W	0x0	CSI_CCI0_CCI1_CLK_GATING Gating CCI0 and CCI1 Special Clock Clock source is OSC24M. 0: Clock is OFF 1: Clock is ON

3.3.5.138. CSI TOP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_TOP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000:PLL_VIDEO0(1X) 001:PLL_ISP 010:PLL_VE 011:PLL_PERI0(1X) Others:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

3.3.5.139. CSI Master Clock0 Register (Default Value: 0x0000_0000)

Offset: 0x0C08	Register Name: CSI_MST_CLK0_REG

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MCLK0_GATING Gating CSI Master Clock0 This clock is output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(2X) 011: PLL_PERI1(1X) 100: PLL_ISP Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 32.

3.3.5.140. CSI Master Clock1 Register (Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI_MST_CLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK1_GATING Gating CSI Master Clock1 This clock is output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(2X) 011: PLL_PERI1(1X) 100: PLL_ISP Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 32.

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3.3.5.141. CSI Master Clock2 Register (Default Value: 0x0000_0000)

Offset: 0x0C10			Register Name: CSI_MST_CLK2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK2_GATING Gating CSI Master Clock2 This clock is output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(2X) 011: PLL_PERI1(1X) 100: PLL_ISP Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 32.

3.3.5.142. CSI Master Clock3 Register (Default Value: 0x0000_0000)

Offset: 0x0C14			Register Name: CSI_MST_CLK3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK3_GATING Gating CSI Master Clock3 This clock is output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_VIDEO0(1X) 010: PLL_PERI0(2X) 011: PLL_PERI1(1X) 100: PLL_ISP

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			Others:/
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 32.

3.3.5.143. CSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0C2C			Register Name: CSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI_RST CSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING Gating Clock for CSI 0: Mask 1: Pass

3.3.5.144. MIPI_RX Clock Register (Default Value: 0x0000_0000)

Offset: 0x0C30			Register Name: MIPI_RX_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_GATING Gating Clock for MIPI_RX 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00:PLL_VIDEO0(1X) 01:PLL_PERI0(1X) 10:PLL_ISP 11:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) The range of M is from 1 to 16.

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3.3.5.145. CCU Security Switch Register (Default Value: 0x0000_0000)

Offset: 0x0F00			Register Name: CCU_SEC_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MBUS_SEC MBUS Clock Register Security 0: Secure 1: Non-secure
1	R/W	0x0	BUS_SEC Bus Relevant Registers Security 0: Secure 1: Non-secure
0	R/W	0x0	PLL_SEC PLL Relevant Registers Security 0: Secure 1: Non-secure

3.3.5.146. PLL Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0F04			Register Name: PLL_LOCK_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBG_EN Debug Enable 0: Disable 1: Enable
30:25	/	/	/
24:20	R/W	0x0	DBG_SEL Debug Select 00000: PLL_C0_CPUX 00001: PLL_C1_CPUX 00010: PLL_DDR0 00011:PLL_DDR1 00100: PLL_PERI0 00101: PLL_PERI1 00110:PLL_GPU 00111:/ 01000: PLL_VIDEO0 01001: PLL_VIDEO1 01010: / 01011: PLL_VE 01100: PLL_DE 01101: PLL_ISP 01110: PLL_HSIC

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			01111: PLL_AUDIO 10000: PLL_MIPI 10001: / 10010: / 10011: / 10100: / 10101: / 10110: / 10111: / 11000: PLL_EVE 11001: / 11010: / Others: /
19	/	/	/
18:17	R/W	0x0	UNLOCK_LEVEL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
16	R/W	0x0	LOCK_LEVEL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles
15:0	/	/	/

3.3.5.147. Frequency Detect Control Register (Default Value: 0x0000_0020)

Offset: 0x0F08			**Register Name: FRE_DET_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	ERROR_FLAG Error Flag 0: Write 0 to clear 1: Error
30:9	/	/	/
8:4	R/W	0x2	Detect Time Time=1/32k*(2^RegValue) **NOTE** **RegValue is from 0 to 16.**
3:2	/	/	/
1	R/W	0x0	FRE_DET_IRQ_EN Frequence Detect IRQ Enable 0: Disable 1: Enable

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0	R/W	0x0	FRE_DET_FUN_EN Frequence Detect Function Enable 0: Disable 1: Enable

3.3.5.148. Frequence Up Limit Register (Default Value: 0x0000_0000)

Offset: 0x0F0C			Register Name: FRE_UP_LIM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRE_UP_LIM. Frequence Up Limit. **NOTE** **The register must be an integral multiple of 32. The unit is kHz.**

3.3.5.149. Frequence Down Limit Register (Default Value: 0x0000_0000)

Offset: 0x0F10			Register Name: FRE_DOWN_LIM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRE_DOWN_LIM. Frequence Down Limit. **NOTE** **The register must be an integral multiple of 32. The unit is kHz.**

3.3.5.150. 24M Clock Output Register (Default Value: 0x0000_0000)

Offset: 0x0F20			Register Name: 24M_CLK_OUTPUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	24M_CLK_OUTPUT_EN 24M Clock Output enable 0: Disable 1: Enable
30:0	/	/	/

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3.4. BROM System

3.4.1. Overview

The BROM system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) which could be considered the primary program-loader. On startup process, the T7 starts to fetch the first instruction from address 0x0, where is the BROM located at.

The BROM system is split up into two parts :FEL and Media Boot. The task of FEL is to write the external data to the local NVM, the task of the Media Boot is to load an effective and legitimate BOOT0 from NVM and running.

The BROM system includes the following features:

- CPU0 boot process and NON_CPU0 boot process
- Super super standby wakeup process
- Hotplug process
- Mandatory upgrade process through SMHC0 and USB
- GPIO pin or eFuse to select the kind of boot media to boot
- Supports normal boot and secure boot
- Secure BROM : loads only certified firmware
- Secure BROM : ensures that the Secure Boot is a trusted environment

3.4.2. Operations and Functional Descriptions

3.4.2.1. Boot Media Select

The BROM system supports the following boot media:

- SD/MMC
- NAND FLASH
- SPI NOR FLASH
- SPI NAND FLASH

There are two ways of boot select: GPIO pin select and eFuse select. The BROM will read the state of BOOT_MODE , according to the state of BOOT_MODE to decide whether GPIO pin or eFuse to select the kind of boot media to boot. The BOOT_MODE is actually a bit in the SID. Table 3-4 shows BOOT_MODE setting.

Table 3- 4. BOOT_MODE Setting

BOOT_MODE	Boot Select Type
0	GPIO pin select
1	eFuse select

If the state of the BOOT_MODE is 0,that is to choose the GPIO type ,GPIO type has two pins to select which media to

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boot. Table 3-5 shows GPIO Pin Boot Select Setting.

Table 3- 5. GPIO Pin Boot Select Setting

Pin_Boot_Select[1:0]	Boot media
00	SMHC0-> NAND FLASH
01	SMHC0-> SMHC2
10	SMHC0-> SPI NAND->SPI NOR
11	SMHC0->SMHC2->NAND FLASH->SPI NAND->SPI NOR

If the state of the BOOT_MODE is 1,that is to choose the eFuse type .eFuse type has one 12 bits configuration, every 3 bits is divided into a group of the Boot Select ,so it has four groups of boot_select .Table 3-6 shows eFuse Boot Select Configure.

Table 3- 6. eFuse Boot Select Configure

eFuse_Boot_Select_Cfg[11:0]	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

Table 3-7 describes each group of the eFuse Boot Select Setting. The first group to the third group are the same settings,but the fourth group need to be careful.If eFuse_Boot_Select_4 is set to 111,that means the way of the *Try*.The way of *Try* is followed by SMHC0,SMHC2,NAND FLASH,SPI NAND,SPI NOR.

Table 3- 7. eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot Media
000	*Try*
001	NAND Flash
010	SMHC2
011	SPI NOR
100	SPI NAND
101	Reserved
110	Reserved
111	The next group of the eFuse_Boot_Select,when the n is equal to 4,it will be a way of *Try*.

3.4.2.2. Normal BROM and Secure BROM

If the System on Chip (SoC) has implemented the ARM TrustZone technology,when the Secure Enable Bit is enabled, the SoC will enable the the ARM TrustZone technology. The minimal security functionality an ARM TrustZone technology based system must implement for its Trusted Boot.

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So the BROM is divided into Normal Brom and Secure BROM. the Secure BROM protects against the potential threat of attackers modifying areas of code or data in programmable memory .

On startup,the SOC will read the Secure Enable Bit,if the bit is 0,then mapping Normal Brom code to address 0x0, or mapping Secure Brom code to address 0x0.

3.4.2.2.1. Normal BROM Process

In Normal boot mode,the system boot will start from CPU0 or NON_CPU0, BROM will read CPU ID number to distinguish CPU0 or NON_CPU0,then BROM will read the **Hotplug Flag Regsiter** and the **Supper Standby Flag Regsiter** ,according to the flag whether to go through the appropriate process.Finally,BROM will read the state of the FEL Pin,if the FEL Pin signal is detected to pull to high level, then the system will jump to the Try Media Boot process,or jump to the mandatory upgrade process. Figure 3-5 shows the Normal BROM Process.

NOTE

NON_CPU0 means the CPU core n(n>0).

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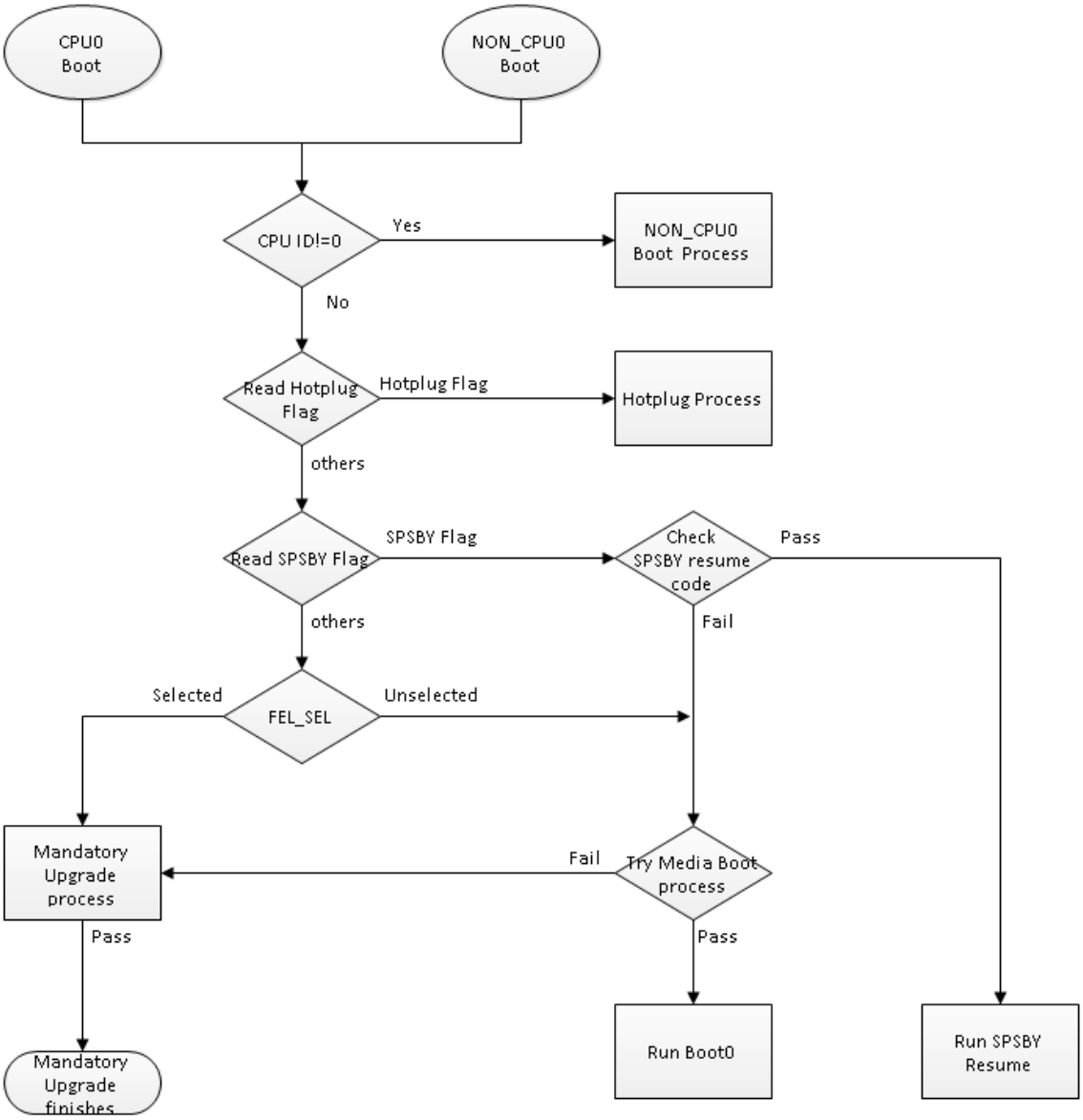

Figure 3- 5. Normal Mode Boot Process

3.4.2.2.2. Secure BROM Process

In Secure Boot mode, by comparison with Normal BROM,after the Try Media Boot Process finishes, the system will go to run Secure BROM Software.Figure 3-6 shows the Secure BROM Process.

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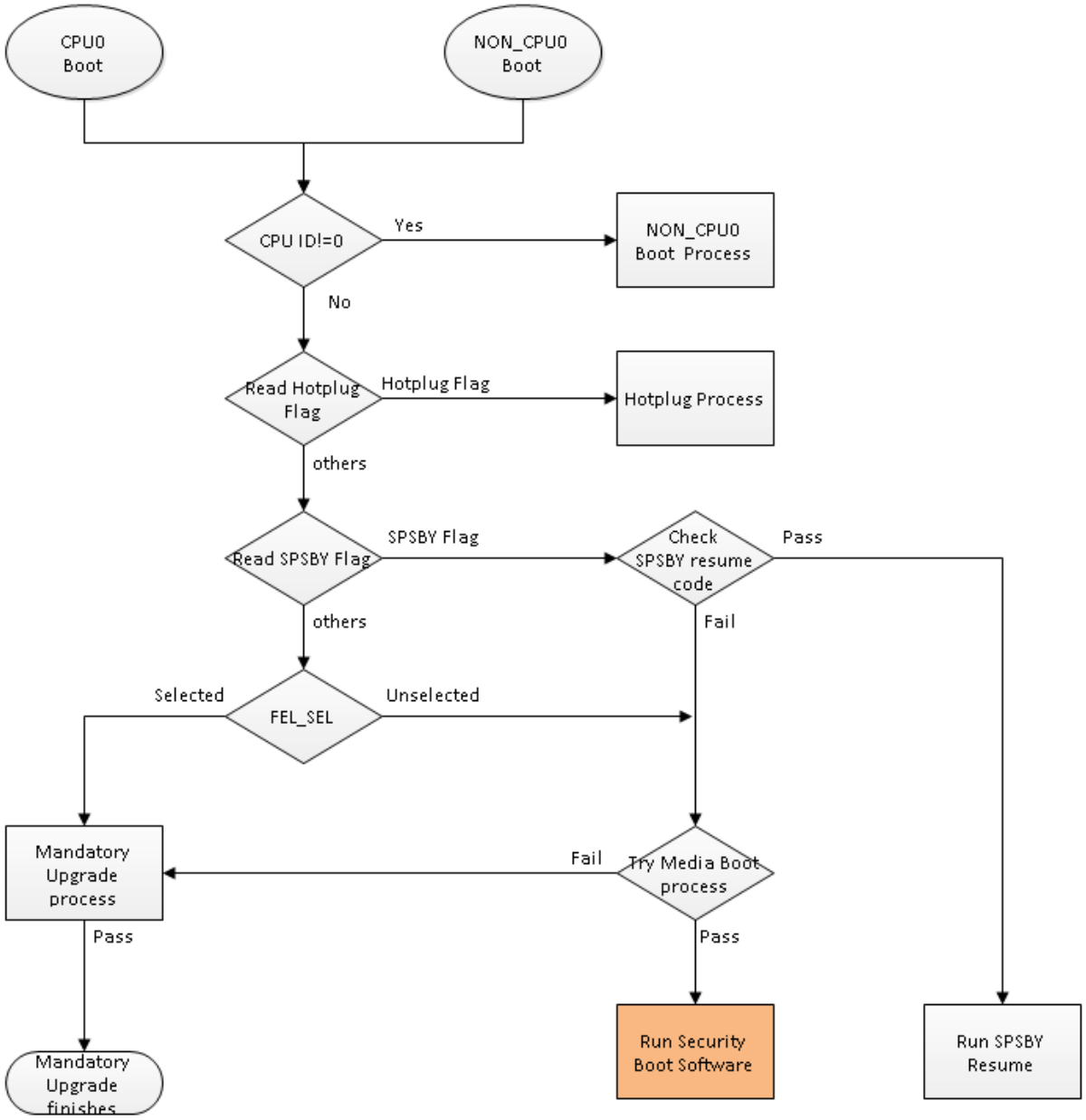

Figure 3- 6. Secure BROM Process Diagram

3.4.2.2.3. Secure BROM Requirement

The Secure BROM has the following some requirements:

- Supports X509 certificate
- Supports cryptographic algorithms
  - AES-128
  - SHA-256
  - RSA-2048
  - AES,DES
- Supports OTP/eFuse

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Before runing Security Boot software, the software must check whether it has been modified or replaced,so the system will check and verify the integrity of the certificate,because the certificate uses the RSA algorithm signature.The system also uses of the Crypto Engine (CE) hardware module to accelerate the speed of encryption and decryption.Using standard cryptography ensures that the firmware images can be trusted,so the Secure BROM ensures the system security state is as expected.

3.4.2.3. BROM System Process Description

3.4.2.3.1. NON_CPU0 Boot Process

If CPU ID is greater than 0,the system boot from boot from NON_CPU0, BROM will read the Soft Entry Address Register,then jump the Soft Entry Address,and run NON_CPU0 boot code. Figure 3-7 shows the NON_CPU0 Boot Process.

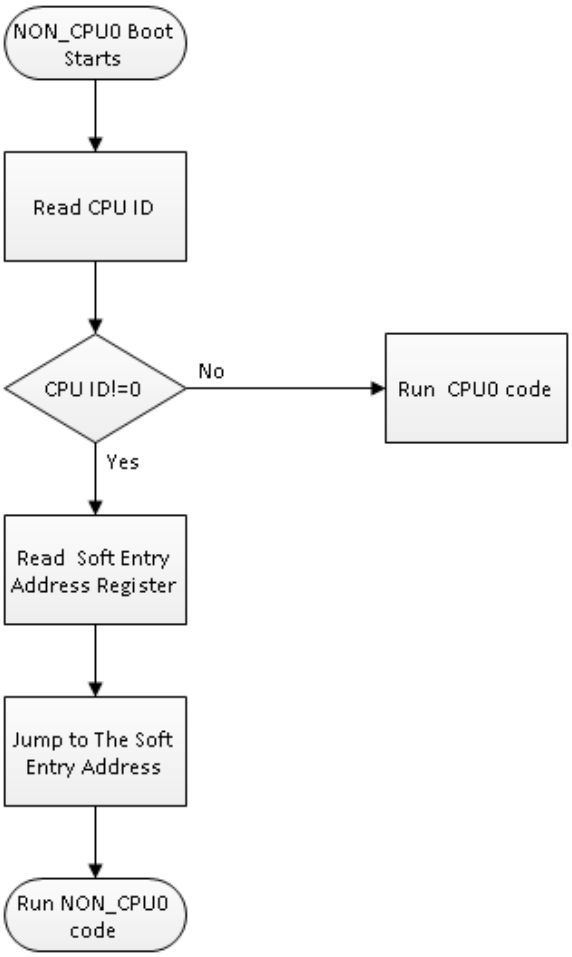

Figure 3- 7. NON_CPU0 Boot Process

NOTE

The Soft Entry Address Register is 0x070001BC.

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3.4.2.3.2. CPU0 Hot Plug Process

The Hot Plug Flag determines whether the system will do hotplug boot. If CPU Hotplug Flag value is equal to 0×FA50392F, then read the Soft Entry Register and the system will jump to the Soft Entry Address. Figure 3-8 shows the CPU0 Hotplug Process.

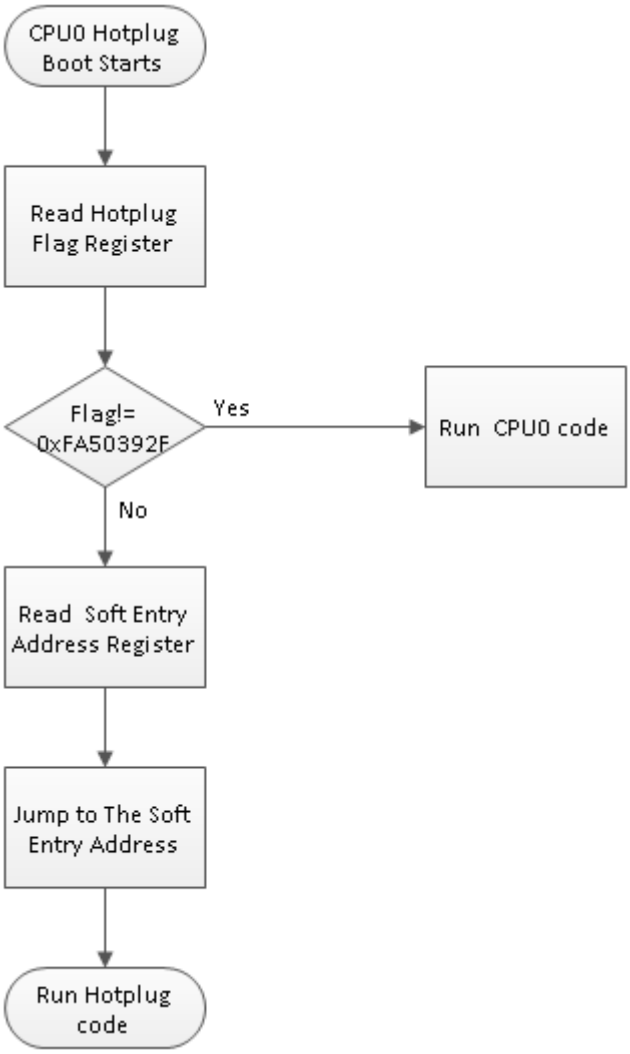

Figure 3- 8. CPU0 Hot Plug Process

NOTE

The Hotplug Flag Register is 0x030001B8. The Soft Entry Address Register is 0x070001BC.

3.4.2.3.3. Super Standby Wakeup Process

Super Standby(SPSBY) wakeup will be started by CPUs, and will be carried on by CPU0 after the CPU0 released. If the SPSBY register value is checked to be the SPSBY flag, then the system will go to SPSBY wakeup process.Figure 3-9 shows the SPSBY Wakeup Process.

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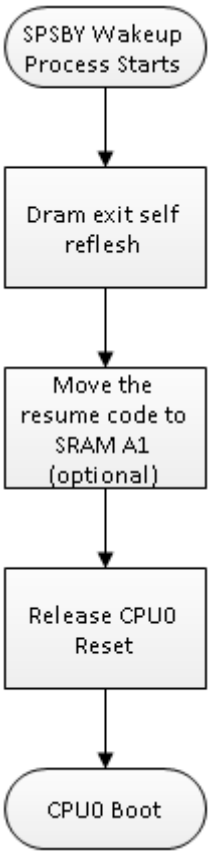

Figure 3- 9. SPSBY Wakeup Process

During the SPSBY wakeup, the system will first check the SPSBY resume code pointed by SPSBY resume code pointer.If it is right, then the system will run SPSBY wakeup, otherwise the system will jump to the Try Media Boot process. Figure 3-10 shows the SPSBY Resume Code Check Process.

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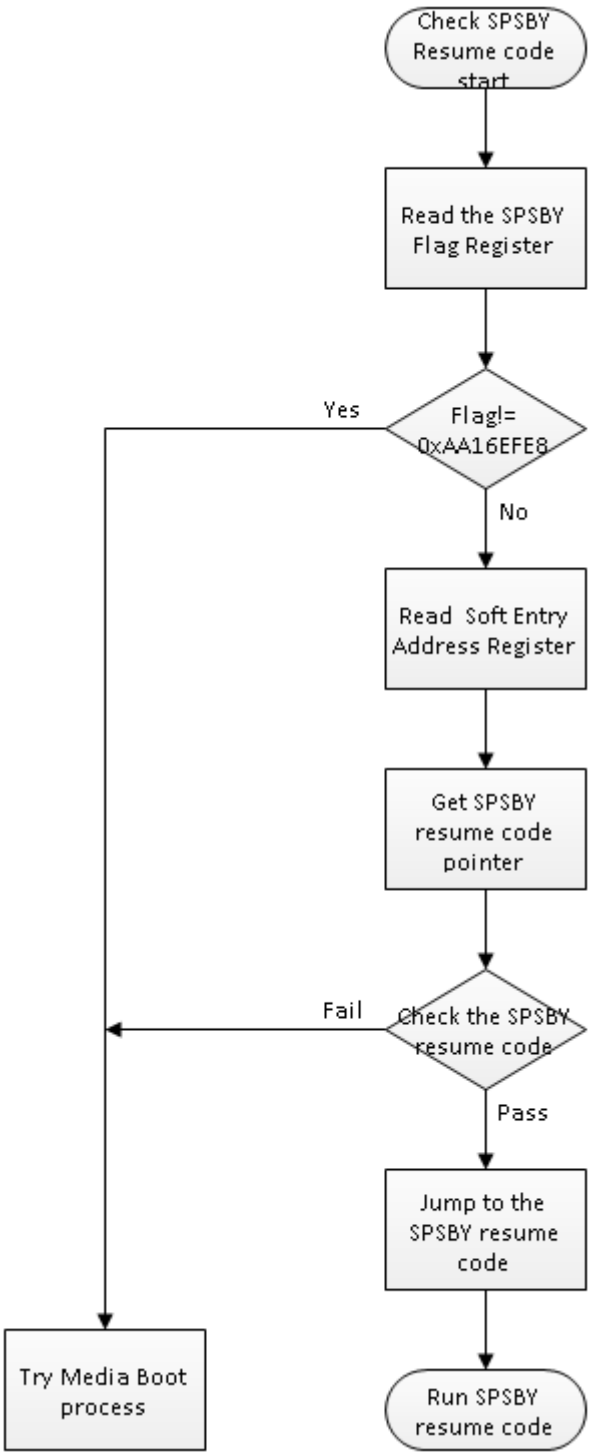

Figure 3- 10. SPSBY Resume Code Check Process

3.4.2.3.4. Mandatory Upgrade Process

If the FEL Pin signal is detected to pull low, then the system will jump to mandatory upgrade process. Figure 3-11 shows the mandatory upgrade process.

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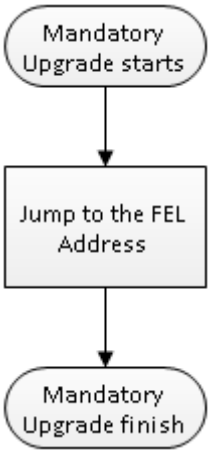

Figure 3- 11. Mandatory Upgrade Process

NOTE

The FEL address of the Normal BROM is 0x20. The FEL address of the Secure BROM is 0x60.

3.4.2.3.5. FEL Process

When the system chooses to enter Mandatory Upgrade Process, then the system will jump to the FEL process.Figure 3-12 shows the FEL upgrade process.

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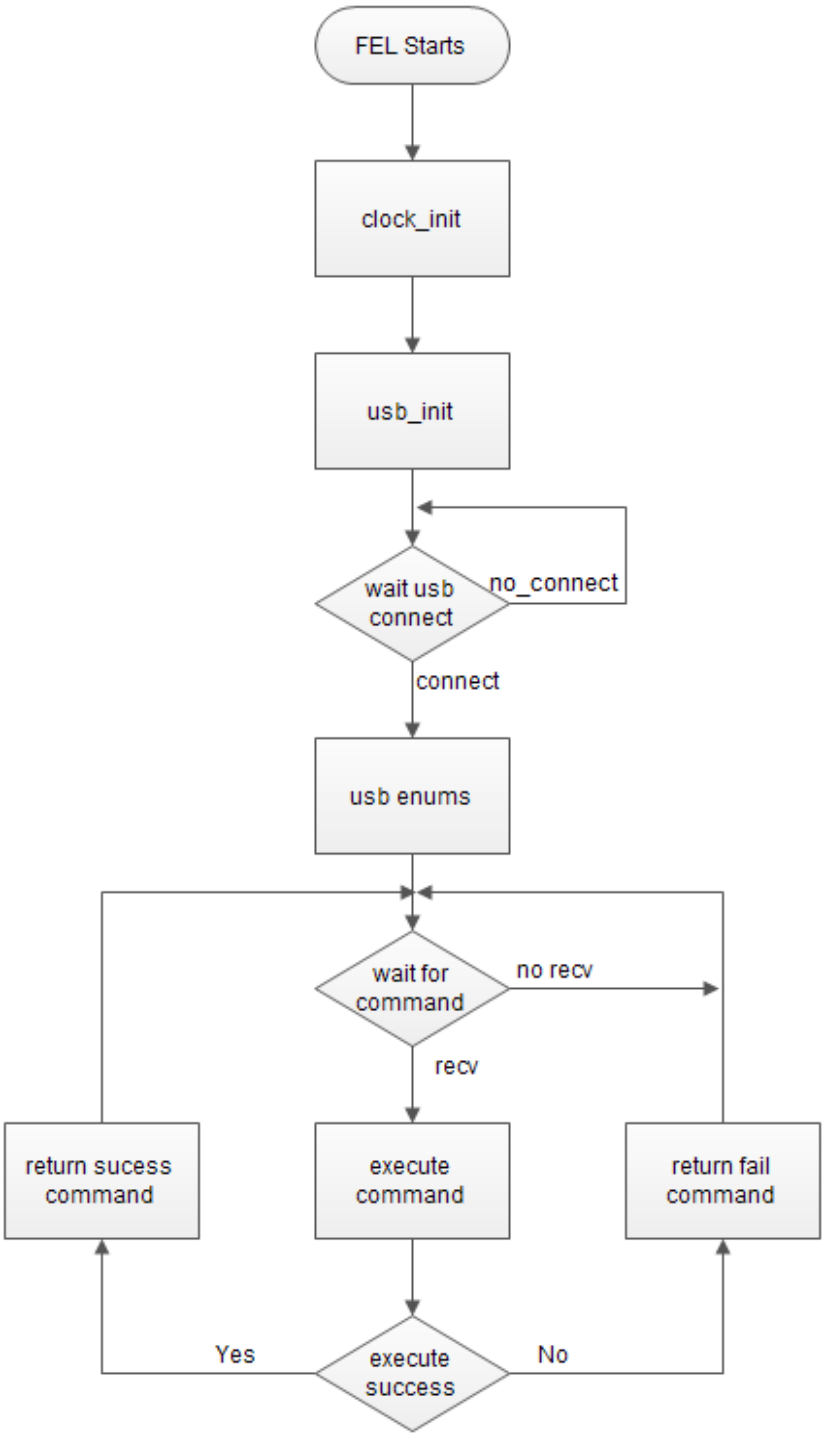

Figure 3- 12. USB FEL Process

3.4.2.3.6. Normal Try Media Boot Process

If the FEL Pin signal is detected to pull high, then the system will jump to the Try Media Boot Process.
Try Media Boot Process will read the state of BOOT_MODE register,according to the state of BOOT_MODE, GPIO pin or eFuse is descided to select which boot media to boot.Figure 3-13 shows Normal BROM GPIO Pin Boot Select Process.

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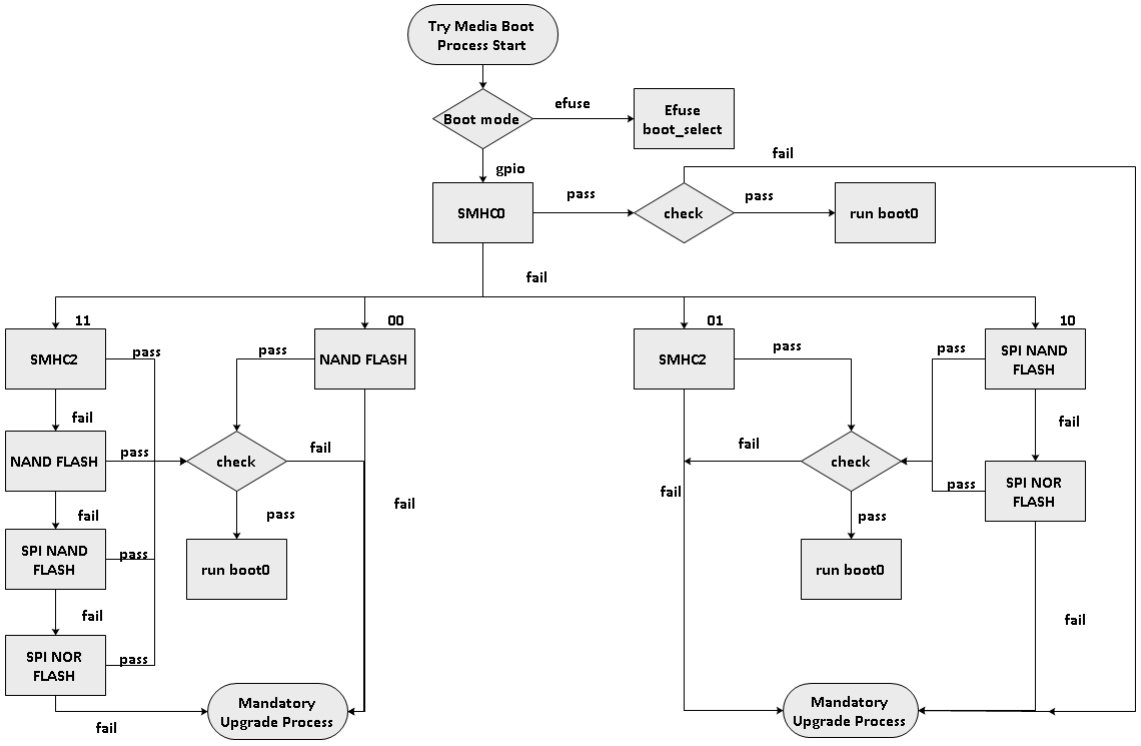

Figure 3- 13. Normal BROM GPIO Pin Boot Select Process

NOTE

SMHC0 is external SD/TF card. SMHC2 is external eMMC.

Figure 3-14 shows Normal BROM eFuse Boot Select Process.

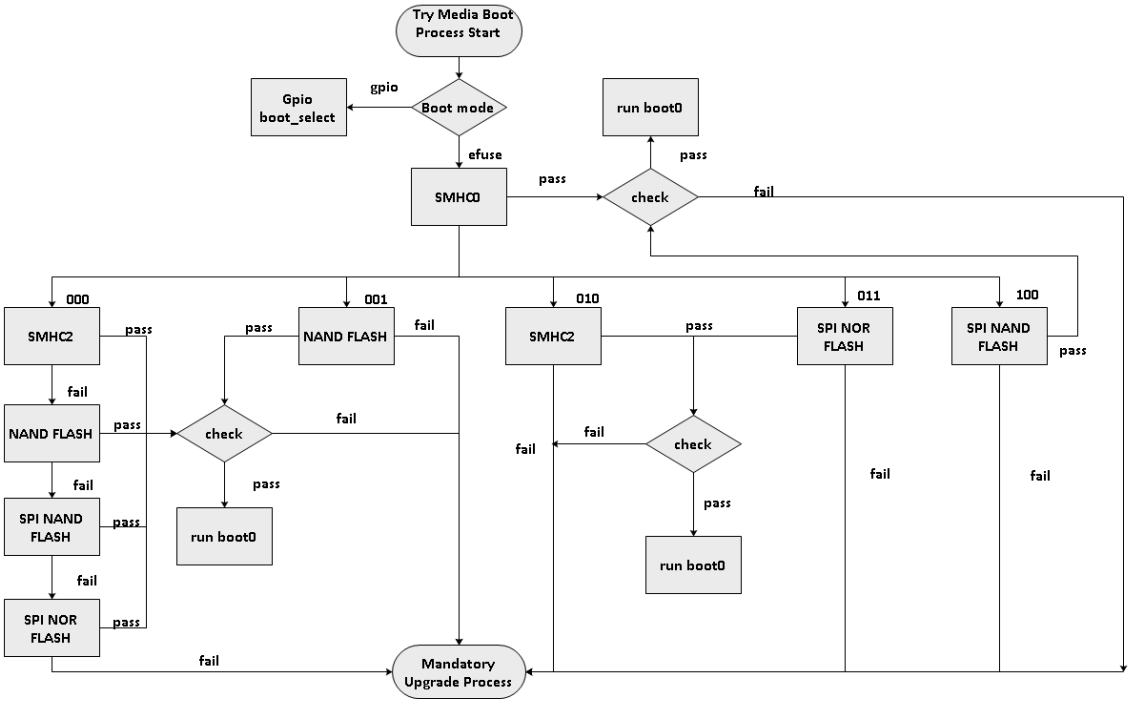

Figure 3- 14. Normal BROM eFuse Boot Select Process

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3.4.2.3.7. Secure Try Media Boot Process

By comparison with Normal Try Media Boot Process,the system will verify the integrity of the certificate ,if right, go to run Security BROM software,or go to the Mandatory Upgrade Process. Figure 3-15 shows Secure BROM GPIO Pin Boot Select Process.

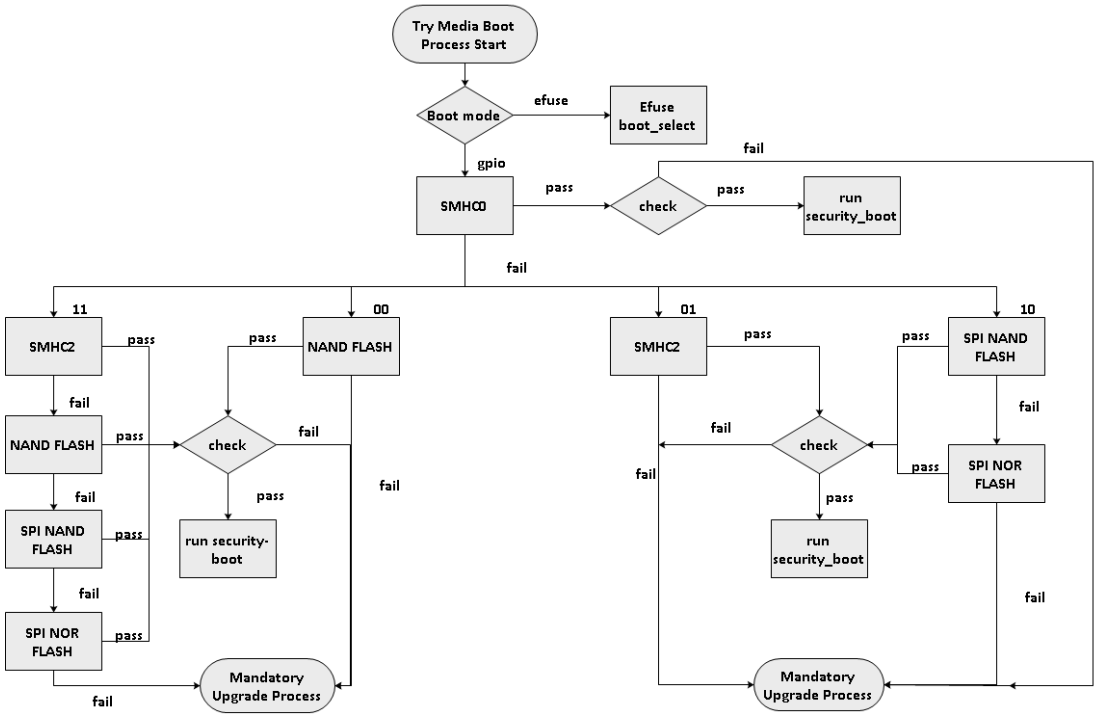

Figure 3- 15. Secure BROM GPIO Pin Boot Select Process

Figure 3-16 shows Secure BROM eFuse Boot Select Process.

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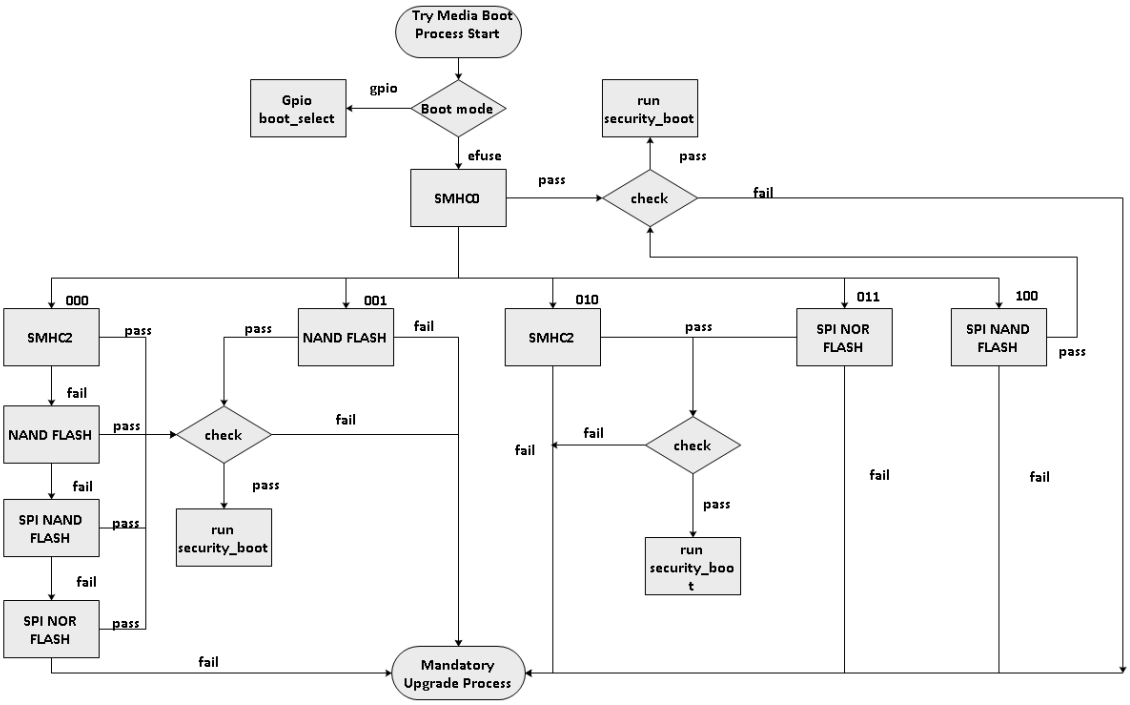

Figure 3- 16. Secure BROM eFuse Boot Select Process

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3.5. System Configuration

3.5.1. Overview

The system configuration module is used to configure parameter for system domain, such as SRAM, CPU, PLL,BROM, and so on.

The address range of SRAM is as follows.

Area	Address	Size(Bytes)
SRAM A1	0x0002 0000---0x0002 7FFF	32K
SRAM A2	0x0010 0000---0x0010 3FFF	16K
	0x0010 4000---0x0011 FFFF	112K
SRAM C	0x0002 8000---0x0004 FFFF	160K

3.5.2. Register List

Module Name	Base Address
SYS_CFG	0x03000000

Register Name	Offset	Description
VER_REG	0x0024	Version Register
EMAC_EPHY_CLKC_REG	0x0030	EMAC-EPHY Clock Register
BROM_OUTPUT_REG	0x00A4	BROM Output Register

3.5.3. Register Description

3.5.3.1. Version Register

Offset:0x0024			Register Name: VER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	Reserved
15:11	R/W	0x0	Reserved
10:9	R	UDF	BOOT_SEL_1_0_PAD_STA 00: SMHC0-> NAND FLASH 01: SMHC0-> SMHC2 10: SMHC0-> SPI NAND->SPI NOR 11: SMHC0->SMHC2->NAND FLASH->SPI NAND->SPI NOR
8	R	UDF	FEL_SEL_PAD_STA Fel Select Pin Status

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			0: Run_FEL 1:Try Media Boot
7:3	/	/	/
2:0	R	0x0	Reserved

3.5.3.2. EMAC-EPHY Clock Register (Default Value: 0x0005_8000)

Offset:0x0030			Register Name: EMAC_EPHY_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	BPS_EFUSE
27	R/W	0x0	XMII_SEL 0: Internal SMI and MII 1: External SMI and MII
26:25	R/W	0x0	EPHY_MODE Operation Mode Selection 00: Normal Mode 01: Sim Mode 10: AFE Test Mode 11:/
24:20	R/W	0x0	PHY_ADDR PHY Address
19	R/W	0x0	BIST_CLK_EN 0: BIST clk disable 1: BIST clk enable
18	R/W	0x1	CLK_SEL 0:25MHz 1:OSC24M
17	R/W	0x0	LED_POL 0:High active 1:Low active
16	R/W	0x1	SHUTDOWN 0:Power up 1:Shut down
15	R/W	0x1	PHY_SELECT 0:External PHY 1:Internal PHY
14	/	/	/
13	R/W	0x0	RMII_EN 0:Disable RMII module 1:Enable RMII module When the bit assert, MII or RMII interface is disabled.(It means bit13 is prior to bit12)
12:10	R/W	0x0	ETXDC

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			Configure EMAC Transmit Clock Delay Chain
9:5	R/W	0x0	ERXDC Configure EMAC Receive Clock Delay Chain
4	R/W	0x0	ERXIE Enable EMAC Receive Clock Invertor 0:Disable 1:Enable
3	R/W	0x0	ETXIE Enable EMAC Transmit Clock Invertor 0:Disable 1:Enable
2	R/W	0x0	EPIT EMAC PHY Interface Type 0:MII 1:RGMII
1:0	R/W	0x0	ETCS EMAC Transmit Clock Source 00:Transmit clock source for MII 01:External transmit clock source for GMII and RGMII 10:Internal transmit clock source for GMII and RGMII 11:Reserved

3.5.3.3. BROM Output Register (Default Value: 0x0000_0000)

Offset:0x00A4			**Register Name: BROM_OUTPUT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	BROM_OUTPUT_VALUE 0: U-Boot pin output 0 1: U-Boot pin output 1
0	R/W	0x0	BROM_OUTPUT_ENALBE 0: Disable U-Boot pin output 1: Enable U-Boot pin output

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3.6. Timer

3.6.1. Overview

The timer module implements the timing and counting functions.The timer module includes timer0 and timer1,watchdog, AVS and 64-bit counter.

The timer0 and timer1 are completely consistent.The timer0/1 has the following features:

- Configurable count clock: LOSC and OSC24M. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transimit a reset signal to reset the entire system after an exception occurs in the system.The watchdog has the following features:

- Single clock source: OSC24M/750
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

The AVS is used to the synchronization of audio and video. The AVS module includes AVS0 and AVS1, the AVS0 and AVS1 are completely consistent.The AVS has the following features:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Initial value can be updated anytime
- 12-bit frequency divider factor
- Pause/Start function

The 64-bit counter is used to count timing for GPU.The 64-bit counter has the following features:

- 64-bit counter
- Supports clear zero function
- Performs latch operation once before getting the current counter value

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3.6.2. Block Diagram

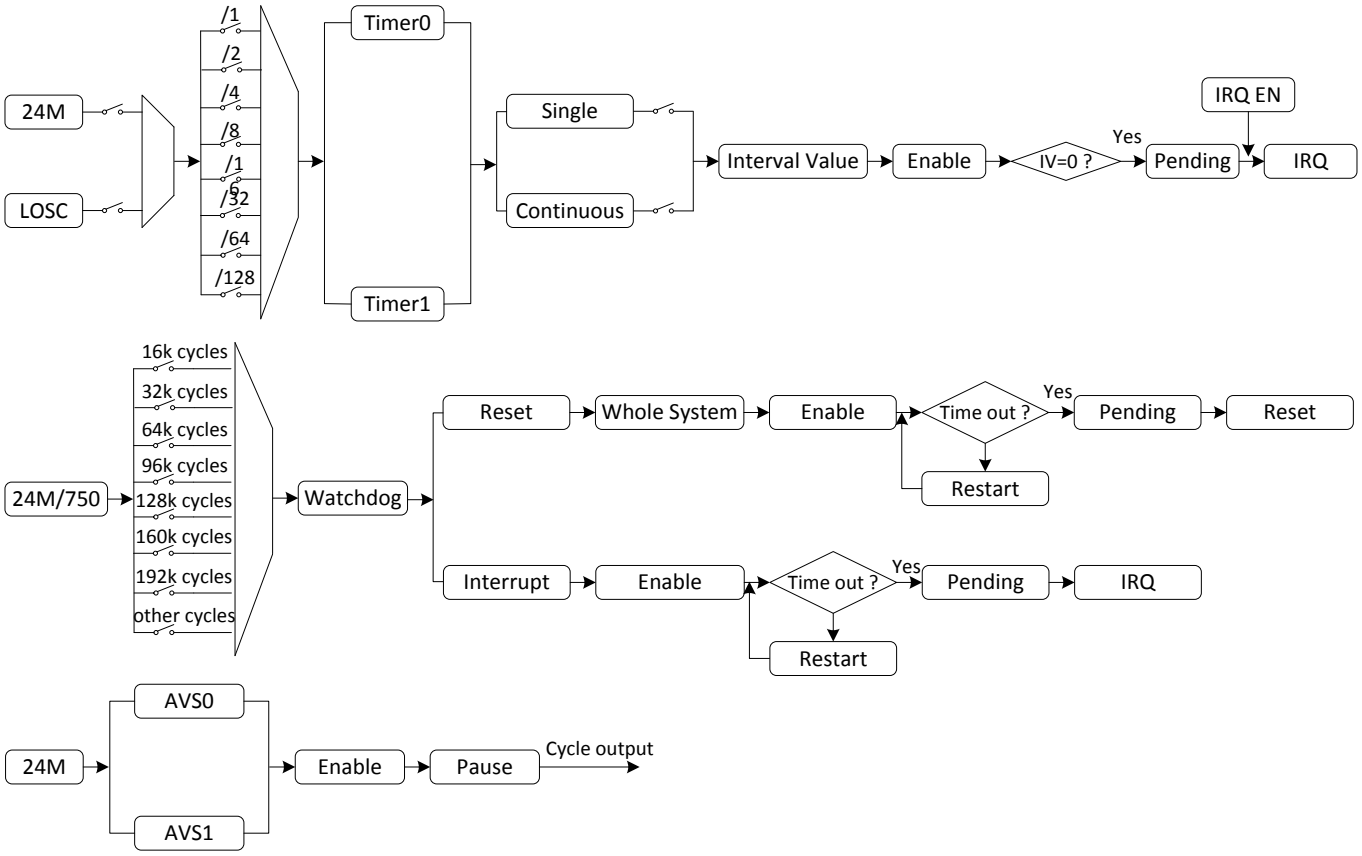

Figure 3- 17. Timer Block Diagram

3.6.3. Operations and Functional Descriptions

3.6.3.1. Timer Formula

$$T_{timer0} = \frac{TMR0\_INTV\_VALUE\_REG - TMR0\_CUR\_VALUE\_REG}{TMR0\_CLK\_SRC} \times TMR0\_CLK\_PRES$$

TMR0_INTV_VALUE_REG: timer initial value;
TMR0_CUR_VALUE_REG: timer current counter;
TMR0_CLK_SRC: timer clock source;
TMR0_CLK_PRES: timer clock prescale ratio.

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3.6.3.2. Typical Application

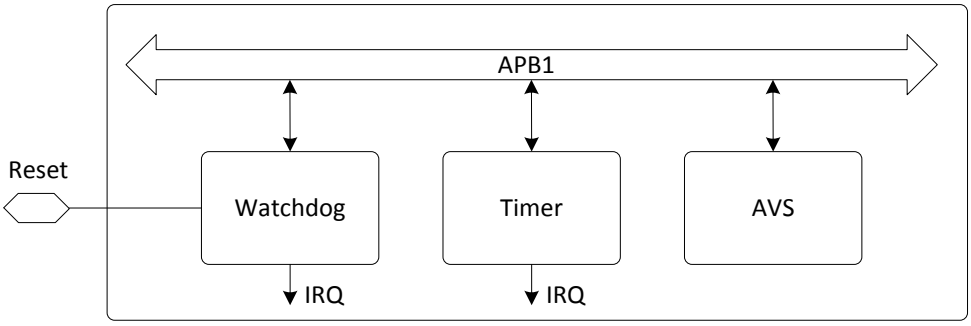

Figure 3- 18. Timer Application Diagram

3.6.3.3. Function Implemention

3.6.3.3.1. Timer

The timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each timer has independent interrupt.

The timer has two operating modes.

- **Continuous mode**

The bit7 of the TMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the timer module reloads data from TMRn_INTV_VALUE_REG then continues to count.

- **Single mode**

The bit7 of the TMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the timer stops counting. The timer starts to count again only when a new initial value is loaded.

Each timer has a prescaler that divides the working clock frequency of each timer by 1,2,4,8,16,32,64,128.

3.6.3.3.2. Watchdog

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The watchdog has two operating modes.

- **Interrupt mode**

The WDOG0_CFG_REG is set to 0x10, when the counter value reaches 0 and WDOG0_IRQ_EN_REG is enabled, the watchdog generates an interrupt.

- **Reset mode**

The WDOG0_CFG_REG is set to 0x01, when the counter value reaches 0, the watchdog generates a reset signal to reset

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the entire system.

The clock source of the watchdog is OSC24M/750.There are 12 configurable initial count values.
The watchdog can restart to count by setting the WDOG0_CTRL_REG: write 0xA57 to bit[12:1],then write 1 to bit[0].

3.6.3.3.3. AVS

The AVS is a 33-bit up counter.The counter value is increased by 1 on each rising edge of the count clock.
The AVS can be operated after its clock gating in CCU module is opened.
The AVS has an OSC24M clock source and a 12-bit division factor N. When the timer increases to N from 0, AVS counter adds 1; when the counter reaches 33-bit upper limit,the AVS will start to count from initial value again.
In counter working process, the division factor and initial counter of the AVS can be changed anytime.And the AVS can stop or start to operate counter anytime.

3.6.3.4. Operating Mode

3.6.3.4.1. Timer Initial

(1) Configure the timer parameters: clock source, prescale factor, working mode. The configuration of these parameters have no sequence,and can be implemented by writing **TMRn_CTRL_REG**.
(2) Write the initial value: write **TMRn_INTV_VALUE_REG** to provide an initial value for the timer; write the bit[1] of **TMRn_CTRL_REG** to load the initial value to the timer, the bit[1] can not be written again before it is cleared automatically.
(3) Enable timer: write the bit[0] of **TMRn_CTRL_REG** to enable timer count; read **TMRn_CUR_VALUE_REG** to get the current count value.

3.6.3.4.2. Timer Interrupt

(1) Enable interrupt: write corresponding interrupt enable bit of **TMR_IRQ_EN_REG**, when timer counter time reaches, the corresponding interrupt generates.
(2) After enter interrupt process, write **TMR_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.3. Watchdog Initial

(1) Write **WDOG0_CFG_REG** to configure the generation of the interrupts and the output of reset signal.
(2) Write **WDOG0_MODE_REG** to configure the initial count value.
(3) Write **WDOG0_MODE_REG** to enable the watchdog.

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3.6.3.4.4. Watchdog Interrupt

Watchdog interrupt is only used for the counter.

(1) Write **WDOG0_IRQ_EN_REG** to enable the interrupt.

(2) After enter the interrupt process, write **WDOG0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.5. AVS Start/Pause

(1) Write **AVS_CNT_DIV_REG** to configure the division factor.

(2) Write **AVS_CNT_REG** to configure the initial count value.

(3) Write **AVS_CNT_CTL_REG** to enable AVS counter. AVS counter can be paused at any time.

3.6.4. Programming Guidelines

3.6.4.1. Timer

Take making a 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR_0_INTV);                      //Set interval value
writel(0x94, TMR_0_CTRL);                       //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);   //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);                //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);   //Enable Timer0
```

If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0.

If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1.

In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.4.2. Watchdog Reset

In the following instance making configurations for Watchdog: configurate clock source as 24M/750, configurate Interval Value as 1s and configurate Watchdog Configuration as To whole system. This instance indicates that reset system after 1s.

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```
writel(0x1, WDOG_CONFIG);                          //To whole system
writel(0x10, WDOG_MODE);                           //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);        //Enable Watchdog
```

3.6.4.3. Watchdog Restart

In the following instance making configurations for Watchdog: configurate clock source as 24M/750, configurate Interval Value as 1s and configurate Watchdog Configuration as To whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(0x1, WDOG_CONFIG);                          //To whole system
writel(0x10, WDOG_MODE);                           //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);        //Enable Watchdog
----other codes---
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0)，WDOG_CTRL); //Writel 0xA57 at Key Field and Restart Watchdog
```

3.6.5. Register List

Module Name	Base Address
Timer	0x03009000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register
WDOG_MODE_REG	0x00B8	Watchdog Mode Register
AVS_CNT_CTL_REG	0x00C0	AVS Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Divisor Register
CNT64_CTRL_REG	0x0100	64-bit Counter Control Register

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CNT64_LOW_REG	0x0104	64-bit Counter Low Register
CNT64_HIGH_REG	0x0108	64-bit Counter High Register

3.6.6. Register Description

3.6.6.1. Timer IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	TMR1_IRQ_EN Timer 1 Interrupt Enable 0: No effect 1: Timer 1 Interval Value reached interrupt enable
0	R/W1S	0x0	TMR0_IRQ_EN Timer 0 Interrupt Enable 0: No effect 1: Timer 0 Interval Value reached interrupt enable

3.6.6.2. Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	TMR1_IRQ_PEND Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
0	R/W1C	0x0	TMR0_IRQ_PEND Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached

3.6.6.3. Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR0_MODE Timer 0 mode 0: Continuous mode. When interval value reached, the timer will not disable

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			automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD Timer 0 Reload 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR0_EN Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.4. Timer 0 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: TMR0_INTV_VALUE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_INTV_VALUE Timer 0 Interval Value

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NOTE

The value setting should consider the system clock and the timer clock source.

3.6.6.5. Timer 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE Timer 0 Current Value Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.6. Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE Timer 1 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES Select the pre-scale of timer 1 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD Timer 1 Reload 0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it is cleared automatically.

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0	R/W	0x0	TMR1_EN Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.7. Timer 1 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE Timer 1 Interval Value

NOTE

The value should consider the system clock and the timer clock source.

3.6.6.8. Timer 1 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_CUR_VALUE Timer 1 Current Value Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.9. Watchdog IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name:WDOG_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1S	0x0	WDOG_IRQ_EN Watchdog Interrupt Enable 0: No effect 1: Watchdog interrupt enable

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3.6.6.10. Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name:WDOG_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ _PEND Watchdog IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending. Watchdog interval value is reached.

3.6.6.11. Watchdog Control Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name:WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD Watchdog Key Field It should be written to 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART Watchdog Restart 0: No effect 1: Restart the Watchdog

3.6.6.12. Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name:WDOG_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	WDOG_CONFIG 00: To CPUS 01: To whole system 10: Only interrupt 11: To CPU0

3.6.6.13. Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name:WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE

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			Watchdog Interval Value Watchdog clock source is OSC24M / 750. If the clock source is turned off, Watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) Others:Reserved
3:1	/	/	/
0	R/W1S	0x0	WDOG_EN Watchdog Enable 0: No effect 1: Enable the Watchdog

3.6.6.14. AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/Disable The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 0 Enable/Disable The counter source is OSC24M.

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			0: Disable 1: Enable

3.6.6.15. AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter will not increase.

3.6.6.16. AVS Counter 1 Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name:AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter will not increase.

3.6.6.17. AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset: 0x00CC			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit

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			counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.

3.6.6.18. 64-bit Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			**Register Name: CNT64_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	CNT64_CLK_SRC_SEL 64-bit Counter Clock Source Select 0: OSC24M 1: /
1	R/W	0x0	CNT64_RL_EN 64-bit Counter Read Latch Enable 0: No effect 1: To latch the 64-bit Counter to the Low/Hi registers.It will change to zero after the registers are latched.
0	R/W	0x0	CNT64_CLR_EN 64-bit Counter Clear Enable 0: No effect 1: To clear the 64-bit Counter Low/Hi registers. It will change to zero after the registers are cleared. It is not recommended to clear this counter arbitrarily.

NOTE

This 64-bit up-counter will start to count as soon as the system power on finished.

3.6.6.19. 64-bit Counter Low Register (Default Value: 0x0000_0000)

Offset: 0x0104	**Register Name: CNT64_LOW_REG**

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Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	CNT64_LO 64-bit Counter [31:0]

3.6.6.20. 64-bit Counter High Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: CNT64_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CNT64_HI 64-bit Counter [63:32]

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3.7. High Speed Timer

3.7.1. Overview

The high speed timer(HSTimer) module implements the timing and counting functions.

The HSTimer has the following features:

- Timing clock is AHB1 that can provides more accurate timing clock
- Configurable 5 prescale factor
- Configurable 56-bit down timer
- Supports 2 working modes: continuous mode and single mode
- Supports test mode
- Generates an interrupt when the count is decreased to 0

3.7.2. Block Diagram

Figure 3-19 shows a block diagram of the HSTimer.

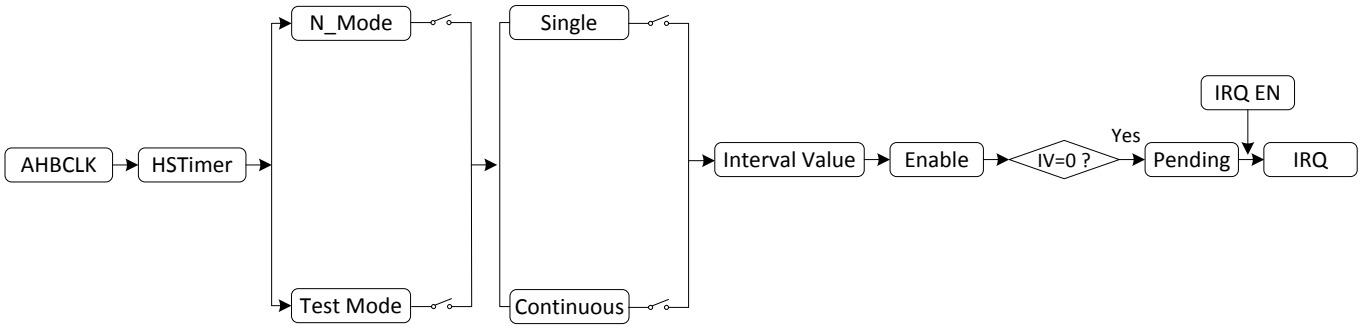

Figure 3- 19. HSTimer Block Diagram

3.7.3. Operations and Functional Description

3.7.3.1. HSTimer Formula

$$\frac{(HS\_TMR\_INTV\_HI\_REG<<32 + HS\_TMR\_INTV\_LO\_REG) - (HS\_TMR\_CURNT\_HI\_REG<<32 + HS\_TMR\_CURNT\_LO\_REG)}{AHB1CLK} \times HS\_TMR\_CLK$$

HS_TMR_INTV_HI_REG: Initial of Counter Higher Bit
HS_TMR_INTV_LO_REG: Initial of Counter Lower Bit
HS_TMR_CURNT_HI_REG: Current Value of Counter Higher Bit
HS_TMR_CURNT_LO_REG: Current Vaule of Counter Lower Bit

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AHB1CLK: AHB1 Clock Frequency
HS_TMR_CLK: Time Prescale Ratio of Counter

3.7.3.2. Typical Application

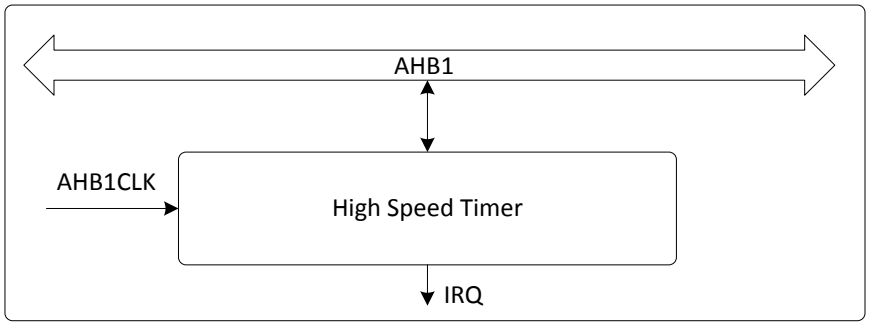

Figure 3- 20. HSTimer Application Diagram

The high speed timer is on AHB1, and the high speed timer controls registers by AHB1.
The high speed timer has single clock source: AHB. The high speed timer can generate interrupt.

3.7.3.3. Function Implemention

The high speed timer is a 56-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The high speed timer has two timing modes.

- Continuous mode : The bit7 of **HS_TMR0_CTRL_REG** is set to the continuous mode, when the count value is decreased to 0, the high speed timer module reloads data from **HS_TMR_INTV_LO_REG** and **HS_TMR_INTV_HI_REG** then continues to count.
- Single mode : The bit7 of **HS_TMR0_CTRL_REG** is set to the single mode, when the count value is decreased to 0, the high speed timer stops counting. The high speed timer starts to count again only when a new initial value is loaded.

The high speed timer has two operating modes.

- Normal mode: When the bit31 of **HS_TMR0_CTRL_REG** is set to the normal mode, the high speed timer is used as 56-bit down counter, which can continuous timing and single timing.
- Test mode: When the bit31 of **HS_TMR0_CTRL_REG** is set to the normal mode, then **HS_TMR_INTV_LO_REG** must be set to 0x1, the high speed timer is used as 24-bit down counter, and **HS_TMR_INTV_HI_REG** is the initial value of the high speed timer.

Each high speed timer has a prescaler that divides the working clock frequency of each working timer by 1,2,4,8,16.

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3.7.3.4. Operating Mode

3.7.3.4.1. Clock Gating and Reset

By default the HSTimer clock gating is mask. When it is necessary to use HSTimer, HSTimer clock gating should be opened in **HSTIMER Bus Gating Reset Register** and then de-asserted the software reset in **HSTIMER Bus Gating Reset Register** through CCU module.If it is no need to use HSTimer, both the gating bit and software reset bit should be set 0.

3.7.3.4.2. HSTimer Initial

(1) AHB1 clock management: Open the clock gating of AHB1 and de-assert the soft reset of AHB1 in CCU.
(2) Configure the corresponding parameters of the high speed timer: clock source, prescaler factor, working mode, counting mode. These parameters that are written to **HS_TMR0_CTRL_REG** have no sequences.
(3) Write the initial value: Firstly write the low-bit register **HS_TMR_INTV_LO_REG**, then write the high-bit register **HS_TMR_INTV_HI_REG**. Write the bit1 of **HS_TMR0_CTRL_REG** to load the initial value. If in timing stop stage of high speed timer, write the bit1 and bit0 of **HS_TMR0_CTRL_REG** to reload the initial value.
(4) Enable high speed timer: Write the bit[0] of **HS_TMR0_CTRL_REG** to enable high speed timer to count.

3.7.3.4.3. HSTimer Interrupt

(1) Enable interrupt: Write the corresponding interrupt enable bit of **HS_TMR_IRQ_EN_REG**, when the counting time of high speed timer reaches , the corresponding interrupt generates.
(2) After enter the interrupt process, write **HS_TMR_IRQ_STAS_REG** to clear the interrupt pending.
(3) Resume the interrupt and continue to execute the interrupted process.

3.7.3.4.4. HSTimer Reload

Differing from the reload of Timer, when interval value is reloaded into current value register, the reload bit would not turn to 0 automatically until you clear it. If software hopes the current value register to down-count from the new interval value in pause status, the reload bit and the enable bit should be written 1 at the same time.

3.7.4. Programming Guidelines

Take making a 1us delay using HSTimer0 for an instance as follow, AHB1CLK will be configurated as 100MHz and n_mode,single mode and 2 pre-scale will be selected in this instance.

```
writel(0x0, HS_TMR0_INTV_HI);          //Set interval value Hi 0x0
writel(0x32, HS_TMR0_INTV_LO);         //Set interval value Lo 0x32
writel(0x90, HS_TMR0_CTRL);            //Select n_mode,2 pre-scale,single mode
```

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```
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL);     //Set Reload bit
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL);     //Enable HSTimer0
while(!(readl(HS_TMR_IRQ_STAS)&1));                   //Wait for HSTimer0 to generate pending
writel(1,HS_TMR_IRQ_STAS);                            //Clear HSTimer0 pending
```

3.7.5. Register List

Module Name	Base Address
High Speed Timer	0x03005000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0040	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0044	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0048	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x004C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0050	HS Timer 1 Current Value High Register

3.7.6. Register Description

3.7.6.1. HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	HS_TMR1_INT_EN High Speed Timer 1 Interrupt Enable 0: No effect 1: High Speed Timer1 Interval Value reached interrupt enable
0	R/W1S	0x0	HS_TMR0_INT_EN High Speed Timer 0 Interrupt Enable 0: No effect 1: High Speed Timer0 Interval Value reached interrupt enable

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3.7.6.2. HS Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	HS_TMR1_IRQ_PEND High Speed Timer 1 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 1 interval value is reached.
0	R/W1C	0x0	HS_TMR0_IRQ_PEND High Speed Timer 0 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 0 interval value is reached.

3.7.6.3. HS Timer 0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST High Speed Timer 0 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE High Speed Timer 0 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

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1	R/W1S	0x0	HS_TMR0_RELOAD High Speed Timer 0 Reload 0: No effect 1: Reload High Speed Timer 0 Interval Value
0	R/W	0x0	HS_TMR0_EN High Speed Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.4. HS Timer 0 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HS_TMR0_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO High Speed Timer 0 Interval Value [31:0]

3.7.6.5. HS Timer 0 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: HS_TMR0_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI High Speed Timer 0 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.7.6.6. HS Timer 0 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO

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			High Speed Timer 0 Current Value [31:0]

3.7.6.7. HS Timer 0 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI High Speed Timer 0 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

3.7.6.8. HS Timer 1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR1_TEST High Speed Timer 1 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR1_MODE High Speed Timer 1 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

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1	R/W1S	0x0	HS_TMR1_RELOAD High Speed Timer 1 Reload 0: No effect 1: Reload High Speed Timer 1 Interval Value
0	R/W	0x0	HS_TMR1_EN High Speed Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.9. HS Timer 1 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO High Speed Timer 1 Interval Value [31:0]

3.7.6.10. HS Timer 1 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: HS_TMR1_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI High Speed Timer 1 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.7.6.11. HS Timer 1 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO

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			High Speed Timer 1 Current Value [31:0]

3.7.6.12. HS Timer 1 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI High Speed Timer 1 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

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3.8. GIC

3.8.1. Interrupt Source

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	GPADC	0x0080	GPADC interrupt
33	/	/	/
34	/	/	/
34	/	/	/

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
36	/	/	/
37	OWA	0x0094	OWA interrupt
38	/	/	/
39	DMIC	0x009C	DMIC interrupt
40	/	/	/
41	DRAM	0x00A4	DRAM interrupt
42	DMA	0x00A8	DMA interrupt
43	MBOX	0x00AC	Message BOX interrupt
44	SPINLOCK	0x00B0	Spinlock interrupt
45	/	0x00B4	/
46	WDOG	0x00B8	Watchdog interrupt
47	PWM	0x00BC	PWM interrupt
48	CLK_DET	0x00C0	Clock Detect interrupt
49	BUS_TIMEOUT	0x00C4	Bus Timeout interrupt
50	/	/	/
51	PSI	0x00CC	PSI interrupt
52	/	/	/
53	G2D	0x00D4	G2D interrupt
54	EVE	0x00D8	EVE interrupt
55	/	/	/
56	/	/	/
57	VE	0x00E4	VE interrupt
58	/	/	/
59	EMAC	0x00EC	EMAC interrupt
60	TS	0x00F0	TS interrupt
61	/	/	/
62	Audio Codec	0x00F8	Audio Codec interrupt
63	NAND	0x00FC	NAND interrupt
64	TVE	0x0100	TVE interrupt
65	DE	0x0104	DE interrupt
66	/	/	/
67	DI	0x010C	De-interlace interrupt
68	ISP0	0x0110	ISP0 interrupt
69	ISP1	0x0114	ISP1 interrupt
70	CE_NS	0x0118	CE_NS interrupt
71	CE_S	0x011C	CE_S interrupt
72	/	0x0120	/
73	I2S/PCM0	0x0124	I2S/PCM0 interrupt
74	I2S/PCM1	0x0128	I2S/PCM1 interrupt
75	I2S/PCM2	0x012C	I2S/PCM2 interrupt
76	SCR	0x0130	SCR interrupt
77	/	0x0134	/

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
78	TWI0	0x0138	TWI0 interrupt
79	TWI1	0x013C	TWI1 interrupt
80	TWI2	0x0140	TWI2 interrupt
81	TWI3	0x0144	TWI3 interrupt
82	TWI4	0x0148	TWI4 interrupt
83	MIPI_DSI	0x014C	MIPI_DSI interrupt
84	SMHC0	0x0150	SMHC0 interrupt
85	SMHC1	0x0154	SMHC1 interrupt
86	SMHC2	0x0158	SMHC2 interrupt
87	SMHC3	0x015C	SMHC3 interrupt
88	TVD0	0x0160	TVD0 interrupt
89	TVD1	0x0164	TVD1 interrupt
90	TVD2	0x0168	TVD2 interrupt
91	TVD3	0x016C	TVD3 interrupt
92	UART0	0x0170	UART0 interrupt
93	UART1	0x0174	UART1 interrupt
94	UART2	0x0178	UART2 interrupt
95	UART3	0x017C	UART3 interrupt
96	UART4	0x0180	UART4 interrupt
97	SPI0	0x0184	SPI0 interrupt
98	SPI1	0x0188	SPI1 interrupt
99	HSTIMER0	0x018C	HSTIMER0 interrupt
100	HSTIMER1	0x0190	HSTIMER1 interrupt
101	TIMER0	0x0194	TIMER0 interrupt
102	TIMER1	0x0198	TIMER1 interrupt
103	TCON_LCD0	0x019C	TCON_LCD0 interrupt
104	TCON_LCD1	0x01A0	TCON_LCD1 interrupt
105	TCON_TV	0x01A4	TCON_TV interrupt
107	USB2.0_OTG_DEVICE	0x01AC	USB2.0_OTG_DEVICE interrupt
108	USB2.0_OTG_EHCI	0x01B0	USB2.0_OTG_EHCI interrupt
109	USB2.0_OTG_OHCI	0x01B4	USB2.0_OTG_OHCI interrupt
110	USB2.0_HOST1_EHCI	0x01B8	USB2.0_HOST1_EHCI interrupt
111	USB2.0_HOST1_OHCI	0x01BC	USB2.0_HOST1_OHCI interrupt
112	USB2.0_HOST2_EHCI	0x01C0	USB2.0_HOST2_EHCI interrupt
113	USB2.0_HOST2_OHCI	0x01C4	USB2.0_HOST2_OHCI interrupt
114	USB2.0_HOST3_EHCI	0x01C8	USB2.0_HOST3_EHCI interrupt
115	USB2.0_HOST3_OHCI	0x01CC	USB2.0_HOST3_OHCI interrupt
116	GPIOB	0x01D0	GPIOB interrupt
117	GPIOF	0x01D4	GPIOF interrupt
118	GPIOG	0x01D8	GPIOG interrupt
119	GPIOH	0x01DC	GPIOH interrupt
120	GPIOJ	0x01E0	GPIOJ interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
121	GPU-GP	0x01E4	GPU-GP interrupt
122	GPU-GPMMU	0x01E8	GPU-GPMMU interrupt
123	GPU-PP0	0x01EC	GPU-PP0 interrupt
124	GPU-PPMMU0	0x01F0	GPU-PPMMU0 interrupt
125	GPU-PMU	0x01F4	GPU-PMU interrupt
126	GPU-PP1	0x01F8	GPU-PP1 interrupt
127	GPU-PPMMU1	0x01FC	GPU-PPMMU1 interrupt
128	GPU-PP2	0x0200	GPU-PP2 interrupt
129	GPU-PPMMU2	0x0204	GPU-PPMMU2 interrupt
130	GPU-PP3	0x0208	GPU-PP3 interrupt
131	GPU-PPMMU3	0x020C	GPU-PPMMU3 interrupt
132	CSI_DMA0	0x0210	CSI0_DMA0 interrupt
133	CSI_DMA1	0x0214	CSI0_DMA1 interrupt
134	CSI_DMA2	0x0218	CSI0_DMA2 interrupt
135	CSI_DMA3	0x021C	CSI0_DMA3 interrupt
136	CSI_PARSER0	0x0220	CSI0_PARSER0 interrupt
137	CSI_PARSER1	0x0224	CSI0_PARSER1 interrupt
138	CSI_CCI0	0x0228	CSI0_CCI0 interrupt
139	CSI_CCI1	0x022C	CSI0_CCI1 interrupt
140	CSI_MIPI0_RX	0x0230	CSI0_MIPI0_RX interrupt
141	CSI_MIPI1_RX	0x0234	CSI0_MIPI1_RX interrupt
142	CSI_DMA4	0x0238	CSI1_DMA0 interrupt
143	CSI_DMA5	0x023C	CSI1_DMA1 interrupt
144	CSI_DMA6	0x0240	CSI1_DMA2 interrupt
145	CSI_DMA7	0x0244	CSI1_DMA3 interrupt
146	CSI_PARSER2	0x0248	CSI1_PARSER0 interrupt
147	CSI_PARSER3	0x024C	CSI1_PARSER1 interrupt
148	CSI_CCI2	0x0250	CSI1_CCI0 interrupt
149	CSI_CCI3	0x0254	CSI1_CCI1 interrupt
150	TWI5	0x0258	TWI5 interrupt
151	TWI6	0x025C	TWI6 interrupt
160	External NMI	0x0280	External NMI interrupt
161	R_TIMER0	0x0284	R_TIMER0 interrupt
162	R_TIMER1	0x0288	R_TIMER1 interrupt
163	R_TIMER2	0x028C	R_TIMER2 interrupt
164	R_TIMER3	0x0290	R_TIMER3 interrupt
165	R_Alarm0	0x0294	R_Alarm0 interrupt
166	R_Alarm1	0x0298	R_Alarm1 interrupt
167	R_WDOG	0x029C	R_WDOG interrupt
168	R_TWDOG	0x02A0	TWDOG interrupt
169	R_PWM	0x02A4	R_PWM interrupt
170	R_GPIOL	0x02A8	R_GPIOL interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
171	R_GPIOM	0x02AC	R_GPIOM interrupt
172	R_LRADC	0x02B0	R_LRADC interrupt
173	R_UART0	0x02B4	R_UART0 interrupt
174	R_UART1	0x02B8	R_UART1 interrupt
175	R_UART2	0x02BC	R_UART2 interrupt
176	R_UART3	0x02C0	R_UART3 interrupt
177	R_UART4	0x02C4	R_UART4 interrupt
178	R_TWI0	0x02C8	R_TWI0 interrupt
179	R_TWI1	0x02CC	R_TWI1 interrupt
180	R_TWI2	0x02D0	R_TWI2 interrupt
181	/	0x02D4	/
182	R_RSB	0x02D8	R_RSB interrupt
183	R_CIR_RX	0x02DC	R_CIR_RX interrupt
184	R_CPU_IDLE	0x02E0	R_CPU_IDLE interrupt
185	R_THS	0x02E4	R_THS interrupt
186	R_VM	0x02E8	Voltage monitor interrupt
187	R_SPI	0x02EC	R_SPI interrupt
188	/	/	/
190	/	/	/
191	/	/	/
192	C0_CTI0	0x0300	C0_CTI0 interrupt
193	C0_CTI1	0x0304	C0_CTI1 interrupt
194	C0_CTI2	0x0308	C0_CTI2 interrupt
195	/	/	/
196	C0_COMMTX0	0x0310	C0_COMMTX0 interrupt
197	C0_COMMTX1	0x0314	C0_COMMTX1 interrupt
198	C0_COMMTX2	0x0318	C0_COMMTX2 interrupt
199	/	/	/
200	C0_COMMRX0	0x0320	C0_COMMRX0 interrupt
201	C0_COMMRX1	0x0324	C0_COMMRX1 interrupt
202	C0_COMMRX2	0x0328	C0_COMMRX2 interrupt
203	/	/	/
204	C0_PMU0	0x0330	C0_PMU0 interrupt
205	C0_PMU1	0x0334	C0_PMU1 interrupt
206	C0_PMU2	0x0338	C0_PMU2 interrupt
207	/	/	/
208	C0_AXI_ERROR	0x0340	C0_AXI_ERROR interrupt
209	/	/	/
210	C0_AXI_WR	0x0348	C0_AXI_WR interrupt
211	C0_AXI_RD	0x034C	C0_AXI_RD interrupt
212	C1_CTI0	0x0350	C1_CTI0 interrupt
213	C1_CTI1	0x0354	C1_CTI1 interrupt

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Interrupt Number	Interrupt Source	Interrupt Vector	Description
214	C1_CTI2	0x0358	C1_CTI2 interrupt
215	/	/	/
216	C1_COMMTX0	0x0360	C1_COMMTX0 interrupt
217	C1_COMMTX1	0x0364	C1_COMMTX1 interrupt
218	C1_COMMTX2	0x0368	C1_COMMTX2 interrupt
219	/	/	/
220	C1_COMMRX0	0x0370	C1_COMMRX0 interrupt
221	C1_COMMRX1	0x0374	C1_COMMRX1 interrupt
222	C1_COMMRX2	0x0378	C1_COMMRX2 interrupt
223	/	/	/
224	C1_PMU0	0x0380	C1_PMU0 interrupt
225	C1_PMU1	0x0384	C1_PMU1 interrupt
226	C1_PMU2	0x0388	C1_PMU2 interrupt
227	/	/	/
228	C1_AXI_ERROR	0x0390	C1_AXI_ERROR interrupt
229	/	/	/
230	C1_AXI_WR	0x0398	C1_AXI_WR interrupt
231	C1_AXI_RD	0x039C	C1_AXI_RD interrupt
232	CCI400_0	0x03A0	CCI400_0 interrupt
233	CCI400_1	0x03A4	CCI400_1 interrupt

For complete GIC information, refer to the ***IHI0048B_b_gic_architecture_specification***.

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3.9. DMA

3.9.1. Overview

The direction memory access (DMA) is used to transfer data between a peripheral and a memory, between peripherals, or between memories. DMA is a high-speed data transfer operation that reduces the CPU resources.

The DMA has the following features:

- 12 channels DMA
- Provides 32 peripheral DMA requests for data read and 32 peripheral DMA requests for data write
- Transfer with linked list
- Programmable 8-,16-,32-,64-bit data width
- Programmable DMA burst length
- DRQ response includes wait mode and handshake mode
- Memory devices support non-aligned transform
- DMA channel supports pause function

3.9.2. Block Diagram

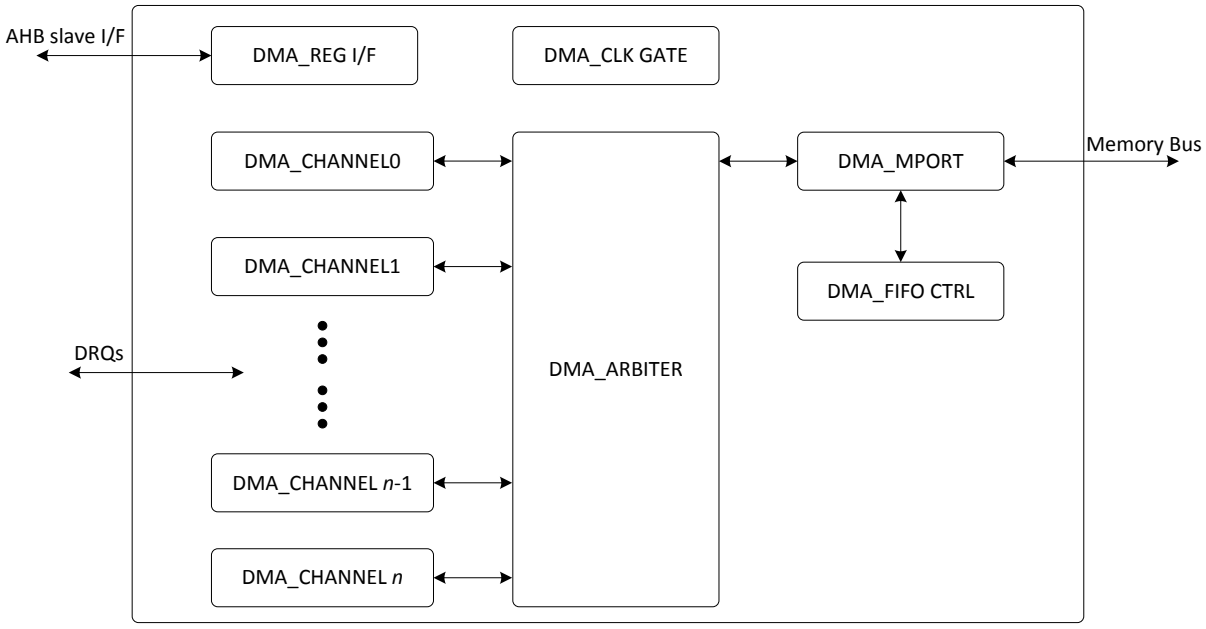

Figure 3- 21. DMA Block Diagram

DMA_ARBITER: Arbitrate DMA read/write requirement of each channel, and convert to read/write requirement of each port.

DMA_CHANNEL: DMA transform engine.Each channel is independent. The priorities of DMA channels uses polling mechanism. When the DMA requests from two peripherals are valid simultaneously, if DMA_ARBITER is non-idle ,the next channel of the current channel has the higher priority; if DMA_ARBITER is idle, the channel0 has the highest

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priority, whereas the channel11 has the lowest priority.
DMA_MPORT: Receive read/write requirement of DMA_ARBITER ,and convert to the corresponding MBUS access.
DMA_FIFOCTL: Internal FIFO cell control module.
DMA_REGIF: Common register module, mainly used to resolve AHB1 demand.
DMA_CLKGATE: Hardware auto clock gating control module.

DMA integrates 12 independent DMA channels. When DMA channel starts, DMA gets DMA descriptor by DMA_DESC_ADDR_REG to use for the configuration information of the current DMA package transfer ,and DMA can transfer data between the specified peripherals through the configuration information. When a package transfer finished, DMA judges if the current channel transfer finished through the linked information in descriptor.

3.9.3. Operations and Functional Description

3.9.3.1. Clock and Reset

DMA is on AHB1.The clock of AHB1 influences the transfer efficiency of DMA.

3.9.3.2. Typical Application

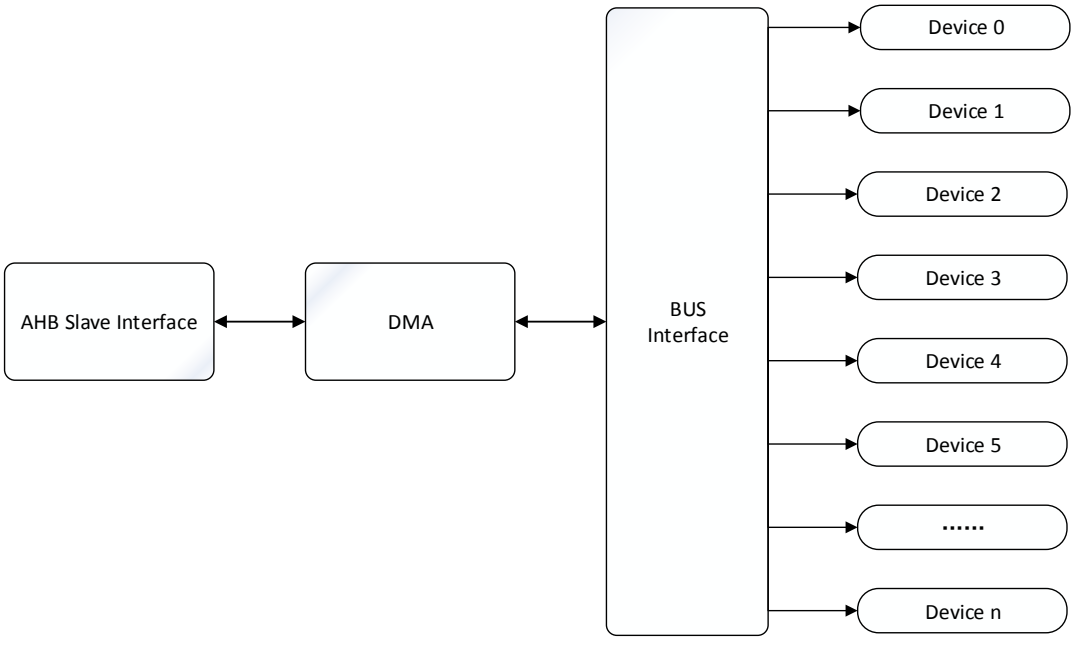

Figure 3- 22. DMA Typical Application Diagram

3.9.3.3. DRQ Type

Table 3- 8. DMA DRQ Table

Source DRQ Type	Destination DRQ Type

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port0	SRAM	port0	SRAM
port1	DRAM	port1	DRAM
port2	OWA-RX	port2	OWA-TX
port3	I2S/PCM0-RX	port3	I2S/PCM0-TX
port4	I2S/PCM1-RX	port4	I2S/PCM1-TX
port5	I2S/PCM2-RX	port5	I2S/PCM2-TX
port6	Audio Codec	port6	Audio Codec
port7	DMIC	port7	
port8		port8	
port9		port9	
port10	NAND	port10	NAND
port11		port11	
port12	GPADC	port12	
port13		port13	
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX
port18	UART4-RX	port18	UART4-TX
port19		port19	
port20		port20	
port21		port21	
port22	SPI0-RX	port22	SPI0-TX
port23	SPI1-RX	port23	SPI1-TX
port24		port24	
port25		port25	
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	USB2.0_OTG_EP1	Port30	USB2.0_OTG_EP1
Port31	USB2.0_OTG_EP2	Port31	USB2.0_OTG_EP2
Port32	USB2.0_OTG_EP3	Port32	USB2.0_OTG_EP3
Port33	USB2.0_OTG_EP4	Port33	USB2.0_OTG_EP4
Port34	USB2.0_OTG_EP5	Port34	USB2.0_OTG_EP5

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3.9.3.4. DMA Descriptor

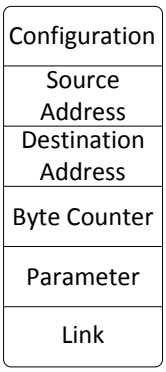

Figure 3- 23. DMA Descriptor

DMA descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words, in turn, configuration, source address, destination address, byte counter, parameter, link.

Configuration : Configure the following information by DMA_CFG_REG.

- DRQ type of source and destination.
- Transferred address count mode : IO mode indicates the address is fixed during transfer; linear mode indicates the address is increasing during transfer.
- Transferred block length : block length is the amount of DMA transferred data in one-shot valid DRQ. The block length supports 1-bit,4-bit,8-bit or 16-bit mode.
- Transferred data width: data width indicates the data width of every operation, and supports 8-bit,16-bit,32-bit or 64-bit mode.

Source Address: Configure the transferred source address.

Destination Address: Configure the transferred destination address.

DMA reads data from the source address , then writes data to the destination address.

Byte counter: Configure the amount of a package. The maximum package is not more than (2^25-1) bytes. If the amount of the package reaches the maximum value, even if DRQ is valid, DMA should stop the current transfer.

Parameter: Configure the interval between data block. The parameter is valid for non-memory peripherals. When DMA detects that DRQ is high level, DMA transfers block cycle. And during time, the changing of DRQ is ignored.After transferred, DMA waits the setting cycle(WAIT_CYC), then executes the next DRQ detection.

If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. DMA will stop transfer after the package is transferred; if the value of the link is not 0xFFFFF800, the value of the link is considered the descriptor address of the next package.

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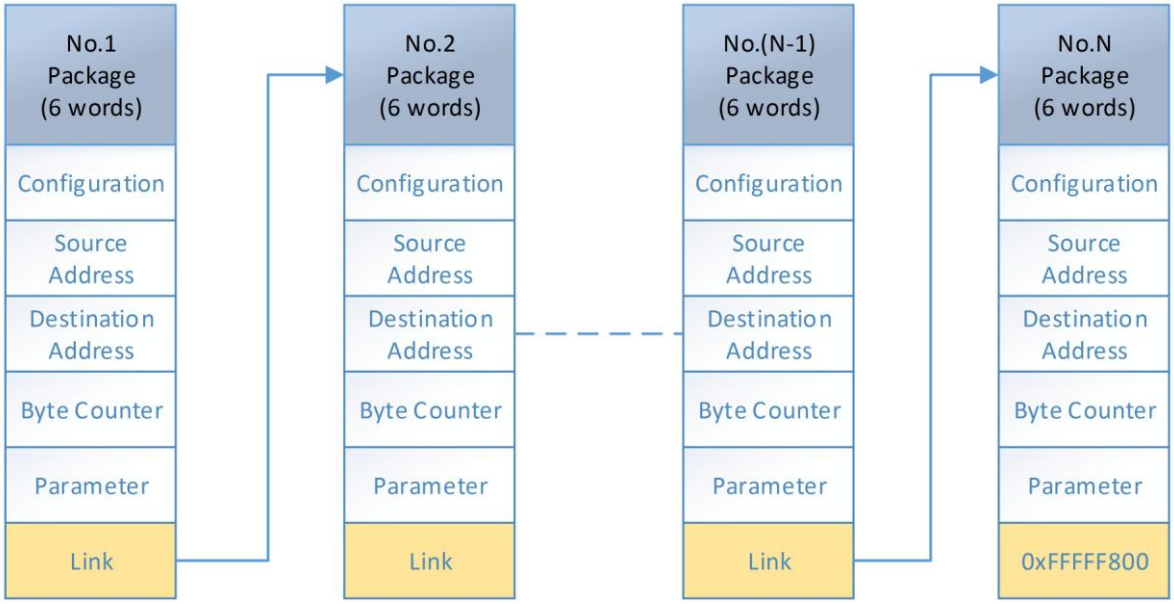

Figure 3- 24. DMA Chain Transfer

3.9.3.5. Interrupt

The half package interrupt is enabled, DMA sends half package interrupt after the half package transfer completes. The total package interrupt is enabled, DMA sends package end interrupt after the total package transfer completes. The total queue interrupt is enabled, DMA sends queue end interrupt after the total queue completes. Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts generate very closely, the later interrupt may override the former one. So DMA has only a system interrupt source.

3.9.3.6. Clock Gating

DMA CLK GATE module is the clock module of auto-controlled by hardware. DMA CLK GATE module is mainly used to generate the clock of DMA sub-module and the local circuit in module, including clock gating of channel and clock gating of public part.

The clock gating of the channel indicates DMA clock can auto-open when the system accesses the current DMA channel register and DMA channel is enabled. When DMA transfer is completed, DMA channel clock can auto-close after 16 HCLK delay, meanwhile the clock of the corresponding channel control and FIFO control will be closed.

The clock gating of the common part indicates the clock of the common circuit can auto-close when all DMA channels are opened. The common circuit includes the common circuit of FIFO control module, MPORT module and memory bus clock.

DMA clock gating can support all the functions stated above or not by software.

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3.9.3.7. Transfer Mode

DMA supports two data transfer modes: wait mode and handshake mode.

(1) Wait Mode

When device request signal enters DMA, the device request signal is transformed into the internal DRQ signal through block and wait counter. The transformed principle is as follows.

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically.
- After the internal DRQ holds low automatically to the DMA cycle of wait counter times, DMA restarts to detect the external request, if the external request signal is valid, then the next transfer starts.

(2) Handshake Mode

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically; meanwhile within the last operation , DMA follows the operating demand to send DMA last signal simultaneously.
- The DMA last signal that is used as a part of DMA demand transmits at BUS, when the device receives the operating demand of DMA last at BUS, the device can judge DMA transfer block length finished, that is before transmit the request again ,DMA operation cannot appear, and a DMA active signal is generated to the DMA controller. Notice that each DRQ signal of device corresponds to an active signal, if the device has many DRQ signals, then DMA returns different active signal through different bus operation.
- When DMA receives the transmitted active signal of devices, DMA ACK signal is returned to devices.
- After the device receives DMA ACK signal, if all operations of devices are completed , FIFO status and DRQ status are refreshed, then active signal is set as invalid.
- When DMA detects the falling edge of active signal, then the corresponding ACK signal is set as invalid, and DMA restarts to detect the external request signal. If the request signal is valid, then the next transfer starts.

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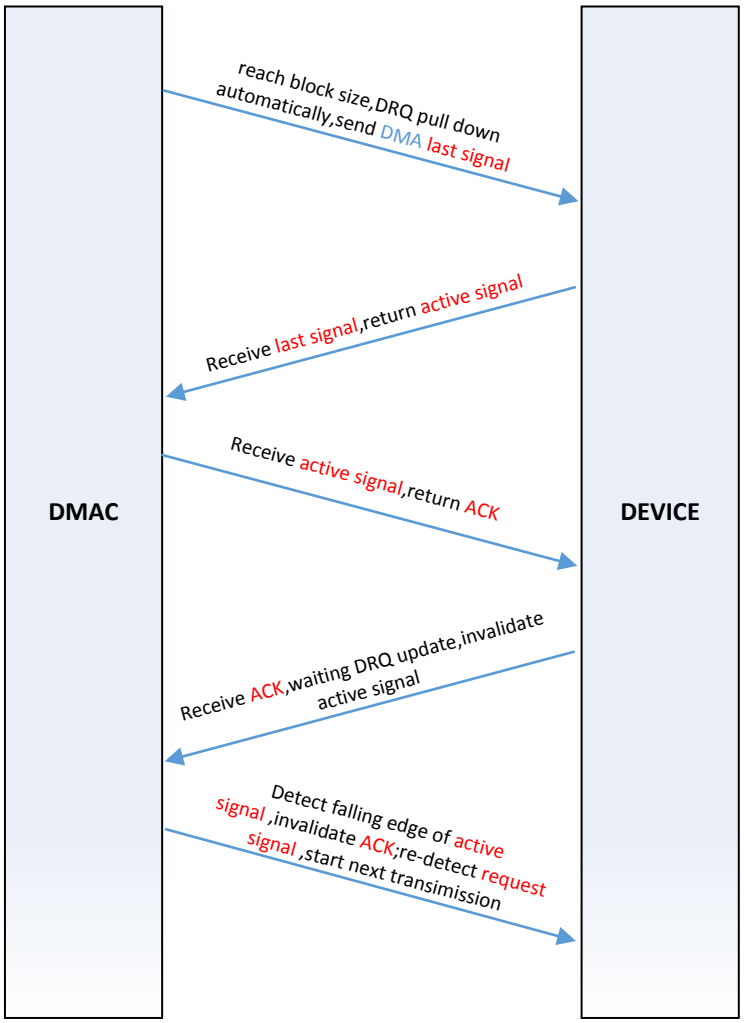

Figure 3- 25. DMA Transfer Mode

3.9.3.8. Auto-alignment Function

The DMA supports address alignment of non-IO devices, that is when the start address of non-IO devices is non 32-byte aligned, DMA firstly aligns the burst transfer within 32-byte to 32-byte. If the device of a DMA channel is configured to non-IO type, and the start address is 0x86, then DMA firstly aligns 26-byte burst transfer to 0xA0, then DMA transfers by 64-byte burst(maximum transfer amount of MBUS allowed). The address alignment function helps to improve the DRAM access efficiency.

IO devices do not support address alignment, so the bit width of IO devices must match the address offset, or not DMA ignores the non-consistency and indirectly transmits data of the corresponding bit width to the address.

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3.9.3.9. Operating Mode

3.9.3.9.1. Clock Control

- The DMA clock is synchronous with AHB1 clock. Make sure that open the DMA gating bit of AHB1 clock before access DMA register.
- The reset input signal of DMA is asynchronous with AHB1, and is low valid by default. Make sure that de-assert the reset signal of DMA before access DMA register.
- To avoid indefinite state within registers , firstly de-assert the reset signal, secondly open the gating bit of AHB1.
- DMA has the function of clock auto gating ,DMA clock can be disabled in DMA idle state using software to reduce power consumption. DMA enables clock auto gating by default.

3.9.3.9.2. DMA Transfer Process

The DMA transfer process is as follows.

(1) Request DMA channel, and judge the idle state of the channel by the enable or disable of DMA channel.
(2) Write the descriptor with 6-word into memory, the descriptor must be word-aligned. Refer to 3.9.3.4 DMA descriptor in detail.
(3) Write the start address of storing descriptor to **DMA_DESC_ADDR_REG**.
(4) Enable DMA channel, and write the corresponding channel to **DMA_EN_REG**.
(5) DMA obtains the descriptor information.
(6) Start to transmit a package ,when half package is completed, DMA sends **Half Package Transfer Interrupt**; when total package is completed, DMA sends **Package End Transfer Interrupt**. These interrupt status can be read by **DMA_IRQ_PEND_REG**.
(7) Set **DMA_PAU_REG** to pause or resume the data transfer.
(8) After completed the total package transfer, DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; if the link is other value, the next package starts to transmit. When the transfer ends, DMA sends **Queue End Transfer Interrupt**.
(9) Disable the DMA channel.

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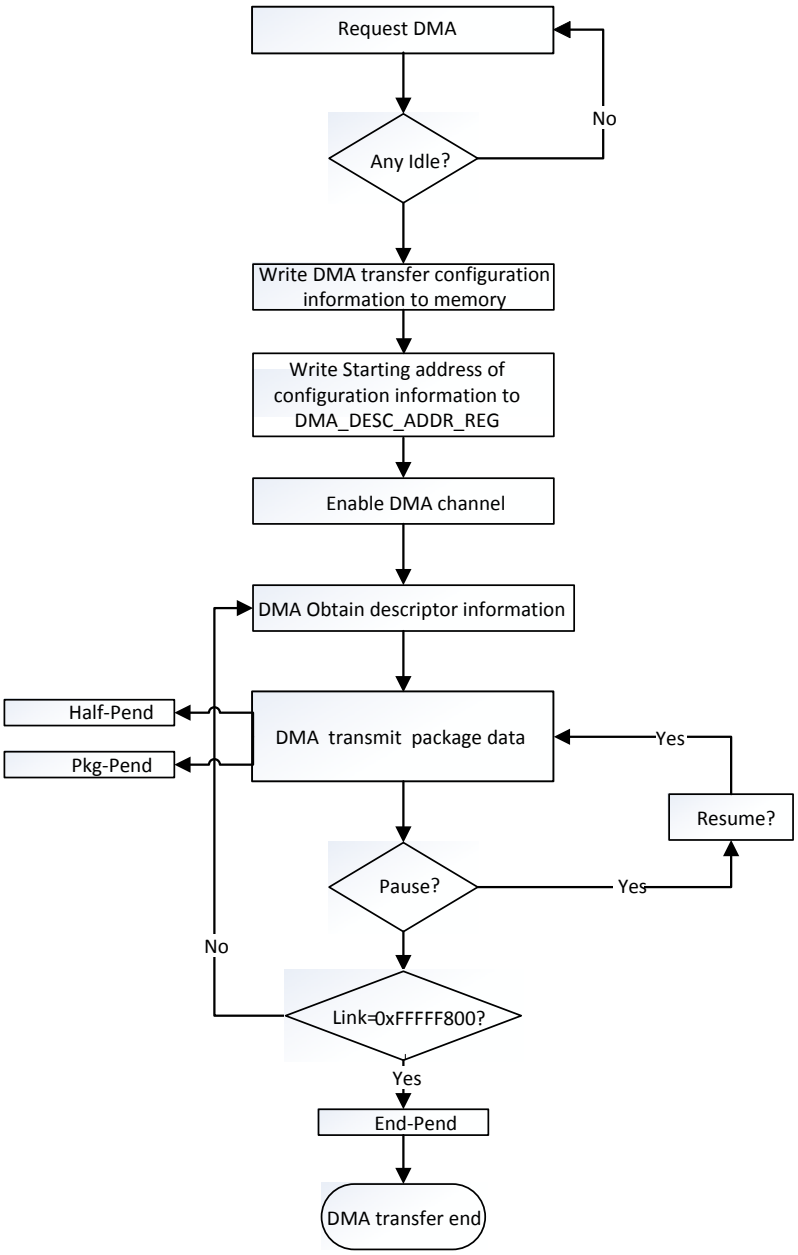

Figure 3- 26. DMA Transfer Process

3.9.3.9.3. DMA Interrupt

(1) Enable interrupt: write the corresponding interrupt enable of **DMA_IRQ_EN_REG**, when the corresponding interrupt condition is satisfied,the corresponding interrupt generates.

(2) After enter the interrupt process, write **DMA_IRQ_PEND_REG** to clear the interrupt pending，and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

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3.9.4. Programming Guidelines

(1) The transfer width of IO type device is consistent with the offset of start address.
(2) MBUS protocol does not support read operation of non-integer word, so for non-integer word read operation, device must ignore redundant inconsistent data between data width and configuration, that is, the device of non-integer word must interpret DMA demand through its FIFO width instead of read demand width.
(3) When the DMA transfer is paused, this is equivalent to invalid DRQ. Because DMA transfer command has a certain time delay, DMA will not stop transfer immediately until the current command and the command in Arbiter finished, at most 32byte data.

DMA application example :

```
writel(0x00000000, mem_address + 0x00);   //Setting configuration, mem_address must be word-aligned
writel(0x00001000, mem_address + 0x04);    // Setting the start address for the source device
writel(0x20000000, mem_address + 0x08);   //Setting the start address for the destination device
writel(0x00000020, mem_address + 0x0C);   // Setting data package size
writel(0x00000000, mem_address + 0x10);   //Setting parameter
writel(0xFFFFF800, mem_address + 0x14);    //Setting the start address for the next descriptor
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Setting the start address for the DMA channel0 descriptor
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure writing operation valid
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);      // Enable DMA channel0 transfer
```

DMA supports increasing data package in transfer, there are a few points to note here.

- When the value of **DMA Channel Descriptor Address Register** is 0xFFFFF800, it indicates that DMA channel has got back the descriptor of the last package. When DMA channel completed the package data transfer, DMA channel will stop automatically data transfer.
- If needing increase data package,then at first it is essential to judge that whether DMA channel has got back the descriptor of the last package, if DMA channel has got back the descriptor of the last package, then this is impossible for increasing data package, DMA channel need start again. If DMA is not transmitting the last package,then the last descriptor address 0xFFFFF800 can be changed to the start address of the next descriptor.
- To ensure that the data changed valid, we can read again the value of **DMA Channel Descriptor Address Register** after changed the data. If there is not 0xFFFFF800,then it indicates that increasing data package is succeed, and fail otherwise. Because the process of increasing data package need some time, during this time,DMA channel may get back the descriptor of the last package.At the moment we can read again **DMA Channel Current Source Address Register** and **DMA Channel Current Destination Address Register**, if the increasing memory address accords with the information of the increasing data package, then the increasing data package is succeed, and fail otherwise.
- To ensure the higher success rate, it is suggested that increase data package before half package interrupt of penultimate data package.

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3.9.5. Register List

Module Name	Base Address
DMA	0x03002000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register 1
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register 0
DMA_IRQ_PEND_REG1	0x0014	DMA IRQ Pending Register 1
DMA_SEC_REG	0x0020	DMA Security Register
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x0040	DMA Channel Enable Register (N=0~11)
DMA_PAU_REG	0x0100+N*0x0040+0x0004	DMA Channel Pause Register(N=0~11)
DMA_DESC_ADDR_REG	0x0100+N*0x0040+0x0008	DMA Channel Start Address Register(N=0~11)
DMA_CFG_REG	0x0100+N*0x0040+0x000C	DMA Channel Configuration Register(N=0~11)
DMA_CUR_SRC_REG	0x0100+N*0x0040+0x0010	DMA Channel Current Source Register(N=0~11)
DMA_CUR_DEST_REG	0x0100+N*0x0040+0x0014	DMA Channel Current Destination Register(N=0~11)
DMA_BCNT_LEFT_REG	0x0100+N*0x0040+0x0018	DMA Channel Byte Counter Left Register(N=0~11)
DMA_PARA_REG	0x0100+N*0x0040+0x001C	DMA Channel Parameter Register(N=0~11)
DMA_MODE_REG	0x0100+N*0x0040+0x0028	DMA Mode Register(N=0~11)
DMA_FDESC_ADDR_REG	0x0100+N*0x0040+0x002C	DMA Former Descriptor Address Register(N=0~11)
DMA_PKG_NUM_REG	0x0100+N*0x0040+0x0030	DMA Package Number Register(N=0~11)

3.9.6. Register Description

3.9.6.1. DMA IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable

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			0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable 0: Disable

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			1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN

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			DMA 0 Half Package Transfer Interrupt Enable 0: Disable 1: Enable

3.9.6.2. DMA IRQ Enable Register1 (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11 Package End Transfer Interrupt Enable 0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA 10 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA 10 Package End Transfer Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	DMA10_HLAF_IRQ_EN DMA 10 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA 9 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA 9 Package End Transfer Interrupt Enable 0: Disable 1: Enable

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4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA 9 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA 8 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA 8 Package End Transfer Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA 8 Half Package Transfer Interrupt Enable 0: Disable 1: Enable

3.9.6.3. DMA IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset:0x0010			**Register Name: DMA_IRQ_PEND_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

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25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit will

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			clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

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3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND DMA 0 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.9.6.4. DMA IRQ Pending Status Register 1 (Default Value: 0x0000_0000)

Offset:0x0014			**Register Name: DMA_IRQ_PEND_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND DMA 11 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
13	R/W1C	0x0	DMA11_PKG_IRQ_PEND DMA 11 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND DMA 11 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND DMA 10 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_PEND

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			DMA 10 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND DMA 10 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND DMA 9 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_PEND DMA 9 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND DMA 9 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND DMA 8 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_PEND DMA 8 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND DMA 8 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

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3.9.6.5. DMA Security Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: DMA_SEC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DMA11_SEC DMA channel 11 security 0: Secure 1: Non-secure
10	R/W	0x0	DMA10_SEC DMA channel 10 security 0: Secure 1: Non-secure
9	R/W	0x0	DMA9_SEC DMA channel 9 security 0: Secure 1: Non-secure
8	R/W	0x0	DMA8_SEC DMA channel 8 security 0: Secure 1: Non-secure
7	R/W	0x0	DMA7_SEC DMA channel 7 security 0: Secure 1: Non-secure
6	R/W	0x0	DMA6_SEC DMA channel 6 security 0: Secure 1: Non-secure
5	R/W	0x0	DMA5_SEC DMA channel 5 security 0: Secure 1: Non-secure
4	R/W	0x0	DMA4_SEC DMA channel 4 security 0: Secure 1: Non-secure
3	R/W	0x0	DMA3_SEC DMA channel 3 security 0: Secure 1: Non-secure
2	R/W	0x0	DMA2_SEC DMA channel 2 security 0: Secure 1: Non-secure

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1	R/W	0x0	DMA1_SEC DMA channel 1 security 0: Secure 1: Non-secure
0	R/W	0x0	DMA0_SEC DMA channel 0 security 0: Secure 1: Non-secure

3.9.6.6. DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT DMA MCLK interface circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT DMA common circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT DMA channel circuit auto gating bit 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, the bit-2 should be set up.

3.9.6.7. DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	MBUS FIFO Status 0: Empty 1: Not Empty
29:12	/	/	/
11	R	0x0	DMA11_STATUS DMA Channel 11 Status 0: Idle

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			1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status 0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status 0: Idle 1: Busy

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3.9.6.8. DMA Channel Enable Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040 (N=0~11)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN DMA Channel Enable 0: Disable 1: Enable

3.9.6.9. DMA Channel Pause Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0004(N=0~11)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE Pausing DMA Channel Transfer Data 0: Resume Transferring 1: Pause Transferring

3.9.6.10. DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0008(N=0~11)			Register Name: DMA_DESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMA_DESC_ADDR DMA Channel Descriptor Address The Descriptor Address must be word-aligned.

3.9.6.11. DMA Channel Configuration Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x000C(N=0~11)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH DMA Destination Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit

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24	R	0x0	DMA_ADDR_MODE DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE DMA Destination Block Size 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH DMA Source Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE DMA Source Address Mode 0: Linear Mode 1: IO Mode
7:6	R	0x0	DMA_SRC_BLOCK_SIZE DMA Source Block Size 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.9.6.12. DMA Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0010(N=0~11)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC DMA Channel Current Source Address, read only.

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3.9.6.13. DMA Chacnnel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0014(N=0~11)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST DMA Channel Current Destination Address, read only.

3.9.6.14. DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0018(N=0~11)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT DMA Channel Byte Counter Left, read only.

3.9.6.15. DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x001C(N=0~11)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC Wait Clock Cycles

3.9.6.16. DMA Mode Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0028(N=0~11)			Register Name: DMA_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE 0: Wait mode 1: Handshake mode
2	R/W	0x0	DMA_SRC_MODE 0: Wait mode 1: Handshake mode
1:0	/	/	/

3.9.6.17. DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x002C(N=0~11)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	R	0x0	DMA_FDESC_ADDR This register is used to store the former value of DMA Channel Descriptor Address Register.

3.9.6.18. DMA Package Number Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0030(N=0~11)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM This register will record the number of packages which has been completed in one transmission.

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3.10. RTC

3.10.1. Overview

The RTC(Real Time Clock) is used to display the real time and periodically wakeup .The RTC can display the year, month, day, week, hour, minute, second in real time. It has a built-in leap year generator and a independent power pin (RTC_VIO). The RTC has the independent power to continue to work in system power-off.

The RTC has the following features:

- Provides a 7-bit counter for counting year, 4-bit counter for counting month, 5-bit counter for counting day, 3-bit counter for counting week, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32768Hz low-frequency oscillator for count clock
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- Stores power-off information in eight 32-bit general purpose register
- Records BROM related information

3.10.2. Block Diagram

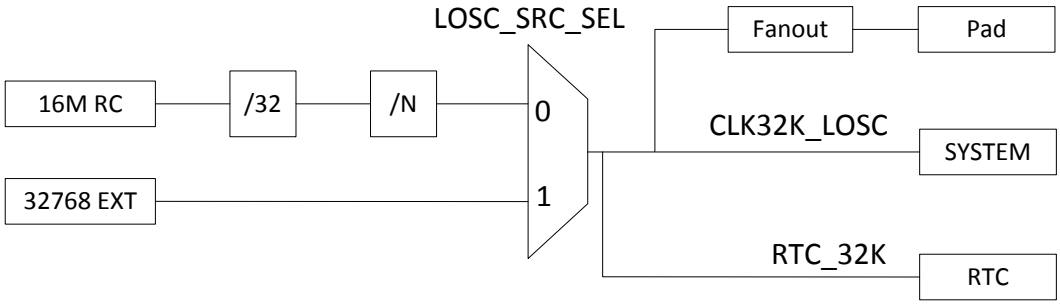

Figure 3- 27. RTC Block Diagram

3.10.3. Operations and Functional Descriptions

3.10.3.1. External Signals

Table 3- 9. RTC External Signals

Signal	Description
X32KIN	32KHz oscillator input
X32KOUT	32KHz oscillator output
X32KFOUT	32KHz clock fanout, provides low frequency clock for external devices

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NMI	Alarm wakeup generates low level into NMI
RTC-VIO	RTC low voltage,generated via internal LDO
VCC-RTC	RTC high voltage,generated via external power

3.10.3.2. Clock and Reset

The RTC module has the independent reset signal, the signal follows VCC-RTC. When VCC-RTC powers on, the reset signal resets the RTC module; after VCC-RTC reaches stable, the reset signal always holds high level.

3.10.3.3. Typical Application

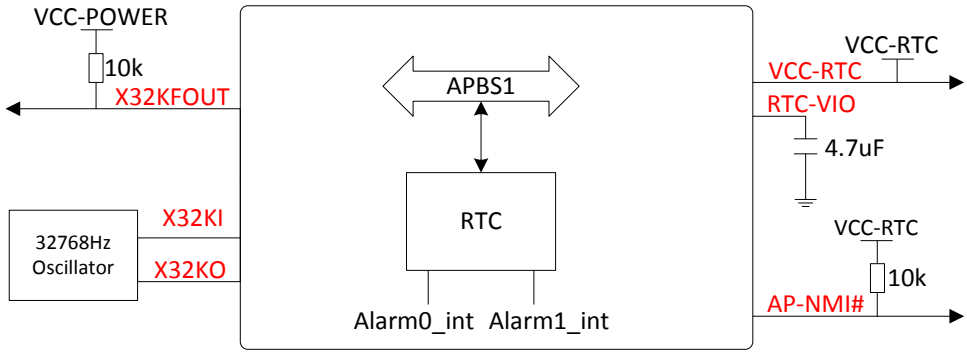

Figure 3- 28. RTC Application Diagram

The system accesses RTC register by APB1 to generate the real time.

The external low-frequency oscillator must be 32.768 kHz.

If the external devices need low-frequency oscillator, X32KFOUT can provide.

AP-NMI# and alarm0 in common generate low level signal.

3.10.3.4. Function Implementation

3.10.3.4.1. Clock Sources

The RTC has two clock sources: internal RC , external low frequency oscillator.

The internal RC can change RTC clock by changing division ratio ;the external clock can not change clock.

The RTC selects the internal RC by default, when the system starts, the RTC can select by software the external low frequency oscillator to provide much accuracy clock.

The clock accurate of the RTC is related to the accurate of the external low frequency oscillator. The external oscillator usually selects 32.768 kHz oscillator with ±20ppm frequency tolerance.

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3.10.3.4.2. Real Time Clock

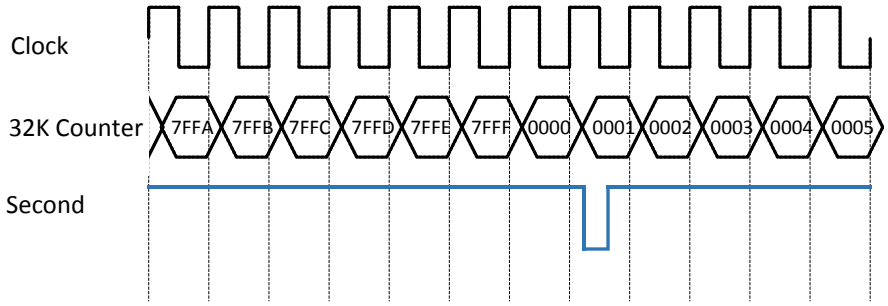

Figure 3- 29. RTC Counter

The 32K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x8000,32KHz counter starts to count again from 0, and the second counter adds 1. The 32KHz counter block diagram is as follows.

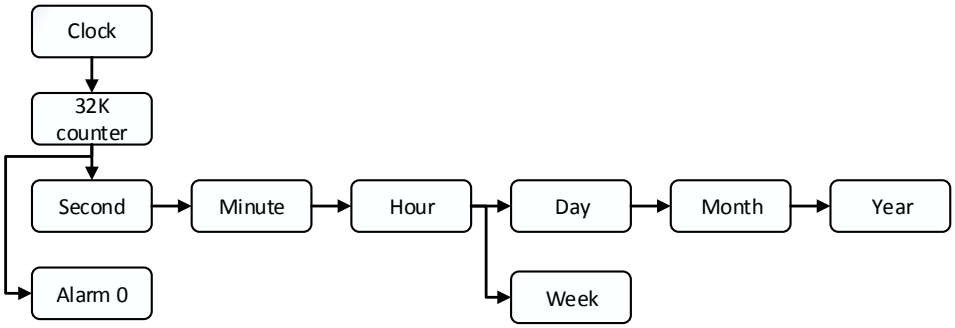

Figure 3- 30. RTC 32KHz Counter Block Diagram

According to above implementation, the changing range of each counter is as follows.

Table 3- 10. RTC Counter Changing Range

Counter	Range
Second	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Minute	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Hour	If the counter value is not in the range from 0 to 23, then the counter value can change to 23 automatically.
Week	If the counter value is not in the range from 0 to 6, then the counter value can change to 6 automatically.
Day	If the counter value is not in the range from 1 to 31, then the counter value can change to the maximum value of that month automatically.
Month	If the counter value is not in the range from 1 to 12, then the counter value can change to 12 automatically.
Year	The software can set a reference year, the leap year can only set by software.

3.10.3.4.3. Alarm 0

The principle of alarm0 is similar to the second counter, the difference is that alarm0 is a 32-bit down counter. When the counter decreases to 0 from the initial value, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

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3.10.3.4.4. Alarm 1

The alarm1 can set alarm response time and the response cycle. When the system real time satisfies the setting time, the RTC generates alram1 interrupt to handle alarm interrupt function.

3.10.3.4.5. Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.10.3.4.6. RTC-VIO

The RTC module has a LDO ,the input source of the LDO is VCC-RTC,the output of the LDO is RTC-VIO,the value of RTC-VIO is adjustable,it is mainly used for internal digital logic.

3.10.3.5. Operating Mode

3.10.3.5.1. RTC Clock Control

(1) Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default, when the system starts, the clock source can be switched to the external 32K oscillator by software.
(2) Auto switch: After enabled the bit[14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external oscillator could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.
(3) After auto switch is valid, the clock source status bit cannot be changed, because the two functions are independent.

3.10.3.5.2. RTC Calendar

(1) Write time initial value: Write the current time to **RTC_HH_MM_SS_REG** and **RTC_YY_MM_DD_REG**.
(2) After update time, the RTC restarts to count again .The software can read the current time anytime.
(3) The leap year function can be set only by the software.

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3.10.3.5.3. Alarm0

(1) Enable alram0 interrupt by writing **ALARM0_IRQ_EN**.
(2) Set the counter initial value, write the count-down second number to **ALARM0_COUNTER_REG**.
(3) Enable alarm0 function by writing **ALARM0_ENABLE_REG**, then the software can query alarm count value in real time.
(4) After enter the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(5) Resume the interrupt and continue to execute the interrupted process.
(6) Power-off wakeup is generated via SoC hardware and PMIC, software only need set pending condition of alarm0, and set 1 to **ALARM0_CONFIG_REG**.

3.10.3.5.4. Alarm 1

(1) Set alarm1 initial value : write the hour,minute,second of alarm1 to **ALARM1_WK_HH_MM_SS**.
(2) Write alarm week number enable bit to **ALARM1_EN_REG**.
(3) When the bit[20:0] of **RTC_HH_MM_SS_REG** is equal to **ALARM1_WK_HH_MM-SS,** and the bit[31:29] of **RTC_HH_MM_SS_REG** is equal to the week number of **ALARM1_EN_REG**, then the condition of alarm 1 is satisfied, pending is set automatically by hardware.
(4) When **ALARM0_IRQ_EN** is set to 1, the RTC enters into the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(5) Resume the interrupt and continue to execute the interrupted process.

3.10.3.5.5. Fanout

The bit0 of **LOSC_OUT_GATING_REG** is set to 1, and external pull-up resistor and voltage is normal, then 32.768kHz square wave can be output.

3.10.3.5.6. Pad Hold

When the corresponding bit of **GPL_HOLD_OUTPUT_REG** and **GPM_HOLD_OUTPUT_REG** is set to 1, the corresponding pin can hold in stable state(high level,low level or high impedance). The function is used to prevent output pin from changing when corresponding power changes.

3.10.4. Programming Guidelines

3.10.4.1. RTC Clock Sources Setting

```
writel(0x16aa4000,LOSC_CTRL);      //write key field
writel(0x16aa4001,LOSC_CTRL);      //select external clock
```

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3.10.4.2. Real Time Clock

```
writel(0x00173b3b,RTC_HMS);
writel(1<<22|1<<8|31<<0,RTC_YMD);
readl(RTC_HMS);
readl(RTC_YMD);
```

3.10.4.3. Alarm 0

```
irq_request(GIC_SRC_R_ALM0,ALM0_HANDLER);
irq_enable(GIC_SRC_R_ALM0);
writel(1,ALM0_COUNTER);                    //set 1 second corresponding to normal mode
writel(1,ALM0_EN);
writel(1,ALM_CONFIG); //NMI output
while(!readl(ALM0_IRQ_STA));
writel(1,ALM0_IRQ_EN);
while(readl(ALM0_IRQ_STA));
```

3.10.4.4. Alarm 1

```
irq_request(GIC_SRC_R_ALM1,ALM1_HANDLER);
irq_enable(GIC_SRC_R_ALM1);
writel(0,ALM1_WK_HMS);
writel(0x7f,ALM1_EN);
writel(1,ALM1_IRQ_STA);
writel(0x00173b3b | week<<29,RTC_HMS);  //set 1 second corresponding to normal mode
while(readl(RTC_HMS)&0xff);
while(!readl(ALM1_IRQ_STA));
writel(1,ALM1_IRQ_EN);
while(readl(ALM1_IRQ_STA));
```

3.10.5. Register List

Module Name	Base Address
RTC	0x07000000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register

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INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
RTC_YY_MM_DD_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM-SS	0x0040	Alarm 1 Week HMS Register
ALARM1_ENABLE_REG	0x0044	Alarm 1 Enable Register
ALARM1_IRQ_EN	0x0048	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	0x004C	Alarm 1 IRQ Status Register
ALARM0_CONFIG_REG	0x0050	Alarm 0 Configuration Register
LOSC_OUT_GATING_REG	0x0060	LOSC Output Gating Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0~7)
GPL_HOLD_OUTPUT_REG	0x0180	GPL Hold Output Register
GPM_HOLD_OUTPUT_REG	0x0184	GPM Hold Output Register
RTC-VIO_REG	0x0190	RTC-VIO Regulate Register
CPU_SOFT_ENT_REG0	0x01BC	CPU Software Entry Register 0
SUP_STAN_FLAG_REG	0x01F8	Super Standby Flag Register
CPU_SOFT_ENT_REG1	0x01FC	CPU Software Entry Register 1
CRY_CONFIG_REG	0x0210	Crypto Configuration Register
CRY_KEY_REG	0x0214	Crypto Key Register
CRY_EN_REG	0x0218	Crypto Enable Register

3.10.6. Register Description

3.10.6.1. LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			**Register Name: LOSC_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN LOSC Auto Switch Enable 0: Disable 1: Enable
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE ALARM DD-HH-MM-SS access

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			After writing the **Alarm 1 Week HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE RTC HH-MM-SS access After writing the **RTC HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished. After writing the **RTC HH-MM-SS Register**, the **RTC HH-MM-SS Register** will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD_ACCE RTC YY-MM-DD access After writing the **RTC YY-MM-DD Register**, this bit is set and it will be cleared until the real writing operation is finished. After writing the **RTC YY-MM-DD Register**, the **RTC YY-MM-DD Register** will be refreshed for at most one second.
6:4	/	/	/
3:2	R/W	0x0	EXT_LOSC_GSM External 32768Hz Crystal GSM 00: Low 01: / 10: / 11 High
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock source Select. '**N**' is the value of **Internal OSC Clock Prescalar Register**. 0: Internal OSC/N 1: External 32.768kHz OSC Internal OSC is about 16MHz.

NOTE

If the bit[9:7] of LOSC_CTRL_REG is set, the corresponding of Alarm 1 Week HH-MM-SS Register, RTC HH-MM-SS Register, RTC YY-MM-DD Register cannot be written.

3.10.6.2. LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			**Register Name: LOSC_AUTO_SWT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA 0: External 32.768kHz OSC work normally 1: External 32.768kHz OSC work abnormally
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending 0: No effect

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			1: Auto switches pending Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC Clock Source Status. '**N**' is the value of **Internal OSC Clock Prescalar Register**. 0: Internal OSC /(32* N) 1: External 32.768KHz OSC The Internal OSC is 16MHz

3.10.6.3. Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			**Register Name: INTOSC_CLK_PRESCAL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0xF	INTOSC_CLK_PRESCAL Internal OSC Clock Prescalar value N. 00000: 1 00001: 2 00010: 3 ..... 11111: 32

3.10.6.4. RTC YY-MM-DD Register

Offset:0x0010			**Register Name: RTC_YY_MM_DD_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	LEAP Leap Year 0: Not 1: Leap year This bit can not set by hardware. It should be set or cleared by software.
22:16	R/W	UDF	YEAR Year Range from 0~127.
15:12	/	/	/
11:8	R/W	UDF	MONTH Month Range from 1~12.
7:5	/	/	/
4:0	R/W	UDF	DAY Day

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			Range from 1~31. The number of days in different month may be different.

NOTE

If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area.

3.10.6.5. RTC HH-MM-SS Register

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	WK_NO Week number 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
28:21	/	/	/
20:16	R/W	UDF	HOUR Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Range from 0~59
7:6	/	/	/
5:0	R/W	UDF	SECOND Range from 0~59

NOTE

If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.10.6.6. Alarm 0 Counter Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: ALARM0_COUNTER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is based on second. If the second is set to 0, it will be 1 second in fact.

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3.10.6.7. Alarm 0 Current Value Register

Offset:0x0024			Register Name: ALARM0_CUR_VLU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	UDF	ALARM0_CUR_VLU Check Alarm 0 Counter Current Values. If the second is set to 0, it will be 1 second in fact.

3.10.6.8. Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable If this bit is set to "1", the valid bits of **Alarm 0 Counter Register** will down count to zero, and the alarm pending bit will be set to "1". 0: Disable 1: Enable

3.10.6.9. Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: ALARM0_IRQ_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.10.6.10. Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

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3.10.6.11. Alarm 1 Week HH-MM-SS Register

Offset:0x0040			Register Name: ALARM1_WK_HH_MM_SS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Range from 0~23.
15:14	/	/	/
13:8	R/W	UDF	MINUTE Range from 0~59.
7:6	/	/	/
5:0	R/W	UDF	SECOND Range from 0~59.

NOTE

If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.10.6.12. Alarm 1 Enable Register (Default Value: 0x0000_0000)

Offset:0x0044			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	WK6_ALM1_EN Week 6 (Sunday) Alarm 1 Enable 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 6, the week 6 alarm irq pending bit will be set to “1”.
5	R/W	0x0	WK5_ALM1_EN Week 5 (Saturday) Alarm 1 Enable 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 5, the week 5 alarm irq pending bit will be set to “1”.
4	R/W	0x0	WK4_ALM1_EN Week 4 (Friday) Alarm 1 Enable 0: Disable

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			1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the register bit[31:29] of **RTC HH-MM-SS Register** is 4, the week 4 alarm irq pending bit will be set to “1”.
3	R/W	0x0	WK3_ALM1_EN Week 3 (Thursday) Alarm 1 Enable 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 3, the week 3 alarm irq pending bit will be set to “1”.
2	R/W	0x0	WK2_ALM1_EN Week 2 (Wednesday) Alarm 1 Enable 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 2, the week 2 alarm irq pending bit will be set to “1”.
1	R/W	0x0	WK1_ALM1_EN Week 1 (Tuesday) Alarm 1 Enable 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 1, the week 1 alarm irq pending bit will be set to “1”.
0	R/W	0x0	WK0_ALM1_EN Week 0 (Monday) Alarm 1 Enable 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 0, the week 0 alarm irq pending bit will be set to “1”.

3.10.6.13. Alarm 1 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0048			**Register Name: ALARM1_IRQ_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN

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			Alarm 1 IRQ Enable 0: Disable 1: Enable

3.10.6.14. Alarm 1 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x004C			Register Name: ALARM1_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM1_WEEK_IRQ_PEND Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending 0: No effect 1: Pending, week counter value is reached If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.10.6.15. Alarm 0 Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM0_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_WAKEUP Configuration of alarm0 wake up output 0: Disable alarm0 wake up output 1: Enable alarm0 wake up output

3.10.6.16. LOSC Output Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: LOSC_OUT_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	LOSC_OUT_GATING Configuration of LOSC output, and without LOSC output by default. 0: Disable LOSC output gating 1: Enable LOSC output gating

3.10.6.17. General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~7)			Register Name: GP_DATA_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	R/W	0x0	GP_DATA Data [31:0]

NOTE

General purpose register 0~7 value can be stored if the RTC-VIO is larger than 1.0V.

3.10.6.18. GPL Hold Output Register (Default Value: 0x0000_0000)

Offset:0x0180			Register Name: GPL_HOLD_OUTPUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	GPL9_HOLD_OUTPUT Hold the output of GPIOL9 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
8	R/W	0x0	GPL8_HOLD_OUTPUT Hold the output of GPIOL8 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
7	R/W	0x0	GPL7_HOLD_OUTPUT Hold the output of GPIOL7 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPL6_HOLD_OUTPUT Hold the output of GPIOL6 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPL5_HOLD_OUTPUT Hold the output of GPIOL5 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPL4_HOLD_OUTPUT Hold the output of GPIOL4 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other output may not

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			hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPL3_HOLD_OUTPUT Hold the output of GPIOL3 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPL2_HOLD_OUTPUT Hold the output of GPIOL2 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPL1_HOLD_OUTPUT Hold the output of GPIOL1 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPL0_HOLD_OUTPUT Hold the output of GPIOL0 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

3.10.6.19. GPM Hold Output Register (Default Value: 0x0000_0000)

Offset:0x0184			**Register Name: GPM_HOLD_OUTPUT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	GPM31_HOLD_OUTPUT Hold the output of GPIOM31 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
30	R/W	0x0	GPM30_HOLD_OUTPUT Hold the output of GPIOM30 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

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29	R/W	0x0	GPM29_HOLD_OUTPUT Hold the output of GPIOM29 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
28	R/W	0x0	GPM28_HOLD_OUTPUT Hold the output of GPIOM28 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
27	R/W	0x0	GPM27_HOLD_OUTPUT Hold the output of GPIOM27 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
26	R/W	0x0	GPM26_HOLD_OUTPUT Hold the output of GPIOM26 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
25	R/W	0x0	GPM25_HOLD_OUTPUT Hold the output of GPIOM25 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
24	R/W	0x0	GPM24_HOLD_OUTPUT Hold the output of GPIOM24 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
23	R/W	0x0	Reserved
22	R/W	0x0	Reserved
21	R/W	0x0	GPM21_HOLD_OUTPUT Hold the output of GPIOM21 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
20	R/W	0x0	GPM20_HOLD_OUTPUT

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			Hold the output of GPIOM20 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
19	R/W	0x0	GPM19_HOLD_OUTPUT Hold the output of GPIOM19 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
18	R/W	0x0	GPM18_HOLD_OUTPUT Hold the output of GPIOM18 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
17	R/W	0x0	GPM17_HOLD_OUTPUT Hold the output of GPIOM17 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
16	R/W	0x0	GPM16_HOLD_OUTPUT Hold the output of GPIOM16 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
15	R/W	0x0	GPM15_HOLD_OUTPUT Hold the output of GPIOM15 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
14	R/W	0x0	GPM14_HOLD_OUTPUT Hold the output of GPIOM14 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
13	R/W	0x0	GPM13_HOLD_OUTPUT Hold the output of GPIOM13 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on.

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			0: Hold disable 1: Hold enable
12	R/W	0x0	GPM12_HOLD_OUTPUT Hold the output of GPIOM12 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
11	R/W	0x0	GPM11_HOLD_OUTPUT Hold the output of GPIOM11 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
10	R/W	0x0	GPM10_HOLD_OUTPUT Hold the output of GPIOM10 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
9	R/W	0x0	GPM9_HOLD_OUTPUT Hold the output of GPIOM9 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
8	R/W	0x0	GPM8_HOLD_OUTPUT Hold the output of GPIOM8 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
7	R/W	0x0	GPM7_HOLD_OUTPUT Hold the output of GPIOM7 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPM6_HOLD_OUTPUT Hold the output of GPIOM6 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPM5_HOLD_OUTPUT

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			Hold the output of GPIOM5 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPM4_HOLD_OUTPUT Hold the output of GPIOM4 when the power of system changes. The outputs must be low level (0) or high level (1) or High-Z; any other output may not hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPM3_HOLD_OUTPUT Hold the output of GPIOM3 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPM2_HOLD_OUTPUT Hold the output of GPIOM2 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPM1_HOLD_OUTPUT Hold the output of GPIOM1 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPM0_HOLD_OUTPUT Hold the output of GPIOM0 when the power of system changes. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable

3.10.6.20. RTC-VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			**Register Name: RTC-VIO_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x4	RTC-VIO_REGU These bits are useful for regulating the RTC-VIO from 0.7V to 1.4V , and the regulation step is 0.1V.

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			000: 0.7V 001: 0.8V 010: 0.9V 011: 1.0V 100: 1.1V 101: 1.2V 110: 1.3V 111: 1.4V

3.10.6.21. CPU Software Entry Register (Default Value: 0x0000_0000)

Offset:0x01BC			Register Name: CPU_SOFT_ENT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Boot CPU software entry register when acting from hot plug or Non-boot CPU software entry register.

3.10.6.22. Super Standby Flag Register (Default Value: 0x0000_0000)

Offset:0x01F8			Register Name: SUP_STAN_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SUP_STANDBY_FLAG Key Field Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only fellow the appropriate process, the super standby flag can be written in the lower 16 bits. Refer to Description and Diagram.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA Refer to Description and Diagram

NOTE

When system is turned on, the low 16 bits in the Super Standby Flag Register should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written 0x16AA at first. Then, software programmer must write 0xAA16XXXX in the Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID.

3.10.6.23. CPU Software Entry Register1 (Default Value: 0x0000_0000)

Offset:0x01FC			Register Name: CPU_SOFT_ENT_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CPU software entry register when acting from super standby.

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3.10.6.24. Crypto Configuration Register (Default Value: 0x0000_0000)

Offset:0x0210			Register Name: CRY_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field

3.10.6.25. Crypto Key Register (Default Value: 0x0000_0000)

Offset:0x0214			Register Name: CRY_KEY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CRY_KEY Crypto Key

3.10.6.26. Crypto Enable Register (Default Value: 0x0000_0000)

Offset:0x0218			Register Name: CRY_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypto Enable

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3.11. Thermal Sensor Controller

3.11.1. Overview

Thermal sensors have became common elements in wide range of modern system on chip (SOC) platform. Thermal sensors are used to constantly monitor the temperature on the chip.

The Thermal Sensor Controller(THS) embeds 4 thermal sensors, sensor0 for CPU1,sensor1 for CPU0,sensor2 for DDR and sensor3 for GPU. Thermal sensors can generate interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

The THS has the following features:

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Power supply voltage:AVCC
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.11.2. Block Diagram

Figure 3-31 shows a block diagram of the Thermal Sensor Controller.

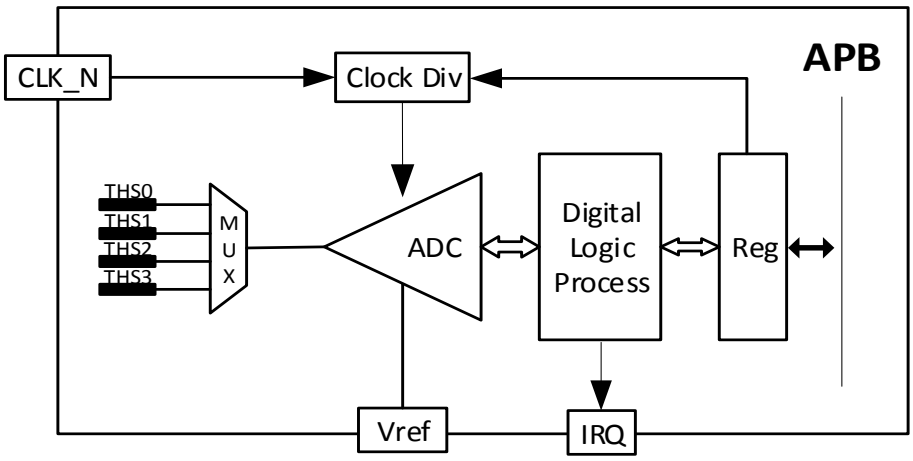

Figure 3- 31. Thermal Sensor Controller Block Diagram

3.11.3. Operations and Functional Descriptions

3.11.3.1. Clock Sources

The THS gets one clock source. Table 3-11 describes the clock source for Thermal Sensor Controller. Users can see

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Clock Controller Unit(CCU) for clock setting, configuration and gating information.

Table 3- 11. Thermal Sensor Controller Clock Sources

Clock Sources	Description
OSC24M	24MHz OSC

3.11.3.2. Timing Requirements

CLK_IN = 24MHz
CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)
TACQ> 1/(24MHz/24Cycles)
THERMAL_PER > ADC Sample Frequency > TACQ+CONV_TIME

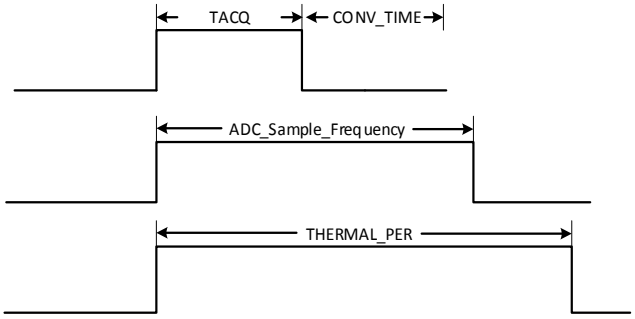

Figure 3- 32. Thermal Sensor Time Requirement

3.11.3.3. Interrupt

The THS has four interrupt sources, such as DATA_IRQ , SHUTDOWN_IRQ, ALARM_IRQ and ALARM_OFF_IRQ. Figure 3-33 shows the thermal sensor interrupt sources.

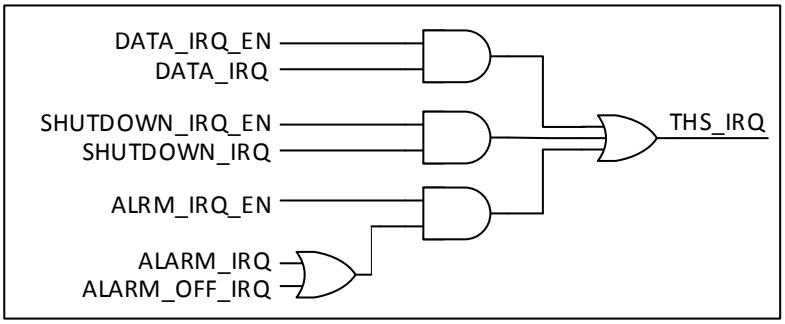

Figure 3- 33. Thermal Sensor Controller Interrupt Source

When temperature is higher than Alarm_Threshold, ALARM_IRQ is generated. When temperature is lower than Alarm_Off_Thershold, ALARM_OFF_IRQ is generated. ALARM_OFF_IRQ is fall edge trigger.

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3.11.3.4. THS Temperature Conversion Formula

T= (sensor_data - 2266)/(-8.532), the unit of T is Celsius.
sensor_data: read from sensor data register.

3.11.4. Programming Guidelines

The initial process of the THS is as follows.

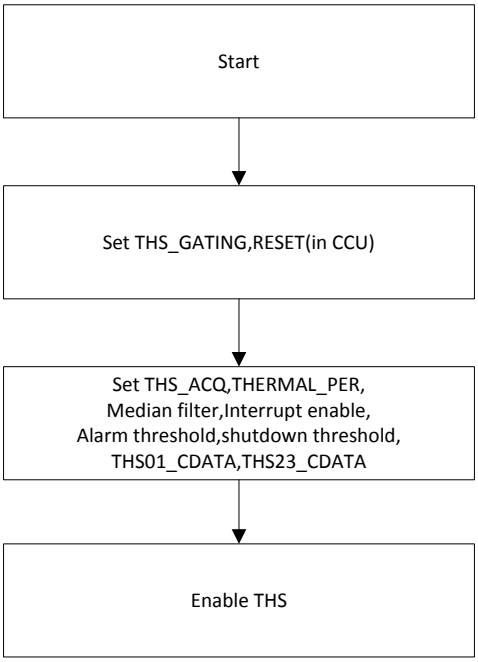

Figure 3- 34. THS Initial Process

The formula of THS is y=-ax+b. In FT stage, THS is calibrated through ambient temperature, the calibration value is written in EFUSE. Please refer to SID Spec about EFUSE information.

Before enabling THS, read EFUSE value and write the value to **THS01_CDATA, THS23_CDATA**.

(1).Query Mode

Step1: Write 0x1 to the bit31 of **R_VM_CLK_REG(0x07010140 register)** to enable clock, write 0x1 to the bit24 of **R_VM_CLK_REG(0x07010140 register)** to select 24MHz clock source.
Step2: Write 0x1 to the bit16 of **R_THS_BGR_REG(0x0701015C register)** to dessert reset, write 0x1 to the bit0 of **R_THS_BGR_REG(0x0701015C register)** to open THS clock.
Step3: Write 0x2F to the bit[15:0] of **THS_CTRL** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL** to set ADC sample frequency divider.
Step5: Write 0x3A to the bit[31:12] of **THS_PER** to set THS work period.
Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.
Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.
Step8: Read THS efuse value from SID, then write the efuse value to **THS01_CDATA/THS23_CDATA** to calibrate

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THS0/THS1/THS2/TH3.

Step9: Write 0xF to the bit[3:0] 0f **THS_EN** to enable THS0/THS1/THS2/TH3.

Step10: Read the bit[3:0] of **THS_DATA_INTS**, if is 1, temperature conversion is complete.

Step11: Read the bit[11:0] of **THS0_DATA/THS1_DATA/THS2_DATA/THS3_DATA**, calculate THS0/THS1/THS2/THS3 temperature based on THS Temperature Conversion Formula in Section 3.11.3.4.

(2). Interrupt Mode

Step1: Write 0x1 to the bit31 of **R_VM_CLK_REG(0x07010140 register)** to enable clock, write 0x1 to the bit24 of **R_VM_CLK_REG(0x07010140 register)** to select 24MHz clock source.

Step2: Write 0x1 to the bit16 of **R_THS_BGR_REG(0x0701015C register)** to dessert reset, write 0x1 to the bit0 of **R_THS_BGR_REG(0x0701015C register)** to open THS clock.

Step3: Write 0x2F to the bit[15:0] of **THS_CTRL** to set ADC acquire time.

Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL** to set ADC sample frequency divider.

Step5: Write 0x3A to the bit[31:12] of **THS_PER** to set THS work period.

Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.

Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.

Step8: Read THS efuse value from SID, then write the efuse value to **THS01_CDATA/THS23_CDATA** to calibrate THS0/THS1/THS2/THS3.

Step9: Write 0xF to the bit[3:0] of **THS_DATA_INTC** to enable the interrupt of THS0/THS1/THS2/THS3.

Step10: Set GIC interface based on IRQ 185, write the bit[25] of the **0x03021120** register to 0x1.

Step11: Put interrupt handler address into interrupt vector table.

Step12: Write 0xF to the bit[3:0] 0f **THS_EN** to enable THS0/THS1/THS2/THS3.

Step13: Read the bit[3:0] of **THS_DATA_INTS**, if is 1, temperature conversion is complete.

Step14: Read the bit[11:0] of **THS0_DATA/THS1_DATA/THS2_DATA/THS3_DATA**, calculate THS0/THS1/THS2/THS3 temperature based on THS Temperature Conversion Formula in Section 3.11.3.4.

3.11.5. Register List

Module Name	Base Address
Thermal Sensor	0x07030400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register

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THS0_ALARM_CTRL	0x0040	THS0 Alarm Threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm Threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm Threshold Control Register
THS3_ALARM_CTRL	0x004C	THS3 Alarm Threshold Control Register
THS01_SHUTDOWN_CTRL	0x0080	THS0&1 Alarm Threshold Control Register
THS23_SHUTDOWN_CTRL	0x0084	THS2&3 Shutdown Threshold Control Register
THS01_CDATA	0x00A0	THS0&1 Calibration Data
THS23_CDATA	0x00A4	THS2&3 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register
THS3_DATA	0x00CC	THS3 Data Register

3.11.6. Register Description

3.11.6.1. THS Control Register(Default Value : 0x01DF_002F)

Offset: 0x0000			**Register Name: THS_CTRL**
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1DF	FS_DIV ADC Sample Frequency Divider CLK_IN/(N+1) , N > 0x17 The default value indicates 50 kHz.
15:0	R/W	0x2F	TACQ ADC Acquire Time CLK_IN/(n+1) The default value indicates 2us.

3.11.6.2. THS Enable Register(Default Value : 0x0000_0000)

Offset: 0x0004			**Register Name: THS_EN**
Bit	**Rear/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	THS3_EN Enable temperature measurement sensor3 0:Disable 1:Enable
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_EN

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			Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_EN Enable temperature measurement sensor0 0:Disable 1:Enable

3.11.6.3. THS Period Control Register(Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x3A	THERMAL_PER 4096*(n+1)/CLK_IN The default value indicates 10ms.
11:0	/	/	/

3.11.6.4. THS Data Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	THS3_DATA_IRQ_EN Selects temperature measurement data of sensor3 0:Disable 1:Enable
2	R/W	0x0	THS2_DATA_IRQ_EN Selects temperature measurement data of sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects temperature measurement data of sensor0 0:Disable 1:Enable

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3.11.6.5. THS Shut Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	SHUT_INT3_EN Selects shutdown interrupt for sensor3 0:Disable 1:Enable
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.11.6.6. THS Alarm Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS_ALARM_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ALARM_INT3_EN Selects alarm interrupt for sensor3 0:Disable 1:Enable
2	R/W	0x0	ALARM_INT2_EN Selects alarm interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects alarm interrupt for sensor0 0:Disable 1:Enable

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3.11.6.7. THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	THS3_DATA_IRQ_STS Data interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	THS2_DATA_IRQ_STS Data interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ_STS Data interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ_STS Data interrupt status for sensor0 Write '1' to clear this interrupt.

3.11.6.8. THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	SHUT_INT3_STS Shutdown interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt .

3.11.6.9. THS Alarm Off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS_ALARMO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	ALARM_OFF3_STS

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			Alarm interrupt off pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

3.11.6.10. THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	ALARM_INT3_STS Alarm interrupt pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

3.11.6.11. Median Filter Control Register(Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2

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			01: 4 10: 8 11: 16

3.11.6.12. THS0 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal Sensor0 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal Sensor0 alarm threshold for hysteresis temperature

3.11.6.13. THS1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal Sensor1 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal Sensor1 alarm threshold for hysteresis temperature

3.11.6.14. THS2 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: THS2_ALARM_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal Sensor2 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal Sensor2 alarm threshold for hysteresis temperature

3.11.6.15. THS3 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x004C	Register Name: THS3_ALARM_CTRL

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Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM3_T_HOT Thermal Sensor3 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM3_T_HYST Thermal Sensor3 alarm threshold for hysteresis temperature

3.11.6.16. THS0&1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: THS01_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal Sensor1 shutdown threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal Sensor0 shutdown threshold for hot temperature

3.11.6.17. THS2&3 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0084			Register Name: THS23_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
27:16	R/W	0x4E9	SHUT3_T_HOT Thermal Sensor3 shutdown threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal Sensor2 shutdown threshold for hot temperature

3.11.6.18. THS0&1 Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS01_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

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3.11.6.19. THS2&3 Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x00A4			Register Name: THS23_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
27:16	R/W	0x800	THS3_CDATA Thermal Sensor3 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

3.11.6.20. THS0 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

3.11.6.21. THS1 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

3.11.6.22. THS2 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: THS2_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

3.11.6.23. THS3 Data Register(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: THS3_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/

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11:0	R	0x0	THS3_DATA Temperature measurement data of sensor3

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3.12. PSI

3.12.1. Overview

PSI（Peripheral System Interconnect）is a peripheral bus interconnect device based on AHB and APB protocol, which supports 16 AHB master and 16 slave bus. The type of slave bus can be AHB bus or APB bus. Each bus supports 64 slave devices.

3.12.2. Block Diagram

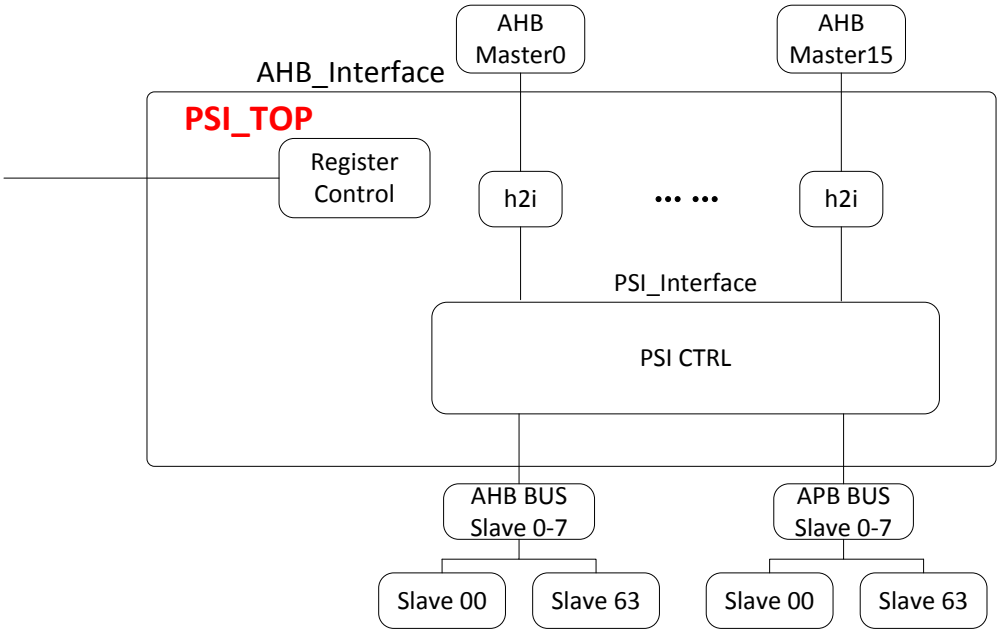

Figure 3- 35. PSI Block Diagram

For complete PSI information, refer to the ***Allwinner T7 PSI Specification***.

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3.13. Message Box

3.13.1. Overview

The Message Box(MSGBOX) provides interrupt communication mechanism for on-chip processor.

The MSGBOX has the following features:

- Eight message queues
- Each of queues could be configured as transmitter or receiver for user
- FIFO depth is 4 x 32 bits
- The communication parties are CPUS and CPUX
- The communication parties transmit information through channel
- Message reception and queue-not-full notification interrupt mechanism

3.13.2. Block Diagram

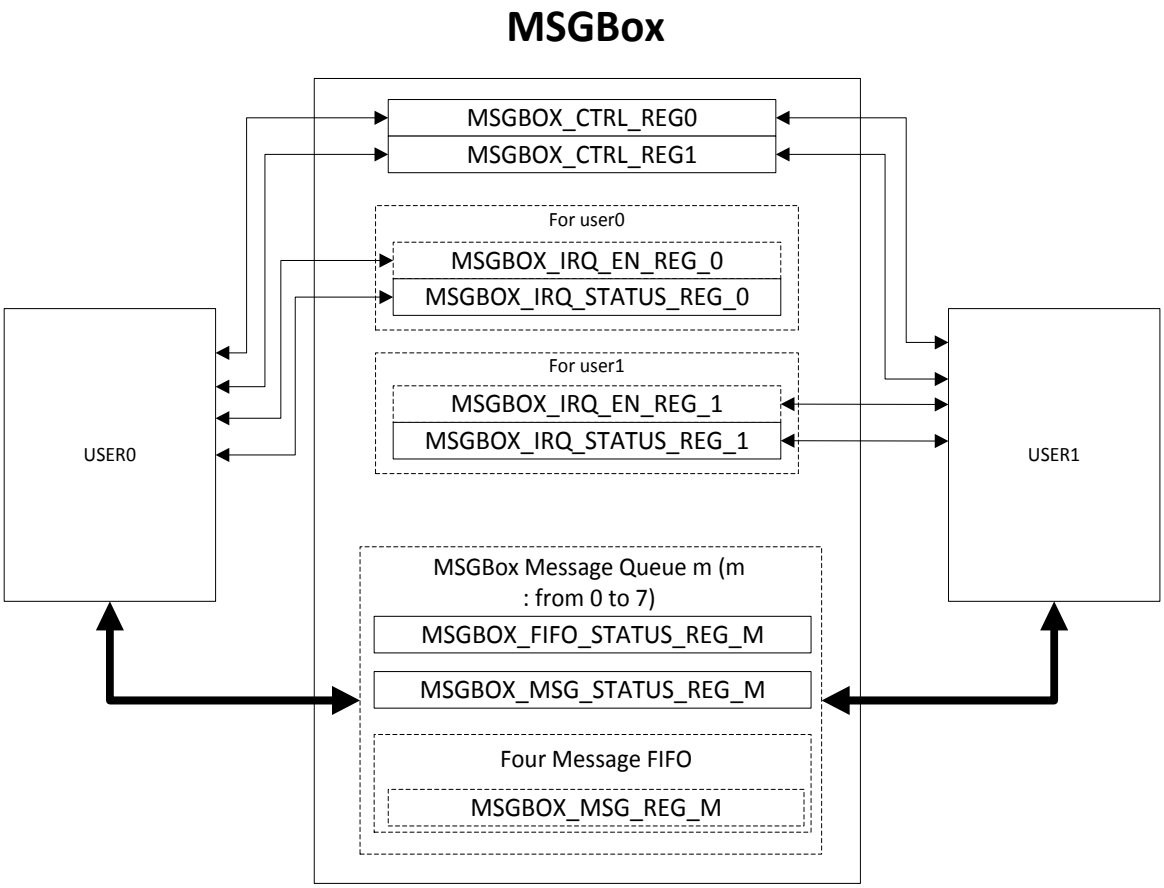

Figure 3- 36. Message Box Block Diagram

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Message Box supports a set of registers for a processor to establish an interconnection channel with the others. The processor determines message queue numbers for interconnection and the used queues to be transmitter or receiver for itself and the interconnectible one. Every queue has a **MSGBox FIFO Status Register** for processor to check out queue FIFO full status and a **MSGBox Message Status Register** for processor to check out message numbers in queue FIFO. Otherwise, every queue has a corresponding IRQ status bit and a corresponding IRQ enable bit, which are used for requesting an interrupt.

3.13.3. Operations and Functional Descriptions

3.13.3.1. Clock and Reset

MSGBOX is on AHB1 bus. To access MSGBOX, perform the following steps about AHB1 bus:
Step1: De-assert MSGBOX reset signal.
Step2: Open MSGBOX gating signal.

3.13.3.2. Typical Application

Two different CPU can build communication by configuring MSGBOX. The communication parties have 8 bidirectional channels. If a party is receiver, then another is transmitter. During communication process, the current status can be judged through interrupt or FIFO status.

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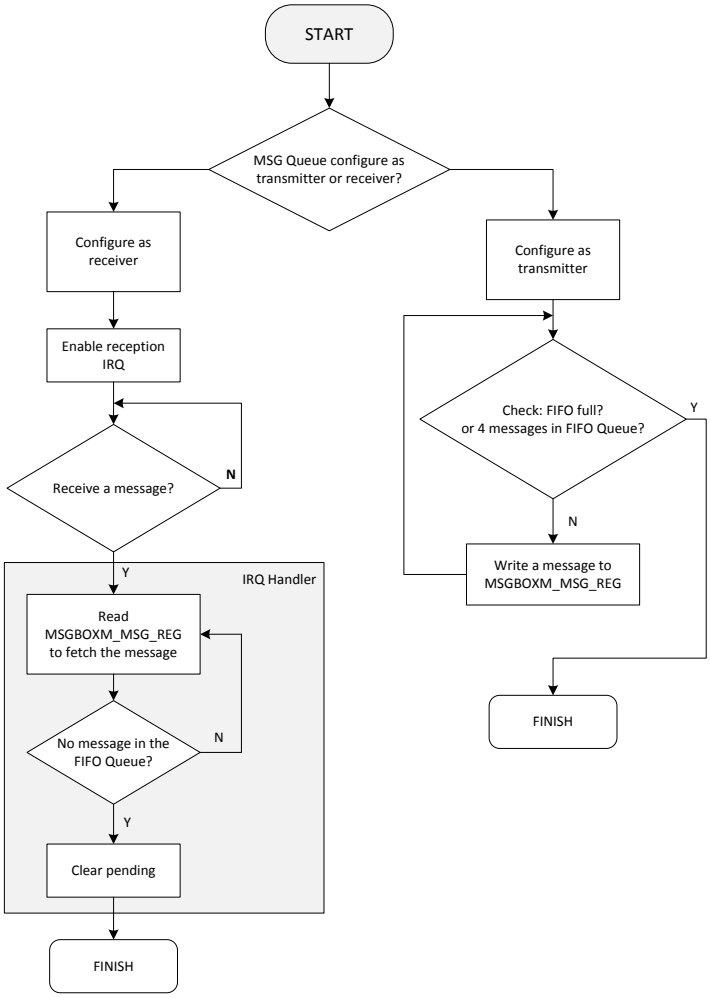

Figure 3- 37. Message Box Typical Application Chart

3.13.3.3. Message Queue Assignment

When a processor needs to transmit or receive a message from the other one, it should configure the Message Queue assignment for the other one and itself. **MSGBOX_CTRL_REG0** and **MSGBOX_CTRL_REG1** hold the eight Message Queues assignment. For an instance, The **RECEPTION_MQ0** bit is set to 0 and the **TRANSMIT_MQ0** bit is set to 1, that means, user1 transmits messages and user0 receives them. Or the **RECEPTION_MQ0** bit and the **TRANSMIT_MQ0** bit are both set to 0, which means user0 transmits messages to itself.

3.13.3.4. Interrupt Request

Message Box provides message reception and queue-not-full notification interrupt mechanism. When a message queue is configured as transmitter for a user, this queue transmit pending bit will always be set to 1 for this user if it is not full. When a message queue is configured as receiver for a user, this queue reception pending bit will be set to 1 for this user only if it receives a new message. For example, message queue0 is configured as a transmitter for user0 and a receiver for user1. If message queue0 is not full always, then TRANSMIT_MQ0_IRQ_PEND bit is set to 1. If TRANSMIT_MQ0_IRQ_EN is set to 1, user0 will request a queue-not-full interrupt. When message queue0 has received

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a new message, RECEPTION_MQ0_IRQ_PEND would be set to 1 and user1 will request a new message reception interrupt if **RECEPTION_MQ0_IRQ_EN** is set to 1. **MSGBox IRQ Status Register u***(u=0,1)* hold the IRQ status for user0 and user1. **MSGBox IRQ Enable Register u***(u=0,1)* determines whether the user could request the interrupt or not.

3.13.3.5. Transmit and Receive Messages

Every message queue has a couple of private registers for query: **MSGBox Message Status Register** , **MSGBox FIFO Status Register** , and **MSGBox Message Queue Register**.

MSGBox Message Status Register records present message number in the message queue.

MSGBox FIFO Status Register indicates whether the message queue is full obviously.

MSGBox Message Queue Register stores the next to be read message of the message FIFO queue or the message to be written into the queue FIFO. If queue is not full usually ,it indicates that you could write messages into the queue FIFO ,if there is one or more message in the queue FIFO, it indicates that you could read messages from the queue FIFO.

Writing a message into the queue FIFO realizes a transmission and reading a message makes a reception ture. You could transmit messages by writing messages to **MSGBox Message Queue Register** continuously or receive messages by reading **MSGBox Message Queue Register** continuously. The continuous writing or reading operation means it's no need to make a delay between operations.

3.13.3.6. Operating Mode

3.13.3.6.1. Transfer Mode Configuration

- Queue n (n=0~3)transmitter mode: Write 1 to the bit[8*n+4] of **MSGBOX_CTRL_REG0**.
- Queue m (m=4~7)transmitter mode : Write 1 to the bit[8*(m-4)+4] of **MSGBOX_CTRL_REG1**.
- Queue n (n=0~3) receiver mode: Write 1 to the bit[8*n] of **MSGBOX_CTRL_REG0**.
- Queue m (m=4~7) receiver mode : Write 1 to the bit[8*(m-4)] of **MSGBOX_CTRL_REG1**.

3.13.3.6.2. Interrupt Check Transfer Status

(1) Configure transmitter and receiver mode through **chapter 3.13.3.6.1. Transfer Mode Configuration**.
(2) Interrupt enable bit: Configure the interrupt enable bit of transmitter/receiver through **MSGBOX_IRQ_EN_REG**.
(3) When FIFO is not full, an interrupt pending generates to remind the transmitter to transmit data, at this time, to write data to FIFO in interrupt handler ,and clear the pending bit and the enable bit of *Transmitter IRQ*.
(4) When FIFO has new data, an interrupt pending generates to remind the receiver to receive data, at this time, to read data from FIFO in interrupt handler, and clear the pending bit and the enable bit of *Receiver IRQ*.

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3.13.3.6.3. FIFO Check Transfer Status

(1) Configure transmitter and receiver mode through **chapter 3.13.3.6.1. Transfer Mode Configuration**.
(2) When FIFO is not full, the transmitter fills FIFO to 4*32 bits.
(3) When the receiver considers FIFO is full, then the receiver reads FIFO data, and reads **MSGBOXM_MSG_STATUS_REG** to require the current FIFO number.

3.13.3.6.4. Debug

To use MSGBOX in debug mode, performs the following steps:
(1) Write 1 to the bit0 of **MSGBOX_DEBUG_REG**.
(2) The control bit of the corresponding channel is set to 1.

3.13.4. Programming Guidelines

Example: User1 as transmitter of MQ0123 (MQ:Message Queue) and as receiver of MQ4567, User0 as receiver of MQ0123 and as transmitter of MQ4567.

The working process of user1 and user0 is as follows.

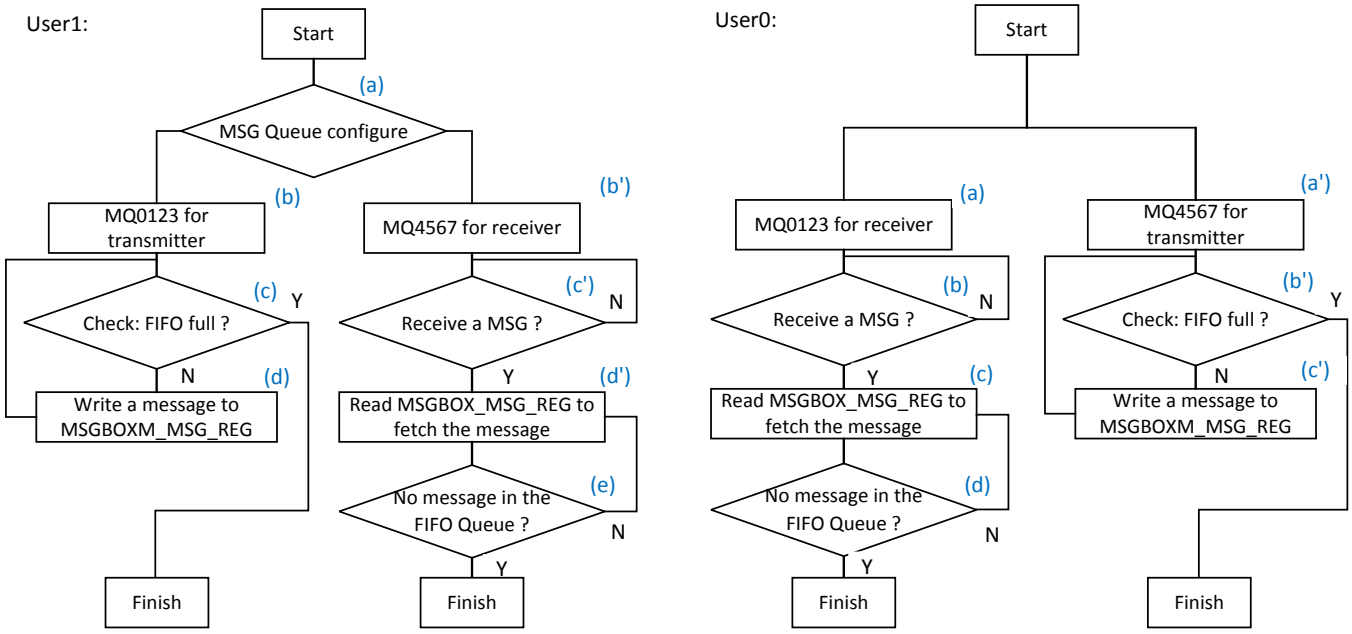

Figure 3- 38. User1 and User0 Working Process

User1:
(a) The user1 is as the transmitter of MQ0123 and as the receiver of MQ4567.
(b) Queue n (n=0~3) transmitter mode: write 1 to the bit[8*n+4] of MSGBOX_CTRL_REG0.

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(b') Queue m (m=4~7) receiver mode: write 1 to the bit[8*(m-4)] of MSGBOX_CTRL_REG1.
(c) Check whether the FIFO is full by the status of MSGBOXM_FIFO_STATUS_REG. If the FIFO is full, the program finish, otherwise, go to step (d).
(c') Check whether to receive a message by the status of MSGBOXM_MSG_STATUS_REG. If you donot receive, then continue to wait, otherwise, go to step (d').
(d) Write a message to MSGBOXM_MSG_REG.
(d') Read MSGBOX_MSG_REG to fetch the message.
(e) If there is no message in FIFO Queue, step up to (d'), otherwise, the program finish.

User0:
(a) The user0 is as the receiver of MQ0123.
(a') The user0 is as the transmitter of MQ4567.
(b) Check whether to receive a message by the status of MSGBOXM_MSG_STATUS_REG. If you donot receive, then continue to wait, otherwise, go to step (c).
(b') Check whether the FIFO is full by the status of MSGBOXM_FIFO_STATUS_REG. If the FIFO is full, the program finish, otherwise, step up to (c').
(c) Read MSGB OX_MSG_REG to fetch the message.
(c') Write a message to MSGBOXM_MSG_REG.
(d) If there is no message in FIFO Queue, go to step (c), otherwise, the program finish.

3.13.5. Register List

Module Name	Base Address
MSGBOX	0x03003000

Register Name	Offset	Description
MSGBOX_CTRL_REG0	0x0000	Message Queue Attribute Control Register 0
MSGBOX_CTRL_REG1	0x0004	Message Queue Attribute Control Register 1
MSGBOXU_IRQ_EN_REG	0x0040+n*0x20	IRQ Enable for User n (n=0,1)
MSGBOXU_IRQ_STATUS_REG	0x0050+n*0x20	IRQ Status for User n (n=0,1)
MSGBOXM_FIFO_STATUS_REG	0x0100+N*0x04	FIFO Status for Message Queue N(N = 0~7)
MSGBOXM_MSG_STATUS_REG	0x0140+N*0x04	Message Status for Message Queue N(N=0~7)
MSGBOXM_MSG_REG	0x0180+N*0x04	Message Register for Message Queue N(N=0~7)
MSGBOX_DEBUG_REG	0x01C0	MSGBOX Debug Register

3.13.6. Register Description

3.13.6.1. MSGBox Control Register 0(Default Value: 0x1010_1010)

Offset: 0x0000			Register Name: MSGBOX_CTRL_REG0
Bit	Read/Write	Default/Hex	Description

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31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ3 Message Queue 3 is a transmitter of user u 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ3 Message Queue 3 is a receiver of user u 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ2 Message Queue 2 is a transmitter of user u 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ2 Message Queue 2 is a receiver of user u 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ1 Message Queue 1 is a transmitter of user u 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ1 Message Queue 1 is a receiver of user u 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ0 Message Queue 0 is a transmitter of user u 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ0 Message Queue 0 is a receiver of user u 0: user0 1: user1

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3.13.6.2. MSGBox Control Register 1(Default Value: 0x1010_1010)

Offset: 0x0004			Register Name: MSGBOX_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	TRANSMIT_MQ7 Message Queue 7 is a transmitter of user u 0: user0 1: user1
27:25	/	/	/
24	R/W	0x0	RECEPTION_MQ7 Message Queue 7 is a receiver of user u 0: user0 1: user1
23:21	/	/	/
20	R/W	0x1	TRANSMIT_MQ6 Message Queue 6 is a transmitter of user u 0: user0 1: user1
19:17	/	/	/
16	R/W	0x0	RECEPTION_MQ6 Message Queue 6 is a receiver of user u 0: user0 1: user1
15:13	/	/	/
12	R/W	0x1	TRANSMIT_MQ5 Message Queue 5 is a transmitter of user u 0: user0 1: user1
11:9	/	/	/
8	R/W	0x0	RECEPTION_MQ5 Message Queue 5 is a receiver of user u 0: user0 1: user1
7:5	/	/	/
4	R/W	0x1	TRANSMIT_MQ4 Message Queue 4 is a transmitter of user u 0: user0 1: user1
3:1	/	/	/
0	R/W	0x0	RECEPTION_MQ4 Message Queue 4 is a receiver of user u 0: user0 1: user1

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3.13.6.3. MSGBox IRQ Enable Register u(Default Value: 0x0000_0000)

Offset:0x0040+N*0x20(N=0,1)			Register Name: MSGBOX_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	TRANSMIT_MQ7_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 is not full.)
14	R/W	0x0	RECEPTION_MQ7_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 7 has received a new message.)
13	R/W	0x0	TRANSMIT_MQ6_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 is not full.)
12	R/W	0x0	RECEPTION_MQ6_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 6 has received a new message.)
11	R/W	0x0	TRANSMIT_MQ5_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 is not full.)
10	R/W	0x0	RECEPTION_MQ5_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 5 has received a new message.)
9	R/W	0x0	TRANSMIT_MQ4_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 is not full.)
8	R/W	0x0	RECEPTION_MQ4_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 4 has received a new message.)
7	R/W	0x0	TRANSMIT_MQ3_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 3 is not full.)
6	R/W	0x0	RECEPTION_MQ3_IRQ_EN 0: Disable

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			1: Enable (It will notify user u by interrupt when Message Queue 3 has received a new message.)
5	R/W	0x0	TRANSMIT_MQ2_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 is not full.)
4	R/W	0x0	RECEPTION_MQ2_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 2 has received a new message.)
3	R/W	0x0	TRANSMIT_MQ1_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 is not full.)
2	R/W	0x0	RECEPTION_MQ1_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 1 has received a new message.)
1	R/W	0x0	TRANSMIT_MQ0_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 is not full.)
0	R/W	0x0	RECEPTION_MQ0_IRQ_EN 0: Disable 1: Enable (It will notify user u by interrupt when Message Queue 0 has received a new message.)

3.13.6.4. MSGBox IRQ Status Register u(Default Value: 0x0000_AAAA)

Offset:0x0050+N*0x20(N=0,1)			**Register Name: MSGBOXU_IRQ_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W1C	0x1	TRANSMIT_MQ7_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 is not full. Setting 1 to this bit will clear it.
14	R/W1C	0x0	RECEPTION_MQ7_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 7 has received a new message. Setting 1 to this bit will clear it.
13	R/W1C	0x1	TRANSMIT_MQ6_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 is not full. Setting 1 to this bit will clear it.

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12	R/W1C	0x0	RECEPTION_MQ6_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 6 has received a new message. Setting 1 to this bit will clear it.
11	R/W1C	0x1	TRANSMIT_MQ5_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 is not full. Setting 1 to this bit will clear it.
10	R/W1C	0x0	RECEPTION_MQ5_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 5 has received a new message. Setting 1 to this bit will clear it.
9	R/W1C	0x1	TRANSMIT_MQ4_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 is not full. Set 1 to this bit will clear it.
8	R/W1C	0x0	RECEPTION_MQ4_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 4 has received a new message. Setting 1 to this bit will clear it.
7	R/W1C	0x1	TRANSMIT_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 is not full. Setting 1 to this bit will clear it.
6	R/W1C	0x0	RECEPTION_MQ3_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 3 has received a new message. Setting 1 to this bit will clear it.
5	R/W1C	0x1	TRANSMIT_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 is not full. Setting 1 to this bit will clear it.
4	R/W1C	0x0	RECEPTION_MQ2_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 2 has received a new message. Setting 1 to this bit will clear it.
3	R/W1C	0x1	TRANSMIT_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 is not full. Setting 1 to this bit will clear it.
2	R/W1C	0x0	RECEPTION_MQ1_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 1 has received a new message. Setting 1 to this bit will clear it.
1	R/W1C	0x1	TRANSMIT_MQ0_IRQ_PEND

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			0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 is not full. Setting 1 to this bit will clear it.
0	R/W1C	0x0	RECEPTION_MQ0_IRQ_PEND 0: No effect 1: Pending. This bit will be pending for user u when Message Queue 0 has received a new message. Setting 1 to this bit will clear it.

3.13.6.5. MSGBox FIFO Status Register m(Default Value: 0x0000_0000)

Offset:0x0100+N*0x04 (N=0~7)			Register Name: MSGBOXM_FIFO_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	FIFO_FULL_FLAG 0: The Message FIFO queue is not full (space is available) 1: The Message FIFO queue is full. This FIFO status register has the status related to the message queue.

3.13.6.6. MSGBox Message Status Register m(Default Value: 0x0000_0000)

Offset:0x0140+N*0x04 (N=0~7)			Register Name: MSGBOXM_MSG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	MSG_NUM Number of unread messages in the message queue. Here, limited to four messages per message queue. 000: There is no message in the message FIFO queue. 001: There is 1 message in the message FIFO queue. 010: There are 2 messages in the message FIFO queue. 011: There are 3 messages in the message FIFO queue. 100: There are 4 messages in the message FIFO queue. 101~111:/

3.13.6.7. MSGBox Message Queue Register m(Default Value: 0x0000_0000)

Offset:0x0180+N*0x04 (N=0~7)			Register Name: MSGBOXM_MSG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	The message register stores the next to be read message of the message FIFO queue. Reads remove the message from the FIFO queue.

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3.13.6.8. MSGBox Debug Register(Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: MSGBOX_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	FIFO_CTRL MQ[7:0] Control. In the debug mode, the corresponding FIFO channel will disable and only one register space valid for a message exchange. 0: Normal Mode 1: Disable the corresponding FIFO (Clear FIFO)
7:1	/	/	/
0	R/W	0x0	DEBUG_MODE In the debug mode, each user can transmit messages to itself through each message queue. 0: Normal Mode 1: Debug Mode

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3.14. Spinlock

3.14.1. Overview

In multi-core system,the Spinlock offers hardware synchronization mechanism, lock operation can prevent multi processors from handling data-sharing at the same time, and ensure coherence of data.

The Spinlock has the following features:

- Spinlock module includes 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable(less than 200 cycles)

3.14.2. Block Diagram

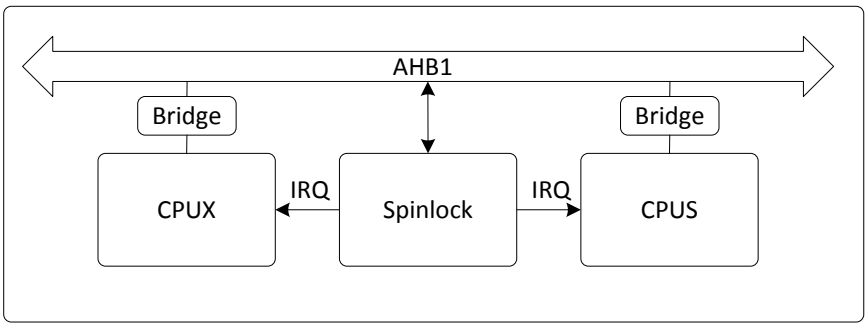

Figure 3- 39. Spinlock Block Diagram

3.14.3. Operations and Functional Descriptions

3.14.3.1. Clock and Reset

The Spinlock is hung on AHB1. Before accessing Spinlock register, open the corresponding gating bit on AHB1 and de-assert reset signal. The correct operation order is to de-assert reset signal at first, and then open the corresponding gating signal.

3.14.3.2. Typical Application

A processor lock spinlock0, when the status is locked, the processor executes specific code, and then unlocks code. Other processors is released to start reading/writing operation.

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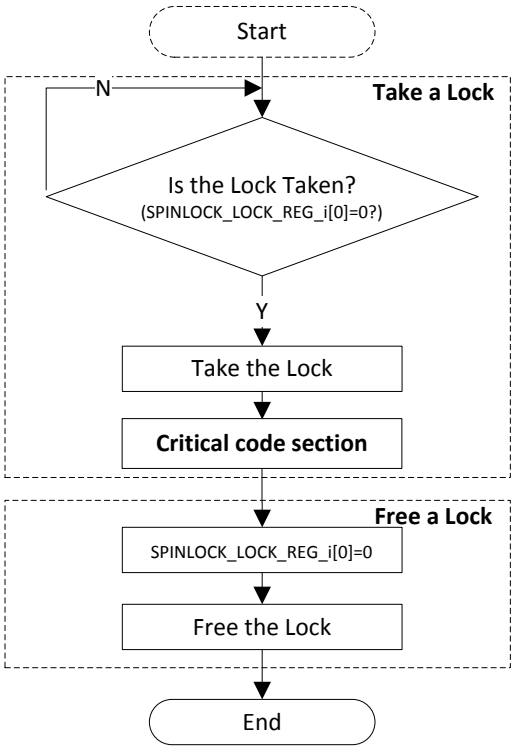

Figure 3- 40. Spinlock Typical Application Diagram

3.14.3.3. Function Implemention

3.14.3.3.1. Spinlock State Machine

When a processor uses spinlock, it needs to acquire spinlock's status through **SPINLOCK_STATUS_REG**.

Reading operation: when the return value is 0, spinlock comes into locked status; when read this status bit again, the return value is 1, spinlock comes into locked status.

Writing operation: when the Spinlock is in locked status, the Spinlock can convert to unlocked status through writing 0. After reset, the Spinlock is in unlocked status by default.

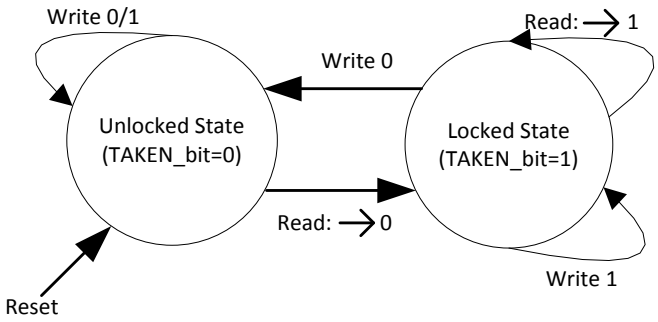

Figure 3- 41. Spinlock State Machine

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3.14.3.3.2. Take and Free Spinlock

Checking out **SpinLock Register Status** is necessary when a processor would like to take a spinlock. This register stores all 32 lock registers' status: TAKEN or NOT TAKEN(free).

In order to request to take a spinlock, a processor has to do a read-access to the corresponding lock register. If lock register returns 0, the processor takes this spinlock. And if lock register returns 1, the processor must retry.

Writing 0 to a lock register frees the corresponding spinlock. If the lock register is not taken, write-access has no effect. For a taken spinlock, every processor has the privilege to free this spinlock. But it is suggested that the processor which has taken the spinlock free it for strictness.

3.14.3.4. Operating Mode

3.14.3.4.1. Switch Status

(1) When the read value from **SPINLOCKN_LOCK_REG** is 0,the Spinlock come into locked status.
(2) Execute application code, the status of **SPINLOCKN_STATUS_REG** is 1.
(3) Write 0 to **SPINLOCKN_LOCK_REG**, the Spinlock comes into unlocked status, corresponding spinlock is released.

3.14.4. Programming Guidelines

Take CPU0's synchronization with CPUS with Spinlock0 for an example, CPU0 takes the spinlock0 firstly in the instance.

To taking/freeing spinlock0, CPU0 and CPUS perform the following steps:

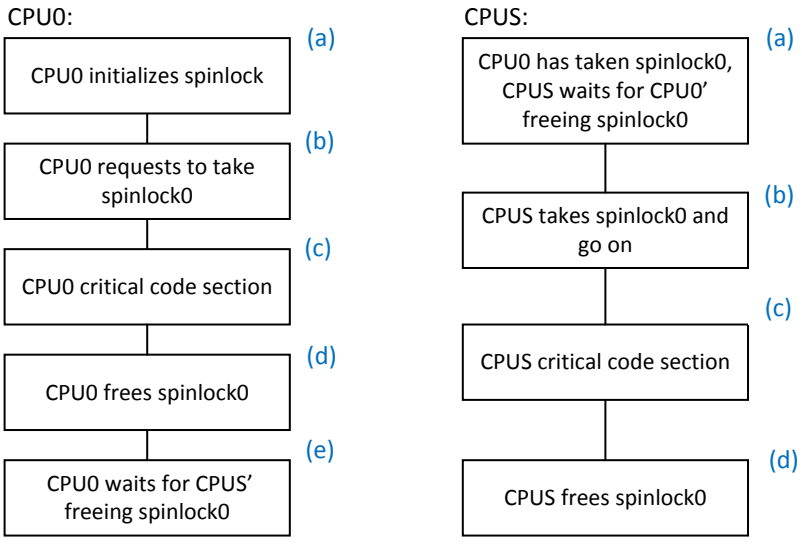

Figure 3- 42. CPU0 and CPUS Taking/Freeing Spinlock0 Process

CPU0:

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(a) The CPU0 initializes Spinlock.
(b) Firstly, check lock register0(SPINLOCK_STATUS_REG0) status, if it is taken, check till CPU0 frees spinlock0. Then request to take spinlock0, if fail, retry till lock register0 is taken.
(c) Execute CPU0 critical code.
(d) After executing CPU0 critical code, the CPU0 frees spinlock0.
(e) The CPU0 waits for CPUS' freeing spinlock0.

CPUS:

(a) If the CPU0 has taken spinlock0, the CPUS waits for CPU0' freeing spinlock0.
(b) The CPUS requests to take spinlock0, if fail, retry till lock register0 is taken.
(c) Execute CPUS critical code.
(d) After executing CPUS critical code, the CPUS frees spinlock0.

The following codes are for reference.

```
----------------------------------------------------------------------CPU0 of Cluster0----------------------------------------------------------------------
Step 1: CPU0 initializes Spinlock
        put_wvalue(SPINLOCK_BGR_REG,0x00010000);
        put_wvalue(SPINLOCK_BGR_REG,0x00010001);
Step 2: CPU0 requests to take spinlock0
        rdata=readl(SPINLOCK_STATUS_REG0);                  //Check lock register0 status
        if(rdata != 0)    writel (0, SPINLOCK_LOCK_REG0);   //If it is taken, check till CPU0 frees spinlock0
        rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
        if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  //If fail, retry till lock register0 is taken
  ---------- CPU0 critical code section ----------
Step 3: CPU0 free spinlock0
        writel (0, SPINLOCK_LOCK_REG0);                     //CPU0 frees spinlock0
Step 4: CPU0 waits for CPUS' freeing spinlock0
        writel (readl(SPINLOCK_STATUS_REG0) == 1);          //CPU0 waits for CPUS' freeing spinlock0

------------------------------------------------------------------------CPUS----------------------------------------------------------------------
Step 1: CPU0 has taken spinlock0, CPUS waits for CPU0' freeing spinlock0
        while(readl(SPINLOCK_STATUS_REG0) == 1);            //CPUS waits for CPU0' freeing spinlock0
  Step 2: CPUS takes spinlock0 and go on
        rdata=readl(SPINLOCK_LOCK_REG0);                    //Request to take spinlock0
        if(rdata != 0)    rdata=readl(SPINLOCK_LOCK_REG0);  //If fail, retry till lock register0 is taken
---------- CPUS critical code section ----------
Step 3: CPUS frees spinlock0
        writel (0, SPINLOCK_LOCK_REG0);                     //CPUS frees spinlock0
```

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3.14.5. Register List

Module Name	Base Address
Spinlock	0x03004000

Register Name	Offset	Description
SPINLOCK_SYSTATUS_REG	0x0000	Spinlock System Status Register
SPINLOCK_STATUS_REG	0x0010	Spinlock Status Register
SPINLOCK_LOCK_REGN	0x0100+N*0x04	Spinlock Register N (N=0~31)

3.14.6. Register Description

3.14.6.1. Spinlock System Status Register (Default Value: 0x1000_0000)

Offset: 0x0000			Register Name: SPINLOCK_SYSTATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R	0x1	LOCKS_NUM Number of lock registers implemented 00: This instance has 32 lock registers. 01: This instance has 64 lock registers. 10: This instance has 128 lock registers. 11: This instance has 256 lock registers.
27:9	/	/	/
8	R	0x0	IU0 In-Use flag0, covering lock register0-31 0: All lock register 0-31 are in the NotTaken state. 1: At least one of the lock register 0-31 is in the Taken state.
7:0	/	/	/

3.14.6.2. Spinlock Register Status(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPINLOCK_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
[i] (i=0~31)	R	0x0	LOCK_REG_STATUS SpinLock[i] status (i=0~31) 0: The Spinlock is free 1: The Spinlock is taken

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3.14.6.3. Spinlock Register N (N=0 to 31)(Default Value: 0x0000_0000)

Offset:0x0100+N*0x04 (N=0~31)			Register Name: SPINLOCKN_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TAKEN Lock State Read 0x0: The lock was previously Not Taken (free).The requester is granted the lock. Write 0x0: Set the lock to Not Taken (free). Read 0x1: The lock was previously Taken. The requester is not granted the lock and must retry. Write 0x1: No update to the lock value.

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Chapter 4 Video and Graphics

4.1. DE

The Display Engine(DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 4-1.

The DE has the following features:

- Output size up to 2048x2048
- Four alpha blending channels for main display,two channels for aux display
- Four overlay layers in each channel, and has a independent scaler
- Potter-duff compatible blending operation
- Input format: YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports write back for high efficient dual display and miracast

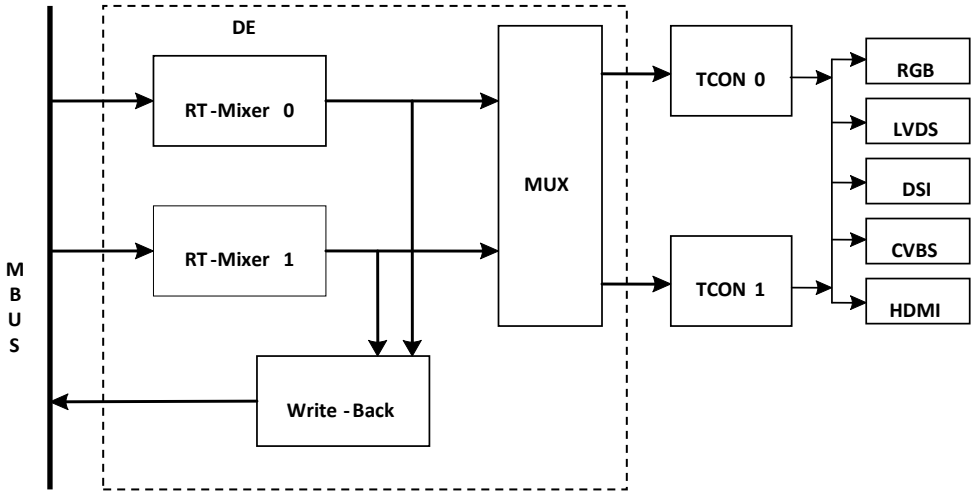

Figure 4- 1. DE Block Diagram

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For complete DE information, refer to the ***Allwinner T7 DE Specification***.

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4.2. De-interlacer

The De-interlacer(DI) is a module which provides de-interlacing functions.

The DI has the following features:

- Off-line processing mode
- Supports NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined data format
- Input video resolution from 32 x 32 to 2048 x 2048 pixel
- Supports weave/pixel-motion-adaptive de-interlacer method
- Noise reduction function

For complete DI information, refer to the ***Allwinner T7 DI Specification***.

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4.3. G2D

The Graphic 2D(G2D) Engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Layer size up to 2048 x 2048 pixels
- Supports pre-multiply alpha image data
- Color key
- Two pipes porter-duff alpha blending
- Input/output format: YUV422(interleaved, semi-planar and planar format)/YUV420(semi-planar and planar format)/YUV411(semi-planar and planar format)/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports memory scan order option
- Multiple formats convert function
- 1/16x to 32x resize ratio
- 32-phase 8-tap horizontal anti-alias filter, 32-phase 4-tape vertical anti-alias filter
- Window clip
- FillRectangle, BitBlit,StretchBlit and MaskBlit
- Horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

For complete G2D information, refer to the ***Allwinner T7 G2D Specification***.

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4.4. Video Encoder

The Video Encoder consists of the video encoding unit and JPEG encoder. The video encoding unit supports H.264 and H.265 encoding, and JPEG encoder supports JPEG/MJPEG encoding.

4.4.1. Video Encoding Unit

4.4.1.1. Overview

The video encoding unit is a CODEC that supports H.264 and H.265 protocol by using hardware. It features high compressing rate, low CPU usage, short delay and low power consumption.

The video encoding unit has the following features:

- Supports ITU-T H.265 main profile@level 4.1 main-tier encoding
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Single reference frame
  - Three prediction unit (PU) types of 32x32, 16x16 and 8x8 for inter-prediction
  - Four prediction unit types of 32x32, 16x16, 8x8 and 4x4 for intra-prediction
  - Skip mode and Merge mode with a maximum of two candidates processing to be merged
  - Four transform unit (TU) types of 32x32, 16x16, 8x8 and 4x4
  - CABAC entropy encoding
  - De-blocking filtering
  - Sample adaptive offset (SAO)
- Supports ITU-T H.264 high profile/main profile/baseline profile@level 4.2 encoding
  - Encoding of multiple slice
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Single reference frame
  - Four prediction unit (PU) types of 16x16,16x8,8x16 and 8x8 for inter-prediction
  - Three prediction unit types of Intra16x16, Intra8x8 and Intra4x4 for intra-prediction
  - Trans4x4 and trans8x8
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
- Supports Classify, MB-RateControl, Syclic-Intra-Refresh, Dynamic-ME, Inter-Only-in-P-Frame, Intra-4x4-Disable in general function
- Supports the output picture format of semi-planar YCbCr4:2:0
- Supports configurable picture resolutions
  - Minimum picture resolution: 192x96
  - Maximum picture resolution: 4096x4096
  - Step of the picture width or height: 2
- Supports region of interest (ROI) encoding
  - Maximum of 8 ROIs
  - Independent enable/disable control for the encoding function of each ROI

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- Supports on-screen display (OSD) encoding protection that can be enabled or disabled
- Supports OSD front-end overlaying
  - OSD overlaying before encoding for a maximum of 8 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP
- Supports the output bit rate ranging from 2 kbit/s to 100 Mbit/s
- Supports Frame Buffer Compression

4.4.1.2. Block Diagram

The functional block diagram of the video encoding unit is as follows.

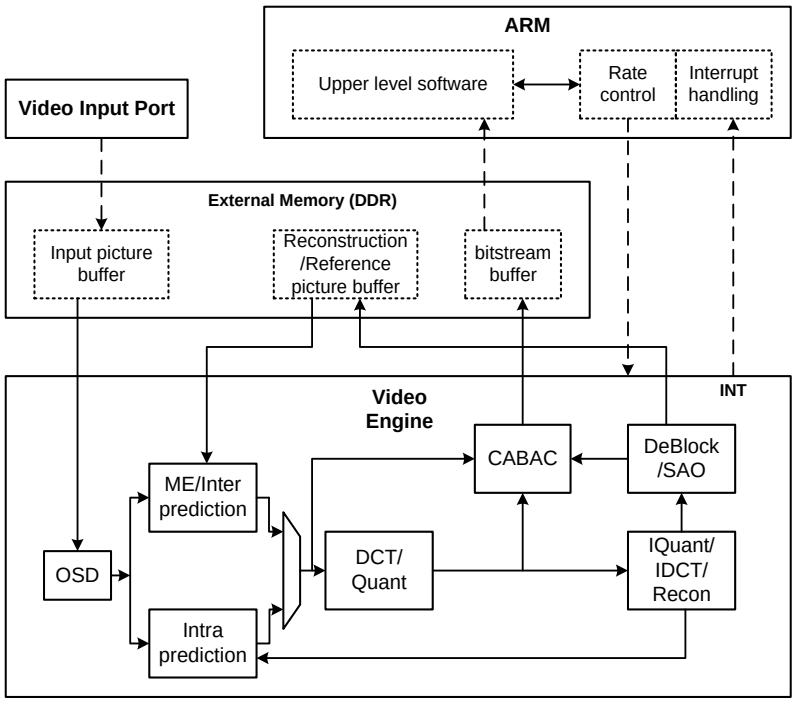

Figure 4- 2. Video Encoding Unit Block Diagram

Based on related protocols and algorithms, the video encoding unit supports motion estimation/inter-prediction, intra-prediction, transform/quantization, inverse transform/inverse quantization, CABAC encoding/stream generation and DeBlock/SAO. The ARM software controls the bitrate and handles interrupt.

Before the encoding is enabled, software allocates three types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The video encoding unit reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the Video Input Port module.

- **Reconstruction/Reference picture buffer**

  The video encoding unit writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames, reference pictures are read from this buffer.

- **Stream buffer**

  This buffer stores encoded streams. The video encoding unit writes streams to this buffer during encoding. This

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buffer is read by software.

4.4.2. JPEG Encoder

4.4.2.1. Overview

The JPEG encoder is a high-performance hardware encoder. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPEG encoder has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0, YCbCr4:2:2 and YCbCr4:4:4
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Semi-planar YCbCr4:4:4
- Supports JPEG encoding with the performance of 1080p@60fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192x96
  - Maximum picture resolution: 8192x8192
- Supports the picture width or height step of 8
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlapping
  - OSD overlaying before encoding for a maximum of 8 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports the color-to-gray function
- Supports the MJPEG output bit rate ranging from 2 kbit/s to 100 Mbit/s

4.4.2.2. Block Diagram

The functional block diagram of the JPEG encoder is as follows.

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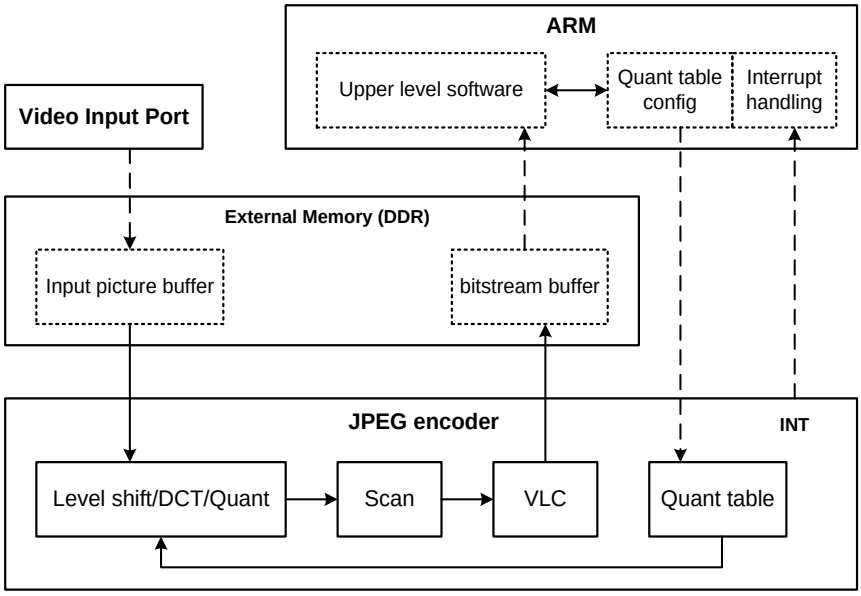

Figure 4- 3. JPEG Encoder Block Diagram

Based on the protocols that require a large number of operands, the JPEG encoder supports OSD, level shift, DCT, quantization, scanning, VLC encoding and stream generation. The ARM software configures quantization tables and handles interrupt.

Before the JPEG encoder is enabled, the software allocates two types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The JPEG encoder reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the Video Input Port module.

- **Stream buffer**

  This buffer stores encoded streams. The JPEG encoder writes streams to this buffer during encoding. This buffer is read by software.

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4.5. Video Decoder

4.5.1. Overview

The Video Decoder consists of Video Control Firmware(VCF) running on ARM processor and embedded hardware Video Engine(VE). VCF gets the bitstream from topper software, parses bitstream, invokes the Video Engine, and generates the decoding image sequence. The decoder image sequence is transmitted by the video output controller to the display device under the control of the topper software.

The Video Decoder has the following features:

- Supports ITU-T H.265 Main Profile@Level 4.1
  - Maximum video resolution: 4096 x 2048
  - Maximum decoding rate: 60Mbit/s, 1080p@60fps
- Supports ITU-T H.264 Base/Main/High Profile@Level 4.2
  - Maximum video resolution: 4096 x 2048
  - Maximum decoding rate: 60Mbit/s, 1080p@45fps
- Supports ITU-T H.263 Base Profile
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 100Mbit/s, 1080p@45fps
- Supports VP8
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 40Mbit/s, 1080p@45fps
- Supports MPEG4 SP/ASP L5
  - Maximum video resolution: 3840 x 2160
  - Maximum decoding rate: 100Mbit/s, 1080p@45fps
- Supports MPEG2 MP/HL
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 100Mbit/s, 1080p@45fps
- Supports MPEG1 MP/HL
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 100Mbit/s, 1080p@45fps
- Supports VC1 SP/MP/AP
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 100Mbit/s, 1080p@30fps
- Supports xvid
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 100Mbit/s, 1080p@45fps
- Supports Sorenson Spark
  - Maximum video resolution: 1920 x 1080
  - Maximum decoding rate: 100Mbit/s, 1080p@45fps
- Supports AVS/AVS+ JiZhun
  - Maximum video resolution: 1920 x 1080

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- Maximum decoding rate: 30Mbit/s, 1080p@45fps

• Supports JPEG HFIF file format
  - Maximum video resolution: 16384 x 16384
  - Maximum decoding rate: 45MPPS

4.5.2. Block Diagram

The functional block diagram of the Video Decoder is as follows.

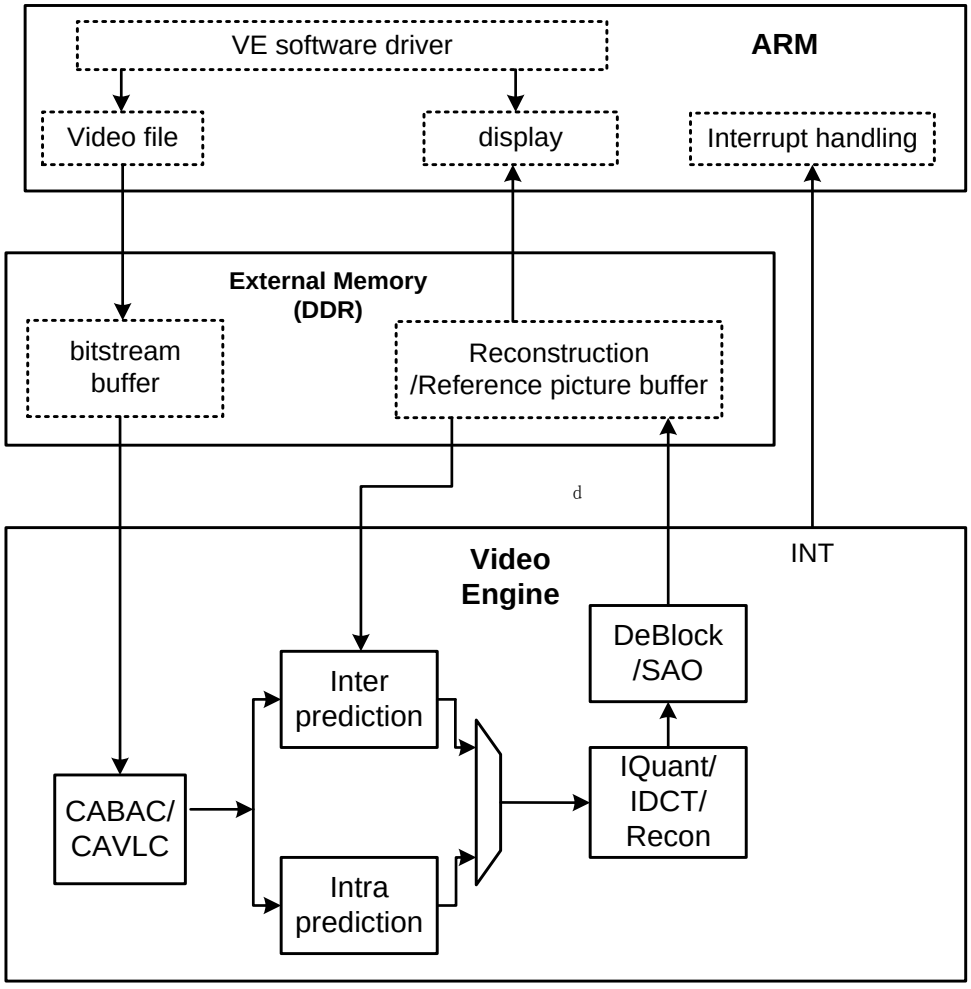

Figure 4- 4. Video Decoder Block Diagram

The Video Engine software driver parses the video file into the corresponding standard video stream, and configures the DDR address of the saved video stream, the DDR address of the reference picture, the DDR address of the reconstructed frame and other necessary information to Video Engine, and starts decoding.

The process of Video Decoder includes reading video stream and parsing syntax, intra-frame prediction, inter-frame prediction, inverse quantization, inverse transform, de-blocking filter, and finally writing the decoded picture into DDR. After the interrupt of Video Decoder, Video Decoder sends the picture in DDR to the display module.

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Chapter 5 Memory

5.1. SDRAM Controller(DRAMC)

5.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to the industy-standard DDR3/ DDR3L SDRAM and Low Power DDR2/DDR3 SDRAM. It supports up to a 24G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register setting.

The DRAMC has the following features:

- Compatible with JEDEC standard DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- 32-bit bus width
- Two chip selects
- Different memory device's power voltage of 1.5V, 1.2V
- Clock frequency up to 800MHz for DDR3/DDR3L
- Clock frequency up to 672MHz for LPDDR3
- Clock frequency up to 533MHz for LPDDR2
- Memory capacity up to 24G bits (3G bytes)
- Supports 16 address lines and 3 bank address lines
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be changed for different application(MDFS supported)
- Supports controller clock on/off by hardware automatically
- Auto self-refresh entry(ASRE)/Exit(ASRX)
- Clock pad enable/disable hardware automatically support when ASRE/ASRX
- Priority of transferring through multiple ports is programmable
- Random read or write operation is supported

For complete DRAMC information, refer to the ***Allwinner T7 DRAMC Specification***.

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5.2. NAND Flash Controller(NDFC)

5.2.1. Overview

The NDFC is the NAND Flash Controller which supports all NAND flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 80 bits error per 1024 bytes data. The on chip ECC and parity checking circuit of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. There are three different kinds of modes for serial read access, mode0 is for conventional serial access , mode1 is for EDO type and the mode2 is for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NDFC has the following features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Configure randomize engine seed by using software
- Software configure method for various system and memory types
- Supports 2 chip selects, and 2 ready_busy signals
- Up to 8-bit data bus width
- Supports 1024, 2048, 4096, 8192, 16384, 32768 bytes size per page
- Conventional and EDO serial access method for serial reading Flash
- 80 bits/1 KB On-the-fly BCH code ECC check and error correction
- Output bits number information about corrected error
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its registers, and interrupt is supported
- One Command FIFO
- Internal DMA controller based on chain-structured descriptor list
- Two 256x32-bit RAM for Pipeline Procession
- Supports SDR, ONFI DDR1.0 , Toggle DDR1.0, ONFI DDR2.0 and Toggle DDR2.0 RAW NAND FLASH
- Maximum IO rate of 50MHz in SDR mode, and 60MHz in both DDR1.0 and DDR2.0 mode
- Self-debug for NDFC debug

5.2.2. Block Diagram

The block diagram of the NDFC is shown as follows.

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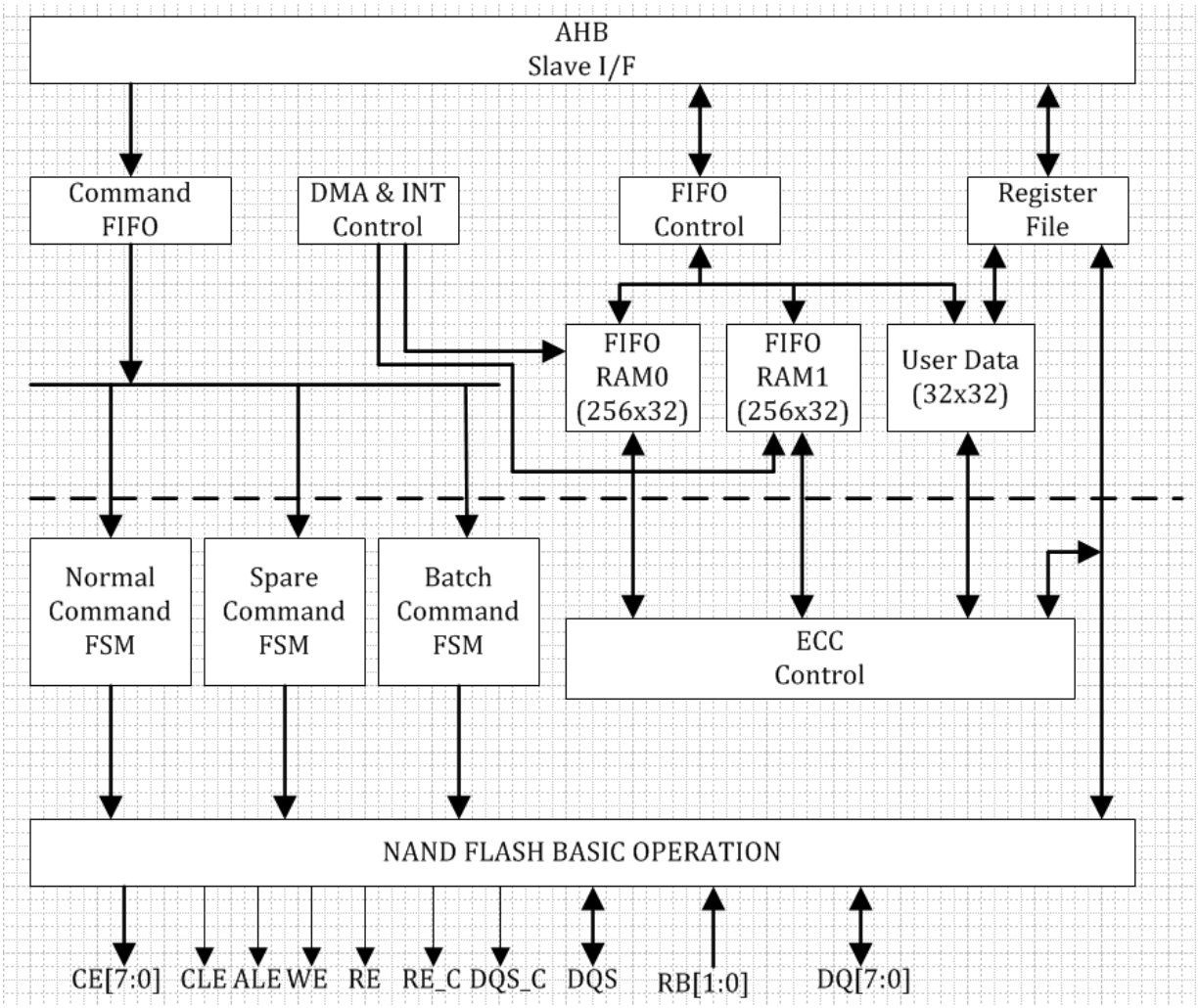

Figure 5- 1. NDFC Block Diagram

5.2.3. Operations and Functional Descriptions

5.2.3.1. External Signals

Table 5-1 describes the external signals of NDFC. DQ0~DQ7 and DQS are bidirectional I/O. WE,ALE,CLE,CE,RE are output pin, RB is input pin. The RB pin in the NAND device is an open-drain driver, which must need a pull-up resistor.

Table 5- 1. NDFC External Signals

Signal	Description	Type
NAND_WE	Write Enable	O
NAND_RE	Read Enable	O
NAND_ALE	Address Latch Enable, High is Active	O
NAND_CLE	Command Latch Enable, High is Active	O
NAND_CE0	Chip Enable, Low is Active	O
NAND_CE1	Chip Enable, Low is Active	O

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NAND_RB0	Ready/Busy, Low is Active	I
NAND_RB1	Ready/Busy, Low is Active	I
NAND_DQ0	Data Input / Output	I/O
NAND_DQ1	Data Input / Output	I/O
NAND_DQ2	Data Input / Output	I/O
NAND_DQ3	Data Input / Output	I/O
NAND_DQ4	Data Input / Output	I/O
NAND_DQ5	Data Input / Output	I/O
NAND_DQ6	Data Input / Output	I/O
NAND_DQ7	Data Input / Output	I/O
NAND_DQS	Data Strobe	I/O

5.2.3.2. Clock Sources

To ensure ECC efficiency,ECC engine and NDFC internal logic use different clock. The clock of NDFC internal logic is set by **NAND Clock0 Register**, the clock of ECC engine is set by **NAND Clock1 Register** .Note that **NAND Clock0 Register** set the internal logic clock of NDFC, but the frequency of external Nand Flash device is half of NDFC internal logic clock. That is, if external Nand Flash runs at 40MHz, then NDFC need set to 80MHz.

Both ECC engine and NDFC internal logic have five different clock sources. Users can select one of them to make ECC engine or internal logic clock source. Table 5-2 describles the clock sources of NDFC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 5- 2. NDFC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1.2GHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1.2GHz

5.2.3.3. Timing Diagram

Typically, there are two kinds of serial access methods. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.

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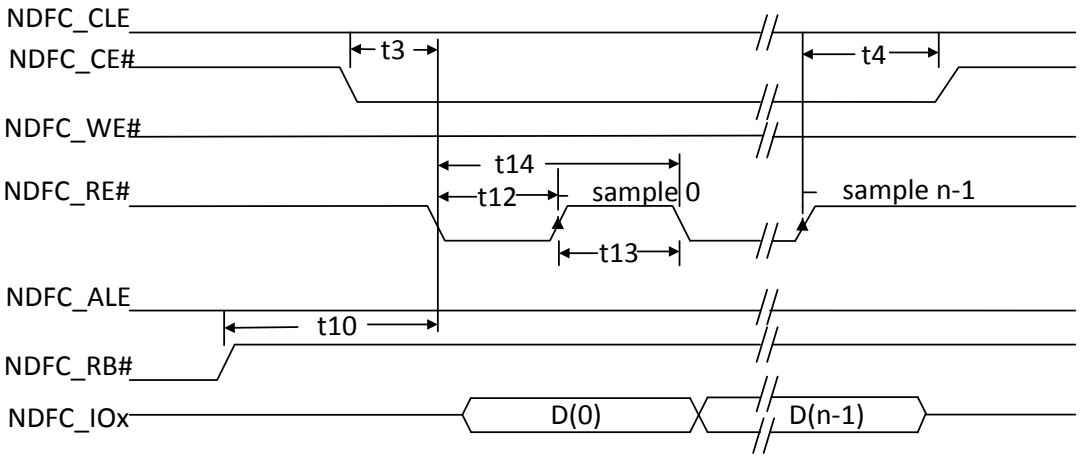

Figure 5- 2. Conventional Serial Access Cycle Diagram (SAM0)

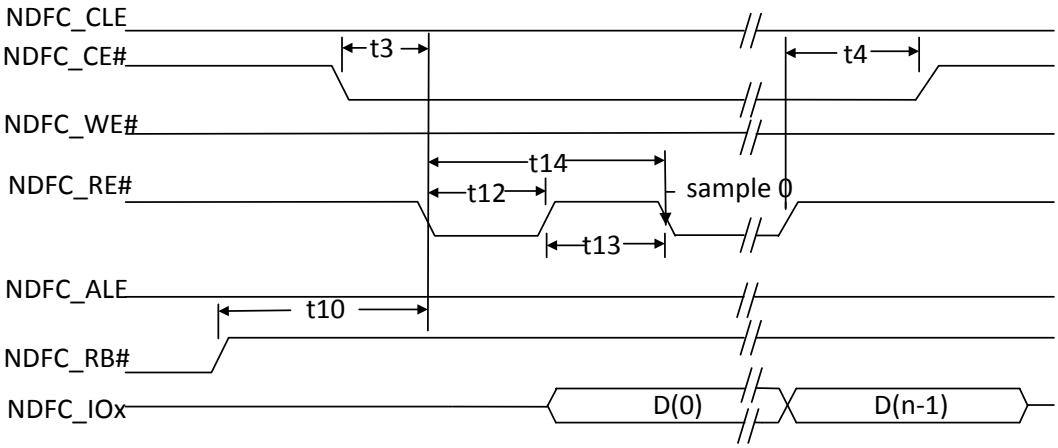

Figure 5- 3. EDO Type Serial Access after Read Cycle (SAM1)

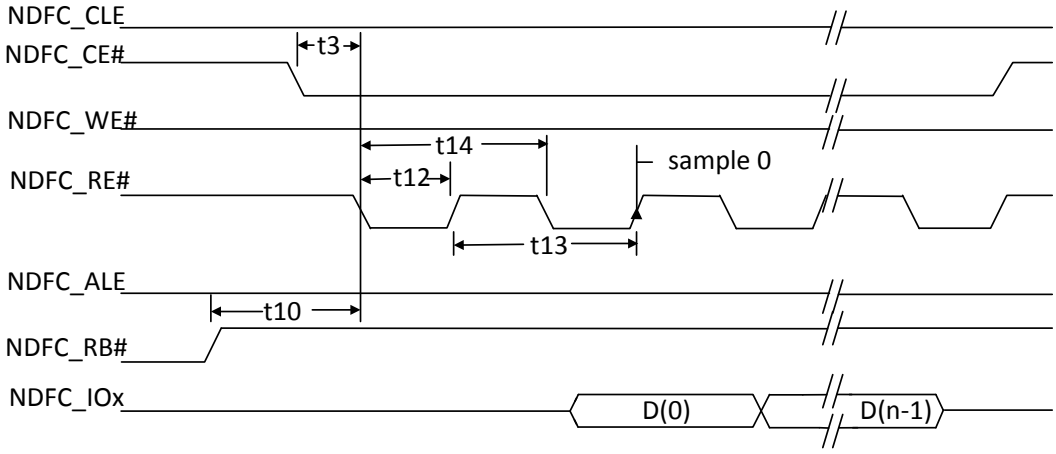

Figure 5- 4. Extending EDO Type Serial Access Mode (SAM2)

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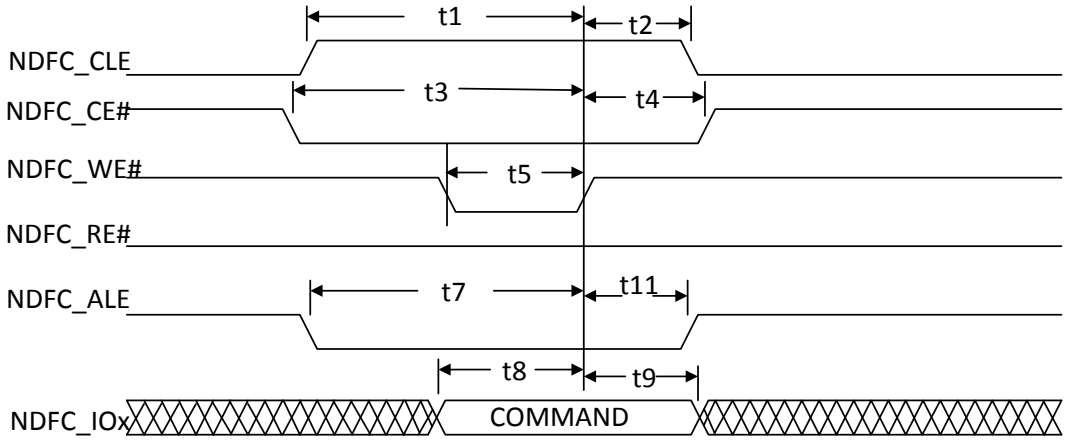

Figure 5- 5. Command Latch Cycle

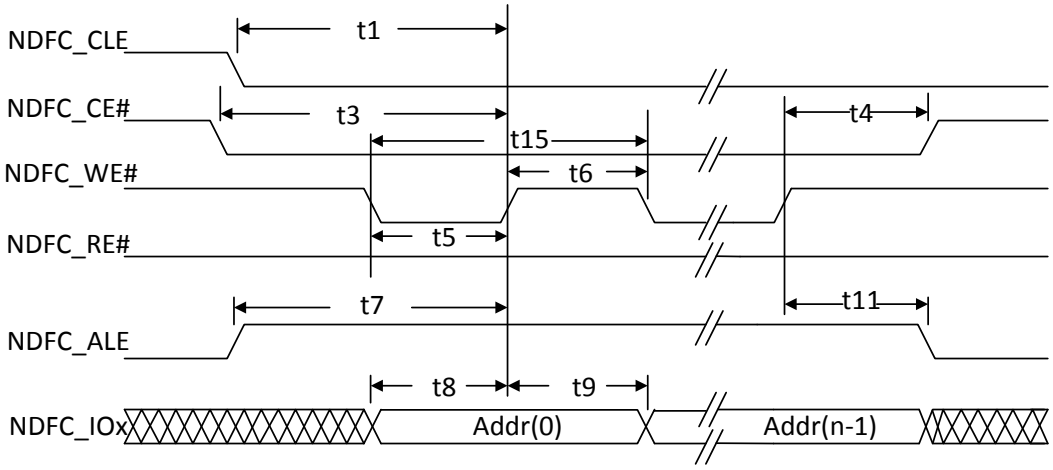

Figure 5- 6. Address Latch Cycle

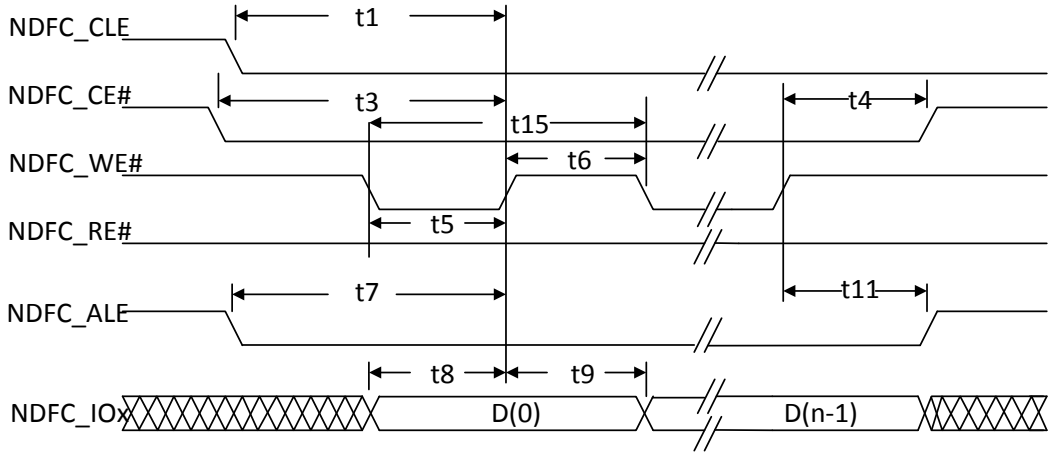

Figure 5- 7. Write Data to Flash Cycle

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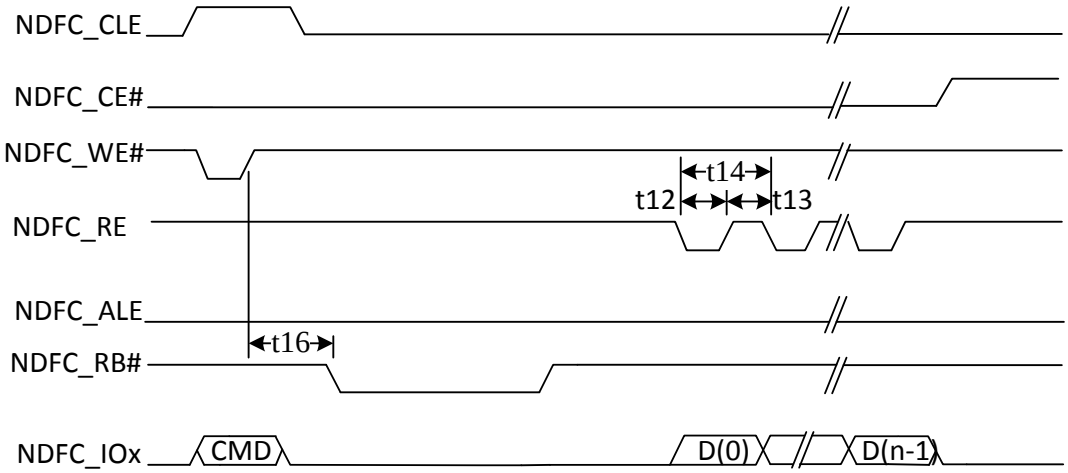

Figure 5- 8. Waiting R/B# Ready Diagram

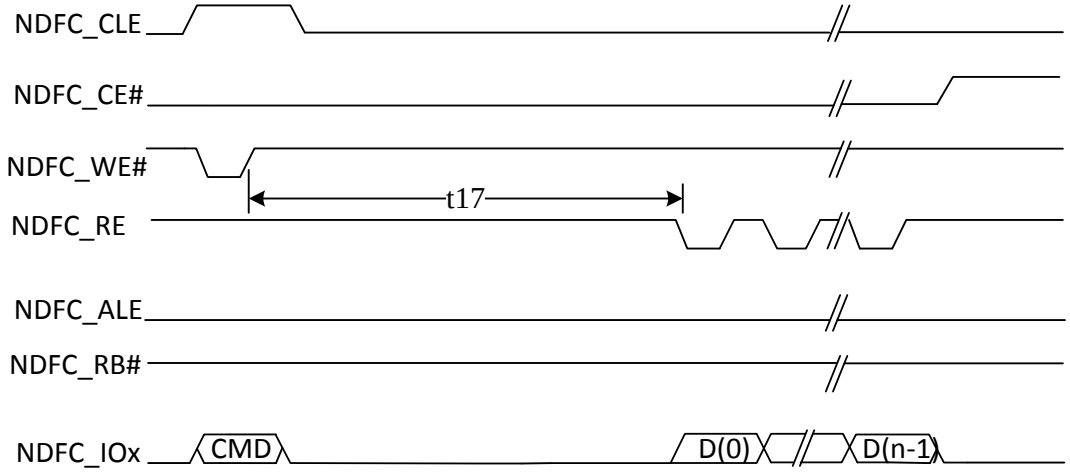

Figure 5- 9. WE# High to RE# Low Timing Diagram

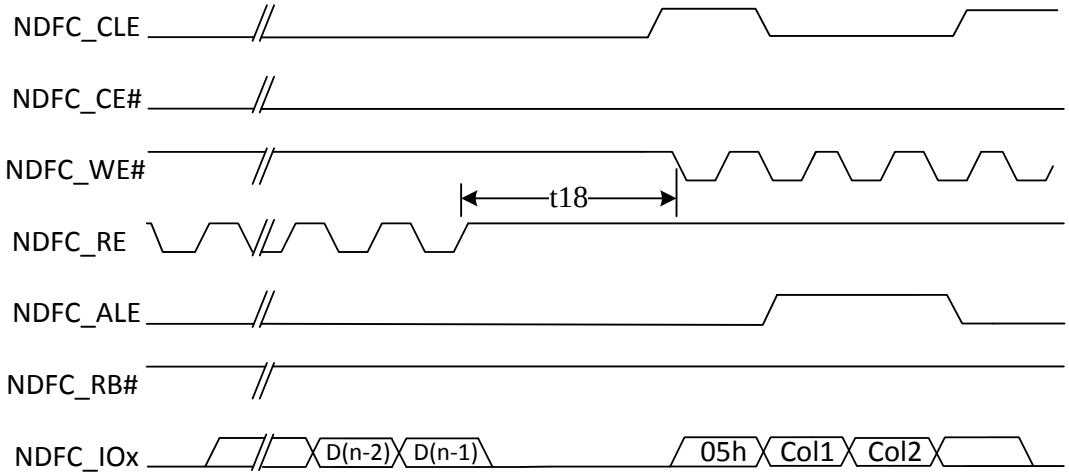

Figure 5- 10. RE# High to WE# Low Timing Diagram

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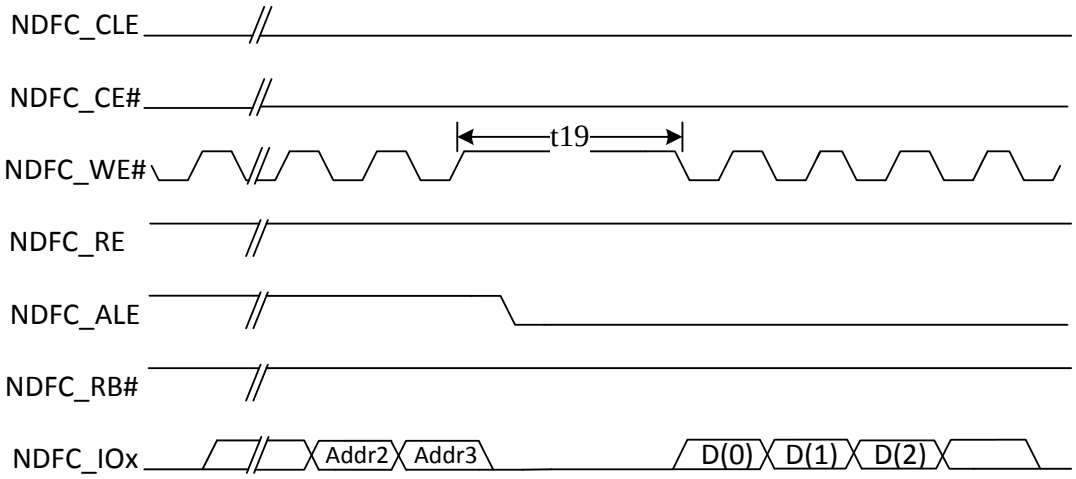

Figure 5- 11. Address to Data Loading Timing Diagram

Timing cycle list:

ID	Parameter	Timing	Notes
t1	NDFC_CLE setup time	2T	
t2	NDFC_CLE hold time	2T	
t3	NDFC_CE setup time	2T	
t4	NDFC_CE hold time	2T	
t5	NDFC_WE# pulse width	T(1)	
t6	NDFC_WE# hold time	T	
t7	NDFC_ALE setup time	2T	
t8	Data setup time	T	
t9	Data hold time	T	
t10	Ready to NDFC_RE# low	3T	
t11	NDFC_ALE hold time	2T	
t12	NDFC_RE# pulse width	T	
t13	NDFC_RE# hold time	T	
t14	Read cycle time	2T	
t15	Write cycle time	2T	
t16	NDFC_WE# high to R/B# busy	T_WB(2)	Specified by timing configure register (NDFC_TIMING_CFG)
t17	NDFC_WE# high to NDFC_RE# low	T_WHR(3)	Specified by timing configure register (NDFC_TIMING_CFG)
t18	NDFC_RE# high to NDFC_WE# low	T_RHW(4)	Specified by timing configure register (NDFC_TIMING_CFG)
t19	Address to Data Loading time	T_ADL(5)	Specified by timing configure register (NDFC_TIMING_CFG)

Note(1): T is the cycle of the internal clock.

Note(2),(3),(4),(5): These values are configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.

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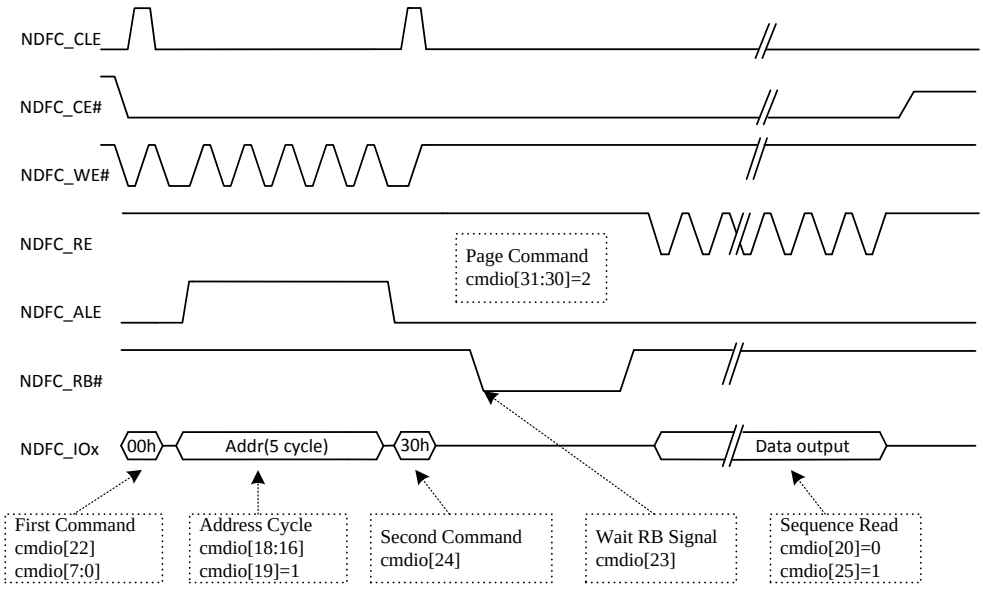

Figure 5- 12. Page Read Command Diagram

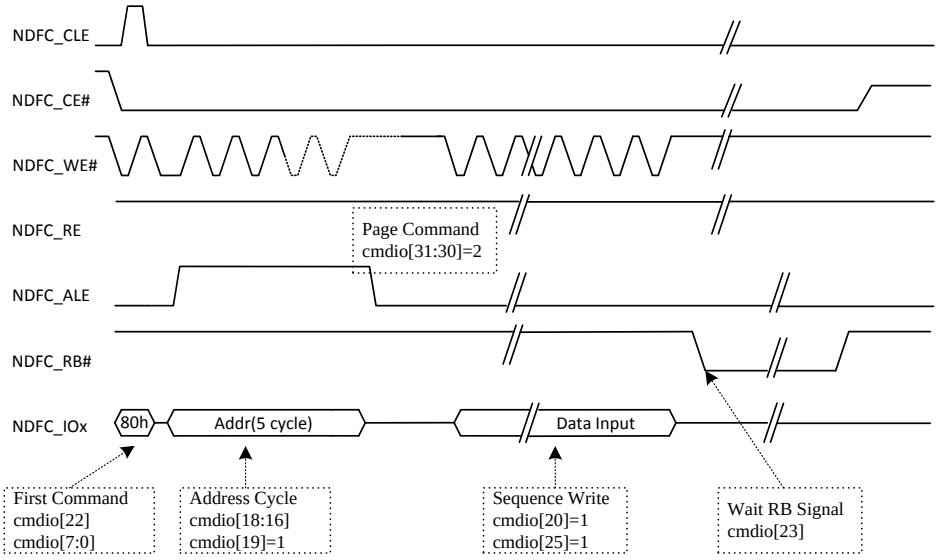

Figure 5- 13. Page Program Diagram

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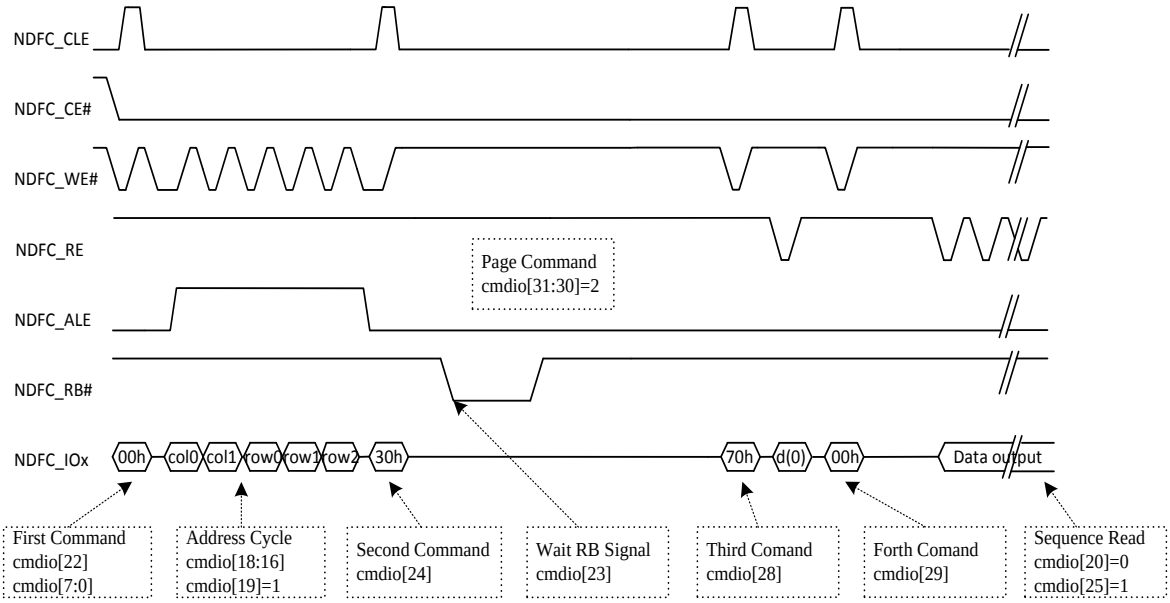

Figure 5- 14. EF-NAND Page Read Diagram

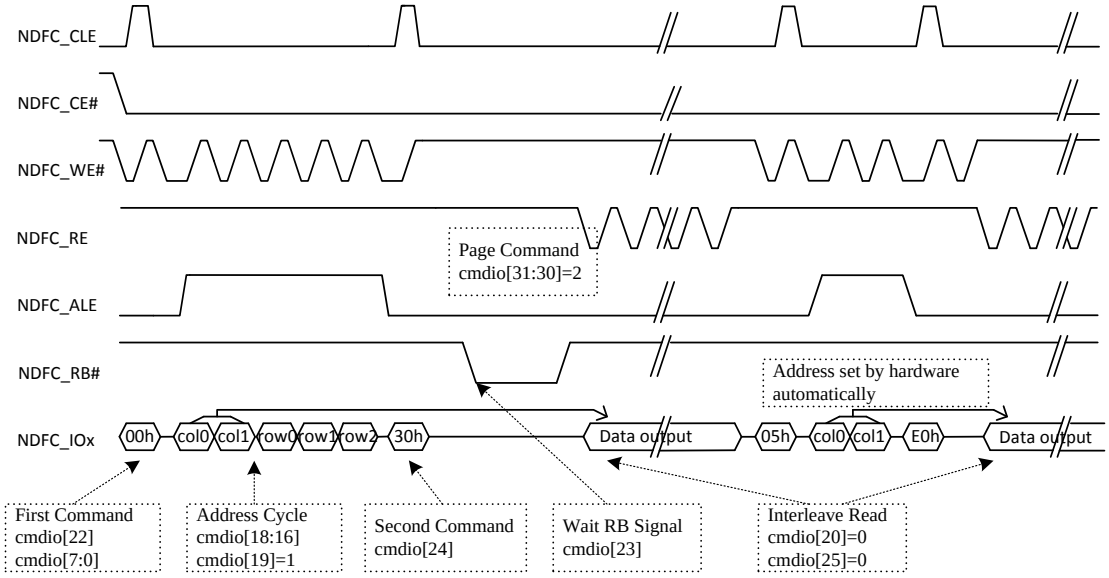

Figure 5- 15. Interleave Page Read Diagram

5.2.3.4. Internal DMA Controller Descriptors

5.2.3.4.1. Descriptor Structure

The internal DMA controller of the NDFC can transfer data between DMA FIFO in NDFC and DMA buffer in host memory using DMA descriptors. DMA descriptors in the host memory with chain structure is shown in Figure 5-16.

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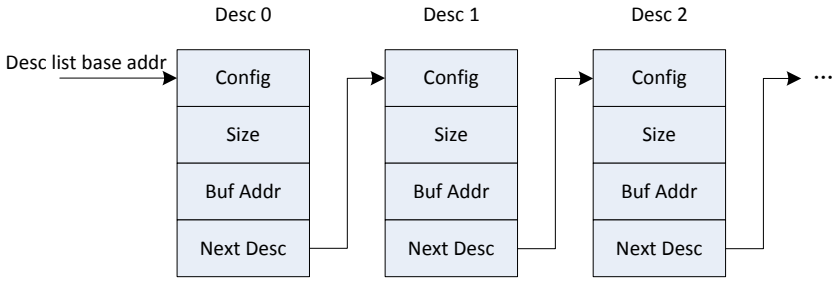

Figure 5- 16. Internal DMA Descriptor Chain Structure

The start address of DMA descriptor list must be word (32-bit) aligned, and will be configured to **NDFC DMA Descriptor List Base Address Register**. Each DMA descriptor consists of four words(32-bit).

5.2.3.4.2. Descriptor Definition

Config	
Bit	**Description**
31:4	/
3	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first descriptor.
2	LAST_FLAG When set, this bit indicates that the buffers pointed by this descriptor are the last data buffer.
1:0	/

Size	
Bit	**Description**
31:16	/
15:0	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 8 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

Buff Addr	
Bit	**Description**
31:0	BUFF_ADDR These bits indicate the physical address of DMA data buffer in host memory. The buffer address must be 4 bytes aligned.

Next Description	
Bit	**Description**
31:0	NEXT_DESC_ADDR These bits indicate the pointer to the physical host memory of the next descriptor is present.

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5.2.3.5. NDFC Data Block Mask Register

ECC_DATA_BLOCK is written or read through the value of **NDFC Data Block Mask Register**.But in real application scenario, capacity can not possibly waste, so writing operation does not use the function,only reading operation uses. In reading operation, we divides Sequence mode and Interleave mode through the store position of user_data.
Sequence mode: The user_data of every 1K main area data and ECC encoder data are next to main area data.
Interleave mode: All user_data and ECC encoder data are stored from page_size position.

When any **ECC_DATA_BLOCK** within page is read through batch command(**NDFC_CMD_TYPE** in 0x24 register is 0x10), the register is used differently for Sequence mode and Interleave mode.

Sequence mode can only support continue **ECC_DATA_BLOCK**,the register value can only be 0x1,0x3,0x7,etc.But Interleave mode has not limit.

Whether Sequence mode or Interleave mode, the first reading **ECC_DATA_BLOCK** is used to calculate corresponding column address, and column address is written to 0x14 and 0x18 register.

5.2.3.6. NDFC Enhanced Feature Register

The bit[24] and bit[23:16] of the register are used to judge whether free space need be padded random data except valid data when batch command function is used.

Take a SanDisk chip(SDTNQGAMA-008G) as an example:
Refer to the specification of the SanDisk chip, the page_size of the SanDisk chip is (16384+1280) bytes, but BCH level uses 40bit/1K, if user_data is 32 bytes, then the used space is 1152 bytes(14*40/8*16+32), the 128 bytes (1280-1152) space is not written. If there need be filled with 1 page, then the bit[24] of the register can be set to 1, and the bit[23:16] is written to 0x80, that the controller can automatically pad 128 bytes random data.

NOTE

Make sure that random function is enabled if there need be sent random data,that is, the NDFC_RANDOM_EN of 0x34 register is 0x1, or else the padding data is non-random, is all-0.

5.2.3.7. NDFC Command IO Register

The bit[27] of the **NDFC Command IO Register** is used to enable the operation about whether tramsmitting the second random command, the function is only for writing operation.
The bit[9:8] of the **NDFC Command IO Register** is the address quantity that follows after random read/write operation commond in Interleave mode when batch command function is used. Usually the address number is 2 bytes column address,but for individual TLC chip(for example TOSHIBA), the address quantity that follows after random read/write command is 5 bytes, so you should set here in particular.

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5.2.4. Programming Guidelines

5.2.4.1. Initializing Nand Flash

The NAND Flash is initialized as follows:

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step2:Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; write 0xFF to NDFC_CMD[NDFC_CMD_LOW_BYTE] to send reset command.

Step3: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

5.2.4.2. Erasing Nand Flash

The NAND Flash is erased as follows:

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step2: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB;
Configure NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of address to be transferred;
Write the address of the block to be erased in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;
Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x60 to send block erase command.

Step3: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

Step4: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step5: Set NDFC_CMD[NDFC_WAIT_FLAG] to 1 to ensure wait RB, set NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command; set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0xD0 to send erasing command.

Step6: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

Step7: Read flash state until flash is ready, configure NDFC_CNT[NDFC_DATA_CNT] to set 1byte transfer data, set NDFC_CMD[NDFC_SEND_FIRST_CMD, NDFC_DATA_TRANS] to 0x3 to send the first command and transfer data. Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x70 to send read status command, read RAM0_BASE to wait ready status.

5.2.4.3. Writing Nand Flash

Step1: Erase the address of the block to be operated.

Step2: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step3: Configure RAM0_BASE to write data to RAM0.

Step4: Configure NDFC_CNT[NDFC_DATA_CNT] to set transferred data;
Set NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure

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NDFC_CMD[NDFC_DATA_TRANS, NDFC_ACCESS_DIR] to 0x3 to set access direction as writing;

Set NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of the address to be transferred, write the address of the block to be operated in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;

Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x80 to send page program command.

Step5: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step6: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; configure NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x10 to send end command.

Step7: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

5.2.4.4. Reading Nand Flash

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step2: Configure NDFC_CNT[NDFC_DATA_CNT] to set transferred data;

Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command;

Configure NDFC_CMD[NDFC_ACCESS_DIR] to 0 to set access direction as reading;

Set NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of the address to be transferred, write the address of the block to be operated in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;

Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x00 to send page read command.

Step3: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.

Step4: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; configure NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x30 to send end command.

Step5: Read RAM0_BASE to get data from flash.

Step6: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

5.2.5. Register List

Module Name	Base Address
NDFC	0x04011000

Register Name	Offset	Description
NDFC_CTL	0x0000	NDFC Configure and Control Register
NDFC_ST	0x0004	NDFC Status Information Register
NDFC_INT	0x0008	NDFC Interrupt Control Register
NDFC_TIMING_CTL	0x000C	NDFC Timing Control Register
NDFC_TIMING_CFG	0x0010	NDFC Timing Configure Register
NDFC_ADDR_LOW	0x0014	NDFC Low Word Address Register

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NDFC_ADDR_HIGH	0x0018	NDFC High Word Address Register
NDFC_DATA_BLOCK_MASK	0x001C	NDFC Data Block Mask Register
NDFC_CNT	0x0020	NDFC Data Counter Register
NDFC_CMD	0x0024	NDFC Commands IO Register
NDFC_RCMD_SET	0x0028	NDFC Read Command Set Register
NDFC_WCMD_SET	0x002C	NDFC Write Command Set Register
NDFC_ECC_CTL	0x0034	NDFC ECC Control Register
NDFC_ECC_ST	0x0038	NDFC ECC Status Register
NDFC_DATA_PAT_STA	0x003C	NDFC Data Pattern Status Register
NDFC_EFR	0x0040	NDFC Enhanced Feature Register
NDFC_RDATA_STA_CTL	0x0044	NDFC Read Data Status Control Register
NDFC_RDATA_STA_0	0x0048	NDFC Read Data Status Register 0
NDFC_RDATA_STA_1	0x004C	NDFC Read Data Status Register 1
NDFC_ERR_CNT_N	0x0050+0x04*N	NDFC Error Counter Register(N from 0 to 7)
NDFC_USER_DATA_LEN_N	0x0070+0x04*N	NDFC User Data Length Register(N from 0 to 3)
NDFC_USER_DATA_N	0x0080+0x04*N	NDFC User Data Field Register N (N from 0 to 31)
NDFC_EFNAND_STA	0x0110	NDFC EFNAND Status Register
NDFC_SPARE_AREA	0x0114	NDFC Spare Area Register
NDFC_PAT_ID	0x0118	NDFC Pattern ID Register
NDFC_DDR2_SPEC_CTL	0x011C	NDFC DDR2 Specific Control Register
NDFC_NDMA_MODE_CTL	0x0120	NDFC Normal DMA Mode Control Register
NDFC_MDMA_DLBA_REG	0x0200	NDFC MBUS DMA Descriptor List Base Address Register
NDFC_MDMA_STA	0x0204	NDFC MBUS DMA Interrupt Status Register
NDFC_DMA_INT_MASK	0x0208	NDFC MBUS DMA Interrupt Enable Register
NDFC_MDMA_CUR_DESC_ADDR	0x020C	NDFC MBUS DMA Current Descriptor Address Register
NDFC_MDMA_CUR_BUF_ADDR	0x0210	NDFC MBUS DMA Current Buffer Address Register
NDFC_DMA_CNT	0x0214	NDFC DMA Byte Counter Register
NDFC_IO_DATA	0x0300	NDFC Input/Output Data Register

5.2.6. Register Description

5.2.6.1. NDFC Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: NDFC_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	NDFC_DDR_TYPE Type of DDR data interface This bit is valid when NF_TYPE is 0x2 or 0x3. 0: DDR 1: DDR2
27:24	R/W	0x0	NDFC_CE_SEL Chip Select for NAND Flash Chips

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			0000: NDFC Select Chip 0 0001: NDFC Select Chip 1 0010: NDFC Select Chip 2 0011: NDFC Select Chip 3 0100: NDFC Select Chip 4 0101: NDFC Select Chip 5 0110: NDFC Select Chip 6 0111: NDFC Select Chip 7 1000: NDFC Select Chip 8 1001: NDFC Select Chip 9 1010: NDFC Select Chip 10 1011: NDFC Select Chip 11 1100: NDFC Select Chip 12 1101: NDFC Select Chip 13 1110: NDFC Select Chip 14 1111: NDFC Select Chip 15
23:22	/	/	/
21	R/W	0x0	NDFC_DDR_RM DDR Repeat Data Mode 0: Lower byte 1: Higher byte
20	R/W	0x0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0x0	NF_TYPE NAND Flash Type 00: Normal SDR NAND 01: Reserved 10: ONFI DDR NAND 11: Toggle DDR NAND
17	R/W	0x0	NDFC_CLE_POL NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0x0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0x0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0x0	NDFC_RAM_METHOD Access internal RAM method 0: Access internal RAM by AHB method

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			1: Access internal RAM by DMA method
13:12	/	/	/
11:8	R/W	0x0	NDFC_PAGE_SIZE 000: 1KB 001: 2KB 010: 4KB 011: 8KB 100: 16KB 101: 32KB The page size is for main field data.
7	/	/	/
6	R/W	0x0	NDFC_CE_ACT Chip Select Signal CE# Control during NAND Operation 0: De-active Chip Select Signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatic controls Chip Select Signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled
5	/	/	/
4:3	R/W	0x0	NDFC_RB_SEL NDFC External R/B Signal Select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0x0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus
1	R/W1C	0x0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset
0	R/W	0x0	NDFC_EN NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

5.2.6.2. NDFC Status Register (Default Value: 0x0000_0F00)

Offset: 0x0004			**Register Name: NDFC_ST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is more than threshold value. 1: The number of bit 1 during current read operation is less than or equal to threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1.

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			The threshold value is configured in NDFC_RDATA_STA_TH.
12	R	0x0	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is more than threshold value. 1: The number of bit 0 during current read operation is less than or equal to the threshold value. This field only is valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
11	R	0x1	NDFC_RB_STATE3 NAND Flash R/B 3 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	0x1	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	0x1	NDFC_RB_STATE1 NAND Flash R/B 1 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	0x1	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0x0	NDFC_STA 0: NDFC FSM in IDLE state 1: NDFC FSM in BUSY state When NDFC_STA is 0, NDFC can accept new command and process command.
3	R	0x0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W1C	0x0	NDFC_DMA_INT_FLAG When it is 1, it means that a pending DMA is completed. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
1	R/W1C	0x0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command Mode or one Batch Command Work Mode. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
0	R/W1C	0x0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be cleared after writing 1 to this bit.

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5.2.6.3. NDFC Interrupt and DMA Enable Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: NDFC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.
1	R/W	0x0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a single command in normal command work mode or one batch command work mode. 0: Disable 1: Enable
0	R/W	0x0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state. 0: Disable 1: Enable

5.2.6.4. NDFC Timing Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: NDFC_TIMING_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	NDFC_READ_PIPE In SDR mode: 00: Normal 01: EDO 10: E-EDO Others: Reserved In DDR mode: 1~15 is valid.(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0x0	NDFC_DC_CTL NDFC Delay Chain Control. These bits are only valid in DDR data interface, and configure the relative phase between DQS and DQ[0…7] .

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5.2.6.5. NDFC Timing Configure Register(Default Value: 0x0000_0095)

Offset: 0x0010			Register Name: NDFC_TIMING_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	T_WC Write Cycle Time 00: 1*2T 01: 2*2T 10: 3*2T 11: 4*2T
17:16	R/W	0x0	T_CCS Change Column Setup Time 00: 12*2T 01: 20*2T 10: 28*2T 11: 60*2T
15:14	R/W	0x0	T_CLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0x0	T_CS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0x0	T_CDQSS DQS Setup Time for Data Input Start 0: 4*2T 1: 20*2T
10:8	R/W	0x0	T_CAD Command, Address, Data Delay 000: 2*2T 001: 6*2T 010: 10*2T 011: 14*2T 100: 22*2T 101: 30*2T 110/111: 62*2T
7:6	R/W	0x2	T_RHW Cycle Number from RE# High to WE# Low 00: 4*2T

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			01: 12*2T 10: 20*2T 11: 28*2T
5:4	R/W	0x1	T_WHR Cycle Number from WE# High to RE# Low 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
3:2	R/W	0x1	T_ADL Cycle Number from Address to Data Loading 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
1:0	R/W	0x1	T_WB Cycle Number from WE# High to Busy 00:14*2T 01: 22*2T 10: 30*2T 11: 38*2T

5.2.6.6. NDFC Address Low Word Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: NDFC_ADDR_LOW
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA4 NAND Flash 4th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA3 NAND Flash 3rd Cycle Address Data
15:8	R/W	0x0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0x0	ADDR_DATA1 NAND Flash 1st Cycle Address Data

5.2.6.7. NDFC Address High Word Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: NDFC_ADDR_HIGH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA7

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			NAND Flash 7th Cycle Address Data
15:8	R/W	0x0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0x0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

5.2.6.8. NDFC Data Block Mask Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: NDFC_DATA_BLOCK_MASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 31 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
30	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 30 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
29	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 29 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
28	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 28 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
27	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 27 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
26	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 26 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable

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			1: Enable 1 data block = 1024 bytes main field data.
25	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 25 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
24	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 24 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
23	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 23 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
22	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 22 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
21	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 21 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
20	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 20 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
19	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 19 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
18	R/W	0x0	NDFC_DATA_BLOCK_MASK

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			It is used to indicate the data block 18 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
17	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 17 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
16	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 16 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
15	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 15 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
14	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 14 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
13	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 13 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
12	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 12 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
11	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 11 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable

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			1: Enable 1 data block = 1024 bytes main field data.
10	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 10 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
9	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 9 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
8	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 8 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
7	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 7 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
6	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 6 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
5	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 5 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
4	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 4 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
3	R/W	0x0	NDFC_DATA_BLOCK_MASK

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			It is used to indicate the data block 3 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
2	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 2 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
1	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 1 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.
0	R/W	0x0	NDFC_DATA_BLOCK_MASK It is used to indicate the data block 0 should be written or read during batch command procession(NDFC_CMD_TYPE=0x10 in **NDFC_CMD**). 0: Disable 1: Enable 1 data block = 1024 bytes main field data.

5.2.6.9. NDFC Data Counter Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: NDFC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	NDFC_DATA_CNT Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

5.2.6.10. NDFC Command IO Register (Default Value: 0x0000_0000)

Offset: 0x0024			**Register Name: NDFC_CMD**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	NDFC_CMD_TYPE 00: Common command for normal operation 01: Special command for Flash spare field operation 10: Page command for batch process operation 11: Reserved

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29	R/W	0x0	NDFC_SEND_FOURTH_CMD 0: Donot send fourth set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
28	R/W	0x0	NDFC_SEND_THIRD_CMD 0: Donot send third set command 1: Send it on the external memory's bus It is used for EF-NAND page read.
27	R/W	0x0	NDFC_SEND_RANDOM_CMD2_CTL 0: Donot send random cmd2 (NDFC_RANDOM_CMD2) 1: Send random cmd2 **NOTE** **It is only valid in batch cmd operation and writing operation.**
26	R/W	0x0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for common command and special command. 0: No action 1: DMA transfer automatically It only is active when NDFC_RAM_METHOD is 1. If this bit is set to 1, NDFC should setup DRQ to fetch data before output to Flash or NDFC should setup DRQ to send to system memory after fetching data from Flash. If this bit is set to 0, NDFC output the data in internal RAM or do nothing after fetching data from Flash.
25	R/W	0x0	NDFC_SEQ User data & BCH check word position. It only is active for Page Command, donot care about this bit for other two commands. 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0x0	NDFC_SEND_SECOND_CMD 0: Donot send second set command 1: Send it on the external memory's bus
23	R/W	0x0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY; otherwise it cannot when the internal NDFC_RB wire is BUSY
22	R/W	0x0	NDFC_SEND_FIRST_CMD 0: Donot send first set command 1: Send it on the external memory's bus
21	R/W	0x0	NDFC_DATA_TRANS 0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field NDFC_ACCESS_DIR
20	R/W	0x0	NDFC_ACCESS_DIR 0: Read NAND Flash

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			1: Write NAND Flash
19	R/W	0x0	NDFC_SEND_ADR 0: Donot send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by NDFC_ADR_NUM field
18:16	R/W	0x0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field 111: 8 cycles address field
15:10	/	/	/
9:8	R/W	0x0	NDFC_ADR_NUM_IN_PAGE_CMD The number of address cycles during page command. 00: 2 address cycles 11: 5 address cycles Others: reserved
7:0	R/W	0x0	NDFC_CMD_LOW_BYTE NDFC command low byte data This command will be sent to external Flash by NDFC.

5.2.6.11. NDFC Command Set Register 0(Default Value: 0x00E0_0530)

Offset: 0x0028			Register Name: NDFC_CMD_SET0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x00	NDFC_RANDOM_CMD2 Used for Batch Operation
23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1 Used for Batch Read Operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for Batch Read Operation
7:0	R/W	0x30	NDFC_READ_CMD Used for Batch Read Operation

5.2.6.12. NDFC Command Set Register 1(Default Value: 0x7000_8510)

Offset: 0x002C			Register Name: NDFC_CMD_SET1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x70	NDFC_READ_CMD0

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			Used for EF-NAND Page Read Operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND Page Read Operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for Batch Write Operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for Batch Write Operation

5.2.6.13. NDFC ECC Control Register(Default Value: 0x4A80_0008)

Offset: 0x0034			**Register Name: NDFC_ECC_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x4a80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when NDFC_RANDOM_EN is set to '1'.
15:8	R/W	0x0	NDFC_ECC_MODE 00000000: BCH-16 00000001: BCH-24 00000010: BCH-28 00000011: BCH-32 00000100: BCH-40 00000101: BCH-44 00000110: BCH-48 00000111: BCH-52 00001000: BCH-56 00001001: BCH-60 00001010: BCH-64 00001011: BCH-68 00001100: BCH-72 00001101: BCH-76 00001110: BCH-80 Others : Reserved
7	R/W	0x0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size
6	R/W	0x0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
5	R/W	0x0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
4	R/W	0x0	NDFC_ECC_EXCEPTION

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			0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. **NOTE** **It is only active when ECC is ON**
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error Correction function no pipeline with next block operation 1: Error Correction pipeline
2:1	/	/	/
0	R/W	0x0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

5.2.6.14. NDFC ECC Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: NDFC_ECC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 31 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[31] of this register is corresponding the 31th ECC data block. 1 ECC Data Block = 1024 bytes.
30	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 30 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[30] of this register is corresponding the 30th ECC data block. 1 ECC Data Block = 1024 bytes.
29	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 29 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[29] of this register is corresponding the 29th ECC data block. 1 ECC Data Block = 1024 bytes.
28	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 28 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[28] of this register is corresponding the 28th ECC data block. 1 ECC Data Block = 1024 bytes.

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27	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 27 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[27] of this register is corresponding the 27th ECC data block. 1 ECC Data Block = 1024 bytes.
26	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 26 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[26] of this register is corresponding the 26th ECC data block. 1 ECC Data Block = 1024 bytes.
25	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 25 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[25] of this register is corresponding the 25th ECC data block. 1 ECC Data Block = 1024 bytes.
24	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 24 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[24] of this register is corresponding the 24th ECC data block. 1 ECC Data Block = 1024 bytes.
23	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 23 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[23] of this register is corresponding the 23th ECC data block. 1 ECC Data Block = 1024 bytes.
22	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 22 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[22] of this register is corresponding the 22th ECC data block. 1 ECC Data Block = 1024 bytes.
21	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 21 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[21] of this register is corresponding the 21th ECC data block. 1 ECC Data Block = 1024 bytes.
20	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 20 0: ECC can correct these error bits or there is no error bit

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			1: Error bits number beyond of ECC correction capability and cannot correct them The bit[20] of this register is corresponding the 20th ECC data block. 1 ECC Data Block = 1024 bytes.
19	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 19 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[19] of this register is corresponding the 19th ECC data block. 1 ECC Data Block = 1024 bytes.
18	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 18 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[18] of this register is corresponding the 18th ECC data block. 1 ECC Data Block = 1024 bytes.
17	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 17 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[17] of this register is corresponding the 17th ECC data block. 1 ECC Data Block = 1024 bytes.
16	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 16 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[16] of this register is corresponding the 16th ECC data block. 1 ECC Data Block = 1024 bytes.
15	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 15 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[15] of this register is corresponding the 15th ECC data block. 1 ECC Data Block = 1024 bytes.
14	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 14 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[14] of this register is corresponding the 14th ECC data block. 1 ECC Data Block = 1024 bytes.
13	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 13 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[13] of this register is corresponding the 13th ECC data block. 1 ECC Data Block = 1024 bytes.

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12	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 12 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[12] of this register is corresponding the 12th ECC data block. 1 ECC Data Block = 1024 bytes.
11	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 11 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[11] of this register is corresponding the 11th ECC data block. 1 ECC Data Block = 1024 bytes.
10	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 10 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[10] of this register is corresponding the 10th ECC data block. 1 ECC Data Block = 1024 bytes.
9	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 9 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[9] of this register is corresponding the 9th ECC data block. 1 ECC Data Block = 1024 bytes.
8	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 8 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[8] of this register is corresponding the 8th ECC data block. 1 ECC Data Block = 1024 bytes.
7	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 7 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[7] of this register is corresponding the 7th ECC data block. 1 ECC Data Block = 1024 bytes.
6	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 6 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[6] of this register is corresponding the 6th ECC data block. 1 ECC Data Block = 1024 bytes.
5	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 5 0: ECC can correct these error bits or there is no error bit

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			1: Error bits number beyond of ECC correction capability and cannot correct them The bit[5] of this register is corresponding the 5th ECC data block. 1 ECC Data Block = 1024 bytes.
4	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 4 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[4] of this register is corresponding the 4th ECC data block. 1 ECC Data Block = 1024 bytes.
3	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 3 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[3] of this register is corresponding the 3rd ECC data block. 1 ECC Data Block = 1024 bytes.
2	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 2 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[2] of this register is corresponding the 2nd ECC data block. 1 ECC Data Block = 1024 bytes.
1	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 1 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[1] of this register is corresponding the 1st ECC data block. 1 ECC Data Block = 1024 bytes.
0	R	0x0	NDFC_ECC_ERR Error information bit of Data Block 0 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and cannot correct them The bit[0] of this register is corresponding the 0 ECC data block. 1 ECC Data Block = 1024 bytes.

5.2.6.15. NDFC Data Pattern Status Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: NDFC_DATA_PAT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 31 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
30	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 30 when read from

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			external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
29	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 29 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
28	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 28 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
27	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 27 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
26	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 26 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
25	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 25 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
24	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 24 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
23	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 23 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
22	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 22 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
21	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 21 when read from

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			external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
20	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 20 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
19	R	0x0	Special pattern (all 0x00 or all 0xff) found Flag for Data Block 19 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
18	R	0x0	Special pattern (all 0x00 or all 0xff) Found flag for Data Block 18 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
17	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 17 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
16	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 16 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
15	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 15 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
14	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 14 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
13	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 13 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
12	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 12 when read from

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			external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
11	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 11 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
10	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 10 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
9	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 9 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
8	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 8 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
7	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 7 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
6	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 6 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
5	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 5 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
4	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 4 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
3	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 3 when read from

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			external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
2	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 2 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
1	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 1 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.
0	R	0x0	Special pattern (all 0x00 or all 0xff) found flag for Data Block 0 when read from external NAND flash. 0: No found 1: Special pattern is found The register of NDFC_PAT_ID would indicate which kind of pattern is found.

5.2.6.16. NDFC Enhanced Feature Register(Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: NDFC_EFR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DB_CNT_EN Dummy_Byte_Count_EN 0:Disable fill Dummy Byte. 1:Enable fill Dummy Byte.
23:16	R/W	0x0	DB_CNT Dummy_Byte_Count After PAGE CMD operation finishing sending out the main data , user data and ECC code, controller would send dummy byte to fill the unused space in one page. **NOTE** **It is only valid in PAGE CMD operation(NDFC_CMD_TYPE=0x3), and this function is disabled when Dummy_Byte_Count_EN is 0.** **If the NDFC_RANDOM_EN = 0x0, the value of the dummy byte is 0, so in order to improve the stability, when using this function , it is better to set the NDFC_RANDOM_EN to 0x1.**
15:9	/	/	/
8	R/W	0x0	NDFC_WP_CTRL NAND Flash Write Protect Control Bit

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			0: Write Protect is active 1: Write Protect is not active When this bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0x0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, special error bits are inserted before writing external Flash Memory. 0: No error is inserted (ECC Normal Operation) n: N bits error are inserted

5.2.6.17. NDFC Read Data Status Control Register(Default Value: 0x0100_0000)

Offset: 0x0044			Register Name: NDFC_RDATA_STA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN 0: Disable to count the number of bit 1 and bit 0 during current read operation 1: Enable to count the number of bit 1 and bit 0 during current read operation The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:19	/	/	/
18:0	R/W	0x0	NDFC_RDATA_STA_TH The threshold value to generate data status If the number of bit 1 during current read operation is less than or equal to threshold value, the bit 13 of NDFC_ST register will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, the bit 12 of NDFC_ST register will be set.

5.2.6.18. NDFC Read Data Status Register 0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: NDFC_RDATA_STA_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when next command is executed.

5.2.6.19. NDFC Read Data Status Register 1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: NDFC_RDATA_STA_1
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	R	0x0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when next command is executed.

5.2.6.20. NDFC Error Counter Register N(Default Value: 0x0000_0000)

Offset: 0x0050+N*0x04(N=0~7)			Register Name: NDFC_ERR_CNT_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[8M+7: 8M] (M=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[N*0x04+M] 00000000: No corrected bits 00000001: 1 corrected bit 00000010: 2 corrected bits ..... 01010000 : 80 corrected bits Others: Reserved **NOTE** **1 ECC Data Block =1024 bytes**

5.2.6.21. NDFC User Data Length Register N(Default Value: 0x0000_0000)

Offset: 0x0070+N*0x04(N=0~3)			Register Name: NDFC_USER_DATA_LEN_N
Bit	**Read/Write**	**Default/Hex**	**Description**
[4M+3 : 4M] (M=0~7)	R/W	0x0	It's used to indicate user data's length of ECC DATA BLOCK[0x08*N+M]. 0000 : no user data 0001 : 4 bytes user data 0010 : 8 bytes user data 0011 : 12 bytes user data 0100 : 16 bytes user data 0101 : 20 bytes user data 0110 : 24 bytes user data 0111 : 28 bytes user data 1000 : 32 bytes user data Other : reserved

5.2.6.22. NDFC User Data Register N(Default Value: 0xFFFF_FFFF)

Offset: 0x0080 + N*0x04(N=0~31)			Register Name: NDFC_USER_DATA_N
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xffffffff	USER_DATA All of the user data in one page is stored in NDFC_USER_DATA_N.

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			The start register address of each ECC DATA BLOCK's user data is determined by its length configured in NDFC_USER_DATA_LEN_N. For example: ECC DATA BLOCK[0] user data len = 8 Bytes, address = 0x80 ECC DATA BLOCK[1] user data len = 0 Bytes, ECC DATA BLOCK[2] user data len = 4 Bytes, address = 0x80+8 ECC DATA BLOCK[3] user data len = 4 Bytes, address = 0x80+8+4 ECC DATA BLOCK[4] user data len = 0 Bytes ECC DATA BLOCK[5] user data len = 16 Bytes, address = 0x80+8+4+4 ECC DATA BLOCK[6] user data len = 0 Bytes ECC DATA BLOCK[7] user data len = 0 Bytes

5.2.6.23. NDFC EFNAND Status Register(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: NDFC_EFNAND_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	EF_NAND_STATUS The status value for EF-NAND page read operation

5.2.6.24. NDFC Spare Area Register(Default Value: 0x0000_0400)

Offset: 0x0114			Register Name: NDFC_SPARE_AREA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the spare area first byte address for NDFC interleave page operation.

5.2.6.25. NDFC Pattern ID Register(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: NDFC_PAT_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
n (n=0~31)	R	0x0	PAT_ID Special Pattern ID for ECC data block[n] 0: All 0x00 is found 1: All 0xFF is found

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5.2.6.26. NDFC DDR2 Specific Control Register(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: NDFC_DDR2_SPEC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	DLEN_WR The number of latency DQS cycle for write 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
11:8	R/W	0x0	DLEN_RD The number of latency DQS cycle for read 0000: No latency 0001: One latency DQS cycle 0010: Two latency DQS cycle 0011: Four latency DQS cycle
7:3	/	/	/
2	R/W	0x0	EN_RE_C Enable the complementary RE# signal 0: Disable 1: Enable
1	R/W	0x0	EN_DQS_C Enable the complementary DQS signal 0: Disable 1: Enable
0	/	/	/

5.2.6.27. NDFC Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0120			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	DMA_ACT_STA 00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	DMA_ACK_EN 0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	DELAY_CYCLE The counts of hold cycles from DMA last signal high to dma_active high

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5.2.6.28. NDFC MBUS DMA Descriptor List Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: NDFC_MDMA_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_DESC_BASE_ADDR Start Address of Descriptor List Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the DMA internally. Hence these LSB bits are read-only.

5.2.6.29. NDFC MBUS DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: NDFC_MDMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_FINISH_INT Transfer Finish Interrupt Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

5.2.6.30. NDFC MBUS DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: NDFC_DMA_INT_MASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NFC_MDMA_TRANS_INT_ENB Transfer Interrupt Enable When set, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled. Bit 0: Corresponding DMA descriptor 0 Bit 1: Corresponding DMA descriptor 1 … Bit 31: Corresponding DMA descriptor 31

5.2.6.31. NDFC MBUS DMA Current Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: NDFC_MDMA_CUR_DESC_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_DESC_ADDR Current Descriptor Address Pointer

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			Cleared on reset. Pointer updated by DMA during operation. This register points to the start address of the current descriptor read by the DMA.

5.2.6.32. NDFC MBUS DMA Current Buffer Address Register(Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: NDFC_MDMA_CUR_BUF_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_BUFF_ADDR Current Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation. This register points to the current Data Buffer Address being accessed by the DMA.

5.2.6.33. NDFC DMA Byte Counter Register(Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: NDFC_DMA_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	DMA_CNT DMA data counter, including MBUS DMA and Normal DMA

5.2.6.34. NDFC IO Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: NDFC_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_IO_DATA Read/Write data into internal RAM Access unit is 32-bit.

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5.3. SD/MMC Host Controller(SMHC)

5.3.1. Overview

The SD-MMC Host Controller(SMHC) controls the read/write operations on the secure digital(SD) card and multimedia card(MMC),and supports various extended devices based on the secure digital input/output(SDIO) protocol.The T7 provides four SMHC interfacs for controlling the SD card,MMC and SDIO device.

The SMHC has the following features:

- Supports eMMC boot operation
- Supports command completion signal and interrupt to host processor and command completion signal disable feature
- SMHC0 supports SD (Version1.0 to 2.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - DDR mode 50MHz@3.3V IO pad
- SMHC1 supports SDIO(Version1.1 to 3.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
- SMHC2 supports MMC(Version3.3 to 5.0), 8-bit bus width
  - SDR mode 150MHz@1.8V IO pad
  - SDR mode 50MHz@3.3V IO pad
  - DDR mode 100MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
- SMHC3 supports SD (Version1.0 to 2.0),4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - DDR mode 50MHz@3.3V IO pad
- Hardware CRC generation and error detection
- Programmable baud rate
- Host pull-up control
- SDIO interrupts in 1-bit and 4-bit modes
- Block size of 1 to 65535 bytes
- Descriptor-based internal DMA controller
- Internal 1KB FIFO for data transfer

5.3.2. Block Diagram

Figure 5-17 shows a block diagram of the SMHC.

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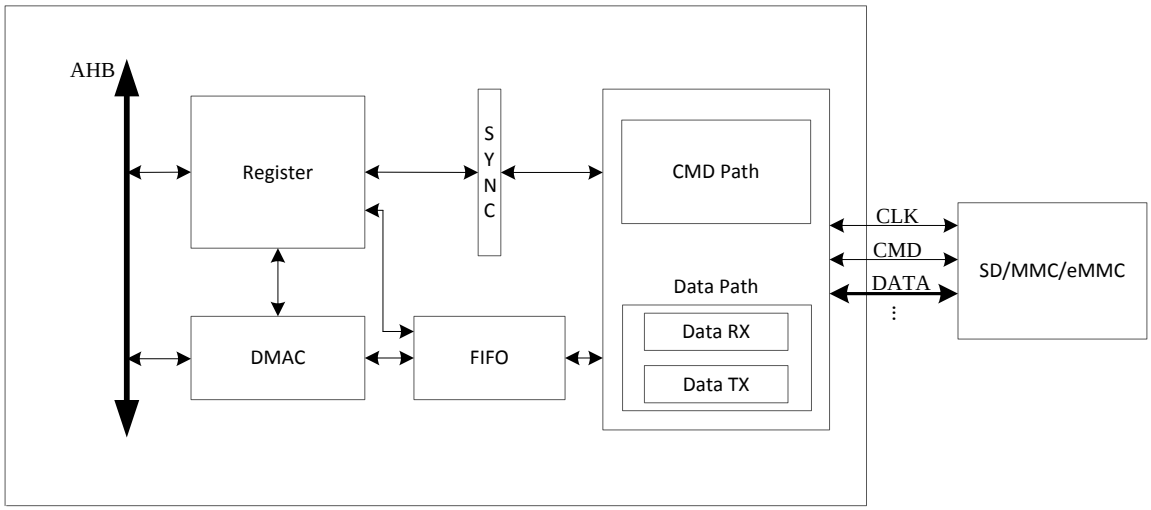

Figure 5- 17. SMHC Block Diagram

5.3.3. Operations and Functional Descriptions

5.3.3.1. External Signals

Table 5-3 describes the external signals of SMHC.

Table 5- 3. SMHC External Signals

Port Name	Width	Type	Description
SDC0_CLK	1	O	Clock output for SD/TF card
SDC0_CMD	1	I/O,OD	CMD line for SD/TF card
SDC0_D[i] (i=0~3)	4	I/O	Data line for SD/TF card
SDC1_CLK	1	O	Clock output for SDIO Wi-Fi
SDC1_CMD	1	I/O,OD	CMD line for SDIO Wi-Fi
SDC1_D[i] (i=0~3)	4	I/O	Data line for SDIO Wi-Fi
SDC2_CLK	1	O	Clock output for MMC
SDC2_CMD	1	I/O,OD	CMD line for MMC
SDC2_D[i] (i=0~7)	8	I/O	Data line for MMC
SDC2_RST	1	O	Reset signal for MMC
SDC2_DS	1	I	Data Strobe for MMC
SDC3_CLK	1	O	Clock output for SD/TF card
SDC3_CMD	1	I/O,OD	CMD line for SD/TF card
SDC3_D[i] (i=0~3)	4	I/O	Data line for SD/TF card

5.3.3.2. Clock Sources

Each SMHC gets three different clocks. User can select one of them to make SMHC clock source. Table 5-4 describes

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the clock sources of SMHC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 5- 4. SMHC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERI0(2X)	Peripheral Clock, the default value is 1.2GHz
PLL_PERI1(2X)	Peripheral Clock, the default value is 1.2GHz

5.3.3.3. Timing Diagram

Please refer to relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card(eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card(eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard(5.0)

5.3.3.4. Internal DMA Controller Description

SMHC has an internal DMA controller (IDMAC) to transfer data between host memory and SMHC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

5.3.3.4.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

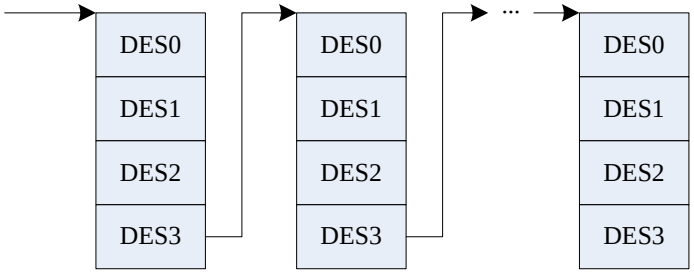

Figure 5- 18. IDMAC Descriptor Structure Diagram

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This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96] bits in a descriptor.

5.3.3.4.2. DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:5	/	/
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor
0	/	/

5.3.3.4.3. DES1 Definition

For SMHC0/SMCH1/SMHC3:

Bits	Name	Descriptor
31:16	/	/
15:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

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For SMHC2:

Bits	Name	Descriptor
31:13	/	/
12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

5.3.3.4.4. DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32.

5.3.3.4.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present.

5.3.3.5. Calibrate Delay Chain

The sample clock delay chain and Data Strobe delay chain(the chain is only in SMHC2) are used to generate delay to make proper timing between data strobe and data signals. Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through **SMHC Bus Gating Reset Register** and **SMHC2 Clock Register**.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(CCU). Calibration delay chain is an internal function in SMHC and do not need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200MHz.

Step3: Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain**(bit[5:0]). Then write 0x0 to **delay control register** to clear the value.

Step4: Write 0x8000 to **delay control register** to start calibrate delay chain.

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Step5: Wait until the flag(bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at bit[13:8] in **delay control register**. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the cycle of SMHC's clock and the result of calibration.

NOTE

In the above descriptions,**delay control register** contains **SMHC Sample Delay Control Register** and **SMHC Data Strobe Delay Control Register**. **Delay Software Enable** contains **Sample Delay Software Enable** and **Data Strobe Delay Software Enable**. **Delay chain** contains **Sample Delay Software** and **Data Strobe Delay Software**.

5.3.4. Programming Guidelines

5.3.4.1. Initialization

Before data and command are exchanged between a card and the SMHC, the SMHC need to be initialized .The SMHC is initialized as follows.

Step1: Configure GPIO register as SMHC function by Port Controller module; reset clock by writing 1 to SMHC_BGR_REG[SMHCx_RST], open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING]; select clock sources and set division factor by configuring the SMHCx_CLK_REG(x=0,1,2) register.

Step2: Configure SMHC_CTRL to enable total interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupt and error abnormal interrupt, and register interrupt function.

Step3: Configure SMHC_CLKDIV to open clock for device; configure SMHC_CMD as change clock command(for example 0x80202000); send update clock command to deliver clock to device.

Step4: Configure SMHC_CMDARG, configure SMHC_CMD to set response type,etc, then command can send. According to initial process in the protocol, you can finish SMHC initializing by sending corresponding command one by one.

5.3.4.2. Writing a Single Data Block

To Write a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write 0x82 to SMHC_IDMAC to enable IDMAC interrupt, configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 1 data block to the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD24(Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, send CMD24 command to write data to device.

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Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD24 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.3.4.3. Reading a Single Data Block

To read a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 1 data block from the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD17(Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD , send CMD17 command to read data from device to DRAM/SRAM.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD17 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.4.4. Writing Open-ended Multiple Data Blocks(CMD25+Auto CMD12)

To write open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

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Step3: If writing 3 data blocks to the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25(Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, send CMD25 command to write data to device, when data transfer is complete, CMD12 will be sent automatically .

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.3.4.5. Reading Open-ended Multiple Data Blocks(CMD18+Auto CMD12)

To read open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks from the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD , send CMD18 command to read data to device, when data transfer is complete, CMD12 will be sent automatically.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD18 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.4.6. Writing Pre-defined Multiple Data Blocks(CMD23+CMD25)

To write pre-defined multiple data blocks, perform the following steps:

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Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks, then set SMHC_CMDARG to 0x3 to ensure the block number to be operated, send CMD23 command by writing 0x80000157 to SMHC_CMD .Check whether SMHC_RINTSTS[CC] is 1.If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25(Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, send CMD25 command to write data to device.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step8: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD,go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.3.4.7. Reading Pre-defined Multiple Data Blocks(CMD23+CMD18)

To read pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks, then set SMHC_CMDARG to 0x3 to ensure the block number to be operated, send CMD23 command by writing 0x80000157 to SMHC_CMD .Check whether SMHC_RINTSTS[CC] is 1.If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, send CMD18 command to read data from device to DRAM/SRAM.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

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Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD18 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.3.5. Register List

Module Name	Base Address
SMHC0	0x04020000
SMHC1	0x04021000
SMHC2	0x04022000
SMHC3	0x04023000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register
SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_CTYPE	0x000C	Bus Width Register
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register
SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_DBGC	0x0050	Current Debug Control Register
SMHC_CSDC	0x0054	CRC Status Detect Control Register (Only for SMHC2)
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_IDMAC	0x0080	IDMAC Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_IDST	0x0088	IDMAC Status Register
SMHC_IDIE	0x008C	IDMAC Interrupt Enable Register

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SMHC_THLD	0x0100	Card Threshold Control Register
EMMC_DDR_SBIT_DET	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RES_CRC	0x0110	Response CRC from Device
SMHC_D7_CRC	0x0114	CRC in Data7 from Device
SMHC_D6_CRC	0x0118	CRC in Data6 from Device
SMHC_D5_CRC	0x011C	CRC in Data5 from Device
SMHC_D4_CRC	0x0120	CRC in Data4 from Device
SMHC_D3_CRC	0x0124	CRC in Data3 from Device
SMHC_D2_CRC	0x0128	CRC in Data2 from Device
SMHC_D1_CRC	0x012C	CRC in Data1 from Device
SMHC_D0_CRC	0x0130	CRC in Data0 from Device
SMHC_CRC_STA	0x0134	CRC Status from Device in Write Operation
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
SMHC_FIFO	0x0200	Read/Write FIFO

5.3.6. Register Description

5.3.6.1. SMHC Global Control Register(Default Value: 0x0000_0100)

Offset: 0x0000			**Register Name: SMHC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 0: DMA bus 1: AHB bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit is used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit is used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this filed should be

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			cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

5.3.6.2. SMHC Clock Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: SMHC_CLKDIV**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM is in IDLE state

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16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card Clock Divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

5.3.6.3. SMHC Timeout Register(Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit When Host read data,data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),a next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data,no Data Timeout Limit.
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

5.3.6.4. SMHC Bus Width Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

5.3.6.5. SMHC Block Size Register(Default Value:0x0000_0200)

Offset: 0x0010	Register Name: SMHC_BLKSIZ

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Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

5.3.6.6. SMHC Byte Count Register(Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred; should be integer multiple of Block Size for block transfers.

5.3.6.7. SMHC Command Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge When software sets this bit along in mandatory boot operation, the controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation

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			10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; when this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send *Stop* or *Abort* command to stop current data transfer in progress.(CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the **SMHC_RESP1** will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type

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			0:Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without response 1: Command with response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

5.3.6.8. SMHC Command Argument Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

5.3.6.9. SMHC Response 0 Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

5.3.6.10. SMHC Response 1 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

5.3.6.11. SMHC Response 2 Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

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5.3.6.12. SMHC Response 3 Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

5.3.6.13. SMHC Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable

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4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

5.3.6.14. SMHC Masked Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	M_CARD_REMOVAL_INT Card Removed
30	R/W	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R/W	0x0	M_SDIO_INT SDIO Interrupt
15	R/W	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R/W	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R/W	0x0	M_DSE_BC_INT Data Start Error When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared.
12	R/W	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R/W	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R/W	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R/W	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start

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8	R/W	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R/W	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R/W	0x0	M_RCE_INT Response CRC Error
5	R/W	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R/W	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R/W	0x0	M_DTC_INT Data Transfer Complete
2	R/W	0x0	M_CC_INT Command Complete
1	R/W	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

5.3.6.15. SMHC Raw Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: SMHC_RINTSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE

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			Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error When set during receiving data, it means that host controller found a error start bit. It is valid at 4-bit or 8-bit bus mode. When it set, host found start bit at data0, but did not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host did not find start bit on data0. This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bits.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.

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5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

5.3.6.16. SMHC Status Register(Default Value: 0x0000_0006)

Offset: 0x003C			**Register Name: SMHC_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY

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			Card Data Busy Inverted version of DATA[0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data[3] Status level of DATA[3], checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA Command FSM States 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO Full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO RX Water Level Flag 0: FIFO didn’t reach receive trigger level 1: FIFO reached receive trigger level

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5.3.6.17. SMHC FIFO Water Level Register(Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst Size of Multiple Transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved It should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) FIFO_DEPTH = 256, FIFO_SIZE = 256 * 32 = 1K Recommended: MSize = 16, TX_TL = 240, RX_TL = 15 (for SMHC2) MSize = 8, TX_TL = 248, RX_TL = 7 (for SMHC0,SMHC1,SMHC3)
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF: Reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15, for SMHC2) 7 (means greater than 7, for SMHC0,SMHC1,SMHC3)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: No trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual.

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			Recommended: 240(means less than or equal to 240, for SMHC2) 248(means less than or equal to 248, for SMHC0,SMHC1,SMHC3)

5.3.6.18. SMHC Function Select Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

5.3.6.19. SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

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5.3.6.20. SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.3.6.21. SMHC CRC Status Detect Control Register(Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 110: HS400 speed mode 011: Other speed mode

NOTE

The register is only for SMHC2.

5.3.6.22. SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A. SD_A12A set the argument of command 12 automatically send by controller.

5.3.6.23. SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:28	/	/	/
27	R/W	0x0	DAT0_BYPASS

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			Select data0 input asyn or bypass sample logic, it is used to check card busy or not 0: Enable data0 bypass 1: Disable data0 bypass
26:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear command line's and data lines' input phase during update clock operation, 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Clear data lines' input phase before receive CRC status. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Clear data lines' input phase before transfer data. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Clear data lines' input phase before receive data. 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command rx phase before send command. 0: Disable 1: Enable
15:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore
3:0	/	/	/

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.24. SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x78			Register Name: SMHC_HWRST
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:1	/	/	/
0	R/W	0x1	HW_RST 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

5.3.6.25. SMHC IDMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When IDMAC fetches a descriptor, if the valid bit of a descriptor is not set, IDMAC FSM will go to the suspend state. Setting this bit will make IDMAC refetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable When set, the IDMAC is enabled.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

5.3.6.26. SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List Contains the base address of the First Descriptor. The LSB bits [1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

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5.3.6.27. SMHC IDMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	Reserved
12:10	R	0x0	IDMAC_ERR_STA Error Bits Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved EB is read-only.
9	R/W1C	0x0	ABN_INT_SUM Abnormal Interrupt Summary Logical OR of the following: IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: Descriptor Unavailable bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM Normal Interrupt Summary Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt

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			This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit.

5.3.6.28. SMHC IDMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt Summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

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5.3.6.29. SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_RD_THLD Card Read Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB (only for SMHC2) Card Write Threshold Enable(HS400) 0: Card write threshold disabled 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy clear interrupt disabled 1: Busy clear interrupt enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card read threshold disabled 1: Card read threshold enabled Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO.

5.3.6.30. SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit.

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			For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

5.3.6.31. SMHC Response CRC Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: SMHC_RESP_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.32. SMHC Data7 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: SMHC_DAT7_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT7_CRC Data[7] CRC CRC in data[7] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.33. SMHC Data6 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: SMHC_DAT6_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT6_CRC Data[6] CRC CRC in data[6] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data.

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			In 4 bits DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.34. SMHC Data5 CRC Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SMHC_DAT5_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT5_CRC Data[5] CRC CRC in data[5] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode,it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.35. SMHC Data4 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: SMHC_DAT4_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT4_CRC Data[4] CRC CRC in data[4] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.36. SMHC Data3 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: SMHC_DAT3_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT3_CRC

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			Data[3] CRC CRC in data[3] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.37. SMHC Data2 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: SMHC_DAT2_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT2_CRC Data[2] CRC CRC in data[2] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.38. SMHC Data1 CRC Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: SMHC_DAT1_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT1_CRC Data[1] CRC CRC in data[1] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

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5.3.6.39. SMHC Data0 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: SMHC_DAT0_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT0_CRC Data[0] CRC CRC in data[0] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.40. SMHC CRC Status Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: SMHC_CRC_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	CRC_STA CRC Status CRC status from device in write operation Positive CRC status token: 3’b010 Negative CRC status token: 3’b101

NOTE

This register is valid for SMHC0,SMHC1 and SMHC3.

5.3.6.41. SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode, 90^0 at HS400 mode. 1: Data drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode, 0^0 at HS400 mode.
16	R/W	0x1	CMD_DRV_PH_SEL

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			Command Drive Phase Select 0: Command drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode, 90^0 at HS400 mode. 1: Command drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode, 180^0 at HS400 mode.
15:0	/	/	/

5.3.6.42. SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

5.3.6.43. SMHC Data Strobe Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

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15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

5.3.6.44. SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			**Register Name: SMHC_FIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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Chapter 6 EMAC

6.1. Overview

The Ethernet Medium Access Controller (EMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000 Mbit/s external PHY with MII/RMII/RGMII interface in both full and half duplex mode. The Internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4 Kbytes TXFIFO and 16 Kbytes RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC has the following features:

- Supports 10/100/1000 Mbit/s data transfer rates
- Supports MII/RMII/RGMII PHY interface
- Supports MDIO
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 Kbytes
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 Kbytes of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 Kbytes TXFIFO for transmission packets and 16 Kbytes RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

6.2. Block Diagram

The block diagram of the EMAC is shown as follows.

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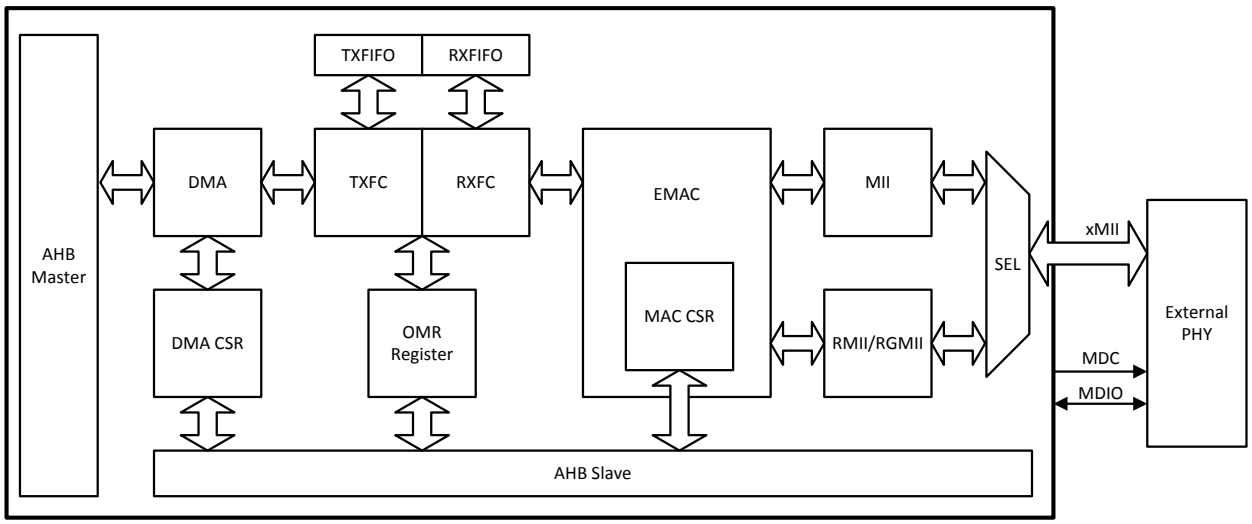

Figure 6- 1. EMAC Block Diagram

6.3. Operations and Functional Descriptions

6.3.1. External Signals

Table 6-1 describes the pin mapping of EMAC.

Table 6- 1. EMAC Pin Mapping

Pin Name	RGMII	MII	RMII
RGMII_RXD3/MII_RXD3/RMII_NULL	RXD3	RXD3	
RGMII_RXD2/MII_RXD2/RMII_NULL	RXD2	RXD2	
RGMII_RXD1/MII_RXD1/RMII_RXD1	RXD1	RXD1	RXD1
RGMII_RXD0/MII_RXD0/RMII_RXD0	RXD0	RXD0	RXD0
RGMII_RXCK/MII_RXCK/RMII_NULL	RXCK	RXCK	
RGMII_RXCTL/MII_RXDV/RMII_CRS_DV	RXCTL	RXDV	CRS_DV
RGMII_NULL/MII_RXERR/RMII_RXER		RXERR	RXER
RGMII_TXD3/MII_TXD3/RMII_NULL	TXD3	TXD3	
RGMII_TXD2/MII_TXD2/RMII_NULL	TXD2	TXD2	
RGMII_TXD1/MII_TXD1/RMII_TXD1	TXD1	TXD1	TXD1
RGMII_TXD0/MII_TXD0/RMII_TXD0	TXD0	TXD0	TXD0
RGMII_NULL/MII_CRS/RMII_NULL		CRS	
RGMII_TXCK/MII_TXCK/RMII_TXCK	TXCK	TXCK	TXCK
RGMII_TXCTL/MII_TXEN/RMII_TXEN	TXCTL	TXEN	TXEN
RGMII_NULL/MII_TXERR/RMII_NULL		TXERR	
RGMII_CLKIN/MII_COL/RMII_NULL	CLKIN	COL	

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MDC	MDC	MDC	MDC
MDIO	MDIO	MDIO	MDIO

Table 6-2 describes the pin list of RGMII.

Table 6- 2. EMAC RGMII Pin List

Pin Name	Description	Type
RGMII_TXD[3:0]	EMAC RGMII Transmit Data	O
RGMII_TXCTL	EMAC RGMII Transmit Control	O
RGMII_TXCK	EMAC RGMII Transmit Clock	O
RGMII_RXD[3:0]	EMAC RGMII Receive Data	I
RGMII_RXCTL	EMAC RGMII Receive Control	I
RGMII_RXCK	EMAC RGMII Receive Clock	I
RGMII_CKIN	EMAC RGMII 125MHz Reference Clock Input	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O

Table 6-3 describes the pin list of MII.

Table 6- 3. EMAC MII Pin List

Pin Name	Description	Type
MII_TXD[3:0]	EMAC MII Transmit Data	O
MII_TXEN	EMAC MII Transmit Enable	O
MII_TXCK	EMAC MII Transmit Clock	I
MII_TXERR	EMAC MII Transmit Error	O
MII_RXD[3:0]	EMAC MII Receive Data	I
MII_RXDV	EMAC MII Receive Data Valid	I
MII_RXCK	EMAC MII Receive Clock	I
MII_RXERR	EMAC MII Receive Error	I
MII_COL	EMAC MII Collision	I
MII_CRS	EMAC MII Carrier Sense	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O

Table 6-4 describes the pin list of RMII.

Table 6- 4. EMAC RMII Pin List

Pin Name	Description	Type
RMII_TXD[1:0]	EMAC RMII Transmit Data	O
RMII_TXEN	EMAC RMII Transmit Enable	O

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RMII_TXCK	EMAC RMII Transmit Clock	I
RMII_RXD[1:0]	EMAC RMII Receive Data	I
RMII_CRS_DV	EMAC RMII Receive Data Valid	I
RMII_RXER	EMAC RMII Receive Error	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O

6.3.2. Clock Sources

Table 6-5 describes the clock of EMAC.

Table 6- 5. EMAC Clock

Clock Name	Description	Type
RGMII_TXCK/ MII_TXCK/ RMII_TXCK	In RGMII mode, output 2.5MHz/25MHz/125MHz. In MII mode, input 2.5MHz/25MHz. In RMII mode, input 5MHz/50MHz.	O/I
RGMII_RXCK/ MII_RXCK/ RMII_NULL	In RGMII mode, input 2.5MHz/25MHz/125MHz. In MII mode, input 2.5MHz/25MHz. In RMII mode, no input	I
RGMII_CLKIN/ MII_COL/ RMII_NULL	In RGMII mode, input 125M Reference Clock In MII mode, no clock In RMII mode, no clock	I

6.3.3. Typical Application

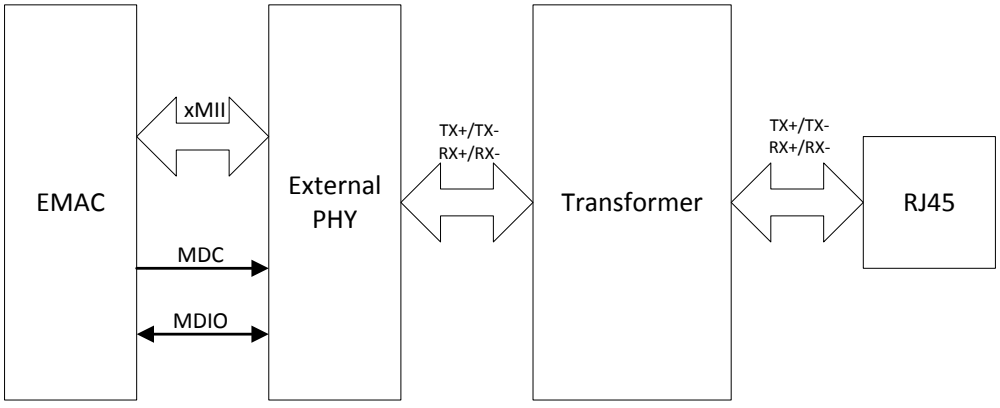

Figure 6- 2. EMAC Typical Application

6.3.4. EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of

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descriptors. Each descriptor consists of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in Figure 6-3. The address of each descriptor must be 32-bit aligned.

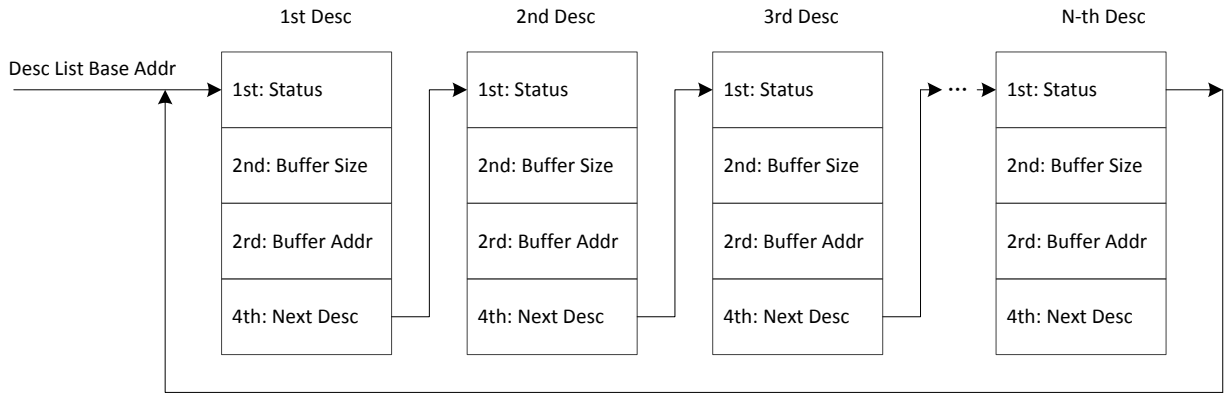

Figure 6- 3. EMAC RX/TX Descriptor List

6.3.5. Transmit Descriptor

6.3.5.1. 1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR

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	When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

6.3.5.2. 2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set, and the current frame has been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

6.3.5.3. 3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

6.3.5.4. 4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

6.3.6. Receive Descriptor

6.3.6.1. 1st Word of Receive Descriptor

Bits	Description

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31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame does not pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame does not pass SA filter.
12	Reserved
11	RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR When set, there is a late collision during reception in half-duplex mode.
5	Reserved
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.
2	Reserved
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

6.3.6.2. 2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When set , and a frame has been received, the RX_INT will not be set.
30:11	Reserved

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10:0	BUF_SIZE The size of buffer specified by current descriptor.

6.3.6.3. 3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

6.3.6.4. 4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

6.4. Register List

Module Name	Base Address
EMAC	0x05020000

Register Name	Offset	Description
EMAC_BASIC_CTL0	0x0000	EMAC Basic Control Register0
EMAC_BASIC_CTL1	0x0004	EMAC Basic Control Register1
EMAC_INT_STA	0x0008	EMAC Interrupt Status Register
EMAC_INT_EN	0x000C	EMAC Interrupt Enable Register
EMAC_TX_CTL0	0x0010	EMAC Transmit Control Register0
EMAC_TX_CTL1	0x0014	EMAC Transmit Control Register1
EMAC_TX_FLOW_CTL	0x001C	EMAC Transmit Flow Control Register
EMAC_TX_DMA_DESC_LIST	0x0020	EMAC Transmit Descriptor List Address Register
EMAC_RX_CTL0	0x0024	EMAC Receive Control Register0
EMAC_RX_CTL1	0x0028	EMAC Receive Control Register1
EMAC_RX_DMA_DESC_LIST	0x0034	EMAC Receive Descriptor List Address Register
EMAC_RX_FRM_FLT	0x0038	EMAC Receive Frame Filter Register
EMAC_RX_HASH0	0x0040	EMAC Hash Table Register0
EMAC_RX_HASH1	0x0044	EMAC Hash Table Register1
EMAC_MII_CMD	0x0048	EMAC Management Interface Command Register
EMAC_MII_DATA	0x004C	EMAC Management Interface Data Register
EMAC_ADDR_HIGH0	0x0050	EMAC MAC Address High Register0
EMAC_ADDR_LOW0	0x0054	EMAC MAC Address Low Register0

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EMAC_ADDR_HIGHx	0x0050+0x08*N(N=1~7)	EMAC MAC Address High RegisterN(N:1~7)
EMAC_ADDR_LOWx	0x0054+0x08*N(N=1~7)	EMAC MAC Address Low RegisterN(N:1~7)
EMAC_TX_DMA_STA	0x00B0	EMAC Transmit DMA Status Register
EMAC_TX_CUR_DESC	0x00B4	EMAC Current Transmit Descriptor Register
EMAC_TX_CUR_BUF	0x00B8	EMAC Current Transmit Buffer Address Register
EMAC_RX_DMA_STA	0x00C0	EMAC Receive DMA Status Register
EMAC_RX_CUR_DESC	0x00C4	EMAC Current Receive Descriptor Register
EMAC_RX_CUR_BUF	0x00C8	EMAC Current Receive Buffer Address Register
EMAC_RGMII_STA	0x00D0	EMAC RGMII Status Register

6.5. Register Description

6.5.1. EMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMAC_BASIC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

6.5.2. EMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: EMAC_BASIC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA priority 0: Same priority 1: RX priority over TX

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0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.

6.5.3. EMAC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this asserted, the RX DMA cannot acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume

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			when writing to RX_DMA_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Frame is transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to TX_DMA_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.

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6.5.4. EMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: EMAC_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt

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			0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

6.5.5. EMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: EMAC_TX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disable, transmit will continue until current transmit finishes.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

6.5.6. EMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission. 1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH

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			Threshold value of TX DMA FIFO When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO 0: Enable 1: Disable

6.5.7. EMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable

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			0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

6.5.8. EMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

6.5.9. EMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x

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			standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

6.5.10. EMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: EMAC_RX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_DMA_START When set, the RX DMA will not work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable,base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128

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			NOTE **Only valid when RX_MD == 0, full frames with a length less than the threshold are transferred automatically.**
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when receive descriptors/buffers is unavailable 1: Disable

6.5.11. EMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			**Register Name: EMAC_RX_DMA_LIST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

6.5.12. EMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: EMAC_RX_FRM_FLT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST

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			1: Receive All
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass Frames whose SA field matches SA MAC address registers 1: Pass Frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it passes the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

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6.5.13. EMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: EMAC_RX_HASH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

6.5.14. EMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: EMAC_RX_HASH1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

6.5.15. EMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved **NOTE** **MDC Clock is divided from AHB clock.**
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/W	0x0	MII_BUSY 0: Write no valid, read 0 indicates finish in read or write operation

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			1: Write start read or write operation, read 1 indicates busy.

6.5.16. EMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

6.5.17. EMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: EMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16 bits of the 1st MAC address.

6.5.18. EMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: EMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

6.5.19. EMAC MAC Address High RegisterN (Default Value: 0x0000_0000)

Offset: 0x0050+0x08*N (N=1~7)			Register Name: EMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: Used to compare with the destination address of the received frame 1: Used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of MAC address. When the bit

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			of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0x0	MAC_ADDR_HIGH The upper 16bits of the MAC address.

6.5.20. EMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x08*N (N=1~7)			Register Name: EMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32bits of MAC address N (N: 1~7).

6.5.21. EMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, When reset or disable TX DMA 001: RUN_FETCH_DESC, Fetching TX DMA descriptor 010: RUN_WAIT_STA, Waiting for the status of TX frame 011: RUN_TRANS_DATA, Passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, Closing TX descriptor 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow

6.5.22. EMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: EMAC_TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

6.5.23. EMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: EMAC_TX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit DMA buffer.

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6.5.24. EMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: EMAC_RX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, When reset or disable RX DMA 001: RUN_FETCH_DESC, Fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, Waiting for frame 100: SUSPEND, RX descriptor unavailable 101: RUN_CLOSE_DESC, Closing RX descriptor 110: Reserved 111: RUN_TRANS_DATA, Passing frame from host memory to RX DMA FIFO;

6.5.25. EMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: EMAC_RX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive descriptor

6.5.26. EMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: EMAC_RX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive DMA buffer

6.5.27. EMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: EMAC_RGMII_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface 0: down 1: up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz

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			10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

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Chapter 7 Video Output Interfaces

7.1. TCON_LCD

7.1.1. Overview

The TCON_LCD(Timing Controller_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features:

- RGB interface with DE/SYNC mode, up to 1366 x 768@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- LVDS interface with dual link, up to 1920 x 1200@60fps
- LVDS interface with single link, up to 1366 x 768@60fps
- i8080 interface, up to 800x480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

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7.1.2. Block Diagram

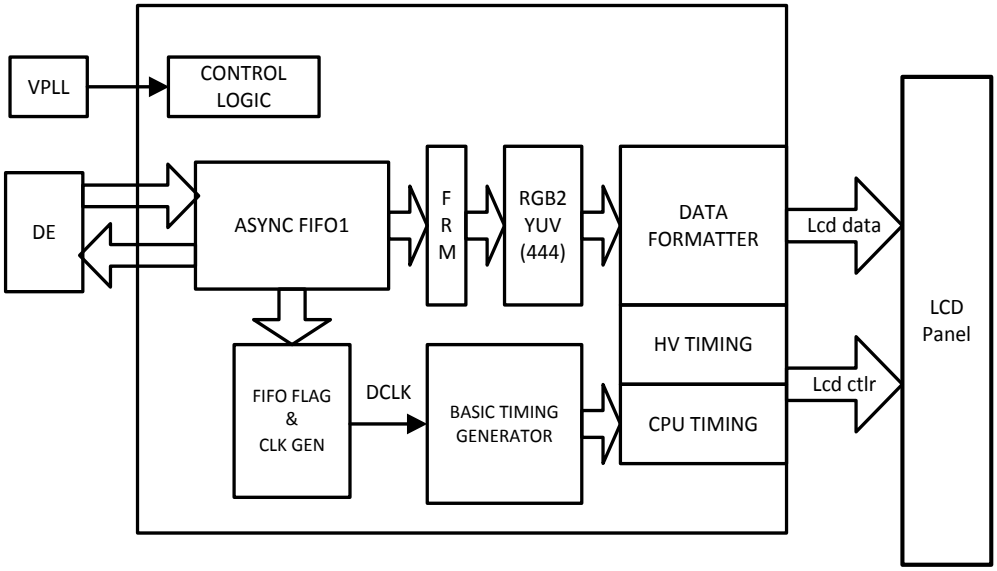

Figure 7- 1. TCON_LCD Block Diagram

7.1.3. Operations and Functional Descriptions

7.1.3.1. External Signals

The LCD external signals are used to connect to panel interface.The panel interface has various types.

7.1.3.1.1. HV Interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 application.

Table 7- 1. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

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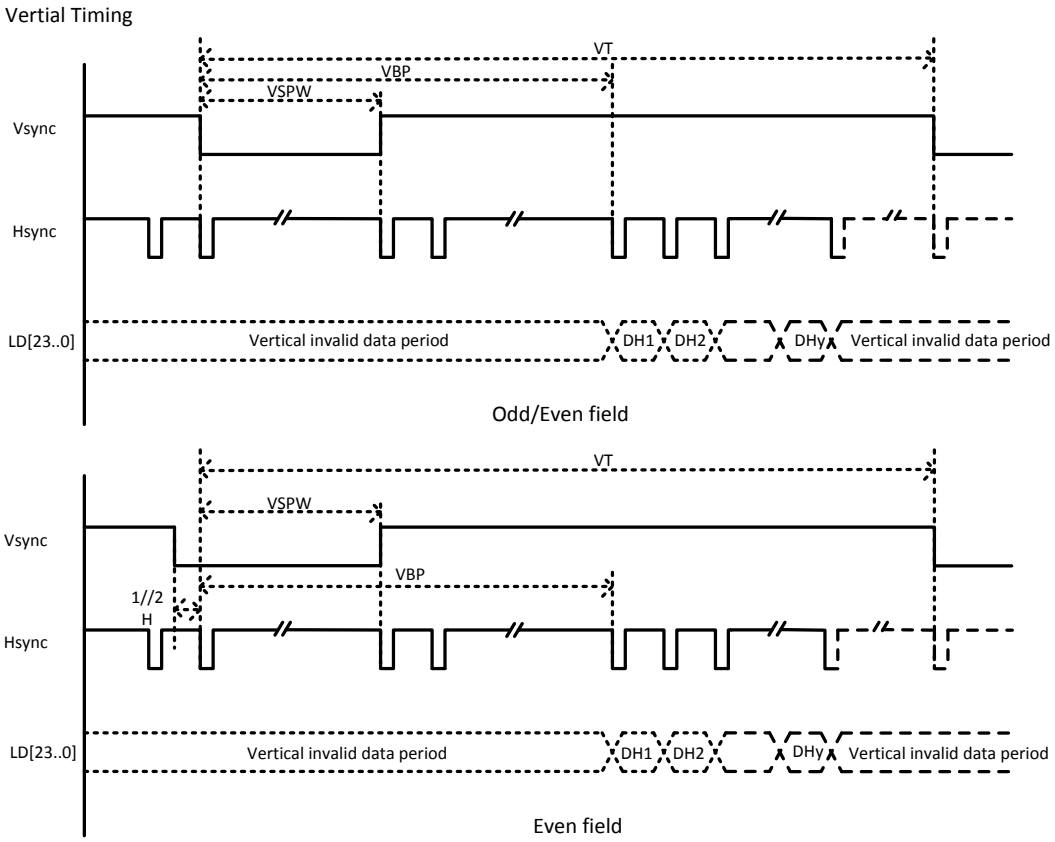

Figure 7- 2. HV Interface Vertical Timing

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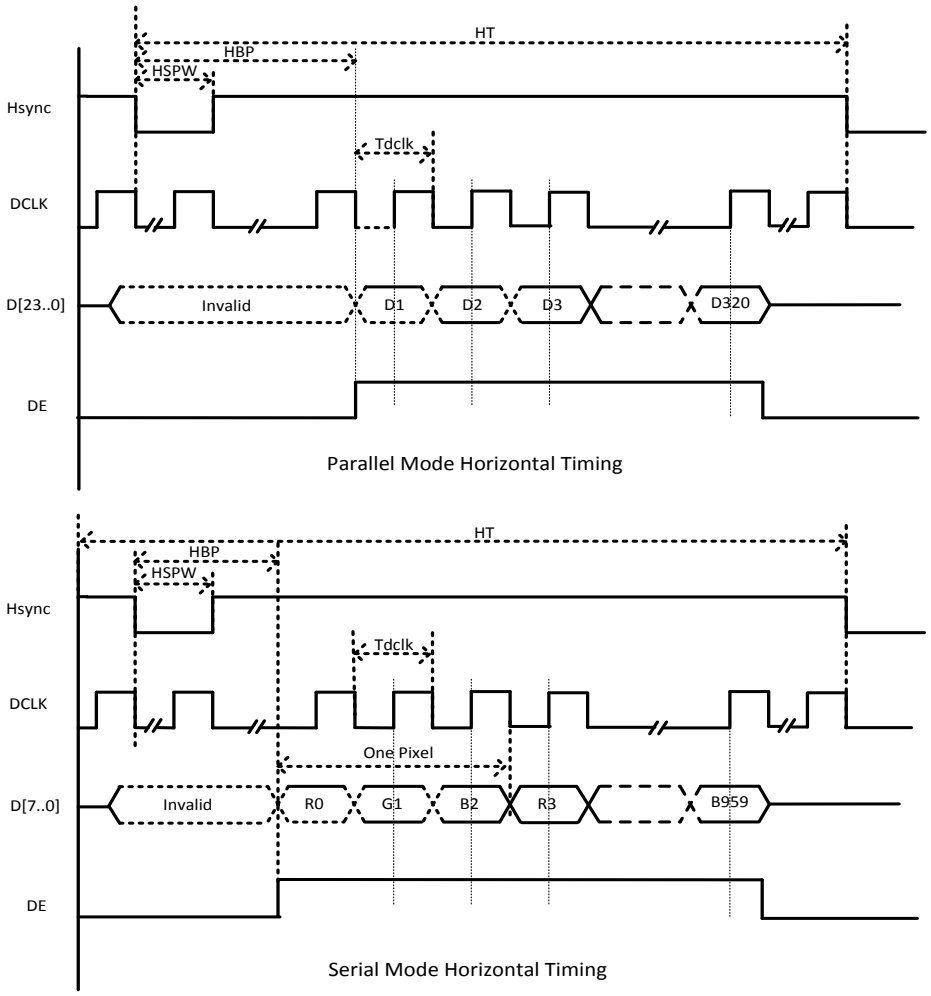

Figure 7- 3. HV Interface Horizontal Timing

7.1.3.1.2. BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 7- 2. BT656 Panel Signals

Signal	Description	Type
DCLK	Clock signal	O
DATA[7:0]	Data signal	O

Its logic is:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕H

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P2 = F ⊕H

P1 = F ⊕V

P0 = F ⊕V ⊕H

Where ⊕represents the exclusive-OR function

The 4 byte SAV/EAV sequence is as follows.

Table 7- 3. EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

7.1.3.1.3. i8080 Interface

i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels.CPU control signals are active low.

Table 7- 4. CPU Panel Signals

Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180^{o} delay of DCLK; CS is active when pixel data are valid; RD is always set to 1; A1 are set by “LCD_CPUI/F”.

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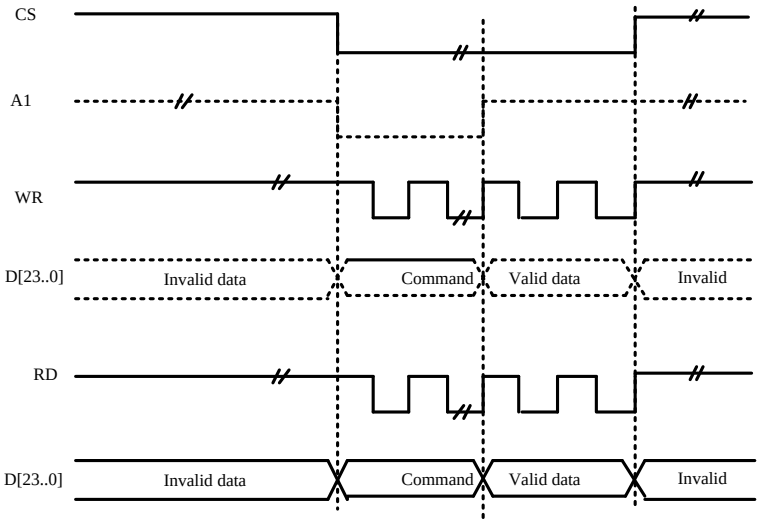

Figure 7- 4. i8080 Interface Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

7.1.3.1.4. LVDS Interface

Table 7- 5. LVDS Interface Signals

Signal	Description	Type
CKP	Positive port of clock	AO
CKN	Negative port of clock	AO
D0P	Positive port of data channel 0	AO
D0N	Negative port of data channel 0	AO
D1P	Positive port of data channel 1	AO
D1N	Negative port of data channel 1	AO
D2P	Positive port of data channel 2	AO
D2N	Negative port of data channel 2	AO
D3P	Positive port of data channel 3	AO
D3N	Negative port of data channel 3	AO

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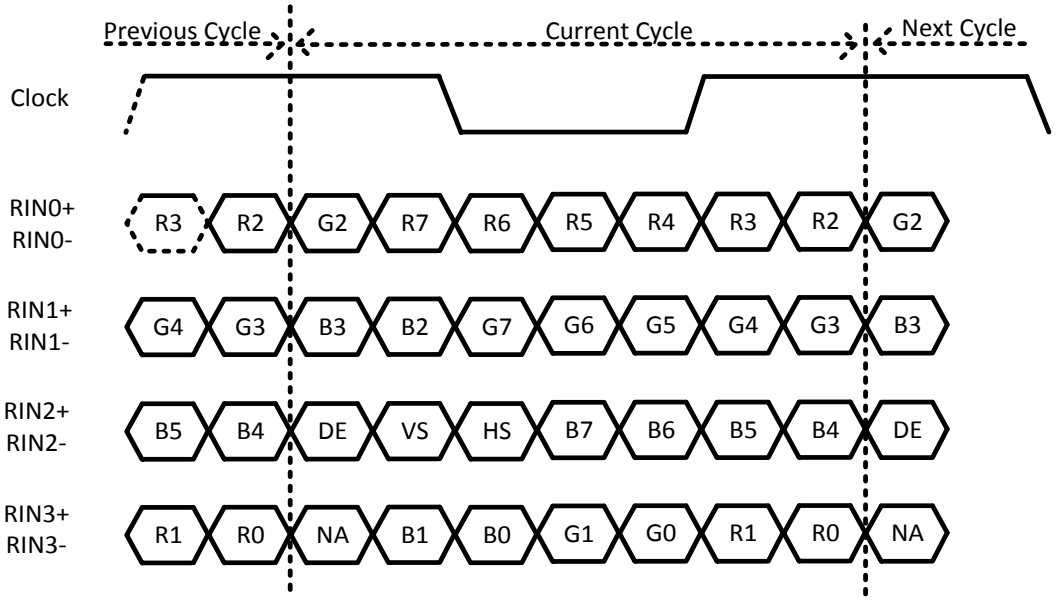

Figure 7- 5. LVDS Single Link JEDIA Mode Interface Timing

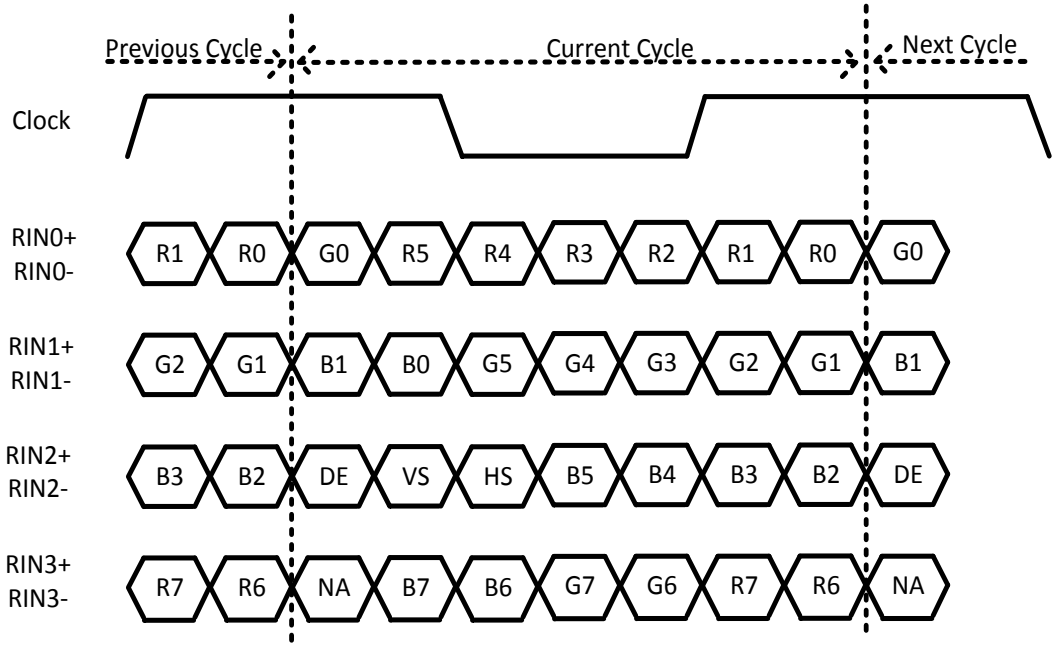

Figure 7- 6. LVDS Single Link NS Mode Interface Timing

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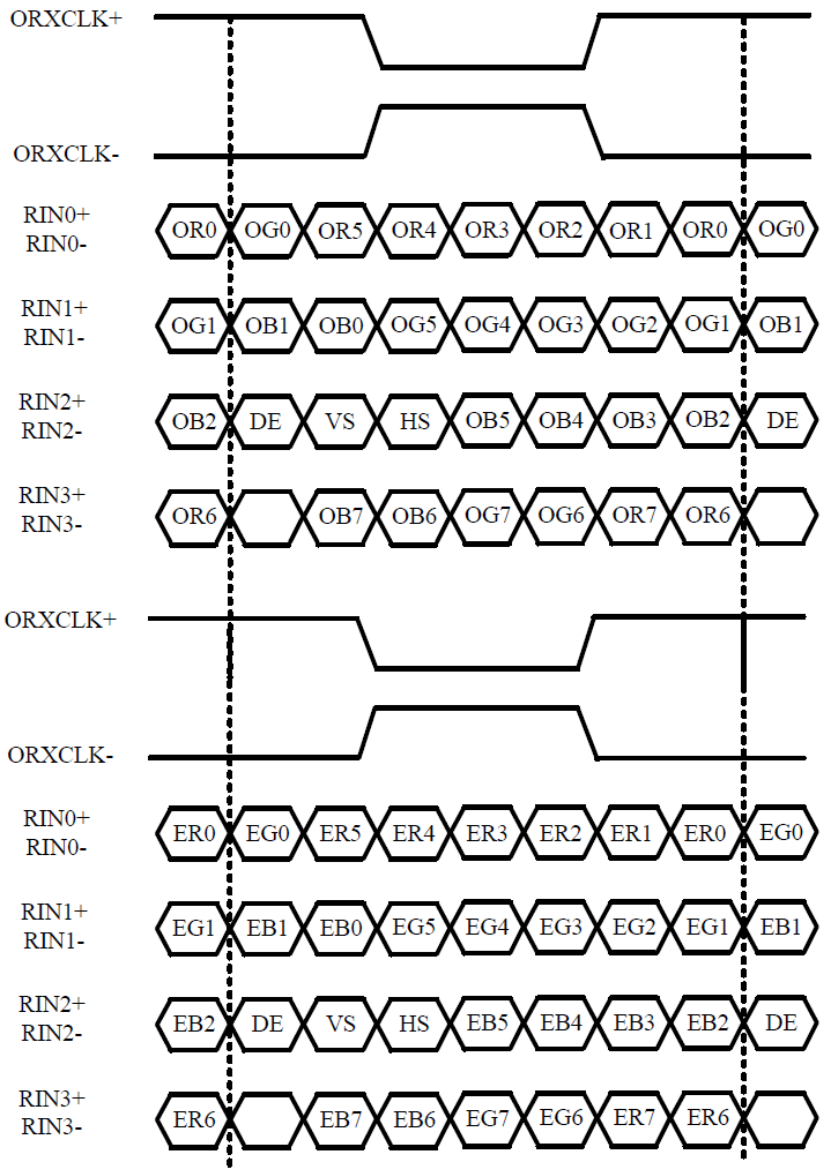

Figure 7- 7. LVDS Dual Link NS Mode Interface Timing

7.1.3.2. Clock Sources

The following table describes the clock sources of TCON_LCD. Table 7-6 describes the clock sources of TCON_LCD.

Table 7- 6. TCON_LCD Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	Video PLL Clock,default value is 297MHz
PLL_VIDEO0(2X)	Video PLL Clock,default value is 594MHz
PLL_VIDEO1(1X)	Video PLL Clock,default value is 297MHz
PLL_VIDEO1(2X)	Video PLL Clock,default value is 594MHz
PLL_MIPI	MIPI PLL Clock,default value is 594MHz

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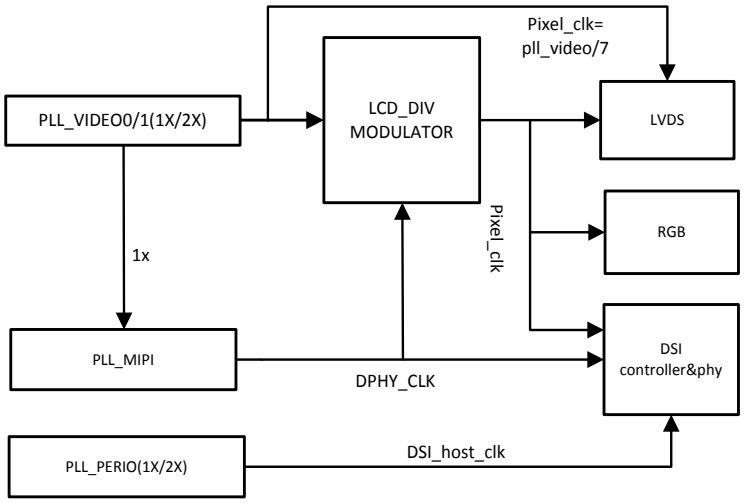

Figure 7- 8. TCON_LCD Clock System

The clock source of TCON_LCD is derived from PLL_VIDEO. The clock source of TCON_LCD(T_{sclk}) is get by configuring TCON_LCD0_CLK_REG and DISPLAY_IF_TOP_BGR_REF, then DCLK is produced by configuring the LCD_DCLK_DIV bit in TCON LCD. T_{dclk} = T_{sclk} * LCD_DCLK_DIV. For RGB interface, when the LCD_DCLK_EN bit enables dclk1&dclk2, LCD_DCLK_DIV>=6; only enables dclk, LCD_DCLK_DIV>=1. For LVDS interface, the frequency of DCLK is one-seventh of PLL_VIDEO, then LCD_DCLK_DIV = 7. Please refer to LVDS timing parameters about more details.

DCLK is a synchronous clock for pixel data. The DCLK frequency depends on the timing parameter of the LCD panel. Please refer to panel datasheet, which generally meets DCLK=Pixel_CLK=Ht*Vt*frame.

MIPI_DSI_HOST_CLK provides the clock of digital part (DSI_host_clk), PLL_MIPI provides the clock of analog PHY(DPHY_CLK). When TCON_LCD interface is DSI interface, TCON_LCD0_CLK_REG will select PLL_MIPI to provide clock at the same time.

DPHY_CLK=Ht*Vt*frame*bit_per_pixel/lane_num. To ensure that TCON Bus frequency matchs DSI data frequency, TCON DCLK >= Ht*Vt*frame. Using 4-lane DSI as an example, DPHY_CLK=Ht*Vt*frame*24/4, then TCON DCLK>=DPHY_CLK/6, LCD_DCLK_DIV can be set to 4.

7.1.3.3. RGB Gamma Correction

Function: This module correct the RGB input data of DE.
A 256*8*3 Byte register file is used to store the gamma table. The following is the layout.

Table 7- 7. RGB Gamma Correction Table

Offset	Value
0x400, 0x401, 0x402	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....

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0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.1.3.4. CEU Module

This module enhances color data from DE .

R’ = ((Rr*R + Rg*G + Rb*B +16)/16+ Rc+16)/16

G’ = ((Gr*R + Gg*G + Gb*B +16)/16+Gc+16)/16

B’ = ((Br*R + Bg*G + Bb*B +16)/16+ Bc+16)/16

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb s13 (-16,16)

Rc, Gc, Bc s19 (-16384, 16384)

R, G, B u8 [0-255]

R’ have the range of [Rmin ,Rmax]

G’ have the range of [Rmin ,Rmax]

B’ have the range of [Rmin ,Rmax]

7.1.3.5. CMAP Module

Function: This module map color data from DE.

Every 4 input pixels as a unit. A unit is divided into 12 bytes. Output byte can select one of those 12 bytes.Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).

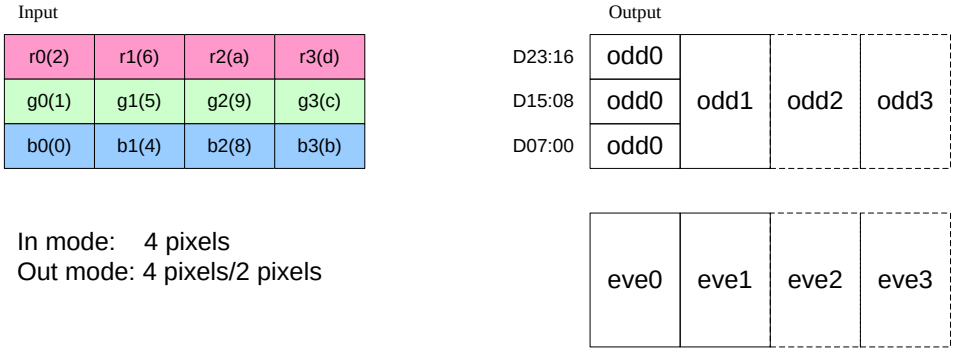

Figure 7- 9. CMAP Module

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7.1.4. Programming Guidelines

7.1.4.1. HV Mode Configuration Process

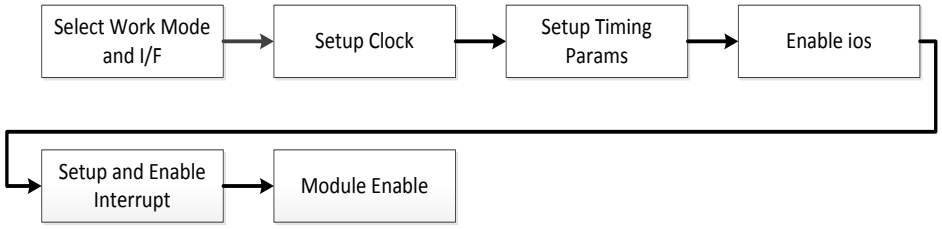

Figure 7- 10. HV Mode Initial Process

Step1: Select HV interface type: parallel RGB or serial RGB.

Step2: Set clock, if phase changing function need be used, then the bit[31:28] of **LCD_DCLK_REG** should be set to 0xf.

Step3: Set timing parameter x, ht,hbp,hspw,y,vt,vbp,vspw. Note that hbp includes hspw,vbp includes vspw, and vt need be set to twice as actual value.

Step4: Open IO output.

Step5: Set and open interrupt function.Note that when using line interrupt, the **LCD_LINE_INT_NUM** bit of **LCD_GINT1_REG** need be set first,then **LCD_LINE_INT_EN** bit of **LCD_GINT0_REG** is set to 1.

Step6: Open module enable.

7.1.4.2. LVDS Configuration Process

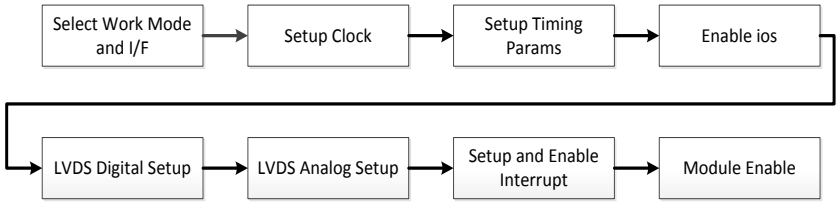

Figure 7- 11. LVDS Mode Initial Process

Step closes to HV mode, the Step1 is to select parallel RGB interface type, and to increase LVDS digital part and analog part configurations. Select digital control part before configuring LVDS analog part, then this circuit can determine the routing automatically, such as using TCON_LCD to drive dual link LVDS, should first configure LVDS_EN and dual link choice , then analog setting.

LVDS Digital Setup: choose single link or dual link mode, NS mode or JEDIA mode, choose an LVDS clock source, note that when choosing MIPI PLL as clock source of LVDS, the clock source of TCON_LCD also needs MIPI PLL.

LVDS Analog Setup: Set analog parameters of LVDS, open LVDS PHY power, set up the common mode voltage and differential voltage amplitude.

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7.1.4.3. i8080 Configuration Process

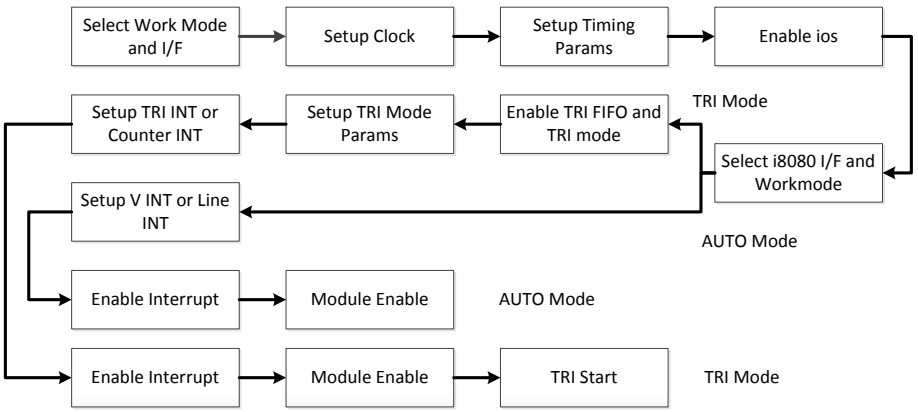

Figure 7- 12. i8080 Mode Initial Process

Step1: Select i8080 interface type.

Step2: The step is the same as HV mode,but pulse adjustment function is invalid.

Step3: The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode , or a handful of functions such as CMAP will not be able to apply.

Step4: The step is the same as HV mode.

Step5: Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------**TRI mode**----------

Step6: Open TRI FIFO switch, and TRI mode function.

Step7: Set parameters of TRI mode, including block size,block space and block number.

NOTE

When output interface is parallel mode,then the setting value of block space parameter is not less than 20.

When output interface is 2 cycle serial mode,then the setting value of block space parameter is not less than 40.

When output interface is 3 cycle serial mode,then the setting value of block space parameter is not less than 60.

When output interface is 4 cycle serial mode,then the setting value of block space parameter is not less than 80.

Step8: Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 8c register is set to "1", to open up input of pad.

Step9: Open interrupt total switch.

Step10: Open interrupt total enable.

Step11: Operate tri start operation(the bit1 of LCD_CPU_IF_REG is set to"1")

----------**Auto mode**----------

Step6: Set and open V interrupt or Line interrupt, the step is the same as HV mode.

Step7：Open module total enable.

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7.1.4.4. Notes of MIPI DSI Mode

Notes of using MIPI DSI mode :

(1) Using DSI display, data clk of TCON_LCD should start first.

(2) When using TCON_LCD in conjunction with DSI video mode,the block space parameter should satisfy the following relationship:

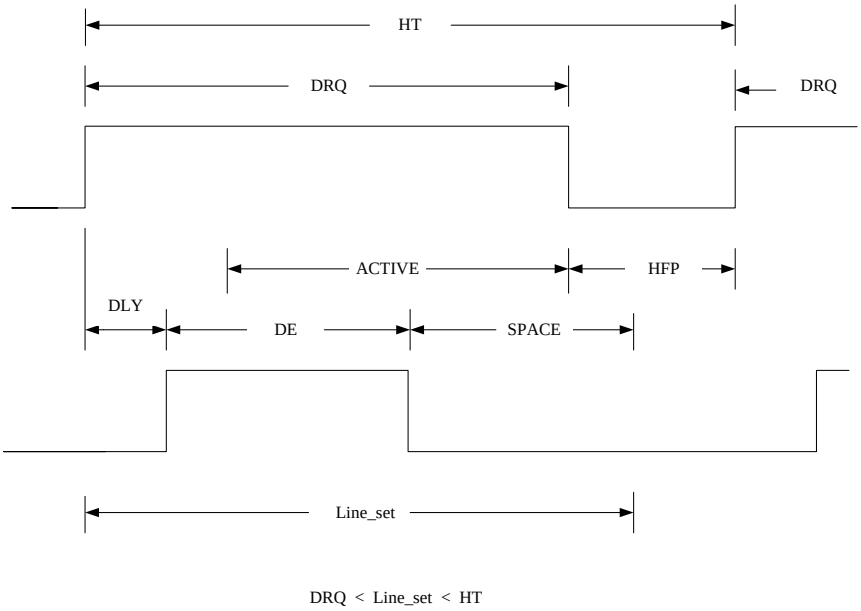

Figure 7- 13. DSI Video Mode Data Request Timing

7.1.5. Register List

Module Name	Base Address
TCON_LCD0	0x06511000
TCON_LCD1	0x06512000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04	LCD FRM Seed Register(N=0,1,2,3,4,5)
LCD_FRM_TAB_REG	0x002C+N*0x04	LCD FRM Table Register(N=0,1,2,3)
LCD_3D_FIFO_REG	0x003C	LCD 3D FIFO Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2

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LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1
LCD_LVDS_IF_REG	0x0084	LCD LVDS IF Register
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x0110+N*0x04	LCD CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10	LCD CEU Coefficient Register1(N=0,1,2)
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04	LCD CEU Coefficient Register2(N=0,1,2)
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x0180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x0190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x0194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x0198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x019C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register
LCD_LVDS_ANA_REG0	0x0220	LCD LVDS Analog Register0
LCD_LVDS_ANA_REG1	0x0224	LCD LVDS Analog Register1

7.1.6. Register Description

7.1.6.1. LCD Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: LCD_GCTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	LCD_GAMMA_EN 0: Disable 1: Enable Enable the Gamma correction function.

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29:0	/	/	/

7.1.6.2. LCD Global Interrupt Register0(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_VB_INT_EN 0: Disable 1: Enable Enable the Vb interrupt.
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN 0: Disable 1: Enable Enable the line interrupt.
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN 0: Disable 1: Enable Enable the trigger finish interrupt.
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN 0: Disable 1: Enable Enable the trigger counter interrupt.
25:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 matched the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when cpu trigger mode finished. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reached this value. Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when sync by DSI but not finish Write 0 to clear it.
8:0	/	/	/

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7.1.6.3. LCD Global Interrupt Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger(including inactive lines) Setting it for the specified line of trigger0. **NOTE** **SY0 is writable only when LINE_TRG0 is disabled.**
15:0	/	/	/

7.1.6.4. LCD FRM Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN 0:Disable 1:Enable Enable the dither function.
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R 0: 6-bit frm output 1: 5-bit frm output The R component output bits are in dither function.
5	R/W	0x0	LCD_FRM_MODE_G 0: 6-bit frm output 1: 5-bit frm output The G component output bits are in dither function.
4	R/W	0x0	LCD_FRM_MODE_B 0: 6-bit frm output 1: 5-bit frm output The B component output bits are in dither function.
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST 00: FRM 01: half 5-/6-bit, half FRM 10: half 8-bit, half FRM 11: half 8-bit, half 5-/6-bit Set the test mode of dither function.

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7.1.6.5. LCD FRM Seed Register(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04 (N=0,1,2,3,4,5)			Register Name: LCD_FRM_SEED_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Set the seed used in dither function. **NOTE** **Avoid setting it to 0**

7.1.6.6. LCD FRM Table Register(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0,1,2,3)			Register Name: LCD_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7f7f7777

7.1.6.7. LCD 3D FIFO Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN 0: Disable 1: Enable Enable the 3rd fifo bist test function.
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1 Only valid when 3D_FIFO_SETTING is set as 2.

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3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING 00: Bypass 01: Used as normal FIFO 10: Used as 3D interlace FIFO 11: Reserved

7.1.6.8. LCD Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable It executes at the beginning of the first blank line of LCD timing.
30:26	/	/	/
25:24	R/W	0x0	LCD_IF 00: HV(Sync+DE) 01: 8080 I/F 1x: reservd Set the interface type of LCD controller.
23	R/W	0x0	LCD_RB_SWAP 0: Default 1: Swap RED and BLUE data at FIFO1 Enable the function to swap red data and blue data in FIFO1.
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 **NOTE** **1 holding time must more than 1 DCLK**
20	R/W	0x0	LCD_INTERLACE_EN 0:Disable 1:Enable This flag is valid only when LCD_EN == 1
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DELAY The unit of delay is T_{line}. Valid only when LCD_EN == 1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL 000: DE 001: Color Check

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			010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reserved 111: Gridding Check

7.1.6.9. LCD Data Clock Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others:Reversed
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk * DCLKDIV **NOTE** **If dclk1&dclk2 used, DCLKDIV >=6. If dclk only, DCLKDIV >=1**

7.1.6.10. LCD Basic Timing Register0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	Y Panel height is Y+1

7.1.6.11. LCD Basic Timing Register1(Default Value: 0x0000_0000)

Offset: 0x004C	Register Name: LCD_BASIC1_REG

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Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation: 1) parallel: HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

7.1.6.12. LCD Basic Timing Register2(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

7.1.6.13. LCD Basic Timing Register3(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

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7.1.6.14. LCD HV Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE 0000: 24-bit/1cycle parallel mode 1000: 8-bit/3 cycle RGB serial mode(RGB888) 1010: 8-bit/4 cycle Dummy RGB(DRGB) 1011: 8-bit/4 cycle RGB Dummy(RGBD) 1100: 8-bit/2 cycle YUV serial mode(CCIR656) Set the HV mode of LCD controller.
27:26	R/W	0x0	RGB888_ODD_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at odd lines of the panel (line 1, 3, 5, 7…)
25:24	R/W	0x0	RGB888_EVEN_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at even lines of the panel (line 2, 4, 6, 8…)
23:22	R/W	0x0	YUV_SM 00: YUYV 01: YVYU 10: UYVY 11: VYUY Serial YUV mode output sequence 2-pixel-pair of every scan line
21:20	R/W	0x0	YUV EAV/SAV F LINE DELAY 00:F toggle right after active video line 01:delay 2 line(CCIR PAL) 10:delay 3 line(CCIR NTSC) 11:reserved Set the delay line mode.
19	R/W	0x0	CCIR_CSC_DIS 0: Enable 1: Disable Only valid when HV mode is “1100”. Select ‘0’ LCD convert source from RGB to YUV
18:0	/	/	/

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7.1.6.15. LCD CPU Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE 0000: 18-bit/256K mode 0010: 16-bit mode0 0100: 16-bit mode1 0110: 16-bit mode2 1000: 16-bit mode3 1010: 9-bit mode 1100: 8-bit 256K mode 1110: 8-bit 65K mode xxx1: 24-bit for DSI Set the i8080 interface work mode.
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG Status of Write Operation 0:Write operation is finishing 1:Write operation is pending
22	R	0x0	RD_FLAG Status of Read Operation 0:Read operation is finishing 1:Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode If it is 1, all the valid data during this frame are written to panel. This bit is sampled by Vsync.
16	R/W	0x0	FLUSH Direct Transfer Mode If it is enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRIGGER_FIFO_BIST_EN 0: Disable 1: Enable Entry addr is 0xFF8
2	R/W	0x0	TRIGGER_FIFO_EN

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			0:Disable 1:Enable Enable the trigger FIFO.
1	R/W1S	0x0	TRIGGER_START Write '1' to start a frame flush, writing '0' has no effect. This flag indicated frame flush is running. Sofeware must write '1' only when this flag is '0'.
0	R/W	0x0	TRIGGER_EN 0: Trigger mode disable 1: Trigger mode enable Enable trigger mode.

7.1.6.16. LCD CPU Panel Write Data Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus

7.1.6.17. LCD CPU Panel Read Data Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus

7.1.6.18. LCD CPU Panel Read Data Register1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus

7.1.6.19. LCD LVDS IF Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: LCD_LVDS_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x0	LCD_LVDS_EN 0: Disable 1: Enable Enable LVDS interface.
30	R/W	0x0	LCD_LVDS_LINK 0:Single link 1:Dual link Select work in single link mode or dual link mode.
29	R/W	0x0	LCD_LVDS_EVEN_ODD_DIR 0: Normal 1: Reverse Set the order of even field and odd field.
28	R/W	0x0	LCD_LVDS_DIR 0: Normal 1: Reverse Set the LVDS direction.
27	R/W	0x0	LCD_LVDS_MODE 0: NS mode 1: JEIDA mode Set the LVDS data mode.
26	R/W	0x0	LCD_LVDS_BITWIDTH 0: 24-bit 1: 18-bit Set the bit width of data.
25	R/W	0x0	LCD_LVDS_DEBUG_EN 0: Disable 1: Enable Enable LVDS debug function.
24	R/W	0x0	LCD_LVDS_DEBUG_MODE 0: Mode0 Random data 1: Mode1 Output CLK period=7/2 LVDS CLK period Set the output signal in debug mode.
23	R/W	0x0	LCD_LVDS_CORRECT_MODE 0: Mode0 1: Mode1 Set the LVDS correct mode.
22:21	/	/	/
20	R/W	0x0	LCD_LVDS_CLK_SEL 0: Reserved 1: LCD CLK Select the clock source of LVDS.
19:5	/	/	/
4	R/W	0x0	LCD_LVDS_CLK_POL 0: Reverse 1: Normal

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			Set the clock polarity of LVDS.
3:0	R/W	0x0	LCD_LVDS_DATA_POL 0: Reverse 1: Normal Set the data polarity of LVDS.

7.1.6.20. LCD IO Polarity Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	IO_OUTPUT_SEL 0: Normal output 1: Register output When it is set as '1', d[23:0], io0, io1,io3 sync to dclk.
30:28	R/W	0x0	DCLK_SEL 000: Used DCLK0(normal phase offset) 001: Used DCLK1(1/3 phase offset) 010: Used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 Others: Reserved Set the phase offset of clock and data in hv mode.
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert Enable invert function of IO3.
26	R/W	0x0	IO2_ INV 0: Not invert 1: Invert Enable invert function of IO2.
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert Enable invert function of IO1.
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert Enable invert function of IO0.
23:0	R/W	0x0	Data_INV 0: Normal polarity 1: Invert the specify output LCD output port D[23:0] polarity control, with independent bit control.

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7.1.6.21. LCD IO Control Register(Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN 0: Normal 1: Bits_invert Set the endian of data bits.
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO3.
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO2.
25	R/W	0x1	IO1_OUTPUR_TRI_EN 1: Disable 0: Enable Enable the output of IO1.
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO0.
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN 1: Disable 0: Enable LCD output port D[23:0] output enable, with independent bit control.

7.1.6.22. LCD Debug Register(Default Value: 0x2000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	LCD_FIFO_UNDERFLOW 0: Not underflow 1: Underflow The flag shows whether the fifo is in underflow status.
30	/	/	/
29	R	0x1	LCD_FIELD_POL 0: Second field 1: First field The flag indicates the current field polarity.

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28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line.
15:0	/	/	/

7.1.6.23. LCD CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: Bypass 1: Enable Enable CEU function.
30:0	/	/	/

7.1.6.24. LCD CEU Coefficient Register0(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb Signed 13bit value, range of (-16,16)

7.1.6.25. LCD CEU Coefficient Register1(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0: Rc N=1: Gc

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			N=2: Bc Signed 19bit value, range of (-16384, 16384)

7.1.6.26. LCD CEU Coefficient Register2(Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0,1,2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0,255]

7.1.6.27. LCD CPU Panel Trigger Register0(Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set to 20*pixel above.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block.It is usually set as X.

7.1.6.28. LCD CPU Panel Trigger Register1(Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks.It is usually set as Y.

7.1.6.29. LCD CPU Panel Trigger Register2(Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DELAY

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			Tdly = (Start_Delay +1) * De_clk*8
15	R/W	0x0	TRANS_START_MODE 0: ecc_fifo+tri_fifo 1: tri_fifo Select the FIFOs used in CPU mode.
14:13	R/W	0x0	SYNC_MODE 0x: auto 10: 0 11: 1 Set the sync mode in CPU interface.
12:0	R/W	0x0	TRANS_START_SET Usual set as the length of a line.

7.1.6.30. LCD CPU Panel Trigger Register3(Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode When it is set as 2b'01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. When it is set as 2b'10 or 2b'11, io0 is map as TE input.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor.
7:0	R/W	0x0	COUNTER_M The value of counter factor.

7.1.6.31. LCD CPU Panel Trigger Register4(Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN 0: Disable 1: Enable Enable the plug mode used in dsi command mode.
27:25	/	/	/

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24	R/W	0x0	A1 Valid in first Block.
23:0	R/W	0x0	D23-D0 Valid in first Block.

7.1.6.32. LCD CPU Panel Trigger Register5(Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	A1 Valid in Block except first
23:0	R/W	0x0	D23-D0 Valid in Block except first

7.1.6.33. LCD Color Map Control Register(Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: LCD_CMAP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN 0: Bypass 1: Enable Enable the color map function. This module only work when X is divided by 4.
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1 Set the pixel output format in color map function.

7.1.6.34. LCD Color Map Odd Line Register0(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0

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			0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.35. LCD Color Map Odd Line Register1(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3 bit15-12: Reserved

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			bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

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7.1.6.36. LCD Color Map Even Line Register0(Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3

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			1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.37. LCD Color Map Even Line Register1(Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2

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			1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.38. LCD Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time,LCD controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line Select the safe mode.

7.1.6.39. LCD LVDS0 Analog Register(Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: LCD_LVDS0_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LVDS0_EN_MB Enable the bias circuit of the LVDS0_ANA module. 0: Disable 1: Enable
30	R/W	0x0	LVDS0_EN_LDO Enable the LDO circuit of the LVDS0_ANA module. 0: Disable 1: Enable
29:25	/	/	/

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24	R/W	0x0	LVDS0_EN_DRVC Enable Clock Channel Drive 0: Disable 1: Enable Enable all circuits working when transmitting the data in channel clock of LVDS_TX0.
23:20	R/W	0x0	LVDS0_EN_DRV Enable Data Channel[3:0] Drive 0: Disable 1: Enable Enable all circuits working when transmitting the data in channel<3:0> of LVDS_TX0.
19	R/W	0x0	LVDS0_REG_DRAM_TEST 0:Dram test clk disable 1:Dram test clk enable Enable LVDS debug function to output dram clock.
18:17	R/W	0x0	LVDS0_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 00:250mV 01:300mV 10:350mV 11:400mV
16	R/W	0x0	LVDS0_REG_DENC Choose data output or PLL test clock output in LVDS_TX.
15:12	R/W	0x0	LVDS0_REG_DEN Choose data output or PLL test clock output in LVDS_TX.
11:10	/	/	/
9:8	R/W	0x0	LVDS0_REG_V Adjust common mode voltage of the differential signals in five channels. Single signal high level: 00:1.1V 01:1.19V 10:1.3V 11:1.43V
7:6	/	/	/
5:4	R/W	0x0	LVDS0_REG_PD Adjust the slew rate of output data.
3:2	/	/	/
1	R/W	0x0	LVDS0_REG_PWSLV Adjust voltage amplitude of low power in LVDS_ANA.
0	R/W	0x0	LVDS0_REG_PWSMB Adjust voltage amplitude of mbias voltage reference in LVDS_ANA.

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7.1.6.40. LCD LVDS1 Analog Register(Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: LCD_LVDS1_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LVDS1_EN_MB Enable the bias circuit of the LVDS1_ANA module. 0: Disable 1: Enable
30	R/W	0x0	LVDS1_EN_LDO Enable the LDO circuit of the LVDS1_ANA module. 0: Disable 1: Enable
29:25	/	/	/
24	R/W	0x0	LVDS1_EN_DRVC Enable Clock Channel Drive 0: Disable 1: Enable Enable all circuits working when transmitting the data in channel clock of LVDS_TX0.
23:20	R/W	0x0	LVDS1_EN_DRV Enable Data Channel[3:0] Drive 0: Disable 1: Enable Enable all circuits working when transmitting the data in channel<3:0> of LVDS_TX0.
19	R/W	0x0	LVDS1_REG_DRAM_TEST 0:Dram test clk disable 1:Dram test clk enable Enable LVDS debug function to output dram clock.
18:17	R/W	0x0	LVDS1_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude. 00:250mV 01:300mV 10:350mV 11:400mV
16	R/W	0x0	LVDS1_REG_DENC Choose data output or PLL test clock output in LVDS_TX.
15:12	R/W	0x0	LVDS1_REG_DEN Choose data output or PLL test clock output in LVDS_TX.
11:10	/	/	/
9:8	R/W	0x0	LVDS1_REG_V Adjust common mode voltage of the differential signals in five channels. Single signal high level: 00:1.1V

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			01:1.19V 10:1.3V 11:1.43V
7:6	/	/	/
5:4	R/W	0x0	LVDS1_REG_PD Adjust the slew rate of output data.
3:2	/	/	/
1	R/W	0x0	LVDS1_REG_PWSLV Adjust voltage amplitude of low power in LVDS_ANA.
0	R/W	0x0	LVDS1_REG_PWSMB Adjust voltage amplitude of mbias voltage reference in LVDS_ANA.

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7.2. TCON_TV

7.2.1. Overview

The TCON_TV(Timing Controller_TV) is a module that processes video signals received from systems using a complicated arithmetic and then generates control signals and transmits them to the HDMI or TVE.

The TCON_TV includes the following features:

- Supports Gamma correction with R/G/B channel independence

7.2.2. Block Diagram

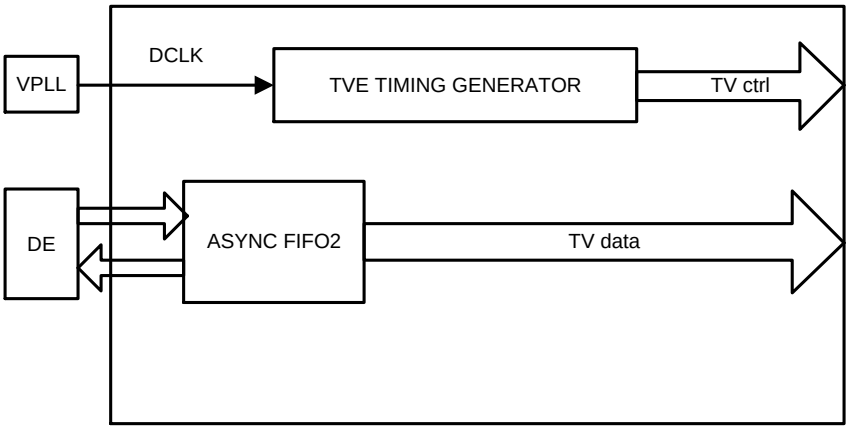

Figure 7- 14. TCON_TV Block Diagram

7.2.3. Operations and Functional Descriptions

7.2.3.1. Panel Interface

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.Its signals are defined as:

Table 7- 8. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O

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LD[23..0]	24Bit RGB/YUV output from input FIFO for panel	O

HV control signals are active low.

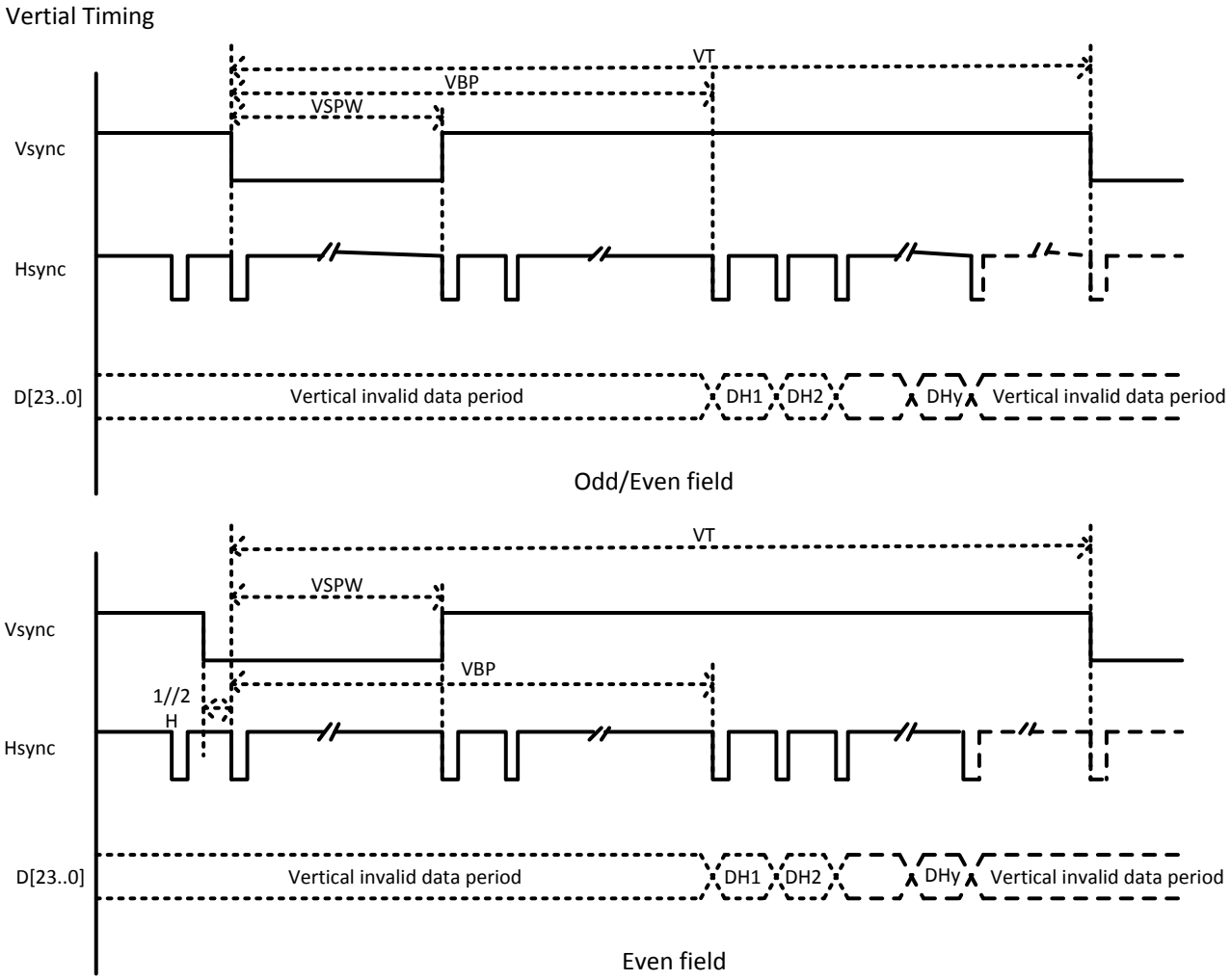

Figure 7- 15. HV Interface Vertical Timing

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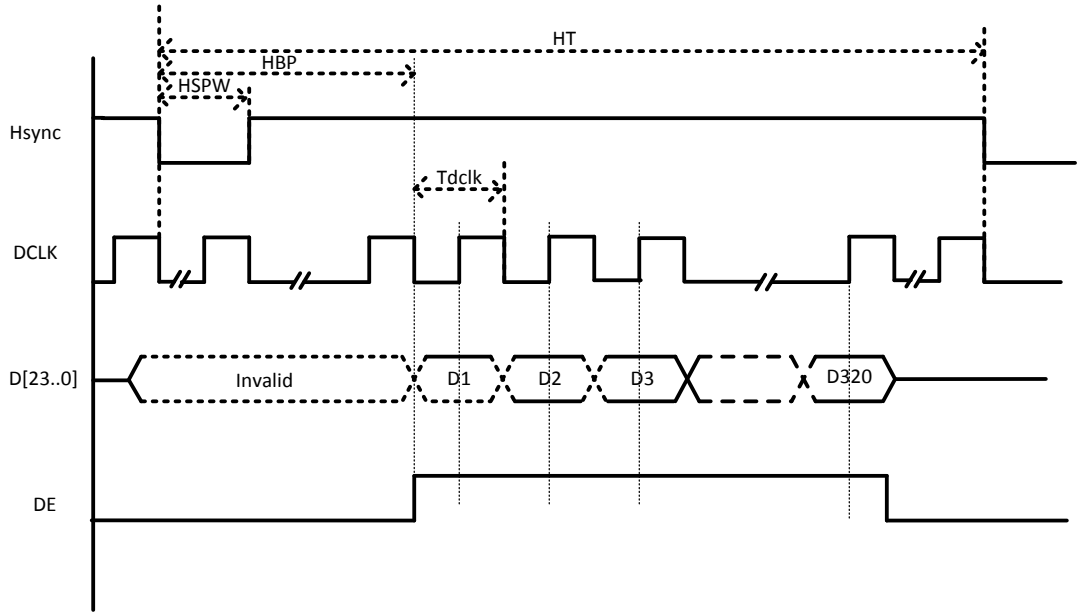

Figure 7- 16. HV Interface Horizontal Timing

7.2.3.2. Clock Sources

The following table describes the clock sources of TCON_TV. Table 7-9 describes the clock sources of TCON_TV.

Table 7- 9. TCON_TV Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	Video PLL Clock,default value is 297MHz
PLL_VIDEO0(2X)	Video PLL Clock,default value is 594MHz
PLL_VIDEO1(1X)	Video PLL Clock,default value is 297MHz
PLL_VIDEO1(2X)	Video PLL Clock,default value is 594MHz

The clock system of TCON_TV is as follows.

Figure 7- 17. TCON_TV Clock System

TCON_TV_CLK is produced by internal frequency division. If deflick function is enabled, TCON_TV_CLK is one-eighth of TVE_CLK; if deflick function is disabled, TCON_TV_CLK is one-sixteenth of TVE_CLK.

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7.2.3.3. RGB Gamma Correction

This module corrects the RGB input data of DE .

A 256*8*3 Byte register file is used to store the gamma table. The following is the layout.

Table 7- 10. RGB Gamma Correction Table

Offset	Value
0x400	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.2.3.4. CEU Module

This module enhances color data from DE .

R’ = ((Rr*R + Rg*G + Rb*B +16)/16+ Rc+16)/16

G’ = ((Gr*R + Gg*G + Gb*B +16)/16+Gc+16)/16

B’ = ((Br*R + Bg*G + Bb*B +16)/16+ Bc+16)/16

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb	**s13**	**(-16,16)**
Rc, Gc, Bc	**s19**	**(-16384, 16384)**
R, G, B	**u8**	**[0-255]**

R’ have the range of [Rmin ,Rmax]

G’ have the range of [Rmin ,Rmax]

B’ have the range of [Rmin ,Rmax]

7.2.4. Programming Guidelines

7.2.4.1. TCON_TV Configuration Process

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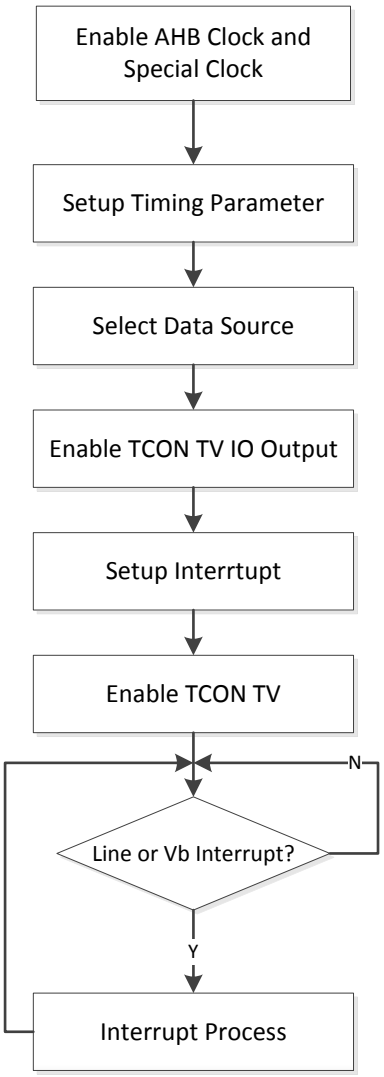

Figure 7- 18. TCON TV Initial Process

Step1: Set special clock of CCU ,and dessert TCON TV related AHB clock gating and AHB reset .

Step2: Set timing parameter register of TCON TV, set corresponding resolution and standards followed, such as EIA or VESA.There are 8 parameters, including X,HT,HBP,HSPW,Y,VT,VBP,VSPW. Note that for the controller,HBP includes HSPW width, VBP includes VSPW width, this is different with standard HBP and VBP.Note that for conversion.

Step3: Select TCON TV data sources. For the selecting of TCON TV data sources, it is decided by two setting. The first setting is the bit1(TV_SRC_SEL_GOBAL) of **TV_CTL_REG**, if setting to 1,then blue data is output; if setting to 0, then data source is decided by **TV0_SRC_CTL_REG**. According to needs, set up TV_SRC_SEL, select the required data sources.

Step4: The register offset of **TCON TV IO Output Function Setting** is 0x8c, writing 0 to the register open output function.

Step5: Set and open interrupt. When using line interrupt, firstly the TV_LINE_INT_NUM bit of **TV_GINT1** need be set, secondly line interrupt is enabled, that is , the bit 28(TV_LINE_INT_EN) of **TV_GINT0** is set to 1.

Step6: Start TCON TV.

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7.2.4.2. 3D Mode Notes

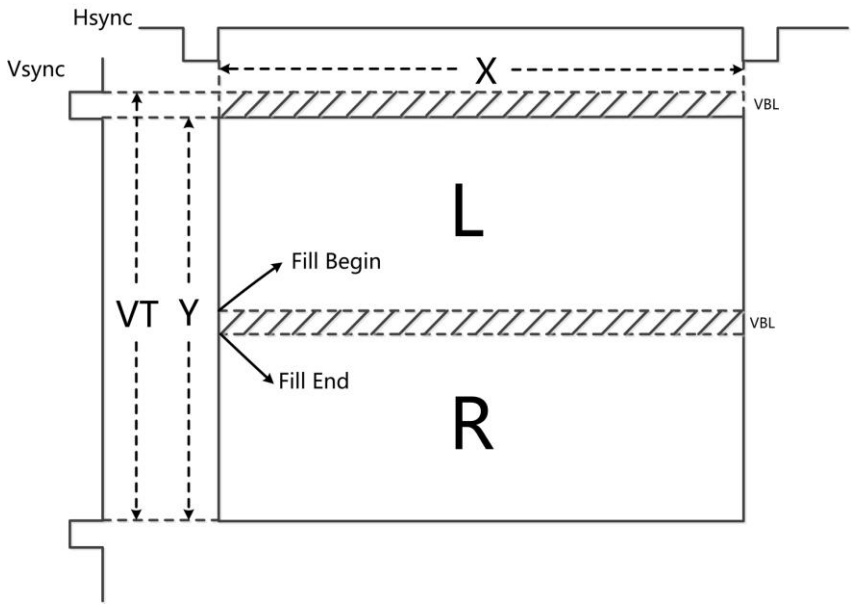

Figure 7- 19. TCON TV 3D Mode Diagram

As shown in the above figure, VT= $VBL_L + Y_L + VBL_R + Y_R$, Y = $Y_L + VBL_R + Y_R$. But note that VT in this picture is the actual VT, is the half of VT in register.

In 3D mode, the 2 frames is synthesized into 1 frame to send data, so the effective data area will contain a blank area, this blank need be filled, and generally filled 0. The rest is to confirm the beginning and the end line of padding, the formula is as follows:

L_{begin} = VT/2 + 1, L_{end}=VT/2+(VT-Y)/2

Lastly, write L_{begin} to the bit[23:12] of **TV_FILL_BEGIN_REG0**(0x304), write L_{end} to the bit[23:12] of **TV_FILL_END_RGB0**(0x308), write 0 to **TV_FILL_DATA_REG0**(0x30C).

7.2.5. Register List

Module Name	Base Address
TCON_TV0	0x06515000

Register Name	Offset	Description
TV_GCTL_REG	0x0000	TV Global Control Register
TV_GINT0_REG	0x0004	TV Global Interrupt Register0
TV_GINT1_REG	0x0008	TV Global Interrupt Register1
TV_SRC_CTL_REG	0x0040	TV Source Control Register
TV_IO_POL_REG	0x0088	TV IO Polarity Register
TV_IO_TRI_REG	0x008C	TV IO Control Register
TV_CTL_REG	0x0090	TV Control Register
TV_BASIC0_REG	0x0094	TV Basic Timing Register0

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TV_BASIC1_REG	0x0098	TV Basic Timing Register1
TV_BASIC2_REG	0x009C	TV Basic Timing Register2
TV_BASIC3_REG	0x00A0	TV Basic Timing Register3
TV_BASIC4_REG	0x00A4	TV Basic Timing Register4
TV_BASIC5_REG	0x00A8	TV Basic Timing Register5
TV_ECC_FIFO_REG	0x00F8	TV ECC FIFO Register
TV_DEBUG_REG	0x00FC	TV Debug Register
TV_CEU_CTL_REG	0x0100	TV CEU Control Register
TV_CEU_COEF_MUL_REG	0x0110+N*0x04	TV CEU Coefficient Register0(N=0,1,2,4,5,6,8,9,10)
TV_CEU_COEF_ADD_REG	0x011C+N*0x10	TV CEU coefficient register1(N=0,1,2)
TV_CEU_COEF_RANG_REG	0x0140+N*0x04	TV CEU Coefficient Register2(N=0,1,2)
TV_SAFE_PERIOD_REG	0x01F0	TV Safe Period Register
TV_FILL_CTL_REG	0x0300	TV Fill Data Control Register
TV_FILL_BEGIN_REG0	0x0304	TV Fill Data Begin Register0
TV_FILL_END_REG0	0x0308	TV Fill Data End Register0
TV_FILL_DATA_REG0	0x030C	TV Fill Data Value Register0
TV_FILL_BEGIN_REG1	0x0310	TV Fill Data Begin Register1
TV_FILL_END_REG1	0x0314	TV Fill Data End Register1
TV_FILL_DATA_REG1	0x0318	TV Fill Data Value Register1
TV_FILL_BEGIN_REG2	0x031C	TV Fill Data Begin Register2
TV_FILL_END_REG2	0x0320	TV Fill Data End Register2
TV_FILL_DATA_REG2	0x0324	TV Fill Data Value Register2

7.2.6. Registers Description

7.2.6.1. TV Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: TV_GCTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	TV_GAMMA_EN 0: Disable 1: Enable Enable the Gamma correction function.
29:0	/	/	/

7.2.6.2. TV Global Interrupt Register0(Default Value: 0x0000_0000)

Offset: 0x0004	**Register Name: TV_GINT0_REG**

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Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	TV_VB_INT_EN 0: Disable 1: Enable Enable the Vb interrupt.
29	/	/	/
28	R/W	0x0	TV_LINE_INT_EN 0: Disable 1: Enable Enable the line interrupt.
27:15	/	/	/
14	R/W	0x0	TV_VB_INT_FLAG Assert during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TV_LINT_INT_FLAG Trigger when SY1 match the current TV scan line Write 0 to clear it.
11:0	/	/	/

7.2.6.3. TV Global Interrupt Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TV_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	TV_LINE_INT_NUM Scan line for TV line trigger(including inactive lines) Setting it for the specified line of trigger 1. **NOTE** **SY1 is writable only when LINE_TRG1 is disabled.**

7.2.6.4. TV Source Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TV_SRC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	TV_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check

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			011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

7.2.6.5. TV IO Polarity Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TV_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert Enable invert function of IO3.
26	R/W	0x0	IO2_ INV 0: Not invert 1: Invert Enable invert function of IO2.
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert Enable invert function of IO1.
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert Enable invert function of IO0.
23:0	R/W	0x0	Data_INV 0: Normal polarity 1: Invert the specify output LCD output port D[23:0] polarity control, with independent bit control.

7.2.6.6. TV IO Control Register(Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: TV_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO3.
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable

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			0: Enable Enable the output of IO2.
25	R/W	0x1	IO1_OUTPUR_TRI_EN 1: Disable 0: Enable Enable the output of IO1.
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO0.
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN 1: Disable 0: Enable TV output port D[23:0] output enable, with independent bit control.

7.2.6.7. TV Control Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TV_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_EN 0: Disable 1: Enable
30:9	/	/	/
8:4	R/W	0x0	START_DELAY This is for DE.
3:2	/	/	/
1	R/W	0x0	TV_SRC_SEL_GOBAL 0: reserved 1: BLUE data(FIFO2 disable, RGB=0000FF) **NOTE** **The priority of this bit is higher than TV_SRC_SEL(bit[2:0]) in TV_SRC_CTL_REG.**
0	/	/	/

7.2.6.8. TV Basic Timing Register0(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: TV_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	XI source width is X+1

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15:12	/	/	/
11:0	R/W	0x0	YI source height is Y+1

7.2.6.9. TV Basic Timing Register1(Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TV_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO Width is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO Width is LS_YO+1 **NOTE** **LS_YO = TV_YI**

7.2.6.10. TV Basic Timing Register2(Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TV_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TV_XO Width is TV_XO+1
15:12	/	/	/
11:0	R/W	0x0	TV_YO Height is TV_YO+1

7.2.6.11. TV Basic Timing Register3(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TV_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Horizontal total time T_{hcycle} = (HT+1) * T_{hdclk}
15:12	/	/	/
11:0	R/W	0x0	HBP Horizontal back porch T_{hbp} = (HBP +1) * T_{hdclk}

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7.2.6.12. TV Basic Timing Register4(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TV_BASIC4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT Vertical total time (in HD line) T_{vt} = VT/2 * T_h
15:12	/	/	/
11:0	R/W	0x0	VBP Vertical back porch (in HD line) T_{vbp} = (VBP +1) * T_h

7.2.6.13. TV Basic Timing Register5(Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TV_BASIC5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Horizontal Sync Pulse Width (in dclk) T_{hspw} = (HSPW+1) * T_{dclk} HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Vertical Sync Pulse Width (in lines) T_{vspw} = (VSPW+1) * T_h VT/2 > (VSPW+1)

7.2.6.14. TV ECC FIFO Register(Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: TV_ECC_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ECC_FIFO_BIST_EN 0: Disable 1: Enable Enable ECC FIFO BIST test function.
30	R	0x0	ECC_FIFO_ERR_FLAG Indicates the error information in ECC FIFO.
29:24	/	/	/
23:16	R	0x0	ECC_FIFO_ERR_BITS

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			Indicates the error information in ECC FIFO.
15:9	/	/	/
8	R/W	0x0	ECC_FIFO_BLANK_EN 0: Disable ECC function in blanking 1: Enable ECC function in blanking ECC function is tent to trigger in blanking area at HV mode, set '0' when in HV mode.
7:4	/	/	/
3	R/W	0x0	ECC_FIFO_SETTING 0:Enable 1:Disable Enable ECC FIFO function.
2:0	/	/	/

7.2.6.15. TV Debug Register(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TV_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	TV_FIFO_UNDERFLOW 0: Not underflow 1: Underflow The flag shows whether the FIFOs in underflow status.
29	/	/	/
28	R	0x0	TV_FIELD_POL 0: Second field 1: First field The flag indicates the current field polarity.
27:12	/	/	/
13	R/W	0x0	ECC_FIFO_BYPASS 0: Used 1: Bypass Setup that whether to bypass ECC FIFO.
12	/	/	/
11:0	R	0x0	TV_CURRENT_LINE Current scan line.

7.2.6.16. TV CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TV_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN

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			0: Bypass 1: Enable Enable CEU function.
30:0	/	/	/

7.2.6.17. TV CEU Coefficient Register0(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TV_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb Signed 13-bit value, range of (-16,16).

7.2.6.18. TV CEU Coefficient Register1(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: TV_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0: Rc N=1: Gc N=2: Bc Signed 19-bit value, range of (-16384, 16384).

7.2.6.19. TV CEU Coefficient Register2(Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0,1,2)			Register Name: TV_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0,255]

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15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0,255]

7.2.6.20. TV Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TV_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM,LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time,LCD controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line Select the save mode.

7.2.6.21. TV Fill Data Control Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TV_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TV_FILL_EN 0: Bypass 1: Enable Enable the fill data function in blanking area.This is only used in HDMI 3D mode.
30:0	/	/	/

7.2.6.22. TV Fill Data Begin Register0(Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: TV_FILL_BEGIN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

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23:0	R/W	0x0	FILL_BEGIN Set the begin point of the fill data area.

7.2.6.23. TV Fill Data End Register0(Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: TV_FILL_END_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Set the end point of the fill data area.

7.2.6.24. TV Fill Data Value Register0(Default Value: 0x0000_0000)

Offset: 0x030C			Register Name: TV_FILL_DATA_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE Set the data value which is used to fill into the blanking area between two frames in HDMI 3D mode.

7.2.6.25. TV Fill Data Begin Register1(Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: TV_FILL_BEGIN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN Set the begin point of the fill data area.

7.2.6.26. TV Fill Data End Register1(Default Value: 0x0000_0000)

Offset: 0x314			Register Name: TV_FILL_END_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Set the end point of the fill data area.

7.2.6.27. TV Fill Data Value Register1(Default Value: 0x0000_0000)

Offset: 0x0318	Register Name: TV_FILL_DATA_REG1

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Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	0x0	FILL_VALUE Set the data value which is used to fill into the blanking area between two frames in HDMI 3D mode.

7.2.6.28. TV Fill Data Begin Register2(Default Value: 0x0000_0000)

Offset: 0x031C			Register Name: TV_FILL_BEGIN_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN Set the begin point of the fill data area.

7.2.6.29. TV Fill Data End Register2(Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: TV_FILL_END_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END Set the end point of the fill data area.

7.2.6.30. TV Fill Data Value Register2(Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: TV_FILL_DATA_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_VALUE Set the data value which is used to fill into the blanking area between two frames in HDMI 3D mode.

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7.3. MIPI DSI

7.3.1. Overview

The MIPI Display Serial Interface(DSI) is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces.This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.01 and a D-PHY module which is compliance with MIPI DPHY specification V1.00.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI v1.01
- 1/2/3/4 data lanes configuration and up to 1Gbit/s per lane
- Supports video mode with sync pulse/sync event,burst mode and command mode
- Pixel format: RGB888, RGB666, RGB666 packed, and RGB565
- Supports MIPI DCS, bidirectional configuration in LP
- Supports HS-TX, LP-TX, LP-RX,LP-CD compliance with D-PHY v1.00
- Supports turn around mode
- Supports low power data transmission
- Supports ULPS and Reset-Trigger in escape mode

7.3.2. Block Diagram

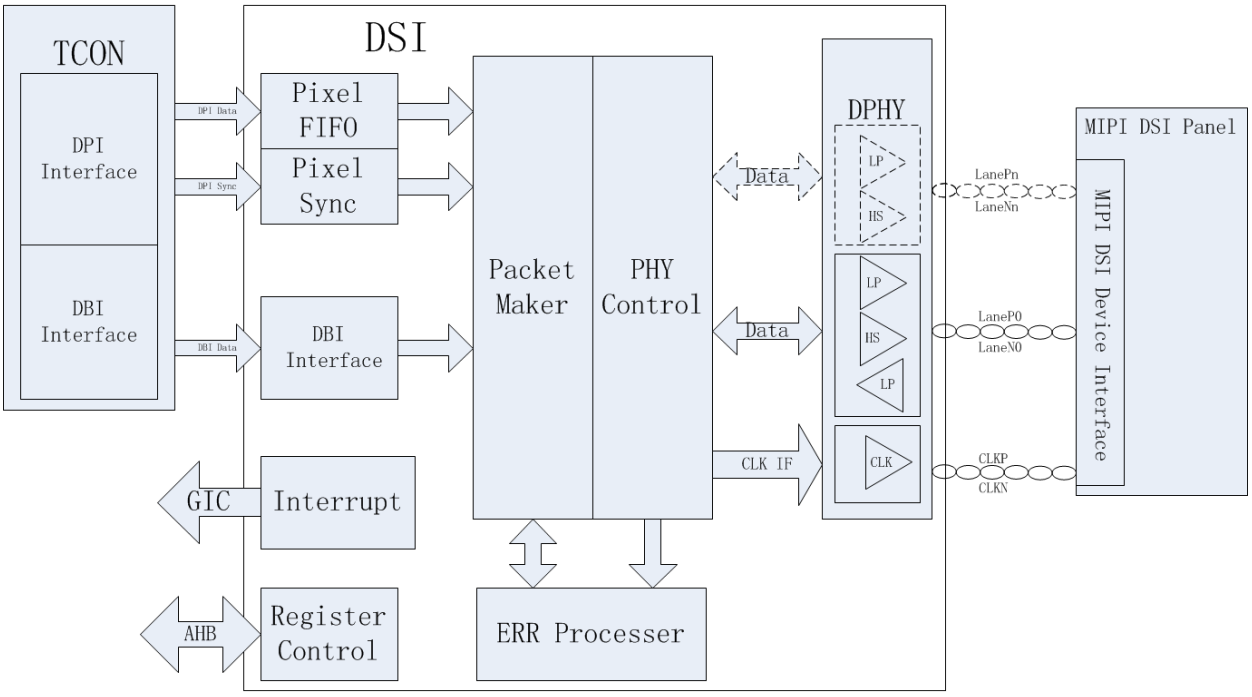

Figure 7- 20. MIPI DSI System Block Diagram

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TCON is connected with DSI Controller through DPI and DBI. Packet Maker transforms pixel data of TCON into data packets, according to a designated mode(video mode with sync pulse/video mode with sync event/burst mode/command mode). PHY Control distributes data packets into every lane, and starts aligned fill operation. When data packets arrive at DPHY, they start to serialize, then they are sent into sink end. ERR processor monitors the whole process, if there is a mistake, the corresponding state position is set to “1”.

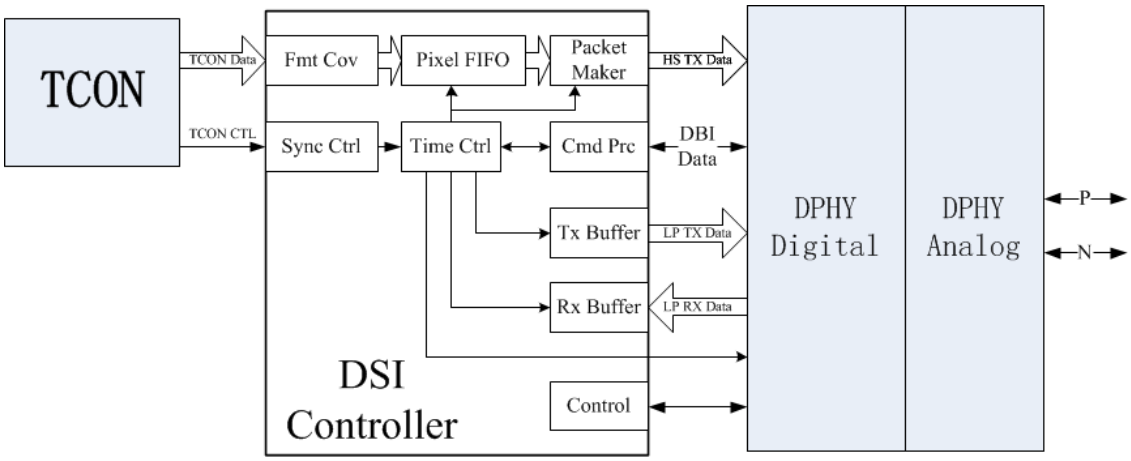

Figure 7- 21. MIPI DSI Internal Unit

TCON synchronous signals come into DSI Controller, and input into Time Ctrl. According to TCON synchronous signals, Time Ctrl controls and drives every sub module’s operation.

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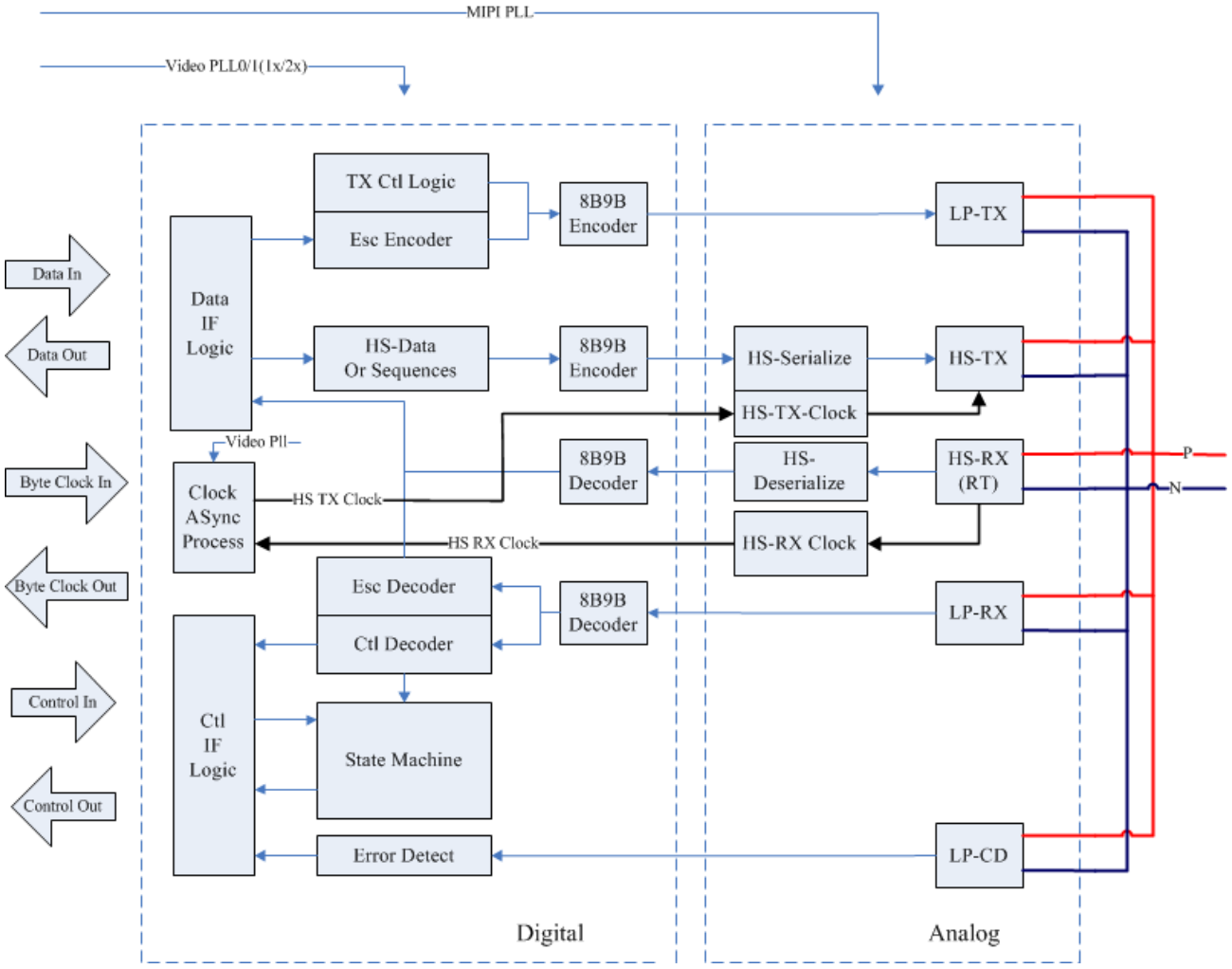

Figure 7- 22. DPHY Block Diagram

Serialization and deserialization of high speed data are operated in the analog part of DPHY. Digital and analog part of DPHY use two different clocks, so the transmit process and receive process of high speed data are asynchronous. The work clock of digital part is Byte Clock, usually set at about 150 MHz, which are lower than clocks of analog part. In order to provide the reliability of transmission, DPHY supports 9-bit code mode, but it needs extra bandwidth to transmit additional bits.

7.3.3. Operations and Functional Descriptions

7.3.3.1. External Signals

The following table describes the external signals of MIPI DSI.

Table 7- 11. MIPI DSI External Signals

Signal	Description	Type
DSI-CKN	MIPI DSI Differential Clock Negative	AO
DSI-CKP	MIPI DSI Differential Clock Positive	AO
DSI-D0N	MIPI DSI Differential Data0 Negative	A I/O

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DSI-D0P	MIPI DSI Differential Data0 Positive	A I/O
DSI-D1N	MIPI DSI Differential Data1 Negative	AO
DSI-D1P	MIPI DSI Differential Data1 Positive	AO
DSI-D2N	MIPI DSI Differential Data2 Negative	AO
DSI-D2P	MIPI DSI Differential Data2 Positive	AO
DSI-D3N	MIPI DSI Differential Data3 Negative	AO
DSI-D3P	MIPI DSI Differential Data3 Positive	AO
VCC-DSI	MIPI DSI Power Supply	P

7.3.3.2. Clock Sources

The following tables describe the clock sources of MIPI DSI. Table 7-12 describes the clock sources of MIPI DSI Controller and Table 7-13 describes the clock source of D-PHY.

Table 7- 12. MIPI DSI Controller Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	Video PLL Clock, default value is 297MHz
PLL_VIDEO1(1X)	Video PLL Clock, default value is 297MHz
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz

Table 7- 13. MIPI D-PHY Clock Source

Clock Sources	Description
PLL_MIPI	MIPI PLL Clock, default value is 594MHz

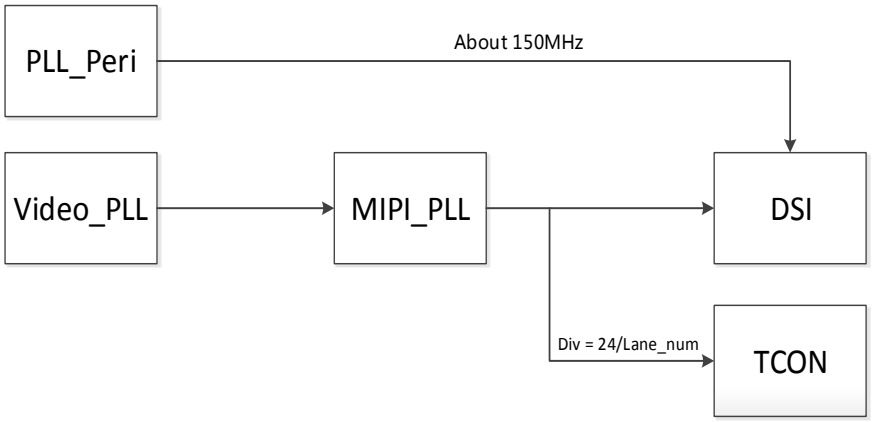

Figure 7- 23. MIPI DSI Clock System

DSI needs two clocks, one is a local clock of about 150MHz from external PLL, and another one is a work clock of DPHY analog part from MIPI PLL. When the clock of TCON_LCD is in DSI, the clock source shall be set as MIPI PLL, internal frequency division coefficient is 24/lane_num. MIPI PLL is a PLL in DPHY. MIPI PLL takes Video PLL as an input resource, and then outputs Video PLL into analog part of DPHY through internal frequency. Video PLL becomes a work clock of DPHY. MIPI PLL has two LDO inside, LDO need to be opened when setting MIPI PLL. Setting 1 on bit22(LDO2_EN) and

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bit23(LDO1_EN) of PLL_MIPI Control Register in CCU can open LDO. Please refer to CCU Spec about clock's calculation formula.

7.3.3.3. D-PHY Analog Power Operation Sequence

Power on operation sequence:
(1).Enable enib(DPHY_ANA2_REG bit[1])
(2).Enable enldor(DPHY_ANA3_REG bit[18])
(3).Enable enldoc(DPHY_ANA3_REG bit[25]) and enldod(DPHY_ANA3_REG bit[24])

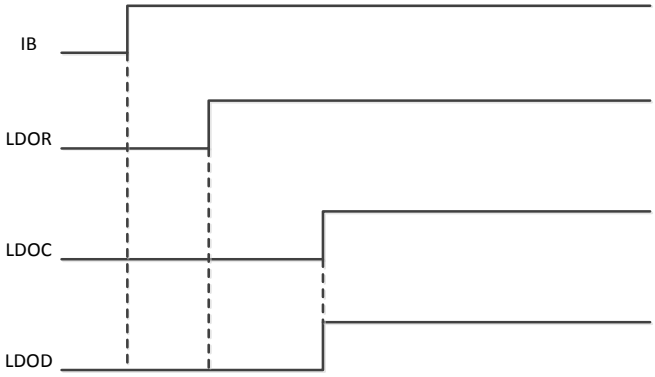

Figure 7- 24. D-PHY Analog Power Power-on Sequence

Power off operation sequence:
(1).Disable enldoc(DPHY_ANA3_REG bit[25]) and enldod(DPHY_ANA3_REG bit[24])
(2).Disable enldor(DPHY_ANA3_REG bit[18])
(3).Disable enib(DPHY_ANA2_REG bit[1])

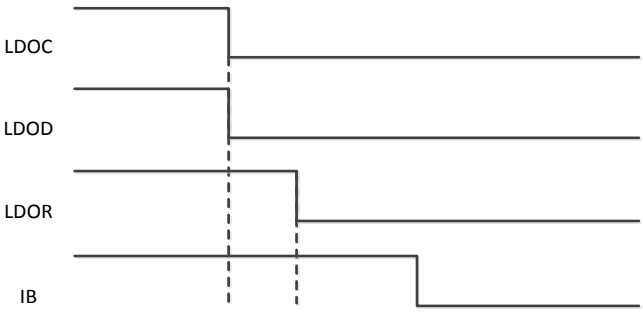

Figure 7- 25. D-PHY Analog Power Power-off Sequence

7.3.3.4. MIPI DSI Protocol Escape Entry

The following table shows the escape entry codes in MIPI DSI.

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Table 7- 14. Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	Mode	11100001
Ultra-Low Power State	Mode	00011110
Undefined-1	Mode	10011111
Undefined-2	Mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

7.3.3.5. MIPI DSI Data Type

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown as follows.

Table 7- 15. MIPI DSI Data Type

Data Type (hex)	Data Type (binary)	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long

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29h	10 1001	Generic Long Write	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
x0h and xFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

The following table presents the complete set of peripheral-to-processor Data Types.

Table 7- 16. Complete Set of Peripheral-to-Processor Data Types

Data Type (hex)	Data Type (binary)	Description	Packet Size
00h – 01h	00 000x	Reserved	Short
02h	00 0010	Acknowledge and Error Report	Short
03h – 07h	00 0011 – 00 0111	Reserved	
08h	00 1000	End of Transmission packet (EoTp)	Short
09h – 10h	00 1001 – 01 0000	Reserved	
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
13h – 19h	01 0011 – 01 1001	Reserved	
1Ah	01 1010	Generic Long READ Response	Long
1Bh	01 1011	Reserved	
1Ch	01 1100	DCS Long READ Response	Long
1Dh – 20h	01 1101 – 10 0000	Reserved	
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short
23h – 3Fh	10 0011 – 11 1111	Reserved	

The following table shows the bit assignment for all error reports.

Table 7- 17. Error Report Bit Definitions

Bit	Description
0	SoT Error

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1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

7.3.3.6. D-PHY Lane State

The following table shows all the Lane States of D-PHY in MIPI DSI standard.

Table 7- 18. D-PHY Lane State

State Code	Line Voltage Levels		High-Speed	Low-Power	
	DP-Line	DN-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

7.3.3.7. D-PHY Lane Sequence

The sequence in data lane:

SOT sequence: LP-11, LP-01, LP-00, HS Sync-sequence ('00011101')
EOT sequence: Diff HS-0 or HS-1, LP-11
Escape mode request: LP-11, LP-10, LP-00, LP-01, LP-00, escape entry command

The following table shows the entry command that the controller supports.

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Table 7- 19. Entry Command

Escape Mode Action	Command Type	Entry Command Pattern
Ultra-Low Power State	mode	00011110
Reset-Trigger [Remote Application]	Trigger	01100010

The sequence in clock lane:

Clock Lane only supports ULPS, an Escape mode entry code is not required.

During Data and Clock ULPS state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

7.3.3.8. D-PHY Timing

SOT and EOT:

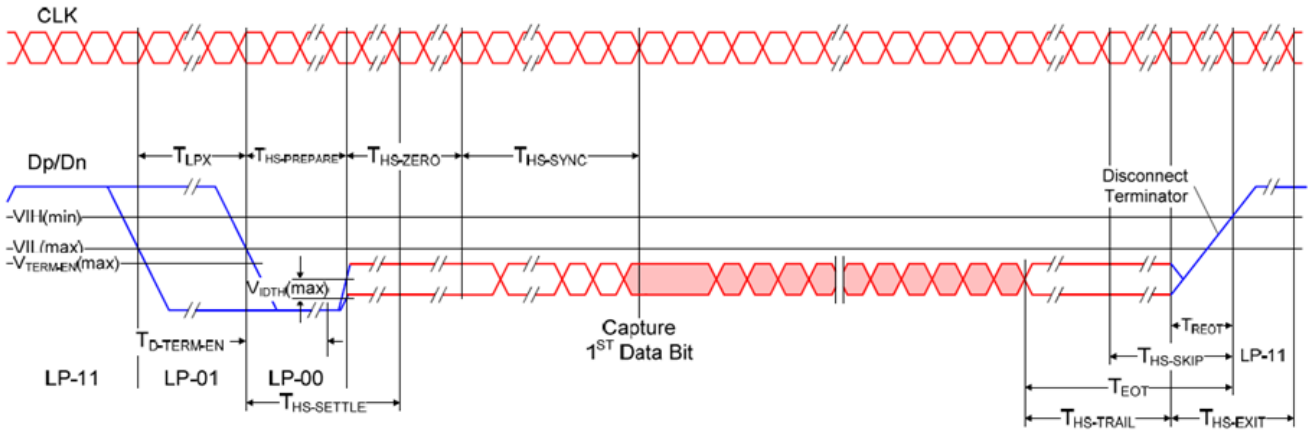

Figure 7- 26. DPHY SOT and EOT Timing

Escape mode timing:

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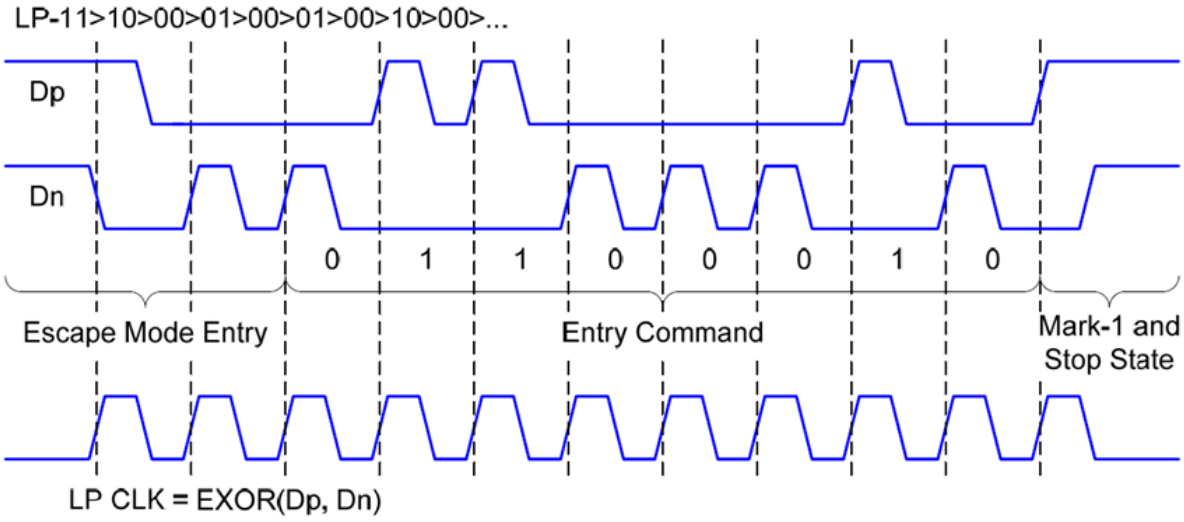

Figure 7- 27. DPHY Escape Mode Timing

Ultra-Low power state is exited by means of a Mark-1 state with a length T_{WAKEUP} followed by a Stop state.

Clock switching between HS and LP:

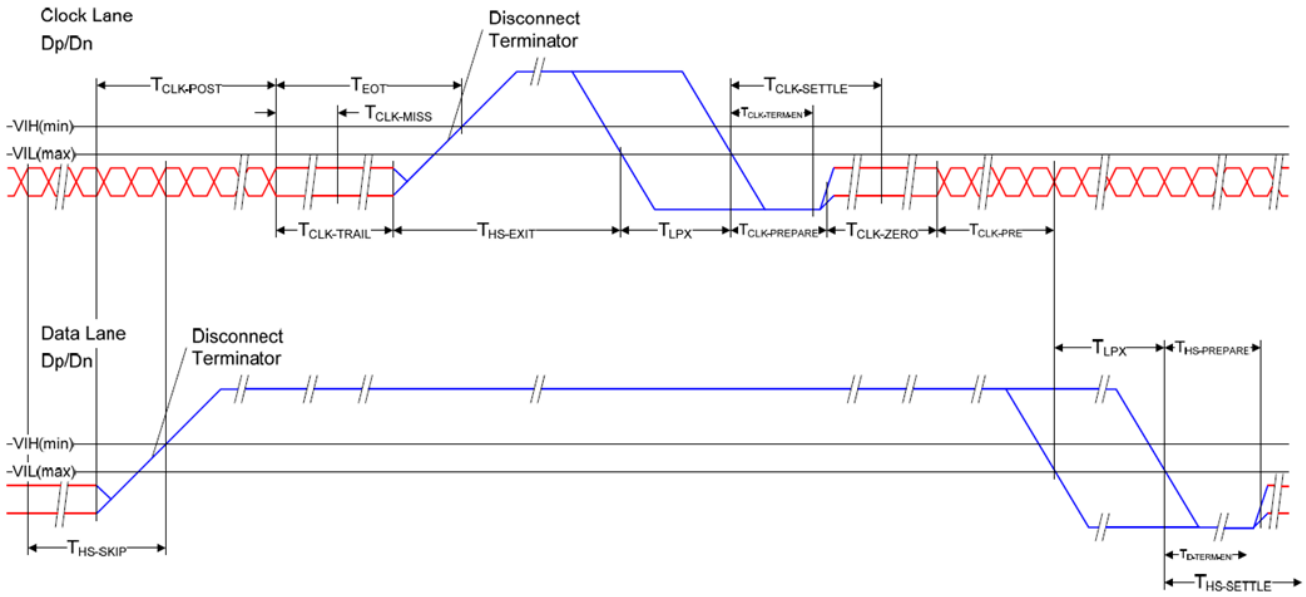

Figure 7- 28. Switching Between HS and LP Timing

7.3.3.9. D-PHY Error Behavior

SoT Error

The Leader sequence for Start of High-Speed Transmission is fault tolerant for any single-bit error. The synchronization may be usable, but confidence in the payload data is lower. If this situation occurs, a SoT Error is indicated.

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SoT Sync Error

If the SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected, a SoT Sync Error is indicated.

Escape Mode Entry Command Error

If the receiving Lane Module does not recognize the received Entry Command for Escape mode , a Escape Mode Entry Command Error is indicated.

False Control Error

If a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence, a False Control Error is indicated. This error is also indicated if a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).

7.3.4. Programming Guidelines

7.3.4.1. Video Mode Initial Sequence

The following diagram shows the initial sequence for video mode.

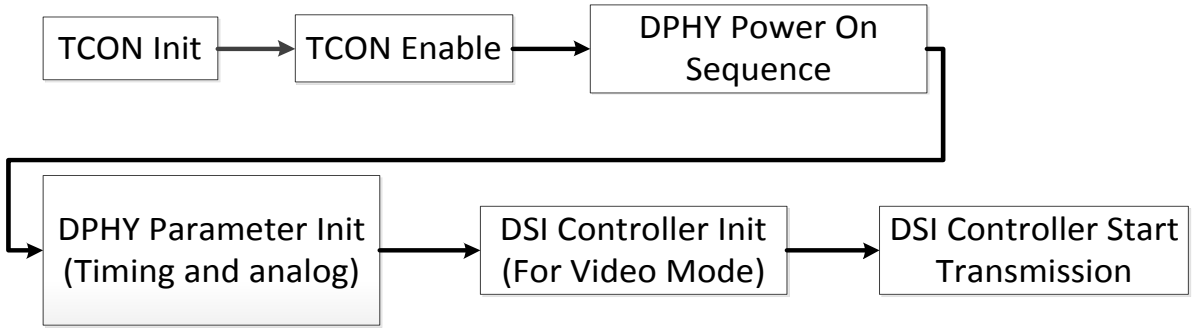

Figure 7- 29. Initial Sequence for Video Mode

7.3.4.2. Command Mode Initial Sequence

The following diagram shows the initial sequence for command mode.

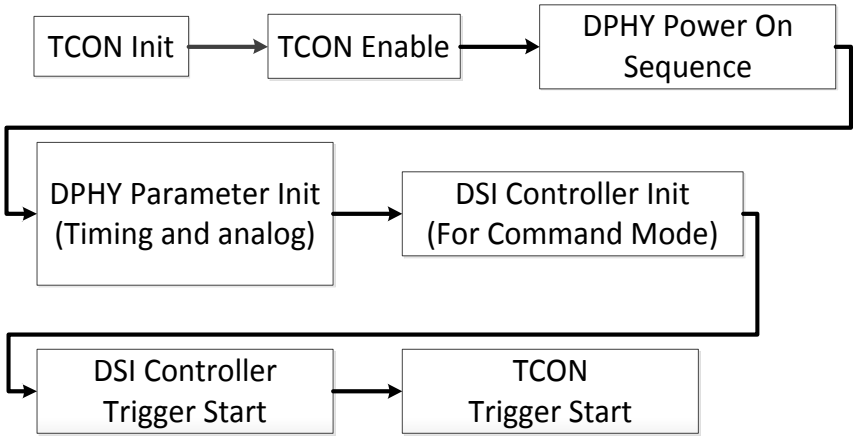

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Figure 7- 30. Initial Sequence for Command Mode

7.3.5. Register List

Module Name	Base Address
MIPI DSI0	0x01CA0000

Register Name	Offset	Description
DSI_CTL_REG	0x0000	DSI Control Register
DSI_GINT0_REG	0x0004	DSI Global Interrupt Register0
DSI_GINT1_REG	0x0008	DSI Global Interrupt Register1
DSI_BASIC_CTL_REG	0x000C	DSI Basic Control Register
DSI_BASIC_CTL0_REG	0x0010	DSI Basic Control Register0
DSI_BASIC_CTL1_REG	0x0014	DSI Basic Control Register1
DSI_BASIC_SIZE0_REG	0x0018	DSI Basic Timing Register0
DSI_BASIC_SIZE1_REG	0x001C	DSI Basic Timing Register1
DSI_BASIC_INST0_REG	0x0020+N*0x04	DSI Basic Instruction Register0 (N=0,1,2,3,4,5,6,7)
DSI_BASIC_INST1_REG	0x0040	DSI Basic Instruction Register1
DSI_BASIC_INST2_REG	0x0044	DSI Basic Instruction Register2
DSI_BASIC_INST3_REG	0x0048	DSI Basic Instruction Register3
DSI_BASIC_INST4_REG	0x004C	DSI Basic Instruction Register4
DSI_BASIC_INST5_REG	0x0050	DSI Basic Instruction Register5
DSI_BASIC_INST6_REG	0x0054	DSI Basic Instruction Register6
DSI_BASIC_TRAN0_REG	0x0060	DSI Basic Transmission Register0
DSI_BASIC_TRAN1_REG	0x0064	DSI Basic Transmission Register1
DSI_BASIC_TRAN2_REG	0x0068	DSI Basic Transmission Register2
DSI_BASIC_TRAN3_REG	0x0074	DSI Basic Transmission Register3
DSI_BASIC_TRAN4_REG	0x0078	DSI Basic Transmission Register4
DSI_BASIC_TRAN5_REG	0x007C	DSI Basic Ttransmission Register5
DSI_PIXEL_CTL0_REG	0x0080	DSI Pixel Control Register0
DSI_PIXEL_PH_REG	0x0090	DSI Pixel Packet Header Register
DSI_PIXEL_PD_REG	0x0094	DSI Pixel Packet Data Register
DSI_PIXEL_PF0_REG	0x0098	DSI Pixel Packet Footer Register0
DSI_PIXEL_PF1_REG	0x009C	DSI Pixel Packet Footer Register1
DSI_SYNC_HSS_REG	0x00B0	DSI H Sync Start Register
DSI_SYNC_HSE_REG	0x00B4	DSI H Sync End Register
DSI_SYNC_VSS_REG	0x00B8	DSI V Sync Start Register
DSI_SYNC_VSE_REG	0x00BC	DSI V Sync End Register
DSI_BLK_HSA0_REG	0x00C0	DSI Blanking H Sync Active Register0
DSI_BLK_HSA1_REG	0x00C4	DSI Blanking H Sync Active Register1

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DSI_BLK_HBP0_REG	0x00C8	DSI Blanking H Back Porch Register0
DSI_BLK_HBP1_REG	0x00CC	DSI Blanking H Back Porch Register0
DSI_BLK_HFP0_REG	0x00D0	DSI Blanking H Front Porch Register0
DSI_BLK_HFP1_REG	0x00D4	DSI Blanking H Front Porch Register1
DSI_BLK_HBLK0_REG	0x00E0	DSI H Blanking Register0
DSI_BLK_HBLK1_REG	0x00E4	DSI H Blanking Register1
DSI_BLK_VBLK0_REG	0x00E8	DSI V Blanking Register0
DSI_BLK_VBLK1_REG	0x00EC	DSI V Blanking Register1
DSI_BURST_LINE_REG	0x00F0	DSI Burst Line Register
DSI_BURST_DRQ_REG	0x00F4	DSI Burst DRQ Register
DSI_DEBUG_REG	0x00FC	DSI Debug Register
DSI_SAFE_PERIOD_REG	0x01F0	DSI Safe Period Register
DSI_CMD_CTL_REG	0x0200	DSI Command Control Register
DSI_CMD_RX_REG	0x0240+N*0x04	DSI Command rx Register (N=0,1,2,3,4,5,6,7)
DSI_CMD_TX_REG	0x0300+N*0x04	DSI Command tx Register (N=0,1,2,…,63)
DSI_DEBUG0_REG	0x02E0	DSI Debug Register0
DSI_DEBUG1_REG	0x02E4	DSI Debug Register1
DSI_DEBUG2_REG	0x02F0	DSI Debug Register2
DSI_DEBUG3_REG	0x02F4	DSI Debug Register3
DSI_DEBUG4_REG	0x02F8	DSI Debug Register4
DSI_FIFO_BIST_REG	0x0FF8	DSI FIFO Bist Register
/	/	/
DPHY_CTL_REG	0x1000	DPHY Control Register
DPHY_TX_CTL_REG	0x1004	DPHY TX Control Register
DPHY_RX_CTL_REG	0x1008	DPHY RX Control Register
/	/	/
DPHY_TX_TIME0_REG	0x1010	DPHY TX Timing Parameter 0 Register
DPHY_TX_TIME1_REG	0x1014	DPHY TX Timing Parameter 1 Register
DPHY_TX_TIME2_REG	0x1018	DPHY TX Timing Parameter 2 Register
DPHY_TX_TIME3_REG	0x101C	DPHY TX Timing Parameter 3 Register
DPHY_TX_TIME4_REG	0x1020	DPHY TX Timing Parameter 4 Register
/	/	/
DPHY_RX_TIME0_REG	0x1030	DPHY RX Timing Parameter 0 Register
DPHY_RX_TIME1_REG	0x1034	DPHY RX Timing Parameter 1 Register
DPHY_RX_TIME2_REG	0x1038	DPHY RX Timing Parameter 2 Register
DPHY_RX_TIME3_REG	0x1040	DPHY RX Timing Parameter 3 Register
/	/	/
DPHY_ANA0_REG	0x104C	DPHY Analog 0 Register
DPHY_ANA1_REG	0x1050	DPHY Analog 1 Register
DPHY_ANA2_REG	0x1054	DPHY Analog 2 Register
DPHY_ANA3_REG	0x1058	DPHY Analog 3 Register
DPHY_ANA4_REG	0x105C	DPHY Analog 4 Register

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/	/	/
DPHY_INT_EN0_REG	0x1060	DPHY Interrupt Enable 0 Register
DPHY_INT_EN1_REG	0x1064	DPHY Interrupt Enable 1 Register
DPHY_INT_EN2_REG	0x1068	DPHY Interrupt Enable 2 Register
DPHY_INT_PD0_REG	0x1070	DPHY Interrupt Pending 0 Register
DPHY_INT_PD1_REG	0x1074	DPHY Interrupt Pending 1 Register
DPHY_INT_PD2_REG	0x1078	DPHY Interrupt Pending 2 Register
/	/	/
DPHY_DBG0_REG	0x10E0	DPHY Debug 0 Register
DPHY_DBG1_REG	0x10E4	DPHY Debug 1 Register
DPHY_DBG2_REG	0x10E8	DPHY Debug 2 Register
DPHY_DBG3_REG	0x10EC	DPHY Debug 3 Register
DPHY_DBG4_REG	0x10F0	DPHY Debug 4 Register

7.3.6. Registers Description

7.3.6.1. DSI_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DSI_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DSI_EN 0: Disable 1: Enable When it's disabled, the module will be reset to idle state.

7.3.6.2. DSI_GINT0_REG(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DSI_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R	0x0	PDE_PEDGE_IN_DRQ_ERR In video mode: Drq is the signal that dsi request data from tcon. Pde is the data valid signal that tcon send data to dsi. If during an active time of Drq signal, there is no rising edge of Pde or there are more than 1 rising edge of Pde appeared, it indicated that an error occurs, this bit will be set to 1.
26	R	0x0	PDE_PEDGE_IN_DRQ_TOO_MANY If during an active time of Drq signal, there are more than 1 rising edge

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			appeared, it indicated that an timing error occurs, this bit will be set to 1.
25	R	0x0	PDE_NEDGE_IN_DRQ_ERR Drq is the signal that dsi request data from tcon. Pde is the data valid signal that tcon send data to dsi. If during an active time of Drq signal, there is no falling edge of Pde or there are more than 1 rising edge of Pde appeared, it indicated that an error occurs, this bit will be set to 1.
24	R	0x0	PDE_NEDGE_IN_DRQ_TOO_MANY If during an active time of Drq signal, there are more than 1 falling edge appeared, it indicated that an timing error occurs, this bit will be set to 1.
23:21	/	/	/
20	R	0x0	BURST_LP_OVERLAP When enable HS transmission, if the LP driver source is still working, an error occurs, this bit will be set to 1.
19	R/W	0x0	LINE_INT_FLAG The flag of line interrupt.
18	R/W	0x0	VB_INT_FLAG The flag of Vb interrupt.
17	R/W	0x0	INSTRU_STEP_FLAG When finish 1 instruction ,this bit will be set to 1.
16	R/W	0x0	INTSTRU_END_FLAG When finish all instructions ,this bit will be set to 1.
15:4	/	/	/
3	R/W	0x0	LINE_INT_EN 0: Disable 1: Enable Enable Line interrupt.
2	R/W	0x0	VB_INT_EN 0: Disable 1: Enable Enable Vb interrupt.
1	R/W	0x0	INSTRU_STEP_EN 0: Disable 1: Enable Enable instructions step interrupt.
0	R/W	0x0	INSTRU_END_EN 0: Disable 1: Enable Enable instructions end interrupt.

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7.3.6.3. DSI_GINT1_REG(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DSI_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_INT_NUM Set the trigger line of line interrupt.

7.3.6.4. DSI_BASIC_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: DSI_BASIC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
26:24	R/W	0x0	BRDY_1_SET
23:16	R/W	0x0	BRDY_SET When use 4 lanes, set the delay time for module to deal with the data arrangement in data subpackage.
15:8	/	/	/
7:4	R/W	0x0	TRAIL_INV 0000: Disable 0001: Enable Others:Reserved Enable trail inversion to deal with 4 lanes bytes aligning.
3	R/W	0x0	TRAIL_FILL 0: Disable 1: Enable fill 2bytes as trail Enable trail padding to deal with 4 lanes bytes aligning.
2	R/W	0x0	HBP_DIS 0: Normal mode 1: HBP disable Disable HBP packets.
1	R/W	0x0	HSA_HSE_DIS 0: Normal mode 1: HSA and HSE disable Disable HSA packets and HSE packets.
0	R/W	0x0	VIDEO_MODE_BURST 0: Normal mode 1: Burst mode Enable video burst mode. When in burst mode, enter LP11 each line.

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7.3.6.5. DSI_BASIC_CTL0_REG(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DSI_BASIC_CTL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	HS_EOTP_EN 0: Disable 1: Enable Enable eotp packet at the end of every HS transmission. Format: "08h" "0fh" "0fh" "01h"
17	R/W	0x0	CRC_EN 0: Disable 1: Enable Enable the CRC function.
16	R/W	0x0	ECC_EN 0: Disable 1: Enable Enable the ECC function.
15:13	/	/	/
12	R/W	0x0	FIFO_GATING 0: Disable 1: Enable Gating data from TCON, note that TCON data is gating in frame unit.
11	/	/	/
10	R/W	0x0	FIFO_MANUAL_RESET Write 1 to reset all correlation FIFO, writing 0 has no effect.
9:6	/	/	/
5:4	R/W	0x0	SRC_SEL 00: TCON data 01: Test data 1x: Reserved Select the data source of DSI.
3:1	/	/	/
0	R/W	0x0	INSTRU_EN 0: Disable 1: Enable When instruction enable, dsi process from instruction0.

7.3.6.6. DSI_BASIC_CTL1_REG(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DSI_BASIC_CTL1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/

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11:4	R/W	0x0	VIDEO_START_DELAY Delay by lines, only valid in video mode.
3	/	/	/
2	R/W	0x0	VIDEO_PRECISION_MODE_ALIGN 0: Cut mode 1: Fill mode In precision mode(set in VIDEO_FRAME_MODE),if the data length is not the integer times of lanes number, we should choose cut mode.
1	R/W	0x0	VIDEO_FRAME_MODE 0: Normal mode 1: Precision mode Set 0 to start new frame by inst, set 1 to start new frame by counter.
0	R/W	0x0	DSI_MODE 0: Command mode 1: Video mode In video mode, enable timing define in basic size.

7.3.6.7. DSI_BASIC_SIZE0_REG(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DSI_BASIC_SIZE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	VIDEO_VBP Set the VBP length.
15:12	/	/	/
11:0	R/W	0x0	VIDEO_VSA Set the VSA length.

7.3.6.8. DSI_BASIC_SIZE1_REG(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DSI_BASIC_SIZE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VIDEO_VT Set the VT length.
15:12	/	/	/
11:0	R/W	0x0	VIDEO_VACT Set the VACT length.

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7.3.6.9. DSI_BASIC_INST0_REG(Default Value: 0x0000_0000)

Offset: 0x0020+N*0x04 (N=0,1,2,3,4,5,6,7)			Register Name: DSI_BASIC_INST0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	INSTRU_MODE 000: Stop(LP-11) 001: TBA 010: HS 011: Escape 100: HS Exit(only use in clk lane) 101: Nop Others: reserved Set the instruction type.
27:24	R/W	0x0	ESCAPE_ENRTY 000: LPDT 001: ULPS 010: Undef-1 011: Undef-2 100: Trigger-Reset 101: Undef-3 110: Undef-4 111: Undef-5 Others: reserved Set the Escape entry code,valid in Escape.
23:20	R/W	0x0	TRANS_PACKET 000: Pixel Packet 001: Command Packet 010: Pixel + Sync + Blk Packet Others: reserved Valid in HS or Escape LPDT.
19:16	R/W	0x0	TRANS_START_CONDITION 000: Immediate, used in cmd_tx 001: Trans FIFO ready TRANS_FIFO_NUM, used in command mode 010: TCON hsync delay DSI_DELAY_CYCLE,used in video mode 011: DSI HT end, DSI new line start,used in video mode Others: reserved Valid in HS or Escape LPDT.
15:5	/	/	/
4:0	R/W	0x0	LANE_SEL Bit4: clk lane selected Bit3: data3 lane selected Bit2: data2 lane selected Bit1: data1 lane selected Bit0: data0 lane selected

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			0: Disable 1: Enable Instruction is valid on selected lane.

7.3.6.10. DSI_BASIC_INST1_REG(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: DSI_BASIC_INST1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	LOOP_SEL Bit31-28: Instruction7 Bit27-24: Instruction6 Bit23-20: Instruction5 Bit19-16: Instruction4 Bit15-12: Instruction3 Bit11-08: Instruction2 Bit07-04: Instruction1 Bit03-00: Instruction0 000: only one times 010: (LOOP_N0+1) times 011: (LOOP_N1+1) times Others: reserved Note LOOP_N0, LOOP_N1 is defined in DSI_BASIC_INST2_REG.

7.3.6.11. DSI_BASIC_INST2_REG(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: DSI_BASIC_INST2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LOOP_N1 Set the instructions loop time.
15:12	/	/	/
11:0	R/W	0x0	LOOP_N0 Set the instructions loop time.

7.3.6.12. DSI_BASIC_INST3_REG(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: DSI_BASIC_INST3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	JUMP_SEL Bit31-28: Instruction7 Bit27-24: Instruction6

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			Bit23-20: Instruction5 Bit19-16: Instruction4 Bit15-12: Instruction3 Bit11-08: Instruction2 Bit07-04: Instruction1 Bit03-00: Instruction0 0000: Jump Instruction0 0001: Jump Instruction1 0010: Jump Instruction2 0011: Jump Instruction3 0100: Jump Instruction4 0101: Jump Instruction5 0110: Jump Instruction6 0111: Jump Instruction7 1111: Jump End Others: reserved Set the instruction order.

7.3.6.13. DSI_BASIC_INST4_REG(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: DSI_BASIC_INST4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	JUMP_CFG0_EN 0:Disable instructions jump function 1:Enable instructions jump function
27:24	/	/	/
23:20	R/W	0x0	JUMP_CFG0_TO Set the instruction which will be jump to after finishing the instructions loop.
19:16	R/W	0x0	JUMP_CFG0_POINT Set the entry instruction of the instructions loop.
15:0	R/W	0x0	JUMP_CFG0_NUM Set the loop time of the instructions loop.

7.3.6.14. DSI_BASIC_INST5_REG(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: DSI_BASIC_INST5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	JUMP_CFG1_EN 0:Disable instructions jump function 1:Enable instructions jump function

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27:24	/	/	/
23:20	R/W	0x0	JUMP_CFG1_TO Set the instruction which will be jump to after finishing the instructions loop.
19:16	R/W	0x0	JUMP_CFG1_POINT Set the entry instruction of the instructions loop.
15:0	R/W	0x0	JUMP_CFG1_NUM Set the loop time of the instructions loop.

7.3.6.15. DSI_BASIC_INST6_REG(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: DSI_BASIC_INST6_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LOOP_N1_SHADOW In video burst mode, replace LOOP_N1 at blanking.
15:12	/	/	/
11:0	R/W	0x0	LOOP_N0_SHADOW In video burst mode, replace LOOP_N0 at blanking.

7.3.6.16. DSI_BASIC_TRAN0_REG(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: DSI_BASIC_TRAN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	TRANS_START_SET In video mode, hs tx by timing start. In command mode, hs tx when fifo reach this numbers.

7.3.6.17. DSI_BASIC_TRAN4_REG(Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: DSI_BASIC_TRAN4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

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15:0	R/W	0x0	HS_ZERO_REDUCE_SET Setting a value to reduce HS Zero time. Delay time to info D-PHY into HS. TRANS_START_SET- HS_ZERO_REDUCE_SET = DSI_HS_ZERO_TIME. Total hs zero time = DSI_HS_ZERO_TIME + DPHY_HS_ZERO_TIME. It should be HS_ZERO_REDUCE_SET < (TRANS_START_SET-30). Note that HS_ZERO_REDUCE_SET should be 7 hsbyte clk earlier than TRANS_START_SET, and this value is refer to lp clk. If hs=300M lp=150M,(1/300)x8x7 ÷ (1/150)=28

7.3.6.18. DSI_BASIC_TRAN5_REG(Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: DSI_BASIC_TRAN5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	DRQ_MODE 0: Request tcon data at new line start 1: Request tcon data reference to Drq_set Set the DRQ request condition.
27:10	/	/	/
9:0	R/W	0x0	DRQ_SET Request tcon data reference setting, this bit is only valid when DRQ_MODE='1'.

7.3.6.19. DSI_PIXEL_CTL0_REG(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: DSI_PIXEL_CTL0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PD_PLUG_DIS Disable PD plug before pixel bytes.
15:5	/	/	/
4	R/W	0x0	PIXEL_ENDIAN 0: LSB first 1: MSB first Set the endian of the pixel data.
3:0	R/W	0x0	PIXEL_FORMAT Command mode 0000: 24bit (rgb888) 0001: 18bit (rgb666) 0010: 16bit (rgb565)

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			Video mode 1000: 24bit(rgb888) 1001: 18bit(rgb666L) 1010: 18bit (rgb666) 1011: 16bit(rgb565) Others: reserved Set the pixel format.

7.3.6.20. DSI_PIXEL_PH_REG(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: DSI_PIXEL_PH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Only valid when DSI ECC is disable.
23:8	R/W	0x0	WC WC is byte numbers of PD in a pixel packet.
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT Video mode 24bit, set as "3eh" Video mode L18bit, set as "2eh" Video mode 18bit, set as "1eh" Video mode 16bit, set as "0eh" Command mode, set as "39h"

7.3.6.21. DSI_PIXEL_PD_REG(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: DSI_PIXEL_PD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	PD_TRANN Used in transmissions except 1st one, set as "3Ch",only valid when PD_PLUG_DIS is set to '0'.
15:8	/	/	/
7:0	R/W	0x0	PD_TRAN0 Used in 1st transmission, set as "2Ch", only valid when PD_PLUG_DIS is set to '0'.

7.3.6.22. DSI_PIXEL_PF0_REG(Default Value: 0x0000_0000)

Offset: 0x0098	Register Name: DSI_PIXEL_PF0_REG

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Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0	CRC_FORCE CRC force to this value, this value is only valid when CRC is disable.

7.3.6.23. DSI_PIXEL_PF1_REG(Default Value: 0xFFFF_FFFF)

Offset: 0x009C			Register Name: DSI_PIXEL_PF1_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0xffff	CRC_INIT_LINEN CRC initial to this value in transmition except 1st one, only valid when CRC is enable.
15:0	R/W	0xffff	CRC_INIT_LINE0 CRC initial to this value in 1st transmition every frame, only valid when CRC is enable.

7.3.6.24. DSI_SYNC_HSS_REG(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: DSI_SYNC_HSS_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	ECC Set as "12h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT HSS, set as "21h".

7.3.6.25. DSI_SYNC_HSE_REG(Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: DSI_SYNC_HSE_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	ECC Set as "01h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".

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7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT HSE, set as "31h".

7.3.6.26. DSI_SYNC_VSS_REG(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: DSI_SYNC_VSS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Set as "07h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT VSS, set as "01h".

7.3.6.27. DSI_SYNC_VSE_REG(Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: DSI_SYNC_VSE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ECC Set as "14h".
23:16	R/W	0x0	D1 Set as "00h".
15:8	R/W	0x0	D0 Set as "00h".
7:6	R/W	0x0	VC Virtual Channel.
5:0	R/W	0x0	DT VSE, set as "11h".

7.3.6.28. DSI_BLK_HSA0_REG(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: DSI_BLK_HSA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HSA_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet.

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			Set the packet header value of HSA packets.

7.3.6.29. DSI_BLK_HSA1_REG(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: DSI_BLK_HSA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HSA_PF Set the packet footer value of HSA packets.
15:8	/	/	/
7:0	R/W	0x0	HSA_PD Set the packet value of HSA packets.

7.3.6.30. DSI_BLK_HBP0_REG(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: DSI_BLK_HBP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HBP_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet. Set the packet header value of HBP packets.

7.3.6.31. DSI_BLK_HBP1_REG(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: DSI_BLK_HBP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HBP_PF Set the packet footer value of HBP packets.
15:8	/	/	/
7:0	R/W	0x0	HBP_PD Set the packet value of HBP packets.

7.3.6.32. DSI_BLK_HFP0_REG(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: DSI_BLK_HFP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HFP_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet. Set the packet header value of HFP packets.

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7.3.6.33. DSI_BLK_HFP1_REG(Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: DSI_BLK_HFP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HFP_PF Set the packet footer value of HFP packets.
15:8	/	/	/
7:0	R/W	0x0	HFP_PD Set the packet value of HFP packets.

7.3.6.34. DSI_BLK_HBLK0_REG(Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: DSI_BLK_HBLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HBLK_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet. Set the packet header value of HBLK packets.

7.3.6.35. DSI_BLK_HBLK1_REG(Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: DSI_HBLK_BLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	HBLK_PF Set the packet footer value of HBLK packets.
15:8	/	/	/
7:0	R/W	0x0	HBLK_PD Set the packet value of HBLK packets.

7.3.6.36. DSI_BLK_VBLK0_REG(Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: DSI_BLK_VBLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VBLK_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet. Set the packet header value of VBLK packets.

7.3.6.37. DSI_BLK_VBLK1_REG(Default Value: 0x0000_0000)

Offset: 0x00EC			Register Name: DSI_BLK_VBLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:16	R/W	0x0	VBLK_PF Set the packet footer value of VBLK packets.
15:8	/	/	/
7:0	R/W	0x0	VBLK_PD Set the packet value of VBLK packets.

7.3.6.38. DSI_BRUST_LINE_REG(Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: DSI_BRUST_LINE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	LINE_SYNCPOINT In video burst mode, set the start time of the first HS data transmission. It is set as 30 by default .
15:0	R/W	0x0	LINE_NUM In video burst mode ,set the total time of each line whose unit is the cycle of symbol.

7.3.6.39. DSI_BRUST_DRQ_REG(Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: DSI_BRUST_DRQ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	DRQ_EDGE1 In video burst mode, DRQ_EDGE0 and DRQ_EDGE1 is used to control the create time of dsi_drq. There is a timer working during burst mode. If DRQ_EDGE1<timer value<DRQ_EDGE0,the dsi_drq will be set to 1.
15:0	R/W	0x0	DRQ_EDGE0 In video burst mode,DRQ_EDGE0 and DRQ_EDGE1 is used to control the create time of dsi_drq. There is a timer working during burst mode. If DRQ_EDGE1<timer value<DRQ_EDGE0,the dsi_drq will be set to 1.

7.3.6.40. DSI_DEBUG_REG(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: DSI_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DSI_FIFO_UNDER_FLOW It will be set to 1 when the DSI FIFO is underflow.
30:0	/	/	/

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7.3.6.41. DSI_SAFE_PERIOD_REG(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: DSI_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, dsi controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, dsi controller allow dram controller to change frequency. The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line

7.3.6.42. DSI_CMD_CTL_REG(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: DSI_CMD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
26	R/W1C	0x0	RX_OVERFLOW 1: rx data is overflow register buffer Write'1' to clear this bit. Writing '0' has no effect.
25	R/W1C	0x0	RX_FLAG 1: rx has happened Write'1' to clear this bit. Writing '0' has no effect.
24	R	0x0	RX_STATUS 0: rx is finish 1: rx is pending
20:16	R	0x0	RX_SIZE (RX_SIZE+1) is number of bytes in the last rx.
15:10	/	/	/
9	R/W1C	0x0	TX_FLAG 1: tx has happened Write'1' to clear this bit. Writing '0' has no effect.
8	R	0x0	TX_STATUS 0: tx is finish

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			1: tx is pending
7:0	R/W	0x0	TX_SIZE (TX_SIZE+1) is number of bytes ready to tx.

7.3.6.43. DSI_CMD_RX_REG(Default Value: 0x0000_0000)

Offset: 0x0240+N*0x04 (N=0,1,2,3,4,5,6,7)			Register Name: DSI_CMD_RX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data from rx, only in LPDT Only read when RX_Flag is setting. No way to clear this fifo.

7.3.6.44. DSI_CMD_TX_REG(Default Value: 0x0000_0000)

Offset:0x0300+N*0x04 (N=0,1,2…255)			Register Name: DSI_CMD_TX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data for tx, transmission in HS and LPDT, defined by INST_REG.

7.3.6.45. DSI_DEBUG0_REG(Default Value: 0x0000_0000)

Offset: 0x02E0	Register Name: DSI_DEBUG0_REG

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Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R	0x0	VIDEO_CURR_LINE The real time current line.

7.3.6.46. DSI_DEBUG1_REG(Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: DSI_DEBUG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	VIDEO_CURR_LP2HS The current number of LP to HS in real time.

7.3.6.47. DSI_DEBUG2_REG(Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: DSI_DEBUG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W1C	0x0	INSTRU_UNKNOW_FLAG Bit31: Instruction7 Unknow Bit30: Instruction6 Unknow Bit29: Instruction5 Unknow Bit28: Instruction4 Unknow Bit27: Instruction3 Unknow Bit26: Instruction2 Unknow Bit25: Instruction1 Unknow Bit24: Instruction0 Unknow Write '1' to clear this bit. Writing '0' has no effect.
23	/	/	/
22:20	R	0x0	CURR_INSTRU_NUM Instruction number process now.
19:4	R/W	0x0	CURR_LOOP_NUM The loop number of instructions loop.
3:2	/	/	/
1	R/W1C	0x0	TRANS_FAST_FLAG When in active region, transmit FIFO is empty, this bit is set. Write '1' to clear this bit.
0	R/W1C	0x0	TRANS_LOW_FLAG Before trans FIFO reset, trans FIFO is not empty, this bit is set. Write '1' to clear this bit.

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7.3.6.48. DSI_DEBUG3_REG(Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: DSI_DEBUG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	CURR_FIFO_NUM Byte numbers in trans FIFO now.
15:0	/	/	/

7.3.6.49. DSI_DEBUG4_REG(Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: DSI_DEBUG4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	DSI_FIFO_BIST_EN 0: Disable 1: Enable Entry address is 0xFF8.
27:24	/	/	/
23:0	R/W	0x0	TEST_DATA Cooperated with SRC_SEL in DSI_BASIC_CTL0_REG,instead of the data from TCON.

7.3.6.50. DPHY_CTL_REG(Default Value: 0x0000_0000)

Offset:0x1000			Register Name: DPHY_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	LANE_NUM 000: 1 data lane 001: 2 data lane 010: 3 data lane 011: 4 data lane This bits determine lane number used for transmission.
3:1	/	/	/
0	R/W	0x0	MODULE_EN 0: Disable 1: Enable When it's disabled, the module will be reset to idle state.

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7.3.6.51. DPHY_TX_CTL_REG(Default Value: 0x0000_0000)

Offset:0x1004			Register Name: DPHY_TX_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	ULPSTX_ENTER 0: Direct (enter LP-00 after ULPS command) 1: Indirect (enter MARK-I after ULPS command then LP-00)
28	R/W	0x0	HSTX_CLK_CONT 0: Disable 1: Enable When this bit is enable, clk lane continue in HS mode. When this bit is disable, clk lane anto enter LP mode.
27:26	/	/	/
25	R/W	0x0	HSTX_CLK_EXIT 0: No effect 1: Force clock lane exit from HS
24	R/W	0x0	HSTX_DATA_EXIT 0: No effect 1: Force all data lanes exit from HS
23:21	/	/	/
20	R/W	0x0	ULPSTX_CLK_EXIT 0: No effect 1: Force Clock lane exit from ULPS
19	R/W	0x0	ULPSTX_DATA3_EXIT 0: No effect 1: Force data lane 3 exit from ULPS
18	R/W	0x0	ULPSTX_DATA2_EXIT 0: No effect 1: Force data lane 2 exit from ULPS
17	R/W	0x0	ULPSTX_DATA1_EXIT 0: No effect 1: Force data lane 1 exit from ULPS
16	R/W	0x0	ULPSTX_DATA0_EXIT 0: No effect 1: Force data lane 0 exit from ULPS
15:13	/	/	/
12	R/W	0x0	FORCE_LP11 0: No effect 1: Force module work in LP11
11	R/W	0x0	HSTX_8B9B_EN 0: 8B9B Encoding disable 1: 8B9B Encoding enable
10	R/W	0x0	LPTX_8B9B_EN

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			0: 8B9B Encoding disable 1: 8B9B Encoding enable
9	R/W	0x0	HSTX_ENDIAN 0: LSB first 1: MSB first
8	R/W	0x0	LPTX_ENDIAN 0: LSB first 1: MSB first
7:5	/	/	/
4	R/W	0x0	TX_CLK_FORCE Write 1 force into tx default state(lp00), writing 0 has no effect.
3	R/W	0x0	TX_D3_FORCE Write 1 force into tx default state(lp00), writing 0 has no effect.
2	R/W	0x0	TX_D2_FORCE Write 1 force into tx default state(lp00), writing 0 has no effect.
1	R/W	0x0	TX_D1_FORCE Write 1 force into tx default state(lp00), writing 0 has no effect.
0	R/W	0x0	TX_D0_FORCE Write 1 force into tx default state(lp00), writing 0 has no effect.

7.3.6.52. DPHY_RX_CTL_REG(Default Value: 0x0000_0000)

Offset:0x1008			**Register Name: DPHY_RX_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBC_EN Debounce enable.
30:25	/	/	/
24	R/W	0x0	RX_CLK_FORCE 0: No effect 1: Force rx
23	R/W	0x0	RX_D3_FORCE 0: No effect 1: Force rx
22	R/W	0x0	RX_D2_FORCE 0: No effect 1: Force rx
21	R/W	0x0	RX_D1_FORCE 0: No effect 1: Force rx
20	R/W	0x0	RX_D0_FORCE 0: No effect 1: Force rx
19:16	R/W	0x0	LPRX_TRND_MASK

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			0: Not mask 1: Mask, no ack to turnaround in LPRX
15:13	/	/	/
12	R/W	0x0	HSRX_SYNC Receiver synchronization to SoT code 0: Synchronize exactly to SoT (0xb8) 1: Synchronize to SoT (0xb8) with a single bit error
11	R/W	0x0	HSRX_8B9B_EN 0: 8B9B Decoding disable 1: 8B9B Decoding enable
10	R/W	0x0	LPRX_8B9B_EN 0: 8B9B Decoding disable 1: 8B9B Decoding enable
9	R/W	0x0	HSRX_ENDIAN 0: LSB first 1: MSB first
8	R/W	0x0	LPRX_ENDIAN 0: LSB first 1: MSB first
7:0	/	/	/

7.3.6.53. DPHY_TX_TIME0_REG(Default Value: 0x0000_0000)

Offset:0x1010			Register Name: DPHY_TX_TIME0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	HS_TRAIL_SET HS trail = (HS_TRAIL_SET + 2) * Tbyteclk + (2~3)*Tclk - (3~4)*Tclkd8.
23:16	R/W	0x0	HS_PRE_SET The setting of hs prepare time: Begin with LP00, end after (HS_PRE_SET + 4)*Tclk.
15:8	/	/	/
7:0	R/W	0x0	LPX_TM_SET LP pulse = (LPX_TM_SET + 1)*Tclk.

7.3.6.54. DPHY_TX_TIME1_REG(Default Value: 0x0000_0000)

Offset:0x1014			Register Name: DPHY_TX_TIME1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	CK_POST_SET CK_Post_set can not be 0,after the falling edge of entx, keep it for (CK_POST_SET + 2)* Tclk and then turn off the clk.
23:16	R/W	0x0	CK_PRE_SET

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			Clk pre = ((CK_PRE_SET + 2)+ (0 ~ LPX_TM_SET))* Tclk
15:8	R/W	0x0	CK_ZERO_SET CK_Zero_set can not be 0,when entxc is set to 1, after (CK_ZERO_SET + 2)* Tclk, the enckq will be set as 1.
7:0	R/W	0x0	CK_PREP_SET Clk prepare = (CK_PREP_SET + 3)* clk

7.3.6.55. DPHY_TX_TIME2_REG(Default Value: 0x0000_0000)

Offset:0x1018			Register Name: DPHY_TX_TIME2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	HS_DLY_MODE The setting of HS zero time depending on HS_DLYMODE: when HS_DLYMODE=0 ,HS_ZERO_TIME > 20*Tbyteclk When HS_DLYMODE=1,HS_ZERO_TIME = (HS_DLY_SET + 4)*Tclk - 2*(LPX_TM_SET + 1)*Tclk + (20~23)*Tbyteclk - (HS_PRE_SET + 4)*Tclk
27:24	/	/	/
23:8	R/W	0x0	HS_DLY_SET Use this value to prolong the time before LP switch to HS, cut down the length of HS-Zero.
7:0	R/W	0x0	CK_TRAIL_SET CK_TRAIL_SET clk tail =(CK_TRAIL_SET + 2)* Tclk

7.3.6.56. DPHY_TX_TIME3_REG(Default Value: 0x0000_0000)

Offset:0x101C			Register Name: DPHY_TX_TIME3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	LPTX_ULPS_EXIT_SET ULPS exit Cycles.

7.3.6.57. DPHY_TX_TIME4_REG(Default Value: 0x0000_0101)

Offset:0x1020			Register Name: DPHY_TX_TIME4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x1	HSTX_ANA1_SET Cannot be zero.
7:0	R/W	0x1	HSTX_ANA0_SET

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			Cannot be zero.

7.3.6.58. DPHY_RX_TIME0_REG(Default Value: 0x0000_0000)

Offset:0x1030			Register Name: DPHY_RX_TIME0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	HSRX_SYNC_ERR_TO When HS SOT is not detected until reaching the hs sync error timeout counter, the SOT_ERR should be flagged. Only valid for data lane.
23:16	R/W	0x0	HSRX_CLK_MISS When clock lane is detected no clock until hs rx clock miss counter, the receiver disconnect the terminal resister. Only valid for clock lane.
15:8	R/W	0x0	LPRX_TO The timeout counter for receiver in LP mode.
7:6	/	/	/
5	R/W	0x0	HSRX_SYNC_ERR_TO_EN 0: Disable 1: Enable HSRX_SYNC_ERR_TO counter
4	R/W	0x0	HSRX_CLK_MISS_EN 0: Disable 1: Enable HSRX_CLK_MISS counter
3:2	/	/	/
1	R/W	0x0	FREQ_CNT_EN 0: Disable 1: Enable When enabled, the FREQ_CNT counter is counted by DPhy Clock between 1000 Byte Clock.
0	R/W	0x0	LPRX_TO_EN LP RX timeout enable 0: Disable 1: Enable

7.3.6.59. DPHY_RX_TIME1_REG(Default Value: 0x0000_0000)

Offset:0x1034			Register Name: DPHY_RX_TIME1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	0x0	RX_DLY The time that DPhy process hs fifo data and pull off data valid signal to protocol after DPhy has detected the lane state from HS to LP. It should be more than 8 byte clock cycle time.
19:0	R/W	0x0	LPRX_ULPS_WP When receivers detects MARK-I for ULPS Wakeup Cycles, the

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			corresponding ULPS WP is pending. (Valid for clock lane and all data lane)

7.3.6.60. DPHY_RX_TIME2_REG(Default Value: 0x0000_0000)

Offset:0x1038			Register Name: DPHY_RX_TIME2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	HSRX_ANA1_SET Reserved
7:0	R/W	0x0	HSRX_ANA0_SET Reserved

7.3.6.61. DPHY_RX_TIME3_REG(Default Value: 0x0000_0000)

Offset:0x1040			Register Name: DPHY_RX_TIME3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	LPRST_DLY The added delay time that reset the hs-fifo after the DPhy has detected the HS-to-LP.
15:0	R/W	0x0	FREQ_CNT The value of FREQ_CNT counter is counted by DPhy Clock between 1000 Byte Cock.

7.3.6.62. DPHY_ANA0_REG(Default Value: 0x0000_0000)

Offset:0x104C			Register Name: DPHY_ANA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	REG_PWS Register for reference power input level adjust pws=0, vref=1/3hv; pws=1, vref=0.4hv
30	R/W	0x0	REG_PWEND Register for enable the switch of lvdio
29	R/W	0x0	REG_PWENC Register for enable the switch of lvcio
28	R/W	0x0	REG_DMPC Register for HS tx dump option in Clock Lane Set as "1"
27:24	R/W	0x0	REG_DMP Register for HS tx dump option in Data Lane<3:0>

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			Set as "1111"
23:20	R/W	0x0	REG_SRXDT Register for HS rx data polar switch in Data Lane<3:0>
19:16	R/W	0x0	REG_SRXCK Register for HS rx clock polar switch in Data Lane<3:0>
15	R/W	0x0	REG_SDIV2 Coefficient for programmable frequency divider
14:12	R/W	0x0	REG_SLV Register for data/clock power level adjust Set as "111"
11:8	R/W	0x0	REG_DEN Register for HS p2s HS serial clock output in Data Lane<3:0> Set as "1111"
7:4	R/W	0x0	REG_PLR Register for HS p2s data polar switch in Data Lane<3:0>
3:2	R/W	0x0	REG_SFB Register for reference power output level adjust sfb=00, lv=vref, sfb=01, lv=1.067vref, sfb=10, lv=1.103vref, sfb=11, lv=1.143vref,
1	R/W	0x0	REG_RSD Coefficient for programmable frequency divider
0	R/W	0x0	REG_SELSCK Register for switch clock from PLL or ckisys

7.3.6.63. DPHY_ANA1_REG(Default Value: 0x0000_0000)

Offset:0x1050			**Register Name: DPHY_ANA0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	/	REG_VTTMODE 0: Controlled by register 1: Controlled by circuit Use to control the work mode of ENVTT and ENVTTC.It also has an effect on the work mode of ENP2S.
30	/	/	/
29:28	R/W	0x0	REG_CSMPS Register for HS p2s sync mode choose Set as "01"
27:24	R/W	0x0	REG_SVTT Register for HS tx output swing adjust
23:20	R/W	0x0	REG_SVDLC Register for HS rx clock delay adjust in Clock Lane

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19:16	R/W	0x0	REG_SVDL3 Register for HS rx data delay adjust in Data Lane3
15:12	R/W	0x0	REG_SVDL2 Register for HS rx data delay adjust in Data Lane2
11:8	R/W	0x0	REG_SVDL1 Register for HS rx data delay adjust in Data Lane1
7:4	R/W	0x0	REG_SVDL0 Register for HS rx data delay adjust in Data Lane0
3:1	/	/	/
0	R/W	0x0	REG_STXCK Register for HS DDRq clock polar switch in Clock Lane

7.3.6.64. DPHY_ANA2_REG(Default Value: 0x0000_0000)

Offset:0x1054			Register Name: DPHY_ANA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	ENP2S_CPU Enable signal for HS p2s module in Data Lane<3:0>
23:20	R/W	0x0	ENRX_CPU Enable signal for HS rx module is active in Data Lane<3:0>
19:16	R/W	0x0	ENTERM_CPU Enable signal for HS rx terminal resistor is active in Data Lane<3:0>
15	/	/	/
14	R/W	0x0	ENRXC_CPU Enable signal for HS receiver module is active in Clock Lane
13	R/W	0x0	ENTERMC_CPU Enable signal for HS rx terminal resistor is active in Clock Lane
12	/	/	/
11:8	R/W	0x0	ENTX_CPU Enable signal for HS tx module is active in Data Lane<3:0>
10:7	/	/	/
6	R/W	0x0	ENCKQ_CPU Enable signal for DDRq clock in Clock Lane
5	R/W	0x0	ENTXC_CPU Enable signal for HS tx module is active in Clock Lane
4	R/W	0x0	ENCK_CPU Enable signal for ref clock is active to MIPI Set as "1"
3	/	/	/
2	R/W	0x0	ENRVS Enable signal for reverse mode is active
1	R/W	0x0	ENIB

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			Enable signal for current bias is active Set as "1"
0	R/W	0x0	ANA_CPU_EN Enable all register via CPU, when disable, those bits are control by circuit automatic.

7.3.6.65. DPHY_ANA3_REG(Default Value: 0x0000_0000)

Offset:0x1058			Register Name: DPHY_ANA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	ENVTT Enable signal for HS TX LDO in Data Lane<3:0> Set as "11111" when hstx
27	R/W	0x0	ENVTTC Enable signal for HS TX LDO in Clock Lane Set as "1" when hstx
26	R/W	0x0	ENDIV Enable signal for programmable frequency divider of clock from PLL Set as "1"
25	R/W	0x0	ENLDOC Enable signal for clock power LDO is active DSI set as "1"; CSI set as "0"
24	R/W	0x0	ENLDOD Enable signal for data power LDO is active Set as "1"
23:19	/	/	/
18	R/W	0x0	ENLDOR Enable signal for reference power LDO is active Set as "1"
17	R/W	0x0	ENCKDBG Enable signal for debug clock into & out of programmable frequency divider
16	R/W	0x0	ENTEST Enable signal for test mode is active
15	/	/	/
14	R/W	0x0	ENLPCDC_CPU Enable signal for LP cd module is active in Clock Lane
13	R/W	0x0	ENLPTXC_CPU Enable signal for LP tx module is active in Clock Lane
12	R/W	0x0	ENLPRXC_CPU Enable signal for LP rx module is active in Clock Lane
11:8	R/W	0x0	ENLPCD_CPU Enable signal for LP cd module is active in Data Lane<3:0>

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7:4	R/W	0x0	ENLPRX_CPU Enable signal for LP rx module is active in Data Lane<3:0>
3:0	R/W	0x0	ENLPTX_CPU Enable signal for LP tx module is active in Data Lane<3:0>

7.3.6.66. DPHY_ANA4_REG(Default Value: 0x0000_0000)

Offset:0x105C			Register Name: DPHY_ANA4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:25	R/W	0x0	REG_SLLPTX Control the slew rate of LPTX.
24	R/W	0x0	REG_DMPLVC Use to make the internal LDO stable.
23:20	R/W	0x0	REG_DMPLVD Use to make the internal LDO stable.
19:17	/	/	/
16:12	R/W	0x0	REG_CKDV Coefficient for programmable frequency divider. Set as "00001".
11:10	R/W	0x0	REG_TMSC Register for HS rx resistance adjustment in Clock Lane. Set as "01".
9:8	R/W	0x0	REG_TMSD Register for HS rx resistance adjustment in Data Lanes. Set as "01".
7:6	R/W	0x0	REG_TXDNSC Register for HS tx pulldown resistance adjustment in Clock Lane. Set as "01".
5:4	R/W	0x0	REG_TXDNSD Register for HS tx pulldown resistance adjustment in Data Lanes. Set as "01".
3:2	R/W	0x0	REG_TXPUSC Register for HS tx pullup resistance adjustment in Clock Lane. Set as "01".
1:0	R/W	0x0	REG_TXPUSD Register for HS tx pullup resistance adjustment in Data Lanes. set as "01".

7.3.6.67. DPHY_INT_EN0_REG(Default Value: 0x0000_0000)

Offset:0x1060	Register Name: DPHY_INT_EN0_REG

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CD_LP1_ERR_D3_INT Contention Detection detects LP1 error interrupt
30	R/W	0x0	CD_LP0_ERR_D3_INT Contention Detection detects LP0 error interrupt
29	R/W	0x0	CD_LP1_ERR_D2_INT Contention Detection detects LP1 error interrupt
28	R/W	0x0	CD_LP0_ERR_D2_INT Contention Detection detects LP0 error interrupt
27	R/W	0x0	CD_LP1_ERR_D1_INT Contention Detection detects LP1 error interrupt
26	R/W	0x0	CD_LP0_ERR_D1_INT Contention Detection detects LP0 error interrupt
25	R/W	0x0	CD_LP1_ERR_D0_INT Contention Detection detects LP1 error interrupt
24	R/W	0x0	CD_LP0_ERR_D0_INT Contention Detection detects LP0 error interrupt
23	R/W	0x0	CD_LP1_ERR_CLK_INT Contention Detection detects LP1 error interrupt
22	R/W	0x0	CD_LP0_ERR_CLK_INT Contention Detection detects LP0 error interrupt
21:16	/	/	/
15	R/W	0x0	RX_ALG_ERR_D3_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
14	R/W	0x0	RX_ALG_ERR_D2_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
13	R/W	0x0	RX_ALG_ERR_D1_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN
12	R/W	0x0	RX_ALG_ERR_D0_INT The payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
11	R/W	0x0	SOT_SYNC_ERR_D3_INT DPHY RX cannot detect SOT sequence at Data Lane 0 interrupt.
10	R/W	0x0	SOT_SYNC_ERR_D2_INT DPHY RX cannot detect SOT sequence at Data Lane 0 interrupt.
9	R/W	0x0	SOT_SYNC_ERR_D1_INT DPHY RX cannot detect SOT sequence at Data Lane 0 interrupt.
8	R/W	0x0	SOT_SYNC_ERR_D0_INT DPHY RX cannot detect SOT sequence at Data Lane 0 interrupt.
7	R/W	0x0	SOT_ERR_D3_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0

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			interrupt.
6	R/W	0x0	SOT_ERR_D2_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
5	R/W	0x0	SOT_ERR_D1_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
4	R/W	0x0	SOT_ERR_D0_INT DPHY RX detected SOT sequence with 1-bit error at Data Lane 0 interrupt.
3	R/W	0x0	SOT_D3_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 3 interrupt.
2	R/W	0x0	SOT_D2_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 2 interrupt.
1	R/W	0x0	SOT_D1_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 1 interrupt.
0	R/W	0x0	SOT_D0_INT 0: Disable 1: Enable DPHY RX detected SOT sequence at Data Lane 0 interrupt.

7.3.6.68. DPHY_INT_EN1_REG(Default Value: 0x0000_0000)

Offset:0x1064			**Register Name: DPHY_INT_EN1_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FALSE_CTL_D3_INT A false control occurs at Data Lane 3 interrupt.
30	R/W	0x0	FALSE_CTL_D2_INT A false control occurs at Data Lane 2 interrupt.
29	R/W	0x0	FALSE_CTL_D1_INT A false control occurs at Data Lane 1 interrupt.
28	R/W	0x0	FALSE_CTL_D0_INT A false control occurs at Data Lane 0 interrupt.
27	R/W	0x0	ESC_CMD_ERR_D3_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 3 interrupt.
26	R/W	0x0	ESC_CMD_ERR_D2_INT

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			DPHY RX received cannot recognize the Escape Entry Command at Data Lane 2 interrupt.
25	R/W	0x0	ESC_CMD_ERR_D1_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 1 interrupt.
24	R/W	0x0	ESC_CMD_ERR_D0_INT DPHY RX received cannot recognize the Escape Entry Command at Data Lane 0 interrupt.
23	R/W	0x0	RST_D3_INT DPHY RX detected Reset Trigger sequence at Data Lane 3 interrupt.
22	R/W	0x0	RST_D2_INT DPHY RX detected Reset Trigger sequence at Data Lane 2 interrupt.
21	R/W	0x0	RST_D1_INT DPHY RX detected Reset Trigger sequence at Data Lane 1 interrupt.
20	R/W	0x0	RST_D0_INT DPHY RX detected Reset Trigger sequence at Data Lane 0 interrupt.
19	R/W	0x0	UNDEF5_D0_INT DPHY RX received undefined 5 sequence at Data Lane 0 interrupt.
18	R/W	0x0	UNDEF4_D0_INT DPHY RX received undefined 4 sequence at Data Lane 0 interrupt.
17	R/W	0x0	UNDEF3_D0_INT DPHY RX received undefined 3 sequence at Data Lane 0 interrupt.
16	R/W	0x0	UNDEF2_D0_INT DPHY RX received undefined 2 sequence at Data Lane 0 interrupt.
15	R/W	0x0	UNDEF1_D0_INT DPHY RX received undefined 1 sequence at Data Lane 0 interrupt.
14	R/W	0x0	TX_TRND_ERR_D0_INT DPHY TX turn around error at Data Lane 0 interrupt.
13	R/W	0x0	RX_TRND_D0_INT DPHY RX received turn around sequence at Data Lane 0 interrupt.
12	R/W	0x0	LPDT_D0_INT DPHY RX complete LPDT transfer at Data Lane 0 interrupt.
11:10	/	/	/
9	R/W	0x0	ULPS_WP_CLK_INT DPHY RX detected ULPS wakeup at Clock Lane interrupt.
8	R/W	0x0	ULPS_CLK_INT DPHY RX detected ULPS sequence at Clock Lane interrupt.
7	R/W	0x0	ULPS_WP_D3_INT DPHY RX detected ULPS wakeup at Data Lane 3 interrupt.
6	R/W	0x0	ULPS_WP_D2_INT DPHY RX detected ULPS wakeup at Data Lane 2 interrupt.
5	R/W	0x0	ULPS_WP_D1_INT DPHY RX detected ULPS wakeup at Data Lane 1 interrupt.
4	R/W	0x0	ULPS_WP_D0_INT

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			DPHY RX detected ULPS wakeup at Data Lane 0 interrupt.
3	R/W	0x0	ULPS_D3_INT DPHY RX detected ULPS sequence at Data Lane 3 interrupt.
2	R/W	0x0	ULPS_D2_INT DPHY RX detected ULPS sequence at Data Lane 2 interrupt.
1	R/W	0x0	ULPS_D1_INT DPHY RX detected ULPS sequence at Data Lane 1 interrupt.
0	R/W	0x0	ULPS_D0_INT DPHY RX detected ULPS sequence at Data Lane 0 interrupt.

7.3.6.69. DPHY_INT_EN2_REG(Default Value: 0x0000_0000)

Offset:0x1068			Register Name: DPHY_INT_EN2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

7.3.6.70. DPHY_INT_PD0_REG(Default Value: 0x0000_0000)

Offset:0x1070			Register Name: DPHY_INT_PD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CD_LP1_ERR_D3_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
30	R/W1C	0x0	CD_LP0_ERR_D3_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
29	R/W1C	0x0	CD_LP1_ERR_D2_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
28	R/W1C	0x0	CD_LP0_ERR_D2_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
27	R/W1C	0x0	CD_LP1_ERR_D0_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
26	R/W1C	0x0	CD_LP0_ERR_D0_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
25	R/W1C	0x0	CD_LP1_ERR_D1_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
24	R/W1C	0x0	CD_LP0_ERR_D1_PD

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			Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
23	R/W1C	0x0	CD_LP1_ERR_CLK_PD Contention Detection detects LP1 error interrupt pending. Write "1" to clear.
22	R/W1C	0x0	CD_LP0_ERR_CLK_PD Contention Detection detects LP0 error interrupt pending. Write "1" to clear.
21:16	/	/	/
15	R/W	0x0	RX_ALG_ERR_D3_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
14	R/W	0x0	RX_ALG_ERR_D2_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
13	R/W	0x0	RX_ALG_ERR_D1_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
12	R/W	0x0	RX_ALG_ERR_D0_PD Asserted if the payload that DPHY RX received is not aligned to 8bit or 9bit, which depends on HSRX_8B9B_EN.
11	R/W1C	0x0	SOT_SYNC_ERR_D3_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane 3. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
10	R/W1C	0x0	SOT_SYNC_ERR_D2_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane 2. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
9	R/W1C	0x0	SOT_SYNC_ERR_D1_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane 1. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
8	R/W1C	0x0	SOT_SYNC_ERR_D0_PD Asserted if DPHY RX cannot detect SOT sequence at Data Lane 0. The SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected. Write "1" to clear.
7	R/W1C	0x0	SOT_ERR_D3_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 3. The confidence in the payload data is lower. Write "1" to clear.
6	R/W1C	0x0	SOT_ERR_D2_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 2. The confidence in the payload data is lower. Write "1" to clear.
5	R/W1C	0x0	SOT_ERR_D1_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data

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			Lane 1. The confidence in the payload data is lower. Write "1" to clear.
4	R/W1C	0x0	SOT_ERR_D0_PD Asserted if DPHY RX detected SOT sequence with 1-bit error at Data Lane 0. The confidence in the payload data is lower. Write "1" to clear.
3	R/W1C	0x0	SOT_D3_PD Asserted if DPHY RX detected SOT sequence at Data Lane 3.Write "1" to clear.
2	R/W1C	0x0	SOT_D2_PD Asserted if DPHY RX detected SOT sequence at Data Lane 2.Write "1" to clear.
1	R/W1C	0x0	SOT_D1_PD Asserted if DPHY RX detected SOT sequence at Data Lane 1.Write "1" to clear.
0	R/W1C	0x0	SOT_D0_PD Asserted if DPHY RX detected SOT sequence at Data Lane 0.Write "1" to clear.

7.3.6.71. DPHY_INT_PD1_REG(Default Value: 0x0000_0000)

Offset:0x1074			Register Name: DPHY_INT_PD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FALSE_CTL_D3_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
30	R/W1C	0x0	FALSE_CTL_D2_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
29	R/W1C	0x0	FALSE_CTL_D1_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
28	R/W1C	0x0	FALSE_CTL_D0_PD Asserted if a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape sequence or a HS-Rqst (LP-01) is not correctly followed by a Bridge State (LP-00).Write "1" to clear.
27	R/W1C	0x0	ESC_CMD_ERR_D3_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 3. Write "1" to clear.
26	R/W1C	0x0	ESC_CMD_ERR_D2_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 2. Write "1" to clear.

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25	R/W1C	0x0	ESC_CMD_ERR_D1_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 1. Write "1" to clear.
24	R/W1C	0x0	ESC_CMD_ERR_D0_PD Asserted if DPHY RX received cannot recognize the Escape Entry Command at Data Lane 0. Write "1" to clear.
23	R/W1C	0x0	RST_D3_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 3.Write "1" to clear.
22	R/W1C	0x0	RST_D2_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 2.Write "1" to clear.
21	R/W1C	0x0	RST_D1_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 1.Write "1" to clear.
20	R/W1C	0x0	RST_D0_PD Asserted if DPHY RX detected Reset Trigger sequence at Data Lane 0.Write "1" to clear.
19	R/W1C	0x0	UNDEF5_D0_PD Asserted if DPHY RX received undefined 5 sequence ("10100000") at Data Lane 0. Write "1" to clear.
18	R/W1C	0x0	UNDEF4_D0_PD Asserted if DPHY RX received undefined 4 sequence ("00100001") at Data Lane 0. Write "1" to clear.
17	R/W1C	0x0	UNDEF3_D0_PD Asserted if DPHY RX received undefined 3 sequence ("01011101") at Data Lane 0. Write "1" to clear.
16	R/W1C	0x0	UNDEF2_D0_PD Asserted if DPHY RX received undefined 2 sequence ("11011110") at Data Lane 0 . Write "1" to clear.
15	R/W1C	0x0	UNDEF1_D0_PD Asserted if DPHY RX received undefined 1 sequence ("10011111") at Data Lane 0. Write "1" to clear.
14	R/W1C	0x0	TX_TRND_ERR_D0_PD Asserted if DPHY TX turn around error at Data Lane 0. Write "1" to clear.
13	R/W1C	0x0	RX_TRND_D0_PD Asserted if DPHY RX received turn around sequence at Data Lane 0. Write "1" to clear.
12	R/W1C	0x0	LPDT_D0_PD Asserted if DPHY RX complete LPDT transfer at Data Lane 0. Write "1" to clear.
11:10	/	/	/
9	R/W1C	0x0	ULPS_WP_CLK_PD

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			Asserted if DPHY RX detected ULPS wakeup at Clock Lane. Write "1" to clear.
8	R/W1C	0x0	ULPS_CLK_PD Asserted if DPHY RX detected ULPS sequence at Clock Lane. Write "1" to clear.
7	R/W1C	0x0	ULPS_WP_D3_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 3. Write "1" to clear.
6	R/W1C	0x0	ULPS_WP_D2_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 2. Write "1" to clear.
5	R/W1C	0x0	ULPS_WP_D1_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 1. Write "1" to clear.
4	R/W1C	0x0	ULPS_WP_D0_PD Asserted if DPHY RX detected ULPS wakeup at Data Lane 0. Write "1" to clear.
3	R/W1C	0x0	ULPS_D3_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 3. Write "1" to clear.
2	R/W1C	0x0	ULPS_D2_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 2. Write "1" to clear.
1	R/W1C	0x0	ULPS_D1_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 1. Write "1" to clear.
0	R/W1C	0x0	ULPS_D0_PD Asserted if DPHY RX detected ULPS sequence at Data Lane 0. Write "1" to clear.

7.3.6.72. DPHY_DBG0_REG(Default Value: 0x0000_0000)

Offset: 0x10E0			**Register Name: DPHY_DBG0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x0	DIRECTION 0: No lane switch into HS transmission 1: At least one lane switch into HS transmission
27:19	/	/	/
18:16	R	0x0	LPTX_STA_CLK 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST

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			011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
15	/	/	/
14:12	R	0x0	LPTX_STA_D3 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
11	/	/	/
10:8	R	0x0	LPTX_STA_D2 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
7	/	/	/
6:4	R	0x0	LPTX_STA_D1 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST
3	/	/	/
2:0	R	0x0	LPTX_STA_D0 000: STP_ST 001: HSRQ_ST 010: ESRQ_ST 011: TNRD_ST 100: ULPS_ST 101: HS_ST 110: ESP_ST 111: RX_ST

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7.3.6.73. DPHY_DBG1_REG(Default Value: 0x0000_0000)

Offset: 0x10E4			Register Name: DPHY_DBG1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	LPTX_SET_CK Clock Lane output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
11:10	R/W	0x0	LPTX_SET_D3 Data Lane 3 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
9:8	R/W	0x0	LPTX_SET_D2 Data Lane 2 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
7:6	R/W	0x0	LPTX_SET_D1 Data Lane 1 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
5:4	R/W	0x0	LPTX_SET_D0 Data Lane 0 output state as follow: 00: LP-00 01: LP-01 10: LP-10 11: LP-11
3:2	/	/	/
1	R/W	0x0	HSTX_DBG_EN 0: normal mode 1: debug mode
0	R/W	0x0	LPTX_DBG_EN 0: normal mode 1: debug mode

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7.3.6.74. DPHY_DBG2_REG(Default Value: 0x0000_0000)

Offset: 0x10E8			Register Name: DPHY_DBG2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HSTX_DATA Bit31-24: D3_DATA Bit23-16: D2_DATA Bit15-08: D1_DATA Bit07-00: D0_DATA

7.3.6.75. DPHY_DBG3_REG(Default Value: 0x0000_0000)

Offset:0x10EC			Register Name: DPHY_DBG3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R	0x0	LPRX_STA_CLK 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010:UDF1S 1011:UDF2S 1100:UDF3S 1101:UDF4S 1110:UDF5S
15:12	R	0x0	LPRX_STA_D3 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010:UDF1S 1011:UDF2S

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			1100:UDF3S 1101:UDF4S 1110:UDF5S
11:8	R	0x0	LPRX_STA_D2 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010:UDF1S 1011:UDF2S 1100:UDF3S 1101:UDF4S 1110:UDF5S
7:4	R	0x0	LPRX_STA_D1 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS 1001: RSETS 1010:UDF1S 1011:UDF2S 1100:UDF3S 1101:UDF4S 1110:UDF5S
3:0	R	0x0	LPRX_STA_D0 0000: LP00S 0001: LP01S 0010: LP10S 0011: LP11S 0100: TRNDS 0101: HS_S 0110: LPDTS 0111: ESCPS 1000: ULPSS

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			1001: RSETS 1010:UDF1S 1011:UDF2S 1100:UDF3S 1101:UDF4S 1110:UDF5S

7.3.6.76. DPHY_DBG4_REG(Default Value: 0x0000_0000)

Offset:0x10F0			Register Name: DPHY_DBG4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	LPCD_PHY_CLK 00: LP-00 01: LP-01 10: LP-10 11: LP-11
23:22	R/W	0x0	LPCD_PHY_D3 00: LP-00 01: LP-01 10: LP-10 11: LP-11
21:20	R/W	0x0	LPCD_PHY_D2 00: LP-00 01: LP-01 10: LP-10 11: LP-11
19:18	R/W	0x0	LPCD_PHY_D1 00: LP-00 01: LP-01 10: LP-10 11: LP-11
17:16	R/W	0x0	LPCD_PHY_D0 00: LP-00 01: LP-01 10: LP-10 11: LP-11
15:10	/	/	/
9:8	R/W	0x0	LPRX_PHY_CLK 00: LP-00 01: LP-01 10: LP-10 11: LP-11
7:6	R/W	0x0	LPRX_PHY_D3

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			00: LP-00 01: LP-01 10: LP-10 11: LP-11
5:4	R/W	0x0	LPRX_PHY_D2 00: LP-00 01: LP-01 10: LP-10 11: LP-11
3:2	R/W	0x0	LPRX_PHY_D1 00: LP-00 01: LP-01 10: LP-10 11: LP-11
1:0	R/W	0x0	LPRX_PHY_D0 00: LP-00 01: LP-01 10: LP-10 11: LP-11

7.3.6.77. DPHY_DBG5_REG(Default Value: 0x0000_0000)

Offset:0x10F4			Register Name: DPHY_DBG5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HSRX_DATA Bit31-24: LANE_D3 Bit23-16: LANE_D2 Bit15-08: LANE_D1 Bit07-00: LANE_D0

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7.4. TV Encoder

7.4.1. Overview

The TV Encoder(TVE) module is a highly programmable digital video encoder supporting worldwide video standards Composite Video Broadcast Signal (CVBS).

The TVE includes the following features:

- 1 channel CVBS, PAL and NTSC supported
- Plug status auto detecting
- 10 bits DAC output

7.4.2. Block Diagram

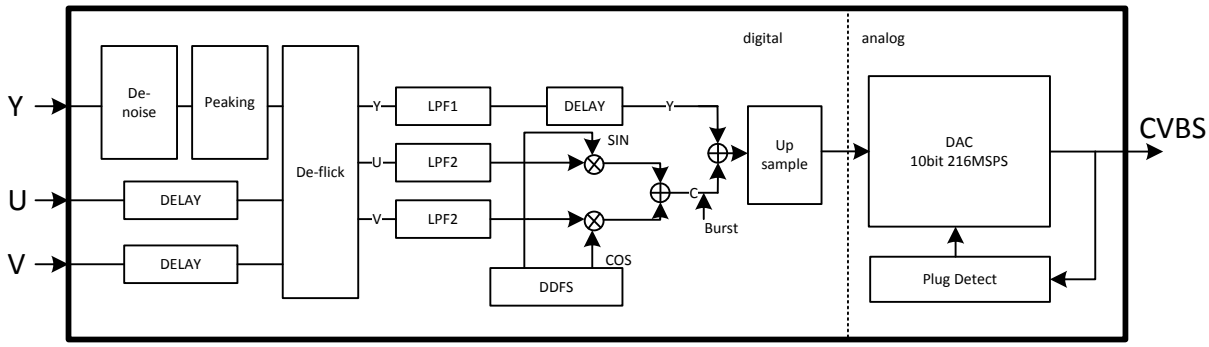

Figure 7- 31. TVE Block Diagram

7.4.3. Operations and Functional Descriptions

7.4.3.1. External Signals

Table 7-20 describes the external signals of TVE.

Table 7- 20. TVE External Signals

Pin Name	Function Description	Type
TV-VCC	TV DAC power	P
TV-OUT	TV CVBS output	AO

7.4.3.2. Clock Sources

The TVE module requires one clock with 50% duty. Digital circuit and Analog circuit work by this clock. Mode and

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Clock frequency is shown below.

Table 7- 21. TVE Clock Sources

Mode	TVE Clock Frequency
NTSC	216MHz
PAL	216MHz

7.4.4. Programming Guidelines

(1) Operate TVE module by the following step, the process is shown in Figure 7-32.

Step1: Set CCU clock source for TVE, and release AHB bus, and module reset.

Step2: Initial DAC amplitude value from efuse calibration value which has burned.

Step3: Enable plug-in detect function, and detect plug-in status every 200ms.

Step4: When plug-in has detected, configure TVE module to output mode setting by application.

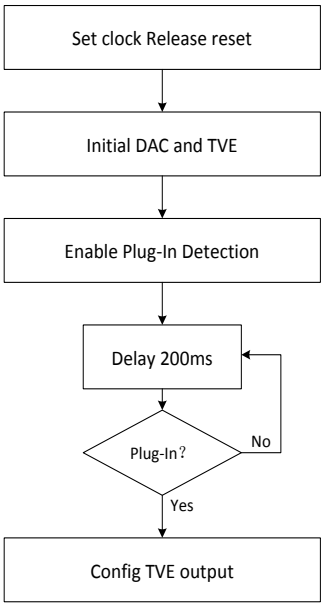

Figure 7- 32. Operate TVE Process

(2) Auto Detect Function

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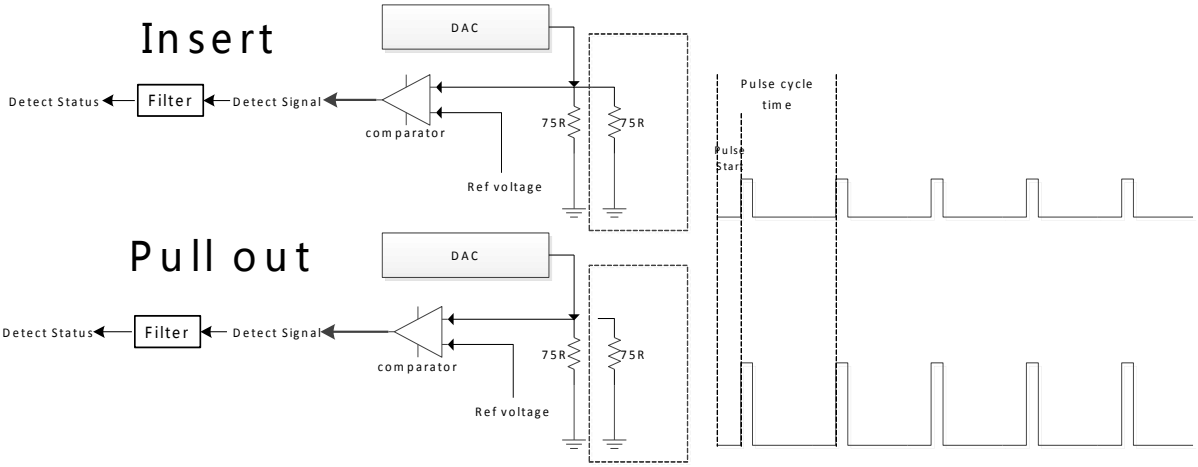

Figure 7- 33. Auto Detect Function

DAC outputs constant current, when insert, external load is 37.5Ω; when pull out, external load is 75Ω. The method that comparator judges pin level can detect plug action.

Because plug action may exist jitter, then there need be a filter to filter jitter, the debounce time of filter is set through the bit[3:0] of TV Encoder Auto Detection de-bounce Setting Register.

The pulse cycle time can be set through the bit[30:16] of TV Encoder Auto Detect Configuration Register1, the pulse start time can be set through the bit[14:0] of TV Encoder Auto Detect Configuration Register1.The clock sources of the two time are 32KHz clock.

Pulse width is cycle time of 4 clock sources.

Pulse amplitude can be set through the bit[9:0] of TV Encoder Auto Detect Configuration Register0.

(3) DAC Calibration

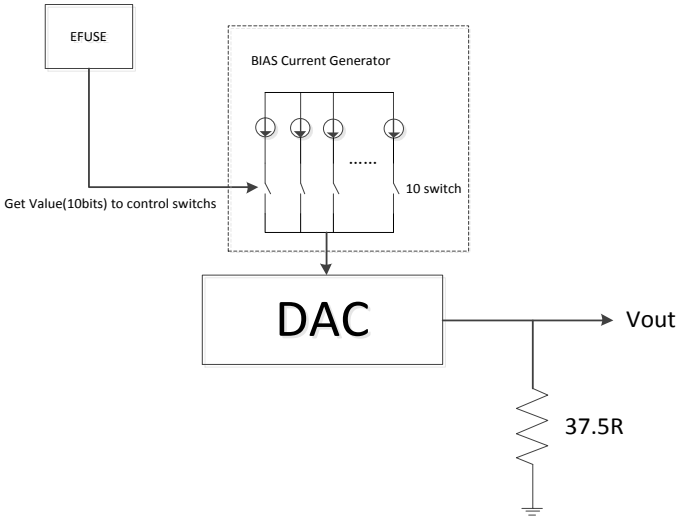

Figure 7- 34. DAC Calibration

After FT, 10-bit calibration value is burned into efuse. Every time software can read the 10-bit calibration value from

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efuse, to control BIAS current and BIAS current switch, then a specific BIAS current is generated to calibrate maximum output voltage of DAC.

7.4.5. Register List

Module Name	Base Address
TVE_TOP	0x06520000
TVE	0x06524000

Register Name	Offset	Description
TVE_TOP		
TVE_DAC_MAP	0x0020	TV Encoder DAC MAP Register
TVE_DAC_STATUS	0x0024	TV Encoder DAC STAUTS Register
TVE_DAC_CFG0	0x0028	TV Encoder DAC CFG0 Register
TVE_DAC_CFG1	0x002C	TV Encoder DAC CFG1 Register
TVE_DAC_CFG2	0x0030	TV Encoder DAC CFG2 Register
TVE_DAC_CFG3	0x0034	TV Encoder DAC CFG2 Register
TVE_DAC_TEST	0x00F0	TV Encoder DAC TEST Register
TVE		
TVE_000_REG	0x0000	TV Encoder Clock Gating Register
TVE_004_REG	0x0004	TV Encoder Configuration Register
TVE_008_REG	0x0008	TV Encoder DAC Register1
TVE_00C_REG	0x000C	TV Encoder Notch and DAC Delay Register
TVE_010_REG	0x0010	TV Encoder Chroma Frequency Register
TVE_014_REG	0x0014	TV Encoder Front/Back Porch Register
TVE_018_REG	0x0018	TV Encoder HD Mode VSYNC Register
TVE_01C_REG	0x001C	TV Encoder Line Number Register
TVE_020_REG	0x0020	TV Encoder Level Register
TVE_024_REG	0x0024	TV Encoder DAC Register2
TVE_030_REG	0x0030	TV Encoder Auto Detection Enable Register
TVE_034_REG	0x0034	TV Encoder Auto Detection Interrupt Status Register
TVE_038_REG	0x0038	TV Encoder Auto Detection Status Register
TVE_03C_REG	0x003C	TV Encoder Auto Detection De-bounce Setting Register
TVE_0F8_REG	0x00F8	TV Encoder Auto Detect Configuration Register0
TVE_0FC_REG	0x00FC	TV Encoder Auto Detect Configuration Register1
TVE_100_REG	0x0100	TV Encoder Color Burst Phase Reset Configuration Register
TVE_104_REG	0x0104	TV Encoder VSYNC Number Register
TVE_108_REG	0x0108	TV Encoder Notch Filter Frequency Register
TVE_10C_REG	0x010C	TV Encoder Cb/Cr Level/Gain Register
TVE_110_REG	0x0110	TV Encoder Tint and Color Burst Phase Register
TVE_114_REG	0x0114	TV Encoder Burst Width Register
TVE_118_REG	0x0118	TV Encoder Cb/Cr Gain Register

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Register Name	Offset	Description
TVE_11C_REG	0x011C	TV Encoder Sync and VBI Level Register
TVE_120_REG	0x0120	TV Encoder White Level Register
TVE_124_REG	0x0124	TV Encoder Video Active Line Register
TVE_128_REG	0x0128	TV Encoder Video Chroma BW and CompGain Register
TVE_12C_REG	0x012C	TV Encoder Register
TVE_130_REG	0x0130	TV Encoder Re-sync Parameters Register
TVE_134_REG	0x0134	TV Encoder Slave Parameter Register
TVE_138_REG	0x0138	TV Encoder Configuration Register0
TVE_13C_REG	0x013C	TV Encoder Configuration Register1
TVE_380_REG	0x0380	TV Encoder Low Pass Control Register
TVE_384_REG	0x0384	TV Encoder Low Pass Filter Control Register
TVE_388_REG	0x0388	TV Encoder Low Pass Gain Register
TVE_38C_REG	0x038C	TV Encoder Low Pass Gain Control Register
TVE_390_REG	0x0390	TV Encoder Low Pass Shoot Control Register
TVE_394_REG	0x0394	TV Encoder Low Pass Coring Register
TVE_3A0_REG	0x03A0	TV Encoder Noise Reduction Register

7.4.6. Register Description

7.4.6.1. TV Encoder DAC MAP Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TVE_DAC_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DAC_MAP 000: OUT0 Others: Reserved
3:2	/	/	/
1:0	R/W	0x0	DAC_SEL 00: Reserved 01: TVE0 10: Reserved 11: Reserved

7.4.6.2. TV Encoder DAC Status Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TVE_DAC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	DAC_STATUS 00: Unconnected

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Offset: 0x0024			Register Name: TVE_DAC_STATUS
Bit	Read/Write	Default/Hex	Description
			01: Connected 11: Short to ground 10: Reserved

7.4.6.3. TV Encoder DAC Configuration0 Register(Default Value: 0x8000_4200)

Offset: 0x0028			Register Name: TVE_DAC_CFG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x1	DAC_CLOCK_INVERT 0: Not invert 1: Invert
30:26	/	/	/
25:16	R/W	0x0	CALI_IN
15:12	R/W	0x4	Reserved
11:10	/	/	/
9	R/W	0x1	Reserved
8	R/W	0x0	Reserved
7:5	/	/	/
4	R/W	0x0	Reserved
3:1	/	/	/
0	R/W	0x0	DAC_EN 0: Disable 1: Enable

7.4.6.4. TV Encoder DAC Configuration1 Register(Default Value: 0x0000_023A)

Offset: 0x002C			Register Name: TVE_DAC_CFG1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x2	Reserved
7:6	/	/	/
5:4	R/W	0x3	REF2_SEL 00: 0.25V 01: 0.30V 10: 0.35V 11: 0.40V (a_refslct2<1:0>)
3:0	R/W	0xA	REF1_SEL 0000: 0.50V 0001: 0.55V

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Offset: 0x002C			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0010: 0.60V 0011: 0.65V 0100: 0.70V 0101: 0.75V 0110: 0.80V 0111: 0.85V 1000: 0.90V 1001: 0.95V 1010: 1.00V 1011: 1.05V 1100: 1.10V 1101: 1.15V 1110: 1.20V 1111: 1.25V (a_refslct1<3:0>) The reference voltage is used for hot plug detect function.

7.4.6.5. TV Encoder DAC Configuration2 Register(Default Value: 0x0000_0010)

Offset: 0x0030			Register Name: TVE_DAC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:6	R/W	0x0	Reserved
5:0	R/W	0x10	Reserved

7.4.6.6. TV Encoder DAC Configuration3 Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TVE_DAC_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	FORCE_DATA_SET Force DAC input data
15:1	/	/	/
0	R/W	0x0	FORCE_DATA_EN 0:DAC input data from TVE 1: DAC input data from FORCE_DATA_SET

7.4.6.7. TV Encoder DAC Test Register(Default Value: 0x0000_0000)

Offset: 0x00F0	Register Name: TVE_DAC_TEST

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Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	DAC_TEST_LENGTH DAC TEST DATA LENGTH
15:6	/	/	/
5:4	R/W	0x0	DAC_TEST_SEL 00: DAC0 01: DAC1 10: DAC2 11: DAC3
3:1	/	/	/
0	R/W	0x0	DAC_TEST_ENABLE 0: Reserved 1: Repeat DAC data from DAC sram

7.4.6.8. TV Encoder Clock Gating Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVE_000_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLOCK_GATE_DIS 0: Enable 1: Disable
30:29	/	/	/
28	R/W	0x0	BIST_EN 0: Normal mode 1: Bist mode
27:23	/	/	/
22	R/W	0x0	upsample for YPbPr 0:1x 1:2x
21:20	R/W	0x0	upsample for CVBS Out up sample 00: 27MHz 01: 54MHz 10: 108MHz 11: 216MHz
19:1	/	/	/
0	R/W	0x0	TVE_EN 0: Disable 1: Enable Video Encoder enable, default disable, write 1 to take it out of the reset state

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7.4.6.9. TV Encoder Configuration Register(Default Value: 0x0001_0000)

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	BYPASS_TV 0: Disable 1: Enable
28:27	R/W	0x0	DAC_SRC_SEL 00: TV Encoder 01: LCD controller, override all other TV encoder setting, the DAC clock can from LCD controller. 10: DAC test mode,DAC using DAC clock 11: DAC test mode, DAC using AHB clock
26	R/W	0x0	DAC_CONTROL_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
25	R/W	0x0	CORE_DATAPATH_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
24	R/W	0x0	CORE_CONTROL_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
23:21	/	/	/
20	R/W	0x0	CB_CR_SEQ_FOR_422_MODE 0: Cb first 1: Cr first
19	R/W	0x0	INPUT_CHROMA_DATA_SAMPLING_RATE_SEL 0: 4:4:4 1: 4:2:2
18	R/W	0x0	YUV_RGB_OUTPUT_EN 0: CVBS 1: Reserved
17	R/W	0x0	YC_EN S-port Video enable Selection. 0: Y/C is disable 1: Reserved This bit selects whether the S-port(Y/C) video output is enabled or disabled.
16	R/W	0x1	CVBS_EN Composite video enables selection 0: Composite video is disabled, Only Y/C is enabled 1: Composite video is enabled., CVBS and Y/C are enabled This bit selects whether the composite video output (CVBS) is enabled or disabled.
15:10	/	/	/

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Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W	0x0	COLOR_BAR_TYPE 0: 75/7.5/75/7.5 (NTSC), 100/0/75/0(PAL) 1: 100/7.5/100/7.5(NTSC), 100/0/100/0(PAL)
8	R/W	0x0	COLOR_BAR_MODE Standard Color bar input selection 0: The Video Encoder input is coming from the Display Engineer 1: The Video Encoder input is coming from an internal standard color bar generator. This bit selects whether the Video Encoder video data input is replaced by an internal standard color bar generator or not.
7:5	/	/	/
4	R/W	0x0	MODE_1080I_1250LINE_SEL 0: 1125 Line mode 1: 1250 Line mode
3:0	R/W	0x0	TVMODE_SELECT 0000: NTSC 0001: PAL 0010: Reserved 0011: Reserved 01xx: Reserved 100x: Reserved 101x: Reserved 110x: Reserved 111x: Reserved **NOTE** **Changing this register value will cause some relative register setting to relative value.**

7.4.6.10. TV Encoder DAC Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TVE_008_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DAC0_SRC_SEL 000: Composite Others: Reserved
3:0	/	/	/

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7.4.6.11. TV Encoder Notch and DAC Delay Register(Default Value: 0x0201_4924)

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CHROMA_FILTER_ACTIVE_VALID 0: Disable 1: Enable
30	R/W	0x0	LUMA_FILTER_LTI_ENABLE 0: Disable Luma filter lti 1: Enable Luma filter lti
27:25	R/W	0x1	Y_DELAY_BEFORE_DITHER
24	R/W	0x0	HD_MODE_CB_FILTER_BYPASS 0: Bypass Enable 1: Bypass Disable
23	R/W	0x0	HD_MODE_CR_FILTER_BYPASS 0: Bypass Enable 1: Bypass Disable
22	R/W	0x0	CHROMA_FILTER_1_444_EN 0: Chroma Filter 1 444 Disable 1: Chroma Filter 1 444 Enable
21	R/W	0x0	CHROMA_HD_MODE_FILTER_EN 0: Chroma HD Filter Disable 1: Chroma HD Filter Enable
20	R/W	0x0	CHROMA_FILTER_STAGE_1_BYPASS 0: Chroma Filter Stage 1 Enable 1: Chroma Filter Stage 1 bypass
19	R/W	0x0	CHROMA_FILTER_STAGE_2_BYPASS 0: Chroma Filter Stage 2 Enable 1: Chroma Filter Stage 2 bypass
18	R/W	0x0	CHROMA_FILTER_STAGE_3_BYPASS 0: Chroma Filter Stage 3 Enable 1: Chroma Filter Stage 3 bypass
17	R/W	0x0	LUMA_FILTER_BYPASS 0: Luma Filter Enable 1: Luma Filter bypass
16	R/W	0x1	NOTCH_EN 0: The luma notch filter is bypassed 1: The luma notch filter is operating Luma notch filter on/off selection **NOTE** **This bit selects if the luma notch filter is operating or bypassed.**
15:12	R/W	0x4	C_DELAY_BEFORE_DITHER
11:0	R/W	0x924	Reserved

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7.4.6.12. TV Encoder Chroma Frequency Register(Default Value: 0x21F0_7C1F)

Offset: 0x0010			Register Name: TVE_010_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21f07c1f	CHROMA_FREQ Specify the ratio between the color burst frequency. 32 bits unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455 MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'): PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

7.4.6.13. TV Encoder Front/Back Porch Register(Default Value: 0x0076_0020)

Offset: 0x0014			Register Name: TVE_014_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x76	BACK_PORCH Specify the width of the back porch in encoder clock cycles. Min value is (*burst_width+breeze_way*+17*)*. 8 bits unsigned integer. 720p mode, is 260 1080i/p mode, is 192
15:12	/	/	/
11:0	R/W	0x20	FRONT_PORCH Must be even. Specify the width of the front porch in encoder clock cycles. 6 bits unsigned even integer. Allowed range is 10 to 62. In 1080i mode the value is 44.

7.4.6.14. TV Encoder HD Mode VSYNC Register(Default Value: 0x0000_0016)

Offset: 0x0018			Register Name: TVE_018_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BROAD_PLUS_CYCLE_NUMBER_IN_HD_MODE_VSYNC
15:12	/	/	/
11:0	R/W	0x16	FRONT_PORCH_LIKE_IN_HD_MODE_VSYNC

7.4.6.15. TV Encoder Line Number Register(Default Value: 0x0016_020D)

Offset: 0x001C			Register Name: TVE_01C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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Offset: 0x001C			Register Name: TVE_01C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x16	FIRST_VIDEO_LINE Specify the index of the first line in a field/frame to have active video. 8 bits unsigned integer. For interlaced video: When VSync5=B'0', FirstVideoLine is restricted to be greater than 7. When VSync5=B'1', FirstVideoLine is restricted to be greater than 9.
15:11	/	/	/
10:0	R/W	0x20D	NUM_LINES Specify the total number of lines in a video frame. 11 bits unsigned integer. Allowed range is 0 to 2048. For interlaced video: When NTSC, and FirstVideoLine is greater than 20, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When NTSC, and FirstVideoLine is not greater than 20, then NumLines is restricted to be greater than 77. When PAL, and FirstVideoLine is greater than 22, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When PAL, and FirstVideoLine is not greater than 22, then NumLines is restricted to be greater than 81. If NumLines is even, then it is restricted to be divisible by 4. If NumLines is odd, then it is restricted to be divisible by 4 with a remainder of 1.

7.4.6.16. TV Encoder Level Register(Default Value: 0x00F0_011A)

Offset: 0x0020			Register Name: TVE_020_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0xf0	BLANK_LEVEL Specify the blank level setting for active lines. 10 bits unsigned integer. Allowed range is from 0 to 1023.
15:10	/	/	/
9:0	R/W	0x11a	BLACK_LEVEL Specify the black level setting. 10 bits unsigned integer. Allowed range is from 240 to 1023.

7.4.6.17. TV Encoder Auto Detection Enable Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: TVE_030_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DAC0_AUTO_DETECT_INTERRUPT_EN
15:1	/	/	/

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Offset: 0x0030			Register Name: TVE_030_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	DAC0_AUTO_DETECT_ENABLE

7.4.6.18. TV Encoder Auto Detection Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TVE_034_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DAC0_AUTO_DETECT_INTERRUPT_ACTIVE_FLAG Write 1 to inactive DAC0 auto detection interrupt

7.4.6.19. TV Encoder Auto Detection Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: TVE_038_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R	0x0	DAC0_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

7.4.6.20. TV Encoder Auto Detection Debounce Setting Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: TVE_03C_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	DAC_TEST_REGISTER DAC test register.
15:4	/	/	/
3:0	R/W	0x0	DAC0_DE_BOUNCE_TIMES The de_bounce time for hot plug detect function.

7.4.6.21. TV Encoder Auto Detection Configuration Register0(Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: TVE_0F8_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	DETECT_PULSE_VALUE

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Offset: 0x00F8			Register Name: TVE_0F8_REG
Bit	Read/Write	Default/Hex	Description
			Use for DAC data input at auto detect pluse. Set the pulse amplitude.

7.4.6.22. TV Encoder Auto Detection Configuration Register1(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TVE_0FC_REG
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:16	R/W	0x0	DETECT_PULSE_PERIODS Use 32K clock
15	/	/	/
14:0	R/W	0x0	DETECT_PULSE_START Detect signal start time

7.4.6.23. TV Encoder Color Burst Phase Reset Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0100			Register Name: TVE_100_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x1	COLOR_PHASE_RESET Color burst phase period selection These bits select the number of fields or lines after which the color burst phase is reset to its initial value as specified by the ChromaPhase parameter, This parameter is application only for interlaced video. 00: 8 field 01: 4 field 10: 2 lines 11: only once

7.4.6.24. TV Encoder VSYNC Number Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: TVE_104_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	VSync5 Number of equalization pulse selection This bit selects whether the number of equalization pulses is 5 or 6. This parameter is applicable only for interlaced video. 0: 5 equalization pulse(default) 1: 6 equalization pulses

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7.4.6.25. TV Encoder Notch Filter Frequency Register (Default Value: 0x0000_0002)

Offset: 0x0108			Register Name: TVE_108_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x2	NOTCH_FREQ Luma notch filter center frequency selection These bits select the luma notch filter (which is a band-reject filter) center frequency. In two of the selections, the filter width affects also the selection of the center frequency. 000: 1.1875 001: 1.1406 010: 1.0938 when notch_wide value is B‘1’ (this selection is proper for CCIR-NTSC), or 1.0000 when notch_wide value is B‘0’ 011: 0.9922. This selection is proper for NTSC with square pixels 100: 0.9531. This selection is proper for PAL with square pixel 101: 0.8359 when notch_wide value is B‘1’ (this selection is proper for CCIR-PAL), or 0.7734 when notch_wide value is B‘0’ 110: 0.7813 111: 0.7188

7.4.6.26. TV Encoder Cb/Cr Level/Gain Register (Default Value: 0x0000_004F)

Offset: 0x010C			Register Name: TVE_10C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	CR_BURST_LEVEL Specify the amplitude of the Cr burst. 8 bit 2’s complement integer. Allowed range is from (-127) to 127.
7:0	R/W	0x4f	CB_BURST_LEVEL Specify the amplitude of the Cb burst. 8 bit 2’s complement integer. Allowed range is from (-127) to 127.

7.4.6.27. TV Encoder Tint and Color Burst Phase Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: TVE_110_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	TINT Specify the tint adjustment of the chroma signal for CVBS and Y/C outputs. The adjustment is effected by setting the sub-carrier phase to the value of this parameter. 8.8 bit unsigned fraction. Units are cycles of the color burst frequency.

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Offset: 0x0110			Register Name: TVE_110_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:0	R/W	0x0	CHROMA_PHASE Specify the color burst initial phase (*ChromaPhase)*. 8.8 bit unsigned fraction. Units are cycles of the color burst frequency. The color burst is set to this phase at the first *HSYNC* and then reset to the same value at further *HSYNC*s as specified by the *CPhaseRset* bits of the *EncConfig5* parameter (see above)

7.4.6.28. TV Encoder Burst Width Register (Default Value: 0x0016_447E)

Offset: 0x0114			Register Name: TVE_114_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	BACK_PORCH Breezeway like in HD mode VSync 720p mode, is 220 2080i/p mode is 88(default)
23	/	/	/
22:16	R/W	0x16	BREEZEWAY Must be even. Specify the width of the breezeway in encoder clock cycles. 5 bit unsigned integer. Allowed range is 0 to 31. In 1080i mode, is 44 In 1080p mode, is 44 In 720p mode,is 40
15	/	/	/
14:8	R/W	0x44	BURST_WIDTH Specify the width of the color frequency burst in encoder clock cycles. 7 bit unsigned integer. Allowed range is 0 to 127. In hd mode, ignored
7:0	R/W	0x7e	HSYNC_WIDTH Specify the width of the horizontal sync pulse in encoder clock cycles. Min value is 16. Max value is (*FrontPorch + ActiveLine - BackPorch*). Default value is 126. The sum of *HSyncSize* and *BackPorch* is restricted to be divisible by 4. In 720p mode, is 40 In 1080i/p mode, is 44

7.4.6.29. TV Encoder Cb/Cr Gain Register (Default Value: 0x0000_A0A0)

Offset: 0x0118			Register Name: TVE_118_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

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Offset: 0x0118			Register Name: TVE_118_REG
Bit	Read/Write	Default/Hex	Description
15:8	R/W	0xa0	CR_GAIN Specify the Cr color gain. 8-bit unsigned fraction.
7:0	R/W	0xa0	CB_GAIN Specify the Cb color gain. 8-bit unsigned fraction.

7.4.6.30. TV Encoder Sync and VBI Level Register (Default Value: 0x0010_00F0)

Offset: 0x011C			Register Name: TVE_11C_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x10	SYNC_LEVEL Specify the sync pulse level setting. 8-bit unsigned integer. Allowed range is from 0 to *ABlankLevel*-1 or *VBlankLevel*-1 (whichever is smaller).
15:10	/	/	/
9:0	R/W	0xf0	VBLANK_LEVEL Specify the blank level setting for non active lines. 10-bit unsigned integer. Allow range is from 0 to 1023.

7.4.6.31. TV Encoder White Level Register (Default Value: 0x01E8_0320)

Offset: 0x0120			Register Name: TVE_120_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x1e8	HD_SYNC_BREEZEWAY_LEVEL Specify the breezeway level setting. 10-bit unsigned integer. Allowed range is from 0 to 1023.
15:10	/	/	/
9:0	R/W	0x320	WHITE_LEVEL Specify the white level setting. 10-bit unsigned integer. Allowed range is from black_level+1 or vbi_blank_level +1 (whichever is greater) to 1023.

7.4.6.32. TV Encoder Video Active Line Register (Default Value: 0x0000_05A0)

Offset: 0x0124			Register Name: TVE_124_REG
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x5A0	ACTIVE_LINE Specify the width of the video line in encoder clock cycles. 12-bit unsigned multiple of 4 integer. Allowed range is from 0 to 4092.

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7.4.6.33. TV Encoder Video Chroma BW and CompGain Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: TVE_128_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	CHROMA_BW Chroma filter bandwidth selection This bit specifies whether the bandwidth of the chroma filter is: 00: Narrow width 0.6MHz 01: Wide width 1.2MHz. 10: Extra width 1.8MHz 11: Ultra width 2.5MHz Default is 0.6MHz(value 0)
15:2	/	/	/
1:0	R/W	0x0	COMP_CH_GAIN Chroma gain selection for the composite video signal. These bits specify the gain of the chroma signal for composing with the luma signal to generate the composite video signal: 00: 100% 01: 25% 10: 50% 11: 75%

7.4.6.34. TV Encoder Register (Default Value: 0x0000_0101)

Offset: 0x012C			Register Name: TVE_12C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x1	NOTCH_WIDTH Luma notch filter width selection This bit selects the luma notch filter (which is a band-reject filter) width. 0: Narrow 1: Wide
7:1	/	/	/
0	R/W	0x1	COMP_YUV_EN This bit selects if the components video output are the RGB components or the YUV components. 0: The three component outputs are the RGB components. 1: The three component outputs are the YUV components, (i.e. the color conversion unit is by-passed)

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7.4.6.35. TV Encoder Re-sync Parameters Register (Default Value: 0x0010_0001)

Offset: 0x0130			Register Name: TVE_130_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RE_SYNC_FIELD Re-sync field
30	R/W	0x0	RE_SYNC_DIS 0: Re-Sync Enable 1: Re-Sync Disable
29:27	/	/	/
26:16	R/W	0x10	RE_SYNC_LINE_NUM Re-sync line number from TCON
15:11	/	/	/
10:0	R/W	0x1	RE_SYNC_PIXEL_NUM Re-sync line pixel from TCON

7.4.6.36. TV Encoder Slave Parameter Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: TVE_134_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	SLAVE_THRESH Horizontal line adjustment threshold selection This bit selects whether the number of lines after which the Video Encoder starts the horizontal line length adjustment is slave mode is 0 or 30. 0: Number of lines is 0 1: Number of lines is 30
7:1	/	/	/
0	R/W	0x0	SLAVE_MODE Slave mode selection This bit selects whether the Video Encoder is sync slave, partial slave or sync master. It should be set to B‘0’. 0: The Video Encoder is not a full sync slave (i.e. it is a partial sync slave or a sync master) 1: Reserved

7.4.6.37. TV Encoder Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: TVE_138_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	INVERT_TOP Field parity input signal (top_field) polarity selection.

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Offset: 0x0138			Register Name: TVE_138_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			This bit selects whether the top field is indicated by a high level of the field parity signal or by the low level. The bit is applicable both when the Video Encoder is the sync master and when the Video Encoder is the sync slave. 0: Top field is indicated by low level 1: Top field is indicated by high level
7:1	/	/	/
0	R/W	0x0	UV_ORDER This bit selects if the sample order at the chroma input to the Video Encoder is Cb first (i.e. Cb 0 Cr 0 Cb 1 Cr 1) or Cr first (i.e. Cr 0 Cb 0 Cr 1 Cb 1). 0: The chroma sample input order is Cb first 1: The chroma sample input order is Cr first

7.4.6.38. TV Encoder Configuration Register (Default Value: 0x0000_0001)

Offset: 0x013C			Register Name: TVE_13C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	RGB_SYNC R, G and B signals sync embedding selection. These bits specify whether the sync signal is added to each of the R, G and B components (b‘1’) or not (b‘0’). The bit[26] specify if the R signal has embedded syncs, the bit[25] specify if the G signal has embedded syncs and the bit[24] specify if the B signal has embedded syncs. When comp_yuv is equal to b‘1’, these bits are N.A. and should be set to b‘000’. When the value is different from b‘000’, **RGB_SETUP** should be set to b‘1’.
23:17	/	/	/
16	R/W	0x0	RGB_SETUP “Set-up” enable for RGB outputs. This bit specifies if the “set-up” implied value (black_level – blank_level) specified for the CVBS signal is used also for the RGB signals. 0: The “set-up” is not used, or i.e. comp_yuv is equal to b‘1’. 1: The implied “set-up” is used for the RGB signals
15:1	/	/	/
0	R/W	0x1	BYPASS_YCLAMP Y input clamping selection This bit selects whether the Video Encoder Y input is clamped to 64 to 940 or not. When not clamped the expected range is 0 to 1023. The U and V inputs are always clamped to the range 64 to 960. 0: The Video Encoder Y input is clamped 1: The Video Encoder Y input is not clamped

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7.4.6.39. TV Encoder Low Pass Control Register(Default Value: 0x0000_0000)

Offset: 0x0380			Register Name: TVE_380_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:10	R/W	0x0	USER_DEFLICKER_COEF up : coef/32 Center :1-coef/16 Down :coef/32
9	R/W	0x0	FIX_COEF_DEFLICKER 0: Auto deflicker 1: User deflicker
8	R/W	0x0	ENABLE_DEFLICKER 0: Disable deflicker 1: Enable deflicker
7:1	/	/	/
0	R/W	0x0	EN LP function enable 0: Disable 1: Enable

7.4.6.40. TV Encoder Low Pass Filter Control Register(Default Value: 0x0000_0000)

Offset: 0x0384			Register Name: TVE_384_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	R/W	0x0	HP_RATIO Default high-pass filter ratio In two complement,the range is from -31 to 31.
15:14	/	/	/
13:8	R/W	0x0	BP0_RATIO Default band-pass filter0 ratio In two complement,the range is from -31 to 31.
7:6	/	/	/
5:0	R/W	0x0	BP1_RATIO Default band-pass filter1 ratio In two complement,the range is from -31 to 31.

7.4.6.41. TV Encoder Low Pass Gain Register(Default Value: 0x0000_0000)

Offset: 0x0388			Register Name: TVE_388_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

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Offset: 0x0388			Register Name: TVE_388_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R/W	0x0	GAIN Peaking gain setting.

7.4.6.42. TV Encoder Low Pass Gain Control Register(Default Value: 0x0000_0000)

Offset: 0x038C			Register Name: TVE_38C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	DIF_UP Gain control: limitation threshold.
15:8	/	/	/
4:0	R/W	0x0	BETA Gain control: large gain limitation.

7.4.6.43. TV Encoder Low Pass Shoot Control Register(Default Value: 0x0000_0000)

Offset: 0x0390			Register Name: TVE_390_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	NEG_GAIN Undershoot gain control.

7.4.6.44. TV Encoder Low Pass Coring Register(Default Value: 0x0000_0000)

Offset: 0x0394			Register Name: TVE_394_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CORTHR Coring threshold.

7.4.6.45. TV Encoder Noise Reduction Register(Default Value: 0x0000_0000)

Offset: 0x03A0			Register Name: TVE_3A0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	T_Value
15:1	/	/	/
0	R/W	0x0	EN

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Chapter 8 Video Input Interfaces

8.1. CSIC

8.1.1. Overview

The CMOS Sensor Interface Controller(CSIC) is an image or video input control module which can receive image or video data over digital camera(DC) interface,BT.656 interface, BT601 interface, BT1120 interface ,high speed serial interface like MIPI. The controller can transfer valid data to embedded ISP or store the data in memory directly.And the CSIC has four built-in Camera Control Interface(CCI) that can be used for external device control.

The CSIC includes the following features:

- Supports 8-,10-,12-,16-bit DC interface
- Supports BT656,BT601,BT1120 interface
- Supports ITU-R BT.656/BT1120 time-multiplexed format
- Supports MIPI interface timing
- Supports DDR sample mode
- Supports image crop function
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution for parallel interface to 1080p@30fps
- Maximum pixel clock for parallel to 148.5MHz
- Maximum video capture resolution for MIPI to 8M@30fps

CCI

- Compatible with I2C transmission in 7 bit slave ID + 1 bit R/W
- Automatic transmission
- 0/8/16/32 bits register address supported
- 8/16/32 bits data supported
- 64 bytes FIFO input CCI data supported
- Synchronized with CSI signal and delay trigger supported
- Repeated transmission with sync signal supported

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8.1.2. Block Diagram

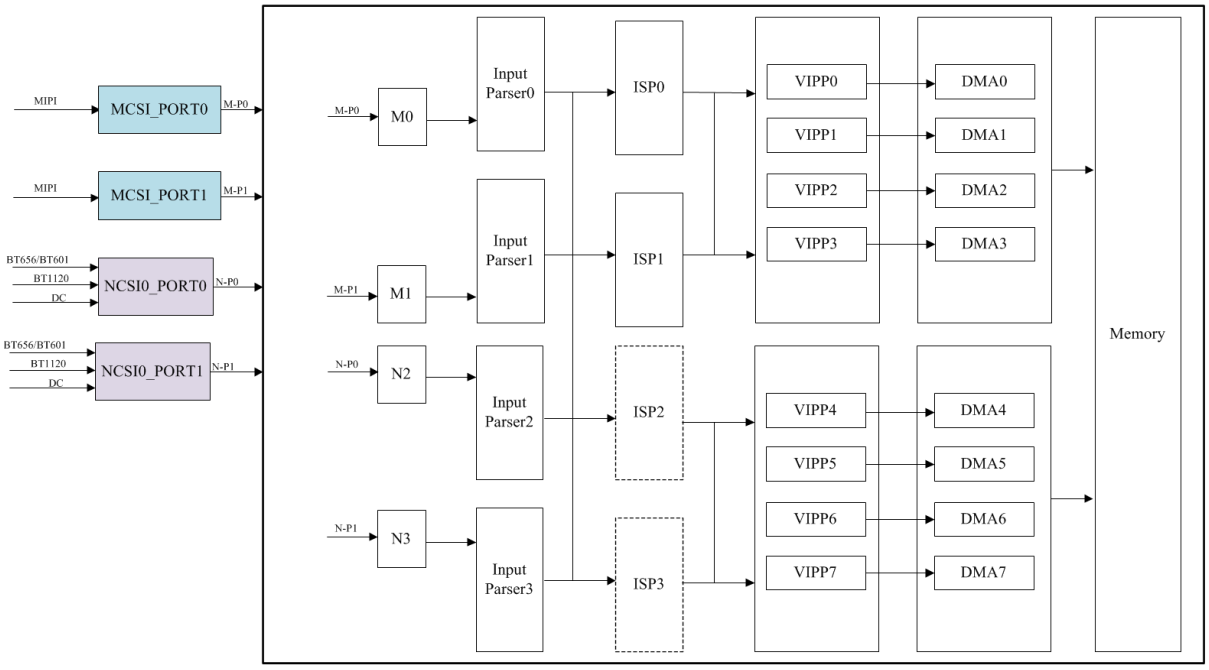

Figure 8- 1. CSIC Block Diagram

The CSIC consists of 4 Input Parser, 2 image signal processor(ISP), 8 Video Input Post Process(VIPP) and 8 DMA Control.

NOTE

ISP2 and ISP3 are empty.

Figure 8-2 shows the block diagram of CCI.

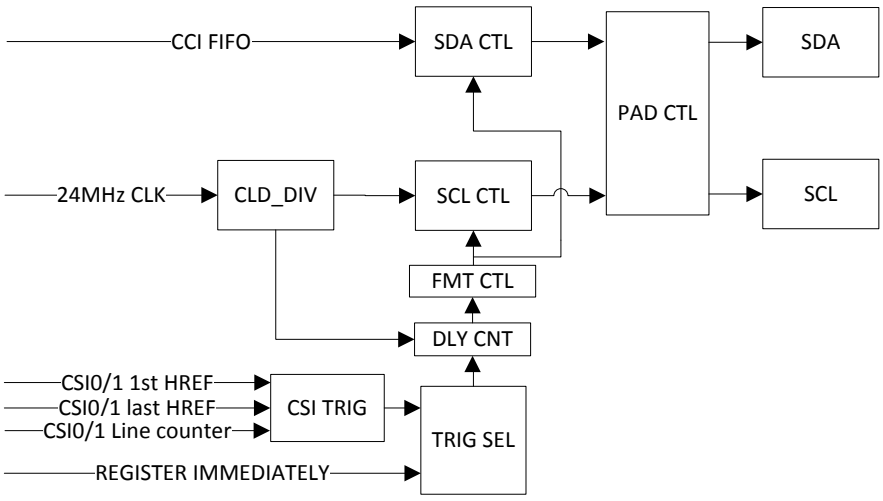

Figure 8- 2. CCI Block Diagram

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8.1.3. Operations and Functional Descriptions

8.1.3.1. External Signals

Table 8- 1. CSIC External Signals

Pin Name	Function Description	Type
NCSI0_MCLK	Parallel CSI0 Master Clock for External Device	O
NCSI0_PCLK	Parallel CSI0 Pixel Clock	I
NCSI0_VSYNC	Parallel CSI0 Vertical SYNC Signal	I
NCSI0_HSYNC	Parallel CSI0 Horizontal SYNC Signal	I
NCSI0_D0	Parallel CSI0 Video Input Data0	I
NCSI0_D1	Parallel CSI0 Video Input Data1	I
NCSI0_D2	Parallel CSI0 Video Input Data2	I
NCSI0_D3	Parallel CSI0 Video Input Data3	I
NCSI0_D4	Parallel CSI0 Video Input Data4	I
NCSI0_D5	Parallel CSI0 Video Input Data5	I
NCSI0_D6	Parallel CSI0 Video Input Data6	I
NCSI0_D7	Parallel CSI0 Video Input Data7	I
NCSI0_D8	Parallel CSI0 Video Input Data8	I
NCSI0_D9	Parallel CSI0 Video Input Data9	I
NCSI0_D10	Parallel CSI0 Video Input Data10	I
NCSI0_D11	Parallel CSI0 Video Input Data11	I
NCSI0_D12	Parallel CSI0 Video Input Data12	I
NCSI0_D13	Parallel CSI0 Video Input Data13	I
NCSI0_D14	Parallel CSI0 Video Input Data14	I
NCSI0_D15	Parallel CSI0 Video Input Data15	I
NCSI0_SCK	Parallel CSI0 CCI Control Clock	O,OD
NCSI0_SDA	Parallel CSI0 CCI Control Data	I/O,OD
CSI_FSIN0	Parallel CSI0 Vertical SYNC Signal to Sensor in Slave Mode	O
NCSI1_MCLK	Parallel CSI1 Master Clock for External Device	O
NCSI1_PCLK	Parallel CSI1 Pixel Clock	I
NCSI1_VSYNC	Parallel CSI1 Vertical SYNC Signal	I
NCSI1_HSYNC	Parallel CSI1 Horizontal SYNC Signal	I
NCSI1_D0	Parallel CSI1 Video Input Data0	I
NCSI1_D1	Parallel CSI1 Video Input Data1	I
NCSI1_D2	Parallel CSI1 Video Input Data2	I
NCSI1_D3	Parallel CSI1 Video Input Data3	I
NCSI1_D4	Parallel CSI1 Video Input Data4	I
NCSI1_D5	Parallel CSI1 Video Input Data5	I
NCSI1_D6	Parallel CSI1 Video Input Data6	I
NCSI1_D7	Parallel CSI1 Video Input Data7	I
NCSI1_D8	Parallel CSI1 Video Input Data8	I
NCSI1_D9	Parallel CSI1 Video Input Data9	I

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NCSI1_D10	Parallel CSI1 Video Input Data10	I
NCSI1_D11	Parallel CSI1 Video Input Data11	I
NCSI1_D12	Parallel CSI1 Video Input Data12	I
NCSI1_D13	Parallel CSI1 Video Input Data13	I
NCSI1_D14	Parallel CSI1 Video Input Data14	I
NCSI1_D15	Parallel CSI1 Video Input Data15	I
NCSI1_SCK	Parallel CSI1 CCI Control Clock	O,OD
NCSI1_SDA	Parallel CSI1 CCI Control Data	I/O,OD
CSI_FSIN1	Parallel CSI1 Vertical SYNC Signal to Sensor in Slave Mode	O
MCSIA_CKP	MIPI CSI ControllerA Clock Differential P	AI
MCSIA_CKN	MIPI CSI ControllerA Clock Differential N	AI
MCSIA_D0P	MIPI CSI ControllerA Data0 Differential P	AI
MCSIA_D0N	MIPI CSI ControllerA Data0 Differential N	AI
MCSIA_D1P	MIPI CSI ControllerA Data1 Differential P	AI
MCSIA_D1N	MIPI CSI ControllerA Data1 Differential N	AI
MCSIA_D2P	MIPI CSI ControllerA Data2 Differential P	AI
MCSIA_D2N	MIPI CSI ControllerA Data2 Differential N	AI
MCSIA_D3P	MIPI CSI ControllerA Data3 Differential P	AI
MCSIA_D3N	MIPI CSI ControllerA Data3 Differential N	AI
MCSIA_MCLK	MIPI CSI ControllerA Master Clock	O
MCSIA_SCK	MIPI CSI ControllerA CCI Control Clock	O,OD
MCSIA_SDA	MIPI CSI ControllerA CCI Control Data	I/O,OD
VCC_MCSIA	MIPI CSI ControllerA Power Supply	P
MCSIB_CKP	MIPI CSI ControllerB Clock Differential P	AI
MCSIB_CKN	MIPI CSI ControllerB Clock Differential N	AI
MCSIB_D0P	MIPI CSI ControllerB Data0 Differential P	AI
MCSIB_D0N	MIPI CSI ControllerB Data0 Differential N	AI
MCSIB_D1P	MIPI CSI ControllerB Data1 Differential P	AI
MCSIB_D1N	MIPI CSI ControllerB Data1 Differential N	AI
MCSIB_D2P	MIPI CSI ControllerB Data2 Differential P	AI
MCSIB_D2N	MIPI CSI ControllerB Data2 Differential N	AI
MCSIB_D3P	MIPI CSI ControllerB Data3 Differential P	AI
MCSIB_D3N	MIPI CSI ControllerB Data3 Differential N	AI
MCSIB_MCLK	MIPI CSI ControllerB Master Clock	O
MCSIB_SCK	MIPI CSI ControllerB CCI Control Clock	O,OD
MCSIB_SDA	MIPI CSI ControllerB CCI Control Data	I/O,OD
VCC_MCSIB	MIPI CSI ControllerB Power Supply	P

8.1.3.2. Clock Configuration Instruction

MCLK: MCLK is provided baseline clock source for camera module, the frequency is set by camera module datasheet. For details about frequency configuration register, see to **CSI_MST_CLK_REG** in CCU. The usual clock frequency is 24MHz,27MHz and 37.25MHz.

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TOP_CLK: TOP_CLK is the clock source of CSIC controller, the frequency need be greater than PCLK of actual application scene, so that CSIC can normally capture the data of camera module. For details about frequency configuration register, see to **CSI_TOP_CLK_REG** in CCU.

NOTE

The higher TOP_CLK frequency, the greater CSIC power consumption is.

8.1.3.3. Typical Application

The CSIC module has 4 input ports and 8 DMA, which means it can support 4 ports input and 8 video streams output to memory simultaneously at most. This make the applications very flexible.

The CSIC module supports following input cases:

- 2 high speed serial inputs
- 2 parallel DC inputs
- 1 serial input + 1 parallel DC input
- 1 BT656/BT1120 input interleaved 4-channel
- 1 BT656 input interleaved 2-channel + 1 BT656 input interleaved 2-channel
- 1 BT1120 input interleaved 2-channel + 1 BT1120 input interleaved 2-channel

8.1.3.4. CSIC FIFO Distribution

Table 8- 2. CSIC FIFO Distribution

Interface	**YUYV422 Interleaved/Raw**			**MIPI Interface**		
Input format	YUV422		Raw	YUV422		Raw
Output format	Planar	UV combined	Raw/RGB /PRGB	Planar	UV combined	Raw/RGB /PRGB
CH0_FIFO0	Y	Y	All pixels data	Y	Y	All pixels data
CH0_FIFO1	Cb (U)	CbCr (UV)	-	Cb (U)	CbCr (UV)	-
CH0_FIFO2	Cr (V)	-	-	Cr (V)	-	-

Interface	**BT656 Interface**		**BT1120 Interface**	
Input format	YUV422		YUV422	
Output format	Planar	UV combined	Planar	UV combined
CH0_FIFO0	Y	Y	Y	Y
CH0_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH0_FIFO2	Cr (V)	-	Cr (V)	-
CH1_FIFO0	Y	Y	Y	Y
CH1_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH1_FIFO2	Cr (V)	-	Cr (V)	-
CH2_FIFO0	Y	Y	Y	Y

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CH2_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH2_FIFO2	Cr (V)	-	Cr (V)	-
CH3_FIFO0	Y	Y	Y	Y
CH3_FIFO1	Cb (U)	CbCr (UV)	Cb (U)	CbCr (UV)
CH3_FIFO2	Cr (V)	-	Cr (V)	-

8.1.3.5. Pixel Format Arrangement

RAW-10:

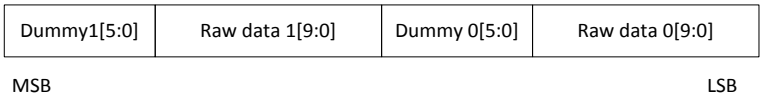

Figure 8- 3. RAW-10 Format

RAW-12:

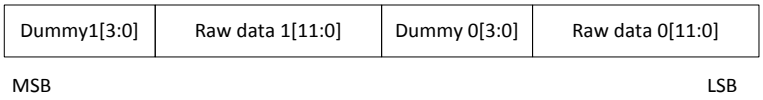

Figure 8- 4. RAW-12 Format

YUV-10:

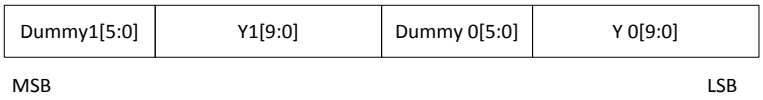

Figure 8- 5. Y of YUV-10 Format

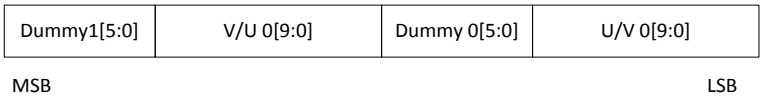

Figure 8- 6. UV Combined of YUV-10 Format

RGB888:

B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

MSB

Figure 8- 7. RGB888 Format

PRGB888:

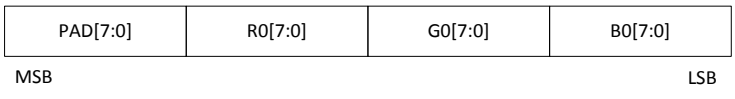

Figure 8- 8. PRGB888 Format

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RGB565:

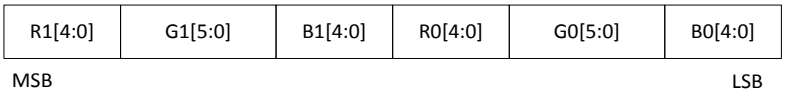

Figure 8- 9. RGB565 Format

8.1.3.6. CSIC Timing

Figure 8-10 shows the timing of 8-bit CMOS Sensor Interface.

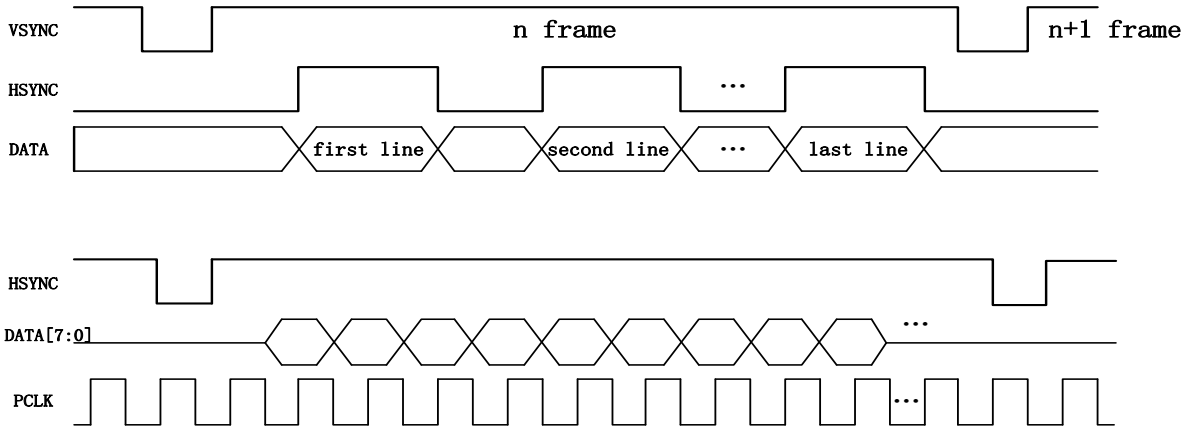

Figure 8- 10. 8-bit CMOS Sensor Interface Timing

(clock rising edge sample.vsync valid = positive,hsycn valid = positive)

Figure 8-11 shows the timing of 8-bit YCbCr4:2:2 BT656.

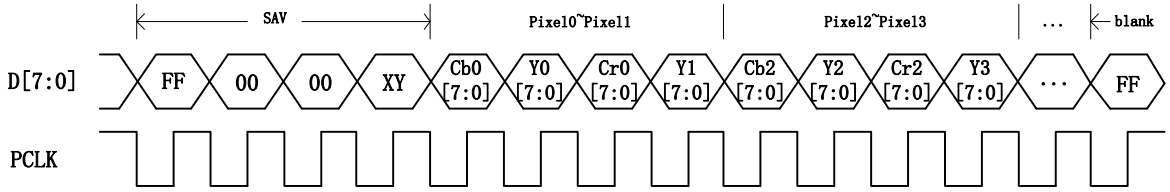

Figure 8- 11. 8-bit YCbCr4:2:2 BT656 Timing

Figure 8-12 shows the timing of multiplexed format (BT656).

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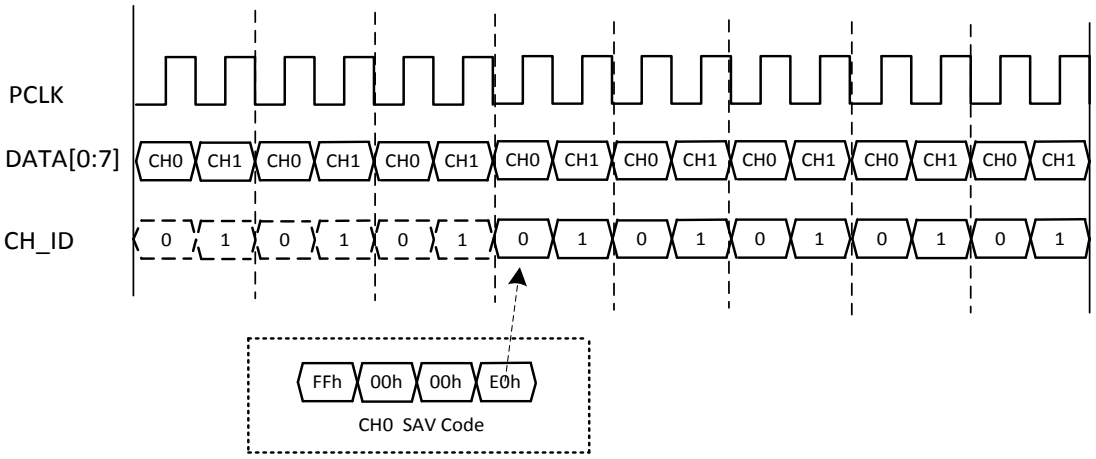

Figure 8- 12. Multiplexed Format(BT656) Timing

Figure 8-13 shows the data sample timing of CSIC.

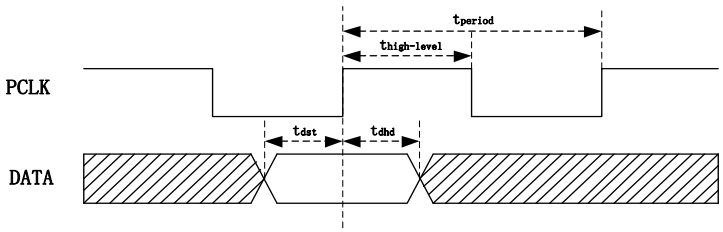

Figure 8- 13. CSIC Data Sample Timing

8.1.3.7. CCIR656 Header Code

Table 8- 3. CCIR656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	x	x	x	x
CS D[8]	x	x	x	x
CS D[7]	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

NOTE

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For compatibility with 8-bit interface, CS D[9] and CS D[8] are not defined.

Table 8- 4. CCIR656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

8.1.3.8. Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.
For YUV422 format, pixel unit is a YU/YV combination.
For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
For Bayer and RAW format, pixel unit is a R/G/B single component.
For RGB565, pixel unit is 2 bytes of RGB565 package.
For RGB888, pixel unit is 3 bytes of RGB combination.

8.1.3.9. Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:
For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be like.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.
For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

8.1.3.10. Camera Communication Interface

The CCI module supports master mode I2C-compatible interface which can access to camera and related devices.
It reads a series of packet from FIFO (accessed by registers) and transmit with the format defined in specific register(or packet data).

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In compact mode, format register define the slave ID, R/W flag, register address width(0/8/16/32…bit), data width(8/16/32…bit) and access counter.

In complete mode, all data and format will be loaded from memory packet.

The access counter should be set to N(N> 0), and it will read N packets from FIFO. The total bytes should not exceed 64 for FIFO input mode.

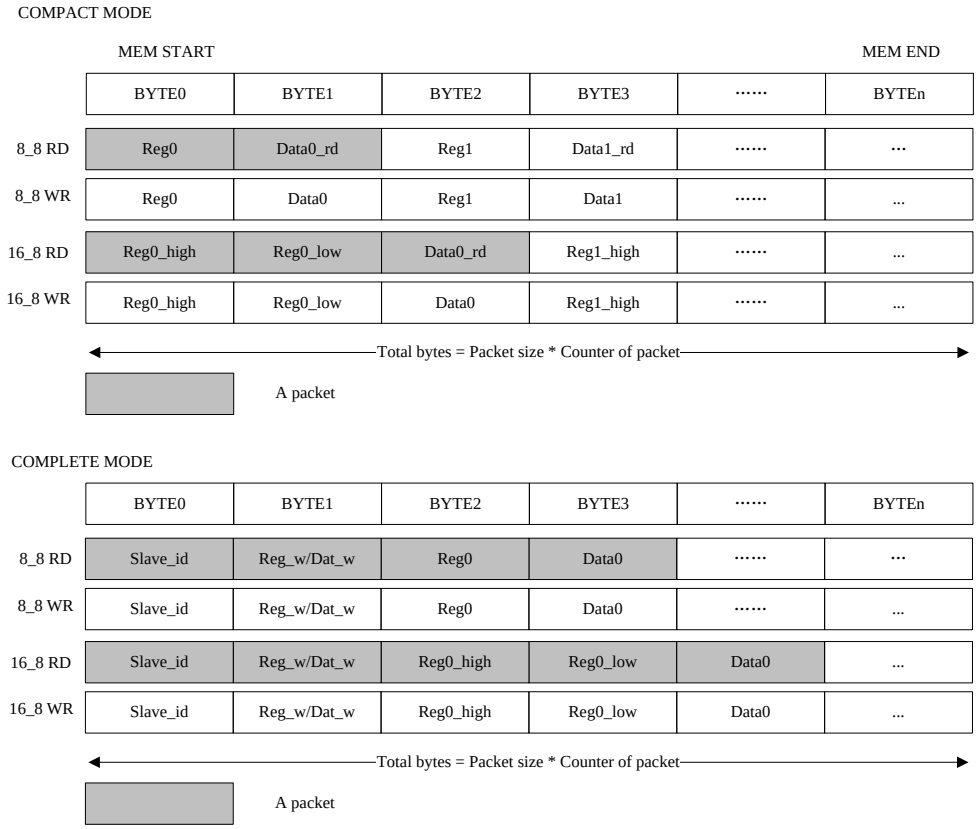

Figure 8- 14. R/W Sequence in Compact/Complete Mode

A packet has several bytes that filled with register address and data(if in complete mode, slave id and data width should be filled too). That is, the low address byte will be transmitted/received first. Bytes will be sent in write access, while some address will be written back with the data received in read access.

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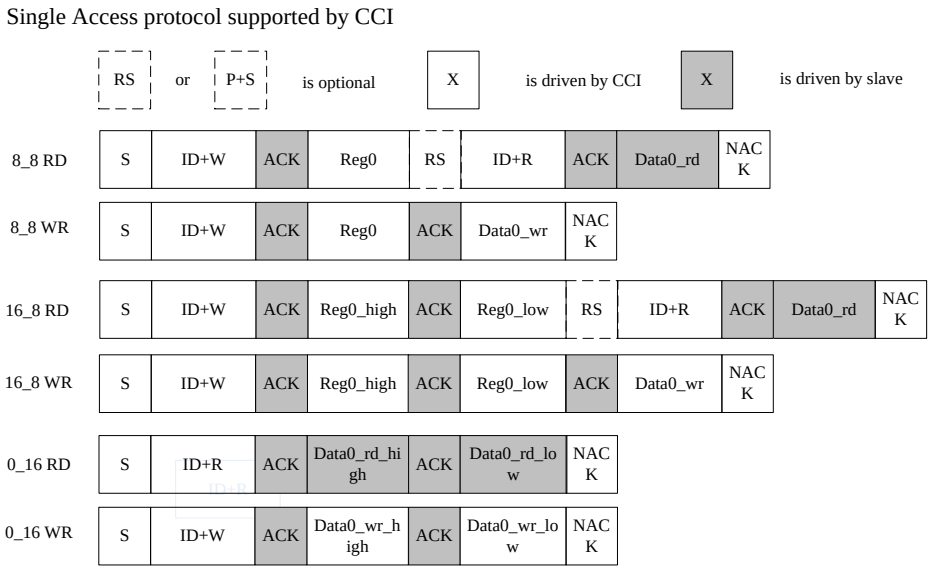

Figure 8- 15. Single R/W Process of the CCI Protocol

After set the execution bit, the module will do the transmission automatically and return the result of success or fail. If any access fails, the whole transmission will be stopped and returns the number when it fails in the access counter.

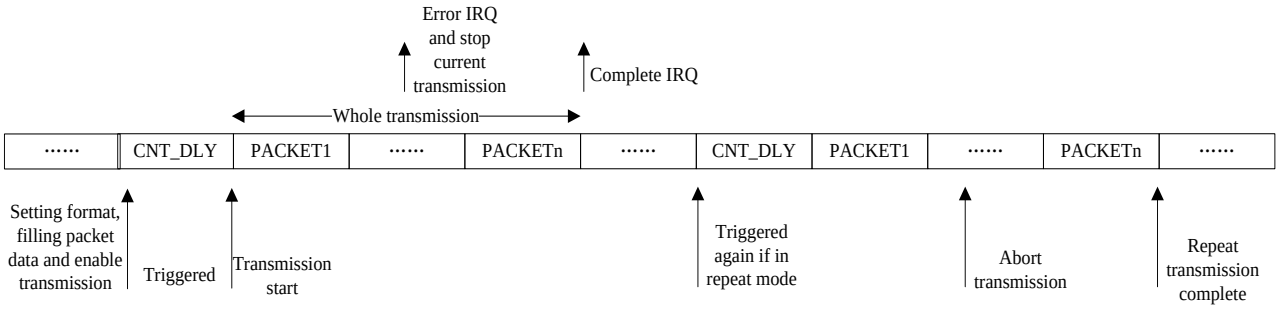

Figure 8- 16. CCI Transmission Control

8.1.4. Register list

Module Name	Base Address
CSIC_BASE	0x06600000
CSIC_TOP	0x06600000
CSIC_PARSER0	0x06601000
CSIC_PARSER1	0x06602000
CSIC_PARSER2	0x06603000
CSIC_PARSER3	0x06604000
CSIC_DMA0	0x06609000
CSIC_DMA1	0x06609200
CSIC_DMA2	0x06609400
CSIC_DMA3	0x06609600
CSIC_DMA4	0x06609800
CSIC_DMA5	0x06609A00
CSIC_DMA6	0x06609C00
CSIC_DMA7	0x06609E00

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CSIC_CCI0	0x06614000
CSIC_CCI1	0x06614400
CSIC_CCI2	0x06614800
CSIC_CCI3	0x06614C00

CSIC TOP register list:

Register Name	Offset	Register name
CSIC_TOP_EN_REG	0x0000	CSI TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSI Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSI Pattern Control Register
/	0x000C~0x001C	Reserved
CSIC_PTN_LEN_REG	0x0020	CSI Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSI Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSI Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_ISP2_INPUT0_SEL_REG	0x0050	CSIC ISP2 Input0 Select Register
CSIC_ISP2_INPUT1_SEL_REG	0x0054	CSIC ISP2 Input1 Select Register
CSIC_ISP2_INPUT2_SEL_REG	0x0058	CSIC ISP2 Input2 Select Register
CSIC_ISP2_INPUT3_SEL_REG	0x005C	CSIC ISP2 Input3 Select Register
CSIC_ISP3_INPUT0_SEL_REG	0x0060	CSIC ISP3 Input0 Select Register
CSIC_ISP3_INPUT1_SEL_REG	0x0064	CSIC ISP3 Input1 Select Register
CSIC_ISP3_INPUT2_SEL_REG	0x0068	CSIC ISP3 Input2 Select Register
CSIC_ISP3_INPUT3_SEL_REG	0x006C	CSIC ISP3 Input3 Select Register
/	0x0070~0x009C	Reserved
CSIC_VIPP0_INPUT_SEL_REG	0x00A0	CSIC VIPP0 Input Select Register
CSIC_VIPP1_INPUT_SEL_REG	0x00A4	CSIC VIPP1 Input Select Register
CSIC_VIPP2_INPUT_SEL_REG	0x00A8	CSIC VIPP2 Input Select Register
CSIC_VIPP3_INPUT_SEL_REG	0x00AC	CSIC VIPP3 Input Select Register
CSIC_VIPP4_INPUT_SEL_REG	0x00B0	CSIC VIPP4 Input Select Register
CSIC_VIPP5_INPUT_SEL_REG	0x00B4	CSIC VIPP5 Input Select Register
CSIC_VIPP6_INPUT_SEL_REG	0x00B8	CSIC VIPP6 Input Select Register
CSIC_VIPP7_INPUT_SEL_REG	0x00BC	CSIC VIPP7 Input Select Register
CSIC_BIST_CONTROL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_REG	0x00E4	CSIC BIST Start Register
CSIC_BIST_END_REG	0x00E8	CSIC BIST End Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register

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PARSER 0/1/2/3 register list:

Register Name	Offset	Register name
PRS_EN_REG	0x0000	Parser Enable Register
PRS_NCSI_IF_CFG_REG	0x0004	Parser NCSI Interface Configuration Register
PRS_MCSI_IF_CFG_REG	0x0008	Parser MCSI Interface Configuration Register
PRS_CAP_REG	0x000C	Parser Capture Register
PRS_SIGNAL_STA_REG	0x0010	Parser Signal Status Register
PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	Parser NCSIC BT656 Header Configuration Register
/	0x0018~0x0020	Reserved
PRS_C0_INFMT_REG	0x0024	Parser Channel_0 Input Format Register
PRS_C0_OUTPUT_HSIZE_REG	0x0028	Parser Channel_0 Output Horizontal Size Register
PRS_C0_OUTPUT_VSIZE_REG	0x002C	Parser Channel_0 Output Vertical Size Register
PRS_C0_INPUT_PARA0_REG	0x0030	Parser Channel_0 Input Parameter0 Register
PRS_C0_INPUT_PARA1_REG	0x0034	Parser Channel_0 Input Parameter1 Register
PRS_C0_INPUT_PARA2_REG	0x0038	Parser Channel_0 Input Parameter2 Register
PRS_C0_INPUT_PARA3_REG	0x003C	Parser Channel_0 Input Parameter3 Register
PRS_C0_INT_EN_REG	0x0040	Parser Channel_0 Interrupt Enable Register
PRS_C0_INT_STA_REG	0x0044	Parser Channel_0 Interrupt Status Register
/	0x0048~0x0120	Reserved
PRS_C1_INFMT_REG	0x0124	Parser Channel_1 Input Format Register
PRS_C1_OUTPUT_HSIZE_REG	0x0128	Parser Channel_1 Output Horizontal Size Register
PRS_C1_OUTPUT_VSIZE_REG	0x012C	Parser Channel_1 Output Vertical Size Register
PRS_C1_INPUT_PARA0_REG	0x0130	Parser Channel_1 Input Parameter0 Register
PRS_C1_INPUT_PARA1_REG	0x0134	Parser Channel_1 Input Parameter1 Register
PRS_C1_INPUT_PARA2_REG	0x0138	Parser Channel_1 Input Parameter2 Register
PRS_C1_INPUT_PARA3_REG	0x013C	Parser Channel_1 Input Parameter3 Register
PRS_C1_INT_EN_REG	0x0140	Parser Channel_1 Interrupt Enable Register
PRS_C1_INT_STA_REG	0x0144	Parser Channel_1 Interrupt Status Register
/	0x0148~0x0220	Reserved
PRS_C2_INFMT_REG	0x0224	Parser Channel_2 Input Format Register
PRS_C2_OUTPUT_HSIZE_REG	0x0228	Parser Channel_2 Output Horizontal Size Register
PRS_C2_OUTPUT_VSIZE_REG	0x022C	Parser Channel_2 Output Vertical Size Register
PRS_C2_INPUT_PARA0_REG	0x0230	Parser Channel_2 Input Parameter0 Register
PRS_C2_INPUT_PARA1_REG	0x0234	Parser Channel_2 Input Parameter1 Register
PRS_C2_INPUT_PARA2_REG	0x0238	Parser Channel_2 Input Parameter2 Register
PRS_C2_INPUT_PARA3_REG	0x023C	Parser Channel_2 Input Parameter3 Register
PRS_C2_INT_EN_REG	0x0240	Parser Channel_2 Interrupt Enable Register
PRS_C2_INT_STA_REG	0x0244	Parser Channel_2 Interrupt Status Register
/	0x0248~0x0320	Reserved
PRS_C3_INFMT_REG	0x0324	Parser Channel_3 Input Format Register
PRS_C3_OUTPUT_HSIZE_REG	0x0328	Parser Channel_3 Output Horizontal Size Register
PRS_C3_OUTPUT_VSIZE_REG	0x032C	Parser Channel_3 Output Vertical Size Register

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PRS_C3_INPUT_PARA0_REG	0x0330	Parser Channel_3 Input Parameter0 Register
PRS_C3_INPUT_PARA1_REG	0x0334	Parser Channel_3 Input Parameter1 Register
PRS_C3_INPUT_PARA2_REG	0x0338	Parser Channel_3 Input Parameter2 Register
PRS_C3_INPUT_PARA3_REG	0x033C	Parser Channel_3 Input Parameter3 Register
PRS_C3_INT_EN_REG	0x0340	Parser Channel_3 Interrupt Enable Register
PRS_C3_INT_STA_REG	0x0344	Parser Channel_3 Interrupt Status Register
/	0x0348~0x04FC	Reserved
PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	Parser NCSIC RX Signal0 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL1_DLY_ADJ_REG	0x0504	Parser NCSIC RX Signal1 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL2_DLY_ADJ_REG	0x0508	Parser NCSIC RX Signal2 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG	0x050C	Parser NCSIC RX Signal3 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG	0x0510	Parser NCSIC RX Signal4 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	Parser NCSIC RX Signal5 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	Parser NCSIC RX Signal6 Delay Adjust Register
PRS_NCSIC_SYNC_EN_REG	0x0520	Parser NCSIC SYNC Enable Register
PRS_NCSIC_SYNC_CFG_REG	0x0524	Parser NCSIC SYNC CFG Register
PRS_NCSIC_SYNC_WAIT_N_REG	0x0528	Parser NCSIC SYNC WAIT N Register
PRS_NCSIC_SYNC_WAIT_M_REG	0x052C	Parser NCSIC SYNC WAIT M Register

DMA0/1/2/3/4/5/6/7 register list:

CSIC_DMA_EN_REG	0x0000	CSIC DMA Enable Register
CSIC_DMA_CFG_REG	0x0004	CSIC DMA Configuration Register
/	0x0008	Reserved
/	0x000C	Reserved
CSIC_DMA_HSIZE_REG	0x0010	CSIC DMA Horizontal Size Register
CSIC_DMA_VSIZE_REG	0x0014	CSIC DMA Vertical Size Register
/	0x0018	Reserved
/	0x001C	Reserved
CSIC_DMA_F0_BUFA_REG	0x0020	CSIC DMA FIFO 0 Output Buffer-A Address Register
/	0x0024	Reserved
CSIC_DMA_F1_BUFA_REG	0x0028	CSIC DMA FIFO 1 Output Buffer-A Address Register
/	0x002C	Reserved
CSIC_DMA_F2_BUFA_REG	0x0030	CSIC DMA FIFO 2 Output Buffer-A Address Register
/	0x0034	Reserved
CSIC_DMA_BUF_LEN_REG	0x0038	CSIC DMA Buffer Length Register
CSIC_DMA_FLIP_SIZE_REG	0x003C	CSIC DMA Flip Size Register
/	0x0040~0x0048	Reserved
CSIC_DMA_CAP_STA_REG	0x004C	CSIC DMA Capture Status Register
CSIC_DMA_INT_EN_REG	0x0050	CSIC DMA Interrupt Enable Register
CSIC_DMA_INT_STA_REG	0x0054	CSIC DMA Interrupt Status Register
CSIC_DMA_LINE_CNT_REG	0x0058	CSIC DMA Line Counter Register
CSIC_DMA_FRM_CNT_REG	0x005C	CSIC DMA Frame Counter Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0060	CSIC DMA Frame Clock Counter Register

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CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0064	CSIC DMA Accumulated And Internal Clock Counter Register
CSIC_DMA_FIFO_STAT_REG	0x0068	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x006C	CSIC DMA FIFO Threshold Register
CSIC_DMA_PCLK_STAT_REG	0x0070	CSIC DMA PCLK Statistic Register
CSIC_FEATURE_REG	0x01F0	CSIC DMA Feature List Register

CCI0/1/2/3 register list:

CCI_CTRL	0x0000	CCI Control Register
CCI_CFG	0x0004	CCI Transmission Configuration Register
CCI_FMT	0x0008	CCI Packet Format Register
CCI_BUS_CTRL	0x000C	CCI Bus Control Register
/	0x0010	Reserved
CCI_INT_CTRL	0x0014	CCI Interrupt Control Register
CCI_LC_TRIG	0x0018	CCI Line Counter Trigger Register
/	0x001C~0x00FC	Reserved
CCI_FIFO_ACC	0x0100~0x013C	CCI FIFO Access Register
/	0x0140~0x01FC	Reserved
CCI_RSV_REG	0x0200~0x0220	CCI Reserved Register

8.1.5. CSIC TOP Register Description

8.1.5.1. CSIC Top Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: CSIC_TOP_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	SRAM_PWDN 0: SRAM in normal 1: SRAM in power down
7:2	/	/	/
1	R/W	0x0	WDR_MODE_EN 0: Normal mode 1: WDR mode
0	R/W	0x0	CSIC_TOP_EN 0: Reset and disable the CSIC module 1: Enable the CSIC module

8.1.5.2. CSIC Pattern Generation Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004	**Register Name: CSIC_PTN_GEN_EN_REG**

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Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	PTN_CYCLE Pattern generating cycle counter. The pattern in dram will be generated in cycles of PTN_CYCLE+1.
15:5	/	/	/
4	R/WAC	0x0	PTN_START CSI pattern generating start 0: Finish 1: Start Software writes this bit to“1” to start pattern generating from DRAM. When finished, the hardware will clear this bit to“0” automatically. Generating cycles depends on PTN_CYCLE.
3:1	/	/	/
0	R/W	0x0	PTN_GEN_EN Pattern generation enable

8.1.5.3. CSIC Pattern Control Register(Default Value: 0x0000_000F)

Offset: 0x0008			Register Name: CSIC_PTN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	PTN_PORT_SEL Pattern generator output port selection 000:MCSIC0 001:MCSIC1 010:NCSIC0 011:NCSIC1 100:NCSIC2 101:NCSIC3
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH 00:8-bit 01:10-bit 10:12-bit 11:reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000~0011:reserved 0100:NCSIC YUV 8 bits width 0101:NCSIC YUV 16 bits width 0110:reserved 0111:reserved 1000:BT656 8 bits width

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			1001:BT656 16 bits width 1010:reserved 1011:reserved 1100:BAYER 12 bits for ISPFE 1101:UYVY422 12 bits for ISPFE 1110:UYVY420 12 bits for ISPFE 1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start

8.1.5.4. CSIC Pattern Generation Length Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

8.1.5.5. CSIC Pattern Generation Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

8.1.5.6. CSIC Pattern ISP Size Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size,only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size,only valid for ISP mode pattern generation.

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8.1.5.7. CSIC ISP0 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input0 Select 000: Input from Parser0 CH0 001: Input from Parser1 CH0 010: Input from Parser2 CH0 011: Input from Parser3 CH0 100: Input from Parser0 CH1 101: Input from Parser1 CH1 110: Input from Parser2 CH1 111: Input from Parser3 CH1 others: reserved

8.1.5.8. CSIC ISP0 Input1 Select Register(Default Value:0x0000_0000)

Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input1 Select 000: Input from Parser0 CH1 001: Input from Parser1 CH1 010: Input from Parser2 CH1 011: Input from Parser3 CH1 others: reserved

8.1.5.9. CSIC ISP0 Input2 Select Register(Default Value:0x0000_0000)

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input2 Select 000: Input from Parser0 CH2 001: Input from Parser1 CH2 010: Input from Parser2 CH2 011: Input from Parser3 CH2 others: reserved

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8.1.5.10. CSIC ISP0 Input3 Select Register(Default Value:0x0000_0000)

Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP0 Input3 Select 000: Input from Parser0 CH3 001: Input from Parser1 CH3 010: Input from Parser2 CH3 011: Input from Parser3 CH3 others: reserved

8.1.5.11. CSIC ISP1 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP1 Input0 Select 000: Input from Parser0 CH0 001: Input from Parser1 CH0 010: Input from Parser2 CH0 011: Input from Parser3 CH0 100: Input from Parser0 CH1 101: Input from Parser1 CH1 110: Input from Parser2 CH1 111: Input from Parser3 CH1

8.1.5.12. CSIC ISP1 Input1 Select Register(Default Value:0x0000_0000)

Offset :0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP1 Input1 Select 000: Input from Parser0 CH1 001: Input from Parser1 CH1 010: Input from Parser2 CH1 011: Input from Parser3 CH1 others: reserved

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8.1.5.13. CSIC ISP1 Input2 Select Register(Default Value:0x0000_0000)

Offset :0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP1 Input2 Select 000: Input from Parser0 CH2 001: Input from Parser1 CH2 010: Input from Parser2 CH2 011: Input from Parser3 CH2 others: reserved

8.1.5.14. CSIC ISP1 Input3 Select Register(Default Value:0x0000_0000)

Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP1 Input3 Select 000: Input from Parser0 CH3 001: Input from Parser1 CH3 010: Input from Parser2 CH3 011: Input from Parser3 CH3 others: reserved

8.1.5.15. CSIC ISP2 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP2 Input0 Select 000: Input from Parser0 CH0 001: Input from Parser1 CH0 010: Input from Parser2 CH0 011: Input from Parser3 CH0 100: Input from Parser0 CH1 101: Input from Parser1 CH1 110: Input from Parser2 CH1 111: Input from Parser3 CH1

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8.1.5.16. CSIC ISP2 Input1 Select Register(Default Value:0x0000_0000)

Offset :0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	ISP2 Input1 Select 000: Input from Parser0 CH1 001: Input from Parser1 CH1 010: Input from Parser2 CH1 011: Input from Parser3 CH1 others: reserved

8.1.5.17. CSIC ISP2 Input2 Select Register(Default Value:0x0000_0000)

Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	ISP2 Input2 Select 000: Input from Parser0 CH2 001: Input from Parser1 CH2 010: Input from Parser2 CH2 011: Input from Parser3 CH2 others: reserved

8.1.5.18. CSIC ISP2 Input3 Select Register(Default Value:0x0000_0000)

Offset :0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	ISP2 Input3 Select 000: Input from Parser0 CH3 001: Input from Parser1 CH3 010: Input from Parser2 CH3 011: Input from Parser3 CH3 others: reserved

8.1.5.19. CSIC ISP3 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/

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2:0	R/W	0x0	ISP3 Input0 Select 000: Input from Parser0 CH0 001: Input from Parser1 CH0 010: Input from Parser2 CH0 011: Input from Parser3 CH0 100: Input from Parser0 CH1 101: Input from Parser1 CH1 110: Input from Parser2 CH1 111: Input from Parser3 CH1

8.1.5.20. CSIC ISP3 Input1 Select Register(Default Value:0x0000_0000)

Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP3 Input1 Select 000: Input from Parser0 CH1 001: Input from Parser1 CH1 010: Input from Parser2 CH1 011: Input from Parser3 CH1 others: reserved

8.1.5.21. CSIC ISP3 Input2 Select Register(Default Value:0x0000_0000)

Offset :0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP3 Input2 Select 000: Input from Parser0 CH2 001: Input from Parser1 CH2 010: Input from Parser2 CH2 011: Input from Parser3 CH2 others: reserved

8.1.5.22. CSIC ISP3 Input3 Select Register(Default Value:0x0000_0000)

Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	ISP3 Input3 Select 000: Input from Parser0 CH3

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			001: Input from Parser1 CH3 010: Input from Parser2 CH3 011: Input from Parser3 CH3 others: reserved

8.1.5.23. CSIC VIPP0 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A0			Register Name: CSIC_VIPP0_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP0 Input Select 000: Input from ISP0 CH0 001: Input from ISP1 CH0 others: reserved

8.1.5.24. CSIC VIPP1 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A4			Register Name: CSIC_VIPP1_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP1 Input Select 000: Input from ISP0 CH0 001: Input from ISP1 CH0 010: Input from ISP0 CH1 011: Input from ISP1 CH1 others: reserved

8.1.5.25. CSIC VIPP2 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A8			Register Name: CSIC_VIPP2_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP2 Input Select 000: Input from ISP0 CH0 001: Input from ISP1 CH0 010: Input from ISP0 CH2 011: Input from ISP1 CH2 others: reserved

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8.1.5.26. CSIC VIPP3 Input Select Register(Default Value:0x0000_0000)

Offset :0x00AC			Register Name: CSIC_VIPP3_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP3 Input Select 000: Input from ISP0 CH0 001: Input from ISP1 CH0 010: Input from ISP0 CH3 011: Input from ISP1 CH3 100: Input from ISP1 CH1 others: reserved

8.1.5.27. CSIC VIPP4 Input Select Register(Default Value:0x0000_0000)

Offset :0x00B0			Register Name: CSIC_VIPP4_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP4 Input Select 000: Input from ISP2 CH0 001: Input from ISP3 CH0 others: reserved

8.1.5.28. CSIC VIPP5 Input Select Register(Default Value:0x0000_0000)

Offset :0x00B4			Register Name: CSIC_VIPP5_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP5 Input Select 000: Input from ISP2 CH0 001: Input from ISP3 CH0 010: Input from ISP2 CH1 011: Input from ISP3 CH1 others: reserved

8.1.5.29. CSIC VIPP6 Input Select Register(Default Value:0x0000_0000)

Offset :0x00B8			Register Name: CSIC_VIPP6_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP6 Input Select

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			000: Input from ISP2 CH0 001: Input from ISP3 CH0 010: Input from ISP2 CH2 011: Input from ISP3 CH2 others: reserved

8.1.5.30. CSIC VIPP7 Input Select Register(Default Value:0x0000_0000)

Offset :0x00BC			Register Name: CSIC_VIPP7_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	VIPP7 Input Select 000: Input from ISP2 CH0 001: Input from ISP3 CH0 010: Input from ISP2 CH3 011: Input from ISP3 CH3 100: Input from ISP3 CH1 others: reserved

8.1.5.31. CSIC BIST Control Register(Default Value:0x0000_0000)

Offset :0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST error status 0:No effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST error pattern
11:10	R	0x0	BIST_ERR_CYC BIST error cycle
9	R	0x1	BIST_STOP BISTstop 0:Running 1:STOP
8	R	0x0	BIST_BUSY BIST busy 0:Idle 1:Busy
7:5	R/W	0x0	BIST_REG_SEL BIST register select

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4	R/W	0x0	BIST_ADDR_Mode_SEL BIST address mode select
3:1	R/W	0x0	BIST_WDATA_PAT BIST write data pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST enable A positive will trigger the BIST to start.

8.1.5.32. CSIC BIST Start Address Register(Default Value:0x0000_0000)

Offset :0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST Start Address It is 32-bit aligned.

8.1.5.33. CSIC BIST End Address Register(Default Value:0x0000_0000)

Offset :0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST END Address It is 32-bit aligned.

8.1.5.34. CSIC BIST Data Mask Register(Default Value:0x0000_0000)

Offset :0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0:Unmask 1:Mask

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8.1.6. CSIC Parser Register Description

8.1.6.1. Parser Enable Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/
16	R/W	0x0	NCSI_EN 0: Reset and disable the NCSI module 1: Enable the NCSI module
15	R/W	0x0	PCLK_EN 0:Gate pclk input 1:Enable pclk input
14:2	/	/	/
1	R/W	0x0	PRS_MODE 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN 0: Reset and disable the parser module 1: Enable the parser module

8.1.6.2. Parser NCSI Interface Configuration Register(Default Value:0x0105_0080)

Offset: 0x0004			Register Name: PRS_NCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode,the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:22	/	/	/
21	R/W	0x0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	/	/	/
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: Negative(field=0 indicate odd, field=1 indicate even) 1: Positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence

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			0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity 0: Negative 1: Positive This register is not applied to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: Negative 1: Positive This register is not applied to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: Active in rising edge 1: Active in falling edge
15:14	R/W	0x0	Field_DT_MODE 00:by both field and vsync 01:by field 10:by vsync 11:reserved Only valid when CSI_IF is YUV and source type is interlaced.
13	R/W	0x0	DDR_SAMPLE_MODE_EN 0:Disable 1:Enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0] 10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH 000: 8 bits data bus 001: 10 bits data bus 010: 12 bits data bus 011: 8+2 bits data bus 100: 2x8 bits data bus Others: Reserved
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU

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			10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:Field mode 1:Frame mode
4:0	R/W	0x0	CSI_IF YUV(separate syncs): 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: 16 bits YUYV422 Interleaved 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16 bits BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16 bits BT656(BT1120 like) 2 channels(All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16 bits BT656(BT1120 like) 4 channels(All data interleaved in one data bus) Others: Reserved

8.1.6.3. Parser MCSI Interface Configuration Register(Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV

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			x1: VU
5	R/W	0x0	OUTPUT_MODE 0:Field mode 1:Frame mode
4:0	/	/	/

8.1.6.4. Parser Capture Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:26	R/W	0x0	CH3_CAP_MASK Vsync number masked before capture.
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	RC/W	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
13:12	/	/	/
21:18	R/W	0x0	CH2_CAP_MASK Vsync number masked before capture.
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	RC/W	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

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15:14	/	/	/
13:10	R/W	0x0	CH1_CAP_MASK Vsync number masked before capture.
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	RC/W	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
7:6	/	/	/
5:2	R/W	0x0	CH0_CAP_MASK Vsync number masked before capture.
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	RC/W	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

8.1.6.5. Parser Signal Status Register(Default Value:0x0000_0000)

Offset: 0x0010			**Register Name: PRS_SIGNAL_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	PCLK_STA Indicates the pclk status 0:Low 1:High

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23:0	R	0x0	DATA_STA Indicates the Dn status(n=0~23),MSB for D23,LSB for D0 0:Low 1:High

8.1.6.6. Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4-bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4-bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4-bit of BT656 header for channel 1 Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4-bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

8.1.6.7. Parser Channel_0 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0024			Register Name: PRS_CH0_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

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8.1.6.8. Parser Channel_0 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0028			Register Name: PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.6.9. Parser Channel_0 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x002C			Register Name: PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.6.10. Parser Channel_0 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.6.11. Parser Channel_0 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0034			Register Name: PRS_CH0_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

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8.1.6.12. Parser Channel_0 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0038			Register Name: PRS_CH0_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.6.13. Parser Channel_0 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x003C			Register Name: PRS_CH0_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.6.14. Parser Channel_0 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0040			Register Name: PRS_CH0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:Disable 1:Enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:Disable 1:Enable

8.1.6.15. Parser Channel_0 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: PRS_CH0_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD

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			Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register updates,this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register updates,this flag is set to 1. Write 1 to clear.

8.1.6.16. Parser Channel_1 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0124			Register Name: PRS_CH1_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.6.17. Parser Channel_1 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0128			Register Name: PRS_CH1_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.6.18. Parser Channel_1 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x012C			Register Name: PRS_CH1_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/

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12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.6.19. Parser Channel_1 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0130			Register Name: PRS_CH1_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.6.20. Parser Channel_1 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0134			Register Name: PRS_CH1_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.6.21. Parser Channel_1 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0138			Register Name: PRS_CH1_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.6.22. Parser Channel_1 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x013C			Register Name: PRS_CH1_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

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8.1.6.23. Parser Channel_1 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0140			Register Name: PRS_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:Disable 1:Enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:Disable 1:Enable

8.1.6.24. Parser Channel_1 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register updates,this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag is set to 1. Write 1 to clear.

8.1.6.25. Parser Channel_2 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0224			Register Name: PRS_CH2_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422

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			0100: YUV420 Others: reserved

8.1.6.26. Parser Channel_2 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0228			Register Name: PRS_CH2_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.6.27. Parser Channel_2 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x022C			Register Name: PRS_CH2_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.6.28. Parser Channel_2 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0230			Register Name: PRS_CH2_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.6.29. Parser Channel_2 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0234			Register Name: PRS_CH2_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT

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			INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.6.30. Parser Channel_2 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0238			Register Name: PRS_CH2_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.6.31. Parser Channel_2 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x023C			Register Name: PRS_CH2_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.6.32. Parser Channel_2 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0240			Register Name: PRS_CH2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:Disable 1:Enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:Disable 1:Enable

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8.1.6.33. Parser Channel_2 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0244			Register Name: PRS_CH2_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register updates,this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag is set to 1. Write 1 to clear.

8.1.6.34. Parser Channel_3 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0324			Register Name: PRS_CH3_INFMT_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.6.35. Parser Channel_3 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0328			Register Name: PRS_CH3_OUTPUT_HSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

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8.1.6.36. Parser Channel_3 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x032C			Register Name: PRS_CH3_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.6.37. Parser Channel_3 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0330			Register Name: PRS_CH3_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.6.38. Parser Channel_3 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0334			Register Name: PRS_CH3_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.6.39. Parser Channel_3 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0338			Register Name: PRS_CH3_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

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8.1.6.40. Parser Channel_3 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x033C			Register Name: PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.6.41. Parser Channel_3 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0340			Register Name: PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:Disable 1:Enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:Disable 1:Enable

8.1.6.42. Parser Channel_3 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0344			Register Name: PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register updates,this flag is set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag is set to 1. Write 1 to clear.

8.1.6.43. Parser NCSI RX Signal0 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0500	Register Name: PRS_NCSI_RX_SIGNAL0_DLY_ADJ_REG

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Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.44. Parser NCSIC RX Signal1 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0504			Register Name: PRS_NCSIC_RX_SIGNAL1_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D23_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D22_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D21_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D20_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.45. Parser NCSIC RX Signal2 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0508			Register Name: PRS_NCSIC_RX_SIGNAL2_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D19_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D18_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D17_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/

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4:0	R/W	0x0	D16_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.46. Parser NCSI RX Signal3 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSI_RX_SIGNAL3_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.47. Parser NCSI RX Signal4 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSI_RX_SIGNAL4_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.48. Parser NCSI RX Signal5 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0514			Register Name: PRS_NCSI_RX_SIGNAL5_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.49. Parser NCSI RX Signal6 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0518			Register Name: PRS_NCSI_RX_SIGNAL6_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D3_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

8.1.6.50. Parser CSIC SYNC Enable Register(Default Value:0x0000_0000)

Offset :0x0520			Register Name: CSIC_SYNC_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	Input vsync singal source select 0000: Vsync signals all from 1 parser 0001: Vsync signals from 2 parser 0010: Vsync signals from 4 parser others:reserved
15:12	/	/	/
11:8	R/W	0x0	Generate sync singal benchmark select

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			Bit8: Use VSYNC_Input0 Bit9: Use VSYNC_Input1 Bit10: Use VSYNC_Input2 Bit11: Use VSYNC_Input3 Set 1 to use input
7:4	R/W	0x0	Parser input vsync singal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1to enable input
3	/	/	/
2	R/W	0x0	Parser sent sync singal by 0: FSYNC0 1: FSYNC1
1	R/W	0x0	Parser sync singal source select 0: From outside 1: Generate by self
0	R/W	0x0	Enable Parser sent sync singal 0: Disable 1: Enable

8.1.6.51. Parser CSIC SYNC Configure Register(Default Value:0x0000_0000)

Offset :0x0524			Register Name: CSIC_PULSE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PUL_WID Sync singal pulse width $N*T_{24M}$, $N*T_{24M} \geqslant 4*Tpclk$
15:0	R/W	0x0	SYNC_DISTANCE The interval of two sync signal

8.1.6.52. Parser CSIC VS Wait N Register(Default Value:0x0000_0000)

Offset :0x0528			Register Name: CSIC_SYNC_WAIT_N_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync signals come, these bits indicate the max wait time.

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8.1.6.53. Parser CSIC VS Wait M Register(Default Value:0x0000_0000)

Offset :0x052C			Register Name: CSIC_SYNC_WAIT_M_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode,vsync comes at the different time,these bits indicate the max wait time.

8.1.7. CSIC DMA Register Description

8.1.7.1. CSIC DMA Enable Register(Default Value:0x0000_0000)

Offset:0x0000			Register Name: CSIC_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	FRAME_CNT_EN When BK_TOP_EN is enabled,setting 1 to the bit indicates the Frame counter start to add. 0: Disable 1: Enable
4	R/W	0x0	DMA_EN When BK_TOP_EN is enabled,setting 1 to the bit indicates module works in DMA mode. 0: Disable 1: Enable
3	R/W	0x0	FBC_EN When BK_TOP_EN is enabled,setting 1 to the bit indicates module works in FBC mode. 0: Disable 1: Enable
2	R/W	0x0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	CLK_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN 0: Disable 1: Enable

8.1.7.2. CSIC DMA Configuration Register(Default Value:0x0000_0000)

Offset: 0x0004	Register Name: CSIC_DMA_CFG_REG

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Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:20	/	/	/
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set to RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: reserved 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: reserved When the input format is set to YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: field planar YCbCr 422 10-bit UV combined(UV sequence) 1101: field planar YCbCr 420 10-bit UV combined(UV sequence) 1110: field planar YCbCr 422 10-bit UV combined(VU sequence) 1111: field planar YCbCr 420 10-bit UV combined(VU sequence) When the input format is set to YUV420 0000: reserved

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			0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011~1100: reserved 1101: field planar YCbCr 420 10-bit UV combined(UV sequence) 1110: reserved 1111: field planar YCbCr 420 10-bit UV combined(VU sequence) Others: reserved
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
9:8	/	/	/
7:6	R/W	0x0	FPS_DS Fps down sample 00: no down sample 01: 1/2 fps, only receives the first frame every 2 frames 10: 1/3 fps, only receives the first frame every 3 frames 11: 1/4 fps, only receives the first frame every 4 frames
5:2	/	/	/
1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 00: 256 bytes (if hflip is enable, always select 256 bytes) 01: 512 bytes 10: 1K bytes 11: 2K bytes

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8.1.7.3. CSI DMA Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0010			Register Name: CSI_DMA_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN When BK_TOP_EN is enabled,FBC_EN is enabled,DMA_EN is disabled,these bits indicate input width in FBC mode. When BK_TOP_EN is enabled,FBC_EN is disabled,DMA_EN is enabled,these bits indicate horizontal pixel unit length. Valid pixel of a line in DMA mode.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.4. CSI DMA Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x0014			Register Name: CSI_DMA_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN When BK_TOP_EN is enabled,FBC_EN is enabled,DMA_EN is disabled,these bits indicate input height in FBC mode. When BK_TOP_EN is enabled,FBC_EN is disabled,DMA_EN is enabled,these bits indicate valid line number of a frame in DMA mode.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.7.5. CSI DMA FIFO 0 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSI_DMA_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When BK_TOP_EN is enabled,FBC_EN is enabled,DMA_EN is disabled,these bits indicate output address of overhead data in FBC mode. When BK_TOP_EN is enabled,FBC_EN is disabled,DMA_EN is enabled,these bits indicate FIFO 0 output buffer-A address in DMA mode.

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8.1.7.6. CSI DMA FIFO 1 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSI_DMA_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F1_BUFA When BK_TOP_EN is enabled,FBC_EN is enabled,DMA_EN is disabled,these bits indicate output address of compressed data in FBC mode. When BK_TOP_EN is enabled,FBC_EN is disabled,DMA_EN is enabled,these bits indicate FIFO 1 output buffer-A address in DMA mode.

8.1.7.7. CSI DMA FIFO 2 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSI_DMA_F2_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

8.1.7.8. CSI DMA Buffer Length Register(Default Value:0x0280_0500)

Offset: 0x0038			Register Name: CSI_DMA_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x280	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:14	/	/	/
13:0	R/W	0x500	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

8.1.7.9. CSI DMA Flip Size Register(Default Value:0x02D0_0500)

Offset: 0x003C			Register Name: CSI_DMA_FLIP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Vertical line number when in VFLIP mode. Unit is line.
15:13	/	/	/
12:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel.

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8.1.7.10. CSIC DMA Capture Status Register(Default Value:0x0000_0000)

Offset: 0x004C			Register Name: CSIC_DMA_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

8.1.7.11. CSI DMA Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSI_DMA_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	CLR_FRAME_CNT_INT_EN Set INT when clearing Frame cnt.
10	R/W	0x0	SENT_SYNC_INT_EN Set INT when sending a SYNC signal.
9	R/W	0x0	FBC_DATA_WRDDR_FULL_EN Error flag of FBC_DATA_WRDDR_FULL.
8	R/W	0x0	FBC_OVHD_WRDDR_FULL_EN Error flag of FBC_OVHD_WRDDR_FULL.
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync comes. And at this time load the buffer address for the coming frame. So after this irq come, changing the buffer address could only effect next frame.
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow

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			The bit is set when 3 FIFOs still overflow after the hblank.
5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame.The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

8.1.7.12. CSI DMA Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0054			**Register Name: CSI_DMA_INT_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
11	R/W1C	0x0	CLR_FRAME_CNT_INT Set INT when clearing Frame cnt.
10	R/W1C	0x0	SENT_SYNC_INT Set INT when sending a SYNC signal.
9	R/W1C	0x0	/
8	R/W1C	0x0	FBC_DATA_WRDDR_FULL_PD Error flag of FBC_DATA_WRDDR_FULL.
7	R/W1C	0x0	FBC_OVHD_WRDDR_FULL_PD Error flag of FBC_OVHD_WRDDR_FULL.

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6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

8.1.7.13. CSI DMA Line Counter Register(Default Value:0x0000_0000)

Offset: 0x0058			**Register Name: CSI_DMA_LINE_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM is set by user,when internal line counter reach the set value,the LC_PD will set.

8.1.7.14. CSIC DMA Frame Counter Register(Default Value:0x0000_0000)

Offset: 0x005C			**Register Name: CSIC_DMA_FRM_CNT_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FRM_CNT_CLR When the bit is set to 1,Frame cnt is cleared to 0
30:16	R/W	0x0	PCLK_DMA_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15:0	R	0x0	FRM_CNT Counter value of frame. When frame done comes, the internal counter value adds 1, and when the reg full ,it is cleared to 0 . When parser sent a sync signal,it is cleared to 0

8.1.7.15. CSI DMA Frame Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0060	**Register Name: CSI_DMA_FRM_CLK_CNT_REG**

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Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

8.1.7.16. CSIC DMA Accumulated and Internal Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0064			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W0C	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software checks this accumulated value and clears it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

8.1.7.17. CSIC DMA FIFO Statistic Register(Default Value:0x0000_0000)

Offset: 0x0068			Register Name: CSIC_DMA_FIFO_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.

8.1.7.18. CSIC DMA FIFO Threshold Register(Default Value:0x0000_0400)

Offset: 0x006C			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x400	FIFO_THRS

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			When FIFO occupied memory exceed the threshold, dram frequency can not change.

8.1.7.19. CSI DMA PCLK Statistic Register(Default Value:0x0000_7FFF)

Offset: 0x0070			Register Name: CSI_DMA_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x7FFF	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

8.1.7.20. CSIC DMA Feature List Register(Default Value:0x0000_0000)

Offset: 0x01F0			Register Name: CSIC_FEATURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R	0x0	DMA1_EMBEDDED_FBC 1: DMA1 Embedded FBC 0: only DMA1
0	R	0x0	DMA0_EMBEDDED_FBC 1: DMA0 Embedded FBC 0: only DMA0

8.1.8. CSIC CCI Register Description

8.1.8.1. CCI Control Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: CCI_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SINGLE_TRAN 0: Transmission idle 1: Start single transmission Automatically cleared to '0' when finished. Abort current transmission immediately if changing from '1' to '0'. If slave does not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. PACKET_CNT will return the sequence number when transmission fails. All format setting and data will be loaded from registers and FIFO when

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			transmission starts.
30	R/W	0x0	REPEAT_TRAN 0: Transmission idle 1: Repeated transmission When this bit is set to 1, transmission repeats when trigger signal (such as VSYNC/ VCAP done) repeats. If changing this bit from '1' to '0' during transmission, the current transmission will be guaranteed then stop.
29	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the CCI action after sending register address.
28	R/W	0x0	READ_TRAN_MODE 0: Send slave_id+W 1: Do not send slave_id+W Setting this bit to 1 if reading from a slave which register width is equal to 0.
27:24	R	0x0	TRAN_RESULT 000: OK 001: FAIL Other: Reserved
23:16	R	0x0	CCI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:2	/	/	/
1	R/W	0x0	SOFT_RESET 0: Normal 1: Reset
0	R/W	0x0	CCI_EN 0: Module disable 1: Module enable

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8.1.8.2. CCI Transmission Configuration Register(Default Value:0x1000_0000)

Offset: 0x0004			Register Name: CCI_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device does not response after **N*F_{SCL}** cycles. And software must do a reset to CCI module and send a stop condition to slave.
23:16	R/W	0x0	INTERVAL Define the interval between each packet in 40*F_{SCL} cycles.
15	R/W	0x0	PACKET_MODE Select load slave id / data width 0: Compact mode 1: Complete mode In compact mode, slave id/register width / data width will be loaded from CCI_FMT register, only address and data read from memory. In complete mode, they will be loaded from packet memory.
14:7	/	/	/
6:4	R/W	0x0	TRIG_MODE Transmit mode 000: Immediately, no trigger 001: Reserved 010: CSI0 int trigger 011: CSI1 int trigger
3:0	R/W	0x0	CSI_TRIG CSI Int trig signal select 0000: First HREF start 0001: Last HREF done 0010: Line counter trigger other: Reserved

8.1.8.3. CCI Packet Format Register(Default Value:0x0011_0001)

Offset: 0x0008			Register Name: CCI_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	SLV_ID 7-bit address
24	R/W	0x0	CMD 0: write 1: read
23:20	R/W	0x1	ADDR_BYTE How many bytes be sent as address 0~15
19:16	R/W	0x1	DATA_BYTE

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			How many bytes be sent/received as data 1~15 Normally use ADDR_DATA with 0_2, 1_1, 1_2, 2_1, 2_2 access mode. If DATA bytes is 0, transmission will not start. In complete mode, the ADDR_BYTE and DATA_BYTE is defined in high/low 4-bit of a byte.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format. Total bytes donot exceed 32bytes.

8.1.8.4. CCI Bus Control Register(Default Value:0x0000_2500)

Offset: 0x000C			Register Name: CCI_BUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	DLY_CYC 0~65535 F_{SCL} cycles between each transmission
15	R/W	0x0	DLY_TRIG 0: Disable 1: Execute transmission after internal counter delay when triggered
14:12	R/W	0x2	CLK_N CCI bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x5	CLK_M CCI output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10
7	R	0x0	SCL_STA SCL current status
6	R	0x0	SDA_STA SDA current status
5	R/W	0x0	SCL_PEN SCL PAD enable
4	R/W	0x0	SDA_PEN SDA PAD enable
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

8.1.8.5. CCI Interrupt Control Register(Default Value:0x0000_0000)

Offset: 0x0014	Register Name: CCI_INT_CTRL

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Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0x0	S_TRAN_ERR_INT_EN
16	R/W	0x0	S_TRAN_COM_INT_EN
15:2	/	/	/
1	R/W1C	0x0	S_TRAN_ERR_PD
0	R/W1C	0x0	S_TRAN_COM_PD

8.1.8.6. CCI Line Counter Trigger Control Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: CCI_LC_TRIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LN_CNT 0~8191: line counter send trigger when 1^{st}~8192^{th} line is received.

8.1.8.7. CCI FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0100~0x013C			Register Name: CCI_FIFO_ACC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DATA_FIFO From 0x100 to 0x13C, CCI data fifo is 64bytes, used in fifo input mode. CCI transmission read/write data from/to fifo in byte.

8.1.8.8. CCI Reserved Register(Default Value:0x0000_0000)

Offset: 0x0200~0x0220			Register Name: CCI_RSV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	From 0x200 to 0x220 address, normal TWI registers are copied here. All transmission will act like hardware controlling these registers. And do not change them in transmission.

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8.2. TV Decoder

8.2.1. Overview

The Television Decoder (TVD) is an interface that transforms Composite Video Broadcast Signal (CVBS) or component signal into YUV data.

Features:

- 4-channel CVBS input or 1-channel YPbPr and 1-channel CVBS
- YPbPr input, 576p/480p/576i/480i supported
- CVBS input, NTSC and PAL supported
- Supports YUV422, YUV420 format
- With 1 channel 3D comb filter
- Detection for signal locked and 625 lines
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

8.2.2. Block Diagram

Figure 8-17 shows the block diagram of TVD_TOP.

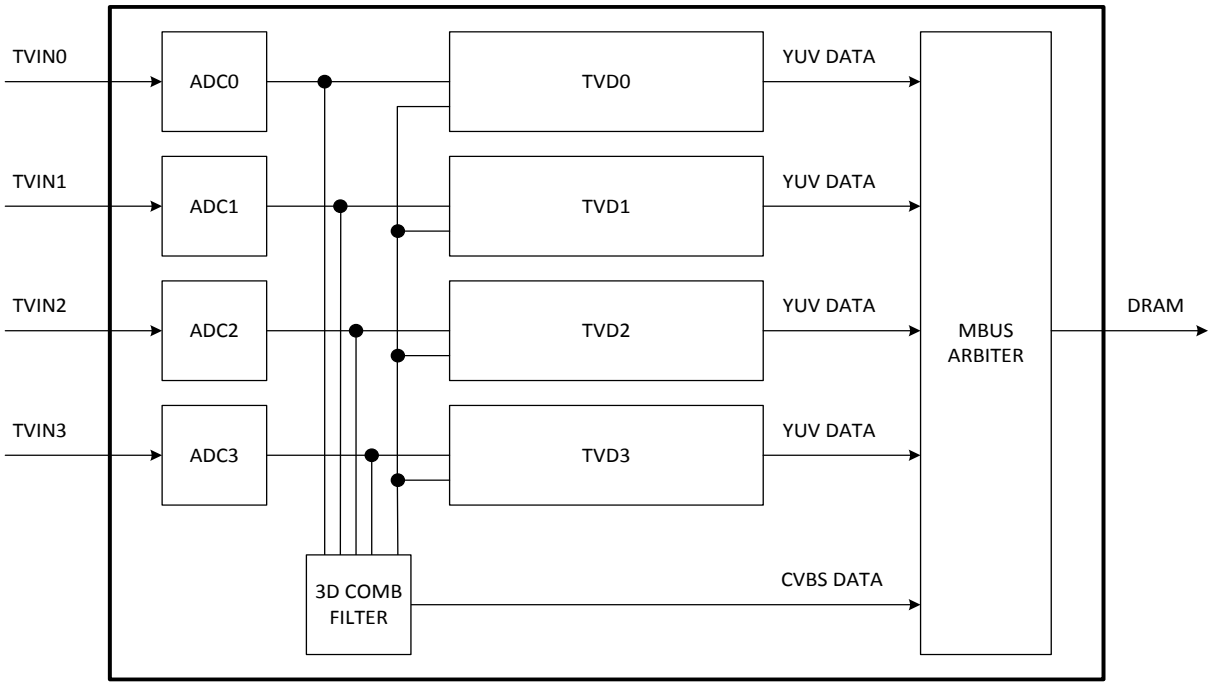

Figure 8- 17. TVD_TOP Block Diagram

Figure 8-18 shows the block diagram of TVD.

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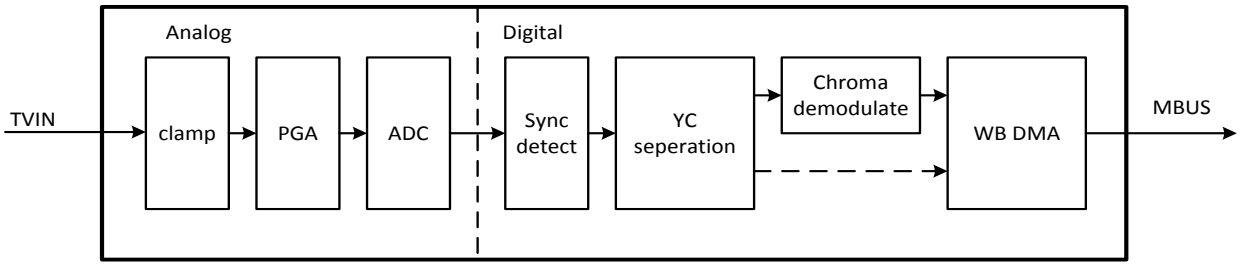

Figure 8- 18. TVD Block Diagram

WB DMA is used for TVD capture image writeback data.

Figure 8-19 shows the typical application diagrams of TVD.

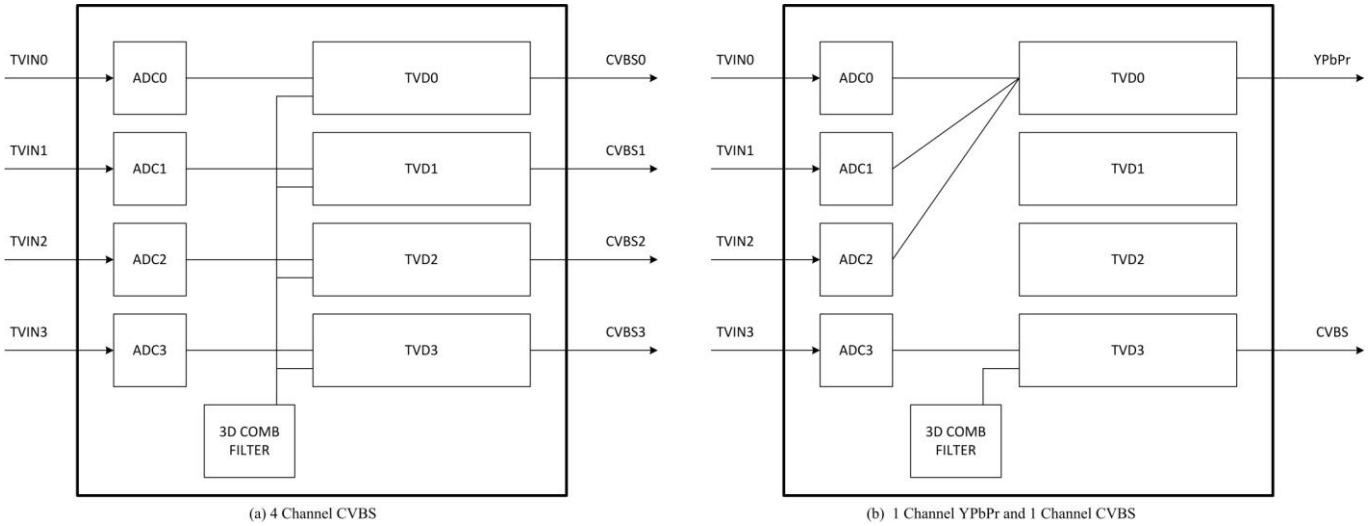

Figure 8- 19. TVD Application Diagram

8.2.3. Operations and Functional Descriptions

8.2.3.1. External Signals

Table 8-5 describes the external signals of TVD.

Table 8- 5. TVD External Signals

Signal	Description	Type
VCC-TVIN	TV ADC Power	P
GND-TVIN	TV ADC GND	P
TVIN-VRP	TV ADC Positive Reference Voltage	P
TVIN-VRN	TV ADC Negative Reference Voltage	P
TVIN0	TV Input Channel 0	AI
TVIN1	TV Input Channel 1	AI
TVIN2	TV Input Channel 2	AI
TVIN3	TV Input Channel 3	AI

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8.2.3.2. Clock Sources

TVD module requires one clock with 50% duty. Digital circuit and analog circuit work by this clock. Mode and clock frequency are shown below.

Table 8- 6. TVD Clock Frequency

	TVD Clock Frequency	Source Select	Clock Divide
NTSC	27MHz	VPLL_1X: 297MHz	11
PAL	29.7MHz	VPLL_1X: 297MHz	10
480I	27MHz	VPLL_1X: 297MHz	11
576I	27MHz	VPLL_1X: 297MHz	11
480P	54MHz	VPLL_2X: 594MHz	11
576P	54MHz	VPLL_2X: 594MHz	11

8.2.3.3. CVBS Timing

The timing of CVBS shows in Figure 8-20.

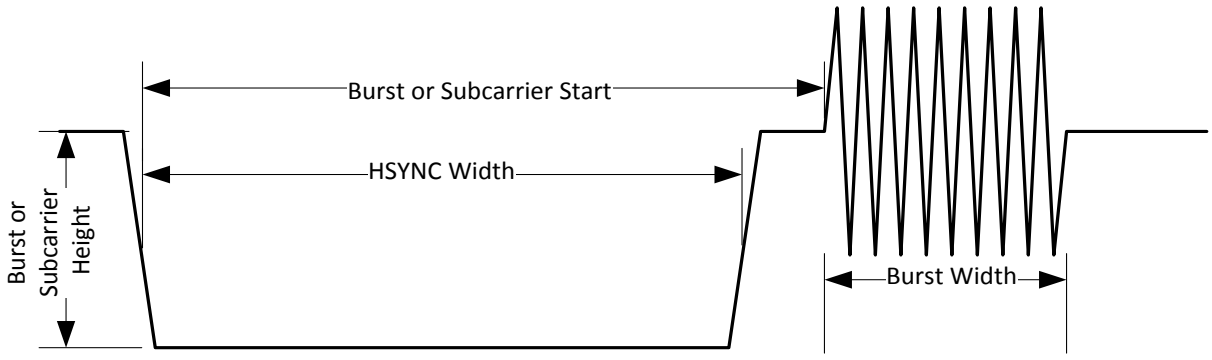

Figure 8- 20. CVBS Timing

The timing parameters of CVBS shows in Table 8-7.

Table 8- 7. CVBS Timing Constants

	Video Standard					
Paramter Description	NTSC-M	NTSC-J	PAL-M	PAL-B,D, G,H,I	PAL-N	PAL-Nc
HSYNC Width (us)	4.7	4.7	4.7	4.7	4.7	4.7
HSYNC VSYNC Height (V)	0.286	0.286	0.2857	0.3	0.2857	0.3

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HSYNC Rise/Fall Time (10% to 90%) (ns)	150	150	150	200	200	200
Burst or Subcarrier Start (us)	5.3	5.3	5.8	5.6	5.6	5.6
Burst Width (us)	2.514 (9 cycle)	2.514 (9 cycle)	2.52 (9 cycle)	2.25 (10 cycle)	2.25 (10 cycle)	2.51 (9 cycle)
Subcarrier Frequency (Hz)	3579545	3579545	3579611.49	4433618.75	4433618.75	3582056.25
Burst or Subcarrier Height (V)	0.2857	0.2857	0.306	0.3	0.3	0.3
Phase Alternation	NO	NO	YES	YES	YES	YES
Number of Lines per Frame	525	525	525	625	625	625
Line Frequency (Hz)	15734.264	15734.264	15734.264	15625	15625	15625
Field Frequency (Hz)	59.94	59.94	59.94	50	50	50
Setup	YES	NO	YES	YES	YES	NO
First Active Line	22	22	22	23	23	23
Last Active Line	262	262	262	309	309	309
HSYNC to Blank End (us)	9.2	9.2	9.2	10.5	9.2	10.5
Blank Begin to HSYNC (us)	1.5	1.5	1.5	1.5	1.5	1.5
Blank to 100% White (V)	0.661	0.714	0.661	0.7	0.661	0.7
Number of Lines each for Vertical Serration, Equalization	3	3	3	2.5	3	2.5

8.2.4. Programming Guidelines

8.2.4.1. Operation Flow Chart

Software is recommended to operation TVD module by the following steps, as shown by Figure 8-21.

(1) Set CCU clock source for TVD, and release AHB bus, and module reset.

(2) Initial ADC register and TVD module enable. After this step, TVD work and detection enable.

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(3) Read the NO_SIG_DET and 625_LINE_DET of the TVD_STATUS4 register in interval time.
(4) When valid signal is detected, configure TVD mode and enable TVD write back.

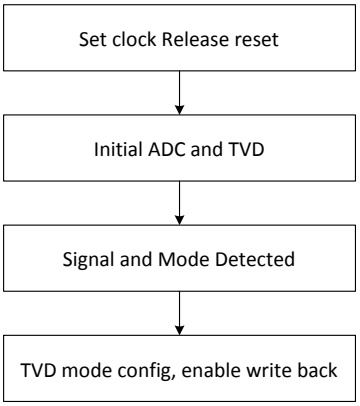

Figure 8- 21. Operation Flow Chart

8.2.4.2. Write Back Buffer Operation

It is recommended to switch write back buffer in FRAME_END_IRQ. FRAME_END_IRQ function handle is required to operation as follows:

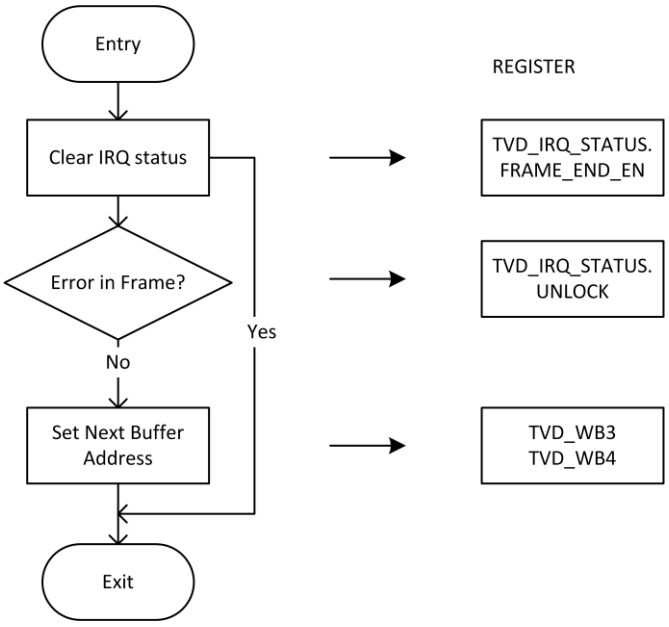

Figure 8- 22. FRAME_END_IRQ Operation

Image buffer ring is recommended to use for TVD buffer switch, and display engineer can show buffer which has completed write back. Image buffer ring is shown as Figure 8-23.

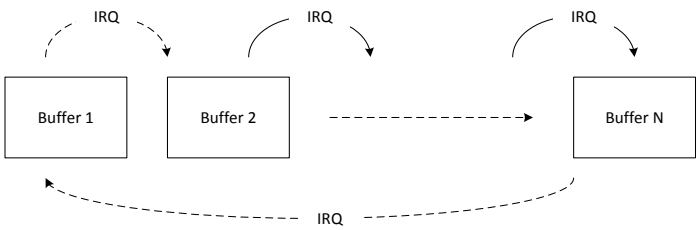

Figure 8- 23. Image Buffer Ring

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RAME_END_IRQ is trigged at vsync falling edge every frame. Vsync falling edge also triggers the WB_ADDR_VALID of the TVD_WB1 register which is set to '1', TVD WB address is auto updated to TVD_WB3/TVD_WB4. As Figure 8-24 shows.

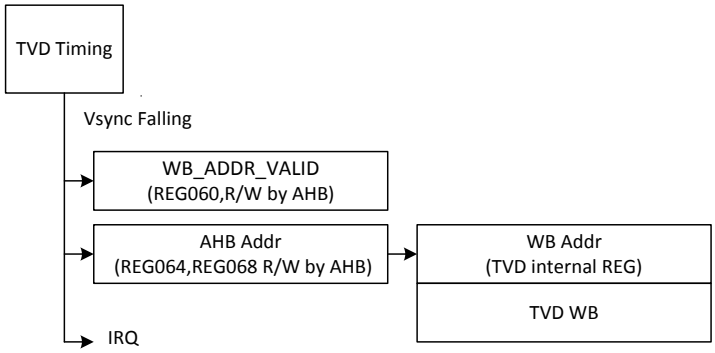

Figure 8- 24. IRQ and Buffer Switch Flow

8.2.5. Register List

Module Name	Base Address
TVD_TOP	0x06530000
TVD0	0x06531000
TVD1	0x06532000
TVD2	0x06533000
TVD3	0x06534000

Register Name	Offset	Description
TVD_TOP		
TVD_TOP_MAP	0x0000	TVD TOP MAP Register
TVD_3D_CTL1	0x0008	TVD 3D DMA Control Register1
TVD_3D_CTL2	0x000C	TVD 3D DMA Control Register2
TVD_3D_CTL3	0x0010	TVD 3D DMA Control Register3
TVD_3D_CTL4	0x0014	TVD 3D DMA Control Register4
TVD_3D_CTL5	0x0018	TVD 3D DMA Control Register5
TVD_TOP _CTL	0x0024+N*0x20(N=0~3)	TVD TOP Control Register
TVD_ADC_CTL	0x0028+N*0x20(N=0~3)	TVD ADC Control Register
TVD_ADC_CFG	0x002C+N*0x20(N=0~3)	TVD ADC Configuration Register
TVD		
TVD_CTRL	0x0000	TVD Module Control Register
TVD_MODE	0x0004	TVD Mode Control Register
TVD_CLAMP_AGC1	0x0008	TVD CLAMP & AGC Control Register1
TVD_CLAMP_AGC2	0x000C	TVD CLAMP & AGC Control Register2
TVD_HLOCK1	0x0010	TVD HLOCK Control Register1
TVD_HLOCK2	0x0014	TVD HLOCK Control Register2
TVD_HLOCK3	0x0018	TVD HLOCK Control Register3

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TVD_HLOCK4	0x001C	TVD HLOCK Control Register4
TVD_HLOCK5	0x0020	TVD HLOCK Control Register5
TVD_VLOCK1	0x0024	TVD VLOCK Control Register1
TVD_VLOCK2	0x0028	TVD VLOCK Control Register2
TVD_CLOCK1	0x002C	TVD Chroma Lock Control Register1
TVD_CLOCK2	0x0030	TVD Chroma Lock Control Register2
TVD_YC_SEP1	0x0040	TVD YC Seperation Control Register1
TVD_YC_SEP2	0x0044	TVD YC Seperation Control Register2
TVD_ENHANCE1	0x0050	TVD Enhancement Control Register1
TVD_ENHANCE2	0x0054	TVD Enhancement Control Register2
TVD_ENHANCE3	0x0058	TVD Enhancement Control Register3
TVD_WB1	0x0060	TVD WB DMA Control Register1
TVD_WB2	0x0064	TVD WB DMA Control Register2
TVD_WB3	0x0068	TVD WB DMA Control Register3
TVD_WB4	0x006C	TVD WB DMA Control Register4
TVD_IRQ_CTL	0x0080	TVD DMA Interrupt Control Register
TVD_IRQ_STATUS	0x0090	TVD DMA Interrupt Status Register
TVD_DEBUG1	0x0100	TVD Debug Control Register1
TVD_STATUS1	0x0180	TVD Debug Status Register1
TVD_STATUS2	0x0184	TVD Debug Status Register2
TVD_STATUS3	0x0188	TVD Debug Status Register3
TVD_STATUS4	0x018C	TVD Debug Status Register4
TVD_STATUS5	0x0190	TVD Debug Status Register5
TVD_STATUS6	0x0194	TVD Debug Status Register6

8.2.6. TVD TOP Register Description

8.2.6.1. TVD TOP Map Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: TVD_TOP_MAP**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	TVD_ADC_MAP 00: NO MAP 01: 4 CVBS 10: 1 YPbPr and 1 CVBS 11: Reserved

8.2.6.2. TVD 3D DMA Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: TVD_3D_CTL1**
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:6	/	/	/
5:4	R/W	0x1	COMB_3D_SEL 00: TVD0 01: TVD1 10: TVD2 11: TVD3
3:2	/	/	/
1	R/W	0x1	COMB_3D_EN 0: Disable 1: Enable
0	R/W	0x0	TVD_EN_3D_DMA 0: Disable 1: Enable Set 0x1 when enable 3D comb filter.

8.2.6.3. TVD 3D DMA Control Register2 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TVD_3D_CTL2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DRAM_TRIG

8.2.6.4. TVD 3D DMA Control Register3 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: TVD_3D_CTL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_ADDR0

8.2.6.5. TVD 3D DMA Control Register4 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TVD_3D_CTL4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_ADDR1

8.2.6.6. TVD 3D DMA Control Register5 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TVD_3D_CTL5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_SIZE

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8.2.6.7. TVD TOP Control Register (Default Value: 0x0000_0000)

Offset: 0x0024+0x20*N(N=0~3)			Register Name: TVD_TOP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	LPF_SEL 0: 6M 1: 8M
23:5	/	/	/
4	R/W	0x0	LPF_DIG_EN 0: Disable 1: Enable
3:0	/	/	/

8.2.6.8. TVD ADC Control Register (Default Value: 0x0000_0000)

Offset: 0x0028+0x20*N(N=0~3)			Register Name: TVD_ADC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:3	R/W	0x0	LPF_SEL 00: 11MHz 01: 16MHz
2	R/W	0x0	LPF_EN 0: Disable LPF circuit 1: Enable LPF circuit
1	R/W	0x0	AFE_EN 0: Disable AFE circuit 1: Enable AFE circuit
0	R/W	0x0	ADC_EN 0: Disable ADC circuit 1: Enable ADC circuit

8.2.6.9. TVD ADC Configuration Register (Default Value: 0x0000_0000)

Offset: 0x002C+0x20*N(N=0~3)			Register Name: TVD_ADC_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_TEST 0: Normal mode 1: For ADC test
30:29	/	/	/
28	R/W	0x0	DATA_DLY 0: No delay

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			1: Delay ADC output data for half circle
27:19	/	/	/
18:16	R/W	0x0	CLP_STEP DC level size step for up and down.
15:14	R/W	0x0	STAGE8_IBIAS
13:12	R/W	0x0	STAGE7_IBIAS
11:10	R/W	0x0	STAGE6_IBIAS
9:8	R/W	0x0	STAGE5_IBIAS
7:6	R/W	0x0	STAGE4_IBIAS
5:4	R/W	0x0	STAGE3_IBIAS
3:2	R/W	0x0	STAGE2_IBIAS
1:0	R/W	0x0	STAGE1_IBIAS

8.2.7. TVD Register Description

8.2.7.1. TVD Module Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: TVD_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	EN_LOCK_DISABLE_WB2
25	R/W	0x0	EN_LOCK_DISABLE_WB1
24:16	/	/	/
15	R/W	0x0	CLR_RSMP_FIFO 0: Release 1: Clear Set 0x1 then 0x0 to reset resample FIFO.
14:1	/	/	/
0	R/W	0x0	TVD_EN_CH 0: Disable 1: Enable

8.2.7.2. TVD Mode Control Register (Default Value: 0x0000_0020)

Offset: 0x0004			**Register Name: TVD_MODE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	BLUE_MODE_COLOR 0: Blue 1: Black
7:6	/	/	/
5:4	R/W	0x2	BLUE_DISPLAY_MODE

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			00 : Disabled 01 : Enabled 10 : Auto 11 : Reserved
3	/	/	/
2	R/W	0x0	PROGRESSIVE_MODE 0: Interlace mode 1: Progressive mode
1	R/W	0x0	SVIDEO_MODE 0 : CVBS 1 : S-Video
0	R/W	0x0	YPBPR_MODE 0 : Disable the component input 1 : Enable the component input

8.2.7.3. TVD CLAMP & AGC Control Register1 (Default Value: 0xA001_DD02)

Offset: 0x0008			Register Name: TVD_CLAMP_AGC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	CAGC_TARGET These bits set the chroma AGC target
23:17	/	/	/
16	R/W	0x1	CAGC_EN 0 : OFF 1 : ON
15:8	R/W	0xDD	AGC_TARGET When AGC_EN = 1 , the AGC_TARGET is used to directly digital AGC circuit. When AGC_EN = 0 , the AGC_TARGET is used to directly drive the analog PGA. (64 represents 1x, 32 represents 0.5x).
7:2	/	/	/
1	R/W	0x1	AGC_FREQUENCE 0 : AGC gain update once per line 1 : AGC gain update once per frame
0	R/W	0x0	AGC_EN 0 : AGC disable 1 : AGC enable

8.2.7.4. TVD CLAMP & AGC Control Register2 (Default Value: 0x8682_6440)

Offset: 0x000C			Register Name: TVD_CLAMP_AGC2
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	R/W	0x1	BLACK_LEVEL_CLAMP 0: subtraction 0 1: subtraction 16
30:29	/	/	/
28:16	R/W	0x682	AGC_GATE_BEGIN Count from hsync to the next line AGC gate
15:8	R/W	0x64	AGC_BACKPORCH_DELAY Count from sync tip to back porch gate
7	/	/	/
6:0	R/W	0x40	AGC_GATE_WIDTH AGC gate width

8.2.7.5. TVD HLOCK Control Register1 (Default Value: 0x2000_0000)

Offset: 0x0010			Register Name: TVD_HLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x20000000	H_SAMPLE_STEP H_SAMPLE_STEP = F_{out}/F_{in} * 2^30

8.2.7.6. TVD HLOCK Control Register2 (Default Value: 0x4ED6_0000)

Offset: 0x0014			Register Name: TVD_HLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x4E	HSYNC_FILTER_GATE_END_TIME These bits specify the end of the horizontal-blank-interval window. Default/Hex = 78
23:16	R/W	0xD6	HSYNC_FILTER_GATE_START_TIME These bits specify the beginning of the horizontal-blank-interval window. Default/Hex = -42
15:4	/	/	/
3:0	R/W	0x0	HTOL 0000: 858 0001: 864 0010~0111: Reserved Horizontal total pixels per line.

8.2.7.7. TVD HLOCK Control Register3 (Default Value: 0x0FE9_502D)

Offset: 0x0018			Register Name: TVD_HLOCK3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0F	HSYNC_TIP_DETECT_WINDOW_END_TIME

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23:16	R/W	0xE9	HSYNC_TIP_DETECT_WINDOW_START_TIME
15:8	R/W	0x50	HSYNC_RISING_DETECT_WINDOW_END_TIME
7:0	R/W	0x2D	HSYNC_RISING_DETECT_WINDOW_START_TIME

8.2.7.8. TVD HLOCK Control Register4 (Default Value: 0x3E3E_8000)

Offset: 0x001C			Register Name: TVD_HLOCK4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x3E	HSYNC_FINE_TO_COARSE_OFFSET
23:16	R/W	0x3E	HSYNC_RISING_TIME_FOR_FINE_DETECT
15:8	R/W	0x80	HSYNC_DETECT_WINDOW_END_TIME_FOR_CORASE_DETECT
7:0	R/W	0x00	HSYNC_DETECT_WINDOW_START_TIME_FOR_COARSE_DETECTION

8.2.7.9. TVD HLOCK Control Register5 (Default Value: 0x4E22_5082)

Offset: 0x0020			Register Name: TVD_HLOCK5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x4E	BACKPORCH_DETECT_WINDOW_END_TIME
23:16	R/W	0x22	BACKPORCH_DETECT_WINDOW_START_TIME
15:8	R/W	0x50	HACTIVE_WIDTH
7:0	R/W	0x82	HACTIVE_START

8.2.7.10. TVD VLOCK Control Register1 (Default Value: 0x0061_0220)

Offset: 0x0024			Register Name: TVD_VLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x61	VACTIVE_HEIGHT
15	/	/	/
14:4	R/W	0x22	VACTIVE_START
3	/	/	/
2:0	R/W	0x0	VTOL 0 : 525 line 1 : 625 line

8.2.7.11. TVD VLOCK Control Register2 (Default Value: 0x000E_0070)

Offset: 0x0028			Register Name: TVD_VLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/

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20:16	R/W	0xE	HSYNC_DETECTOR_DISABLE_END_LINE
15:7	/	/	/
6:0	R/W	0x70	HSYNC_DECTECTOR_DISABLE_START_LINE

8.2.7.12. TVD Chroma Lock Control Register1 (Default Value: 0x0046_3201)

Offset: 0x0030			Register Name: TVD_CLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	COLOR_STD_NTSC 0: NTSC358 1: NTSC443 Only valid when COLOR_STD set as NTSC
27:26	R/W	0x0	CHROMA_LPF 00: Narrow 01: Middle 10: Wide 11: Reserved
25	/	/	/
24	R/W	0x0	WIDE_BURST_GATE 0: Narrow burst gate 1: Wide burst gate
23:16	R/W	0x46	BURST_GATE_END_TIME
15:8	R/W	0x32	BURST_GATE_START_TIME
7:4	/	/	/
3:1	R/W	0x0	COLOR_STD 000: NTSC 001: PAL (I,B,G,H,D,N) 010: PAL (M) 011: PAL (CN) 100: SECAM
0	R/W	0x1	COLOR_KILLER_EN 1: Disable color when chroma unlock

8.2.7.13. TVD Chroma Lock Control Register2 (Default Value: 0x21F0_7C1F)

Offset: 0x0034			Register Name: TVD_CLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21F07C1F	C_SAMPLE_STEP C_SAMPLE_STEP = F_{sc}/Fin * 2^30

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8.2.7.14. TVD YC Seperation Control Register1 (Default Value: 0x0000_4209)

Offset: 0x0040			Register Name: TVD_YC_SEP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	CHROMA_CORING_ENABLE
28:26	R/W	0x0	3D_COMB_FACTOR
25:23	R/W	0x0	2D_COMB_FACTOR
22:20	R/W	0x0	NOTCH_FACTOR
19:17	/	/	/
16	R/W	0x0	COMB_FILTER_BUFFER_CLEAR 0: Not clear 1: Clear
15:10	R/W	0x10	PAL_CHROMA_LEVEL Chroma level threshold for chroma comb filter select
9	R/W	0x1	CHROMA_BANDPASS_FILTER_EN 0: Disable 1: Enable
8	R/W	0x0	SECAM_NOTCH_WIDE Notch bandwidth 0: Narrow 1: Wide
7:4	R/W	0x0	2D_COMB_FILTER_MODE For NTSC: 0000: 2D comb 0001~0010: Reserved 0011: 1D comb 0100~1000: Reserved For PAL: 0000:2D comb filter1 0001: 1D comb filter1 0010: 2D comb filter2 0011: 1D comb filter2 0100: 1D comb filter3 0101: Reserved 0110: 2D comb filter3 0111~1000:Reserved
3	R/W	0x1	3D_COMB_FILTER_DIS 0: Enable 3D comb filter 1: Disable 3D comb filter
2:0	R/W	0x1	3D_COMB_FILTER_MODE 000: 2D mode 001: 3D YC separation mode1 010~011: reserved 0100: 3D YC separation mode2

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8.2.7.15. TVD YC Seperation Control Register2 (Default Value: 0xFF00_00AF)

Offset: 0x0044			Register Name: TVD_YC_SEP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x3	VERTICAL_NOISE_FACTOR
29:28	R/W	0x3	BURST_NOISE_FACTOR
27:26	R/W	0x3	CHROMA_NOISE_FACTOR
25:24	R/W	0x3	LUMA_NOISE_FACTOR
23:17	R/W	0x32	NOISE_THRESHOLD
16	R/W	0x0	NOISE_DETECT_EN
15:9	R/W	0x20	MOTION_DETECT_NOISE_THRESHOLD
8	R/W	0x0	MOTION_DETECT_NOISE_DETECT_EN
7:6	R/W	0x2	CHROMA_VERTICAL_FILTER_GAIN
5:4	R/W	0x2	LUMA_VERTICAL_FILTER_GAIN
3:2	R/W	0x3	HORIZONTAL_CHROMA_FILTER_GAIN
1:0	R/W	0x3	HORIZONTAL_LUMA_FILTER_GAIN

8.2.7.16. TVD Enhancement Control Register1 (Default Value: 0x1420_8000)

Offset: 0x0050			Register Name: TVD_ENHANCE1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	Reserved
29:28	R/W	0x1	SHARP_COEF2
27:25	R/W	0x2	SHARP_COEF1 Y_{sharp} = Y + YH *(SHARP_COEF1/ SHARP_COEF2)
24	R/W	0x0	SHARP_EN 0: Disable 1: Enable
23:16	R/W	0x20	BRIGHT_OFFSET Set 0x00, brightness offset is -32; Set 0x20, brightness offset is 0; Set 0xFF, brightness offset is max.
15:8	R/W	0x80	CONTRAST_GAIN Set 0x00, contrast gain is min ; Set 0x80, contrast gain is 1; Set 0xFF, contrast gain is max.
7:4	/	/	Reserved
3:0	R/W	0x0	YC_DELAY 0000: Y and C no delay 0001: Y delay 1 cycle to C 0010: Y delay 2 cycle to C

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			0011: Y delay 3 cycle to C 0100: Y delay 4 cycle to C 0101: Y delay 5 cycle to C 0110: Y delay 6 cycle to C 0111: Y delay 7 cycle to C 1000: Reserved 1001: Reserved 1010: Reserved 1011: C delay 5 cycle to Y 1100: C delay 4 cycle to Y 1101: C delay 3 cycle to Y 1110: C delay 2 cycle to Y 1111: C delay 1 cycle to Y

8.2.7.17. TVD Enhancement Control Register2 (Default Value: 0x0000_0680)

Offset: 0x0054			Register Name: TVD_ENHANCE2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	Reserved
10:9	R/W	0x3	CHROMA_ENHANCE_STRENGTH 00:Mild 01: Low 10: Middle 11: High
8	R/W	0x0	CHROMA_ENHANCE_EN 0: Disable 1: Enable
7:0	R/W	0x80	SATURATION_GAIN Set 0x00, saturation gain is min ; Set 0x80, saturation gain is 1; Set 0xFF, saturation gain is max.

8.2.7.18. TVD Enhancement Control Register3 (Default Value: 0x0000_0080)

Offset: 0x0058			Register Name: TVD_ENHANCE3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	CB_CR_GAIN_EN
27:16	R/W	0x0	CR_GAIN
15:12	/	/	/
11:0	R/W	0x80	CB_GAIN

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8.2.7.19. TVD WB DMA Control Register1 (Default Value: 0x02D0_0020)

Offset: 0x0060			Register Name: TVD_WB1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	UV_SEQUENCE 0: UVUV 1: VUVU
30:29	/	/	/
28	R/W	0x0	YUV420 Filter Enable 0: disable YUV420 WB data from YUV422 without chroma filter 1: enable YUV420 WB data from YUV422 with chroma filter
27:16	R/W	0x2D0	HACTIVE_STRIDE Horizontal active line stride.
15:9	/	/	/
8	R/W	0x0	WB_ADDR_VALID 0: Invalid 1: Valid
7	/	/	/
6	R/W	0x0	FLIP_FIELD This bit flips even/odd fields
5	R/W	0x1	WB_FRAME_MODE 0: Odd field or even field (desided by bit2) 1: Frame
4	R/W	0x0	WB_MB_MODE 0: Planar mode 1: Mb mode
3	R/W	0x0	HYSCALE_EN
2	R/W	0x0	FIELD_SEL 0: field 0 only 1: filed 1 only
1	R/W	0x0	WB_FORMAT 0: YUV420 1: YUV422
0	R/W	0x0	WB_EN 0: Disable 1: Enable

8.2.7.20. TVD WB DMA Control Register2 (Default Value: 0x00F0_02D0)

Offset: 0x0064			Register Name: TVD_WB2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0xF0	VACTIVE_NUM

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			Vertical active line number.
15:12	/	/	/
11:0	R/W	0x2D0	HACTIVE_NUM Horizontal active pixel number.

8.2.7.21. TVD WB DMA Control Register3 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: TVD_WB3
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CH1_Y_ADDR

8.2.7.22. TVD WB DMA Control Register4 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: TVD_WB4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CH1_C_ADDR

8.2.7.23. TVD DMA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			**Register Name: TVD_IRQ_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_3D_TX_O_EN 0: IRQ disable 1: IRQ enable
30	R/W	0x0	FIFO_3D_TX_U_EN 0: IRQ disable 1: IRQ enable
29	R/W	0x0	FIFO_3D_RX_O_EN 0: IRQ disable 1: IRQ enable
28	R/W	0x0	FIFO_3D_RX_U_EN 0: IRQ disable 1: IRQ enable
27:25	/	/	Reserved
24	R/W	0x0	FRAME_END_EN 0: IRQ disable 1: IRQ enable
23:9	/	/	Reserved
8	R/W	0x0	FIFO_Y_U_EN 0: IRQ disable 1: IRQ enable

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7	R/W	0x0	FIFO_PB_U_EN 0: IRQ disable 1: IRQ enable
6	R/W	0x0	FIFO_PR_U_EN 0: IRQ disable 1: IRQ enable
5	R/W	0x0	FIFO_Y_O_EN 0: IRQ disable 1: IRQ enable
4	R/W	0x0	FIFO_PB_O_EN 0: IRQ disable 1: IRQ enable
3	R/W	0x0	FIFO_PR_O_EN 0: IRQ disable 1: IRQ enable
2	/	/	Reserved
1	R/W	0x0	UNLOCK_EN 0: IRQ disable 1: IRQ enable
0	R/W	0x0	LOCK_EN 0: IRQ disable 1: IRQ enable

8.2.7.24. TVD DMA Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TVD_IRQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FIFO_3D_TX_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
30	R/W1C	0x0	FIFO_3D_TX_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
29	R/W1C	0x0	FIFO_3D_RX_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
28	R/W1C	0x0	FIFO_3D_RX_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.

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27:25	/	/	/
24	R/W1C	0x0	FRAME_END This bit is auto set every write back frame. Set 0x1 to clear this bit.
23:17	/	/	/
16	R/W	0x0	WB_ADDR_CHANGE_ERR Write back address change error
15:9	/	/	/
8	R/W1C	0x0	FIFO_Y_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
7	R/W1C	0x0	FIFO_C_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
6	/	/	/
5	R/W1C	0x0	FIFO_Y_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
4	R/W1C	0x0	FIFO_C_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
3:2	/	/	/
1	R/W	0x0	UNLOCK 0: TVD status no change 1: TVD status change from lock to unlock
0	R/W	0x0	LOCK 0: TVD status no change 1: TVD status change from unlock to lock

8.2.7.25. TVD Debug Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			**Register Name: TVD_DEBUG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	CLAMP_UPDN_CYCLES
24	R/W	0x0	CLAMP_DN_START Write 0x1 to make clamp up, clamp up value is determine by CLAMP_UPDN_CYCLES. Note that this bit is only valid when CLAMP_MODE is set as 0x1.
23	R/W	0x0	CLAMP_UP_START Write 0x1 to make clamp up, clamp up value is determine by

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			CLAMP_UPDN_CYCLES. Note that this bit is only valid when CLAMP_MODE is set as 0x1.
22	R/W	0x0	CLAMP_MODE 0: Normal, auto clamp control 1: Debug mode, clamp control by register
21	R/W	0x0	AFE_GAIN_MODE 0: Auto gain mode 1: Debug mode, AFE gain is determine by AFE_GAIN_VALUE
20	R/W	0x1	UNLOCK_RESET_GAIN_EN
19	R/W	0x0	TRUNCATION_RESET_GAIN_EN
18	R/W	0x0	TRUNCATION2_RESET_GAIN_EN
17	R/W	0x0	TVIN LOCK HIGH
16	R/W	0x0	TVIN LOCK DEBUG
15:8	R/W	0x0	AFE_GAIN_VALUE
7:0	/	/	/

8.2.7.26. TVD Debug Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: TVD_STATUS1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	Reserved
23:16	R	0x0	CHROMA_MAGNITUDE_STATUS These bits contain the chroma magnitude.
15:8	R	0x0	AGC_DEGITAL_GAIN_STATUS These bits contain the digital AGC gain value.
7:0	R	0x0	AGC_ANALOG_GAIN_STATUS These bits contain the analog AGC gain value.

8.2.7.27. TVD Debug Status Register2 (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: TVD_STATUS2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x00000000	CHROMA_SYNC_DTO_STATUS

8.2.7.28. TVD Debug Status Register3 (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: TVD_STATUS3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x00000000	HORIZONTAL_SYNC_DTO_STATUS

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8.2.7.29. TVD Debug Status Register4 (Default Value: 0x0000_0001)

Offset: 0x018C			Register Name: TVD_STATUS4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	VCR_REW VCR Rewind Detected
22	R	0x0	VCR_FF VCR Fast-Forward Detected
21	R	0x0	VCR_TRICK VCR Trick-Mode Detected
20	R	0x0	VCR VCR Detected
19	R	0x0	NOISY Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the “noise_thresh” register (05h).
18	R	0x0	625_LINE_DET 0: 525 lines 1: 625 lines
17	R	0x0	SECAM_DET SECAM Colour Mode Detected
16	R	0x0	PAL_DET PAL Colour Mode Detected
15:11	R	0x0	Reserved
10	R	0x0	VNON_STANDARD Vertical frequency non-standard input signal Detected
9	R	0x0	HNON_STANDARD Horizontal frequency non-standard input signal Detected
8	R	0x0	PROSCAN_DET Progressive Scan Detected
7:5	R	0x0	MACROVISION_COLOR_STRIPES_DET The number indicates the number of color stripe lines in each group
4	R	0x0	MACROVISION_VBI_PSEUDO_SYNC_PULSES_DET 0: Undetected 1: Detected
3	R	0x0	CHROMA_PLL_LOCKED_TO_COLOR_BURST 0: Unlock 1: Locked
2	R	0x0	Vertical lock 0: Unlock 1: Locked
1	R	0x0	Horizontal line locked

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			0: Unlock 1: Locked
0	R	0x1	NO_SIG_DET 0: Signal Detected 1: No Signal Detected

8.2.7.30. TVD Debug Status Register5 (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: TVD_STATUS5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R	0x0	BLANK_LEVEL
15:11	/	/	/
10:0	R	0x0	SYNC_LEVEL

8.2.7.31. TVD Debug Status Register6 (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: TVD_STATUS6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	MASK_UNKNOWN
9	R/W	0x0	MASK_SECAM
8	R/W	0x0	MASK_NTSC443
7	R/W	0x0	MASK_PAL60
6	R/W	0x0	MASK_PALCN
5	R/W	0x0	MASK_PALM
4	R/W	0x0	AUTO_DETECT_EN 0: Disable 1: Enable
3:1	R	0x0	TV STANDARD 001: V525_NTSC 010: V625_PAL 011: V525_PALM 100: V625_PALN 101: V525_PAL60 110: V525_NTSC443 111: V625_SECAM
0	R	0x0	AUTO_DETECT_FINISH

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Chapter 9 Audio

9.1. I2S/PCM

9.1.1. Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format and TDM mode format.

The I2S/PCM controller includes the following features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master/slave mode
- Adjustable interface voltage
- Clock up to 24.576MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Up to 16 channel(fs = 48kHz) which has adjustable width from 8-bit to 32-bit
- Sample rate from 8kHz to 384kHz(CHAN = 2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports loop back mode for test

9.1.2. Block Diagram

The block diagram of I2S/PCM interface is shown as follows.

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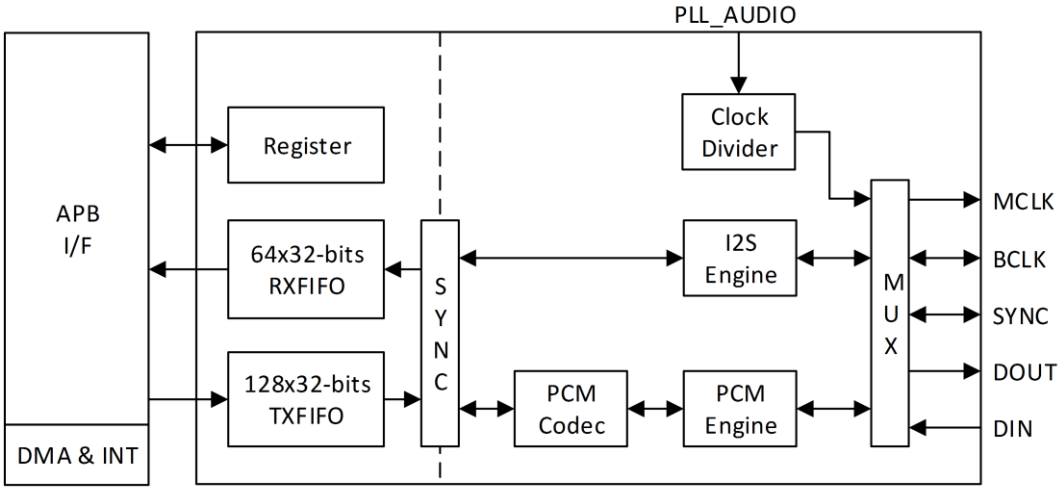

Figure 9- 1. I2S/PCM Interface System Block Diagram

9.1.3. Operations and Functional Descriptions

9.1.3.1. External Signals

Table 9-1 describes the external signals of I2S/PCM interface. SYNC and BCLK are bidirectional I/O, when I2S/PCM interface is configured as Master device, SYNC and BCLK is output pin; when I2S/PCM interface is configured as slave device, SYNC and BCLK is input pin. MCLK is an output pin for external device. DOUT is always the serial data output pin, and DIN is the serial data input pin. For information about General Purpose I/O port, see Port Controller.

Table 9- 1. I2S/PCM External Signals

Signal Name	Description	Type
I2S0_MCLK	I2S0 Master Clock	O
PCM0_BCLK	I2S0/PCM0 Sample Rate Serial Clock	I/O
PCM0_SYNC	I2S0 Sample Rate Left and Right Channel Select Clock/PCM0 Sync	I/O
PCM0_DIN	I2S0/PCM0 Serial Data Input	I
PCM0_DOUT	I2S0/PCM0 Serial Data Output	O
I2S1_MCLK	I2S1 Master Clock	O
PCM1_BCLK	I2S1/PCM1 Sample Rate Serial Clock	I/O
PCM1_SYNC	I2S1 Sample Rate Left and Right Channel Select Clock/PCM1 Sync	I/O
PCM1_DIN	I2S1/PCM1 Serial Data Input	I
PCM1_DOUT	I2S1/PCM1 Serial Data Output	O
I2S2_MCLK	I2S2 Master Clock	O
PCM2_BCLK	I2S2/PCM2 Sample Rate Serial Clock	I/O
PCM2_SYNC	I2S2 Sample Rate Left and Right Channel Select Clock/PCM2 Sync	I/O
PCM2_DIN	I2S2/PCM2 Serial Data Input	I
PCM2_DOUT	I2S2/PCM2 Serial Data Output	O

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9.1.3.2. Clock Sources

Table 9-2 describes the clock sources for I2S/PCM. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 9- 2. I2S/PCM Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

9.1.3.3. Timing Diagram

The I2S/PCM supports standard I2S mode,Left-justified I2S mode,Right-justified I2S mode,PCM mode and TDM mode. Software can select any modes by setting the **I2S/PCM Control Register**.Figure 9-2 to Figure 9-6 describe the waveforms for SYNC,BCLK and DOUT,DIN.

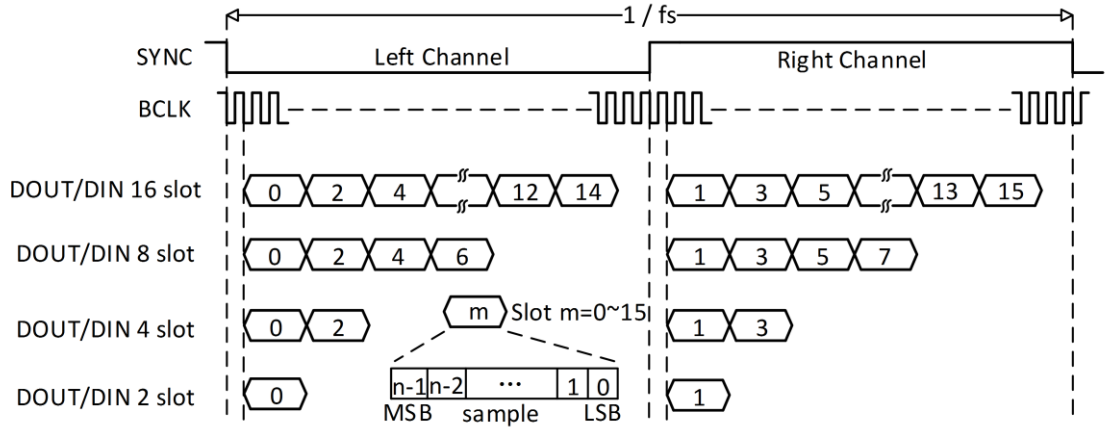

Figure 9- 2. I2S Standard Mode Timing

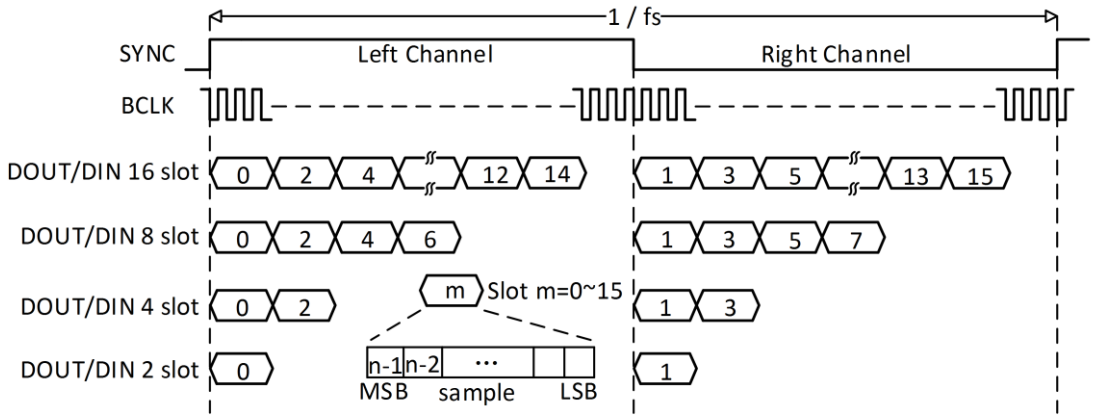

Figure 9- 3. Left-Justified Mode Timing

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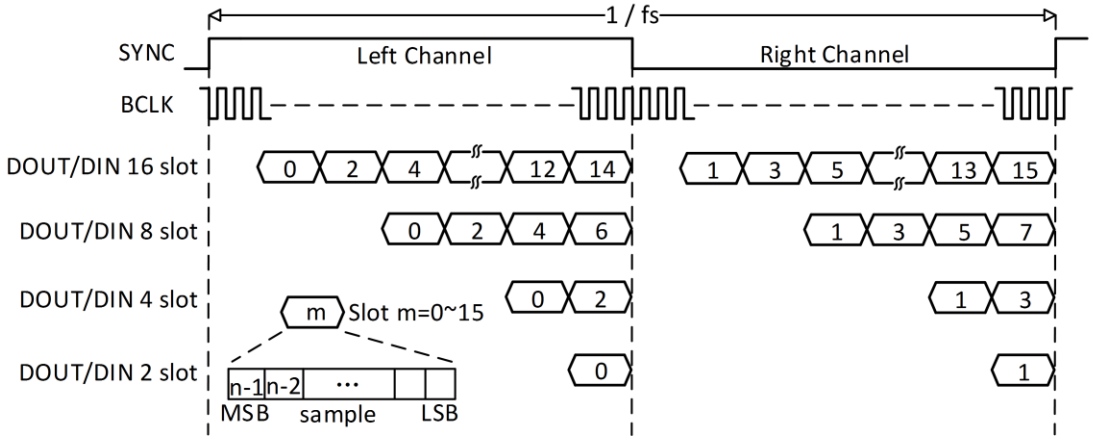

Figure 9- 4. Right-Justified Mode Timing

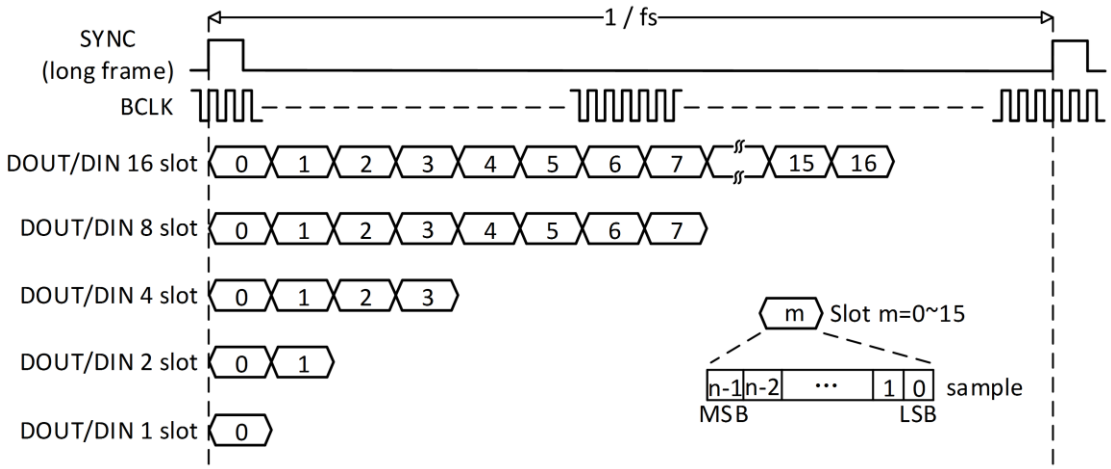

Figure 9- 5. PCM Long Frame Mode Timing

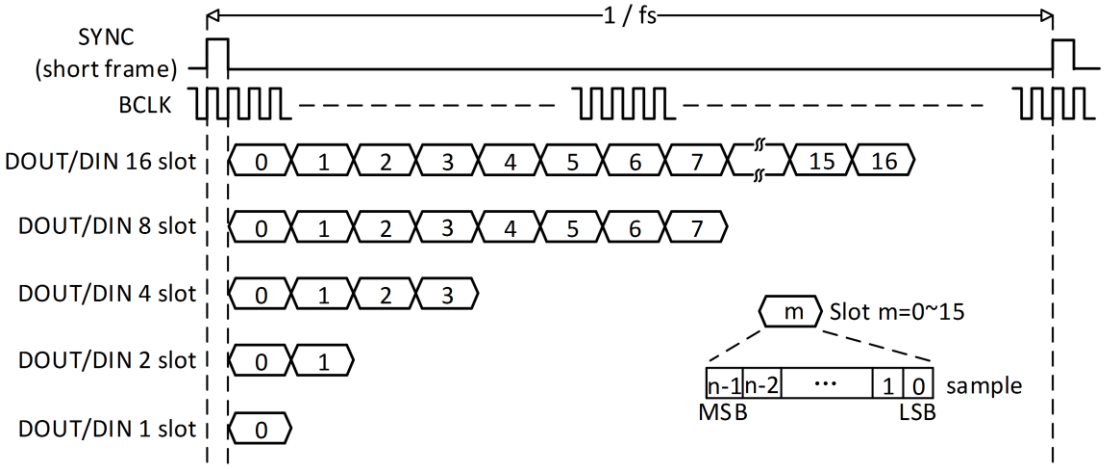

Figure 9- 6. PCM Short Frame Mode Timing

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9.1.3.4. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

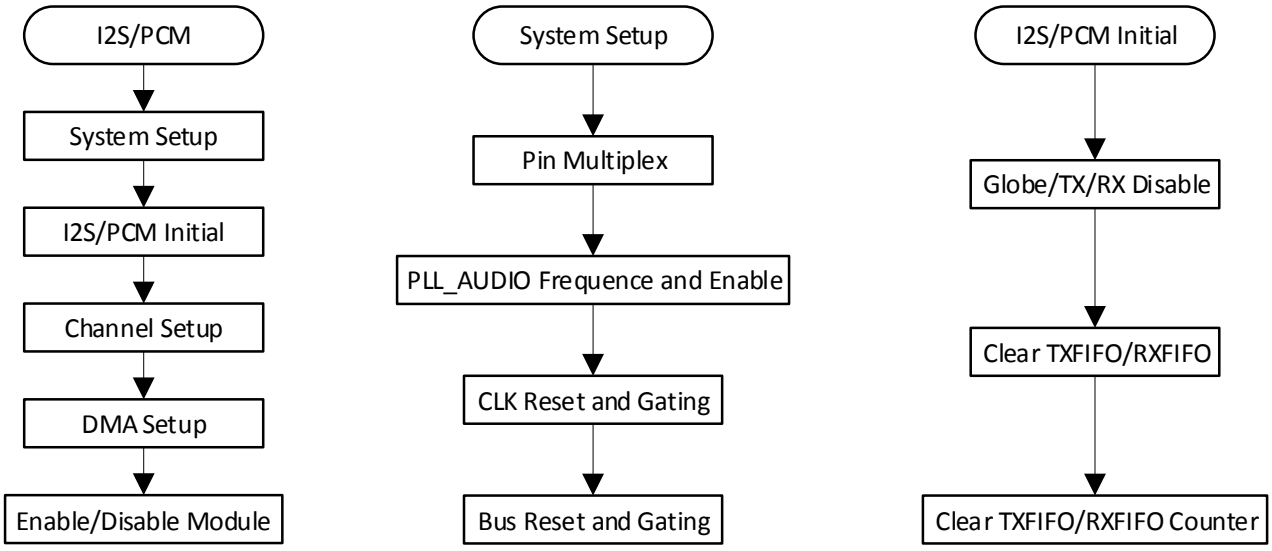

Figure 9- 7. I2S/PCM Operation Flow

(1). System Setup and I2S/PCM Initialization

The clock source for the I2S/PCM should be followed. At first you must disable the PLL_AUDIO through the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. After that, you must open the I2S/PCM gating through the **I2S/PCM_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes to 1. At last, you must reset and open the I2S/PCM bus gating in the **CCU_I2S_BGR_REG**.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the **Globe Enable** bit(I2S/PCM_CTL[0]) , **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit[25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to **I2S/PCM_TXCNT** and **I2S/PCM_RXCNT**.

(2). Channel Setup and DMA Setup

First, you can setup the I2S/PCM of mater and slave. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of slot, the channel slot number and the trigger level and so on. The setup of register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

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(3). Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing **the I2S/PCM_CT**L[2:1]. After that, you must enable I2S/PCM by writing 1 to the **Globe Enable** bit in the I2S/PCM_CTL. Write 0 to the **Globe Enable** bit to disable I2S/PCM.

9.1.4. Programming Guidelines

The following example assumes that the audio channels are stereo channels in I2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits. The recording and playback processes are as follows.

----------GPIO configuration----------

Step1: Ensure that I2S/PCM0 GPIO has power supply.

Step2: Configure GPIOB3/GPIOB4/GPIOB5/GPIOB6/GPIOB7 as Function3.

----------Clock configuration----------

Step1: Configure PLL_AUDIO as 24.576MHz, that is, set **PLL_AUDIO Control Register** to 0xA10D0D00, set **PLL_AUDIO Pattern0 Register** to 0xC000AC02 (If PLL_AUDIO is set as 22.5792MHz,that is, set **PLL_AUDIO Control Register** to 0xA1171500, set **PLL_AUDIO Pattern0 Register** to 0xC001288D).

Step2: Check whether **PLL_AUDIO Control Register**[PLL_AUDIO_LOCK] is 0x1. If is 1, set **I2S/PCM0 Clock Register** to 0x80000000.

Step3: Write 0x1 to the bit16 of **I2S/PCM0 Bus Gating Reset Register** to dessert I2S/PCM0 reset.

Step4: Write 0x1 to the bit0 of **I2S/PCM0 Bus Gating Reset Register** to open I2S/PCM0 gating.

NOTE

Step3 and Step4 is set separately.

----------Initialization I2S/PCM----------

Step1: Set the bit[2:0] of **I2S/PCM Control Register** to 0 to close TXEN,RXEN and GEN.

Step2: Set the bit[25:24] of **I2S/PCM FIFO Control Register** to 0x3 to clear TXFIFO and RXFIFO.

Step3: Set **I2S/PCM TX Counter Register** to 0 to clear TX counter, set **I2S/PCM RX Counter Register** to 0 to clear RX counter.

----------Format configuration----------

Step1: Master/slave configuration. In master mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0x3; in slave mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0.

Step2: Configure the[5:4] of **I2S/PCM Control Register** to 0x1 to set standard I2S mode, configure the bit[21:20] of **I2S/PCM TX Channel Select Register** to 0x1, configure the bit[21:20] of **I2S/PCM RX Channel Select Register** to 0x1.

Step3: Configure the bit[6:4] of **I2S/PCM Format Register0** to 0x3 to set sample resolution, configure the bit[2:0] of **I2S/PCM Format Register0** to 0x3 to set channel width.

Step4: Configure the bit[7:4] of **I2S/PCM Channel Configuration Register** to 0x1 to set RX channel number, configure the bit[3:0] of **I2S/PCM Channel Configuration Register** to 0x1 to set TX channel number. Configure the bit[19:16] of **I2S/PCM TX Channel Select Register** to 0x1, configure the bit[1:0] of **I2S/PCM TX Channel Select**

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Register to 0x3. Configure the bit[19:16] of **I2S/PCM RX Channel Select Register** to 0x1.

Step5: Configure the bit[7:0] of **I2S/PCM TX Channel Mapping Register 1** to 0x10, configure the bit[7:0] of **I2S/PCM RX Channel Mapping Register 1** to 0x10.

----------Clock divider configuration----------

Step1: Set MCLK divider. Configure the bit[3:0] of **I2S/PCM Clock Divide Register** to 0x1, that is, MCLK=24.576MHz. Configure the bit8 of **I2S/PCM Clock Divide Register** to 0x1 to enable MCLK.

Step2: Set BCLK divider. Configure the bit[7:4] of **I2S/PCM Clock Divide Register** to 0xF, that is, BCLK=Sample ratio*Slot_Width*Slot_Num=48K*16*2=1.536MHz.

Step3: Set LRCK divider. Configure the bit[17:8] of **I2S/PCM Format Register** to 0xF, that is, N-1=BCLK/Sample ratio/ Slot_Num =16,N=15.

----------DMA configuration----------

Step1: Set data width of both DMA_SRC and DMA_DEST to 16-bit.

Step2: Set DMA BLOCK SIZE,DMA_SRC BLOCK SIZE and DMA_DEST BLOCK SIZE to 8.

Step3: TX DMA configuration. Set DMA_SRC_DRQ_TYPE to DRAM, set DMA_SRC_ADDR_MODE to Linear Mode, set DMA_DEST_DRQ_TYPE to I2S/PCM0-TX, set DMA_DEST_ADDR_MODE to IO Mode, set DMA_SRC_ADDR to DRAM address of storing data, set DMA_DEST_ADDR to **I2S/PCM TXFIFO**.

Step4: RX DMA configuration. Set DMA_SRC_DRQ_TYPE to I2S/PCM0-RX, set DMA_SRC_ADDR_MODE to IO Mode, set DMA_DEST_DRQ_TYPE to DRAM, set DMA_DEST_ADDR_MODE to Linear Mode, set DMA_SRC_ADDR to **I2S/PCM RXFIFO**, set DMA_DEST_ADDR to DRAM address of storing data.

For more details about DMA, please see to DMA in section 3.9.

NOTE

If data is stored in SRAM, then DRAM is modified to SRAM.

----------Recording/playback/pause----------

Step1: Enable globe, set the bit0 of **I2S/PCM Control Register** to 0x1.

Step2: Recording start: set the bit1 of **I2S/PCM Control Register** to 0x1, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step3: Playback start: set the bit2 of **I2S/PCM Control Register** to 0x1, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step4: Recording pause: set the bit1 of **I2S/PCM Control Register** to 0, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0.

Step5: Playback pause: set the bit2 of **I2S/PCM Control Register** to 0, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0.

9.1.5. Register List

Module Name	Base Address
I2S/PCM0	0x05090000
I2S/PCM1	0x05091000

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I2S/PCM2	0x05092000

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RXFIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TXFIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TXCHCFG	0x0034	I2S/PCM TX Channel Configuration Register
I2S/PCM_TXCHMAP0	0x0044	I2S/PCM TX Channel Mapping Register0
I2S/PCM_TXCHMAP1	0x0048	I2S/PCM TX Channel Mapping Register1
I2S/PCM_RXCHSEL	0x0064	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP0	0x0068	I2S/PCM RX Channel Mapping Register0
I2S/PCM_RXCHMAP1	0x006C	I2S/PCM RX Channel Mapping Register1

9.1.6. Register Description

9.1.6.1. I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16:9	/	/	/
8	R/W	0x0	DOUT_EN 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE

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			0: Normal Transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode (offset 0: Long Frame; offset 1: Short Frame) 01: Left Mode (offset 0: LJ Mode; offset 1: I2S Mode) 10: Right-Justified Mode 11: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When setting to '1' , the bit indicates that the DOUT connects to the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable 0: Disable 1: Enable

9.1.6.2. I2S/PCM Format Register 0(Default Value: 0x0000_0033)

Offset: 0x0004			**Register Name: I2S/PCM_FMT0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH LRCK Width(only apply in PCM mode) 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY In I2S/Left-Justified/Right-Justified mode: 0: Left Channel when LRCK is low 1: Left channel when LRCK is high In PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge

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18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follows: **PCM mode**: Number of BCLKs within (Left + Right) channel width. **I2S/Left-Justified/Right-Justified mode**: Number of BCLKs within each individual channel width (Left or Right) . For example: N = 7: 8 BCLKs width … N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, DOUT drives data at negative edge 1: Invert mode, DOUT drives data at positive edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: DOUT drives data and DIN sample data at the different BCLK edge 1: DOUT drives data and DIN sample data at the same BCLK edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN sample data at positive edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN sample data at positive edge.
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

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9.1.6.3. I2S/PCM Format Register 1(Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

9.1.6.4. I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: TXFIFO underrun pending interrupt Write ‘1’ to clear this interrupt.

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5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No pending interrupt 1: TXFIFO overrun pending interrupt Write '1' to clear this interrupt.
4	R/W1C	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No pending IRQ 1: TXFIFO empty pending interrupt when data in TXFIFO are less than TX trigger level Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: RXFIFO underrun pending interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Write '1' to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ when data in RXFIFO are more than RX trigger level Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

9.1.6.5. I2S/PCM RXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: I2S/PCM_RXFIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

9.1.6.6. I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)

Offset: 0x0014	**Register Name: I2S/PCM_FCTL**

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Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/W1C	0x0	FTX Write '1' to flush TXFIFO, self clear to '0'.
24	R/W1C	0x0	FRX Write '1' to flush RXFIFO, self clear to '0'.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO register 01: Expanding received sample sign bit at MSB of RXFIFO register 10: Truncating received samples at high half-word of RXFIFO register and low half-word of RXFIFO register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO register and high half-word of RXFIFO register is expanded by its sign bit Example for 20-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12'h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

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9.1.6.7. I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO available sample word counter

9.1.6.8. I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When setting to ‘1’, an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable

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			1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When setting to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

9.1.6.9. I2S/PCM TXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written to this register one by one. The left channel sample data is first and then the right channel sample.

9.1.6.10. I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **NOTE** **Whether in slave or master mode, when this bit is set to '1', MCLK should be output.**

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7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

9.1.6.11. I2S/PCM TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is

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			put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

9.1.6.12. I2S/PCM RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

9.1.6.13. I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half cycle of BCLK in the slot 1: Turn to Hi-Z state for the last half cycle of BCLK in the slot
8	R/W	0x0	TX_STATE 0: Transfer level 0 in non-transferring slot 1: Turn to Hi-Z State (TDM) in non-transferring slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot number between CPU/DMA and RXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot number between CPU/DMA and TXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ...

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			1111:16 channels or slots

9.1.6.14. I2S/PCM TX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX_OFFSET TX Offset Tune(TX Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX_CHSEL TX Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX_CHEN TX Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.15. I2S/PCM TX Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX_CH15_MAP TX Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX_CH14_MAP TX Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample

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			1000: 9th Sample ... 1111: 16th sample
23:20	R/W	0x0	TX_CH13_MAP TX Channel 13 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX_CH12_MAP TX Channel 12 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX_CH11_MAP TX Channel 11 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
11:8	R/W	0x0	TX_CH10_MAP TX Channel 10 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX_CH9_MAP TX Channel 9 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX_CH8_MAP TX Channel 8 Mapping

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			0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.16. I2S/PCM TX Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S/PCM_TXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX_CH7_MAP TX Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX_CH6_MAP TX Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	TX_CH5_MAP TX Channel 5 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX_CH4_MAP TX Channel 4 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX_CH3_MAP

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			TX Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	TX_CH2_MAP TX Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX_CH1_MAP TX Channel 1 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX_CH0_MAP TX Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.17. I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S/PCM_RXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX Offset Tune(RX Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0000: 1 channel or slot

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			... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	/	/	/

9.1.6.18. I2S/PCM RX Channel Mapping Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	RX_CH11_MAP

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			RX Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.19. I2S/PCM RX Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

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27:24	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 0000: 1st Sample ... 0111: 8th Sample

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			1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

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9.2. DMIC

9.2.1. Overview

The DMIC controller supports one 8-channels digital microphone interface, the DMIC controller can output 128fs or 64fs (fs= ADC sample rate).

The DMIC controller includes the following features:

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

9.2.2. Block Diagram

Figure 9-8 shows a block diagram of the DMIC.

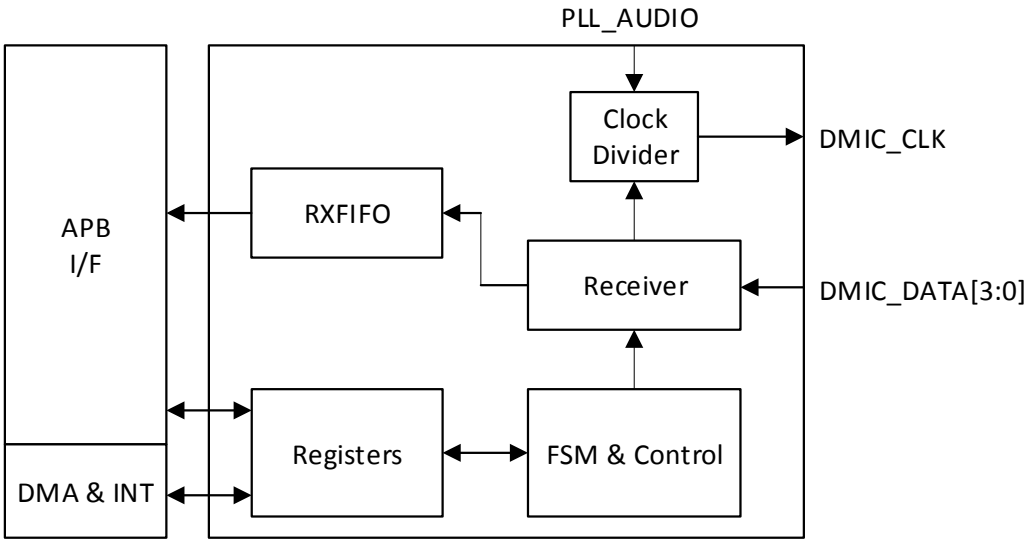

Figure 9- 8. DMIC Block Diagram

9.2.3. Operations and Functional Descriptions

9.2.3.1. External Signals

Table 9-3 describes the external signals of DMIC.

Table 9- 3. DMIC External Signals

Signal	Description	Type

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DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA0	Digital Microphone Data Input	I
DMIC_DATA1	Digital Microphone Data Input	I
DMIC_DATA2	Digital Microphone Data Input	I
DMIC_DATA3	Digital Microphone Data Input	I

9.2.3.2. Clock Sources

Table 9-4 describes the clock source for DMIC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 9- 4. DMIC Clock Sources

Clock Sources	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency.

9.2.3.3. Operation Mode

The software operation of the DMIC is divided into five steps: system setup, DMIC initialization, channel setup, DMA setup and Enable/Disable module. Five steps are described in detail in the following sections.

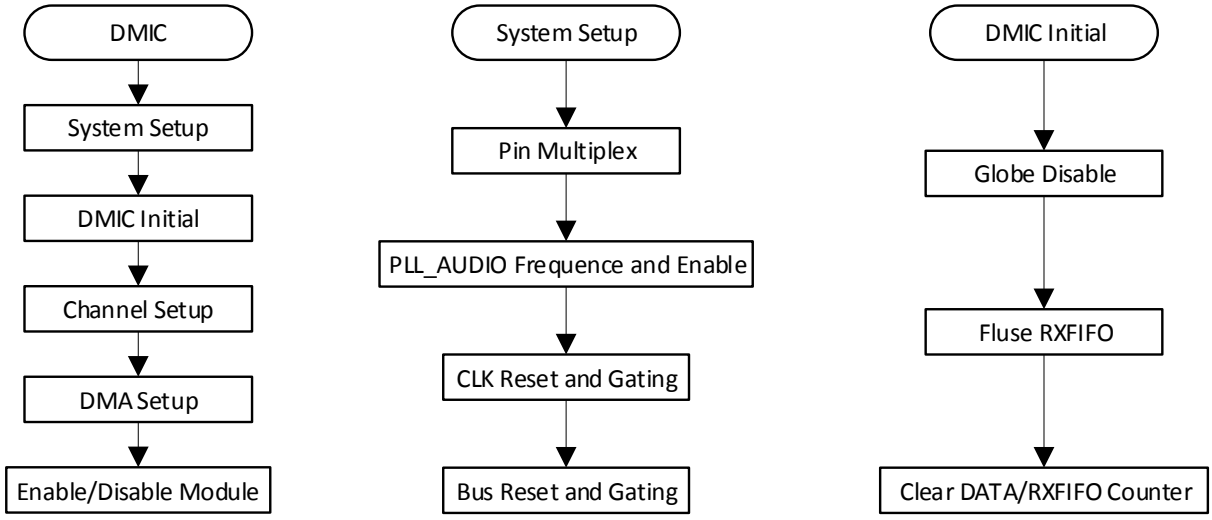

Figure 9- 9. DMIC Operation Mode

9.2.3.3.1. System Setup and DMIC Initialization

The first step in the system setup is properly programming the GPIO. Because the DMIC port is a multiplex pin. You can find the function in the pin multiplex specification.

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The clock source for the DMIC should be followed. At first you must disable the PLL_AUDIO through the PLL_ENABLE bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. Then enable PLL_AUDIO. After that, you must open the DMIC gating through the **DMIC_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes 1. At last, you must reset and open the DMIC bus gating in the **CCU_DMIC_BGR_REG**.

After the system setup, the register of DMIC can be setup. At first, you should initialize the DMIC. You should close the **globe enable bit**(DMIC_EN[8]) , **data channel enable bit**(DMIC_EN[7:0]) by writing 0 to it. After that, you must flush the RXFIFO by writing 1 to register **DMIC_RXFIFO_CTR**[31]. At last, you can clear the Data/RXFIFO counter by writing 1 to **DMIC_RXFIFO_STA,DMIC_CNT**.

9.2.3.3.2. Channel Setup and DMA Setup

You can set up the sample rate, the sample resolution, the over sample rate, the channel number, the RXFIFO output mode and the RXFIFO trigger level and so on. The setup of register can be found in the specification.

The DMIC supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the DMA specification. In this module, you just enable the DRQ.

9.2.3.3.3. Enable and Disable DMIC

To enable the function, you can enable **data channel enable** (DMIC_EN[7:0]) by writing 1 to it. After that, you must enable DMIC by writing 1 to the **Globe Enable** (DMIC_EN[8]). Write 0 to **Globe Enable** to disable DMIC.

9.2.4. Register List

Module Name	Base Address
DMIC	0x05095000

Register Name	Offset	Description
DMIC_EN	0x0000	DMIC Enable Control Register
DMIC_SR	0x0004	DMIC Sample Rate Register
DMIC_CTR	0x0008	DMIC Control Register
DMIC_ DATA	0x0010	DMIC Data Register
DMIC_INTC	0x0014	MIC Interrupt Control Register
DMIC_INTS	0x0018	DMIC Interrupt Status Register
DMIC_RXFIFO_CTR	0x001C	DMIC RXFIFO Control Register
DMIC_RXFIFO_STA	0x0020	DMIC RXFIFO Status Register
DMIC_CH_NUM	0x0024	DMIC Channel Numbers Register
DMIC_CH_MAP	0x0028	DMIC Channel Mapping Register

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DMIC_CNT	0x002C	DMIC Counter Register
DATA0_DATA1_VOL_CTR	0x0030	Data0 and Data1 Volume Control Register
DATA2_DATA3_VOL_CTR	0x0034	Data2 And Data3 Volume Control Register
HPF_EN_CTR	0x0038	High Pass Filter Enable Control Register
HPF_COEF_REG	0x003C	High Pass Filter Coef Register
HPF_GAIN_REG	0x0040	High Pass Filter Gain Register

9.2.5. Register Description

9.2.5.1. DMIC Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: DMIC_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	GLOBE_EN DMIC Globe Enable 0: Disable 1: Enable
7	R/W	0x0	DATA3_CHR_EN DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	DATA3_CHL_EN DATA3 Left Channel Enable 0: Disable 1: Enable
5	R/W	0x0	DATA2_CHR_EN DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	DATA2_CHL_EN DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	DATA1_CHR_EN DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	DATA1_CHL_EN DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	DATA0_CHR_EN

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			DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	DATA0_CHL_EN DATA0 Left Channel Enable 0: Disable 1: Enable

9.2.5.2. DMIC Sample Rate Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMIC_SR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	DMIC_SR Sample Rate of DMIC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit.

9.2.5.3. DMIC Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DMIC_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:9	R/W	0x0	DMICFDT DMIC RXFIFO Delay Time for Writing Data after GLOBE_EN 00: 5ms 01: 10ms 10: 20ms 11: 30ms
8	R/W	0x0	DMICDFEN DMIC RXFIFO Delay Function for Writing Data after GLOBE_EN 0: Disable 1: Enable
7	R/W	0x0	DATA3 Left Data and Right Data Swap Enable 0: Disable 1: Enable

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6	R/W	0x0	DATA2 Left Data and Right Data Swap Enable 0: Disable 1: Enable
5	R/W	0x0	DATA1 Left Data and Right Data Swap Enable 0: Disable 1: Enable
4	R/W	0x0	DATA0 Left Data and Right Data Swap Enable 0: Disable 1: Enable
3:1	/	/	/
0	R/W	0x0	DMIC Oversample Rate 0: 128 (Support 8 kHz ~ 24 kHz) 1: 64 (Support 16 kHz ~ 48 kHz)

9.2.5.4. DMIC DATA Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMIC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMIC_DATA

9.2.5.5. DMIC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DMIC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	RXFIFO_DRQ_EN DMIC RXFIFO Data Available DRQ Enable 0: Disable 1: Enable
1	R/W	0x0	RXFIFO_OVERRUN_IRQ_EN DMIC RXFIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	DATA_IRQ_EN DMIC RXFIFO Data Available IRQ Enable 0: Disable 1: Enable

9.2.5.6. DMIC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0018	Register Name: DMIC_INTS

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Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W1C	0x0	RXFIFO_OVERRUN_IRQ_PENDING DMIC RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/ W1C	0x0	RXFIFO_DATA_IRQ_PENDING DMIC RXFIFO Data Available Pending Interrupt 0: No pending IRQ 1: Data available pending IRQ Writing '1' to clear this interrupt or automatically clear if interrupt condition fails.

9.2.5.7. DMIC RXFIFO Control Register (Default Value: 0x0000_0040)

Offset: 0x001C			Register Name: DMIC_FIFO_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	DMIC_RXFIFO_FLUSH DMIC RXFIFO Flush Writing '1' to flush RXFIFO, self clear to '0'
30:10	/	/	/
9	R/W	0x0	RXFIFO_MODE RXFIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of RXFIFO register 1: Expanding received sample sign bit at MSB of RXFIFO register For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {RXFIFO_O[23:0], 8'h0} Mode 1: RXDATA[31:0] = {8{RXFIFO_O[23]}, RXFIFO_O[23:0]} For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {RXFIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{RXFIFO_O[23]}, RXFIFO_O[23:8]}
8	R/W	0x0	Sample_Resolution 0: 16-bit 1: 24- bit
7:0	R/W	0x40	RXFIFO_TRG_LEVEL RXFIFO Trigger Level (TRLV[7:0]) Interrupt and DMA request trigger level for DMIC RXFIFO normal condition IRQ/DRQ Generated when WLEVEL > TRLV[7:0]) WLEVEL represents the number of valid samples in the DMIC RXFIFO

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9.2.5.8. DMIC RXFIFO Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DMIC_RXFIFO_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DMIC_DATA_CNT DMIC RXFIFO Available Sample Word Counter

9.2.5.9. DMIC Channel Numbers Register (Default Value: 0x0000_0001)

Offset: 0x0024			Register Name: DMIC_CH_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x1	DMIC_CH_NUM DMIC enable channel numbers are (N+1).

9.2.5.10. DMIC Channel Mapping Register (Default Value: 0x7654_3210)

Offset: 0x0028			Register Name: DMIC_CH_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	DMIC_CH7_MAP DMIC Channel 7 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
27:24	R/W	0x6	DMIC_CH6_MAP DMIC Channel 6 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
23:20	R/W	0x5	DMIC_CH5_MAP DMIC Channel 5 Mapping 0000: DATA0 Left Channel

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			0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
19:16	R/W	0x4	DMIC_CH4_MAP DMIC Channel 4 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
15:12	R/W	0x3	DMIC_CH3_MAP DMIC Channel 3 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
11:8	R/W	0x2	DMIC_CH2_MAP DMIC Channel 2 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel
7:4	R/W	0x1	DMIC_CH1_MAP DMIC Channel 1 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel

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			0110: DATA3 Left Channel 0111: DATA3 Right Channel
3:0	R/W	0x0	DMIC_CH0_MAP DMIC Channel0 Mapping 0000: DATA0 Left Channel 0001: DATA0 Right Channel 0010: DATA1 Left Channel 0011: DATA1 Right Channel 0100: DATA2 Left Channel 0101: DATA2 Right Channel 0110: DATA3 Left Channel 0111: DATA3 Right Channel

9.2.5.11. DMIC Counter Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: DMIC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMIC_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **NOTE** **It is used for Audio/ Video Synchronization.**

9.2.5.12. DATA0 and DATA1 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0030			Register Name: DATA0_DATA1_VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA1L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
23:16	R/W	0xA0	DATA1R_VOL

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			(-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA0L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA0R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB

9.2.5.13. DATA2 and DATA3 Volume Control Register (Default Value: 0xA0A0_A0A0)

Offset: 0x0034			Register Name: DATA2_DATA3_VOL_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	DATA3L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB

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23:16	R/W	0xA0	DATA3R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
15:8	R/W	0xA0	DATA2L_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB ……. 0xFF: 71.25 dB
7:0	R/W	0xA0	DATA2R_VOL (-119.25 dB to 71.25 dB, 0.75 dB/Step) 0x00: Mute 0x01: -119.25 dB …….. 0x9F: -0.75 dB 0xA0: 0 dB 0xA1: 0.75 dB …….. 0xFF: 71.25 dB

9.2.5.14. High Pass Filter Enable Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: HPF_EN_CTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	HPF_DATA3_CHR_EN High Pass Filter DATA3 Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	HPF_DATA3_CHL_EN High Pass Filter DATA3 Left Channel Enable 0: Disable 1: Enable

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5	R/W	0x0	HPF_DATA2_CHR_EN High Pass Filter DATA2 Right Channel Enable 0: Disable 1: Enable
4	R/W	0x0	HPF_DATA2_CHL_EN High Pass Filter DATA2 Left Channel Enable 0: Disable 1: Enable
3	R/W	0x0	HPF_DATA1_CHR_EN High Pass Filter DATA1 Right Channel Enable 0: Disable 1: Enable
2	R/W	0x0	HPF_DATA1_CHL_EN High Pass Filter DATA1 Left Channel Enable 0: Disable 1: Enable
1	R/W	0x0	HPF_DATA0_CHR_EN High Pass Filter DATA0 Right Channel Enable 0: Disable 1: Enable
0	R/W	0x0	HPF_DATA0_CHL_EN High Pass Filter DATA0 Left Channel Enable 0: Disable 1: Enable

9.2.5.15. High Pass Filter Coef Register (Default Value: 0x00FF_AA45)

Offset: 0x003C			**Register Name: HPF_COEF_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFAA45	High Pass Filter Coefficient

9.2.5.16. High Pass Filter Gain Register (Default Value: 0x00FF_D522)

Offset: 0x0040			**Register Name: HPF_GAIN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x00FFD522	High Pass Filter Gain

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9.3. OWA

9.3.1. Overview

The OWA(One Wire Audio) provides a serial bus interface for audio data between system. This interface is widely used for consumer audio.

Features:

- IEC-60958 transmitter and receiver functionality
- Compliance with S/PDIF Interface
- Supports channel status insertion for the transmitter
- Supports channel status capture for the receiver
- Hardware parity generation on the transmitter
- Hardware parity checking on the receiver
- One 128×24bits TXFIFO and 64x24bits RXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit,20-bit,24-bit data formats

9.3.2. Block Diagram

The OWA block diagram is shown as follows.

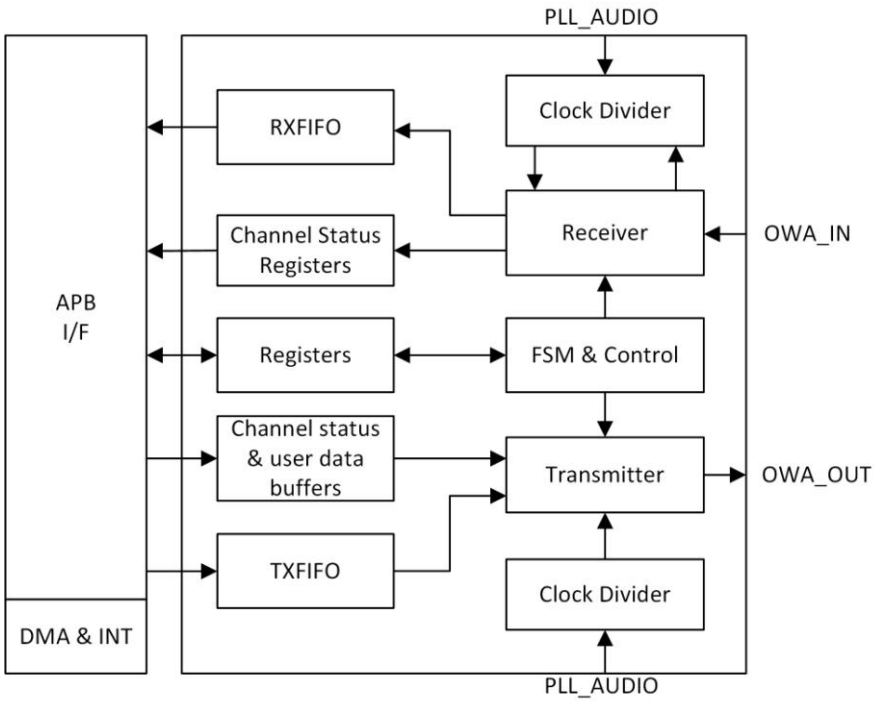

Figure 9- 10. OWA Block Diagram

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9.3.3. Operations and Functional Descriptions

9.3.3.1. External Signals

OWA is a Biphase-Mark Encoding Digital Audio Transfer protocol. In this protocol, the CLK signal and data signals is transfer in the same line. Table 9-5 describes the external signals of OWA. OWA_DOUT is output pin for output CLK and DATA, and OWA_DIN is input pin for input CLK and DATA.

Table 9- 5. OWA External Signals

Signal Name	Description	Type
OWA_OUT	OWA output	O
OWA_IN	OWA input	I

9.3.3.2. Clock Sources

Table 9-6 describes the clock sources for OWA. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 9- 6. OWA Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz serial frequency

9.3.3.3. Biphase-Mark Code (BMC)

In OWA format, the digital signal is coded using the biphase-mark code (BMC). The clock, frame, and data are embedded in only one signal—the data pin. In the BMC system, each data bit is encoded into two logical states (00, 01, 10, or 11) at the pin.Figure 9-11 and Table 9-7 show how data is encoded to the BMC format.

As shown in Figure 9-11, the frequency of the clock is twice the data bit rate. In addition, the clock is always programmed to 128xfs, where fs is the sample rate. The device receiving in OWA format can recover the clock and frame information from the BMC signal.

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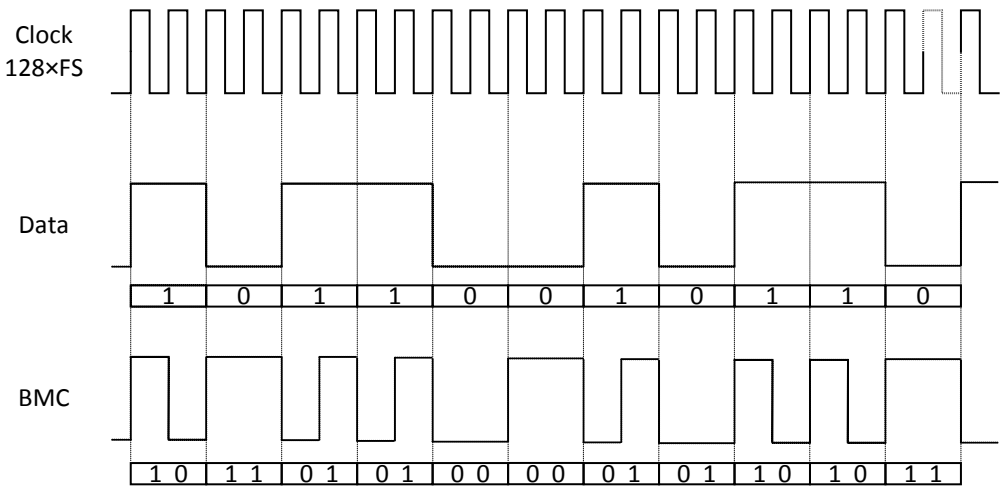

Figure 9- 11. OWA Biphase-Mark Code

Table 9- 7. Biphase-Mark Encoder

Data	Previous State	BMC
0	0	11
0	1	00
1	0	10
1	1	01

9.3.3.4. OWA Transmit Format

The OWA supports digital audio data transfer out and receive in. And it supports full-duplex synchronous work mode. Software can set the work mode by the OWA Control Register.

Every audio sample transmitted in a subframe consists 32-bit, numbered from 0 to 31. Figure 9-12 shows a subframe.The OWA supports the transfer of digital audio data. And it supports full-duplex synchronous work mode.

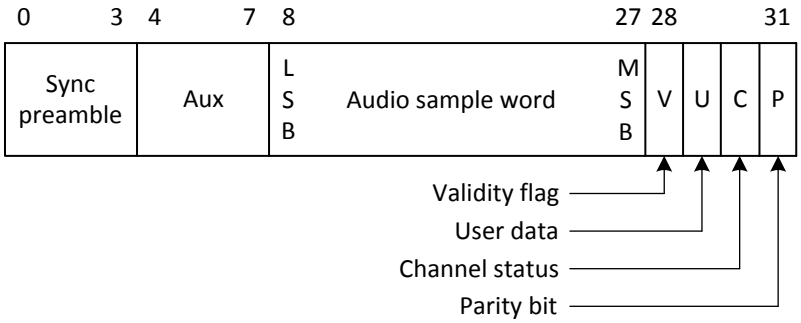

Figure 9- 12. OWA Sub-Frame Format

Bit 0-3 carry one of the four permitted preambles to signify the type of audio sample in the current subframe. The preamble is not encoded in BMC format, and therefore the preamble code can contain more than two consecutive 0

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or 1 logical states in a row. See Table 9-8.

Bit 4-27 carry the audio sample word in linear 2s-complement representation. The most-significant bit (MSB) is carried by bit 27. When a 24-bit coding range is used, the least-significant bit (LSB) is in bit 4. When a 20-bit coding range is used, bit 8-27 carry the audio sample word with the LSB in bit 8. Bit 4-7 may be used for other applications and are designated auxiliary sample bits.

If the source provides fewer bits than the interface allows (either 20 or 24), the unused LSBs are set to logical 0. For a nonlinear PCM audio application or a data application, the main data field may carry any other information.

Bit 28 carries the validity bit (V) associated with the main data field in the subframe.

Bit 29 carries the user data channel (U) associated with the main data field in the subframe.

Bit 30 carries the channel status information (C) associated with the main data field in the subframe. The channel status indicates if the data in the subframe is digital audio or some other type of data.

Bit 31 carries a parity bit (P) such that bit 4-31 carry an even number of 1s and an even number of 0s (even parity). As shown in Table 9-8, the preambles (bit 0-3) are also defined with even parity.

Table 9- 8. Preamble Codes

Preamble Code	Previous Logical State	Logical State	Description
B(or Z)	0	1110 1000	Start of a block and subframe 1
M(or X)	0	1110 0010	Subframe 1
W(or Y)	0	1110 0100	Subframe 2

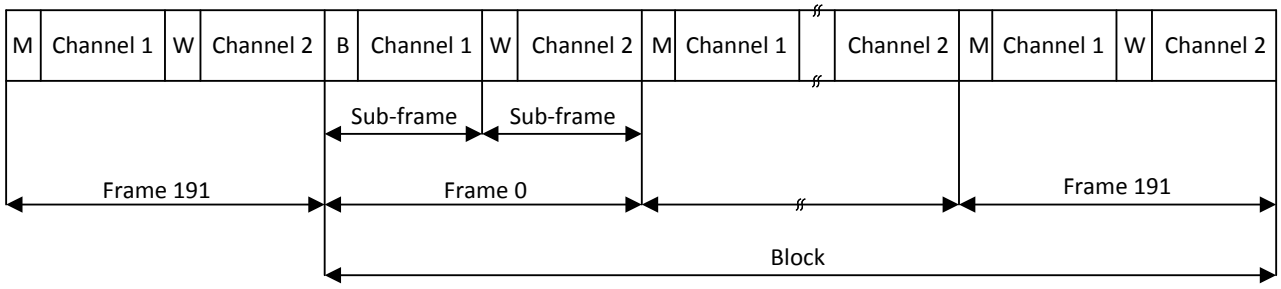

Figure 9- 13. OWA Frame/Block Format

9.3.3.5. Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, channel setup, DMA setup and enable/disable module. These five steps are described in detail in the following sections.

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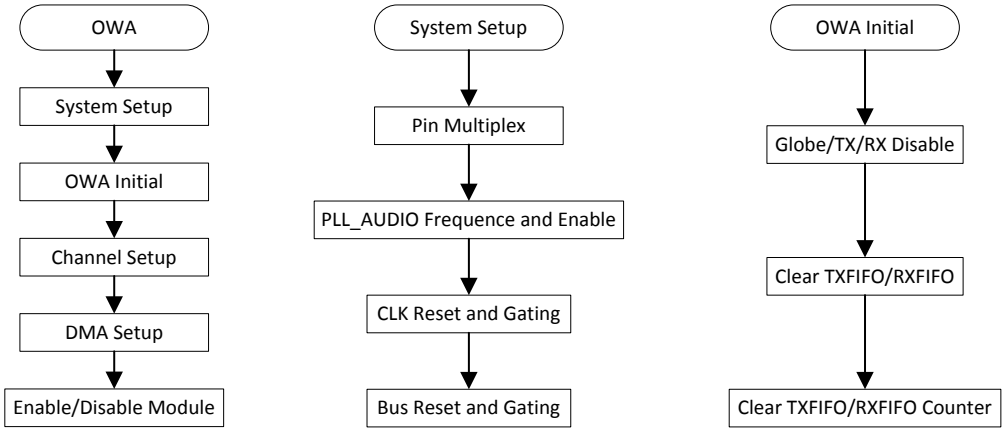

Figure 9- 14. OWA Operation Flow

(1) System Setup and OWA Initialization

The first step in the OWA initialization is properly programming the GPIO. Because the OWA port is a multiplex pin. You can find the function in the **Port Controller**.

The clock source for the OWA should be followed. At first you must reset the audio PLL in the **CCU**. The second step, you must setup the frequency of the Audio PLL. After that, you must open the OWA gating. At last, you must open the OWA bus gating.

After the system setup, the register of OWA can be setup. At first, you should reset the OWA by writing 1 to **OWA_CTL**[0] and clear the TX/RX FIFO by writing 1 to **OWA_FCTL**[17:16]. After that you should enable the globe enable bit by writing 1 to **OWA_CTL**[1] and clear the interrupt and TX/RX counter by the **OWA_ISTA** and **OWA_TX_CNT**/**OWA_RX_CNT**.

(2) Channel Setup and DMA Setup

The OWA supports three methods to transfer the data. The most common way is DMA, the configuration of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3) Enable and Disable OWA

To enable the function, you can enable TX/RX by writing the **OWA_TX_CFIG**[31]/**OWA_RX_CFIG**[0]. After that, you must enable OWA by writing 1to the **GEN** bit in the **OWA_CTL** register. Writing 0 to the **GEN** bit to disable process.

9.3.4. Register List

Module Name	Base Address
OWA	0x05093000

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Register Name	Offset	Description
OWA_GEN_CTL	0x0000	OWA General Control Register
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_RX_CFIG	0x0008	OWA RX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_RXFIFO	0x0010	OWA RXFIFO Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_RX_CNT	0x0028	OWA RX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1
OWA_RXCHSTA0	0x0034	OWA RX Channel Status Register0
OWA_RXCHSTA1	0x0038	OWA RX Channel Status Register1

9.3.5. Register Description

9.3.5.1. OWA General Control Register (Default Value: 0x0000_0080)

Offset: 0x0000			Register Name: OWA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:5	R/W	0x4	Reserved
4	/	/	/
3	R/W	0x0	Reserved
2	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When setting to '1', DOUT and DIN need be connected.
1	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
0	R/W	0x0	RST Reset 0: Normal 1: Reset

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			Self clear to 0.

9.3.5.2. OWA TX Configure Register (Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_SINGLE_MODE Tx Single Channel Mode 0: Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	ASS Audio Sample Select with TX FIFO Underrun when 0: Sending 0 1: Sending the last audio **NOTE** **This bit is only valid in PCM mode.**
16	R/W	0x0	TX_AUDIO TX Data Type 0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio(Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX Clock Divide Ratio Clock divide ratio = TX_TATIO +1 Fs= PLL_AUDIO/[(TX_TATIO +1)*64*2]
3:2	R/W	0x0	TX_SF TX Sample Format 00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A&B set to 0 1: Channel status A&B generated form TX_CHSTA
0	R/W	0x0	TXEN 0: Disabled 1: Enabled

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9.3.5.3. OWA RX Configure Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: OWA_RX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RX_LOCK_FLAG 0: Unlock 1: Lock
3	R/W	0x0	RX_CHST_SRC 0: RX_CH_STA Register Holds Status from Channel A 1: RX_CH_STA Register Holds Status from Channel B
2	/	/	/
1	R/W	0x0	CHST_CP Channel Status Capture 0: Idle or Capture End 1: Capture Channel Status Start When setting to '1', the channel status information is capturing, the bit will clear to '0' after captured.
0	R/W	0x0	RXEN 0: Disabled 1: Enabled

9.3.5.4. OWA Interrupt Status Register (Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	RX_LOCK_INT 0: No Pending IRQ 1: RX Lock Pending Interrupt (RX_LOCK_FLAG 0→1) Write '1' to clear this interrupt.
17	R/W1C	0x0	RX_UNLOCK_INT RX Unlock Pending Interrupt 0: No Pending IRQ 1: RX Unlock Pending Interrupt (RX_LOCK_FLAG 1→0) Write '1' to clear this interrupt.
16	R/W1C	0x0	RX_PARERRI_INT RX Parity Error Pending Interrupt 0: No Pending IRQ 1: RX Parity Error Pending Interrupt Write '1' to clear this interrupt.
15:7	/	/	/
6	R/W1C	0x0	TXU_INT

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			TX FIFO Underrun Pending Interrupt 0: No Pending IRQ 1: FIFO Underrun Pending Interrupt Writing “1” to clear this interrupt.
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Writing “1” to clear this interrupt.
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Writing “1” to clear this interrupt or automatically clear if the interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: RXFIFO Overrun Pending Write ‘1’ to clear this interrupt.
0	R/W1C	0x0	RXA_INT RXFIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.

9.3.5.5. OWA RX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: OWA_RXFIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA Host can get one sample by reading this register, the A channel data is first and then the B channel data.

9.3.5.6. OWA FIFO Control Register (Default Value: 0x0004_0200)

Offset: 0x0014			**Register Name: OWA_FCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable

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30	R/W1C	0x0	FTX Write ‘1’ to flush TXFIFO, self clear to ‘0’.
29	R/W1C	0x0	FRX Write ‘1’ to flush RXFIFO, self clear to ‘0’.
28:20	/	/	/
19:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition. Trigger Level = TXTL
11	/	/	/
10:4	R/W	0x20	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of TXFIFO Register 1: Valid data at the LSB of TXFIFO Register Example for 20-bit transmitted audio sample: Mode 0: TXFIFO[23:0] = {APB_WDATA[31:12], 4’h0} Mode 1: TXFIFO[23:0] = {APB_WDATA[19:0], 4’h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode(Mode 0,1,2,3) 00: Expanding ‘0’ at LSB of RXFIFO Register 01: Expanding received sample sign bit at MSB of RXFIFO Register 10: Truncating received samples at high half-word of RXFIFO Register and low half-word of RXFIFO Register is filled by ‘0’ 11: Truncating received samples at low half-word of RXFIFO Register and high half-word of RXFIFO Register is expanded by its sigh bit Mode 0: APB_RDATA[31:0] = {RXFIFO[23:0], 8’h0} Mode 1: APB_RDATA[31:0] = {8’RXFIFO[23], RXFIFO[23:0]} Mode 2: APB_RDATA[31:0] = {RXFIFO[23:8], 16’h0} Mode 3: APB_RDATA[31:0] ={16’RXFIFO[23], RXFIFO[23:8]}

9.3.5.7. OWA FIFO Status Register (Default Value: 0x8080_0000)

Offset: 0x0018			**Register Name: OWA_FSTA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x1	TXE TXFIFO Empty (indicate TXFIFO is not full) 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>=1 Word)
30:24	/	/	/

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23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>=1 Word)
14:7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO Available Sample Word Counter

9.3.5.8. OWA Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	RX_LOCKI_EN RX LOCK Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	RX_UNLOCKI_EN RX UNLOCK Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	RX_PARERRI_EN RX PARITY ERORR Interrupt Enable 0: Disable 1: Enable
15:8	/	/	/
7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable

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			1: Enable
3	/	/	/
2	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable When setting to '1', RXFIFO DMA Request is asserted if data is available in RXFIFO. 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

9.3.5.9. OWA TX FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. The A channel data is first and then the B channel data.

9.3.5.10. OWA TX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After updated by the initial value, the counter register should count on base of this initial value.

9.3.5.11. OWA RX Counter Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: OWA_RX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

9.3.5.12. OWA TX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1kHz 0001: Not indicated 0010: 48kHz 0011: 32kHz 0100: 22.05kHz 0101: Reserved 0110: 24kHz 0111: Reserved 1000: Reserved 1001: 768kHz 1010: 96kHz 1011: Reserved 1100: 176.4kHz 1101: Reserved 1110: 192kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the kind of equipment that generates the digital audio interface

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			signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = “0”, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 µs / 15 µs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = “1”, other than Linear PCM applications: 000: Default state 001~111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application This bit must be fixed to “0”.

9.3.5.13. OWA TX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency

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			0000: Not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = “0”: 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

9.3.5.14. OWA RX Channel Status Register0 (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: OWA_RX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not Matched
27:24	R/W	0x0	FREQ Sampling Frequency 0000: 44.1kHz 0001: Not Indicated 0010: 48kHz 0011: 32kHz 0100: 22.05kHz 0101: Reserved 0110: 24kHz 0111: Reserved 1000: Reserved 1001: 768kHz 1010: 96kHz 1011: Reserved 1100:176.4kHz 1101: Reserved 1110: 192kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category Code Indicates the Kind of Equipment that Generates the digital audio interface Signal.
7:6	R/W	0x0	MODE Mode 00: Default mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional Format Information For bit 1 = ‘0’, Linear PCM Audio mode: 000: 2 Audio channels without pre-emphasis 001: 2 Audio channels with 50 μs/15 μs pre-emphasis 010: Reserved (For 2 Audio channels with pre-emphasis) 011: Reserved (For 2 Audio channels with pre-emphasis)

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			100~111: Reserved For bit 1 = '1', Other than Linear PCM applications: 000: Default state 001~111: Reserved
2	R/W	0x0	CP Copyright 0: Copyright is asserted 1: No Copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM samples 1: Non-linear PCM audio
0	R/W	0x0	PRO Application Type 0: Consumer application 1: Professional application

9.3.5.15. OWA RX Channel Status Register1 (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: OWA_RX_CHSTA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition is not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original Sampling Frequency 0000: Not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz

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			1110: Reserved 1111: 44.1kHz
3:1	R/W	0x0	WL Sample Word Length For bit 0 = '0': 000: Not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = '1': 000: Not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word Length 0: Maximum Audio sample word length is 20 bits 1: Maximum Audio sample word length is 24 bits

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9.4. Audio Codec

9.4.1. Overview

The Audio Codec has 2 I2S/PCM interfaces, 2 channels DAC and 3 channels ADC with a high level of mixed-signal integration which ideal for smart phone and other portable devices.The DRC with integrated hardware DAP engine can be used in record and playback paths .

The Audio Codec has the following features:

- Two audio digital-to-analog(DAC) channels
  - Supports 8 kHz to 192 kHz sample rate
  - SNR: 100dB ± 2dB
  - Supports 16-bit and 24-bit audio sample resolution
- Two audio outputs
  - One stereo line-out output(LINEOUTL and LINEOUTR)
  - One differential phone-out output(PHONEOUTP and PHONEOUTN)
- Three audio analog-to-digital(ADC) channels
  - Supports 8 kHz to 48 kHz sample rate
  - SNR: 92dB ± 2dB
  - Supports 16-bit and 24-bit audio sample resolution
- Four audio inputs
  - Three differential microphone inputs(MICIN1P and MICIN1N,MICIN2P and MICIN2N, MICIN3P and MICIN3N)
  - One stereo line-in input(LINEINL and LINEINR)
- Supports Dynamic Range Controller(DRC) adjusting the ADC recording and DAC playback
- One low-noise analog microphone bias output
- Analog low-power loop from line-in/microphone inputs to line-out/phone-out outputs
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA support

9.4.2. Block Diagram

Figure 9-15 shows the block diagram of Audio Codec.

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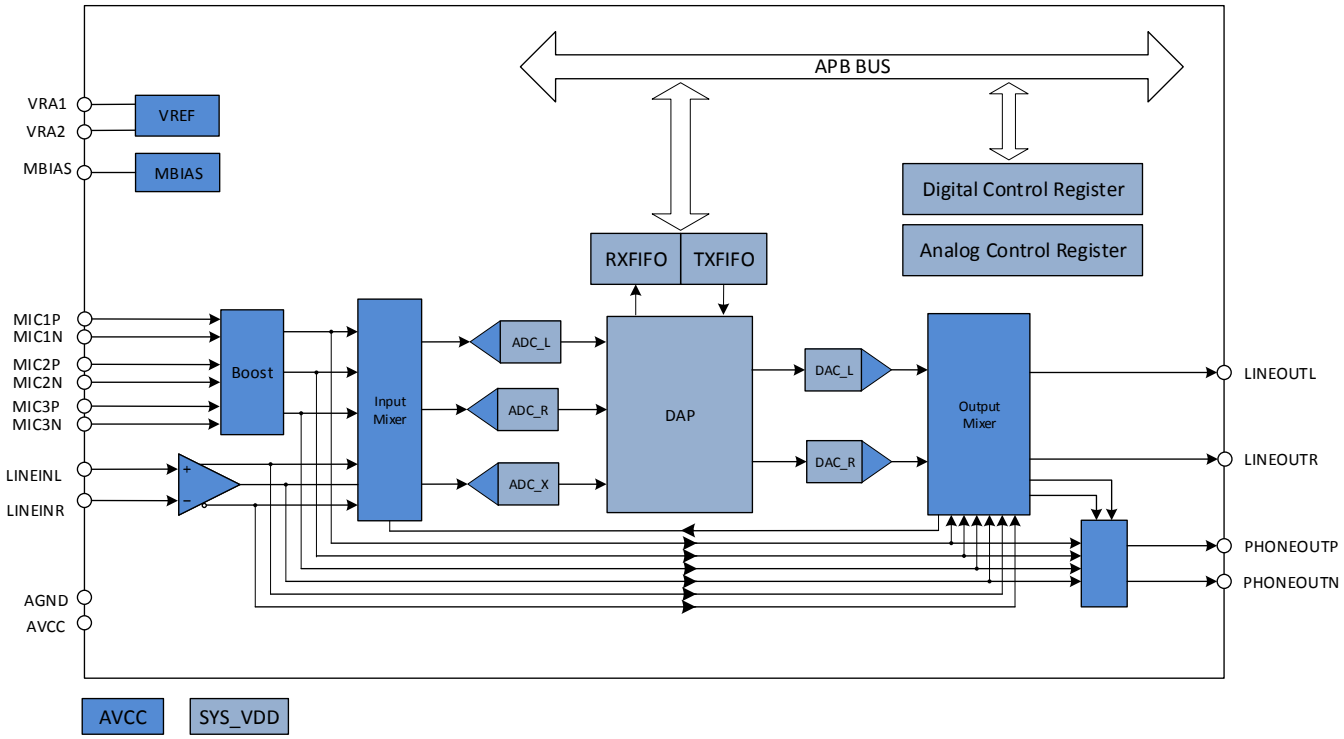

Figure 9- 15. Audio Codec Block Diagram

9.4.3. Operations and Functional Descriptions

9.4.3.1. External Signals

9.4.3.1.1. Analog I/O Pins

Signal	Type	Description
MICIN1P	AI	Positive differential input for MIC1
MICIN1N	AI	Negative differential input for MIC1
MICIN2P	AI	Positive differential input for MIC2
MICIN2N	AI	Negative differential input for MIC2
MICIN3P	AI	Positive differential input for MIC3
MICIN3N	AI	Negative differential input for MIC3
LINEINL	AI	Left single-ended input for LINEIN
LINEINR	AI	Right single-ended input for LINEIN
LINEOUTL	AO	Left single-ended output for LINEOUT
LINEOUTR	AO	Right single-ended output for LINEOUT
PHONEOUTP	AO	Positive differential output for PHONEOUT
PHONEOUTN	AO	Negative differential output for PHONEOUT

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9.4.3.1.2. Reference

Signal	Type	Description
MBIAS	AO	First bias voltage output for main microphone
VRA1	AO	Internal reference voltage
VRA2	AO	Internal reference voltage
VRP	AO	Internal reference voltage

9.4.3.1.3. Power/Ground

Signal	Type	Description
AVCC	P	Analog power
AGND	G	Analog ground

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9.4.3.2. Clock Sources

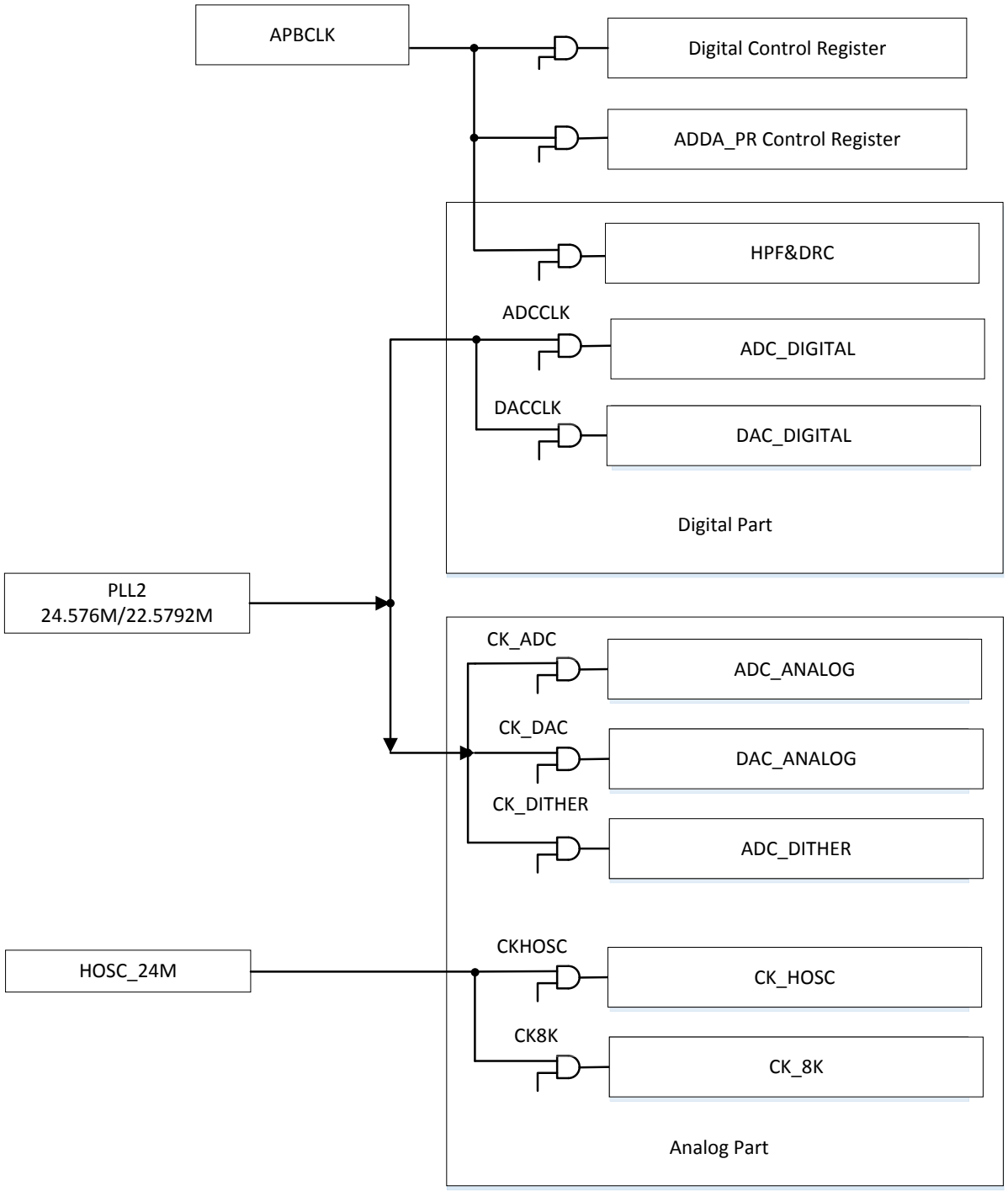

Figure 9- 16. Audio Codec Clock Diagram

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9.4.3.3. Reset System

9.4.3.3.1. Digital Part Reset System

The SYS_RST will be provided by the VDD_SYS domain, which comes from VDD_SYS domain and is produced by RTC domain. Each domain has the de-bounce to confirm the reset system is strong. The codec register part, MIX will be reset by the SYS_RST during the power on or the system soft writing the reset control logic. The other parts will be reset by the soft configure through writing register.

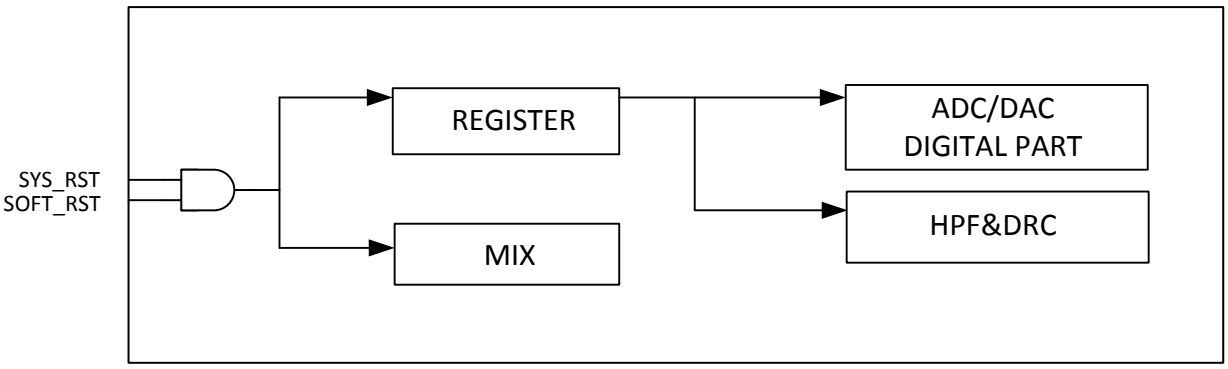

Figure 9- 17. Audio Codec Digital Part Reset System

9.4.3.3.2. Analog Part Reset System

When AVCC is powered on, it will send the AVCC_POR signal. And the AVCC_POR signal passes the level shift and RC filter part to ADDA logic core.

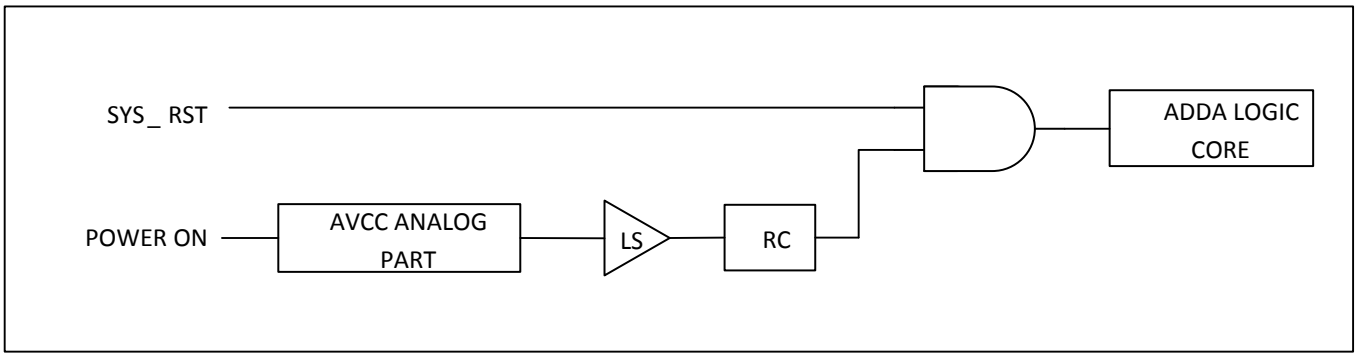

Figure 9- 18. Audio Codec Analog Part Reset System

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9.4.3.4. Data Path Diagram

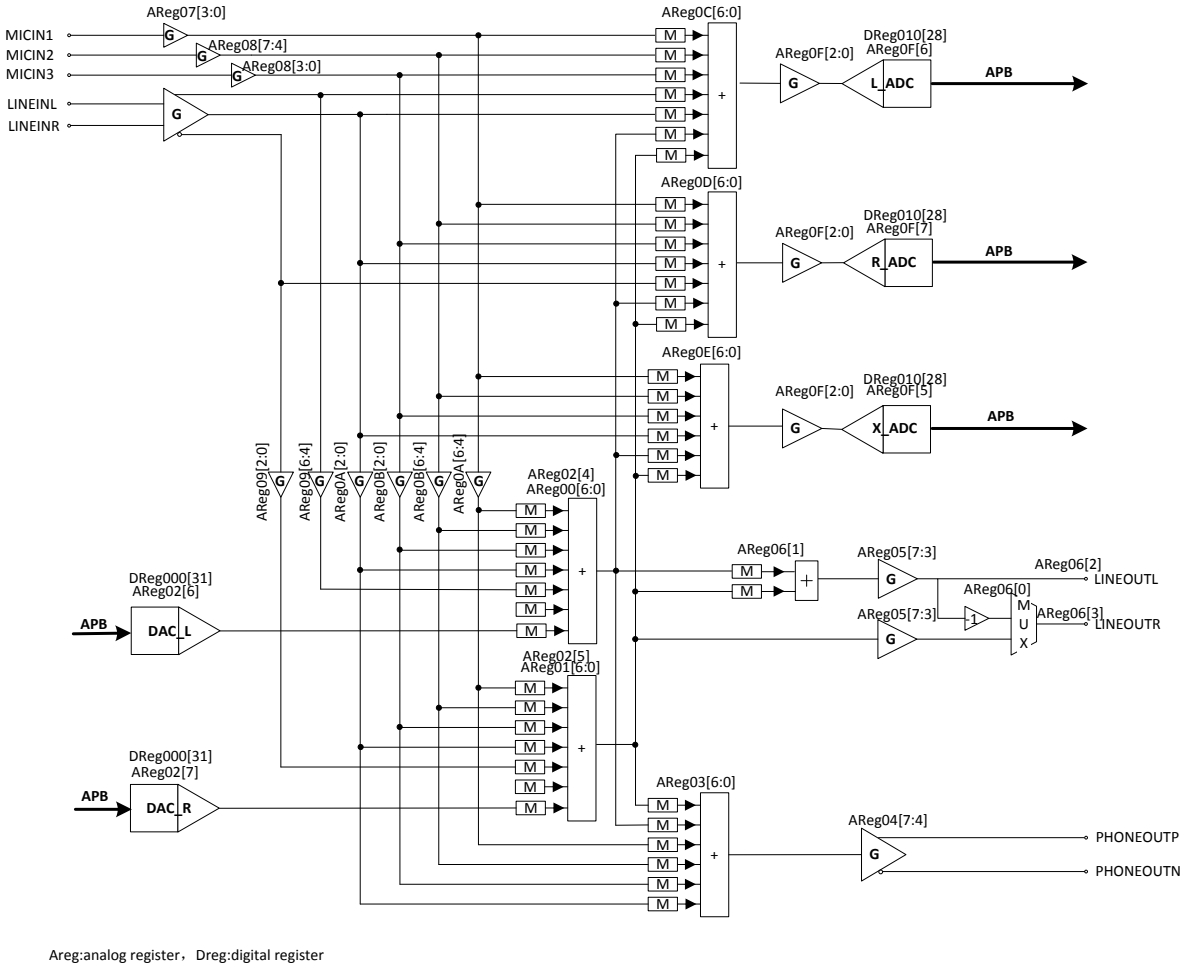

Figure 9- 19. Audio Codec Data Path Diagram

9.4.3.5. Three ADC

The three ADC is used for recording stereo sound and a reference signal. The sample rate of the three ADC is independent of DAC sample rate. In order to save power, the left and right analog ADC part can be enabled/disabled separately by setting the bit[7:5] of the **AC_ADC_CTRL** register. The digital ADC part can be enabled/disabled by the bit28 of the **AC_ADC_FIFOC** register.

9.4.3.6. Stereo DAC

The stereo DAC sample rate can be configured by setting the register. In order to save power, the left and right DAC can be enabled/disabled separately by setting the bit[7:6] of the **DAC_PA_SRC** register. The digital DAC part can be enabled/disabled by the bit[31] of the **AC_DAC_DPC** register.

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9.4.3.7. Mixer

The Codec supports three mixers for all function requirements:

- 2 channels DAC output mixers
- 3 channels ADC Record mixers
- 1 channel Phoneout mixer

(1) ADC Record Mixers

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. The following signals can be mixed into the output mixer.

- LINEINL/R
- LINEINP/N
- MICIN1P/N
- MICIN2P/N
- MICIN3P/N
- Stereo DAC output

(2) Output Mixers

The output mixer is used to drive analog output.The following signals can be mixed into the output mixer.

- LINEINL/R
- LINEINP/N
- MICIN1P/N
- MICIN2P/N
- MICIN3P/N
- Stereo DAC output

(3) Phoneout Mixers

The phoneout mixer is used to drive analog output for phoneout. The following signals can be mixed into the phoneout mixer.

- LINEINP/N
- MICIN1P/N
- MICIN2P/N
- MICIN3P/N
- Output mixer

9.4.3.8. Analog Audio Input Path

The Codec supports five analog audio input paths:

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- LINEINL/R
- LINEINP/N
- MICIN1P/N
- MICIN2P/N
- MICIN3P/N

9.4.3.8.1. LINEINL/R&LINEINP/N

LINEIN provides 1-channel mono differential input or stereo single-ended input that can be mixed into the ADC record mixer or the stereo output mixer. The inputs are suited to receive line level signals from external audio equipment or baseband module .

9.4.3.8.2. Microphone Input

MICIN1P/N, MICIN2P/N and MICIN3P/N provide differential input that can be mixed into the ADC record mixer, or DAC output mixer. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. The gain for each pre-amplifier can be set independently.MBIAS provides reference voltage for electret condenser type(ECM) microphones.

9.4.3.9. Analog Audio Output Path

The Codec has two type analog output ports:

- LINEOUT
- PHONEOUT

9.4.3.9.1. LINEOUT

The LINEOUT provides one stereo output to drive line level signals to external audio equipment .The LINEOUTL output source can be selected from left output mixer or (left+right) output mixer. The LINEOUTR output source can be selected from right output mixer or left output mixer differential output.The volume control is logarithmic with an 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The LINEOUT output buffer is powered up or down by the bit[7:6] of **LINEOUT_MIC2_CTRL**.

9.4.3.9.2. PHONEOUT

The PHONEOUTP/N provides one differential output to drive line level signals to external audio equipment or baseband module .The PHONEOUTP/N input source can be selected from MIC1 pre-amplifier output, MIC2 pre-amplifier output, MIC3 pre-amplifier output, LINEINP/N,left output mixer or right output mixer. The volume control is logarithmic with an 10.5dB rang in 1.5dB step from -4.5dB to 6dB. The PHONEOUTP/N output buffer is powered up or down by the bit[3] of **PHONEOUT_CTRL**.

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9.4.3.10. Microphone BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network.

9.4.3.11. Interrupt

The Audio Codec has two interrupts. Figure 9-20 describes the Audio Codec interrupt system.

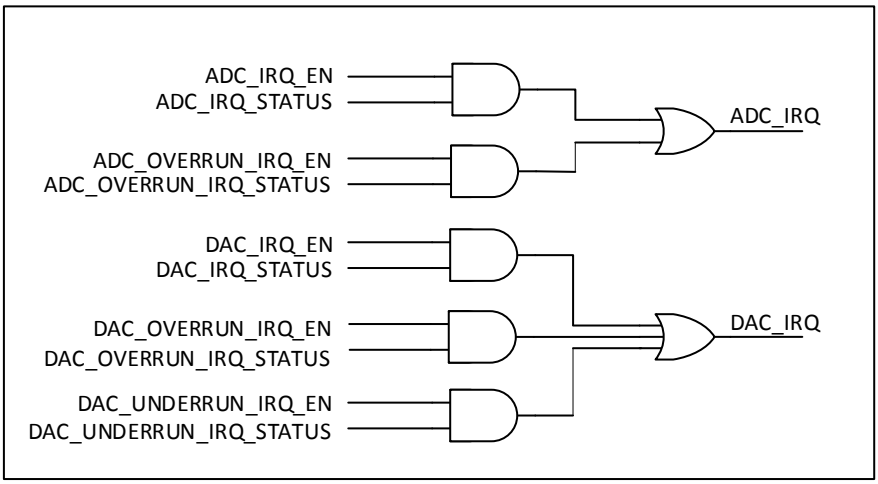

Figure 9- 20. Audio Codec Interrupt System

9.4.3.12. DAP

9.4.3.12.1. DAP Data Flow

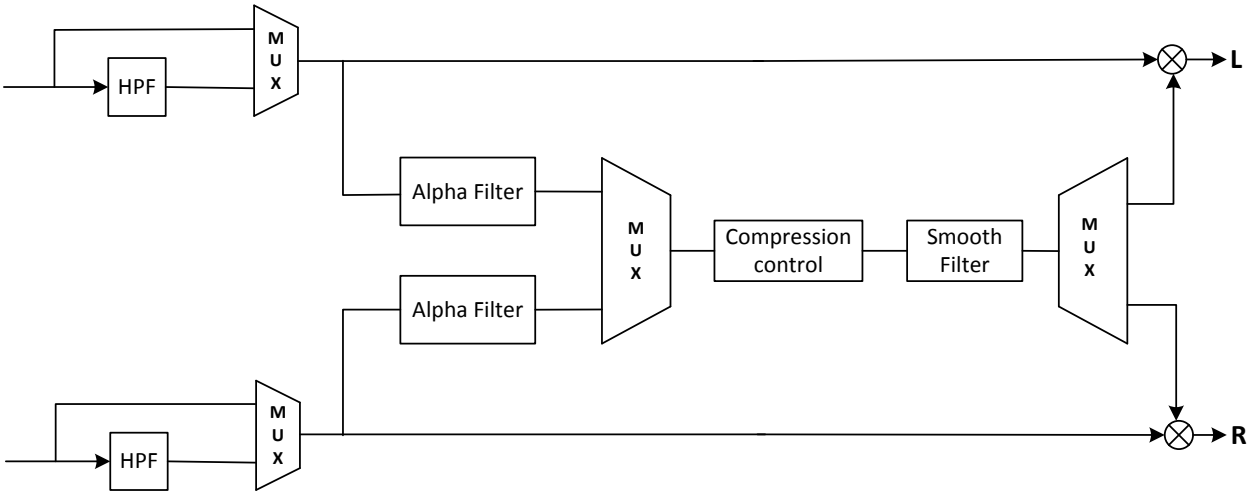

Figure 9- 21. DAP Data Flow

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9.4.3.12.2. HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz that can be removed DC offset from ADC recording. The HPF can also be bypassed.

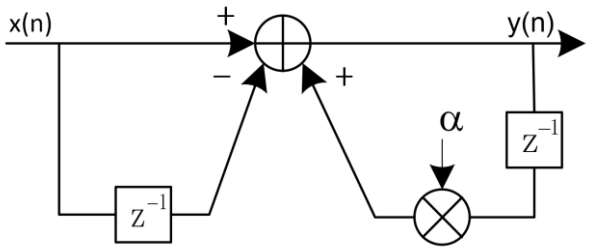

Figure 9- 22. HPF Function

9.4.4. Programming Guidelines

9.4.4.1. Playback Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**. Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate,configure data transfer format, open DAC.
(4) DMA configure and DMA request.
(5) Enable DAC DRQ and DMA.

9.4.4.2. Record Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**.Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate,configure data transfer format, open ADC.
(4) DMA configure and DMA request.
(5) Enable ADC DRQ and DMA.

9.4.5. Register List

Module Name	Base Address
Audio Codec	0x05096000

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Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
AC_DAC_FIFOC	0x0010	DAC FIFO Control Register
AC_DAC_FIFOS	0x0014	DAC FIFO Status Register
AC_DAC_TXDATA	0x0020	DAC TX DATA Register
AC_DAC_CNT	0x0024	DAC TX FIFO Counter Register
AC_DAC_DG	0x0028	DAC Debug Register
AC_ADC_FIFOC	0x0030	ADC FIFO Control Register
AC_ADC_FIFOS	0x0034	ADC FIFO Status Register
AC_ADC_RXDATA	0x0040	ADC RX Data Register
AC_ADC_CNT	0x0044	ADC RX Counter Register
AC_ADC_DG	0x004C	ADC Debug Register
AC_DAC_DAP_CTRL	0x00F0	DAC DAP Control Register
AC_ADC_DAP_CTR	0x00F8	ADC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_RPFHRT	0x0124	DAC DRC Right Peak filter High Release Time Coef Register
AC_DAC_DRC_RPFLRT	0x0128	DAC DRC Right Peak filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_RRMSHAT	0x0134	DAC DRC Right RMS Filter High Coef Register
AC_DAC_DRC_RRMSLAT	0x0138	DAC DRC Right RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Threshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Threshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Threshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold Register
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold Register

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AC_DAC_DRC_HET	0x016C	DAC DRC Expander Threshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Threshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold Register
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold Register
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth Filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth Filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth Filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_OPT	0x01B4	DAC DRC Optimum Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_RPFHAT	0x0214	ADC DRC Right Peak Filter High Attack Time Coef Register
AC_ADC_DRC_RPFLAT	0x0218	ADC DRC Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_RPFHRT	0x0224	ADC DRC Right Peak Filter High Release Time Coef Register
AC_ADC_DRC_RPFLRT	0x0228	ADC DRC Right Peak Filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_RRMSHAT	0x0234	ADC DRC Right RMS Filter High Coef Register
AC_ADC_DRC_RRMSLAT	0x0238	ADC DRC Right RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Threshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold

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		Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Threshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Threshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Threshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Threshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold Register
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold Register
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth Filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth Filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth Filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGLS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_OPT	0x02B4	ADC DRC Optimum Register
AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
Analog Domain Register		
AC_LOMIXSC	0x01	Left Output Mixer Source Select Control Register
AC_ROMIXSC	0x02	Right Output Mixer Source Select Control Register
DAC_PA_SRC	0x03	DAC Analog Enable and PA Source Control Register
LINEIN_GCTR	0x04	Linein Stereo Gain Control Register
LINEINP/N&MIC1_GCTRL	0x05	LINEINP/N and MIC1 Gain Control Register
MIC2&3_GCTR	0x06	MIC2 And MIC3 Gain Control Register
PHONEOUT_CTRL	0x07	Phoneout Control Register
PHOMIX&MICBIAS_CTRL	0x08	PHONEOUT Mixer Source Control and MICBIAS Enable Register
LOUT&LINP/N_VOLCTRL	0x09	LINEOUT Volume and LINEINP/N Gain Control Register
LOUT_MIC1_CTRL	0x0A	LINEOUT Enable Control and MIC1 Boost Register
MIC2&3_BOOST_CTRL	0x0B	MIC2 Boost and MIC3 Boost Register
LADC_MIX_MUTE	0x0C	Left ADC Mixer Mute Control Register
RADC_MIX_MUTE	0x0D	Right ADC Mixer Mute Control Register
XADC_MIX_MUTE	0x0E	XADC Mixer Mute Control Register

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AC_ADC_CTRL	0x0F	ADC Analog Control Register
OP_CTRL0	0x10	OPDRV/OPCOM、OPADC Control Register
OP_CTRL1	0x11	OPMIC、OPVR and OPADC Control Register
USB_BIAS_CTRL	0x12	USB Bias Control Register
ADC_FUN_CTRL	0x13	ADC Function Control Register
CALI_CTRL	0x14	Bias & DA16 Calibration Control Register
DA16CALI_DATA	0x15	DA16 Calibration Data Register
BIASCALI_DATA	0x17	Bias Calibration Data Register
BIASCALI_SET	0x18	Bias Register Setting Data Register

9.4.6. Register Description

9.4.6.1. DAC Digital Part Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: AC_DAC_DPC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EN_DA DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step
11:1	/	/	/
0	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable

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9.4.6.2. DAC FIFO Control Register(Default Value: 0x0000_4000)

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	DAC_FS Sample Rate of DAC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: 192 kHz 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: 96 kHz 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO underrun 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 24-bit transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:8]} 01/11: Reserved For 16-bit transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 01/11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: IRQ/DRQ De-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ generated when WLEVEL ≤ TXTL

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			NOTE **WLEVEL represents the number of valid samples in the TX FIFO.** **Only TXTL[6:0] valid when TXMODE = 0**
7	/	/	/
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data.
5	R/W	0x0	TX_SAMPLE_BITS. Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Underrun IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	FIFO_FLUSH DAC FIFO Flush Write ‘1’ to flush TX FIFO, self clear to ‘0’

9.4.6.3. DAC FIFO Status Register(Default Value: 0x0080_8008)

Offset: 0x0014			**Register Name: AC_DAC_FIFOS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT

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			TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

9.4.6.4. DAC TX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0020			**Register Name: AC_DAC_TXDATA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

9.4.6.5. DAC TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0024			**Register Name: AC_DAC_CNT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **NOTE** **It is used for Audio/Video Synchronization**

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9.4.6.6. DAC Debug Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: Silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC Clock from PLL 1: CODEC Clock from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC Output Channel Swap Enable 0:Disable 1:Enable
5:2	/	/	/
1:0	R/W	0x0	ADDA_LOOP_MODE ADDA Loop Mode Select 00: Disable 01: ADDA LOOP MODE DACL/R connect to ADCL/R 10: ADDA LOOP MODE DACL connect to ADCX 11:Reserved

9.4.6.7. ADC FIFO Control Register(Default Value: 0x0000_0400)

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz

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			011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable
27:26	R/W	0x0	ADCFDT ADC FIFO delay time for writing data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms
25	R/W	0x0	ADCDFEN ADC FIFO delay function for writing data after EN_AD 0: Disable 1: Enable
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:17	/	/	/
16	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits
15	/	/	/
14:12	R/W	0x0	ADC_CHANNEL_EN Bit 14: ADCX enable Bit 13: ADCR enable Bit 12: ADCL enable
11:10	/	/	/
9:4	R/W	0x40	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL[5:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ Generated when WLEVEL ＞ RXTL[5:0] **NOTE**

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			WLEVEL represents the number of valid samples in the RX FIFO.
3	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'.

9.4.6.8. ADC FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: AC_ADC_FIFOS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:15	/	/	/
14:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W1C	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

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9.4.6.9. ADC RX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

9.4.6.10. ADC RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **NOTE** **It is used for Audio/Video Synchronization.**

9.4.6.11. ADC Debug Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	AD_SWP ADC output channel swap enable (for digital filter) 0: Disable 1: Enable
23:0	/	/	/

9.4.6.12. DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDAP_EN DAP for DRC Enable

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			0 : Bypass 1 : Enable
30	/	/	/
29	R/W	0x0	DDAP_DRC_EN DRC enable control 0:Disable 1:Enable
28	R/W	0x0	DDAP_HPF_EN HPF enable control 0:Disable 1:Enable
27:0	/	/	/

9.4.6.13. ADC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_DAP0_EN DAP for ADC enable 0:Bypass 1:Enable
30	/	/	/
29	R/W	0x0	ADC_DRC0_EN ADC DRC0 enable control 0:Disable 1:Enable
28	R/W	0x0	ADC_HPF0_EN ADC HPF0 enable control 0:Disable 1:Enable
27	R/W	0x0	ADC_DAP1_EN The DAP controls the DAC of ADCX/Y.
26	/	/	/
25	R/W	0x0	ADC_DRC1_EN ADC DRC1 enable control 0:Disable 1:Enable
24	R/W	0x0	ADC_HPF1_EN ADC HPF1 enable control 0:Disable 1:Enable
23:0	/	/	/

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9.4.6.14. DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.4.6.15. DAC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

9.4.6.16. DAC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enabled and the drc funciton is disabled. After disabled drc function and this bit goes to 0, the user should write the drc delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc is disabled and the drc buffer data output completely. 0: Don't use the buffer 1: Use the buffer
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable

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5	R/W	0x0	DRC gain min limit enable When this fuction is enabled, it will overwrite the noise detect funciton. 0: Disable 1: Enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0: Disable 1: Enable
3	R/W	0x0	Signal function select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT /AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0: Disable 1: Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0: Disable 1: Enable When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0: Disable 1: Enable When the bit is disabled, Ke and OPE parameter is unused.

9.4.6.17. DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(1ms)

9.4.6.18. DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the

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			equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(1ms)

9.4.6.19. DAC DRC Right Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x0114			Register Name: AC_DAC_DRC_RPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.4.6.20. DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.4.6.21. DAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.22. DAC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.23. DAC DRC Right Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0124			Register Name: AC_DAC_DRC_RPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/

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10:0	R/W	0x00FF	The left peak filter attack time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.24. DAC DRC Right Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0128			Register Name: AC_DAC_DRC_RPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.25. DAC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.26. DAC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.27. DAC DRC Right RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x0134			Register Name: AC_DAC_DRC_RRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0001	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.28. DAC DRC Right RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0138			Register Name: AC_DAC_DRC_RRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:16	/	/	/
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.29. DAC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

9.4.6.30. DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

9.4.6.31. DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

9.4.6.32. DAC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

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9.4.6.33. DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor, which is determined by the equation -OPC/6.0206. The format is 8.24 (-40dB)

9.4.6.34. DAC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor, which is determined by the equation OPC/6.0206. The format is 8.24 (-40dB)

9.4.6.35. DAC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

9.4.6.36. DAC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (-10dB)

9.4.6.37. DAC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

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9.4.6.38. DAC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

9.4.6.39. DAC DRC Limiter High Output at Limiter Threshold Register(Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24 (-25dB)

9.4.6.40. DAC DRC Limiter Low Output at Limiter Threshold Register(Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24 (-25dB)

9.4.6.41. DAC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

9.4.6.42. DAC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

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15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

9.4.6.43. DAC DRC Expander Slope High Setting Register(Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

9.4.6.44. DAC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

9.4.6.45. DAC DRC Expander High Output at Expander Threshold Register(Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24 (-70dB)

9.4.6.46. DAC DRC Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

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9.4.6.47. DAC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0100	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

9.4.6.48. DAC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

9.4.6.49. DAC DRC Smooth Filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

9.4.6.50. DAC DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

9.4.6.51. DAC DRC Smooth filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by

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			the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

9.4.6.52. DAC DRC Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

9.4.6.53. DAC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

9.4.6.54. DAC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

9.4.6.55. DAC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

9.4.6.56. DAC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

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15:0	R/W	0x2C3F	The min gain setting, which is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

9.4.6.57. DAC DRC Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

9.4.6.58. DAC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

9.4.6.59. DAC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.4.6.60. DAC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.4.6.61. ADC DRC High HPF Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.4.6.62. ADC DRC Low HPF Coef Register(Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

9.4.6.63. ADC DRC Control Register(Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enabled and the drc funciton is disabled. After disabled drc function and this bit goes to 0, the user should write the drc delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc is disabled and the drc buffer data output completely. 0: Don't use the buffer 1: Use the buffer
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable
5	R/W	0x0	DRC gain min limit enable. When this fuction is enabled, it will overwrite the noise detect funciton. 0: Disable 1: Enable

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4	R/W	0x0	Control the drc to detect noise when ET is enabled 0: Disable 1: Enable
3	R/W	0x0	Signal function select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT /AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0: Disable 1: Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0: Disable 1: Enable When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0: Disable 1: Enable When the bit is disabled, Ke and OPE parameter is unused.

9.4.6.64. ADC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.4.6.65. ADC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

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9.4.6.66. ADC DRC Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x0214			Register Name: AC_ADC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.4.6.67. ADC DRC Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0218			Register Name: AC_ADC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.4.6.68. ADC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.69. ADC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.70. ADC DRC Right Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0224			Register Name: AC_ADC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter attack time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

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9.4.6.71. ADC DRC Right Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.4.6.72. ADC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.73. ADC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.74. ADC DRC Right RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x0234			Register Name: AC_ADC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.4.6.75. ADC DRC Right RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0238			Register Name: AC_ADC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

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9.4.6.76. ADC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

9.4.6.77. ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

9.4.6.78. ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

9.4.6.79. ADC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

9.4.6.80. ADC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor, which is determined by the equation

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			-OPC/6.0206 The format is 8.24 (-40dB)

9.4.6.81. ADC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor, which is determined by the equation OPC/6.0206 The format is 8.24 (-40dB)

9.4.6.82. ADC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

9.4.6.83. ADC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

9.4.6.84. ADC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

9.4.6.85. ADC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

9.4.6.86. ADC DRC Limiter High Output at Limiter Threshold Register(Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24 (-25dB)

9.4.6.87. ADC DRC Limiter Low Output at Limiter Threshold Register(Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24 (-25dB)

9.4.6.88. ADC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

9.4.6.89. ADC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

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9.4.6.90. ADC DRC Expander Slope High Setting Register(Default Value:0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

9.4.6.91. ADC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

9.4.6.92. ADC DRC Expander High Output at Expander Threshold Register(Default Value:0x0000_F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24 (-70dB)

9.4.6.93. ADC DRC Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24 (-70dB)

9.4.6.94. ADC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0100	The slope of the linear, which is determined by the equation that Kn = 1/R,

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			there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

9.4.6.95. ADC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

9.4.6.96. ADC DRC Smooth Filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

9.4.6.97. ADC DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

9.4.6.98. ADC DRC Smooth Filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

9.4.6.99. ADC DRC Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0298	Register Name: AC_ADC_DRC_SFLRT

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Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

9.4.6.100. ADC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

9.4.6.101. ADC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

9.4.6.102. ADC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

9.4.6.103. ADC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting, which is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

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9.4.6.104. ADC DAP Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

9.4.6.105. ADC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

9.4.6.106. ADC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting, which format is 3.24.(gain = 1)

9.4.6.107. ADC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting, which format is 3.24.(gain = 1)

9.4.7. Audio Codec Analog Part Configuration IO

The analog part configure of Audio Codec is set through the **ADD_PR_CFG_REG** register.The ADDA_PR_RST bit can reset the **ADD_PR_CFG_REG** register. The ADDA_PR_ADDR defines the analog register address, and the ADDA_PR_RW decides the operation is read or write. When the operation is read, we would read data of the analog register from the ADDA_PR_RDAT. When the operation is write, we would write the ADDA_PR_WDAT value to the ADDA_PR_ADDR analog register.

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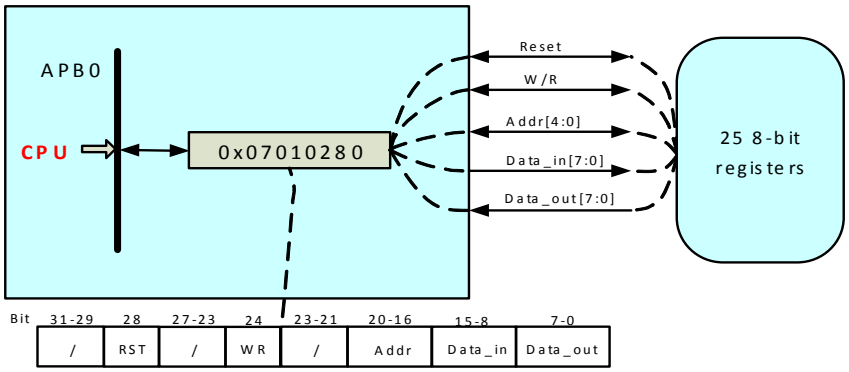

Offset: 0x07010280			Register Name: ADDA_PR_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	ADDA_PR_RST ADDA_PR Reset 0: Assert 1: De-assert
27:25	/	/	/
24	R/W	0x0	ADDA_PR_RW ADDA_PR Read or Write 0: read 1: write
23:21	/	/	/
20:16	R/W	0x0	ADDA_PR _ADDR ADDA_PR Address[4:0]
15:8	R/W	0x0	ADDA_PR _WDAT ADDA_PR Write Data [7:0]
7:0	R/W	0x0	ADDA_PR _RDAT ADDA_PR Read Data[7:0]

9.4.7.1. Left Output Mixer Source Select Control Register(Default Value: 0x00)

Offset: 0x01			Register Name: AC_LOMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	LMIXMUTE Left Output Mixer Mute Control 0: Mute 1: Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: MIC3 Boost Stage Bit 3: LINEINL(P)- LINEINR(N) Bit 2: LINEINL

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			Bit 1: Left Channel DAC Bit 0: Right Channel DAC

9.4.7.2. Right Output Mixer Source Select Control Register(Default Value: 0x00)

Offset: 0x02			Register Name: AC_ROMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RMIXMUTE Right Output Mixer Mute Control 0: Mute 1: Not Mute Bit 6: MIC1 Boost Stage Bit 5: MIC2 Boost Stage Bit 4: MIC3 Boost Stage Bit 3: LINEINL(P)- LINEINR(N) Bit 2: LINEINR Bit 1: Right Channel DAC Bit 0: Left Channel DAC

9.4.7.3. DAC Analog Enable and PA Source Control Register(Default Value: 0x00)

Offset: 0x03			Register Name: DAC_PA_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	DACAREN Internal Analog Right Channel DAC Enable 0:Disable 1:Enable
6	R/W	0x0	DACALEN Internal Analog Left Channel DAC Enable 0:Disable 1:Enable
5	R/W	0x0	RMIXEN Right Analog Output Mixer Enable 0:Disable 1:Enable
4	R/W	0x0	LMIXEN Left Analog Output Mixer Enable 0:Disable 1:Enable
3:0	/	/	/

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9.4.7.4. Linein Stereo Gain Control Register(Default Value: 0x33)

Offset: 0x04			Register Name: LINEIN_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	LINEINLG LINEINL to left output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x3	LINEINRG LINEINR to right output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

9.4.7.5. Linein and MIC1 Gain Control Register(Default Value: 0x33)

Offset: 0x05			Register Name: LINEINP/N&MIC1_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	LINEINGG LINEINL-R to L/R mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x3	MIC1_GAIN MIC1 BOOST stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

9.4.7.6. MIC2 And MIC3 Gain Control Register(Default Value: 0x33)

Offset: 0x06			Register Name: MIC2&3_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	MIC2_GAIN MIC2 BOOST stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x3	MIC3_GAIN MIC2 BOOST stage to L or R output mixer gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

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9.4.7.7. Phoneout Control Register(Default Value: 0x03)

Offset: 0x07			Register Name: PHONEOUT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:4	/	/	/
3	R/W	0x0	PHONEOUT Enable 0: Disable 1: Enable
2:0	R/W	0x3	PHONEOUT PONEOUT Gain Control From -4.5dB to 6 dB,1.5dB/step ,default is 0dB

9.4.7.8. Phoneout Mixer Source Control and MICBIASEN Enable Register(Default Value: 0x00)

Offset: 0x08			Register Name: PHOMIX&MICBIAS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6	R/W	0x0	MMICBIASEN Master Microphone Bias Enable 0: Disable 1: Enable
5:0	R/W	0x0	PONEOUTMIXMUTE Poneout Mixer Source Control 0: Mute 1:On Bit 5: Reserved Bit 4: MIC3 Boost stage Bit 3: MIC1 Boost stage Bit 2: MIC2 Boost stage Bit 1: Right output mixer Bit 0: Left output mixer

9.4.7.9. Lineout Volume and LineinP/N Gain Control Register(Default Value: 0x04)

Offset: 0x09			Register Name: LINEOUT_VOLCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:3	R/W	0x0	LINEOUTVOL Line-out Volume Control, total 31 level, from 0dB to -43.5dB, 1.5dB/step, mute when 00000 & 00001
2:0	R/W	0x4	LINEINL(P)- LINEINR(N) LINEINL(P)- LINEINR(N) Gain, total 8 level, from -12dB to 9dB, 3dB/step, mute,default is 0dB

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9.4.7.10. Lineout Enable Control and MIC1 Boost Register(Default Value: 0x04)

Offset: 0x0A			Register Name: LINEOUT_ MIC1 _CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	Line-out Left Enable 0:Disable 1:Enable
6	R/W	0x0	Line-out Right Enable 0:Disable 1:Enable
5	R/W	0x0	Left Line-out Source Select 0:Left output mixer 1:Left output mixer + right output mixer
4	R/W	0x0	Right Line-out Source Select 0:Right output mixer 1:Left line-out, for differential output
3	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0:Disable 1:Enable
2:0	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

9.4.7.11. MIC2 Boost and MIC3 Boost Register(Default Value: 0x44)

Offset: 0x0B			Register Name: MIC2&3_BOOST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0:Disable 1:Enable
6:4	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB
3	R/W	0x0	MIC3AMPEN MIC3 Boost AMP Enable 0:Disable 1:Enable
2:0	R/W	0x4	MIC3BOOST MIC3 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

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9.4.7.12. Left ADC Mixer Mute Control Register(Default Value: 0x00)

Offset: 0x0C			Register Name: LADC_MIX_MUTE
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	LADCMIXMUTE Left ADC Mixer Mute Control 0: Mute 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: MIC3 Boost stage Bit 3: LINEINL(P)- LINEINR(N) Bit 2: LINEINL Bit 1: Left output mixer Bit 0: Right output mixer

9.4.7.13. Right ADC Mixer Mute Control Register(Default Value: 0x00)

Offset: 0x0D			Register Name: RADC_MIX_MUTE
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control 0: Mute 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: MIC3 Boost stage Bit 3: LINEINL(P)- LINEINR(N) Bit 2: LINEINR Bit 1: Right output mixer Bit 0: Left output mixer

9.4.7.14. XADC Mixer Mute Control Register(Default Value: 0x00)

Offset: 0x0E			Register Name: XADC_MIX_MUTE
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	XADCMIXMUTE X ADC Mixer Mute Control 0: Mute 1:On

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			Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: MIC3 Boost stage Bit 3: LINEINL(P)- LINEINR(N) Bit 2: / Bit 1: Right output mixer Bit 0: Left output mixer

9.4.7.15. ADC Analog Control Register(Default Value: 0x03)

Offset: 0x0F			Register Name: AC_ADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	ADCREN ADC Right Channel Enable 0:Disable 1:Enable
6	R/W	0x0	ADCLEN ADC Left Channel Enable 0:Disable 1:Enable
5	R/W	0x0	ADCXEN ADC X Channel Enable 0:Disable 1:Enable
4:3	R/W	0x0	/
2:0	R/W	0x3	ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB

9.4.7.16. OPDRV/OPCOM、OPADC Control Register(Default Value: 0x55)

Offset: 0x10			Register Name: OP_CTRL0
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	/	/	/
5:4	R/W	0x1	OPADC1_BIAS_CUR OPADC1 Bias Current Select
3:2	R/W	0x1	OPADC2_BIAS_CUR OPADC2 Bias Current Select
1:0	R/W	0x1	OPAAF_BIAS_CUR OPAAF in ADC Bias Current Select

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9.4.7.17. OPMIC、OPVR and OPADC Control Register(Default Value: 0x55)

Offset: 0x11			Register Name: OP_CTRL1
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x1	OPMIC_BIAS_CUR OPMIC Bias Current Control
5:4	R/W	0x1	OPVR_BIAS_CUR OPVR Bias Current Control Especially, the bit 5 can also control HPCOMFB: 0: HPCOMFB pin can be used to PA when R07_[6:5] is not 11 1: HPCOMFB pin always can not be used to PA
3:2	R/W	0x1	OPDAC_BIAS_CUR OPDAC Bias Current Control
1:0	R/W	0x1	OPMIX_BIAS_CUR OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control

9.4.7.18. USB Bias Control Register(Default Value: 0x42)

Offset: 0x12			Register Name: USB_BIAS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:3	/	/	/
2:0	R/W	0x2	USB_BIAS_CUR USB bias current tuning From 23uA to 30uA, Default is 25uA

9.4.7.19. ADC Function Control Register(Default Value: 0xD6)

Offset: 0x13			Register Name: ADC_FUN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x1	MMIC BIAS chopper enable 0: Disable 1: Enable
6:5	R/W	0x2	MMIC BIAS chopper clock select 00: 250 kHz 01: 500 kHz 10: 1 MHz 11: 2 MHz
4	R/W	0x1	DITHER ADC dither on/off control 0: Dither off 1: Dither on
3:2	R/W	0x1	DITHER_CLK_SELECT

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			ADC dither clock select 00: ADC FS * (8/9), about 43 kHz when FS=48 kHz 01: ADC FS * (16/15), about 51 kHz when FS=48 kHz 10: ADC FS * (4/3), about 64 kHz when FS=48 kHz 11: ADC FS * (16/9), about 85 kHz when FS=48 kHz
1:0	R/W	0x2	BIHE_CTRL BIHE control 00: No BIHE 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC

9.4.7.20. Bias & DA16 Calibration Control Register(Default Value: 0x00)

Offset: 0x14			Register Name: CALI_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	PA_SPEED_SELECT PA setup speed control (for testing) 0: Slow 1: Fast
6	R/W	0x0	CURRENT_TEST_SELECT Internal current sink test enable (from LINEIN pin) 0: Normal 1: For Debug
5	R/W	0x0	/
4	R/W	0x0	BIAS and DA16 calibration clock select 0: 1 kHz 1: 500Hz
3	R/W	0x0	BIAS calibration mode select 0: Average 1: Single
2	R/W	0x0	BIAS and DA16 calibration control Write 1 to this bit, the calibration will be done again. Then this bit will be reset to zero automatically
1	R/W	0x0	BIASCALIVERIFY Bias Calibration Verify 0: Calibration 1: Register setting
0	/	/	/

9.4.7.21. DA16 Calibration Data Register

Offset: 0x15	Register Name: DA16CALI_DATA

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Bit	Read/Write	Default/Hex	Description
7:0	R	UDF	DA16CALI DA16 Calibration Data

9.4.7.22. Bias Calibration Data Register

Offset: 0x17			Register Name: BIASCALI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	/	/	/
5:0	R	UDF	BIASCALI Bias Calibration Data

9.4.7.23. Bias Register Setting Data Register(Default Value: 0x20)

Offset: 0x18			Register Name: BIASCALI_SET
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	/	/	/
5:0	R/W	0x20	BIASVERIFY Bias Register Setting Data

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Chapter 10 Interfaces

10.1. TWI

10.1.1. Overview

The TWI is designed as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including slave and master. The communication of the 2-wire bus is carried out by a byte-wise mode based on interrupt or polled handshaking. The TWI can be operated in standard mode (100 kbit/s) or fast-mode (400 kbit/s). The 10-bit addressing mode is supported for this specified application. General call addressing is also supported in slave mode.

The TWI has the following features:

- Software-programmable for slave or master
- Supports repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Supports speed up to 400 kbit/s (‘fast mode’)
- Allows operation from a wide range of input clock frequency

10.1.2. Block Diagram

Figure 10-1 shows the block diagram of TWI.

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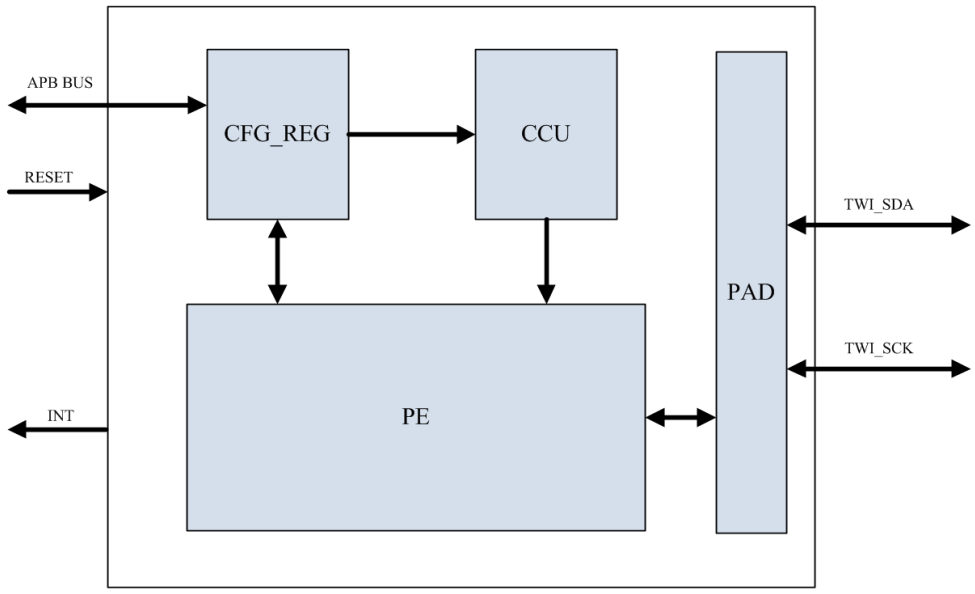

Figure 10- 1. TWI Block Diagram

RESET: Module reset signal

INT: Module output interrupt signal

CFG_REG: Module configuration register in TWI

PE: Packet encoding/decoding

CCU: Module clock controller unit

10.1.3. Operations and Functional Descriptions

10.1.3.1. External Signals

The TWI controller has 10 TWIs.Table 10-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O,when TWI is configured as master device,TWI_SCK is output pin;when TWI is configurable as slave device,TWI_SCK is input pin.other TWI ports are used as General Purpose I/O ports.For information about General Purpose I/O ports,see **Port Controller** in chapter10.

Table 10- 1. TWI External Signals

Signal (x=[6:0])	Description	Type
TWIx_SCK	TWIx Clock Signal for CPUX	I/O,OD
TWIx_SDA	TWIx Serial Data for CPUX	I/O,OD
S_TWI0_SCK	TWI0 Serial Clock Signal for CPUS	I/O,OD
S_TWI0_SDA	TWI0 Serial Data Signal for CPUS	I/O,OD
S_TWI1_SCK	TWI1 Serial Clock Signal for CPUS	I/O,OD
S_TWI1_SDA	TWI1 Serial Data Signal for CPUS	I/O,OD
S_TWI2_SCK	TWI2 Serial Clock Signal for CPUS	I/O,OD
S_TWI2_SDA	TWI2 Serial Data Signal for CPUS	I/O,OD

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10.1.3.2. Clock Sources

Each TWI controller has a fixed clock source.APB2 is the clock source of TWI in CPUX and APBS2 is the clock source of R-TWI in CPUS. Table 10-2 describes the clock sources for TWI. Users can see **Clock Controller Unit(CCU)** in chapter3 for clock setting,configuration and gating information.

Table 10- 2. TWI Clock Sources

Clock Sources	Description
APBS2_CLK	TWI in CPUS,for details on APBS2 refer to PRCM
APB2_CLK	TWI in CPUX,for details on APB2 refer to CCU

After select a proper clock, for using the TWI in CPUX, user must open the gating of TWI and release the reset bit. For using the TWI in CPUS,user also need to open the gating of R-TWI and release the reset bit . For more details on the gating/reset operations ,please refer to the **CCU** and **PRCM** specification**.**

10.1.3.3. Master and Slave Mode

There are four operation modes on the TWI bus. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing command and data to its registers. TWI transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP command is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit of the TWI_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START command and each consequent byte transfer. At each interrupt, the micro-processor needs to check the TWI_STAT register for current status. A transfer has to be concluded with STOP command by setting M_STP bit to high.

In Slave mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write TWI_DATA data register, and set the TWI_CNTR control register. After each byte transfer, a slave device always stop the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START command.

10.1.4. Programming Guidelines

The TWI controller operates in 8-bit data format.The data on the TWI_SDA line is always 8 bits long.At first,the TWI controller will sent a start condition.When in the addressing formats of 7-bit,TWI sends out a 8 bits message which include 7 MSB slave address and 1 LSB read/write flag.The least significant of the salve address indicates the direction of transmission.When TWI works in 10 bit slave address mode,the operation will be divided into two steps,for details on the operation please refer to register description in Section 10.1.6.1 and 10.1.6.2.

Figure 10-2 shows a software operation flow of TWI Initialization.

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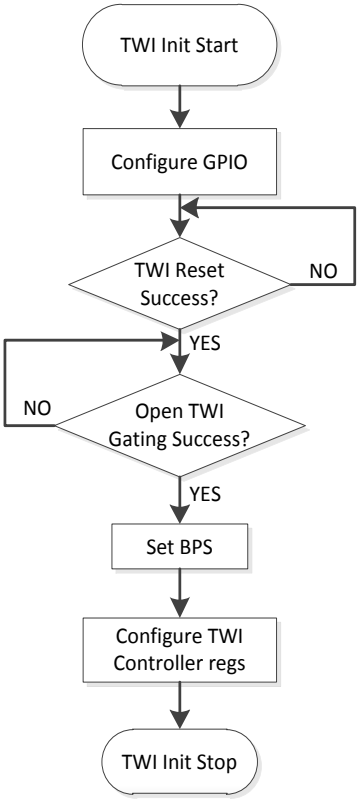

Figure 10- 2. TWI Initial Flow

Figure 10-3 shows a software operation flow of TWI write to device.

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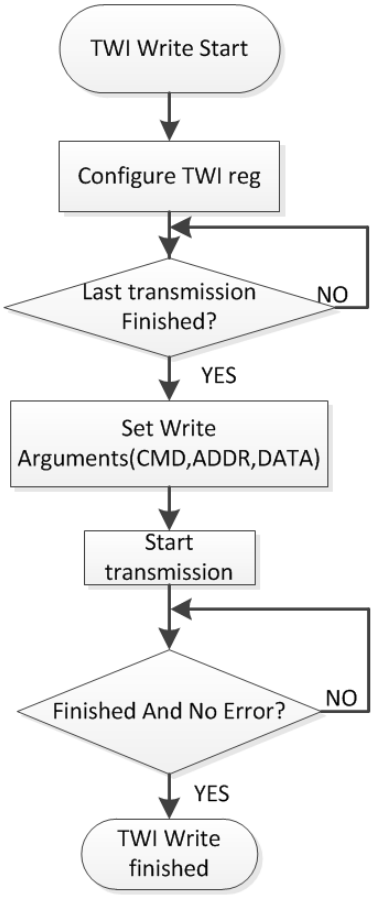

Figure 10- 3. TWI Write Flow

Figure 10-4 shows a software operation flow of TWI read from device.

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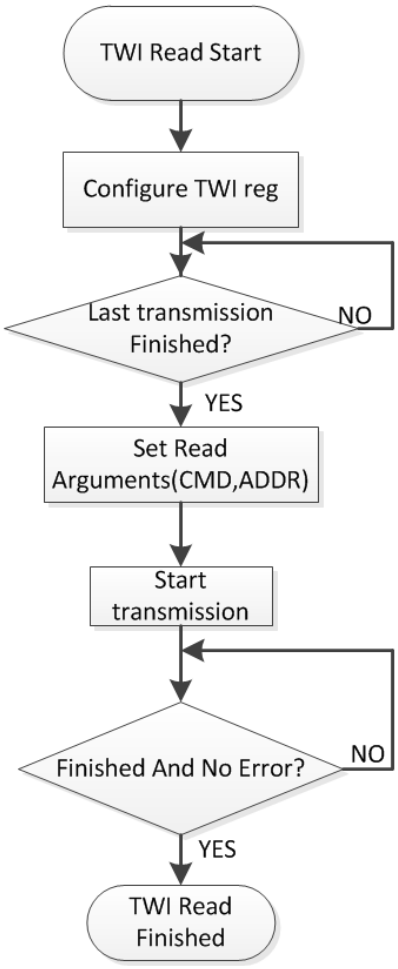

Figure 10- 4. TWI Read Flow

10.1.5. Register List

Module Name	Base Address
TWI0	0x05002000
TWI1	0x05002400
TWI2	0x05002800
TWI3	0x05002C00
TWI4	0x05003000
TWI5	0x05003400
TWI6	0x05003800
R_TWI0	0x07081400
R_TWI1	0x07081800
R_TWI2	0x07081C00

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address

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TWI_XADDR	0x0004	TWI Extended Slave Address
TWI_DATA	0x0008	TWI Data Byte
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register

10.1.6. Register Description

10.1.6.1. TWI Slave Address Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address 7-bit addressing: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

10.1.6.2. TWI Extend Address Register(Default Value:0x0000_0000)

Offset: 0x0004	Register Name: TWI_XADDR

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Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

10.1.6.3. TWI Data Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

10.1.6.4. TWI Control Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus ISDA/ISCL is ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to call to its slave address – and to the general call address if the GCE bit in the ADDR register is set. **NOTE** **In master operation mode, this bit should be set to '1'.**
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released.

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			The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.
4	R/W1C	0x0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the GCE bit in the ADDR register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

10.1.6.5. TWI Status Register(Default Value:0x0000_00F8)

Offset: 0x0010	Register Name: TWI_STAT

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Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

10.1.6.6. TWI Clock Register(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: TWI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/

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6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48 MHz (APB clock input) For 400 kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48 MHz/2^2=12 MHz, F1= F0/(10*(2+1)) = 0.4 MHz For 100 kHz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48 MHz/2^2=12 MHz, F1=F0/(10*(11+1)) = 0.1 MHz

10.1.6.7. TWI Soft Reset Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

10.1.6.8. TWI Enhance Feature Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
0:1	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00 : No data byte can be written after read command 01 : Only 1 byte data can be written after read command 10 : 2 bytes data can be written after read command 11 : 3 bytes data can be written after read command

10.1.6.9. TWI Line Control Register(Default Value:0x0000_003A)

Offset: 0x0020	Register Name: TWI_LCR

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Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0 : Low 1 : High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0 : Low 1 : High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When line control mode is enabled (bit[2] set), this bit decides the output level of TWI_SCL. 0 : Output low level 1 : Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0 : Disable TWI_SCL line control mode 1 : Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When line control mode is enabled (bit[0] set), this bit decides the output level of TWI_SDA. 0 : Output low level 1 : Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0 : Disable TWI_SDA line control mode 1 : Enable TWI_SDA line control mode

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10.2. UART

10.2.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in system where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART has the following features:

- Compatible with industry-standard 16550 UARTs
- 256 bytes transmit and receive data FIFOs
- Capable of speed up to 5 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

10.2.2. Block Diagram

Figure 10-5 shows a block diagram of the UART.

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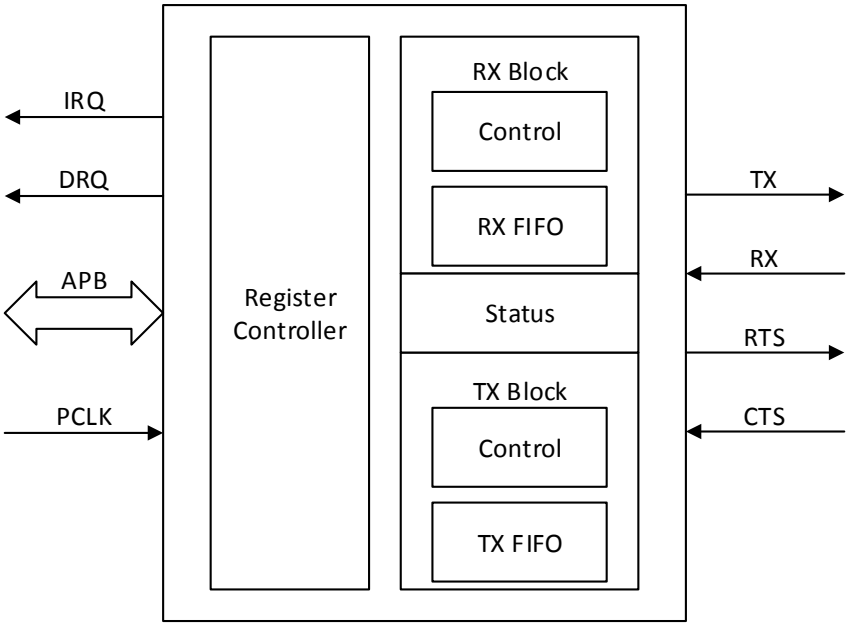

Figure 10- 5. UART Block Diagram

10.2.3. Operations and Functional Descriptions

10.2.3.1. External Signals

Table 10-3 describes the external signals of UART.

Table 10- 3. UART External Signals

Signal	Type	Description
UART0_TX	O	Serial Data Output
UART0_RX	I	Serial Data Input
UART1_TX	O	Serial Data Output
UART1_RX	I	Serial Data Input
UART1_CTS	I	Clear to Send
UART1_RTS	O	Request to Send
UART2_TX	O	Serial Data Output
UART2_RX	I	Serial Data Input
UART2_CTS	I	Clear to Send
UART2_RTS	O	Request to Send
UART3_TX	O	Serial Data Output
UART3_RX	I	Serial Data Input
UART3_CTS	I	Clear to Send
UART3_RTS	O	Request to Send
UART4_TX	O	Serial Data Output
UART4_RX	I	Serial Data Input
UART4_CTS	I	Clear to Send

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UART4_RTS	O	Request to Send
R_UART0_TX	O	Serial Data Output
R_UART0_RX	I	Serial Data Input
R_UART1_TX	O	Serial Data Output
R_UART1_RX	I	Serial Data Input
R_UART1_CTS	I	Clear to Send
R_UART1_RTS	O	Request to Send
R_UART2_TX	O	Serial Data Output
R_UART2_RX	I	Serial Data Input
R_UART2_CTS	I	Clear to Send
R_UART2_RTS	O	Request to Send
R_UART3_TX	O	Serial Data Output
R_UART3_RX	I	Serial Data Input
R_UART3_CTS	I	Clear to Send
R_UART3_RTS	O	Request to Send
R_UART4_TX	O	Serial Data Output
R_UART4_RX	I	Serial Data Input

10.2.3.2. Clock Sources

Table 10-4 describes the clock sources of UART.

Table 10- 4. UART Clock Sources

Clock Sources	Description
APB2_CLK	Clock of APB2

10.2.3.3. Typical Application

Figure 10-6 shows the application block diagram of UART.

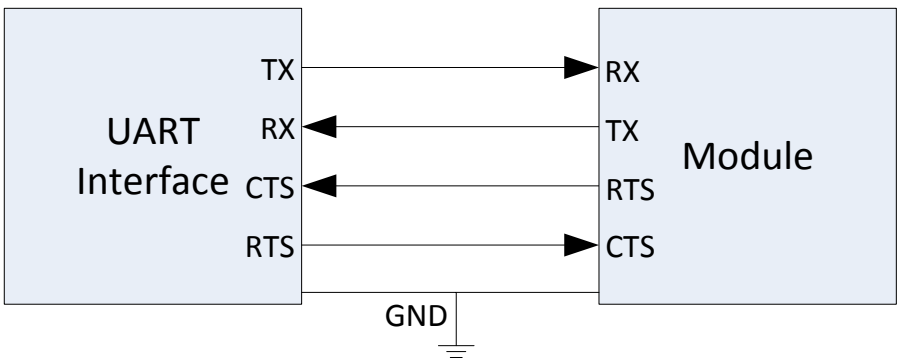

Figure 10- 6. UART Application Diagram

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10.2.3.4. UART Timing Diagram

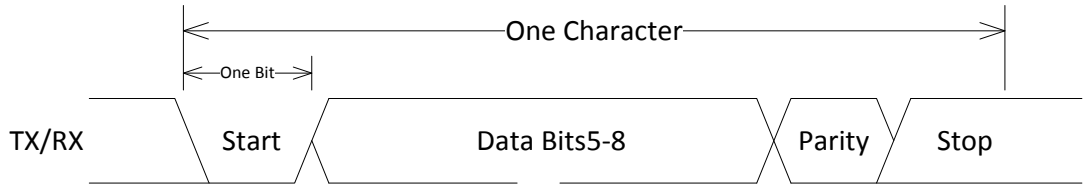

Figure 10- 7. UART Serial Data Format

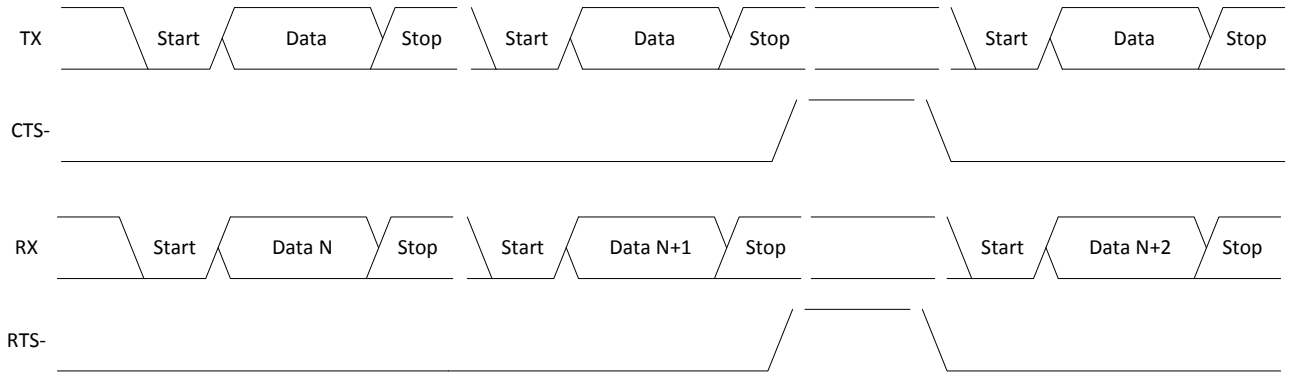

Figure 10- 8. RTS/CTS Autoflow Control Timing

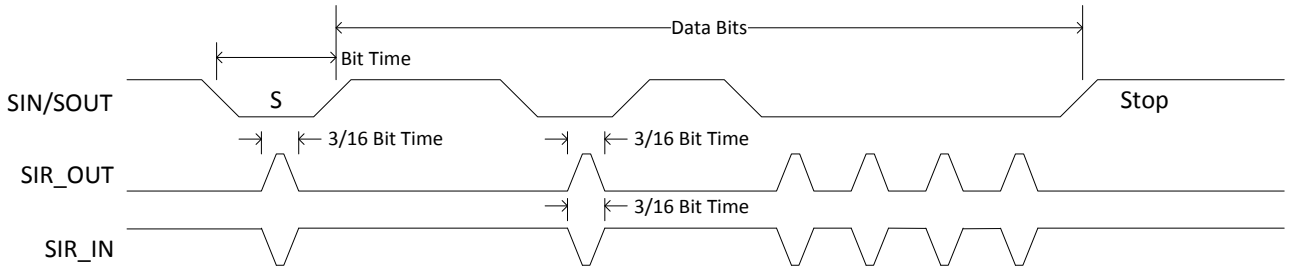

Figure 10- 9. Serial IrDA Data Format

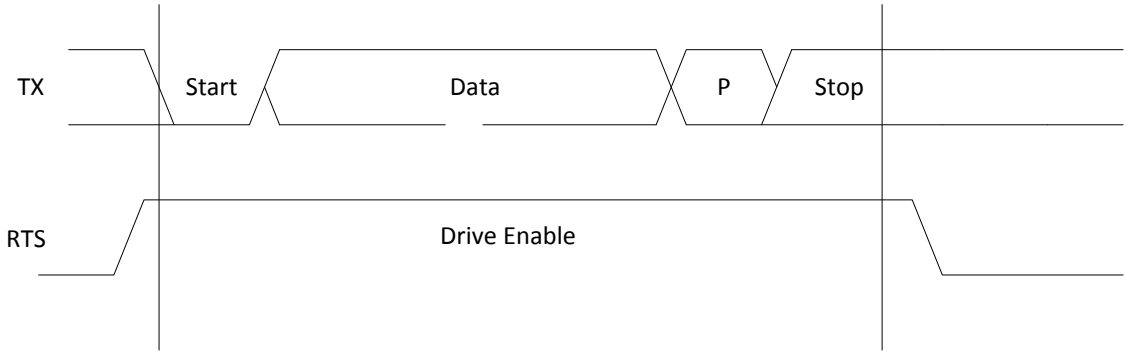

Figure 10- 10. RS-485 Timing

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10.2.3.5. UART Operating Mode

10.2.3.5.1. Basic Mode Setting

The **UART_LCR** register can set basic parameter of a data frame: data width, stop bit number, parity type.
A frame transfer of the UART includes the start signal, data signal, parity bit and stop signal. The LSB is transmitted first.

- Start signal(start bit): It is the start flag of a data frame. According to UART protocol, the low level of TXD signal indicates the start of a data frame. When the UART transmits data, the level need hold high.
- Data signal(data bit): The data bit width can be configured as 5-bit,6-bit,7-bit,8-bit through different applications.
- Parity bit: It is 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the **UART_LCR** register.
- Stop Signal(stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit,1.5-bit and 2-bit by the **UART_LCR** register. The high level of TXD signal indicates the end of a data frame.

10.2.3.5.2. Baud Rate Setting

The baud rate is calculated as follows: Baud rate = SCLK /(16 * divisor). SCLK is usually APB2 and can be set in CCU.
Divisor is frequency divider of UART. The frequency divider has 16-bit,the low 8-bit is in the UART_DLL register, the high 8-bit is in the UART_DLH register.
The relationship between different UART mode and error rate is as follows.

Table 10- 5. UART Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Over sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
64000000	7	576000	16	-0.794
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
64000000	1	4000000	16	0

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Table 10- 6. IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 10- 7. RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16

10.2.3.5.3. DLAB Setting

DLAB control bit (**UART_LCR[7]**) is the access control bit of divisor Latch register.
If DLAB is 0, then 0x00 offset address is **TX/RX FIFO** register, 0x04 offset address is **IER** register.
If DLAB is 1, then 0x00 offset address is **DLL** register, 0x04 offset address is **DLH** register.
When UART initial, divisor need be set. That is, writing 1 to DLAB can access the **DLL** and **DLH** register, after finished setting, writing 0 to DLAB can access the **TX/RX FIFO** register.

10.2.3.5.4. CHCFG_AT_BUSY Setting

The function of **CHCFG_AT_BUSY**(UART_HALT[1]) and **CHANGE_UPDATE**(UART_HALT[2]) are as follows.
CHCFG_AT_BUSY(configure at busy): Enable the bit, software can also set UART controller when UART is busy, such as the LCR,DLH,DLL register.
CHANGE_UPDATE(change update): If **CHCFG_AT_BUSY** is enabled, and **CHANGE_UPDATE** is written to 1, the

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configuration of UART controller can be updated. After completed update, the bit is cleared to 0 automatically.

Setting divisor, performs the following steps:

Step1 Write 1 to **CHCFG_AT_BUSY** to enable configure at busy.

Step2 Write 1 to **DLAB** , and set **DLH** and **DLL**.

Step3 Write 1 to **CHANGE_UPDATE** to update configuration. The bit is cleared to 0 automatically after completed update.

10.2.3.5.5. UART Busy

UART_USR[0] is a busy flag of UART controller or not.

When TX transmits data, or RX receives data,or TX FIFO is not empty, or RX FIFO is not empty, then the BUSY flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

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10.2.4. Programming Guidelines

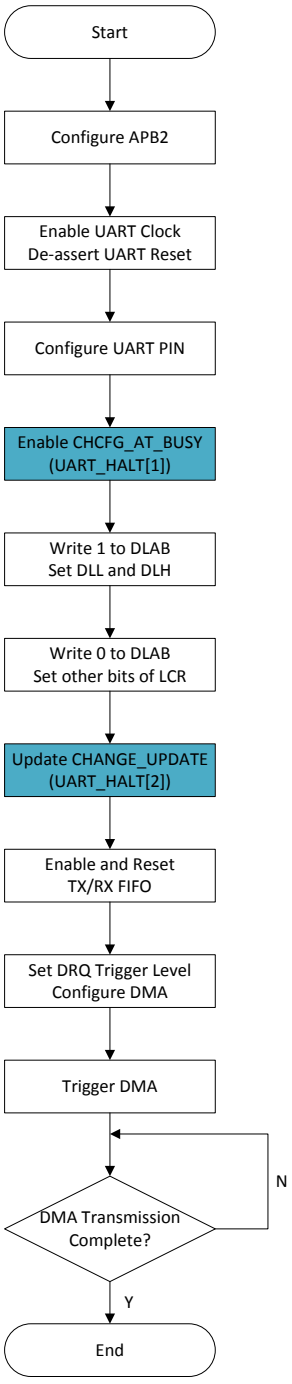

Figure 10- 11. UART DRQ Flow Chart

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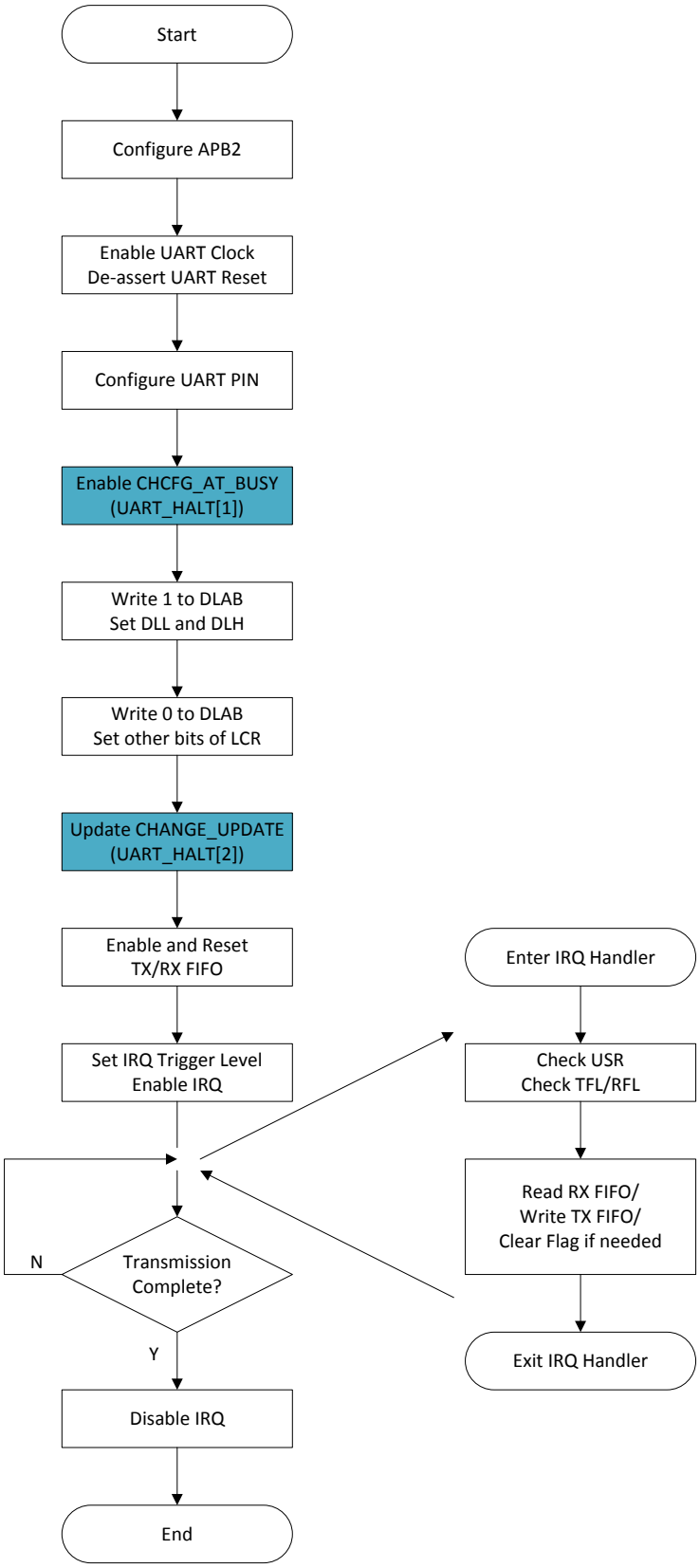

Figure 10- 12. UART IRQ Flow Chart

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10.2.5. Register List

Module Name	Base Address
UART0	0x05000000
UART1	0x05000400
UART2	0x05000800
UART3	0x05000C00
UART4	0x05001000
R_UART0	0x07080000
R_UART1	0x07080400
R_UART2	0x07080800
R_UART3	0x07080C00
R_UART4	0x07081000

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control and Status Register
RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHK	0x00C8	UART RS485 Bus Idle Check Register
TX_DLY	0x00CC	UART TX Delay Register

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10.2.6. Register Description

10.2.6.1. UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register can not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

10.2.6.2. UART Transmit Holding Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters data may be written to the THR before the FIFO is full. When the FIFO is full, any write data results in the write data being lost.

10.2.6.3. UART Divisor Latch Low Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16 bits, read/write, Divisor Latch Register contains the

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			baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that when the Divisor Latch Registers (DLL and DLH) are set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

10.2.6.4. UART Divisor Latch High Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that when the Divisor Latch Registers (DLL and DLH) is set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

10.2.6.5. UART Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/

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4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupt. 0: Disable 1: Enable

10.2.6.6. UART Interrupt Identity Register(Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of

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			the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout The bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/framing errors or break interrupt	Reading the line status register
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE mode disabled) or XMIT FIFO at or below threshold (Program THRE mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

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10.2.6.7. UART FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO when the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT TX Empty Trigger This is used to select the empty threshold level when the THRE Interrupts are generated and the mode is active. It also determines when the dma_tx_req_n signal is asserted in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, if PTE is high and TX FIFO is enabled, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is high and TX FIFO is disabled, the TX DMA request will send when THRE is empty. If PTE is low, the TX DMA request will send when the TX FIFO is empty. If dma_pte_rx is high and RX FIFO is enabled, the rx drq will send when RFL is equal to or more than FIFO Trigger Level. 1: Mode 1 In this mode, if TX FIFO is enabled and the PTE is high, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is low, the TX DMA request will send when TX FIFO is empty and the request stops only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level, the rx drq will be set to 1, in otherwise, it will be set to 0.
2	W	0x0	XFIFOR XMIT FIFO Reset The bit resets the control portion of the transmit FIFO and treats the FIFO

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			as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset The bit resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs The bit enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller portion of FIFOs is reset.

10.2.6.8. UART Line Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If setting to 0, the serial output is forced to the spacing (logic 0) state. When not in Loopback mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE is enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0x0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable/readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity

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			1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 0, indicates that this is a data byte. 10:9th bit = 1, indicates that this is an address byte. **NOTE** **When using this function, PEN(LCR[3]) must set to 1.**
3	R/W	0x0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: Parity disabled 1: Parity enabled
2	R/W	0x0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If setting to 0, one stop bit is transmitted in the serial data. If setting to 1 and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

10.2.6.9. UART Modem Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: UART_MCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 00:UART Mode

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			01:IrDA SIR Mode 10:RS485 Mode 11:Reserved
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control mode disabled 1: Auto Flow Control mode enabled
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] is set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] is set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The RTS (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] is set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] is set to one) and FIFOs enable (FCR[0] is set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] is set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1)

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			1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] is set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

10.2.6.10. UART Line Status Register(Default Value: 0x0000_0060)

Offset:0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to “1” when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided, there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by

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			the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.

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0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

10.2.6.11. UART Modem Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] is set to 1), DSR is the same as MCR[0] (DTR).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange

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			data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. **NOTE** **If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.**
2	RC	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). **NOTE** **If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.**
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).

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			NOTE **If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.**

10.2.6.12. UART Scratch Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: UART_SCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

10.2.6.13. UART Status Register(Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full

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			1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

10.2.6.14. UART Transmit FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

10.2.6.15. UART Receive FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

10.2.6.16. UART DMA Handshake Configuration Register(Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: UART_HSK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xE5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

10.2.6.17. UART Halt TX Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTE The sending of TX_REQ.

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			In DMA1 mode (FIFO on), if PTE is set to 1, when TFL is less than trig, send the DMA request. If PTE is set to 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set to 1 and FIFO is on, when TFL is less than trig, send DMA request. If PTE is set to 1 and FIFO is off, when THRE is empty, send DMA request. If PTE is set to 0, when FIFO is empty, send DMA request.
6	R/W	0x0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, if DMA_PTE_RX is 1 and FIFO is on, when RFL is more than trig, send DRQ. In other cases, once the receive data is valid, send DRQ.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user uses HALT[1] to change the baud rate or LCR configuration, write 1 to update the configuration and wait this bit self clear to 0 to finish update process. Writing 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baud rate register (DLH and DLL) when the UART is busy. 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled  **NOTE** **If FIFOs are not enabled, the setting has no effect on operation.**

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10.2.6.18. UART DBG DLL Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: UART_DBG_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLL

10.2.6.19. UART DBG DLH Register(Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: UART_DBG_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLH

10.2.6.20. UART RS485 Control and Status Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: UART_485_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	Reserved
6	R/W1C	0x0	AAD_ADDR_F In AAD mode, when UART receives an address byte and the byte is the same as RS485_ADDR_MATCH, this bit will be set to 1.If RS485 interrupt is enabled, the RS485 interrupt will arrive. Write 1 to clear this bit and reset the RS485 interrupt.
5	R/W1C	0x0	RS485_ADDR_DET_F This is a flag of the detecting of address bytes. When UART receives an address byte, this bit will be set to 1.If the RS485 Interrupt is enabled, the RS485 interrupt will arrive. 1:An address byte is detected 0:No address byte is detected Write 1 to clear this bit and reset the RS485 interrupt.
4	/	/	/
3	R/W	0x0	RX_BF_ADDR In NMM mode, If setting this bit to 1, UART will receive all the bytes into FIFO before receiving an address byte. If setting to 0, it will not. 1:Receive 0:Not Receive
2	R/W	0x0	RX_AF_ADDR In NMM mode, if setting this bit to 1, UART will receive all the bytes into FIFO after receiving an address byte. If setting to 0, it will not. 1:Receive 0:Not Receive

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1:0	R/W	0x0	RS485_SLAVE_MODE_SEL RS485 Slave Mode 00: Normal Multidrop Operation(NMM) 01: Auto Address Detection Operation(AAD) 10: Reserved 11: Reserved

10.2.6.21. UART RS485 Address Match Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: RS485_ADDR_MATCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	ADDR_MATCH The matching address uses in AAD mode. **NOTE** **It is only available for AAD.**

10.2.6.22. UART RS485 Bus Idle Check Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: BUS_IDLE_CHK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	BUS_IDLE_CHK_EN 0: Disable bus idle check function 1: Enable bus idle check function
6	R	0x0	BUS_STATUS The Flag of Bus Status 0:Idle 1:Busy
5:0	R	0x0	ADJ_TIME Bus Idle Time The unit is 8*16*Tclk.

10.2.6.23. UART TX Delay Register(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: TX_DLY
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLY The delay time between the last stop bit and the next start bit. The unit is 16*Tclk. It is used to control the space between two bytes in TX.

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10.3. RSB

10.3.1. Overview

The RSB(reduced serial bus) Host Controller is designed to communicate with RSB Device using two push-pull wires. It supports a simplified two wire protocol on a push-pull bus. The transfer speed can be up to 20MHz and the performance will be improved much. The RSB bus protocol is designed and implemented by the Allwinner Technology. Allwinner technology has the final interpretation of the IP.

The RSB has the following features:

- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Speed up to 20MHz with ultra low power
- Push-Pull bus
- Supports host mode
- Programmable output delay of CD signal
- Parity check for address and data transmission
- Supports multi-devices

10.3.2. Block Diagram

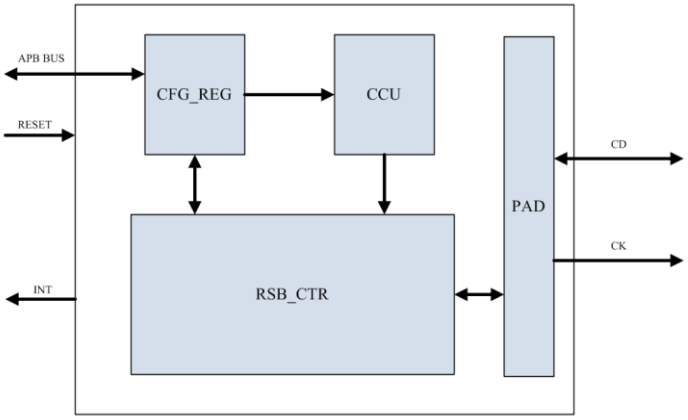

Figure 10- 13. RSB Block Diagram

RESET: Module reset signal
INT: Module output interrupt signal
CFG_REG: Module configuration register
RSB_CTR: Packet encoding/decoding
CCU: Module clock controller unit

For complete RSB information, refer to the ***Allwinner T7 RSB Specification***.

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10.4. SPI

10.4.1. Overview

The SPI is a full-duplex, synchronous, serial communication interface which allows rapid data communication with software interrupts. The SPI controller contains one 64x8 bits receiver buffer (RXFIFO) and one 64x8 bits transmit buffer (TXFIFO). It can work at master mode and slave mode.

The SPI has the following features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports mode0, mode1, mode2 and mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 0 bit to 32 bits
- Supports the SPI NAND flash and SPI NOR flash
- Supports standard SPI,dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI

10.4.2. Block Diagram

Figure 10-14 shows a block diagram of the SPI.

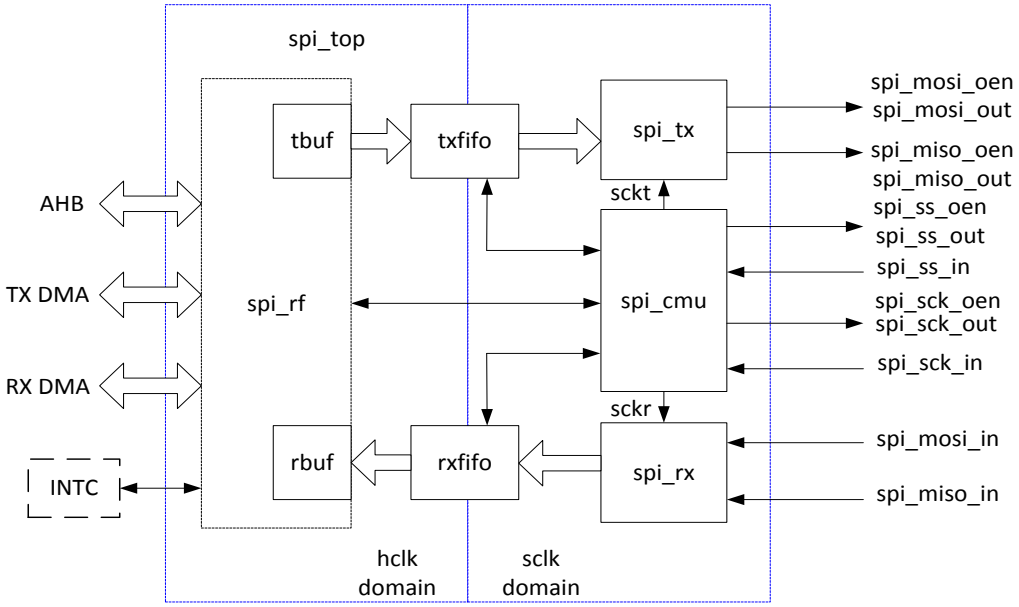

Figure 10- 14. SPI Block Diagram

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The SPI comprises with:
spi_rf: Responsible for implementing the internal register, interrupt and DMA Request.
spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8bits,then the data is written into the rxfifo.
spi_rbuf: The block is used to convert the rxfifo data into read data length of AHB.
txfifo, rxfifo: For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the txfifo; data received from the external serial device into SPI is pushed into the rxfifo.
spi_cmu: Responsible for implementing SPI bus clock, chip select, internal sample and the generation of transfer clock.
spi_tx: Responsible for implementing SPI data transfer ,the interface of the internal txfifo and status register.
spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

10.4.3. Operations and Functional Descriptions

10.4.3.1. External Signals

Table 10-8 describes the external signals of SPI. MOSI and MISO are bidirectional I/O, when SPI is configured as master device, CLK and CS are output pin; when SPI is configurable as slave device, CLK and CS are input pin. The unused SPI ports are used as General Purpose I/O ports.

Table 10- 8. SPI External Signals

Signal	Description	Type
SPI0_CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0_WP	Write protection and active low or Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0_HOLD	The HOLD pin is used to temporarily pause serial communication without deselecting or resetting the device. While the HOLD pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, or Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1_CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
S_SPI_CS	SPI Chip Select Signal, Low Active	I/O
S_SPI_CLK	SPI Clock Signal	I/O
S_SPI_MOSI	SPI Master Data Out, Slave Data In	I/O
S_SPI_MISO	SPI Master Data In, Slave Data Out	I/O

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10.4.3.2. Clock Sources

The SPI0 and SPI1 controller get 5 different clock sources, the S_SPI has 7 different clock sources, users can select one of them to make SPI clock source. Table 10-9 describes the clock sources for SPI.

Table 10- 9. SPI Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1200MHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1200MHz
RC_16M	RC Clock,only for S_SPI, default value is 16MHz
LOSC	32KHz Crystal,only for S_SPI

10.4.3.3. Typical Application

Figure 10-15 shows the application block diagram when the SPI master device is connected to a slave device.

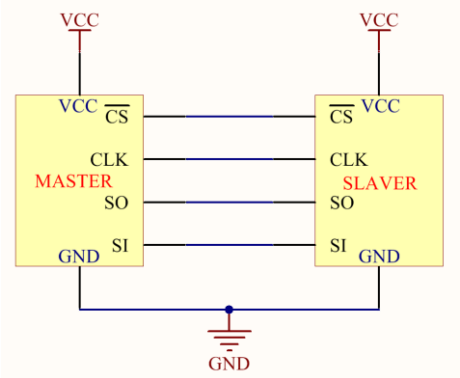

Figure 10- 15. SPI Application Block Diagram

10.4.3.4. SPI Transmit Format

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and

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is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 10-10.

Table 10- 10. SPI Transmit Format

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 10-16 and Figure 10-17 describe four waveforms for SPI_SCLK.

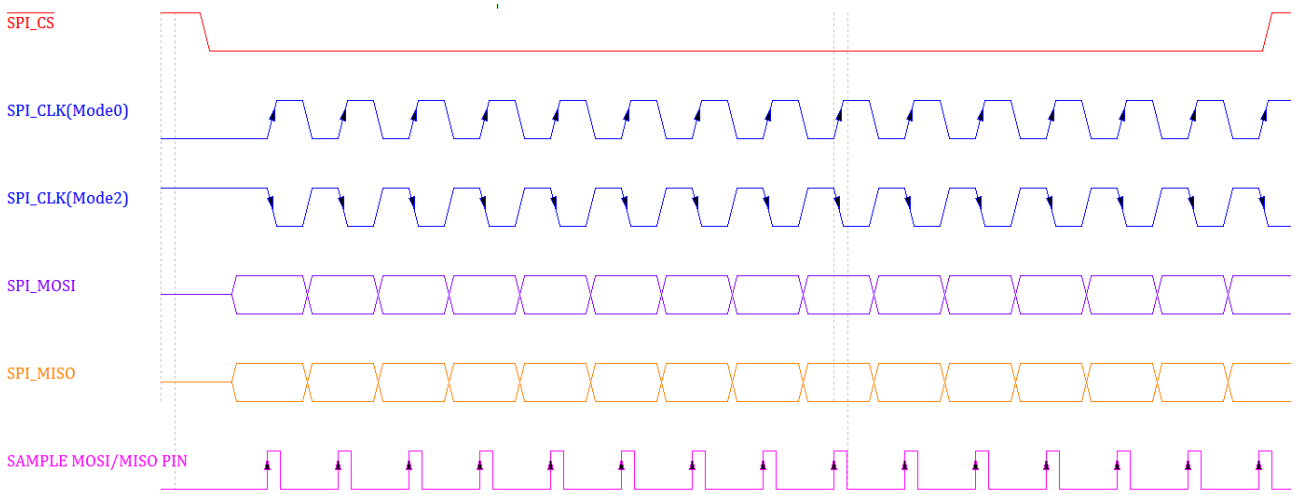

Figure 10- 16. SPI Phase 0 Timing Diagram

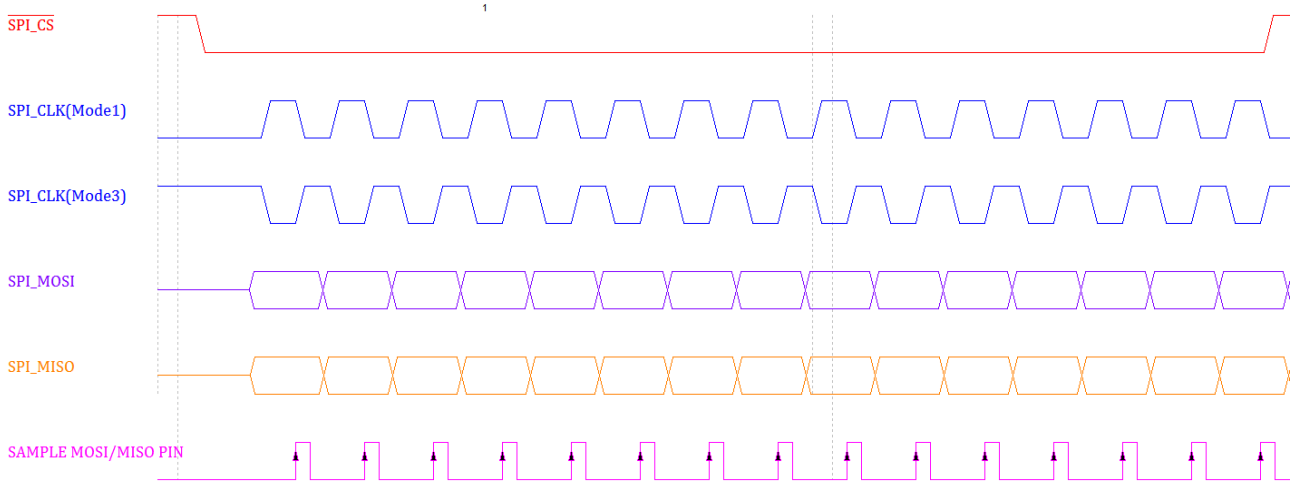

Figure 10- 17. SPI Phase 1 Timing Diagram

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10.4.3.5. SPI Master and Slave Mode

The SPI controller can be configured to a master or slave device. Master mode is selected by setting the **MODE** bit in the **SPI Global Control Register;** slave mode is selected by clearing the the **MODE** bit in the **SPI Global Control Register**.

In master mode, SPI_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received. SPI_SS can be selected SPI auto control or software manual control. When using auto control, **SS_OWNER**(the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control, **SS_OWNER** must be set, Chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In slave mode, after software selects the **MODE** bit to '0',it waits for master initiate a transaction. When the master assertes SPI_SS and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

10.4.3.6. SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the **Work Mode Select(bit[1:0])** is equal to 0x2 in the **SPI Bit-Aligned Transfer Configure Register**. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes this mode.

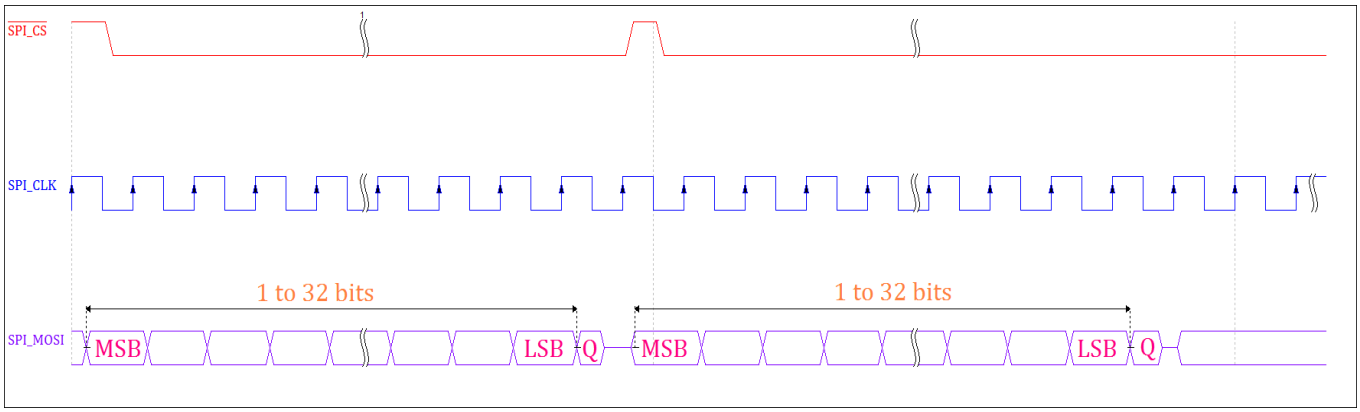

Figure 10- 18. SPI 3-Wire Mode

10.4.3.7. SPI Dual-Input/Dual-Output and Dual I/O Mode

The dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode SPI devices, data can be read at fast speed using two data bits(MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI(Figure 10-19) and the dual I/O SPI(Figure 10-20).

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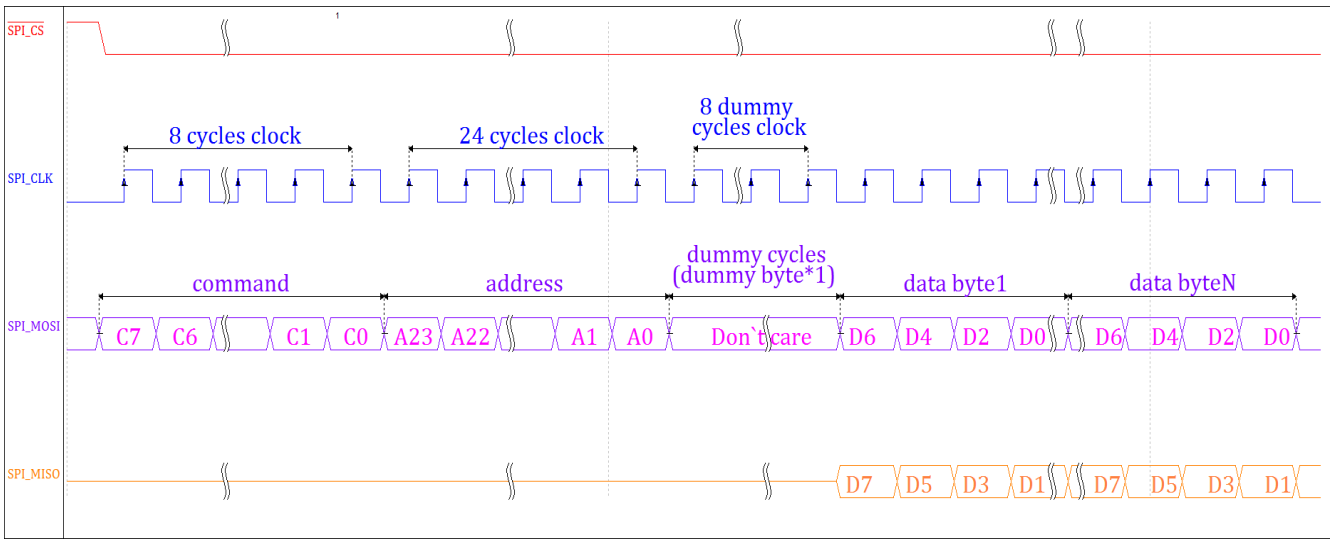

Figure 10- 19. SPI Dual-Input/Dual-Output Mode

In the dual-input/dual-output SPI, the command, address, and the dummy bytes output in unit of a single bit in serial mode through SPI_MOSI line, only the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

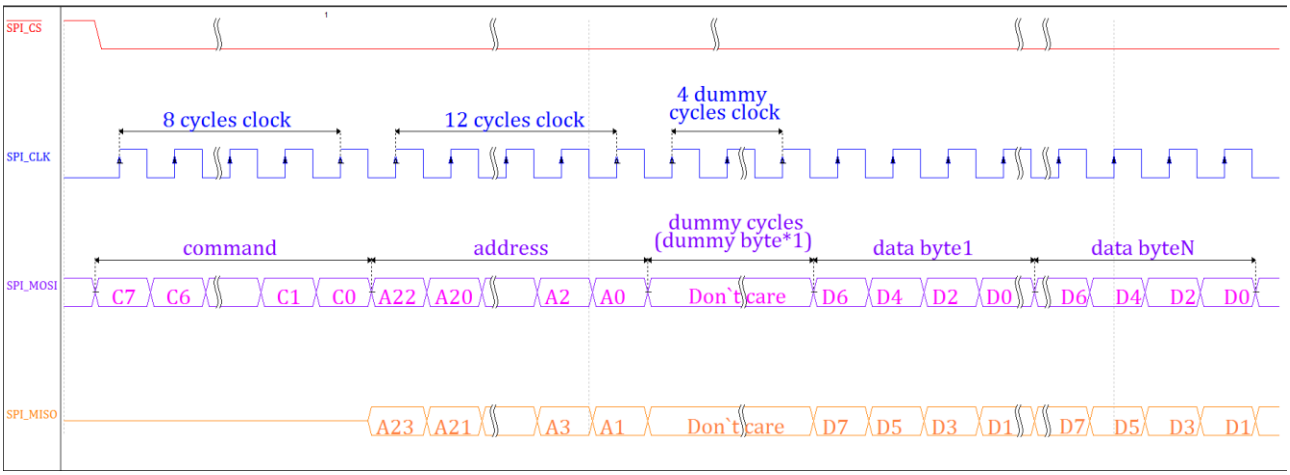

Figure 10- 20. SPI Dual I/O Mode

In the dual I/O SPI, only the command bytes are output in unit of a single bit in serial mode through SPI_MOSI line. The address bytes and the dummy bytes are output in unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

10.4.3.8. SPI Quad-Input/Quad-Output Mode

The quad read mode(SPI x4) is selected when the **Quad_EN**(bit29) is set in the **SPI Master Burst Control Counter Register**. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits(MOSI, MISO, IO2(WP#)and IO3(HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

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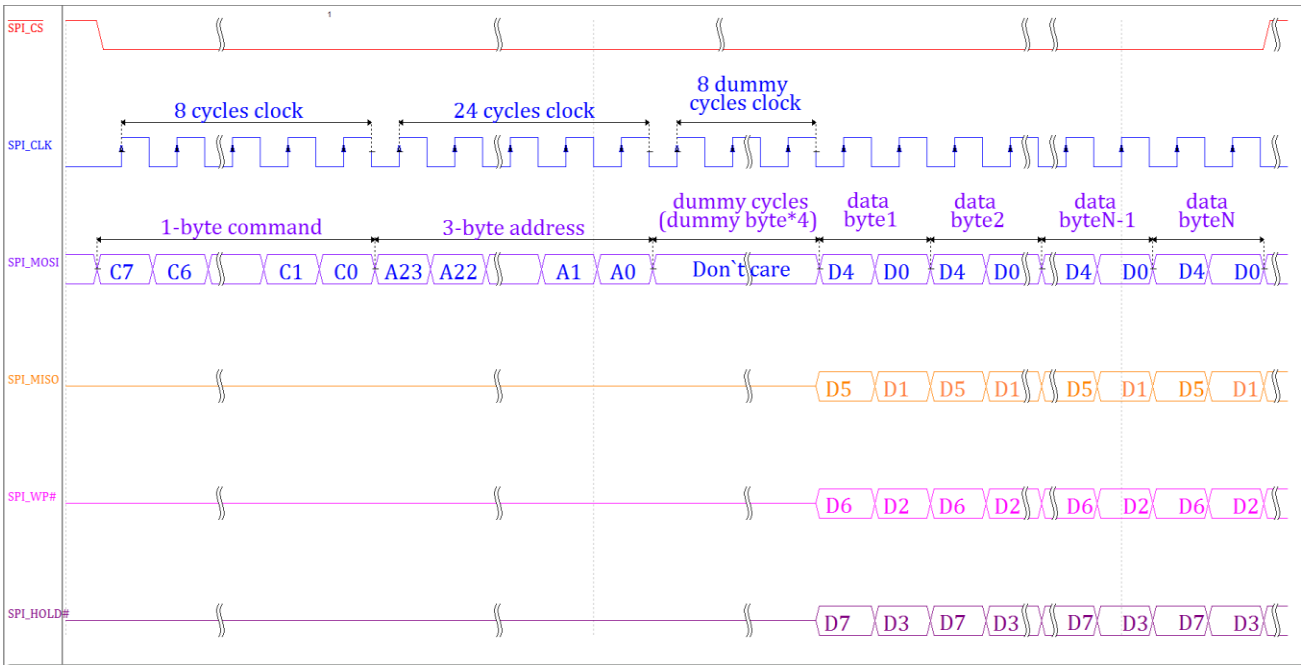

Figure 10- 21. SPI Quad-Input/Quad-Output Mode

In the quad-input/quad-output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output(write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

10.4.4. Programming Guidelines

10.4.4.1. CPU or DMA Operation

The SPI transfers serial data between the processor and external device. CPU and DMA are the two main operational modes for SPI. For each SPI, data is simultaneously transmitted(shifted out serially) and received (shifted in serially).SPI has 2 channels, TX channel and RX channel. TX channel has the path from TX FIFO to external device. RX channel has the path from external device to RX FIFO.

Write Data: CPU or DMA must write data on the register SPI_TXD, data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO,CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends an completed interrupt(the TC bit in SPI Interrupt Status Register) to the processor at the end of each transfer.

(1).CPU Mode

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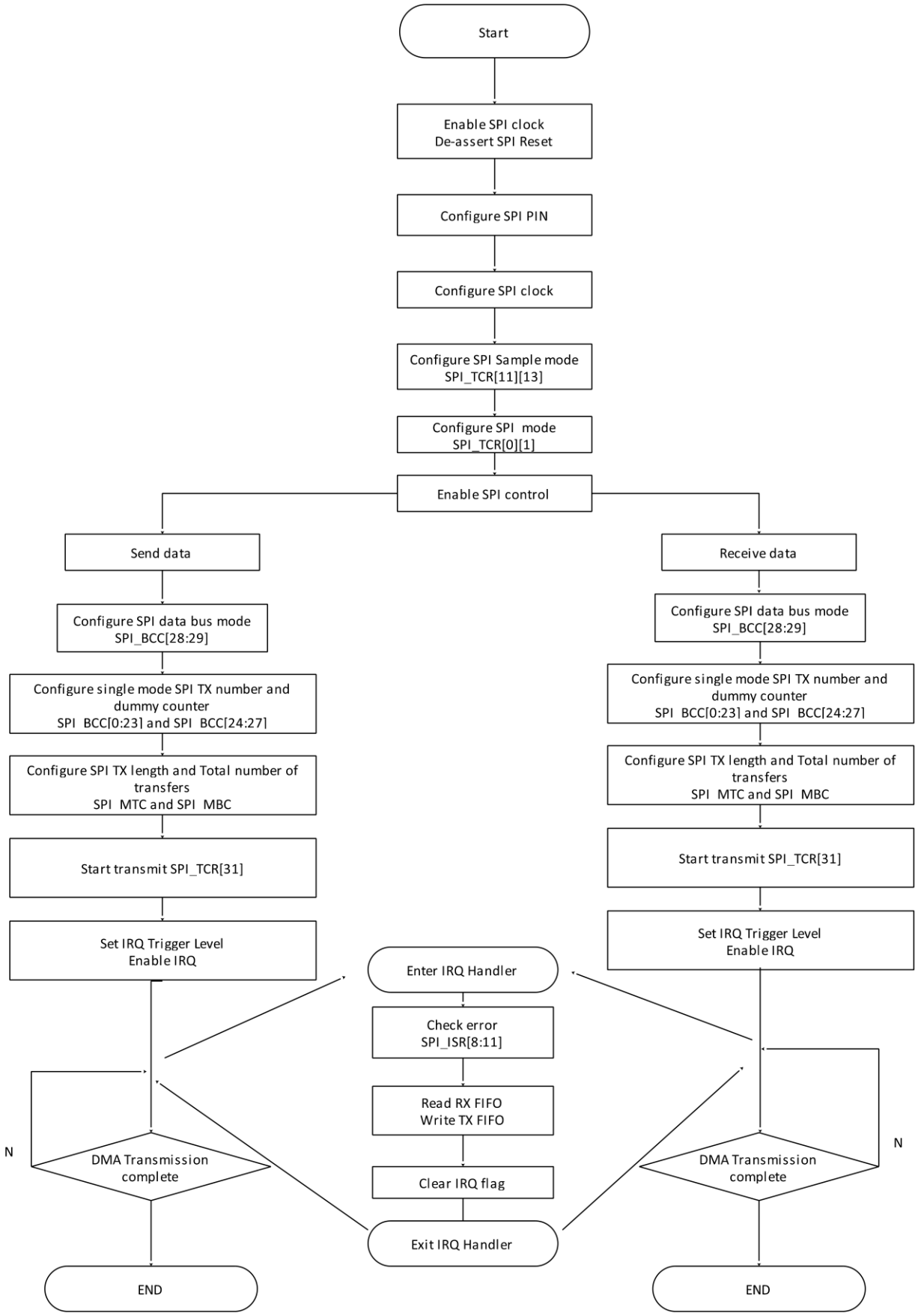

Figure 10- 22. SPI Write/Read Data in CPU Mode

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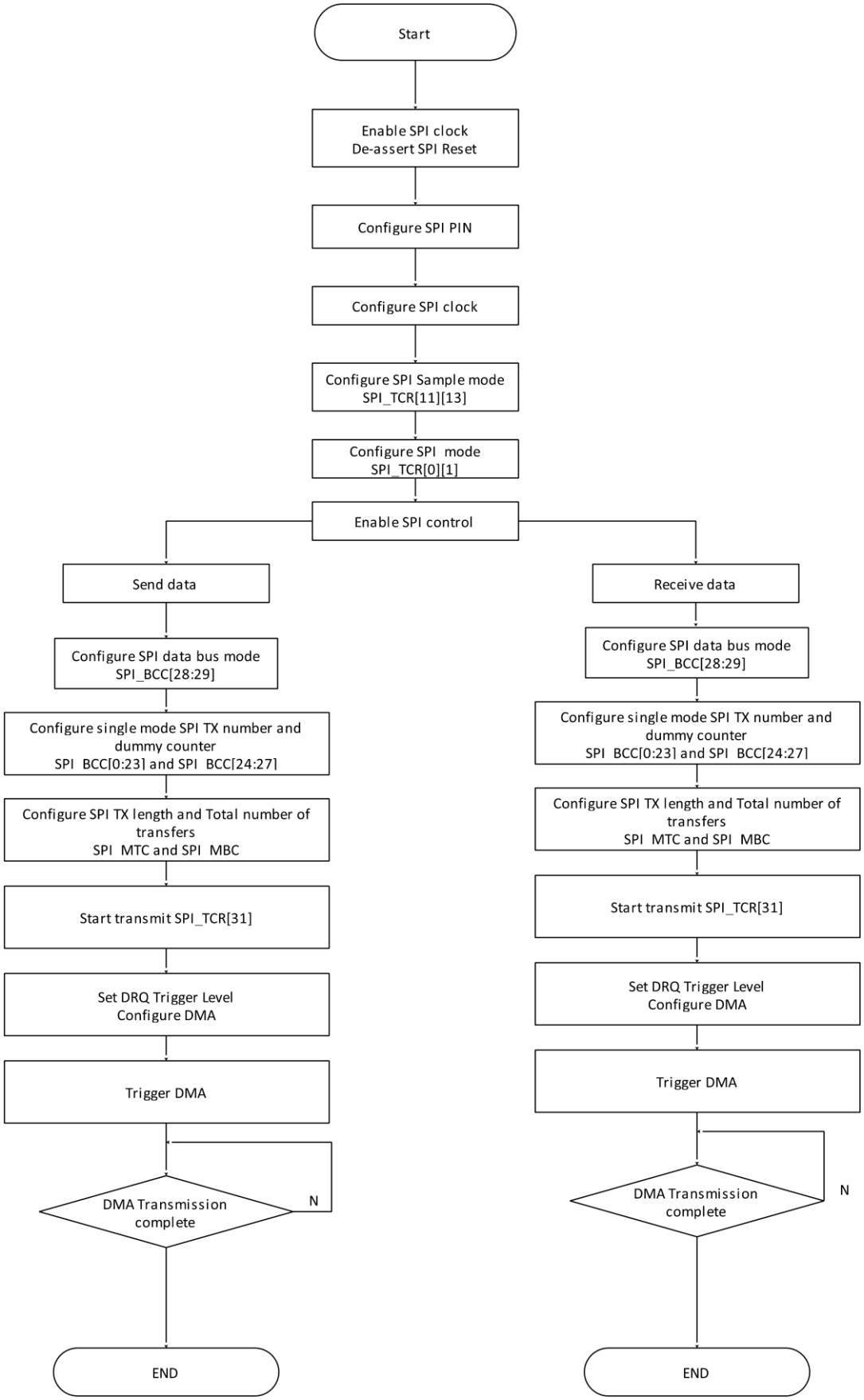

Figure 10- 23. SPI Write/Read Data in DMA Mode

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10.4.4.2. Transmit/Receive Burst in Master Mode

In SPI master mode, the transmit and receive burst(byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmit bursts are written in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** The transmit bursts in single mode before automatically sending dummy burst are written in STC(bit[23:0]) of **SPI Master Burst Control Counter Register.** For dummy data, SPI controller can automatically sent before receiving by writing DBC(bit[27:24]) in **SPI Master Burst Control Counter Register**. If users donot use SPI controller to sent dummy data automatically, then the dummy bursts are used as the transmit counters to write together in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** In master mode, the total burst numbers are written in MBC(bit[23:0]) of **SPI Master Burst Counter Register.** When all transmit burst and receive burst are transferred, SPI controller will send an completed interrupt, at the same time, SPI controller will clear DBC,MWTC and MBC.

10.4.4.3. SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3 kHz~100 MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in master mode. The SPI clock is selected different clock sources, SPI must configure different work mode. There are three work mode: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. When SPI runs at 40 MHz or below 40 MHz, SPI can work at normal sample mode or delay half cycle sample mode. When SPI runs over 60 MHz,setting the **SDC** bit in **SPI Transfer Control Register** to '1' makes the internal read sample point with a half cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. The different configuration of SPI sample mode shows in Table 10-11.

Table 10- 11. SPI Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24MHz
delay half cycle sample	0	0	<=40MHz
delay one cycle sample	0	1	>=60MHz

10.4.4.4. SPI Error Conditions

If any error conditions occur, hardware will set the corresponding status bits in the **SPI Interrupt Status Register** and stop the transfer. For the SPI controller, the following error scenarios can happen:

(1) TX_FIFO Underrun

TX_FIFO underrun happens when the CPU/DMA reads from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_UDF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

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(2) TX_FIFO Overflow

TX_FIFO overflow happens when the CPU/DMA writes into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_OVF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(3) RX_FIFO Underrun

RX_FIFO underrun happens when the CPU/DMA reads from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_UDF bit. To start a new transaction, software has to reset the fifo by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(4) RX_FIFO Overflow

RX_FIFO overflow happens when the CPU/DMA writes into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_OVF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

10.4.5. Register List

Module Name	Base Address
SPI0	0x05010000
SPI1	0x05011000
R_SPI	0x07013000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control Register
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Counter Register
SPI_CCR	0x0024	SPI Clock Rate Control Register
SPI_MBC	0x0030	SPI Burst Counter Register
SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control Register
SPI_BATCR	0x003C	SPI Bit-Aligned Transfer Configure Register

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SPI_3W_CCR	0x0040	SPI 3Wire Clock Configuration Register
SPI_TBR	0x0044	SPI TX Bit Register
SPI_RBR	0x0048	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

10.4.6. Register Description

10.4.6.1. SPI Global Control Register(Default Value: 0x0000_0080)

Offset:0x0004			**Register Name: SPI_GCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes. Writing '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 0: Normal operation, ignore RXFIFO status 1: Stop transmit data when RXFIFO full Cannot be written when XCH=1
6:2	/	/	/
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave mode 1: Master mode Cannot be written when XCH=1
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable After transforming from bit_mode to byte_mode, it must enable the SPI module again.

10.4.6.2. SPI Transfer Control Register(Default Value: 0x0000_0087)

Offset: 0x0008	**Register Name: SPI_TCR**

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Bit	Read/Write	Default/Hex	Description
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Writing “1” to SRST will also clear this bit. Writing ‘0’ to this bit has no effect. Cannot be written when XCH=1.
30:15	/	/	/
14	R/W	0x0	SDDM Sending Data Delay Mode 0:Normal sending 1:Delay sending Set the bit to "1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay sample mode 1: Normal sample mode In normal sample mode, SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Cannot be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point Cannot be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select Select rapid mode for high speed write. 0: Normal write mode 1: Rapid write mode Cannot be written when XCH=1.
9	R/W	0x0	DDB

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			Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Cannot be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Cannot be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Cannot be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Cannot be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Cannot be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Cannot be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
1	R/W	0x1	CPOL

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			SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Cannot be written when XCH=1.

10.4.6.3. SPI Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip select signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable

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			1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

10.4.6.4. SPI Interrupt Status Register(Default Value: 0x0000_0032)

Offset: 0x0014			**Register Name: SPI_ISR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer completed
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun

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			1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available 1: RXFIFO is overflowed
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. TX_WL is the water level of TXFIFO.
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY

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			RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. RX_WL is the water level of RXFIFO.

10.4.6.5. SPI FIFO Control Register(Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, writing to ‘0’ has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable **NOTE** **In normal mode, TX FIFO can only be read by SPI controller, writing ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.**
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, writing ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable **NOTE** **In normal mode, RX FIFO can only be written by SPI controller, writing ‘1’ to this bit will switch RX FIFO read and write function to AHB bus. This bit is**

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			used to test the RX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

10.4.6.6. SPI FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SPI_FSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64: 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

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10.4.6.7. SPI Wait Clock Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). Cannot be written when XCH=1. 0: No wait states inserted n: n SPI_SCLK wait states inserted **NOTE** **These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer.**
15:0	R/W	0x0	WCC Wait Clock Counter (In master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

10.4.6.8. SPI Clock Control Register(Default Value: 0x0000_0002)

Offset: 0x0024			Register Name: SPI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0x0	CDR1_M Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2^CDR1_M).
7:0	R/W	0x2	CDR2_N Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR2_N + 1)).

10.4.6.9. SPI Master Burst Counter Register(Default Value: 0x0000_0000)

Offset: 0x0030	Register Name: SPI_MBC

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Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts **NOTE** **Total transfer data, include the TXD, RXD and dummy burst.**

10.4.6.10. SPI Master Transmit Counter Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

10.4.6.11. SPI Master Burst Control Counter Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable **NOTE** **Quad mode includes Quad-Input and Quad-Output.**
28	R/W	0x0	DRM Master Dual Mode RX Enable

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			0: RX use single-bit mode 1: RX use dual mode Cannot be written when XCH=1; It is only valid when Quad_Mode_EN=0.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data does not care by the device. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1

10.4.6.12. SPI Bit-Aligned Transfer Configure Register(Default Value: 0x0000_00A0)

Offset: 0x0040			Register Name: SPI_BATC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when ***Work Mode Select==0x10/0x11.*** 0: Idle 1: Initiates transfer Writing “1” to this bit will start to transfer serial bits frame(the value comes from the ***SPI TX Bit Register*** or ***SPI RX Bit Register***), and will auto clear after the bursts transfer completely. Writing ‘0’ to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Delay Sample Mode 1: Standard Sample Mode In Standard Sample Mode, SPI master samples the data at the standard rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.

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29:26	/	/	
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in ***SPI TX Bit Register****(or* ***SPI RX Bit Register****)* has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed It is only valid when ***Work Mode Select==0x10/0x11.***
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when ***Work Mode Select==0x10/0x11.***
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
15:14	/	/	/
13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually , set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller

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			1: Software It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when ***Work Mode Select= =0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in standard SPI, dual-output/dual input SPI, dual IO SPI and quad-output/quad-input SPI. 01: Reserved 10: Data frame is bit aligned in 3-wire SPI 11: Data frame is bit aligned in standard SPI

10.4.6.13. SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: SPI_BA_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)).

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

10.4.6.14. SPI TX Bit Register(Default Value: 0x0000_0000)

Offset: 0x0048			**Register Name: SPI_TBR**
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

10.4.6.15. SPI RX Bit Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

10.4.6.16. SPI Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	Delay Cycles The counts of hold cycles from DMA last signal high to dma_active high

10.4.6.17. SPI TX Data Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte

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			accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **NOTE** **This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

10.4.6.18. SPI RX Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **NOTE** **This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

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10.5. USB2.0 OTG

10.5.1. Overview

The USB2.0 OTG is a dual-role device controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB2.0 Specification. It can support high-speed (HS, 480 Mbit/s), full-speed (FS, 12 Mbit/s), and low-speed (LS, 1.5 Mbit/s) transfers in Host mode. It can support high-speed (HS, 480 Mbit/s), and full-speed (FS, 12 Mbit/s) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

The USB2.0 OTG has the following features:

- Complies with USB2.0 Specification
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) in Host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 10 User-Configurable Endpoints for Bulk, Isochronousl and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
- Supports up to (8KB+64Bytes) FIFO for EPs (including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every EPs

10.5.2. Block Diagram

Figure 10-24 shows the block diagram of USB2.0 OTG Controller.

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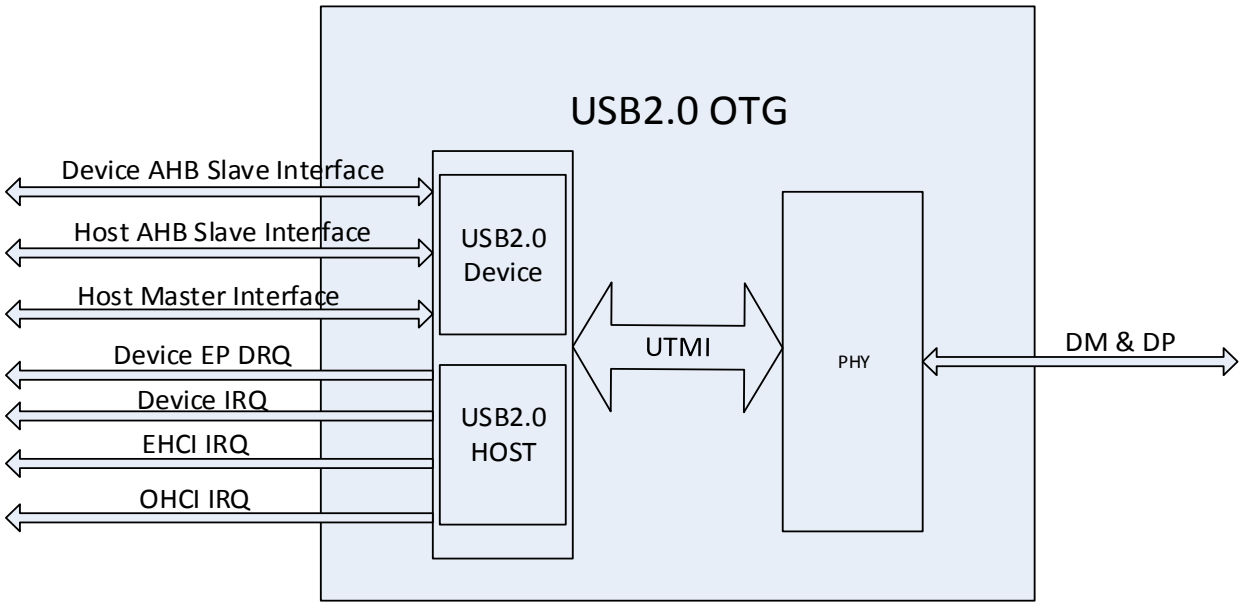

Figure 10- 24. USB2.0 OTG Controller Block Diagram

10.5.3. External Signals

Table 10- 12. USB2.0 OTG External Signals

Signal	Description	Type
USB0-DP	USB2.0 OTG differential signal postive	AI/O
USB0-DM	USB2.0 OTG differential signal negative	AI/O

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10.6. USB2.0 Host Controller

10.6.1. Overview

The USB2.0 Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480 Mbit/s transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

The USB2.0 Host Controller has the following features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports 32-bit Little endian AMBA AHB Slave Bus for register access
- Supports 32-bit Little endian AMBA AHB Master Bus for memory access
- Including an internal DMA controller for data transfer with memory
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) device
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports only 1 USB root port shared between EHCI and OHCI

10.6.2. Block Diagram

Figure 10-25 shows the block diagram of USB2.0 Host Controller.

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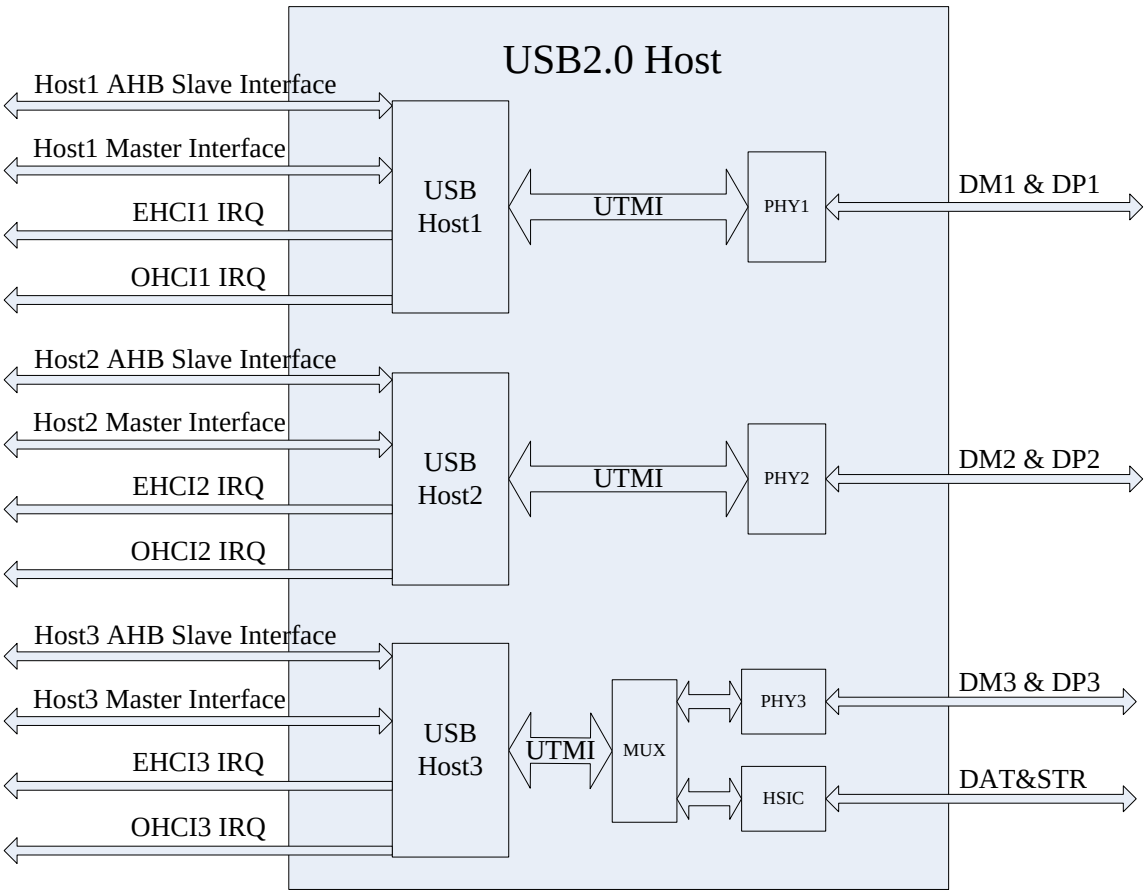

Figure 10- 25. USB2.0 Host Controller Block Diagram

10.6.3. Operations and Functional Descriptions

10.6.3.1. External Signals

Table 10- 13. USB2.0 Host External Signals

Signal	Description	Type
USB1-DP	USB2.0 Host differential signal postive	AI/O
USB1-DM	USB2.0 Host differential signal negative	AI/O
USB2-DP	USB2.0 Host differential signal postive	AI/O
USB2-DM	USB2.0 Host differential signal negative	AI/O
USB3-DP	USB2.0 Host differential signal postive	AI/O
USB3-DM	USB2.0 Host differential signal negative	AI/O
VDD-USB	1.1V USB power supply	P
VCC3V3-USB	3.3V USB power supply	P
HSIC-STR	HSIC strobe	AI/O
HSIC-DAT	HSIC data	AI/O
VCC-HSIC	HSIC power supply	P

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10.6.3.2. Clock and Reset

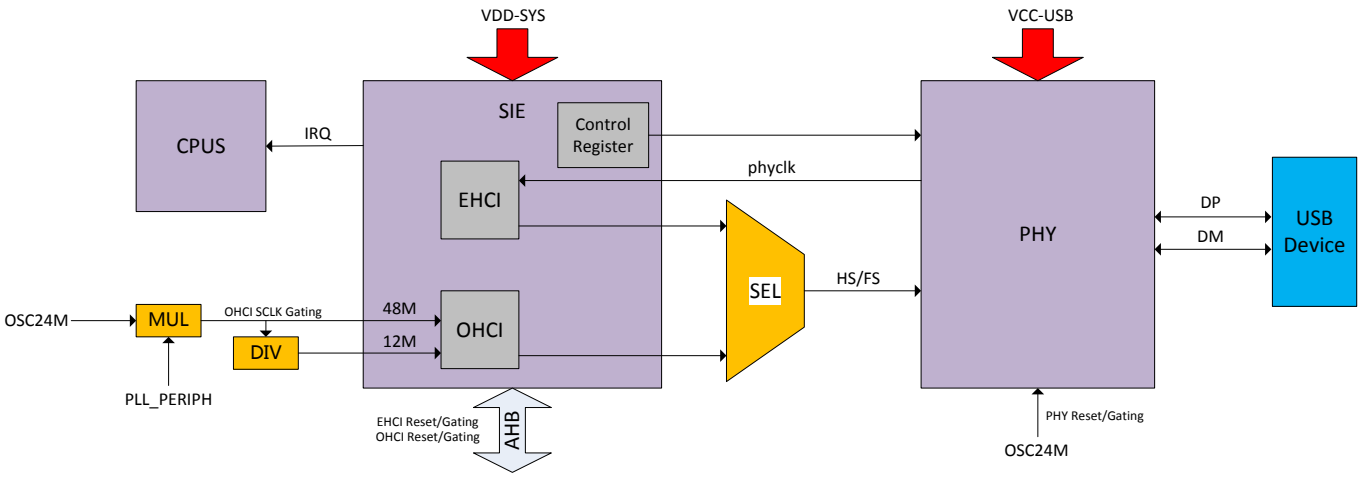

Figure 10- 26. USB2.0 Host Clock Description

10.6.3.3. Function Implementation

Please refer to USB2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

10.6.4. Register List

Module Name	Base Address
USB2.0_HOST1	0x05200000
USB2.0_HOST2	0x05310000
USB2.0_HOST3	0x05311000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x000	EHCI Capability Register Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x00C	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register

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E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x400	OHCI Revision Register
O_HcControl	0x404	OHCI Control Register
O_HcCommandStatus	0x408	OHCI Command Status Register
O_HcInterruptStatus	0x40C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x418	OHCI HCCA Base
O_HcPeriodCurrentED	0x41C	OHCI Period Current ED Base
O_HcControlHeadED	0x420	OHCI Control Head ED Base
O_HcControlCurrentED	0x424	OHCI Control Current ED Base
O_HcBulkHeadED	0x428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x42C	OHCI Bulk Current ED Base
O_HcDoneHead	0x430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x434	OHCI Frame Interval Register
O_HcFmRemaining	0x438	OHCI Frame Remaining Register
O_HcFmNumber	0x43C	OHCI Frame Number Register
O_HcPerioddicStart	0x440	OHCI Periodic Start Register
O_HcLSThreshold	0x444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x44C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x454	OHCI Root Hub Port Status Register
HCI Controller and PHY Interface Register		
HCI Interface	0x800	HCI Interface Register
PHY Control	0x810	PHY Control Register
HSIC PHY tune1	0x81C	HSIC PHY Tune1 Register
HSIC PHY tune2	0x820	HSIC PHY Tune2 Register
HSIC PHY tune3	0x824	HSIC PHY Tune3 Register
HCI SIE Port Disable Control	0x828	HCI SIE Port Disable Control Register

10.6.5. EHCI Register Description

10.6.5.1. EHCI Identification Register(Default Value:0x10)

Offset:0x0000	Register Name: CAPLENGTH

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Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

10.6.5.2. EHCI Host Interface Version Number Register(Default Value:0x0100)

Offset: 0x0002			Register Name: HCIVERSION
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R	0x0100	HCIVERSION This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

10.6.5.3. EHCI Host Control Structural Parameter Register(Default Value:0x0000_0001)

Offset: 0x0004			Register Name: HCSPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R	0x0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	0x0	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0x0	Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0x0	Port Routing Rules This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value: 0 — Meaning: The first N_PCC ports are routed to the lowest numbered

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			<table><tr><td></td><td>function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td></tr><tr><td>1</td><td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td></tr></table> This field will always be '0'.
6:4	/	/	/
3:0	R	0x1	N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

10.6.5.4. EHCI Host Control Capability Parameter Register(Default Value:0x0000_0000)

Offset: 0x0008			**Register Name: HCCPARAMS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R	0x0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R	0x0	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	0x0	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R	0x0	Programmable Frame List Flag

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			If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

10.6.5.5. EHCI Companion Port Route Description(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: HCSP-PORTROUTE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

10.6.5.6. EHCI USB Command Register(Default Value:0x0008_0000)

Offset: 0x0010			Register Name: USBCMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x08	Interrupt Threshold Control The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below: Value | Minimum Interrupt Interval 0x00 | Reserved 0x01 | 1 micro-frame 0x02 | 2 micro-frame 0x04 | 4 micro-frame

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			<table><tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr><tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr><tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr><tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr></table>Any other value in this register yields undefined results. The default value in this field is 0x08 . Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.
15:12	/	/	/
11	R	0x0	Asynchronous Schedule Park Mode Enable(OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.
10	/	/	/
9:8	R	0x0	Asynchronous Schedule Park Mode Count(OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0x0	Light Host Controller Reset(OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host
6	R/W	0x0	Interrupt on Async Advance Doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft- Ware must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a zero after it has set the Interrupt on

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<table>
<tr><td></td><td></td><td></td><td>Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0x0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr><tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0x0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:<table><tr><td>Bit Value</td><td>Meaning</td></tr><tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr><tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr></table>The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W</td><td>0x0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the
Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:<table><tr><td>Bits</td><td>Meaning</td></tr><tr><td>00b</td><td>1024 elements(4096 bytes),default value</td></tr><tr><td>01b</td><td>512 elements(2048 byts)</td></tr><tr><td>10b</td><td>256 elements(1024 bytes)for resource-constrained condition</td></tr><tr><td>11b</td><td>reserved</td></tr></table>The default value is ‘00b’.</td></tr>
<tr><td>1</td><td>R/W</td><td>0x0</td><td>Host Controller Reset
This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.
When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.
All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state.
This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a</td></tr>
</table>

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			zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0x0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

10.6.5.7. EHCI USB Status Register(Default Value:0x0000_1000)

Offset: 0x0014			**Register Name: USBSTS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0x0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware

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			(e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0x0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0x0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

10.6.5.8. EHCI USB Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0018	Register Name: USBINTR

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Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0x0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

10.6.5.9. EHCI Frame Index Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: FRINDEX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11

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			10b	256	10	
			11b	Reserved		

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

10.6.5.10. EHCI Periodic Frame List Base Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: PERIODICLISTBASE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

NOTE

Writes must be Dword Writes.

10.6.5.11. EHCI Current Asynchronous List Address Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: ASYNCLISTADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	R/W	0x0	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

10.6.5.12. EHCI Configure Flag Register(Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CONFIGFLAG
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:1	/	/	/
0	R/W	0x0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follows: Value: 0 – Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 – Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

NOTE

This register is not used in the normal implementation.

10.6.5.13. EHCI Port Status and Control Register(Default Value:0x0000_2000)

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	Wake on Disconnect Enable(WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0x0	Wake on Connect Enable(WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0x0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follows: 0000b: The port is NOT operating in a test mode. 0001b: Test J_STATE 0010b: Test K_STATE 0011b: Test SE0_NAK 0100b: Test Packet 0101b: Test FORCE_ENABLE 0110b-1111b: Reserved The default value in this field is '0000b'.

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<table>
<tr><td>15:14</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>13</td><td>R/W</td><td>0x1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>11:10</td><td>R</td><td>0x0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:
<table>
<tr><td>Bit[11:10]</td><td>USB State</td><td>Interpretation</td></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td></tr>
<tr><td>9</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>8</td><td>R/W</td><td>0x0</td><td>Port Reset
0: Port is not in Reset
1: Port is in Reset
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes.
  NOTE
When software writes this bit to a one , it must also write a zero to the Port Enable bit.

Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is</td></tr>
</table>

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<table>
<tr><td></td><td></td><td></td><td>complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0x0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table><tr><td>Bits[Port Enables, Suspend]</td><td>Port State</td></tr><tr><td>0x</td><td>Disable</td></tr><tr><td>10</td><td>Enable</td></tr><tr><td>11</td><td>Suspend</td></tr></table>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
① Software sets the Force Port Resume bit to a zero(from a one).
② Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>6</td><td>R/W</td><td>0x0</td><td>Force Port Resume
0: No resume (K-state) detected/ driven on port
1: Resume detected/driven on port
This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined.
Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit.</td></tr>
</table>

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			Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/W1C	0x0	Over-current Change This bit is set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	Over-current Active 0: This port does not have an over-current condition 1: This port currently has an over-current condition This bit will automatically transition from a one to a zero when the over current condition is removed.
3	R/W1C	0x0	Port Enable/Disable Change 0: No change 1: Port enabled/disabled status has changed For the root hub, this bit is set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the **USB Specification** for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	Port Enabled/Disabled 0: Disable 1: Enable Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. This field is zero if Port Power is zero.
1	R/WC	0x0	Connect Status Change 1: Change in Current Connect Status 0: No change. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status,

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			even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be “setting” an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

NOTE

This register is only reset by hardware or in response to a host controller reset.

10.6.6. OHCI Register Description

10.6.6.1. HcRevision Register(Default Value:0x10)

Offset: 0x0400				Register Name: HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	/	/	/	/
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

10.6.6.2. HcControl Register(Default Value:0x0000_0000)

Offset: 0x0404				Register Name: HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in *HcInterruptStatus* is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected

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<table>
<tr><td></td><td></td><td></td><td></td><td>This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.</td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>InterruptRouting
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</td></tr>
<tr><td>7:6</td><td>R/W</td><td>R/W</td><td>0x0</td><td>HostControllerFunctionalState for USB
<table><tr><td>00b</td><td>USBReset</td></tr><tr><td>01b</td><td>USBResume</td></tr><tr><td>10b</td><td>USBOperational</td></tr><tr><td>11b</td><td>USBSuspend</td></tr></table>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus.
This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port.
HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.</td></tr>
<tr><td>5</td><td>R/W</td><td>R</td><td>0x0</td><td>BulkListEnable
This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>4</td><td>R/W</td><td>R</td><td>0x0</td><td>ControlListEnable
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.</td></tr>
<tr><td>3</td><td>R/W</td><td>R</td><td>0x0</td><td>IsochronousEnable
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit</td></tr>
</table>

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				when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. CBSR: No. of Control EDs Over Bulk EDs Served 0: 1:1 1: 2:1 2: 3:1 3: 4:1 The default value is 0x0.

10.6.6.3. HcCommandStatus Register(Default Value:0x0000_0000)

Offset: 0x0408				Register Name: HcCommandStatus
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.

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2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit,when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

10.6.6.4. HcInterruptStatus Register(Default Value:0x0000_0000)

Offset: 0x040C				**Register Name: HcInterruptStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.

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4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the SchedulingOverrunCount of *HcCommandStatus* to be incremented.

10.6.6.5. HcInterruptEnable Register(Default Value:0x0000_0000)

Offset: 0x0410				**Register Name: HcInterruptEnable**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Enable

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				0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

10.6.6.6. HcInterruptDisable Register(Default Value:0x0000_0000)

Offset: 0x0414			Register Name: HcInterruptDisable
Bit	**Read/Write**	**Default**	**Description**
	HCD **HC**		
31	R/W R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/ /	/	/
6	R/W R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W R	0x0	UnrecoverableError Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W R	0x0	ResumeDetected Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W R	0x0	StartofFrame Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Start of Flame;
1	R/W R	0x0	WritebackDoneHead Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Write back Done Head;
0	R/W R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore;

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				1	Disable interrupt generation due to Scheduling Overrun;	

10.6.6.7. HcHCCA Register(Default Value:0x0000_0000)

Offset: 0x0418				Register Name: HcHCCA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

10.6.6.8. HcPeriodCurrentED Register(Default Value:0x0000_0000)

Offset: 0x041C				Register Name: HcPeriodCurrentED(PCED)
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED[31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.6.6.9. HcControlHeadED Register(Default Value:0x0000_0000)

Offset: 0x0420				Register Name: HcControlHeadED[CHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	EHCD[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA

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				during the initialization of HC.
3:0	R	R	0x0	EHCD[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.6.6.10. HcControlCurrentED Register

Offset: 0x424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.6.6.11. HcBulkHeadED Register(Default Value:0x0000_0000)

Offset: 0x428				Register Name: HcBulkHeadED[BHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

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10.6.6.12. HcBulkCurrentED Register(Default Value:0x0000_0000)

Offset: 0x42C				Register Name: HcBulkCurrentED [BCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.6.6.13. HcDoneHead Register(Default Value:0x0000_0000)

Offset: 0x430				Register Name: HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of *HcInterruptStatus*.
3:0	R	R	0x0	HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

10.6.6.14. HcFmInterval Register(Default Value:0x0000_2EDF)

Offset: 0x0434				Register Name: HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.

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30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

10.6.6.15. HcFmRemaining Register(Default Value:0x0000_0000)

Offset: 0x0438				**Register Name: HcFmRemaining**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of *HcFmInterval* whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

10.6.6.16. HcFmNumber Register(Default Value:0x0000_0000)

Offset: 0x043C				**Register Name: HcFmNumber**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:16	/	/	/	/
15:0	R	R/W	0x0	FrameNumber This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC

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				has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in *HcInterruptStatus.*

10.6.6.17. HcPeriodicStart Register(Default Value:0x0000_0000)

Offset: 0x0440				Register Name: HcPeriodicStatus
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:14	/	/	/	/
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*. A typical value will be 0x2A3F (0x3e67??). When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

10.6.6.18. HcLSThreshold Register(Default Value:0x0000_0628)

Offset: 0x444				Register Name: HcLSThreshold
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:12	/	/	/	Reserved
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

10.6.6.19. HcRhDescriptorA Register(Default Value:0x0200_1201)

Offset: 0x448				Register Name: HcRhDescriptorA
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/

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<table>
<tr><td>12</td><td>R/W</td><td>R</td><td>0x1</td><td>NoOverCurrentProtection
This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting.<table><tr><td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr><tr><td>1</td><td>No overcurrent protection supported.</td></tr></table></td></tr>
<tr><td>11</td><td>R/W</td><td>R</td><td>0x0</td><td>OverCurrentProtectionMode
This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared.<table><tr><td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr><tr><td>1</td><td>Over-current status is reported on per-port basis.</td></tr></table></td></tr>
<tr><td>10</td><td>R</td><td>R</td><td>0x0</td><td>Device Type
This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.</td></tr>
<tr><td>9</td><td>R/W</td><td>R</td><td>0x1</td><td>PowerSwitchingMode
This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared.<table><tr><td>0</td><td>All ports are powered at the same time.</td></tr><tr><td>1</td><td>Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).</td></tr></table></td></tr>
<tr><td>8</td><td>R/W</td><td>R</td><td>0x0</td><td>NoPowerSwithcing
These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.<table><tr><td>0</td><td>Ports are power switched.</td></tr><tr><td>1</td><td>Ports are always powered on when the HC is powered on.</td></tr></table></td></tr>
<tr><td>7:0</td><td>R</td><td>R</td><td>0x01</td><td>NumberDownstreamPorts
These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.</td></tr>
</table>

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10.6.6.20. HcRhDescriptorB Register (Default Value:0x0000_0000)

Offset: 0x44C				Register Name: HcRhDescriptorB
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. … Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. … Bit15 Device attached to Port #15.

10.6.6.21. HcRhStatus Register(Default Value:0x0000_0000)

Offset: 0x450				Register Name: HcRhStatus Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	W	R	0x0	(write)ClearRemoteWakeupEnable Write a ‘1’ clears DeviceRemoteWakeupEnable. Write a ‘0’ has no effect.
30:18	/	/	/	/
17	R/W	R	0x0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a ‘1’.Writing a ‘0’ has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’. (write)SetGlobalPower

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				In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 ConnectStatusChange is not a remote wakeup event. 1 ConnectStatusChange is a remote wakeup event. (write)SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2	/	/	/	/
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

10.6.6.22. HcRhPortStatus Register(Default Value:0x0000_0100)

Offset: 0x454				**Register Name: HcRhPortStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange

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<table>
<tr><td></td><td></td><td></td><td></td><td>This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect.<table><tr><td>0</td><td>no change in PortOverCurrentIndicator</td></tr><tr><td>1</td><td>PortOverCurrentIndicator has changed</td></tr></table></td></tr>
<tr><td>18</td><td>R/W</td><td>R/W</td><td>0x0</td><td>PortSuspendStatusChange
This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. This bit is also cleared when ResetStatusChange is set.<table><tr><td>0</td><td>resume is not completed</td></tr><tr><td>1</td><td>resume completed</td></tr></table></td></tr>
<tr><td>17</td><td>R/W</td><td>R/W</td><td>0x0</td><td>PortEnableStatusChange
This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table></td></tr>
<tr><td>16</td><td>R/W</td><td>R/W</td><td>0x0</td><td>ConnectStatusChange
This bit is set whenever a connect or disconnect event occurs. The HCD writes a ‘1’ to clear this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.<table><tr><td>0</td><td>no change in PortEnableStatus</td></tr><tr><td>1</td><td>change in PortEnableStatus</td></tr></table>
NOTE
If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</td></tr>
<tr><td>15:10</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>9</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)LowSpeedDeviceAttached
This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.<table><tr><td>0</td><td>full speed device attached</td></tr><tr><td>1</td><td>low speed device attached</td></tr></table>
(write)ClearPortPower
The HCD clears the PortPowerStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect.</td></tr>
</table>

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<table>
<tr><td>8</td><td>R/W</td><td>R/W</td><td>0x1</td><td>(read)PortPowerStatus
This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
<table><tr><td>0</td><td>port power is off</td></tr><tr><td>1</td><td>port power is on</td></tr></table>
(write)SetPortPower
The HCD writes a ‘1’ to set the PortPowerStatus bit. Writing a ‘0’ has no effect.

NOTE
This bit is always reads ‘1b’ if power switching is not supported.</td></tr>
<tr><td>7:5</td><td>/</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>4</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortResetStatus
When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
<table><tr><td>0</td><td>port reset signal is not active</td></tr><tr><td>1</td><td>port reset signal is active</td></tr></table>
(write)SetPortReset
The HCD sets the port reset signaling by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</td></tr>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr></table></td></tr>
</table>

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				1 overcurrent condition detected. (write)ClearSuspendStatus The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.
2	R/W	R/W	0x0	(read)PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0 port is not suspended 1 port is suspended (write)SetPortSuspend The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.
1	R/W	R/W	0x0	(read)PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 port is disabled 1 port is enabled (write)SetPortEnable The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0 No device connected 1 Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no

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				effect. The CurrentConnectStatus is not affected by any write. **NOTE** **This bit is always read as '1' when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).**

10.6.7. HCI Controller and PHY Interface Description

10.6.7.1. HCI Interface Register(Default Value:0x1000_0000)

Offset: 0x800			**Register Name: USB_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	Reserved.
28	R	0x1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0x0	OHCI Count Select 1: Simulation mode, the counters will be much shorter then real time 0: Normal mode, the counters will count full time
24	R/W	0x0	Simulation Mode 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation 0: No effect
23:21	/	/	/
20	R/W	0x0	EHCI HS Force Set 1 to this field force the ehci enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19:13	/	/	/
12	R/W	0x0	PP2VBUS 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY
11	R/W	0x0	AHB Master Interface INCR16 Enable 1: Use INCR16 when appropriate 0: do not use INCR16,use other enabled INCRX or unspecified length burst INCR
10	R/W	0x0	AHB Master Interface INCR8 Enable 1: Use INCR8 when appropriate 0: Do not use INCR8,use other enabled INCRX or unspecified length burst INCR

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9	R/W	0x0	AHB Master Interface Burst Type INCR4 Enable 1: Use INCR4 when appropriate 0: Do not use INCR4,use other enabled INCRX or unspecified length burst INCR
8	R/W	0x0	AHB Master Interface INCRX Align Enable 1: start INCRx burst only on burst x-align address 0: Start burst on any double word boundary **NOTE** **This bit must enable if any bit of 11:9 is enabled.**
7:1	/	/	/
0	R/W	0x0	ULPI Bypass Enable 1: Enable UTMI interface, disable ULPI interface 0: Enable ULPI interface, disable UTMI interface

10.6.7.2. PHY Control Register(Default Value: 0x0000_0002)

Offset: 0x810			Register Name: PHY Control
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	BIST_EN_A
15:9	/	/	/
8	R/W	0x0	500K PULLUP ENABLE
7:2	/	/	/
1	R/W	0x1	SIDDQ write 1 to enable phy
0	R/W	0x0	VC_CLK

10.6.7.3. HSIC PHY Tune1 Register(Default Value: 0x0000_0010)

Offset: 0x81C			Register Name: HSIC_PHY_Tune1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:5	/	/	TXRPUTUNE
5:4	R/W	0x1	TXRPDTUNE
3:0	R/W	0x0	TXSRTUNE

10.6.7.4. HSIC PHY Tune2 Register(Default Value: 0x0000_0010)

Offset: 0x820			Register Name: HSIC_PHY_Tune2
Bit	**Read/Write**	**Default/Hex**	**Description**

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31	/	/	BIST_EN
30	R/W	0x0	TESTBURNIN
29	R/W	0x0	TESTDATAOUTSEL
28	R/W	0x0	TESTCLK
27:24	R/W	0x0	TESTADDR
23:16	R/W	0x0	TESTDATAIN
15:4	R/W	0x1	SIDDQ
3:0	R/W	0x0	REFCLK DIV

10.6.7.5. HSIC PHY Tune3 Register(Default Value: 0x0000_0010)

Offset: 0x824			Register Name: HSIC PHY tune3 Register
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
5	R/W	0x0	HSIC BIST_ERROR
4	R/W	0x0	HSIC BIST_DONE
3:2	R/W	0x0	HSIC TESTDATA OUT[3:2]
1	R/W	0x1	Non_HSIC_MODE_BIST_ERROR testdata out[1]
0	R/W	0x0	Non_HSIC_MODE_BIST_DONE testdata out[0]

10.6.7.6. HCI SIE Port Disable Control Register(Default Value:0x0000_0000)

Offset: 0x828			Register Name: USB_SPDCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	SE0 Status This bit is set when no-se0 is detected before SOF when bit[1:0] is 10b or 11b
15:2	/	/	/
1:0	R/W	0x0	Port Disable Control 00: Port Disable when no-se0 detect before SOF 01: Port Disable when no-se0 detect before SOF 10: No Port Disable when no-se0 detect before SOF 11: Port Disable when no-se0 3 time detect before SOF during 8 frames

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10.7. Port Controller

10.7.1. Overview

The Port Controller can be configured with multi-functional input/output pins. All these ports can be configured as GPIO only if multiplexed functions not used. The total 7 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

The Port Controller has the following features:

- 10 ports(PB,PC,PD,PE,PF,PG,PH,PJ,PL,PM)
- Software control for each signal pin
- GPIO peripheral can produce interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 110 interrupts
- Configurable interrupt edges

10.7.2. Block Diagram

The block diagram of port controller is shown in Figure 10-27.

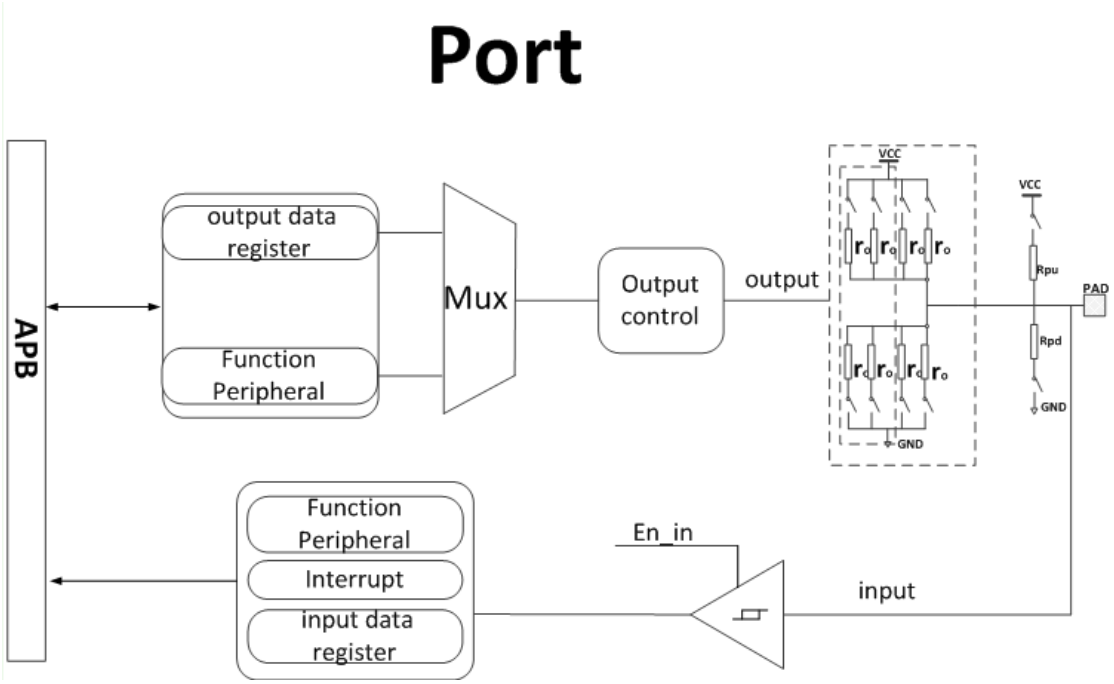

Figure 10- 27. Port Controller Block Diagram

Port controller consists of digital part(GPIO, external interface) and IO analog part(output buffer, dual pull down, pad, etc). Digital part can select output interface by MUX switch; analog part can configure pull up/down, buffer strength.

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When executing GPIO read state, the port controller reads the current level of pin into internal register bus. When not executing GPIO read state, external pin and internal register bus is off-status, that is high-impedance.

10.7.3. Operations and Functional Descriptions

10.7.3.1. Multi-function Port Table

T7 includes 173 multi-functional input/output port pins.There are 10 ports as listed below:

Table 10- 14. Multi-function Port Table

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PB	10	Schmitt	CMOS	UART/I2S/JTAG/UART/SCR/TWI/PB_EINT	3.3V
PC	17	Schmitt	CMOS	NAND/SMHC/SPI	1.8V/3.3V
PD	23	Schmitt	CMOS	LCD/LVDS/PWM	3.3V
PE	23	Schmitt	CMOS	CSI/TWI/TS	1.8V/2.8V/3.3V
PF	7	Schmitt	CMOS	SMHC/UART/JTAG/PF_EINT	3.3V
PG	15	Schmitt	CMOS	SMHC/UART/I2S/DMIC/PG_EINT	1.8V/3.3V
PH	19	Schmitt	CMOS	TWI/UART/OWA/DMIC/CSI/SPI/PH_EINT	3.3V
PJ	19	Schmitt	CMOS	CSI/SMHC/TWI/RGMII/MII/RMII/PJ_EINT	1.8V/2.8V/3.3V
PL	10	Schmitt	CMOS	RSB/UART/JTAG/TWI/PL_EINT	1.8V/3.3V
PM	30	Schmitt	CMOS	PWM/SPI/UART/TWI/PM_EINT	1.8V/3.3V

10.7.3.2. Port Functiom

Port Controller supports 10 GPIOs, every GPIO can configure as Input,Output,Function Peripheral,IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 10- 15. Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/: non-configure, configuration is invalid

Y: configure

X: Select configuration according to actual situation

N: Forbid to configure

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10.7.3.3. Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

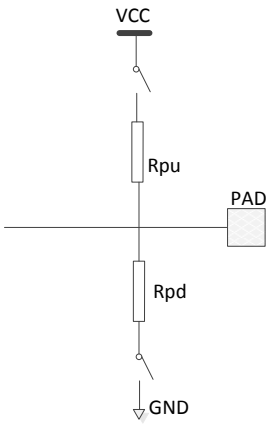

Figure 10- 28. Pull up/down Logic

High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, software configures the switch on Rpu and Rpd as off ,and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by a resistance, the resistance has current-limiting function. When pulling up, the switch on Rpu is breakover by software configuration, IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is breakover by software configuration, IO is pulled down to GND by Rpd.

The pull-up/down of each IO is weak pull-up/down, the resistance is 100kΩ±50%.

The setting of pull-down,pull-up,high-impledance is decided by external circuit.

10.7.3.4. Buffer Strength

Each IO can be set as different buffer strength.The IO buffer diagram is as follows.

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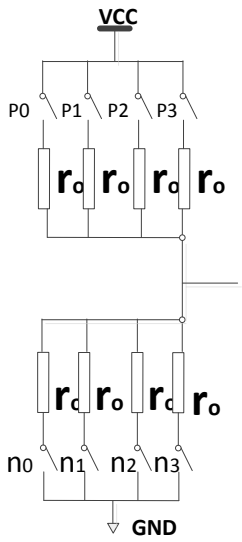

Figure 10- 29. IO Buffer Strength Diagram

When output high level, the n0,n1,n2,n3 of NMOS is off, the p0,p1,p2,p3 of PMOS is on. When buffer strength is set to 0(buffer strength is weakest), only p0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2.When buffer strength is 2, only p0,p1 and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3.When buffer strength is 3, p0,p1,p2 and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0,p1,p2,p3 of PMOS is off, the n0,n1,n2,n3 of NMOS is on. When buffer strength is set to 0(buffer strength is weakest), only n0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only n0,n1 and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, n0,n1,n2 and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between output driver circuit and port is unconnected, driver configuration is invalid.

10.7.3.5. Interrupt

Each group IO has independent interrupt number.IO within group uses one interrupt number, when one IO generates interrupt, Port Controller sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

Interrupt trigger of GPIO supports the following trigger types.

- Positive Edge : When low level changes to high level, the interrupt will generate. No matter how long high level keeps, the interrupt generates only once.
- Negative Edge: When high level changes to low level, the interrupt will generate. No matter how long low level keeps, the interrupt generates only once.
- High Level : Just keep high level and the interrupt will always generate.

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- Low Level : Just keep low level and the interrupt will always generate.
- Double Edge : Positive and negative edge.

External Interrupt Configure Register is used to configure trigger type.

GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using lower sample clock, to reach the debounce effect because of the dither frequency of signal is higher than sample frequency.

Set sample clock source by PIO_INT_CLK_SELECT and prescale factor by DEB_CLK_PRE_SCALE.

10.7.4. CPUX Port Register List

Module Name	Base Address
GPIO	0x0300B000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0(n =1,2,3,4,5,6,7,9)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1(n =1,2,3,4,5,6,7,9)
Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2(n =1,2,3,4,5,6,7,9)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3(n =1,2,3,4,5,6,7,9)
Pn_DAT	n*0x0024+0x10	Port n Data Register(n =1,2,3,4,5,6,7,9)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0(n =1,2,3,4,5,6,7,9)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1(n =1,2,3,4,5,6,7,9)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0(n =1,2,3,4,5,6,7,9)
Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1(n =1,2,3,4,5,6,7,9)
Pn_INT_CFG0	0x0200+n*0x20+0x00	PIO Interrupt Configure Register 0(n =1,5,6,7,9)
Pn _INT_CFG1	0x0200+n*0x20+0x04	PIO Interrupt Configure Register 1(n =1,5,6,7,9)
Pn _INT_CFG2	0x0200+n*0x20+0x08	PIO Interrupt Configure Register 2(n =1,5,6,7,9)
Pn _INT_CFG3	0x0200+n*0x20+0x0C	PIO Interrupt Configure Register 3(n =1,5,6,7,9)
Pn _INT_CTL	0x0200+n*0x20+0x10	PIO Interrupt Control Register(n =1,5,6,7,9)
Pn _INT_STA	0x0200+n*0x20+0x14	PIO Interrupt Status Register(n =1,5,6,7,9)
Pn _INT_DEB	0x0200+n*0x20+0x18	PIO Interrupt Debounce Register(n =1,5,6,7,9)

10.7.5. CPUX Port Register Description

10.7.5.1. PB Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0024			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PB7_SELECT

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			000: Input 010: CPUBIST3 100: UART4_RX 110: PB_EINT7	001: Output 011: PCM0_DIN 101: SIM_DET 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PB6_SELECT 000: Input 010: CPUBIST2 100: UART4_TX 110: PB_EINT6	 001: Output 011: PCM0_DOUT 101: SIM_RST 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PB5_SELECT 000: Input 010: CPUBIST1 100: UART4_CTS 110: PB_EINT5	 001: Output 011: PCM0_BCLK 101: SIM_DATA 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PB4_SELECT 000: Input 010: CPUBIST0 100: UART4_RTS 110: PB_EINT4	 001: Output 011: PCM0_SYNC 101: SIM_CLK 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PB3_SELECT 000: Input 010: UART2_CTS 100: JTAG_DI0 110: PB_EINT3	 001: Output 011: I2S0_MCLK 101: SIM_VPPPP 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PB2_SELECT 000: Input 010: UART2_RTS 100: JTAG_DO0 110: PB_EINT2	 001: Output 011: PCM2_DIN 101: SIM_VPPEN 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PB1_SELECT 000: Input 010: UART2_RX 100: JTAG_CK0 110: PB_EINT1	 001: Output 011: PCM2_DOUT 101: SIM_PWREN 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PB0_SELECT 000: Input 010: UART2_TX	 001: Output 011: PCM2_BCLK

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			100: JTAG_MS0	101: Reserved
			110: PB_EINT0	111: IO Disable

10.7.5.2. PB Configure Register 1 (Default Value: 0x0000_0077)

Offset: 0x0028			Register Name: PB_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:7	/	/	/	
6:4	R/W	0x7	PB9_SELECT 000: Input 010: Reserved 100: UART0_RX 110: PB_EINT9	 001: Output 011: I2S2_MCLK 101: TWI2_SDA 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PB8_SELECT 000: Input 010: Reserved 100: UART0_TX 110: PB_EINT8	 001: Output 011: PCM2_SYNC 101: TWI2_SCK 111: IO Disable

10.7.5.3. PB Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PB_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.4. PB Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PB_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.5. PB Data Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PB_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding

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			bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.5.6. PB Multi-Driving Register 0 (Default Value: 0x0005_5555)

Offset: 0x0038			Register Name: PB_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x1	PB9_DRV PB9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PB8_DRV PB8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PB7_DRV PB7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PB6_DRV PB6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PB5_DRV PB5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PB4_DRV PB4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PB3_DRV PB3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PB2_DRV PB2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PB1_DRV PB1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

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1:0	R/W	0x1	PB0_DRV PB0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.5.7. PB Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PB_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.8. PB Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PB_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	PB9_PULL PB9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PB8_PULL PB8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PB7_PULL PB7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PB6_PULL PB6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PB5_PULL PB5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PB4_PULL PB4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PB3_PULL PB3 Pull-up/down Select

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			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved
5:4	R/W	0x0	PB2_PULL PB2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PB1_PULL PB1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PB0_PULL PB0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

10.7.5.9. PB Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: PB_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.10. PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PC7_SELECT 000:Input 010:NAND_DQ1 100:SPI0_WP 110:Reserved	 001:Output 011:SDC2_D1 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PC6_SELECT 000:Input 010:NAND_DQ0 100:SPI0_HOLD 110:Reserved	 001:Output 011:SDC2_D0 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC5_SELECT 000:Input 010:NAND_RB0 100:SPI0_CS	 001:Output 011:SDC2_CMD 101:Reserved

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			110:Reserved	111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000:Input 010:NAND_RE 100:Reserved 110:Reserved	001:Output 011:SDC2_CLK 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000:Input 010:NAND_CE0 100:SPI0_MISO 110:Reserved	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000:Input 010:NAND_CLE 100:SPI0_MOSI 110:Reserved	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000:Input 010:NAND_ALE 100:Reserved 110:Reserved	001:Output 011:SDC2_DS 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000:Input 010:NAND_WE 100:SPI0_CLK 110:Reserved	001:Output 011:Reserved 101:Reserved 111:IO Disable

10.7.5.11. PC Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x004C			Register Name: PC_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PC15_SELECT 000: Input 010: NAND_CE1 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	

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26:24	R/W	0x7	PC14_SELECT 000: Input 010: NAND_DQS 100: Reserved 110: Reserved	 001: Output 011: SDC2_RST 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PC13_SELECT 000: Input 010: NAND_DQ7 100: Reserved 110: Reserved	 001: Output 011: SDC2_D7 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PC12_SELECT 000: Input 010: NAND_DQ6 100: Reserved 110: Reserved	 001: Output 011: SDC2_D6 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PC11_SELECT 000: Input 010: NAND_DQ5 100: Reserved 110: Reserved	 001: Output 011: SDC2_D5 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PC10_SELECT 000: Input 010: NAND_DQ4 100: Reserved 110: Reserved	 001: Output 011: SDC2_D4 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PC9_SELECT 000: Input 010: NAND_DQ3 100: Reserved 110: Reserved	 001: Output 011: SDC2_D3 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PC8_SELECT 000: Input 010: NAND_DQ2 100: Reserved 110: Reserved	 001: Output 011: SDC2_D2 101: Reserved 111: IO Disable

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10.7.5.12. PC Configure Register 2 (Default Value: 0x0000_0007)

Offset: 0x0050			Register Name: PC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000:Input 001:Output 010:NAND_RB1 011:Reserved 100:Reserved 101:Reserved 110:Reserved 111:IO Disable

10.7.5.13. PC Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: PC_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.14. PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.5.15. PC Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x005C			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PC15_DRV PC15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PC14_DRV PC14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PC13_DRV

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			PC13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PC12_DRV PC12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PC11_DRV PC11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PC10_DRV PC10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PC9_DRV PC9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PC8_DRV PC8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PC7_DRV PC7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PC6_DRV PC6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PC5_DRV PC5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PC4_DRV PC4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PC3_DRV PC3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PC2_DRV PC2 Multi-Driving Select

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			00: Level 0 10: Level 2	01: Level 1 11: Level 3
3:2	R/W	0x1	PC1_DRV PC1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PC0_DRV PC0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.7.5.16. PC Multi-Driving Register 1 (Default Value: 0x0000_0001)

Offset: 0x0060			Register Name: PC_DRV1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:2	/	/	/	
1:0	R/W	0x1	PC16_DRV PC16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.7.5.17. PC Pull Register 0 (Default Value: 0x4000_0440)

Offset: 0x0064			Register Name: PC_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x1	PC15_PULL PC15 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
29:28	R/W	0x0	PC14_PULL PC14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PC13_PULL PC13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PC12_PULL PC12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PC11_PULL	

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			PC11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PC7_PULL PC7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PC6_PULL PC6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x1	PC5_PULL PC5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PC4_PULL PC4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PC2_PULL PC2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PC1_PULL PC Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull-up/down Select

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			00: Pull-up/down disable	01: Pull-up
			10: Pull-down	11: Reserved

10.7.5.18. PC Pull Register 1 (Default Value: 0x0000_0001)

Offset: 0x0068			Register Name: PC_PULL1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:2	/	/	/	
1:0	R/W	0x1	PC16_PULL PC16 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

10.7.5.19. PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD7_SELECT 000: Input 010: LCD_D11 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VNC 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PD6_SELECT 000: Input 010: LCD_D10 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VPC 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PD5_SELECT 000: Input 010: LCD_D7 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VN2 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD4_SELECT 000: Input 010: LCD_D6 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP2 101: Reserved 111: IO Disable
15	/	/	/	

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14:12	R/W	0x7	PD3_SELECT 000: Input 010: LCD_D5 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VN1 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000: Input 010: LCD_D4 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP1 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000: Input 010: LCD_D3 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VN0 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD0_SELECT 000: Input 010: LCD_D2 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP0 101: Reserved 111: IO Disable

10.7.5.20. PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD15_SELECT 000: Input 010: LCD_D21 100: PWM7 110: Reserved	 001: Output 011: LVDS1_VN2 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PD14_SELECT 000: Input 010: LCD_D20 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VP2 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PD13_SELECT 000: Input	 001: Output

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			010: LCD_D19	011: LVDS1_VN1
			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD12_SELECT 000: Input 010: LCD_D18 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VP1 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PD11_SELECT 000: Input 010: LCD_D15 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VN0 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD10_SELECT 000: Input 010: LCD_D14 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VP0 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD9_SELECT 000: Input 010: LCD_D13 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VN3 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD8_SELECT 000: Input 010: LCD_D12 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP3 101: Reserved 111: IO Disable

10.7.5.21. PD Configure Register 2 (Default Value: 0x0777_7777)

Offset: 0x0074			**Register Name: PD_CFG2**	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PD22_SELECT 000: Input 010: PWM0 100: Reserved	 001: Output 011: Reserved 101: Reserved

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			110: Reserved	111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT 000: Input 010: LCD_VSYNC 100: PWM1 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000: Input 010: LCD_HSYNC 100: PWM2 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000: Input 010: LCD_DE 100: PWM3 110: Reserved	001: Output 011: LVDS1_VN3 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000: Input 010: LCD_CLK 100: PWM4 110: Reserved	001: Output 011: LVDS1_VP3 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD17_SELECT 000: Input 010: LCD_D23 100: PWM5 110: Reserved	001: Output 011: LVDS1_VNC 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD16_SELECT 000: Input 010: LCD_D22 100: PWM6 110: Reserved	001: Output 011: LVDS1_VPC 101: Reserved 111: IO Disable

10.7.5.22. PD Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: PD_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/

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10.7.5.23. PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.5.24. PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PD15_DRV PD15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PD14_DRV PD14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PD13_DRV PD13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PD12_DRV PD12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PD11_DRV PD11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PD10_DRV PD10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PD9_DRV PD9 Multi-Driving Select

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			00: Level 0 10: Level 2	01: Level 1 11: Level 3
17:16	R/W	0x1	PD8_DRV PD8 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
15:14	R/W	0x1	PD7_DRV PD7 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
13:12	R/W	0x1	PD6_DRV PD6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PD5_DRV PD5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PD4_DRV PD4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PD3_DRV PD3 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PD2_DRV PD2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PD1_DRV PD1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PD0_DRV PD0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.7.5.25. PD Multi-Driving Register 1 (Default Value: 0x0000_1555)

Offset: 0x0084			Register Name: PD_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/

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13:12	R/W	0x1	PD22_DRV PD22 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD21_DRV PD21 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD20_DRV PD20 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD19_DRV PD19 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD18_DRV PD18 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD17_DRV PD17 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD16_DRV PD16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.5.26. PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PD15_PULL PD15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PD13_PULL PD13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

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			10: Pull-down	11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

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3:2	R/W	0x0	PD1_PULL PD1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.5.27. PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PD22_PULL PD22 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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10.7.5.28. PE Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE7_SELECT 000: Input 010: NCSI0_D3 100: TS_D3 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PE6_SELECT 000: Input 010: NCSI0_D2 100: TS_D2 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PE5_SELECT 000: Input 010: NCSI0_D1 100: TS_D1 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PE4_SELECT 000: Input 010: NCSI0_D0 100: TS_D0 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PE3_SELECT 000: Input 010: NCSI0_VSYNC 100: TS_DVLD 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PE2_SELECT 000: Input 010: NCSI0_HSYNC 100: TS_SYNC 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PE1_SELECT 000: Input 010: NCSI0_MCLK	 001: Output 011: Reserved

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			100: TS_ERR	101: Reserved
			110: Reserved	111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PE0_SELECT	
			000: Input	001: Output
			010: NCSI0_PCLK	011: Reserved
			100: TS_CLK	101: Reserved
			110: Reserved	111: IO Disable

10.7.5.29. PE Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0094			Register Name: PE_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE15_SELECT	
			000: Input	001: Output
			010: NCSI0_D11	011: TWI0_SDA
			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PE14_SELECT	
			000: Input	001: Output
			010: NCSI0_D10	011: TWI0_SCK
			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PE13_SELECT	
			000: Input	001: Output
			010: NCSI0_D9	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PE12_SELECT	
			000: Input	001: Output
			010: NCSI0_D8	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PE11_SELECT	
			000: Input	001: Output
			010: NCSI0_D7	011: Reserved
			100: TS_D7	101: Reserved
			110: Reserved	111: IO Disable

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11	/	/	/
10:8	R/W	0x7	PE10_SELECT 000: Input 001: Output 010: NCSI0_D6 011: Reserved 100: TS_D6 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PE9_SELECT 000: Input 001: Output 010: NCSI0_D5 011: Reserved 100: TS_D5 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PE8_SELECT 000: Input 001: Output 010: NCSI0_D4 011: Reserved 100: TS_D4 101: Reserved 110: Reserved 111: IO Disable

10.7.5.30. PE Configure Register 2 (Default Value: 0x0777_7777)

Offset: 0x0098			Register Name: PE_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PE22_SELECT 000: Input 001: Output 010: CSI_FSIN0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PE21_SELECT 000: Input 001: Output 010: NCSI0_SDA 011: TWI3_SDA 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PE20_SELECT 000: Input 001: Output 010: NCSI0_SCK 011: TWI3_SCK 100: Reserved 101: PLL_LOCK_DBG 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PE19_SELECT

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			000: Input 010: NCSI0_D15 100: Reserved 110: Reserved	001: Output 011: TWI2_SDA 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PE18_SELECT 000: Input 010: NCSI0_D14 100: Reserved 110: Reserved	 001: Output 011: TWI2_SCK 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PE17_SELECT 000: Input 010: NCSI0_D13 100: Reserved 110: Reserved	 001: Output 011: TWI1_SDA 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PE16_SELECT 000: Input 010: NCSI0_D12 100: Reserved 110: Reserved	 001: Output 011: TWI1_SCK 101: Reserved 111: IO Disable

10.7.5.31. PE Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PE_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.32. PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PE_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

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10.7.5.33. PE Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x00A4			Register Name: PE_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PE15_DRV PE15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PE14_DRV PE14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PE13_DRV PE13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PE12_DRV PE12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PE11_DRV PE11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PE10_DRV PE10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PE9_DRV PE9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PE8_DRV PE8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PE7_DRV PE7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PE6_DRV PE6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PE5_DRV

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			PE5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PE4_DRV PE4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PE3_DRV PE3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PE2_DRV PE2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PE1_DRV PE1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PE0_DRV PE0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.5.34. PE Multi-Driving Register 1 (Default Value: 0x0000_1555)

Offset: 0x00A8			Register Name: PE_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PE22_DRV PE22 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PE21_DRV PE21 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PE20_DRV PE20 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PE19_DRV PE19 Multi-Driving Select 00: Level 0 01: Level 1

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			10: Level 2	11: Level 3
5:4	R/W	0x1	PE18_DRV PE18 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PE17_DRV PE17 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PE16_DRV PE16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.7.5.35. PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: PE_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x0	PE15_PULL PE15 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
29:28	R/W	0x0	PE14_PULL PE14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PE13_PULL PE13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull-up/down Select	

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			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PE5_PULL PE5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.5.36. PE Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PE_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/

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13:12	R/W	0x0	PE22_PULL PE22 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PE21_PULL PE21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PE20_PULL PE20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PE19_PULL PE19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE18_PULL PE18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PE17_PULL PE17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE16_PULL PE16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.5.37. PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x7	PF6_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: PF_EINT6 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PF5_SELECT 000: Input 001: Output 010: SDC0_D2 011: JTAG_CK1 100: Reserved 101: Reserved

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			110: PF_EINT5	111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PF4_SELECT 000: Input 010: SDC0_D3 100: Reserved 110: PF_EINT4	 001: Output 011: UART0_RX 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PF3_SELECT 000: Input 010: SDC0_CMD 100: Reserved 110: PF_EINT3	 001: Output 011: JTAG_DO1 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PF2_SELECT 000: Input 010: SDC0_CLK 100: Reserved 110: PF_EINT2	 001: Output 011: UART0_TX 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PF1_SELECT 000: Input 010: SDC0_D0 100: Reserved 110: PF_EINT1	 001: Output 011: JTAG_DI1 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PF0_SELECT 000: Input 010: SDC0_D1 100: Reserved 110: PF_EINT0	 001: Output 011: JTAG_MS1 101: Reserved 111: IO Disable

10.7.5.38. PF Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PF_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.39. PF Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: PF_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	/	/	/

10.7.5.40. PF Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: PF_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.41. PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.5.42. PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PF6_DRV PF6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PF5_DRV PF5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PF4_DRV PF4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PF3_DRV PF3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PF2_DRV

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			PF2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PF1_DRV PF1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PF0_DRV PF0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.5.43. PF Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PF_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.44. PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

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			10: Pull-down	11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

10.7.5.45. PF Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: PF_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.46. PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PG7_SELECT 000: Input 010: UART1_RX 100: Reserved 110: PG_EINT7	 001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PG6_SELECT 000: Input 010: UART1_TX 100: Reserved 110: PG_EINT6	 001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PG5_SELECT 000: Input 010: SDC1_D3 100: Reserved 110: PG_EINT5	 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PG4_SELECT 000: Input 010: SDC1_D2	 001: Output 011: Reserved

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			100: Reserved	101: Reserved
			110: PG_EINT4	111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PG3_SELECT 000: Input 010: SDC1_D1 100: Reserved 110: PG_EINT3	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PG2_SELECT 000: Input 010: SDC1_D0 100: Reserved 110: PG_EINT2	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PG1_SELECT 000: Input 010: SDC1_CMD 100: Reserved 110: PG_EINT1	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000: Input 010: SDC1_CLK 100: Reserved 110: PG_EINT0	 001: Output 011: Reserved 101: Reserved 111: IO Disable

10.7.5.47. PG Configure Register 1 (Default Value: 0x0777_7777)

Offset: 0x00DC			Register Name: PG_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PG14_SELECT 000: Input 010: I2S1_MCLK 100: Reserved 110: PG_EINT14	 001: Output 011: DMIC_DATA3 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PG13_SELECT 000: Input 010: PCM1_DIN 100: Reserved 110: PG_EINT13	 001: Output 011: Reserved 101: Reserved 111: IO Disable

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19	/	/	/
18:16	R/W	0x7	PG12_SELECT 000: Input 001: Output 010: PCM1_DOUT 011: Reserved 100: Reserved 101: Reserved 110: PG_EINT12 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PG11_SELECT 000: Input 001: Output 010: PCM1_BCLK 011: Reserved 100: Reserved 101: Reserved 110: PG_EINT11 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PG10_SELECT 000: Input 001: Output 010: PCM1_SYNC 011: Reserved 100: Reserved 101: Reserved 110: PG_EINT10 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PG9_SELECT 000: Input 001: Output 010: UART1_CTS 011: DMIC_DATA2 100: Reserved 101: Reserved 110: PG_EINT9 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PG8_SELECT 000: Input 001: Output 010: UART1_RTS 011: Reserved 100: Reserved 101: Reserved 110: PG_EINT8 111: IO Disable

10.7.5.48. PG Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PG_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.49. PG Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PG_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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10.7.5.50. PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.5.51. PG Multi-Driving Register 0 (Default Value: 0x1555_5555)

Offset: 0x00EC			Register Name: PG_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x1	PG14_DRV PG14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PG13_DRV PG13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PG12_DRV PG12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PG11_DRV PG11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PG10_DRV PG10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PG9_DRV PG9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PG8_DRV

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			PG8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PG7_DRV PG7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PG6_DRV PG6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PG5_DRV PG5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PG4_DRV PG4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PG3_DRV PG3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PG2_DRV PG2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PG1_DRV PG1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PG0_DRV PG0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.5.52. PG Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: PG_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

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10.7.5.53. PG Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	PG14_PULL PG14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PG13_PULL PG13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PG12_PULL PG12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PG11_PULL PG11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PG10_PULL PG10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PG9_PULL PG9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PG8_PULL PG8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PG7_PULL PG7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PG5_PULL PG5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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9:8	R/W	0x0	PG4_PULL PG4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PG3_PULL PG3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PG2_PULL PG2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PG1_PULL PG1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.5.54. PG Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PG_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.55. PH Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00FC			Register Name: PH_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PH7_SELECT 000: Input 001: Output 010: TWI6_SDA 011: MCSIB_SDA 100: Reserved 101: Reserved 110: PH_EINT7 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PH6_SELECT 000: Input 001: Output 010: TWI6_SCK 011: MCSIB_SCK 100: Reserved 101: Reserved

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			110: PH_EINT6	111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PH5_SELECT 000: Input 010: TWI5_SDA 100: Reserved 110: PH_EINT5	001: Output 011: MCSIA_SDA 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PH4_SELECT 000: Input 010: TWI5_SCK 100: Reserved 110: PH_EINT4	001: Output 011: MCSIA_SCK 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PH3_SELECT 000: Input 010: TWI1_SDA 100: Reserved 110: PH_EINT3	001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PH2_SELECT 000: Input 010: TWI1_SCK 100: Reserved 110: PH_EINT2	001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PH1_SELECT 000: Input 010: TWI0_SDA 100: Reserved 110: PH_EINT1	001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000: Input 010: TWI0_SCK 100: Reserved 110: PH_EINT0	001: Output 011: Reserved 101: Reserved 111: IO Disable

10.7.5.56. PH Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0100			Register Name: PH_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

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30:28	R/W	0x7	PH15_SELECT 000: Input 010: OWA_IN 100: Reserved 110: PH_EINT15	 001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PH14_SELECT 000: Input 010: OWA_OUT 100: Reserved 110: PH_EINT14	 001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PH13_SELECT 000: Input 010: UART3_CTS 100: SPI1_MISO 110: PH_EINT13	 001: Output 011: NCSI1_D15 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PH12_SELECT 000: Input 010: UART3_RTS 100: SPI1_MOSI 110: PH_EINT12	 001: Output 011: NCSI1_D14 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PH11_SELECT 000: Input 010: UART3_RX 100: SPI1_CS 110: PH_EINT11	 001: Output 011: NCSI1_D13 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PH10_SELECT 000: Input 010: UART3_TX 100: SPI1_CLK 110: PH_EINT10	 001: Output 011: NCSI1_D12 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000: Input 010: MCSIB_MCLK 100: Reserved 110: PH_EINT9	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000: Input 010: MCSIA_MCLK	 001: Output 011: Reserved

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			100: Reserved	101: Reserved
			110: PH_EINT8	111: IO Disable

10.7.5.57. PH Configure Register 2 (Default Value: 0x0000_0777)

Offset: 0x0104			Register Name: PH_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:11	/	/	/	
10:8	R/W	0x7	PH18_SELECT 000: Input 010: DMIC_CLK 100: Reserved 110: PH_EINT18	 001: Output 011: TWI4_SDA 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PH17_SELECT 000: Input 010: DMIC_DATA0 100: Reserved 110: PH_EINT17	 001: Output 011: TWI4_SCK 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PH16_SELECT 000: Input 010: DMIC_DATA1 100: Reserved 110: PH_EINT16	 001: Output 011: Reserved 101: Reserved 111: IO Disable

10.7.5.58. PH Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: PH_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.59. PH Data Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the

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			port is configured as functional pin, the undefined value will be read.

10.7.5.60. PH Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0110			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PH15_DRV PH15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PH14_DRV PH14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PH13_DRV PH13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PH12_DRV PH12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PH11_DRV PH11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PH10_DRV PH10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PH9_DRV PH9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PH8_DRV PH8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PH7_DRV PH7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PH6_DRV PH6 Multi-Driving Select

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			00: Level 0 10: Level 2	01: Level 1 11: Level 3
11:10	R/W	0x1	PH5_DRV PH5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PH4_DRV PH4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PH3_DRV PH3 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PH2_DRV PH2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PH1_DRV PH1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PH0_DRV PH0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.7.5.61. PH Multi-Driving Register 1 (Default Value: 0x0000_0015)

Offset: 0x0114			Register Name: PH_DRV1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:6	/	/	/	
5:4	R/W	0x1	PH18_DRV PH18 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PH17_DRV PH17 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PH16_DRV PH16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

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10.7.5.62. PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PH_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PH15_PULL PH15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

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			10: Pull-down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.5.63. PH Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PH_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	PH18_PULL PH18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PH17_PULL PH17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PH16_PULL PH16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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10.7.5.64. PJ Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0144			Register Name: PJ_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PJ7_SELECT 000: Input 001: Output 010: NCSI1_D3 011: SDC3_CMD 100: RGMII_TXD3/MII_TXD3/RMII_NULL 101: Reserved 110: PJ_EINT7 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PJ6_SELECT 000: Input 001: Output 010: NCSI1_D2 011: SDC3_CLK 100: RGMII_NULL/MII_RXERR/RMII_RXER 101: Reserved 110: PJ_EINT6 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PJ5_SELECT 000: Input 001: Output 010: NCSI1_D1 011: SDC3_D0 100: RGMII_RXCTL/MII_RXDV/RMII_CRS_DV 101: Reserved 110: PJ_EINT5 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PJ4_SELECT 000: Input 001: Output 010: NCSI1_D0 011: SDC3_D1 100: RGMII_RXCK/MII_RXCK/RMII_NULL 101: Reserved 110: PJ_EINT4 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PJ3_SELECT 000: Input 001: Output 010: NCSI1_VSYNC 011: Reserved 100: RGMII_RXD0/MII_RXD0/RMII_RXD0 101: Reserved 110: PJ_EINT3 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PJ2_SELECT 000: Input 001: Output 010: NCSI1_HSYNC 011: Reserved 100: RGMII_RXD1/MII_RXD1/RMII_RXD1 101: Reserved 110: PJ_EINT2 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PJ1_SELECT 000: Input 001: Output 010: NCSI1_MCLK 011: Reserved

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			100: RGMII_RXD2/MII_RXD2/RMII_NULL	101: Reserved
			110: PJ_EINT1	111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PJ0_SELECT	
			000: Input	001: Output
			010: NCSI1_PCLK	011: Reserved
			100: RGMII_RXD3/MII_RXD3/ RMII_NULL	101: Reserved
			110: PJ_EINT0	111: IO Disable

10.7.5.65. PJ Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0148			Register Name: PJ_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PJ15_SELECT	
			000: Input	001: Output
			010: NCSI1_D11	011: TWI3_SDA
			100: RGMII_CLKIN/MII_COL/RMII_NULL	101: Reserved
			110: PJ_EINT15	111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PJ14_SELECT	
			000: Input	001: Output
			010: NCSI1_D10	011: TWI3_SCK
			100: RGMII_NULL/MII_TXERR/RMII_NULL	101: Reserved
			110: PJ_EINT14	111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PJ13_SELECT	
			000: Input	001: Output
			010: NCSI1_D9	011: Reserved
			100: RGMII_TXCTL/MII_TXEN/RMII_TXEN	101: Reserved
			110: PJ_EINT13	111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PJ12_SELECT	
			000: Input	001: Output
			010: NCSI1_D8	011: Reserved
			100: RGMII_TXCK/MII_TXCK/RMII_TXCK	101: Reserved
			110: PJ_EINT12	111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PJ11_SELECT	
			000: Input	001: Output
			010: NCSI1_D7	011: Reserved
			100: RGMII_NULL/MII_CRS/RMII_NULL	101: Reserved
			110: PJ_EINT11	111: IO Disable

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11	/	/	/
10:8	R/W	0x7	PJ10_SELECT 000: Input 001: Output 010: NCSI1_D6 011: Reserved 100: RGMII_TXD0/MII_TXD0/RMII_TXD0 101: Reserved 110: PJ_EINT10 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PJ9_SELECT 000: Input 001: Output 010: NCSI1_D5 011: SDC3_D2 100: RGMII_TXD1/MII_TXD1/RMII_TXD1 101: Reserved 110: PJ_EINT9 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PJ8_SELECT 000: Input 001: Output 010: NCSI1_D4 011: SDC3_D3 100: RGMII_TXD2/MII_TXD2/RMII_NULL 101: Reserved 110: PJ_EINT8 111: IO Disable

10.7.5.66. PJ Configure Register 2 (Default Value: 0x0000_0777)

Offset: 0x014C			Register Name: PJ_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:8	R/W	0x7	PJ18_SELECT 000: Input 001: Output 010: CSI_FSIN1 011: Reserved 100: Reserved 101: Reserved 110: PJ_EINT18 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PJ17_SELECT 000: Input 001: Output 010: NCSI1_SDA 011: TWI4_SDA 100: MDIO 101: Reserved 110: PJ_EINT17 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PJ16_SELECT 000: Input 001: Output 010: NCSI1_SCK 011: TWI4_SCK 100: MDC 101: Reserved 110: PJ_EINT16 111: IO Disable

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10.7.5.67. PJ Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: PJ_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.68. PJ Data Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: PJ_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	PJ_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.5.69. PJ Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0158			Register Name: PJ_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PJ15_DRV PJ15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PJ14_DRV PJ14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PJ13_DRV PJ13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PJ12_DRV PJ12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PJ11_DRV PJ11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PJ10_DRV

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			PJ10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PJ9_DRV PJ9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PJ8_DRV PJ8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PJ7_DRV PJ7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PJ6_DRV PJ6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PJ5_DRV PJ5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PJ4_DRV PJ4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PJ3_DRV PJ3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PJ2_DRV PJ2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PJ1_DRV PJ1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PJ0_DRV PJ0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

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10.7.5.70. PJ Multi-Driving Register 1 (Default Value: 0x0000_0015)

Offset: 0x015C			Register Name: PJ_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x1	PJ18_DRV PJ18 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PJ17_DRV PJ17 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PJ16_DRV PJ16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.5.71. PJ Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: PJ_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PJ15_PULL PJ15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PJ14_PULL PJ14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PJ13_PULL PJ13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PJ12_PULL PJ12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PJ11_PULL PJ11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PJ10_PULL

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			PJ10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PJ9_PULL PJ9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PJ8_PULL PJ8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PJ7_PULL PJ7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PJ6_PULL PJ6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PJ5_PULL PJ5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PJ4_PULL PJ4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PJ3_PULL PJ3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PJ2_PULL PJ2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PJ1_PULL PJ1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PJ0_PULL PJ0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

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10.7.5.72. PJ Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: PJ_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	PJ18_PULL PJ18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PJ17_PULL PJ17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PJ16_PULL PJ16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.5.73. PB External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: PB_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

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			0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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10.7.5.74. PB External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PB_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.75. PB External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PB_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.76. PB External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PB_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.77. PB External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PB_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	EINT9_CTL External INT9 Enable

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			0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.7.5.78. PB External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PB_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/

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9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

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0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.7.5.79. PB External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PB_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

10.7.5.80. PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG

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			External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.81. PF External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02A4			Register Name: PF_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:0	/	/	/

10.7.5.82. PF External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PF_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.83. PF External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: PF_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.84. PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable

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			0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.7.5.85. PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit

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			0: No IRQ pending 1: IRQ pending Write '1' to clear

10.7.5.86. PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

10.7.5.87. PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge

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			0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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10.7.5.88. PG External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: PG_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.89. PG External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02C8			Register Name: PG_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.90. PG External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02CC			Register Name: PG_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.91. PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable

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			1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable

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1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.7.5.92. PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

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10.7.5.93. PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PG_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

10.7.5.94. PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name:PH_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.95. PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4	Register Name: PH_EINT_CFG1

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Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge

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			0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.96. PH External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: PH_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode

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			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.97. PH External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: PH_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.98. PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable

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12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL

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			External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.7.5.99. PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS

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			External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS

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			External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.7.5.100. PH External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

10.7.5.101. PJ External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name:PJ_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge

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			0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG

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			External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.102. PJ External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: PJ_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.103. PJ External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0328	Register Name: PJ_EINT_CFG2

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Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.5.104. PJ External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x032C			Register Name: PJ_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.5.105. PJ External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: PJ_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable

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17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL

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			External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.7.5.106. PJ External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: PJ_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
16	R/W1C	0x0	EINT16_STATUS

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			External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS

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			External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

10.7.5.107. PJ External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: PJ_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

10.7.6. CPUS Port Register List

Module Name	Base Address
R_GPIO	0x07022000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0 (n =0,1)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1 (n =0,1)
Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2 (n =0,1)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3 (n =0,1)
Pn_DAT	n*0x0024+0x10	Port n Data Register (n =0,1)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0 (n =0,1)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1 (n =0,1)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0 (n =0,1)
Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1 (n =0,1)
Pn_INT_CFG0	0x0200+n*0x20+0x00	PIO Interrupt Configure Register 0 (n =0,1)
Pn _INT_CFG1	0x0200+n*0x20+0x04	PIO Interrupt Configure Register 1 (n =0,1)
Pn _INT_CFG2	0x0200+n*0x20+0x08	PIO Interrupt Configure Register 2 (n =0,1)
Pn _INT_CFG3	0x0200+n*0x20+0x0C	PIO Interrupt Configure Register 3 (n =0,1)
Pn _INT_CTL	0x0200+n*0x20+0x10	PIO Interrupt Control Register (n =0,1)
Pn _INT_STA	0x0200+n*0x20+0x14	PIO Interrupt Status Register (n =0,1)
Pn _INT_DEB	0x0200+n*0x20+0x18	PIO Interrupt Debounce Register (n =0,1)

10.7.7. CPUS Register Description

10.7.7.1. PL Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0000			Register Name: PL_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PL7_SELECT

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			000: Input	001: Output
			010: S_JTAG_DI	011: Reserved
			100: Reserved	101: Reserved
			110: S_PL_EINT7	111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PL6_SELECT 000: Input 010: S_JTAG_DO 100: Reserved 110: S_PL_EINT6	 001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PL5_SELECT 000: Input 010: S_JTAG_CK 100: Reserved 110: S_PL_EINT5	 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PL4_SELECT 000: Input 010: S_JTAG_MS 100: Reserved 110: S_PL_EINT4	 001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PL3_SELECT 000: Input 010: S_UART0_RX 100: Reserved 110: S_PL_EINT3	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PL2_SELECT 000: Input 010: S_UART0_TX 100: Reserved 110: S_PL_EINT2	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PL1_SELECT 000: Input 010: S_RSB_SDA 100: Reserved 110: S_PL_EINT1	 001: Output 011: S_TWI0_SDA 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PL0_SELECT 000: Input 010: S_RSB_SCK	 001: Output 011: S_TWI0_SCK

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			100: Reserved	101: Reserved
			110: S_PL_EINT0	111: IO Disable

10.7.7.2. PL Configure Register 1 (Default Value: 0x0000_0077)

Offset: 0x0004			Register Name: PL_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:7	/	/	/	
6:4	R/W	0x7	PL9_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT9	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL8_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT8	 001:Output 011:Reserved 101:Reserved 111:IO Disable

10.7.7.3. PL Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PL_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.7.4. PL Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PL_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.7.5. PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding

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			bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.7.6. PL Multi-Driving Register 0 (Default Value: 0x0005_5555)

Offset: 0x0014			Register Name: PL_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x1	PL9_DRV PL9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PL8_DRV PL8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PL7_DRV PL7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PL6_DRV PL6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PL5_DRV PL5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PL4_DRV PL4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PL3_DRV PL3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PL2_DRV PL2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PL1_DRV PL1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

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1:0	R/W	0x1	PL0_DRV PL0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

10.7.7.7. PL Multi-Driving Register 1 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: PL_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.7.8. PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x001C			Register Name: PL_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	PL9_PULL PL9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PL8_PULL PL8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PL7_PULL PL7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PL6_PULL PL6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PL5_PULL PL5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PL3_PULL PL3 Pull-up/down Select

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			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x1	PL1_PULL PL1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

10.7.7.9. PL Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PL_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.7.10. PM Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0024			Register Name: PM_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PM7_SELECT 000: Input 010: S_UART1_RTS 100: Reserved 110: S_PM_EINT7	 001: Output 011: S_PWM6 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PM6_SELECT 000: Input 010: S_UART1_RX 100: Reserved 110: S_PM_EINT6	 001: Output 011: S_PWM5 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PM5_SELECT 000: Input 010: S_UART1_TX 100: Reserved	 001: Output 011: S_PWM4 101: Reserved

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			110: S_PM_EINT5	111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PM4_SELECT 000: Input 010: S_SPI_MISO 100: Reserved 110: S_PM_EINT4	 001: Output 011: S_PWM3 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PM3_SELECT 000: Input 010: S_SPI_MOSI 100: Reserved 110: S_PM_EINT3	 001: Output 011: S_PWM2 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PM2_SELECT 000: Input 010: S_SPI_CS 100: Reserved 110: S_PM_EINT2	 001: Output 011: S_PWM1 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PM1_SELECT 000: Input 010: S_SPI_CLK 100: Reserved 110: S_PM_EINT1	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PM0_SELECT 000: Input 010: S_PWM0 100: Reserved 110: S_PM_EINT0	 001: Output 011: Reserved 101: Reserved 111: IO Disable

10.7.7.11. PM Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0028			Register Name: PM_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PM15_SELECT 000: Input 010: S_CIR_RX 100: Reserved 110: S_PM_EINT15	 001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	

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26:24	R/W	0x7	PM14_SELECT 000: Input 010: Reserved 100: Reserved 110: S_PM_EINT14	 001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PM13_SELECT 000: Input 010: Reserved 100: Reserved 110: S_PM_EINT13	 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PM12_SELECT 000: Input 010: S_UART2_CTS 100: Reserved 110: S_PM_EINT12	 001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PM11_SELECT 000: Input 010: S_UART2_RTS 100: Reserved 110: S_PM_EINT11	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PM10_SELECT 000: Input 010: S_UART2_RX 100: Reserved 110: S_PM_EINT10	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PM9_SELECT 000: Input 010: S_UART2_TX 100: Reserved 110: S_PM_EINT9	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PM8_SELECT 000: Input 010: S_UART1_CTS 100: Reserved 110: S_PM_EINT8	 001: Output 011: S_PWM7 101: Reserved 111: IO Disable

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10.7.7.12. PM Configure Register 2 (Default Value: 0x7777_7777)

Offset: 0x002C			Register Name: PM_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	Reserved	
27	/	/	/	
26:24	R/W	0x7	Reserved	
23	/	/	/	
22:20	R/W	0x7	PM21_SELECT 000: Input 010: S_UART4_RX 100: Reserved 110: S_PM_EINT21	 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PM20_SELECT 000: Input 010: S_UART4_TX 100: Reserved 110: S_PM_EINT20	 001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PM19_SELECT 000: Input 010: S_UART3_CTS 100: Reserved 110: S_PM_EINT19	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PM18_SELECT 000: Input 010: S_UART3_RTS 100: Reserved 110: S_PM_EINT18	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PM17_SELECT 000: Input 010: S_UART3_RX 100: Reserved 110: S_PM_EINT17	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PM16_SELECT 000: Input 010: S_UART3_TX 100: Reserved 110: S_PM_EINT16	 001: Output 011: Reserved 101: Reserved 111: IO Disable

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10.7.7.13. PM Configure Register 3 (Default Value: 0x7777_7777)

Offset: 0x0030			Register Name: PM_CFG3	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PM31_SELECT 000: Input 010: R_WATCHDOG_SIG 100: Reserved 110: S_PM_EINT31	001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PM30_SELECT 000: Input 010: WATCHDOG_SIG 100: Reserved 110: S_PM_EINT30	001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PM29_SELECT 000: Input 010: S_TWI2_SDA 100: Reserved 110: S_PM_EINT29	001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PM28_SELECT 000: Input 010: S_TWI2_SCK 100: Reserved 110: S_PM_EINT28	001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PM27_SELECT 000: Input 010: S_TWI1_SDA 100: Reserved 110: S_PM_EINT27	001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PM26_SELECT 000: Input 010: S_TWI1_SCK 100: Reserved 110: S_PM_EINT26	001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PM25_SELECT	

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			000: Input 010: S_TWI0_SDA 100: Reserved 110: S_PM_EINT25	001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PM24_SELECT 000: Input 010: S_TWI0_SCK 100: Reserved 110: S_PM_EINT24	 001: Output 011: Reserved 101: Reserved 111: IO Disable

10.7.7.14. PM Data Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PM_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PM_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

10.7.7.15. PM Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0038			Register Name: PM_DRV0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x1	PM15_DRV PM15 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
29:28	R/W	0x1	PM14_DRV PM14 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
27:26	R/W	0x1	PM13_DRV PM13 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
25:24	R/W	0x1	PM12_DRV PM12 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
23:22	R/W	0x1	PM11_DRV	

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			PM11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PM10_DRV PM10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PM9_DRV PM9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PM8_DRV PM8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PM7_DRV PM7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PM6_DRV PM6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PM5_DRV PM5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PM4_DRV PM4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PM3_DRV PM3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PM2_DRV PM2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PM1_DRV PM1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PM0_DRV PM0 Multi-Driving Select

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			00: Level 0	01: Level 1
			10: Level 2	11: Level 3

10.7.7.16. PM Multi-Driving Register 1 (Default Value: 0x5555_5555)

Offset: 0x003C			Register Name: PM_DRV1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x1	PM31_DRV PM31 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
29:28	R/W	0x1	PM30_DRV PM30 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
27:26	R/W	0x1	PM29_DRV PM29 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
25:24	R/W	0x1	PM28_DRV PM28 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
23:22	R/W	0x1	PM27_DRV PM27 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
21:20	R/W	0x1	PM26_DRV PM26 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
19:18	R/W	0x1	PM25_DRV PM25 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
17:16	R/W	0x1	PM24_DRV PM24 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
15:14	R/W	0x1	Reserved	
13:12	R/W	0x1	Reserved	
11:10	R/W	0x1	PM21_DRV PM21 Multi-Driving Select	

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			00: Level 0 10: Level 2	01: Level 1 11: Level 3
9:8	R/W	0x1	PM20_DRV PM20 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PM19_DRV PM19 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PM18_DRV PM18 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PM17_DRV PM17 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PM16_DRV PM16 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

10.7.7.17. PM Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PM_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x0	PM15_PULL PM15 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
29:28	R/W	0x0	PM14_PULL PM14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PM13_PULL PM13 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PM12_PULL PM12 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PM11_PULL	

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			PM11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PM10_PULL PM10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PM9_PULL PM9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PM8_PULL PM8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PM7_PULL PM7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PM6_PULL PM6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PM5_PULL PM5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PM4_PULL PM4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PM3_PULL PM3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PM2_PULL PM2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PM1_PULL PM1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PM0_PULL PM0 Pull-up/down Select

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			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved

10.7.7.18. PM Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: PM_PULL1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x0	PM31_PULL PM31 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
29:28	R/W	0x0	PM30_PULL PM30 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PM29_PULL PM29 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
25:24	R/W	0x0	PM28_PULL PM28 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
23:22	R/W	0x0	PM27_PULL PM27 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
21:20	R/W	0x0	PM26_PULL PM26 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
19:18	R/W	0x0	PM25_PULL PM25 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
17:16	R/W	0x0	PM24_PULL PM24 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	Reserved	
13:12	R/W	0x0	Reserved	
11:10	R/W	0x0	PM21_PULL PM21 Pull-up/down Select	

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			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PM20_PULL PM20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PM19_PULL PM19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PM18_PULL PM18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PM17_PULL PM17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PM16_PULL PM16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

10.7.7.19. PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name:PL_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG

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			External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

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			0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.7.20. PL External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0204			Register Name: PL_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.7.21. PL External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0208			Register Name: PL_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

10.7.7.22. PL External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x020C			Register Name: PL_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

10.7.7.23. PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210	Register Name: PL_EINT_CTL

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Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

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10.7.7.24. PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

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1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

10.7.7.25. PL External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

10.7.7.26. PM External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0220			Register Name:PM_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level

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			0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode

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			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.7.27. PM External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: PM_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG

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			External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.7.28. PM External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0228			Register Name: PM_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	Reserved
27:24	R/W	0x0	Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

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			0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

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10.7.7.29. PM External Interrupt Configure Register 3 (Default Value: 0x0000_0000)

Offset: 0x022C			Register Name: PM_EINT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT31_CFG External INT31 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT30_CFG External INT30 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT29_CFG External INT29 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT28_CFG External INT28 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT27_CFG External INT27 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT26_CFG

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			External INT26 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT25_CFG External INT25 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT24_CFG External INT24 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

10.7.7.30. PM External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: PM_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EINT31_CTL External INT31 Enable 0: Disable 1: Enable
30	R/W	0x0	EINT30_CTL External INT30 Enable 0: Disable 1: Enable
29	R/W	0x0	EINT29_CTL External INT29 Enable 0: Disable 1: Enable
28	R/W	0x0	EINT28_CTL External INT28 Enable 0: Disable 1: Enable

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27	R/W	0x0	EINT27_CTL External INT27 Enable 0: Disable 1: Enable
26	R/W	0x0	EINT26_CTL External INT26 Enable 0: Disable 1: Enable
25	R/W	0x0	EINT25_CTL External INT25 Enable 0: Disable 1: Enable
24	R/W	0x0	EINT24_CTL External INT24 Enable 0: Disable 1: Enable
23	R/W	0x0	Reserved
22	R/W	0x0	Reserved
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable

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			1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable

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3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

10.7.7.31. PM External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: PM_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	EINT31_STATUS External INT31 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
30	R/W1C	0x0	EINT30_STATUS External INT30 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
29	R/W1C	0x0	EINT29_STATUS External INT29 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
28	R/W1C	0x0	EINT28_STATUS External INT28 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
27	R/W1C	0x0	EINT27_STATUS External INT27 Pending Bit 0: No IRQ pending

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			1: IRQ pending Write ‘1’ to clear
26	R/W1C	0x0	EINT26_STATUS External INT26 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
25	R/W1C	0x0	EINT25_STATUS External INT25 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
24	R/W1C	0x0	EINT24_STATUS External INT24 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
23	R/W1C	0x0	EINT23_STATUS External INT23 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
22	R/W1C	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
21	R/W1C	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
20	R/W1C	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
19	R/W1C	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending

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			1: IRQ pending Write ‘1’ to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending

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			1: IRQ pending Write ‘1’ to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending

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			1: IRQ pending Write '1' to clear

10.7.7.32. PM External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: PM_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

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10.8. GPADC

10.8.1. Overview

The General Purpose ADC(GPADC) is one analog to digital converter with 12-bit sampling resolution. This ADC is a type of successive approximation register (SAR) converter.

The GPADC has the following features:

- 12-bit resolution
- 8-bit effective SAR type A/D converter
- 64 FIFO depth of data register
- Power supply voltage: 3.0V
- Analog input range: 0 V to 3.0 V
- Maximum sampling frequency: 1 MHz
- Supports data compare and interrupt
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

10.8.2. Block Diagram

Figure 10-30 shows the block diagram of the GPADC.

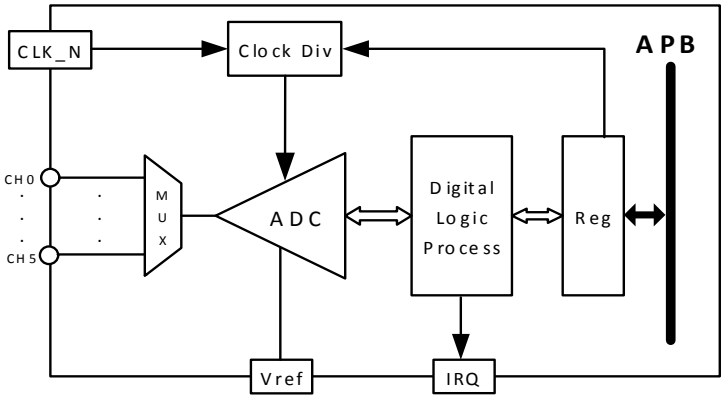

Figure 10- 30. GPADC Block Diagram

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10.8.3. Operations and Functional Descriptions

10.8.3.1. External Signals

Table 10-16 describes the external signals of GPADC.

Table 10- 16. GPADC External Signals

Signal	Description	Type
GPADC0	ADC Input Channel0	AI
GPADC1	ADC Input Channel1	AI
GPADC2	ADC Input Channel2	AI
GPADC3	ADC Input Channel3	AI
GPADC4	ADC Input Channel4	AI
GPADC5	ADC Input Channel5	AI

10.8.3.2. Clock Sources

GPADC has one clock source. Table 10-17 describes the clock source for GPADC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 10- 17. GPADC Clock Sources

Clock Sources	Description
OSC24M	24MHz

10.8.3.3. GPADC Work Mode

(1).Single conversion mode

GPADC completes one conversion in specified channel, the converted data is updated at the data register of corresponding channel.

(2).Continuous conversion mode

GPADC has continuous conversion in specified channel until the software stops, the converted data is updated at the data register of corresponding channel.

(3).Burst conversion mode

GPADC samples and converts in the specified channel, and sequentially stores the results in FIFO.

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10.8.3.4. Clock and Timing Requirements

CLK_IN = 24MHz
CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)
TACQ> 10RC (R is output impedance of ADC sample circuit, C= 6.4pF)
ADC Sample Frequency > TACQ+CONV_TIME

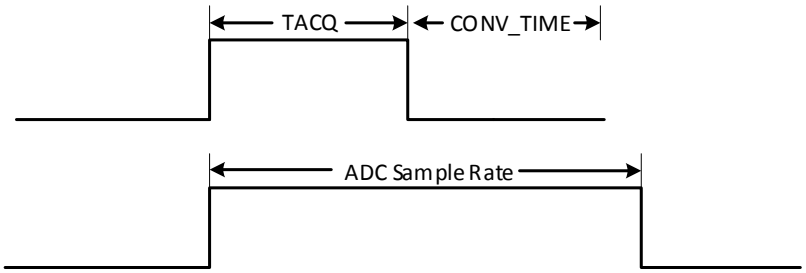

Figure 10- 31. GPADC Clock and Timing Requirement

10.8.3.5. GPADC Calculate Formula

GPADC calculate formula: GPADC_DATA = Vin/V_{REF}*4095
Where:
V_{REF}=3.0V

10.8.4. Programming Guidelines

GPADC initial process is as follows.

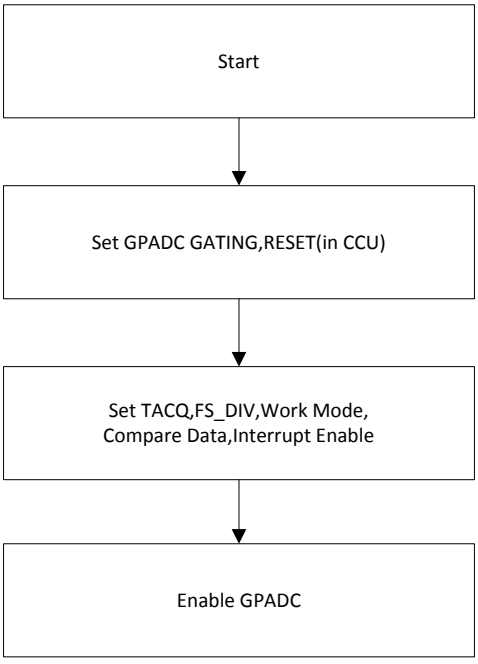

Figure 10- 32. GPADC Initial Process

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(1).Query Mode

Step1: Write 0x1 to the bit[16] of **GPADC_BGR_REG(0x030019EC)** to dessert reset.
Step2: Write 0x1 to the bit[0] of **GPADC_BGR_REG(0x030019EC)** to open GPADC clock.
Step3: Write 0x2F to the bit[15:0] of **GP_SR_CON** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **GP_SR_CON** to set ADC sample frequency divider.
Step5: Write 0x2 to the bit[19:18] of **GP_CTRL** to set continuous conversion mode.
Step6: Write 0x1 to the bit[0] of **GP_CS_EN** to enable analog input channel select.
Step7: Write 0x1 to the bit[16] of **GP_CTRL** to enable ADC.
Step8: Read the bit[0] of **GP_DATA_INTS**, if the bit is 1, then data conversion is complete.
Step9: Read the bit[11:0] of **GP_CH0_DATA**, calculate voltage value based on GPADC calculate formula.

(2).Interrupt Mode

Step1: Write 0x1 to the bit[16] of **GPADC_BGR_REG(0x030019EC)** to dessert reset.
Step2: Write 0x1 to the bit[0] of **GPADC_BGR_REG(0x030019EC)** to open GPADC clock.
Step3: Write 0x2F to the bit[15:0] of **GP_SR_CON** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **GP_SR_CON** to set ADC sample frequency divider.
Step5: Write 0x2 to the bit[19:18] of **GP_CTRL** to set continuous conversion mode.
Step6: Write 0x1 to the bit[0] of **GP_CS_EN** to enable analog input channel select.
Step7: Write 0x1 to the bit[0] of **GP_DATA_INTC** to enable GPADC data interrupt.
Step8: Set GIC interface based on IRQ 32, write 0x1 to the bit[0] of the **0x03021100** register .
Step9: Put interrupt handler address into interrupt vector table.
Step10: Write 0x1 to the bit16 of **GP_CTRL** to enable ADC function.
Step11: Read the bit[11:0] of **GP_CH0_DATA** from the interrupt handler, calculate voltage value based on GPADC calculate formula.

10.8.5. Register List

Module Name	Base Address
GPADC	0x05070000

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register

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GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register
GP_CH2_CMP_DATA	0x0048	GPADC CH2 Compare Data Register
GP_CH3_CMP_DATA	0x004C	GPADC CH3 Compare Data Register
GP_CH4_CMP_DATA	0x0050	GPADC CH4 Compare Data Register
GP_CH5_CMP_DATA	0x0054	GPADC CH5 Compare Data Register
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register
GP_CH2_DATA	0x0088	GPADC CH2 Data Register
GP_CH3_DATA	0x008C	GPADC CH3 Data Register
GP_CH4_DATA	0x0090	GPADC CH4 Data Register
GP_CH5_DATA	0x0094	GPADC CH5 Data Register

10.8.6. Register Description

10.8.6.1. GPADC Sample Rate Configure Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 16	R/W	0x1DF	FS_DIV ADC sample frequency divider CLK_IN/(n+1) Default value: 50K
15:0	R/W	0x2F	TACQ ADC acquire time CLK_IN/(N+1) Default value: 2us

10.8.6.2. GPADC Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/ W	0x0	ADC_FIRST_DLY ADC First Convert Delay Setting ADC conversion of each channel is delayed by N samples.
23:22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias

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			Adjust the bandwidth of the ADC amplifier
19:18	R/W	0x0	GPADC Work Mode 00: Single conversion mode 01: Reserved 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: Start Calibration, it is cleared to 0 after calibration
16	R/W	0x0	ADC_EN ADC Function Enable. Before the bit is enabled, configure ADC parameters including the work mode and channel number,etc. 0: Disable 1: Enable
15:0	/	/	/

10.8.6.3. GPADC Compare and Select Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GP_CS_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	ADC_CH5_CMP_EN Channel5 Compare Enable 0: Disable 1: Enable
20	R/W	0x0	ADC_CH4_CMP_EN Channel4 Compare Enable 0: Disable 1: Enable
19	R/W	0x0	ADC_CH3_CMP_EN Channel 3 Compare Enable 0: Disable 1: Enable
18	R/W	0x0	ADC_CH2_CMP_EN Channel 2 Compare Enable 0: Disable 1: Enable
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable

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			0: Disable 1: Enable
15:6	/	/	/
5	R/W	0x0	ADC_CH5_SELECT Analog input channel 5 Select 0: Disable 1: Enable
4	R/W	0x0	ADC_CH4_SELECT Analog input channel 4 Select 0: Disable 1: Enable
3	R/W	0x0	ADC_CH3_SELECT Analog input channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CH2_SELECT Analog input channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CH1_SELECT Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x0	ADC_CH0_SELECT Analog input channel 0 Select 0: Disable 1: Enable

10.8.6.4. GPADC FIFO Interrupt Control Register (Default Value: 0x0000_1F00)

Offset: 0x000C			**Register Name: GP_FIFO_INTC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL

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			Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/W1C	0x0	FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, clear automatically to '0'.
3:0	/	/	/

10.8.6.5. GPADC FIFO Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING ADC FIFO Overrun IRQ Pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
16	R/W1C	0x0	FIFO_DATA_PENDING ADC FIFO Data Available Pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
15:14	/	/	/
13:8	R	0x0	RXA_CNT ADC FIFO available sample word counter
7:0	/	/	/

10.8.6.6. GPADC FIFO Data Register

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	UDF	GP_FIFO_DATA GPADC Data in FIFO

10.8.6.7. GPADC Calibration Data Register (Default Value: 0x0000_0000)

Offset: 0x0018	Register Name: GP_CDATA

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Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	GP_CDATA GPADC Calibration Data

10.8.6.8. GPADC Low Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	CH5_LOW_IRQ_EN 0: Disable 1: Enable
4	R/W	0x0	CH4_LOW_IRQ_EN 0: Disable 1: Enable
3	R/W	0x0	CH3_LOW_IRQ_EN 0: Disable 1: Enable
2	R/W	0x0	CH2_LOW_IRQ_EN 0: Disable 1: Enable
1	R/W	0x0	CH1_LOW_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_LOW_IRQ_EN 0: Disable 1: Enable

10.8.6.9. GPADC High Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	CH5_HIG_IRQ_EN 0: Disable 1: Enable
4	R/W	0x0	CH4_HIG_IRQ_EN 0: Disable 1: Enable
3	R/W	0x0	CH3_HIG_IRQ_EN 0: Disable

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			1: Enable
2	R/W	0x0	CH2_HIG_IRQ_EN 0: Disable 1: Enable
1	R/W	0x0	CH1_HIG_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_HIG_IRQ_EN 0: Disable 1: Enable

10.8.6.10. GPADC DATA Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	CH5_DATA_IRQ_EN 0: Disable 1: Enable
4	R/W	0x0	CH4_DATA_IRQ_EN 0: Disable 1: Enable
3	R/W	0x0	CH3_DATA_IRQ_EN 0: Disable 1: Enable
2	R/W	0x0	CH2_DATA_IRQ_EN 0: Disable 1: Enable
1	R/W	0x0	CH1_DATA_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_DATA_IRQ_EN 0: Disable 1: Enable

10.8.6.11. GPADC Low Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	CH5_LOW_PENGDING 1: Channel 5 Voltage Low Available Pending IRQ

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			Write ‘1’ to clear this interrupt or automaticlly clear if interrupt condition fails.
4	R/W1C	0x0	CH4_LOW_PENGDING 1: Channel 4 Voltage Low Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
3	R/W1C	0x0	CH3_LOW_PENGDING 1: Channel 3 Voltage Low Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	CH2_LOW_PENGDING 1: Channel 2 Voltage Low Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
1	R/W1C	0x0	CH1_LOW_PENGDING 1: Channel 1 Voltage Low Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_LOW_PENGDING 1: Channel 0 Voltage Low Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.

10.8.6.12. GPADC High Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	CH5_HIG_PENGDING 0: No Pending IRQ 1: Channel 5 Voltage High Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
4	R/W1C	0x0	CH4_HIG_PENGDING 0: No Pending IRQ 1: Channel 4 Voltage High Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
3	R/W1C	0x0	CH3_HIG_PENGDING 0: No Pending IRQ 1: Channel 3 Voltage High Available Pending IRQ Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	CH2_HIG_PENGDING

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			0: No Pending IRQ 1: Channel 2 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
1	R/W1C	0x0	CH1_HIG_PENGDING 0: No Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_HIG_PENGDING 0: No Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

10.8.6.13. GPADC Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	CH5_DATA_PENGDING 0: No Pending IRQ 1: Channel 5 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
4	R/W1C	0x0	CH4_DATA_PENGDING 0: No Pending IRQ 1: Channel 4 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
3	R/W1C	0x0	CH3_DATA_PENGDING 0: No Pending IRQ 1: Channel 3 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	CH2_DATA_PENGDING 0: No Pending IRQ 1: Channel 2 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
1	R/W1C	0x0	CH1_DATA_PENGDING 0: No Pending IRQ 1: Channel 1 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition

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			fails.
0	R/W1C	0x0	CH0_DATA_PENGDING 0: No Pending IRQ 1: Channel 0 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

10.8.6.14. GPADC CH0 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0040			Register Name: GP_CH0_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

10.8.6.15. GPADC CH1 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0044			Register Name: GP_CH1_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

10.8.6.16. GPADC CH2 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0048			Register Name: GP_CH2_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH2_CMP_HIG_DATA Channel 2 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH2_CMP_LOW_DATA Channel 2 Voltage Low Value

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10.8.6.17. GPADC CH3 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x004C			Register Name: GP_CH3_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH3_CMP_HIG_DATA Channel 3 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH3_CMP_LOW_DATA Channel 3 Voltage Low Value

10.8.6.18. GPADC CH4 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0050			Register Name: GP_CH4_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH4_CMP_HIG_DATA Channel 4 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH4_CMP_LOW_DATA Channel 4 Voltage Low Value

10.8.6.19. GPADC CH5 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0054			Register Name: GP_CH5_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH5_CMP_HIG_DATA Channel 5 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH5_CMP_LOW_DATA Channel 5 Voltage Low Value

10.8.6.20. GPADC CH0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GP_CH0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

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10.8.6.21. GPADC CH1 Data Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

10.8.6.22. GPADC CH2 Data Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: GP_CH2_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH2_DATA Channel 2 Data

10.8.6.23. GPADC CH3 Data Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: GP_CH3_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH3_DATA Channel 3 Data

10.8.6.24. GPADC CH4 Data Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: GP_CH4_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH4_DATA Channel 4 Data

10.8.6.25. GPADC CH5 Data Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: GP_CH5_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x000	GP_CH5_DATA Channel 5 Data

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10.9. LRADC

10.9.1. Overview

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 250Hz conversion rate.

Features:

- One LRADC controller with 2 input channels
- 6-bit resolution
- Sample rate up to 250Hz
- Supports hold Key and general Key
- Supports normal,continue and single work mode
- Voltage input range between 0 to 2.0V
- Power supply voltage:3.0V, reference voltage:2.0V
- Interrupt support

10.9.2. Block Diagram

Figure 10-33 shows the block diagram of the LRADC.

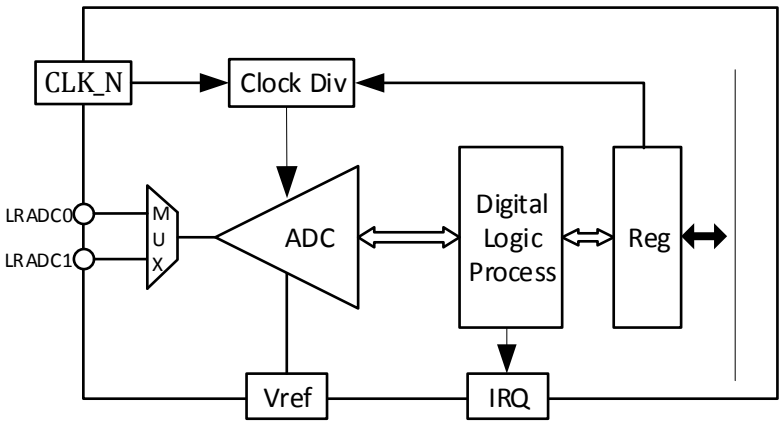

Figure 10- 33. LRADC Block Diagram

10.9.3. Operations and Functional Descriptions

10.9.3.1. External Signals

Table 10-18 describes the external signals of the LRADC. The LRADC pin is the analog input signal.

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Table 10- 18. LRADC External Signals

Signal	Description	Type
LRADC0	Analog Input Channel0	AI
LRADC1	Analog Input Channel1	AI

10.9.3.2. Clock Sources

The LRADC has one clock source. Table 10-19 describes the clock source for LRADC.

Table 10- 19. LRADC Clock Sources

Clock Sources	Description
LOSC	32.768 kHz LOSC

10.9.3.3. LRADC Work Mode

(1).Normal Mode

ADC gathers 8 samples,the average of the 8 samples is updated in data register,and the data interrupt sign is enabled.It is sampled repeatedly according to this mode until ADC stop.

(2).Continue Mode

ADC gathers 8 samples every other 8*(N+1) sample cycle. The average of every 8 samples is updated in the data register, and the data interrupt sign is enabled. (N is defined in the bit[19:16] of **LRADC_CTRL_REG**).

(3).Single Mode

ADC gathers 8 samples, the average of the 8 samples is updated in data register, and the data interrupt sign is enabled, since then ADC stops sample.

10.9.3.4. Interrupt

Each LRADC channel has five interrupt sources and five interrupt enable controls.

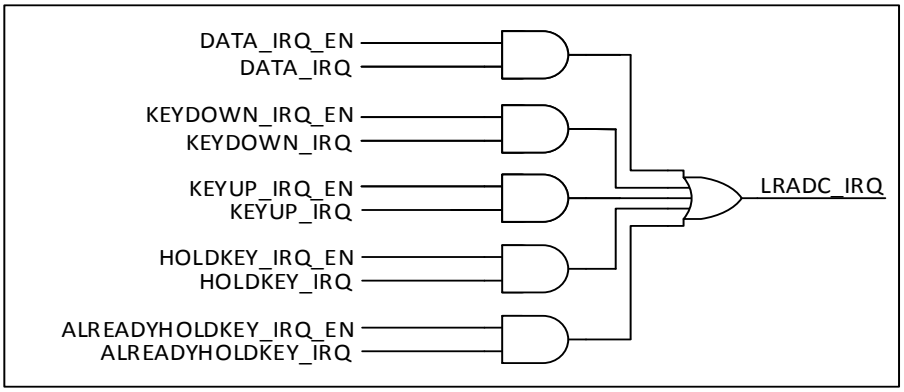

Figure 10- 34. LRADC Interrupt

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When input voltage is between LEVELA(2.0V) and LEVELB(control by the bit[5:4] of LRADC_CTRL), IRQ1 can be generated. When input voltage is lower than LEVELB, IRQ2 can be generated.

If the controller receives IRQ1, and does not receive IRQ2 at some time, then the controller will generate Hold KEY Interrupt, otherwise DATA_IRQ Interrupt.

Hold KEY usually is used for self-locking key.When self-locking key holds locking status, the controller receives IRQ2, then the controller will generate Already Hold Key Interrupt.

10.9.4. Programming Guidelines

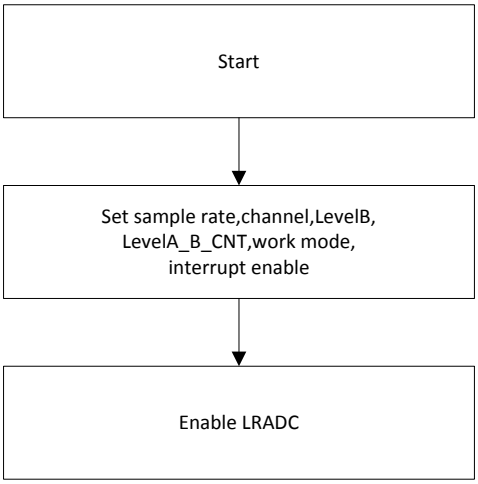

Figure 10- 35. LRADC Initial Process

(1) Set CONTINUE_TIME_SELECT when LRADC works in continue mode.

(2) The range of input voltage is from 0 to LEVELB.

(3) Calculation formula: LRADC_DATA = Vin/V_{REF}*63, V_{REF}=2.0V

(4) LRADC has 6-bit resolution,1-bit offset error, 1-bit quantizing error. After LRADC calibrates 1-bit offset error, LRADC has 5-bit resolution.

10.9.5. Register List

Module Name	Base Address
R_LRADC	0x07030800

Register Name	Offset	Description
LRADC_CTRL	0x0000	LRADC Control Register
LRADC_INTC	0x0004	LRADC Interrupt Control Register
LRADC_INTS	0x0008	LRADC Interrupt Status Register
LRADC_DATA0	0x000C	LRADC Data Register0
LRADC_DATA1	0x0010	LRADC Data Register1

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10.9.6. Register Description

10.9.6.1. LRADC Control Register (Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: LRADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 24	R/W	0x1	FIRST_CONVERT_DLY ADC First Convert Delay Setting ADC conversion is delayed by n samples.
23:22	R/W	0x0	ADC_CHANNEL_SELECT ADC Channel Select 00: LRADC0 Channel 01: LRADC1 Channel 1x: LRADC0 & LRADC1 Channel
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT Continue Mode Time Select One of 8*(N+1) sample as a valuable sample data.
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT Key Mode Select 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples.
7	R/W	0x0	LRADC_HOLD_KEY_EN LRADC Hold KEY Enable 0: Disable 1: Enable
6	R/W	0x1	LRADC_CHANNEL_EN LRADC Channel Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value Setting (the real voltage value) 00: 0x3C (~1.904V) 01: 0x39 (~1.81V) 10: 0x36 (~1.714V) 11: 0x33 (~1.62V)
3: 2	R/W	0x2	LRADC_SAMPLE_RATE LRADC Sample Rate 00: 250 Hz 01: 125 Hz

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			10: 62.5 Hz 11: 31.25 Hz
1	/	/	/
0	R/W	0x0	LRADC_EN LRADC Enable 0: Disable 1: Enable

10.9.6.2. LRADC Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LRADC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	ADC1_KEYUP_IRQ_EN ADC1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN ADC1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC1_HOLD_IRQ_EN ADC1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYDOWN_EN ADC1 Key Down Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN ADC1 Data IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN ADC0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN ADC0 Already Hold Key IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN

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			ADC0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN ADC0 Data IRQ Enable 0: Disable 1: Enable

10.9.6.3. LRADC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LRADC_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W1C	0x0	ADC1_KEYUP_PENDING ADC1 Key up Pending Bit When general key is pulled up, and the corresponding interrupt is enabled, the status bit is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
11	R/W1C	0x0	ADC1_ALRDY_HOLD_PENDING ADC1 Already Hold Pending Bit When hold key is pulled down and the general key is pulled down, and the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
10	R/W1C	0x0	ADC1_HOLDKEY_PENDING ADC1 Hold Key Pending Bit When hold key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
9	R/W1C	0x0	ADC1_KEYDOWN_PENDING ADC1 Key Down IRQ Pending Bit When general key pull down, and the corresponding interrupt is enabled,

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			the status bit is set and the interrupt line is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
8	R/W1C	0x0	ADC1_DATA_PENDING ADC1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
7:5	/	/	/
4	R/W1C	0x0	ADC0_KEYUP_PENDING ADC0 Key up Pending Bit When general key is pulled up, and the corresponding interrupt is enabled, the status bit is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W1C	0x0	ADC0_ALRDY_HOLD_PENDING ADC0 Already Hold Pending Bit When hold key is pulled down and the general key is pulled down, and the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC0_HOLDKEY_PENDING ADC0 Hold Key Pending Bit When hold key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W1C	0x0	ADC0_KEYDOWN_PENDING ADC0 Key Down IRQ Pending Bit When general key is pulled down, and the corresponding interrupt is enabled, the status bit is set and the interrupt line is set. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	ADC0_DATA_PENDING

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			ADC0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

10.9.6.4. LRADC Data Register0 (Default Value: 0x0000_003F)

Offset: 0x000C			Register Name: LRADC_DATA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x3F	LRADC0_DATA LRADC0 Data

10.9.6.5. LRADC Data Register1 (Default Value: 0x0000_003F)

Offset: 0x0010			Register Name: LRADC_DATA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x3F	LRADC1_DATA LRADC1 Data

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10.10. CIR Receiver

10.10.1. Overview

The CIR (Consumer Infrared) receiver is a capturer of the pulse from IR Receiver module and uses Run-Length Code (RLC) to encode the pulse. The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' and the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

In the air, there is always some noise. One threshold can be set to filter the noise to reduce system loading and improve the system stability.

The CIR receiver has the following features:

- Full physical layer implementation
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Programmable FIFO thresholds
- Interrupt support
- Sample clock up to 1 MHz

10.10.2. Block Diagram

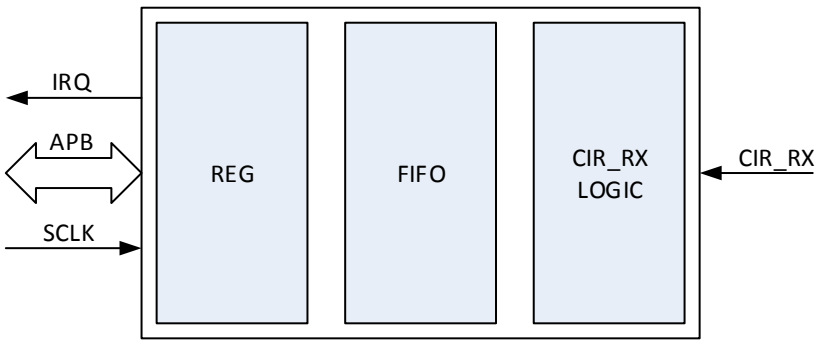

Figure 10- 36. CIR Receiver Block Diagram

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10.10.3. Operations and Functional Descriptions

10.10.3.1. External Signals

Table 10-20 describes the external signals of CIR Receiver.

Table 10- 20. CIR Receiver External Signals

Signal	Description	Type
S_CIR_RX	CIR input signal	I

10.10.3.2. Clock Sources

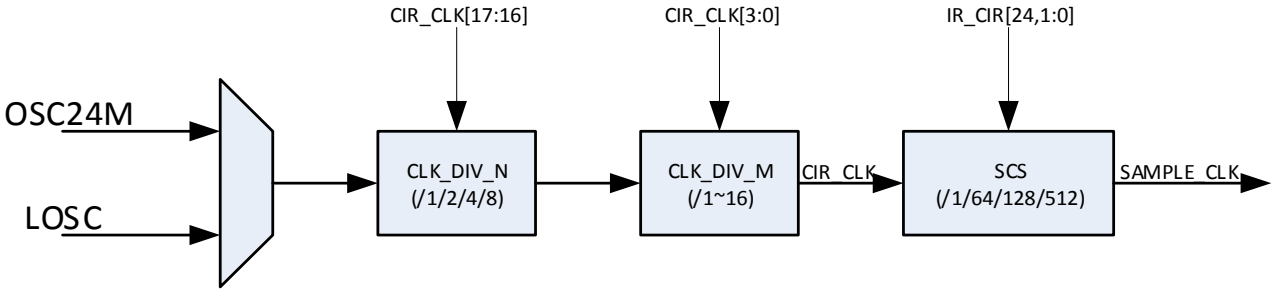

Figure 10- 37. CIR Receiver Clock

10.10.3.3. Typical Application

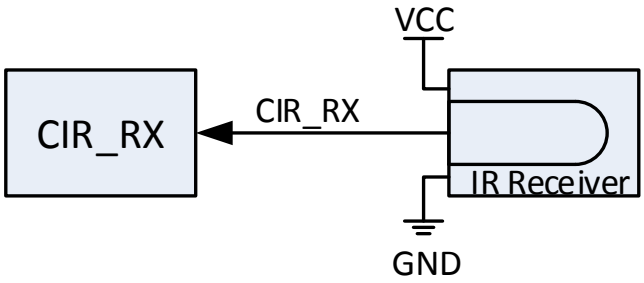

Figure 10- 38. CIR Receiver Application Diagram

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10.10.3.4. Function Implementation

Figure 10- 39. NEC Protocol

In fact, CIR receiver module is a timer with capture function.

When CIR_RX signals satisfy ATHR (Active Threshold), CIR receiver can start to capture. In the process, the signal is ignored if the pulse width of the signal is less than NTHR. when CIR_RX signals satisfy ITHR (Idle Threshold), the capture process is stopped and the Receiver Packet End interrupt is generated, then Receiver Packet End Flag is asserted.

In a capture process, every effective pulse is buffered to FIFO in bytes according to the form of Run-Length Code. The MSB bit of a byte is polarity of pulse, and the rest 7 bits is pulse width by taking Sample Clock as basic unit. This is the code form of RLC-Byte. When the level changes or the pulse width counting overflows, RLC-Byte is buffered to FIFO. The CIR_RX module receives infrared signals transmitted by the infrared remote control, the software decodes the signals.

10.10.3.5. Operating Mode

- **Sample Clock**

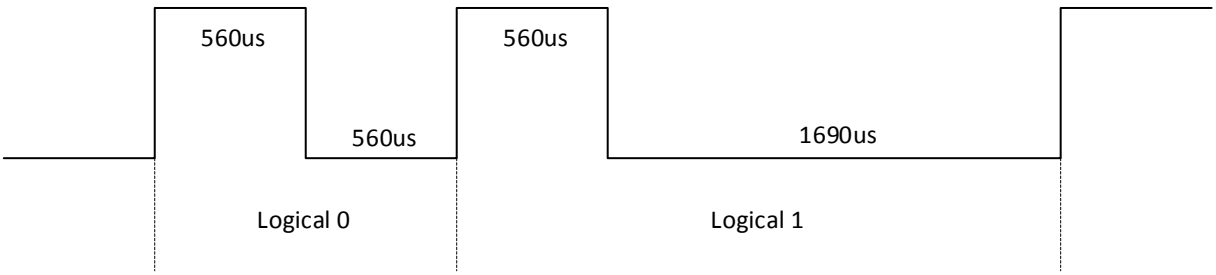

Figure 10- 40. Logical ‘0’ and Logical ‘1’ of NEC Protocol

For NEC protocol, a logical "1" takes 2.25ms(560us+1680us) to transmit, while a logical "0" is only half of that, being 1.12ms(560us+560us). For example, if sample clock is 31.25 kHz, sample cycle is 32us,then 18 sample cycles is 560us.So the RLC of 560us low level is 0x12, the RLC of 560us high level is 0x92. Then a logical “1” takes code 0x12 and code 0xb5 to transmit, a logical “0” takes code 0x12 and code 0x92 to transmit.

- **ATHR(Active Threshold)**

When CIR receiver is in Idle state,if electrical level of CIR_RX signal changes (positive jump or negative jump), and the duration reaches this threshold, then CIR takes the starting of the signal as a lead code, turns into active state and starts to capture CIR_RX signals.

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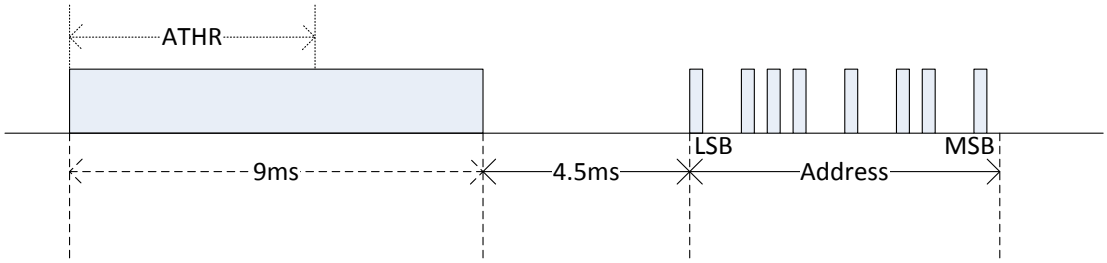

Figure 10- 41. ATHR Definition

- **ITHR(Idle Threshold)**

If electrical level of CIR_RX signals has no change, and the duration reaches this threshold, then CIR receiver enters into Idle state and ends this capture.

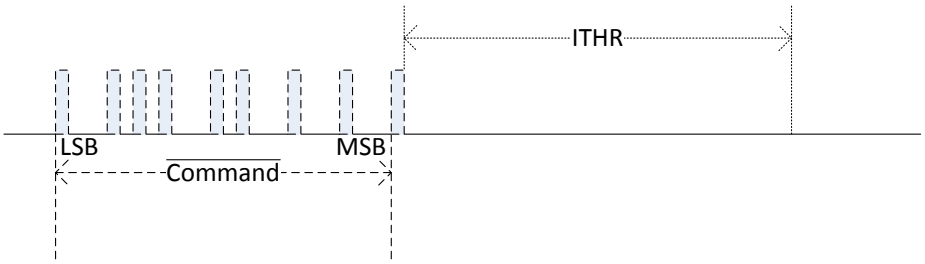

Figure 10- 42. ITHR Definition

- **NTHR(Noise Threshold)**

In capture process,the pulse is ignored if the pulse width is less than Noise Threshold.

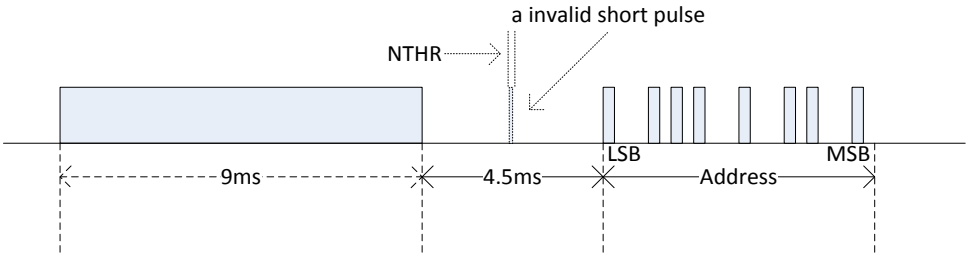

Figure 10- 43. NTHR Definition

- **APAM(Active Pulse Accept Mode)**

APAM is used to fit the type of lead code. If a pulse does not fit the type of lead code, it is not regarded as a lead code even if the pulse width reaches ATHR.

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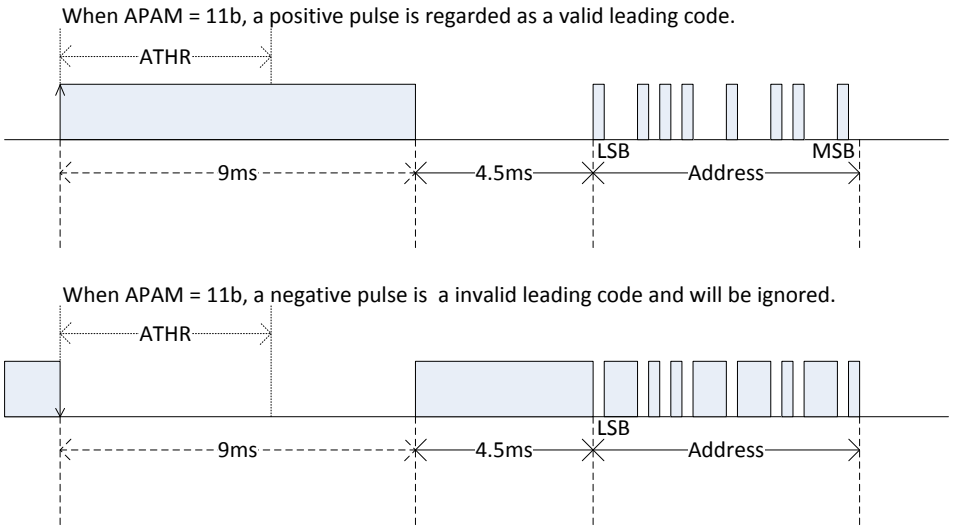

Figure 10- 44. APAM Definition

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10.10.4. Programming Guidelines

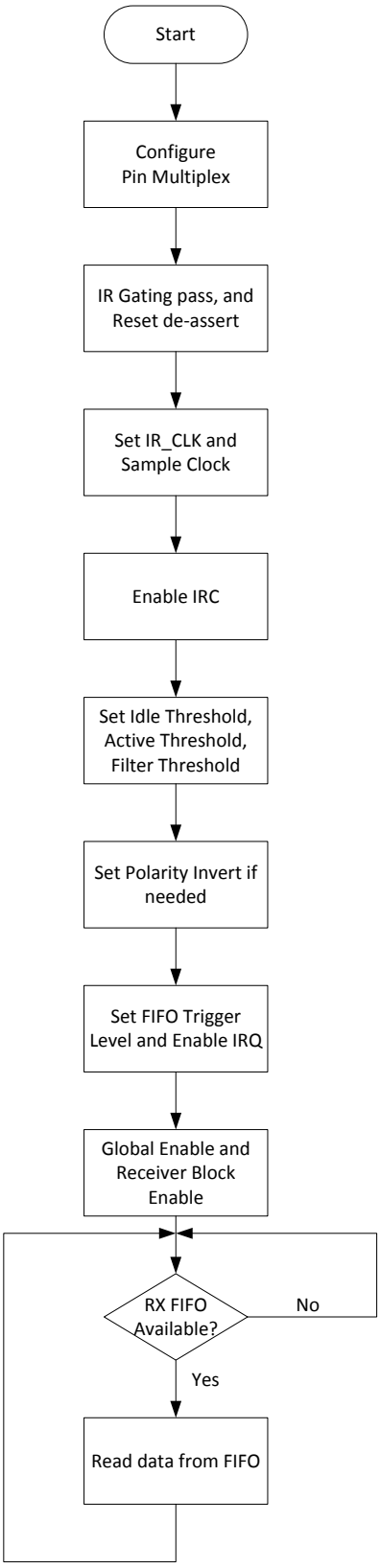

Figure 10- 45. CIR Receiver Process

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10.10.5. Register List

Module Name	Base Address
R_CIR_RX	0x07040000

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Control Register
CIR_RXPCFG	0x0010	CIR Receiver Pulse Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_RXCFG	0x0034	CIR Receiver Configure Register

10.10.6. Register Description

10.10.6.1. CIR Receiver Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	Active Pulse Accept Mode 00, 01: Both positive and negative pulses are valid as a leading code. 10: Only negative pulse is valid as a leading code. 11: Only positive pulse is valid as a leading code.
5:4	R/W	0x0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

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10.10.6.2. CIR Receiver Pulse Configure Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXPCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert 0: Do not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

10.10.6.3. CIR Receiver FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	Receiver Byte FIFO

10.10.6.4. CIR Receiver Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO available received byte level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable

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			1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

10.10.6.5. CIR Receiver Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R	0x0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0: Idle 1: Busy
6:5	/	/	/
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W1C	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

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10.10.6.6. CIR Receiver Configure Register(Default Value: 0x0000_1828)

<table>
<tr><td colspan="3">Offset: 0x0034</td><td>Register Name: CIR_RXCFG</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:25</td><td>/</td><td>/</td><td>/</td></tr>
<tr><td>24</td><td>R/W</td><td>0x0</td><td>SCS2
Bit2 of Sample Clock Select for CIR
This bit is defined by SCS bits below.</td></tr>
<tr><td>23</td><td>R/W</td><td>0x0</td><td>ATHC
Active Threshold Control for CIR
0: ATHR in unit of (Sample Clock)
1: ATHR in unit of (128*Sample Clocks)</td></tr>
<tr><td>22:16</td><td>R/W</td><td>0x0</td><td>ATHR
Active Threshold for CIR
These bits control the duration of CIR from idle to active state. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).</td></tr>
<tr><td>15:8</td><td>R/W</td><td>0x18</td><td>ITHR
Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xA</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.
0: all samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0x0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CIR_CLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>CIR_CLK /128</td></tr>
</table></td></tr>
</table>

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			0	1	0	CIR_CLK /256	
			0	1	1	CIR_CLK /512	
			1	0	0	CIR_CLK	
			1	0	1	Reserved	
			1	1	0	Reserved	
			1	1	1	Reserved	

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10.11. PWM

10.11.1. Overview

The PWM controller has 8 PWM channels(PWM0,PWM1,PWM2,PWM3,PWM4,PWM5,PWM6,PWM7), and divides to 4 PWM pairs:PWM01 pair,PWM23 pair,PWM45 pair,PWM67 pair.PWM01 pair consists of PWM0 and PWM1, PWM23 pair consists of PWM2 and PWM3, PWM45 pair consists of PWM4 and PWM5, PWM67 pair consists of PWM6 and PWM7.Each PWM pair built-in 1 clock module, 2 timer logic module and 1 programmable dead-time generator.

Each PWM channel supports two functions including PWM output and capture input.The clock sources of PWM channel have OSC24M and APB1.PWM channel can output single-pulse waveform or long-period waveform,the frequency range of the output waveform is from 0Hz to 24/100MHz.PWM also can capture input waveform.PWM channel captures the current value of 16-bit adding-counter at the external rising edge, and loads it to Capture Rise Lock Register, PWM channel captures the current value of 16-bit adding-counter at the external falling edge,and loads it to Capture Fall Lock Register,then the frequency of the external clock can be calculated accurately by the value of Capture Rise Lock Register and Capture Fall Lock Register.

PWM pair can output complementary waveform pair or dead-time PWM pair. When the two channels at a PWM pair have the same prescale, the same period register and opposite active state, then the PWM pair outputs a complementary wareform pair; When the programmable dead-time generator of PWM pair is enabled,then the PWM pair outputs the waveform pair with dead-time, and the dead-time is controllable.

PWM channel can configure to generate interrupt. PWM is as output function, when 16-bit adding-counter is equal to the value of entire cycle, PWM channel can be enabled to generate interrupt. PWM is as input function, when PWM channel captures the external rising edge, PWM channel can be enabled to generate one interrupt; when PWM channel captures the external falling edge, PWM channel can be enabled to generated one interrupt;when PWM channel captures rising edge or falling edge,PWM can trigger interrupt.

The PWM has the following features:

- 8 PWM channels(4 PWM pairs)
- Supports pulse,cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform,pulse waveform and complementary pair
- Output frequency range: 0~ 24MHz/100MHz
- Various duty-cycle: 0% ~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

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10.11.2. Block Diagram

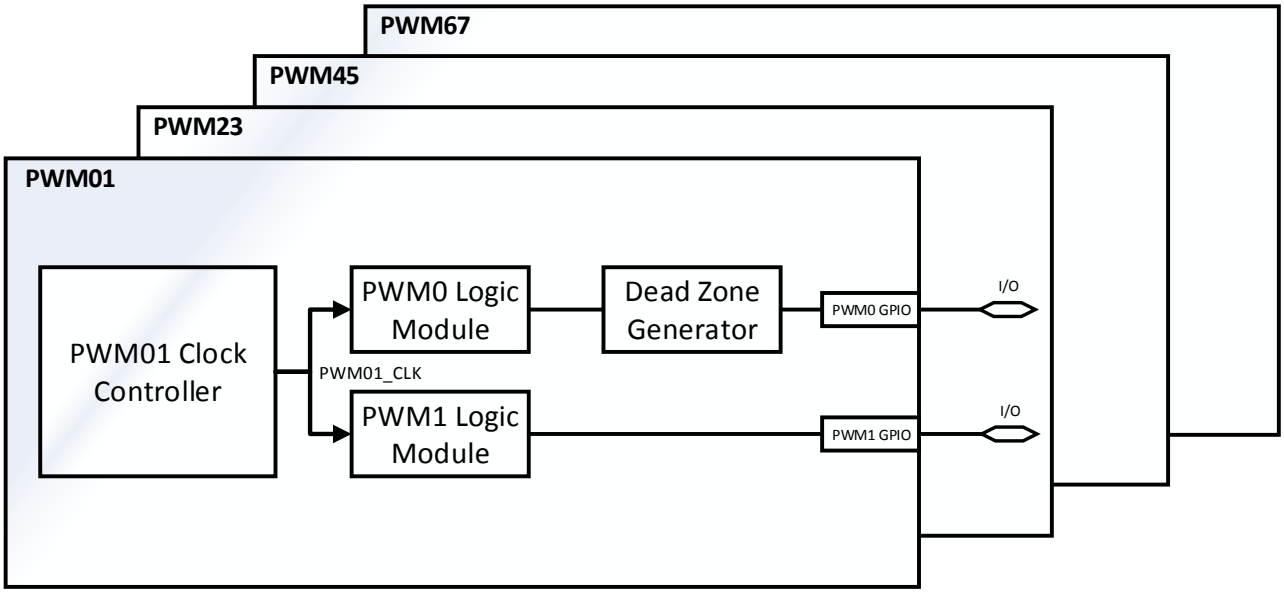

Figure 10- 46. PWM Block Diagram

Each PWM pair consists of 1 clock module, 2 timer logic module and 1 programmable dead-time generator.

10.11.3. Operations and Functional Descriptions

10.11.3.1. External Signals

Table 10-21 describes the external signals of PWM.

Table 10- 21. PWM External Signals

Signal	Description	Type
PWM0	Pulse Width Module Channel0	I/O
PWM1	Pulse Width Module Channel1	I/O
PWM2	Pulse Width Module Channel2	I/O
PWM3	Pulse Width Module Channel3	I/O
PWM4	Pulse Width Module Channel4	I/O
PWM5	Pulse Width Module Channel5	I/O
PWM6	Pulse Width Module Channel6	I/O
PWM7	Pulse Width Module Channel7	I/O

10.11.3.2. Typical Application

- Suitable for display device,such as LCD
- Suitable for electric motor control

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10.11.3.3. Clock Controller

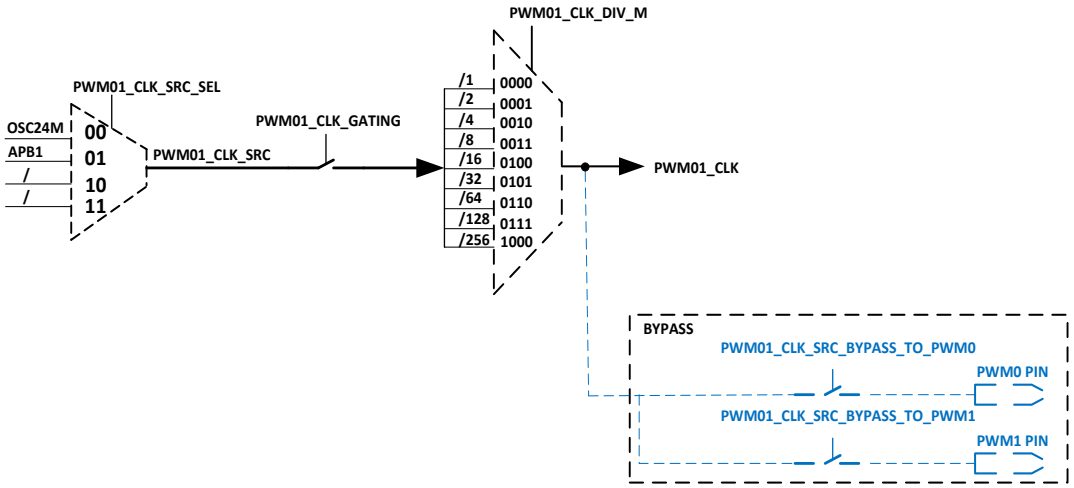

Figure 10- 47. PWM01 Clock Controller Diagram

The clock controller of each PWM pair includes clock source select(PWM01_CLK_SRC_SEL),1~256 scaler (PWM01_CLK_DIV_M), clock source bypass(CLK_SRC_BYPASS) and clock switch(PWM01_CLK_GATING).

The clock sources of PWM have OSC24M and APB1 Bus. OSC24M comes from external high frequency oscillator, APB1 is APB1 bus clock,usually is 100MHz.

The clock source bypass function is that clock source directly accesses PWM output,the PWM output waveform is the waveform of clock controller output. The BYPASS gridlines in the above figure indicates clock source bypass function,the details about implement ,please see Figure 10-48. At last the output clock of the clock controller is sent to PWM logic module.

10.11.3.4. PWM Output

Using PWM01 as an example,Figure 10-48 indicates PWM01 output logic module diagram.Other PWM pairs(PWM23, PWM45, PWM67) logic module diagrams are the same as PWM01.

PWM Timer Logic consists of one 16-bit up-counter and one 16-bit comparator. The up-counter is used to control period, and the comparator is used to control duty-cycle. The up-counter and the comparator support cache-loading, PWM output is enabled, the register value of the counter and the comparator can be changed at any time,the changed value is cached to the cache register,when the value of up-counter is equal to **PWM_ENTIRE_CYCLE**, the value of the cache register is loaded to the counter and the comparator. Cache-loading is good to avoid unstable PWM output waveform with burred feature when updating the counter value and the comparator value.

PWM supports cycle and pulse waveform output.

Cycle mode: When the value of up-counter reaches **PWM_ENTIRE_CYCLE**, the value of up-counter is loaded automatically to 0 and the up-counter continues to count, then the output waveform is a continuous waveform.

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Pulse mode: When the value of up-counter reaches **PWM_ENTIRE_CYCLE**, the value of up-counter is loaded automatically to 0 and the up-counter stops counting, then the output waveform is a pulse waveform.

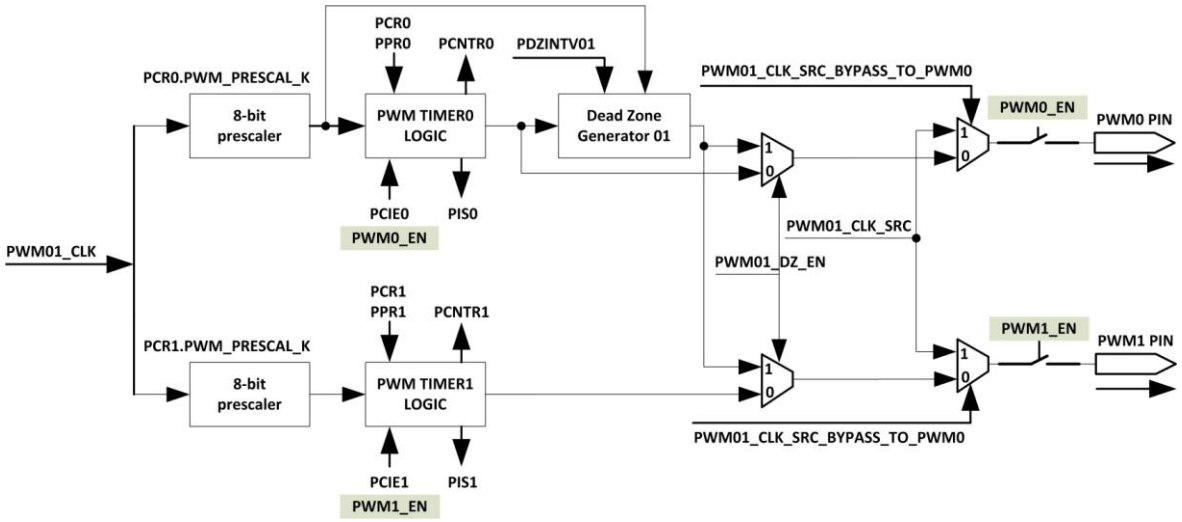

Figure 10- 48. PWM01 Output Logic Module Diagram

10.11.3.5. Up-Counter and Comparator

The period, duty-cycle and active state of PWM output waveform are decided by the up-counter and comparator. The rule of the comparator is as follows.

PCNTR >= (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “active state”
PCNTR < (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “~ (active state)”

(1) Active state of PWM0 channel is high level (PCR0. PWM_ACT_STA = 1)

When PCNTR0 >= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1(high level).
When PCNTR0 < (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0(low level).

The formula of PWM output period and duty-cycle is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE
$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE
$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE)
Duty-cycle = (high level time) / (1 period time)

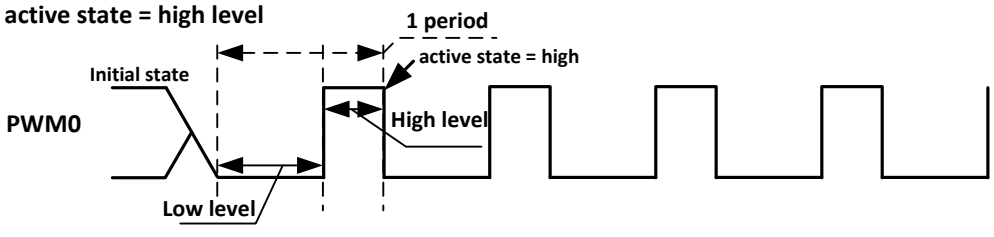

Figure 10- 49. PWM0 High Level Active State

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(2) Active state of PWM0 channel is low level (PCR0. PWM_ACT_STA = 0)

When PCNTR0 >= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0.

When PCNTR0 < (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1.

The formula of PWM output period and duty-cycle is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE)

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

Duty-cycle = (high level time) / (1 period time)

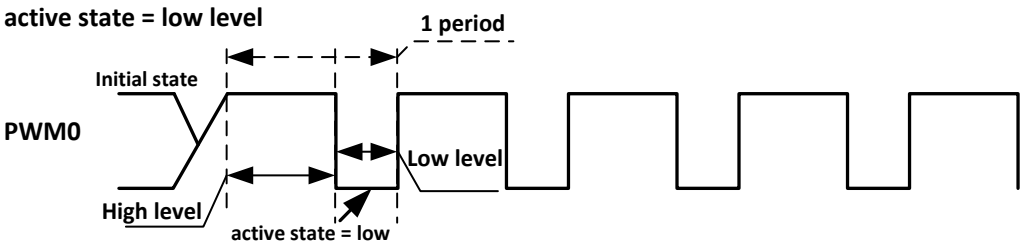

Figure 10- 50. PWM0 Low Level Active State

10.11.3.6. Pulse Mode and Cycle Mode

PWM output supports pulse mode and cycle mode. PWM in pulse mode outputs one pulse waveform, but PWM in cycle mode outputs continuous waveform.Figure 10-51 shows the PWM output waveform in pulse mode and cycle mode.

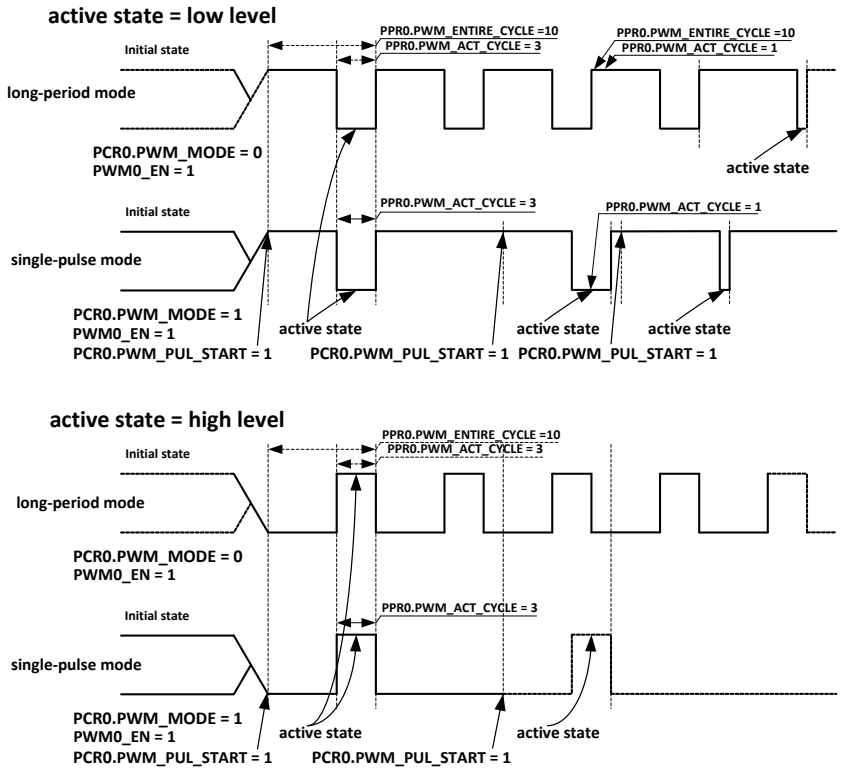

Figure 10- 51. PWM0 Output Waveform in Pulse Mode and Cycle Mode

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When PCR0.PWM_MODE is 0, PWM0 outputs cycle waveform.The calculating formula of T_{period} and $T_{active\text{-}state}$ is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE

$T_{active\ state}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

When PCR0.PWM_ACT_STA is 0, the active state of cycle waveform is low level.

When PCR0.PWM_ACT_STA is 1, the active state of cycle waveform is high level,

When PCR0.PWM_MODE is 1, PWM0 outputs pulse waveform.The calculating formula of pulse length is as follows.

Pulse length = PWM01_CLK / PWM0_PRESCALE_K * PPR0. PWM _ACT_CYCLE

When PCR0.PWM_ACT_STA is 0, the pulse level is low level, PWM0 channel outputs low pulse.

When PCR0.PWM_ACT_STA is 1, the pulse level is high level, PWM0 channel outputs high pulse.

After PWM0 channel enabled, PCR0. PWM_PUL_START need be set to 1 when PWM0 need output pulse waveform, after completed output, PCR0. PWM_PUL_START can be cleared to 0 by hardware.

The up-counter and comparator for PWM0 channel support cache loading, after PWM0 channel enabled, whether cycle mode or pulse mode, PPR0 value is modified and cached to the buffer register of PPR0 , when the up-counter value reaches PPR0. PWM_ENTIRE_CYCLE , the value in the buffer register will be loaded to up-counter and comparator, namely the value of up-counter and comparator will be overloaded in the next cycle.

Take Figure 10-51(active state =low level) as an example.

In cycle mode, the initial PPR0.PWM_ENTIRE_CYCLE value is 10, the initial PPR0. PWM _ACT_CYCLE value is 3. At some time, the value of PPR0 PPR0. PWM _ACT_CYCLE value is modified to 1, during the current cycle, the modified PPR0 values is cached to PPR0 buffer register, at the beginning of the next cycle, the value of PPR0 buffer register is loaded into up-counter and comparator, then up-counter starts to work.

In pulse mode, the initial value of PPR0. PWM _ACT_CYCLE is 3, in the generation process of a single pulse , the value of PPR0. PWM _ACT_CYCLE is modified to 1,during the current cycle, the modified PPR0 values is cached to PPR0 buffer register, when the value of up-counter reaches PPR0. PWM_ENTIRE_CYCLE, then the pulse waveform output ends,the value of PPR0 buffer register is loaded into up-counter and comparator, at the next time,after PCR0. PWM_PUL_START is set to 1, PPR0 modified value has taken effect.

NOTE

The time that loading PPR0 buffer register value into up-counter and comparator is very short, which can be ignored, and does not affect the PWM output.

10.11.3.7. Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time.Figure 10-52 shows the complementary pair output of PWM01.

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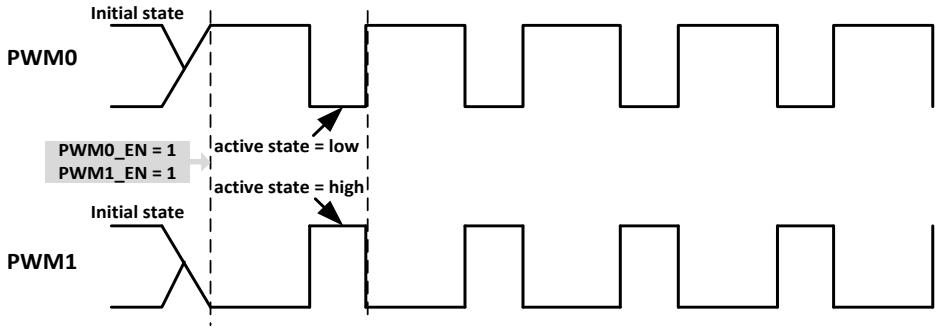

Figure 10- 52. PWM01 Complementary Pair Output

The complementary pair output need satisfy the following three conditions:

- The same frequency,the same duty-cycle
- Opposite active state
- Enable two channels of PWM pair at the same time

10.11.3.8. Dead-time Generator

Every PWM pair has a programmable dead-time generator.When the dead-time function of PWM pair enabled,PWM01 output waveform is desided by PWM timer logic and DeadZone Generator.Figure 10-53 shows the output waveform.

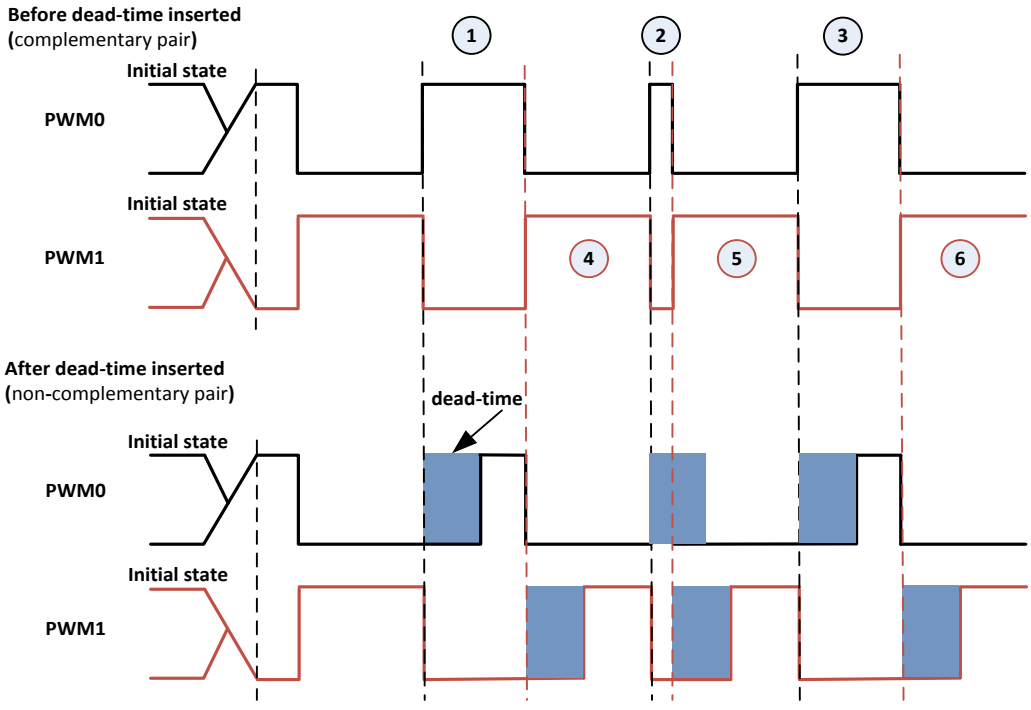

Figure 10- 53. Dead-time Output Waveform

Before dead-time inserted: a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.

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After dead-time inserted: a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01.The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.

For complementary pair of Dead Zone Generator 01 ,the principle of inserting dead-time is that to inserte dead-time as soon as the rising edge came. If high level time for mark② in the above figure is less than dead-time,then dead-time will override the high level.The setting of dead-time need consider the period and duty-cycle of output waveform.Dead-time formula is defined as follows:

Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PDZINTV01

10.11.3.9. Capture Input

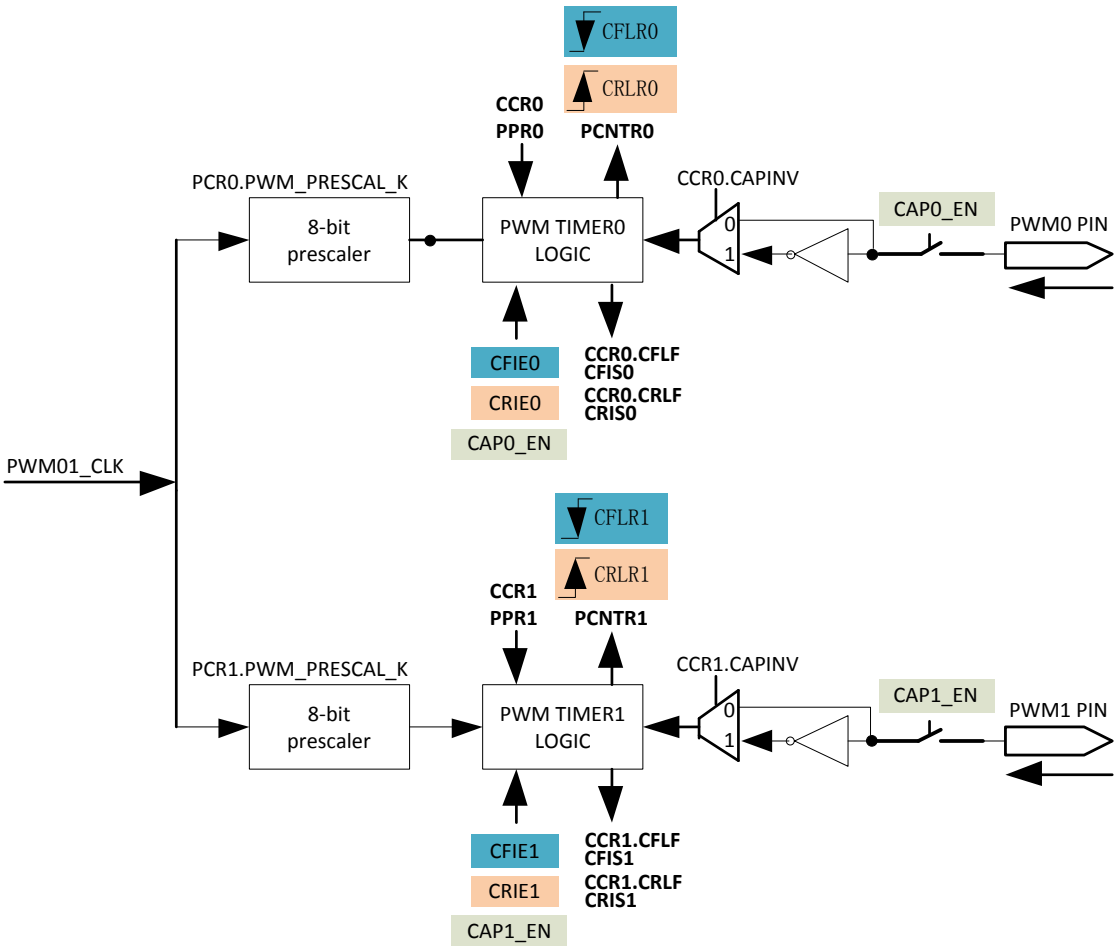

Figure 10- 54. PWM01 Capture Logic Module Diagram

Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture rising edge and falling edge of the external clock.Using PWM0 channel as an example,PWM0 channel has one **CFLR** and one **CRLR** for capturing up-counter value in falling edge, in rising edge,respectively.You can calculate the period of external clock by **CFLR** and **CRLR**.

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

$T_{period} = T_{high\text{-}level} + T_{low\text{-}level}$

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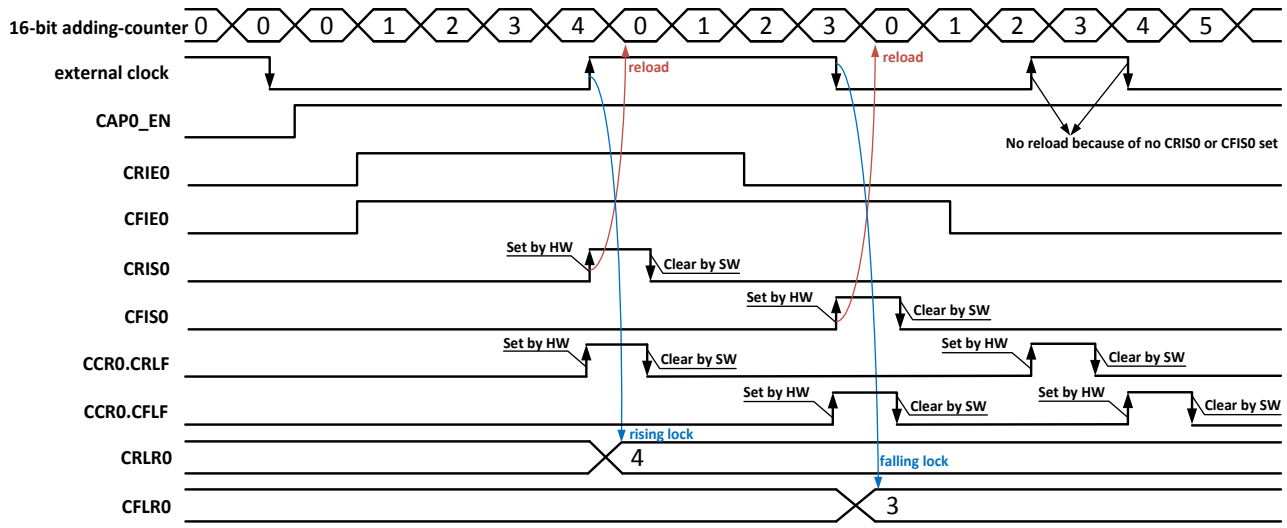

Figure 10- 55. PWM0 Channel Capture Timing

When the capture input function of PWM channel is enabled, the up-counter of PWM0 channel starts to work.

When the timer logic module of PWM0 captures one rising edge,the current value of up-counter is locked to **CRLR**, and **CRLF** is set to 1 . If **CRIE0** is 1, then **CRIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CRIE0** is 0, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of up-counter is locked to **CFLR**, and **CFLF** is set to 1 . If **CFIE0** is 1, then **CFIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CFIE0** is 0, the up-counter is not loaded to 0.

10.11.3.10. Interrupt

PWM supports interrupt generation when PWM channel is configured to PWM output or capture input .

For PWM output function, whether pulse mode or cycle mode, if the value of the up-counter reaches **PWM_ENTIRE_CYCLE**, the timer logic module will automatically set the PIS(PWM Interrupt Status) bit to 1 by hardware. But the PIS bit is cleared by software.

For capture input function, when the timer logic module of the capture channel0 captures rising edge, and **CRIE0** is 1, then **CRIS0** is set to 1; when the timer logic module of the capture channel0 captures falling edge, and **CFIE0** is 1, then **CFIS0** is set to 1.

10.11.4. Register List

Module Name	Base Address
PWM	0x0300A000

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Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register
PCCR23	0x0024	PWM23 Clock Configuration Register
PCCR45	0x0028	PWM45 Clock Configuration Register
PCCR67	0x002C	PWM67 Clock Configuration Register
PDZCR01	0x0030	PWM01 Dead Zone Control Register
PDZCR23	0x0034	PWM23 Dead Zone Control Register
PDZCR45	0x0038	PWM45 Dead Zone Control Register
PDZCR67	0x003C	PWM67 Dead Zone Control Register
PER	0x0040	PWM Enable Register
CER	0x0044	Capture Enable Register
PCR	0x0060+0x00+N*0x20(N=0~7)	PWM Control Register
PPR	0x0060+0x04+N*0x20(N=0~7)	PWM Period Register
PCNTR	0x0060+0x08+N*0x20(N=0~7)	PWM Count Register
CCR	0x0060+0x0C+N*0x20(N=0~7)	Capture Control Register
CRLR	0x0060+0x10+N*0x20(N=0~7)	Capture Rise Lock Register
CFLR	0x0060+0x14+N*0x20(N=0~7)	Capture Fall Lock Register

10.11.5. Register Description

10.11.5.1. PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PWM_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PCIE7 PWM Channel 7 Interrupt Enable 0: PWM channel 7 interrupt disable 1: PWM channel 7 interrupt enable
6	R/W	0x0	PCIE6 PWM Channel 6 Interrupt Enable 0: PWM channel 6 interrupt disable 1: PWM channel 6 interrupt enable
5	R/W	0x0	PCIE5 PWM Channel 5 Interrupt Enable 0: PWM channel 5 interrupt disable 1: PWM channel 5 interrupt enable
4	R/W	0x0	PCIE4 PWM Channel 4 Interrupt Enable

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			0: PWM channel 4 interrupt disable 1: PWM channel 4 interrupt enable
3	R/W	0x0	PCIE3 PWM Channel 3 Interrupt Enable 0: PWM channel 3 interrupt disable 1: PWM channel 3 interrupt enable
2	R/W	0x0	PCIE2 PWM Channel 2 Interrupt Enable 0: PWM channel 2 interrupt disable 1: PWM channel 2 interrupt enable
1	R/W	0x0	PCIE1 PWM Channel 1 Interrupt Enable 0: PWM channel 1 interrupt disable 1: PWM channel 1 interrupt enable
0	R/W	0x0	PCIE0 PWM Channel 0 Interrupt Enable 0: PWM channel 0 interrupt disable 1: PWM channel 0 interrupt enable

10.11.5.2. PWM IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: PWM_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	PIS7 PWM Channel 7 Interrupt Status When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. Reads 1: PWM channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6 PWM Channel 6 Interrupt Status When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. Reads 1: PWM channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5 PWM Channel 5 Interrupt Status When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit.

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			Reads 0: PWM channel 5 interrupt is not pending. Reads 1: PWM channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4 PWM Channel 4 Interrupt Status When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. Reads 1: PWM channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3 PWM Channel 3 Interrupt Status When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. Reads 1: PWM channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2 PWM Channel 2 Interrupt Status When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. Reads 1: PWM channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1 PWM Channel 1 Interrupt Status When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. Reads 1: PWM channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0 PWM Channel 0 Interrupt Status When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. Reads 1: PWM channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 0 interrupt status.

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10.11.5.3. PWM Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: PWM_CAPTURE_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	CFIE7 If the bit is set 1, when capturing channel 7 captures falling edge, it generates a capturing channel 7 pending. 0: Capturing channel 7 fall lock interrupt disable 1: Capturing channel 7 fall lock interrupt enable
14	R/W	0x0	CRIE7 If the bit is set 1, when capturing channel 7 captures rising edge, it generates a capturing channel 7 pending. 0: Capturing channel 7 rise lock interrupt disable 1: Capturing channel 7 rise lock interrupt enable
13	R/W	0x0	CFIE6 If the bit is set 1, when capturing channel 6 captures falling edge, it generates a capturing channel 6 pending. 0: Capturing channel 6 fall lock interrupt disable 1: Capturing channel 6 fall lock interrupt enable
12	R/W	0x0	CRIE6 If the bit is set 1, when capturing channel 6 captures rising edge, it generates a capturing channel 6 pending. 0: Capturing channel 6 rise lock interrupt disable 1: Capturing channel 6 rise lock interrupt enable
11	R/W	0x0	CFIE5 If the bit is set 1, when capturing channel 5 captures falling edge, it generates a capturing channel 5 pending. 0: Capturing channel 5 fall lock interrupt disable 1: Capturing channel 5 fall lock interrupt enable
10	R/W	0x0	CRIE5 If the bit is set 1, when capturing channel 5 captures rising edge, it generates a capturing channel 5 pending. 0: Capturing channel 5 rise lock interrupt disable 1: Capturing channel 5 rise lock interrupt enable
9	R/W	0x0	CFIE4 If the bit is set 1, when capturing channel 4 captures falling edge, it generates a capturing channel 4 pending. 0: Capture channel 4 fall lock interrupt disable 1: Capture channel 4 fall lock interrupt enable
8	R/W	0x0	CRIE4 If the bit is set 1, when capturing channel 4 captures rising edge, it generates a capturing channel 4 pending. 0: Capturing channel 4 rise lock interrupt disable 1: Capturing channel 4 rise lock interrupt enable

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7	R/W	0x0	CFIE3 If the bit is set 1, when capturing channel 3 captures falling edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 fall lock interrupt disable 1: Capturing channel 3 fall lock interrupt enable
6	R/W	0x0	CRIE3 If the bit is set 1, when capturing channel 3 captures rising edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 rise lock interrupt disable 1: Capturing channel 3 rise lock interrupt enable
5	R/W	0x0	CFIE2 If the bit is set 1, when capturing channel 2 captures falling edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 fall lock interrupt disable 1: Capturing channel 2 fall lock interrupt enable
4	R/W	0x0	CRIE2 If the bit is set 1, when capturing channel 2 captures rising edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 rise lock interrupt disable 1: Capturing channel 2 rise lock interrupt enable
3	R/W	0x0	CFIE1 If the bit is set 1, when capturing channel 1 captures falling edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 fall lock interrupt disable 1: Capturing channel 1 fall lock interrupt enable
2	R/W	0x0	CRIE1 If the bit is set 1, when capturing channel 1 captures rising edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 rise lock interrupt disable 1: Capturing channel 1 rise lock interrupt enable
1	R/W	0x0	CFIE0 If the bit is set 1, when capturing channel 0 captures falling edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 fall lock interrupt disable 1: Capturing channel 0 fall lock interrupt enable
0	R/W	0x0	CRIE0 If the bit is set 1, when capturing channel 0 captures rising edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 rise lock interrupt disable 1: Capturing channel 0 rise lock interrupt enable

10.11.5.4. PWM Capture IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0014	Register Name: PWM_CAPTURE_IRQ_STATUS_REG

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Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W1C	0x0	CFIS7 Capturing channel 7 falling lock interrupt status. When capturing channel 7 captures falling edge, if capturing channel 7 fall lock interrupt (**CFIE7**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 7 interrupt is not pending. Reads 1: Capturing channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capturing channel 7 rising lock interrupt status. When capturing channel 7 captures rising edge, if capturing channel 7 rise lock interrupt (**CRIE7**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capturing channel 7 interrupt is not pending. Reads 1: Capturing channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6 Capturing channel 6 falling lock interrupt status. When capturing channel 6 captures falling edge, if capturing channel 6 fall lock interrupt (**CFIE6**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 6 interrupt is not pending. Reads 1: Capturing channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 6 interrupt status.
12	R/W1C	0x0	CRIS6 Capturing channel 6 rising lock interrupt status. When capturing channel 6 captures rising edge, if capturing channel 6 rise lock interrupt (**CRIE6**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 6 interrupt is not pending. Reads 1: Capturing channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capturing channel 5 falling lock interrupt status. When capturing channel 5 captures falling edge, if capturing channel 5 fall lock interrupt (**CFIE5**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 5 interrupt is not pending. Reads 1: Capturing channel 5 interrupt is pending.

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			Writes 0: No effect. Reads 1: Clear capturing channel 5 interrupt status.
10	R/W1C	0x0	CRIS5 Capturing channel 5 rising lock interrupt status. When capturing channel 5 captures rising edge, if capturing channel 5 rise lock interrupt (**CRIE5**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 5 interrupt is not pending. Reads 1: Capturing channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 5 interrupt status.
9	R/W1C	0x0	CFIS4 Capturing channel 4 falling lock interrupt status. When capturing channel 4 captures falling edge, if capturing channel 4 fall lock interrupt (**CFIE4**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 4 interrupt is not pending. Reads 1: Capturing channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 4 interrupt status.
8	R/W1C	0x0	CRIS4 Capturing channel 4 rising lock interrupt status. When capturing channel 4 captures rising edge, if capturing channel 4 rise lock interrupt (**CRIE4**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 4 interrupt is not pending. Reads 1: Capturing channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (**CFIE3**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (**CRIE3**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending.

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			Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (**CFIE2**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (**CRIE2**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (**CFIE1**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (**CRIE1**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (**CFIE0**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending.

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			Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (**CRIE0**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.

10.11.5.5. PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: PWM01_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM01_CLK_SRC Select PWM01 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM1 Bypass PWM01 Clock Source to PWM1 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM0 Bypass PWM01 Clock Source to PWM0 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM01_CLK_GATING Gating Clock for PWM01 0: Mask 1: Pass
3:0	R/W	0x0	PWM01_CLK_DIV_M PWM01 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128

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			1000: /256 others: Reserved

10.11.5.6. PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0024			Register Name: PWM23_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM23_CLK_SRC_SEL Select PWM23 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM3 Bypass PWM23 Clock Source to PWM3 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM2 Bypass PWM23 Clock Source to PWM2 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM23_CLK_GATING Gating Clock for PWM23 0: Mask 1: Pass
3:0	R/W	0x0	PWM23_CLK_DIV_M PWM23 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

10.11.5.7. PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: PWM45_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/

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8:7	R/W	0x0	PWM45_CLK_SRC_SEL Select PWM45 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM5 Bypass PWM45 Clock Source to PWM5 Output 0: Not bypass 1: Bypass
5	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM4 Bypass PWM45 Clock Source to PWM4 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM45_CLK_GATING Gating Clock for PWM45 0: Mask 1: Pass
3:0	R/W	0x0	PWM45_CLK_DIV_M PWM45 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

10.11.5.8. PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: PWM67_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM67_CLK_SRC_SEL Select PWM67 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM7 Bypass PWM67 Clock Source to PWM7 Output 0: Not bypass 1: Bypass

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5	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM6 Bypass PWM67 Clock Source to PWM6 Output 0: Not bypass 1: Bypass
4	R/W	0x0	PWM67_CLK_GATING Gating Clock for PWM67 0: Mask 1: Pass
3:0	R/W	0x0	PWM67_CLK_DIV_M PWM67 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

10.11.5.9. PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: PWM01_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM01_DZ_INTV PWM01 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

10.11.5.10. PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0034			Register Name: PWM23_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN

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			PWM23 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

10.11.5.11. PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0038			Register Name: PWM45_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	PWM45_DZ_INTV PWM45 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN PWM45 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

10.11.5.12. PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x003C			Register Name: PWM67_CLOCK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x0	PWM67_DZ_INTV PWM67 Dead Zone Interval Value
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN PWM67 Dead Zone Enable 0: Dead Zone disable 1: Dead Zone enable

10.11.5.13. PWM Enable Register (Default Value: 0x0000_0000)

Offset:0x0040			Register Name: PWM_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PWM7_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel7 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
6	R/W	0x0	PWM6_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel6 is permitted to output PWM waveform.

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			0: PWM disable 1: PWM enable
5	R/W	0x0	PWM5_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel5 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
4	R/W	0x0	PWM4_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel4 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
3	R/W	0x0	PWM3_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel3 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
2	R/W	0x0	PWM2_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel2 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
1	R/W	0x0	PWM1_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel1 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable
0	R/W	0x0	PWM0_EN When PWM is enabled,the 16-bit up-counter starts working and PWM channel0 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable

10.11.5.14. PWM Capture Enable Register (Default Value: 0x0000_0000)

Offset:0x0044			**Register Name: PWM_CAPTURE_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	CAP7_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

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6	R/W	0x0	CAP6_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
5	R/W	0x0	CAP5_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
4	R/W	0x0	CAP4_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
3	R/W	0x0	CAP3_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
2	R/W	0x0	CAP2_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
1	R/W	0x0	CAP1_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
0	R/W	0x0	CAP0_EN When capture function is enabled,the 16-bit up-counter starts working and capture channel0 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

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10.11.5.15. PWM Control Register (Default Value: 0x0000_0000)

Offset:0x0060+0x0+N*0x20(N=0~7)			Register Name: PWM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM Period Register Ready 0: PWM period register is ready to write 1: PWM period register is busy
10	R/W1S	0x0	PWM_PUL_START PWM Pulse Output Start 0: No effect 1: Output 1 pulse After finishing configuration for outputting pulse, set this bit once and then PWM would output one pulse. After the pulse is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM Output Mode Select 0: Cycle mode 1: Pulse mode
8	R/W	0x0	PWM_ACT_STA PWM Active State 0: Low Level 1: High Level
7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256

10.11.5.16. PWM Period Register

Offset:0x0060+0x04+N*0x20(N=0~7)			Register Name: PWM_PRD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock. 0: 1 cycle 1: 2 cycles … N: N+1 cycles If the register need to be modified dynamically, the PCLK should be faster

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			than the PWM CLK.
15:0	R/W	UDF	PWM_ACT_CYCLE Number of the active cycles in the PWM clock. 0: 0 cycle 1: 1 cycle … N: N cycles

10.11.5.17. PWM Counter Register

Offset:0x0060+0x08+N*0x20(N=0~7)			Register Name: PWM_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	UDF	PWM output or capture input. The field indicates the current value of the PWM 16-bit up-counter.

10.11.5.18. PWM Capture Control Register (Default Value: 0x0000_0000)

Offset:0x0060+0x0C+N*0x20(N=0~7)			Register Name: PWM_CAPTURE_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	CRLF When capturing channel captures the rising edge,the current value of the 16-bit up-counter is latched to **CRLR** and the bit is set to 1 by hardware.Writing 1 to clear the bit.
1	R/W1C	0x0	CFLF When capturing channel captures the falling edge,the current value of the 16-bit up-counter is latched to **CFLR** and the bit is set to 1 by hardware.Writing 1 to clear the bit.
0	R/W	0x0	CAPINV Inversing the input signal from the capturing channel before the 16-bit counter of the capturing channel. 0: Not inverse 1: Inverse

10.11.5.19. PWM Capture Rise Lock Register

Offset:0x0060+0x10+N*0x20(N=0~7)			Register Name: PWM_CAPTURE_RISE_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	UDF	CRLR

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			When the capturing channel captures the rising edge,the current value of the 16-bit up-counter is latched to the register.

10.11.5.20. PWM Capture Fall Lock Register

Offset:0x0060+0x14+N*0x20(N=0~7)			Register Name: PWM_CAPTURE_FALL_LOCK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	UDF	CFLR When the capturing channel captures the falling edge,the current value of the 16-bit up-counter is latched to the register.

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10.12. TSC

10.12.1. Overview

The transport stream controller(TSC) is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1.

The transport stream controller receives multimedia data stream from SSI(Synchronous Serial Port)/SPI(Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before the Packet to be store to memory by DMA, it can be pre-processed by the Transport Stream Descrambler.

The transport stream controller can be used for almost all multi-media application cases, for example: DVB Set top Box, IPTV, Streaming-media Box, multi-media players and so on.

Features:

- Supports SPI/SSI interface,interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Supports multiple transport stream packet (188, 192, 204) format
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

10.12.2. Block Diagram

Figure 10-56 shows a block diagram of the TSC.

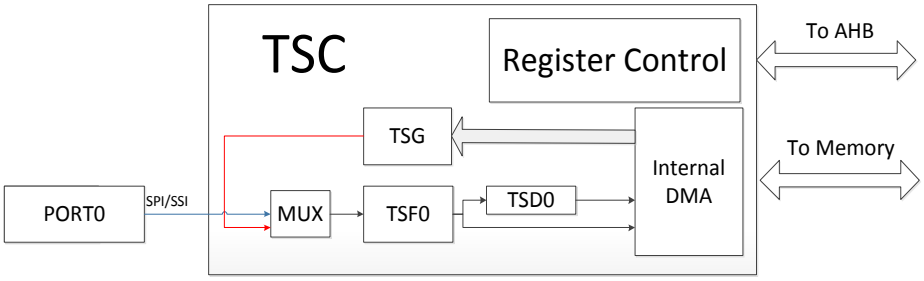

Figure 10- 56. TSC Block Diagram

TSC – TS Controller; TSF – TS Filter; TSD – TS Descrambler; TSG – TS Generator

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10.12.3. Operations and Functional Descriptions

10.12.3.1. External Signals

Table 10-22 describes the external signals of TSC.

Table 10- 22. TSC External Signals

Signal	Description	Type
TS_CLK	Clock of SPI/SSI data input	I
TS_ERR	Error indicate	I
TS_SYNC	Packet sync (or Start flag) for TS packet	I
TS_DVLD	Data valid flag for TS data input	I
TS_D[7:0]	TS data input Data[7:0] are used in SPI mode; Only Data[0] is used in SSI mode.	I

10.12.3.2. Clock Sources

The following table describes the clock sources of TSC.

Table 10- 23. TSC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock,default value is 600MHz

10.12.3.3. Timing Diagram

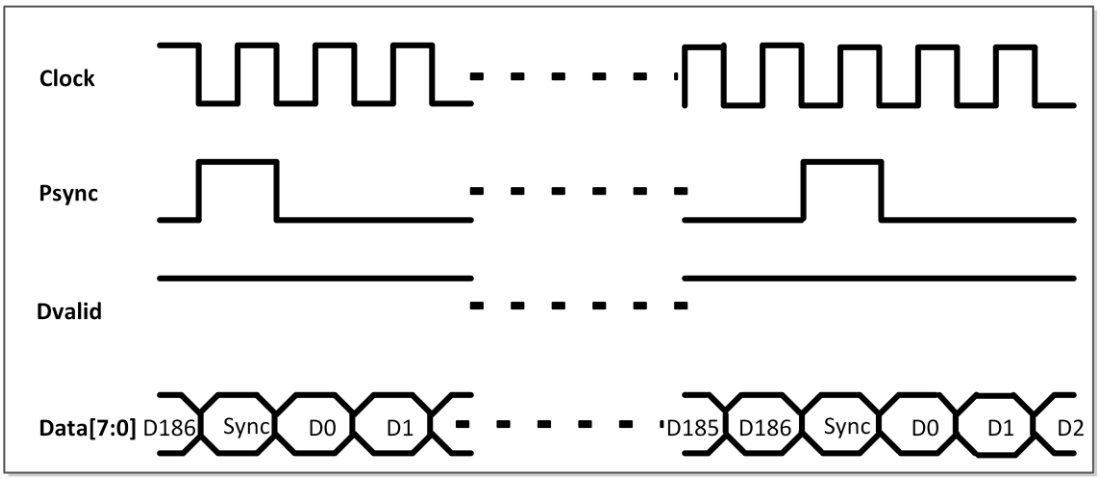

Figure 10- 57. Input Timing for SPI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

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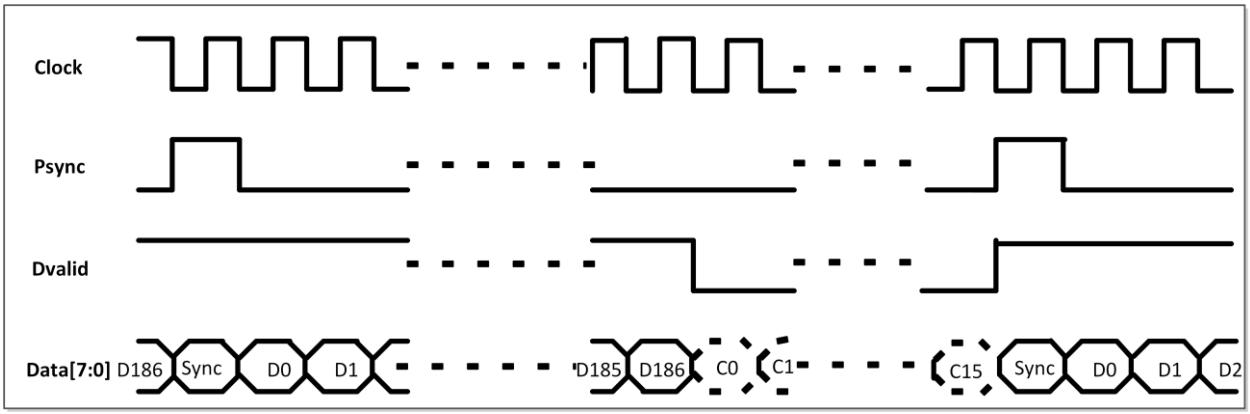

Figure 10- 58. Alternative Input Timing for SPI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

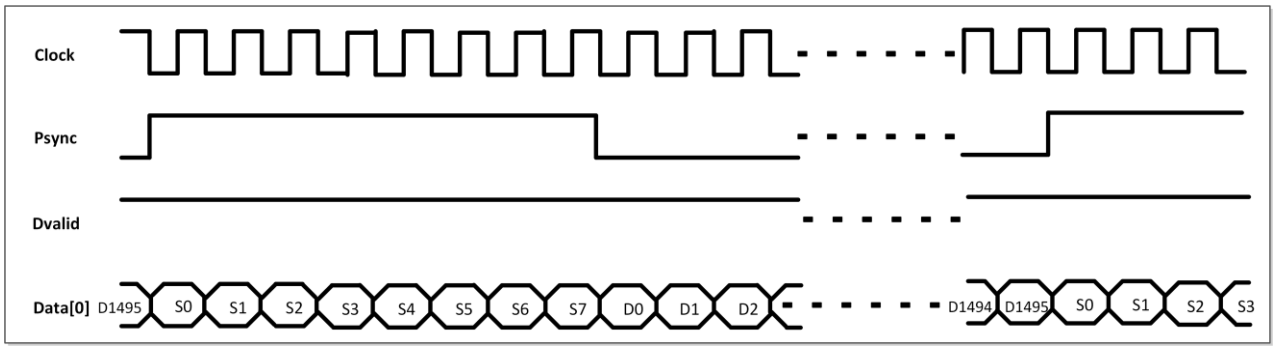

Figure 10- 59. Alternative Input Timing for SSI Mode

(CLOCK = Rising Edge, PSYNC = High Active, DVALID = High Active, Packet Size = 188 Bytes)

10.12.4. Programming Guidelines

10.12.4.1. Initialization

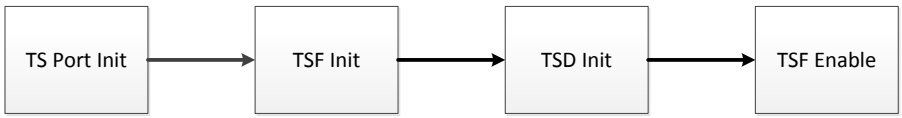

Figure 10- 60. TSC Initialization

The PID,DMA ADDR,DMA SIZE,Write Pointer,Read Pointer Register for TSF must clear to 0 first after power-up.

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10.12.4.2. PID Changing

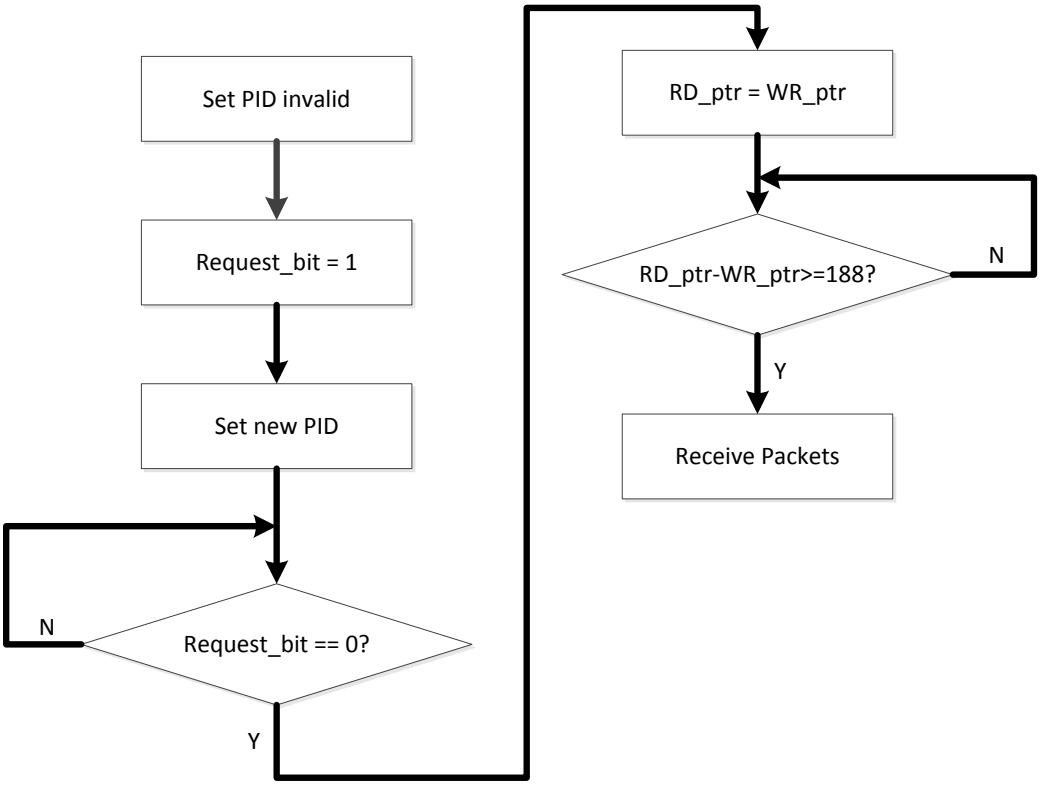

Figure 10- 61. PID Changing

Request_bit is the bit8 of the TSF Control and Status Register.

10.12.5. Register List

Module Name	Base Address
TSC	0x05060000
TSG	0x05060040
TSF	0x05060100
TSD	0x05060180

Register Name	Offset	Description
TSC		
TSC_PCTLR	TSC + 0x10	TSC Port Control Register
TSC_PPARR	TSC + 0x14	TSC Port Parameter Register
TSC_TSFMUXR	TSC + 0x20	TSC TSF Input Multiplex Control Register
TSC_IRQ_STATUS	TSC + 0x30	TSC Interrupt Status Register
TSG		
TSG_CTLR	TSG + 0x00	TSG Control Register
TSG_PPR	TSG + 0x04	TSG Packet Parameter Register

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TSG_STAR	TSG + 0x08	TSG Status Register
TSG_CCR	TSG + 0x0C	TSG Clock Control Register
TSG_BBAR	TSG + 0x10	TSG Buffer Base Address Register
TSG_BSZR	TSG + 0x14	TSG Buffer Size Register
TSG_BPR	TSG + 0x18	TSG Buffer Pointer Register
TSF		
TSF_CTLR	TSF + 0x00	TSF Control Register
TSF_PPR	TSF + 0x04	TSF Packet Parameter Register
TSF_STAR	TSF + 0x08	TSF Status Register
TSF_DIER	TSF + 0x10	TSF DMA Interrupt Enable Register
TSF_OIER	TSF + 0x14	TSF Overlap Interrupt Enable Register
TSF_DISR	TSF + 0x18	TSF DMA Interrupt Status Register
TSF_OISR	TSF + 0x1C	TSF Overlap Interrupt Status Register
TSF_PCRCR	TSF + 0x20	TSF PCR Control Register
TSF_PCRDR	TSF + 0x24	TSF PCR Data Register
TSF_CENR	TSF + 0x30	TSF Channel Enable Register
TSF_CPER	TSF + 0x34	TSF Channel PES Enable Register
TSF_CDER	TSF + 0x38	TSF Channel Descramble Enable Register
TSF_CINDR	TSF + 0x3C	TSF Channel Index Register
TSF_CCTLR	TSF + 0x40	TSF Channel Control Register
TSF_CSTAR	TSF + 0x44	TSF Channel Status Register
TSF_CCWIR	TSF + 0x48	TSF Channel CW Index Register
TSF_CPIDR	TSF + 0x4C	TSF Channel PID Register
TSF_CBBAR	TSF + 0x50	TSF Channel Buffer Base Address Register
TSF_CBSZR	TSF + 0x54	TSF Channel Buffer Size Register
TSF_CBWPR	TSF + 0x58	TSF Channel Buffer Write Pointer Register
TSF_CBRPR	TSF + 0x5C	TSF Channel Buffer Read Pointer Register
TSD		
TSD_CTLR	TSD + 0x00	TSD Control Register
TSD_CWIR	TSD + 0x1C	TSD Control Word Index Register
TSD_CWR	TSD + 0x20	TSD Control Word Register

10.12.6. Register Description

10.12.6.1. TSC Port Control Register(Default Value: 0x0000_0000)

Offset: 0x10			**Register Name: TSC_PCTLR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TSInPort0Ctrl TS Input Port0 Control 0 : SPI 1 : SSI

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10.12.6.2. TSC Port Parameter Register(Default Value: 0x0000_0000)

Offset: 0x14			Register Name:TSC_PPARR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	TS Input Port0 SSI Data Order 0: MSB first for one byte data 1: LSB first for one byte data
3	R/W	0x0	TS Input Port0 CLOCK Signal Polarity 0: Rise edge capturing 1: Fall edge capturing
2	R/W	0x0	TS Input Port0 ERROR Signal Polarity 0: High level active 1: Low level active
1	R/W	0x0	TS Input Port0 DVALID Signal Polarity 0: High level active 1: Low level active
0	R/W	0x0	TS Input Port0 PSYNC Signal Polarity 0: High level active 1: Low level active

10.12.6.3. TSC TSF Input Multiplex Control Register(Default Value: 0x0000_0000)

Offset: 0x20			Register Name: TSC_TSFMUXR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	TSF0InputMuxCtrl TSF0 Input Multiplex Control 0000 : Data from TSG 0001 : Data from TS IN Port0 Others : Reserved

10.12.6.4. TSC Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x30			Register Name:TSC_INT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x0	TSG Interrupt Global Status When all TSG interrupt status bits are cleared ,this bit will be cleared by hardware.

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15:1	/	/	/
0	R	0x0	TSF0 Interrupt Global Status When all TSF0 interrupt status bits are cleared ,this bit will be cleared by hardware.

10.12.6.5. TSG Control and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x00			Register Name: TSG_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	TSGSts Status for TS Generator 00: IDLE state 01: Running state 10: PAUSE state Others: Reserved
23:10	/	/	/
9	R/W	0x0	TSGLBufMode Loop Buffer Mode When set to '1', the TSG external buffer is in loop mode.
8	R/W	0x0	TSGSyncByteChkEn Sync Byte Check Enable Enable/Disable check SYNC byte for receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is receiver, TS Generator would come into PAUSE state. If the correspond interrupt is enabled, the interrupt would happen.
7:3	/	/	/
2	R/W	0x0	TSGPauseBit Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finished this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0x0	TSGStopBit Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finished this operation, this bit will clear to zero by hardware.
0	R/W	0x0	TSGStartBit Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

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10.12.6.6. TSG Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSG+0x04			Register Name: TSG_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0x0	SyncBytePos Sync Byte Position 0: The 1st byte position 1: The 5th byte position This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PktSize Packet Size Byte Size for one TS packet 0: 188 bytes Others: Reserved

10.12.6.7. TSG Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x08			Register Name: TSG_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSGEndIE TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0x0	TSGFFIE TS Generator (TSG) Full Finish Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSGHFIE TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	TSGErrSyncByteIE

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			TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W1C	0x0	TSGEndSts TS Generator (TSG) End Status Write '1' to clear.
2	R/W1C	0x0	TSGFFSts TS Generator (TSG) Full Finish Status Write '1' to clear.
1	R/W1C	0x0	TSGHFSts TS Generator (TSG) Half Finish Status Write '1' to clear.
0	R/W1C	0x0	TSGErrSyncByteSts TS Generator (TSG) Error Sync Byte Status Write '1' to clear.

10.12.6.8. TSG Clock Control Register(Default Value: 0x0000_0000)

Offset: TSG+0x0C			Register Name: TSG_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	TSGCDF_N TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSGCDF_D TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(8*(D+1)). Fi is the input special clock of TSC, and D must not less than N.

10.12.6.9. TSG Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSG+0x10			Register Name: TSG_BBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RW	0x0	TSGBufBase Buffer Base Address This value is a start address of TSG buffer. **NOTE** **This value should be 4-word (16Bytes) align, and the lowest 4-bit of this value should be zero.**

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10.12.6.10. TSG Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSG+0x14			Register Name:TSG_BSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	TSGBufSize Data Buffer Size for TS Generator It is in byte unit. The size should be 4-word (16Bytes) align, and the lowest 4 bits should be zero.

10.12.6.11. TSG Buffer Pointer Register(Default Value: 0x0000_0000)

Offset: TSG+0x18			Register Name: TSG_BPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	TSGBufPtr Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

10.12.6.12. TSF Control and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x00			Register Name: TSF_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/WAC	0x0	Channel Change PID Request This bit is used to send a request to hardware for changing the PID of the channel.It will be cleared by hardware when the channel changing finish. Writing '0' has no effect.
7:3	/	/	/
2	R/W	0x0	TSF Enable 00: Disable TSF Input 01: Enable TSF Input
1	/	/	/
0	R/WAC	0x0	TSFGSRF TSF Global Soft Reset Writing '1' by software will reset all status and state machine of TSF. And it is cleared by hardware after finish reset. Writing '0' by software has no effect.

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10.12.6.13. TSF Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSF+0x04			Register Name: TSF_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LostSyncThd Lost Sync Packet Threshold It is used for packet sync lost by checking the value of sync byte.
27:24	R/W	0x0	SyncThd Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	SyncByteVal Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0x0	SyncMthd Packet Sync Method 00: By PSYNC signal 01: By sync byte 10: By both PSYNC and Sync Byte 11: Reserved
7	R/W	0x0	SyncBytePos Sync Byte Position 0: the 1st byte position 1: the 5th byte position This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PktSize Packet Size Byte size for one TS packet 00: 188 bytes 01: 192 bytes 10: 204 bytes 11: Reserved

10.12.6.14. TSF Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x08			Register Name: TSF_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSFFOIE TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable

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18	R/W	0x0	TSFPPDIE TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSFCOIE TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable 1: Enable
16	R/W	0x0	TSFCDIE TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W1C	0x0	TSFFOIS TS PID Filter (TSF) Internal FIFO Overrun Status Write '1' to clear.
2	R/W1C	0x0	TSFPPDIS TS PCR Packet Found Status When it is '1', one TS PCR Packet is found. Write '1' to clear.
1	R	0x0	TSFCOIS TS PID Filter (TSF) Channel Overlap Status It is global status for 32 channel. It would clear to zero after all channels status bits are cleared.
0	R	0x0	TSFCDIS TS PID Filter (TSF) Channel DMA Status It is global status for 32 channel. It would clear to zero after all channels status bits are cleared.

10.12.6.15. TSF DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x10			Register Name: TSF_DIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMAIE DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

10.12.6.16. TSF Overlap Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x14			Register Name: TSF_OIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	OLPIE Overlap Interrupt Enable

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			Overlap interrupt enable bits for channel 0~31.

10.12.6.17. TSF DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x18			Register Name: TSF_DISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W1C	0x0	DMAIS DMA Interrupt Status DMA interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding DMA Interrupt Enable bits set, the TSF interrupt will generate.

10.12.6.18. TSF Overlap Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x1C			Register Name: TSF_OISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W1C	0x0	OLPIS Overlap Interrupt Status Overlap interrupt Status bits for channel 0~31. Set by hardware, and can be cleared by software writing '1'. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

10.12.6.19. TSF PCR Control Register(Default Value: 0x0000_0000)

Offset: TSF+0x20			Register Name: TSF_PCRCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PCRDE PCR Detecting Enable 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0x0	PCRCIND Channel Index m for Detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0x0	PCRLSB PCR Contest LSB 1 bit--PCR[0].

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10.12.6.20. TSF PCR Data Register(Default Value: 0x0000_0000)

Offset: TSF+0x24			Register Name: TSF_PCRDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PCRMSB PCR Data High 32 bits--PCR[33:1].

10.12.6.21. TSF Channel Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x30			Register Name: TSF_CENR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FILTEREN Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, internal status of the corresponding filter channel will be reset.

10.12.6.22. TSF Channel PES Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x34			Register Name: TSF_CPER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PESEN PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

10.12.6.23. TSF Channel Descramble Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x38			Register Name: TSF_CDER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DESCEN Descramble Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

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10.12.6.24. TSF Channel Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x3C			Register Name: TSF_CINDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0x0	CHIND Channel Index This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is 0x40~0x7f.

10.12.6.25. TSF Channel CW Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x48			Register Name: TSF_CCWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	CWIND Related Control Word Index Index to the control word used by this channel when Descramble Enable of this channel enable. This value is useless when the corresponding Descramble Enable is '0'.

10.12.6.26. TSF Channel PID Register(Default Value: 0x1FFF_0000)

Offset: TSF+0x4C			Register Name: TSF_CPIDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1fff	PIDMSK Filter PID Mask for Channel
15:0	R/W	0x0	PIDVAL Filter PID value for Channel

10.12.6.27. TSF Channel Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSF+0x50			Register Name: TSF_CBBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TSFBufBAddr Data Buffer Base Address for Channel It is 4-word (16Bytes) align address. The LSB four bits should be zero.

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10.12.6.28. TSF Channel Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSF+0x54			Register Name: TSF_CBSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CHDMAIntThd DMA Interrupt Threshold for Channel The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 00: 1/2 data buffer packet size 01: 1/4 data buffer packet size 10: 1/8 data buffer packet size 11: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0x0	CHBufPktSz Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 bytes. The maximum buffer size is 2MB. This size should be 4-word (16Bytes) aligned. The LSB four bits should be zero.

10.12.6.29. TSF Channel Buffer Write Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x58			Register Name: TSF_CBWPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BufWrPtr Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by software during the corresponding channel is enabled.

10.12.6.30. TSF Channel Buffer Read Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x5C			Register Name: TSF_CBRPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BufRdPtr Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is read.

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10.12.6.31. TSD Control Register(Default Value: 0x0000_0000)

Offset: TSD+0x00			Register Name: TSD_CTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TS Descramble Flag Clear 0: Clear 1: Not clear
15:2	/	/	/
1:0	R/W	0x0	DescArith Descramble Arithmetic 00: DVB CSA V1.1 01: DVB CSA V2.1 Others: Reserved

10.12.6.32. TSD Control Word Index Register(Default Value: 0x0000_0000)

Offset: TSD+0x1C			Register Name: TSD_CWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	CWI Control Word Index This value is the control index for control word access. Range is from 0x0 to 0x7.
3:0	R/W	0x0	CWII Control Word Internal Index 0000 : Odd Control Word 1ST 32-bit, OCW[31:0]; 0001 : Odd Control Word 2ND 32-bit, OCW[63:32]; 0100 : Even Control Word 1ST 32-bit, ECW[31:0]; 0101 : Even Control Word 2ND 32-bit, ECW[63:32]; Others: Reserved

10.12.6.33. TSD Control Word Register(Default Value: 0x0000_0000)

Offset: TSD+0x20			Register Name: TSD_CWR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CWD Content of control word corresponding to the TSD_CWIR value

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10.13. SCR

10.13.1. Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

Features:

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

10.13.2. Block Diagram

The top diagram of Smart Card Reader is as follows.

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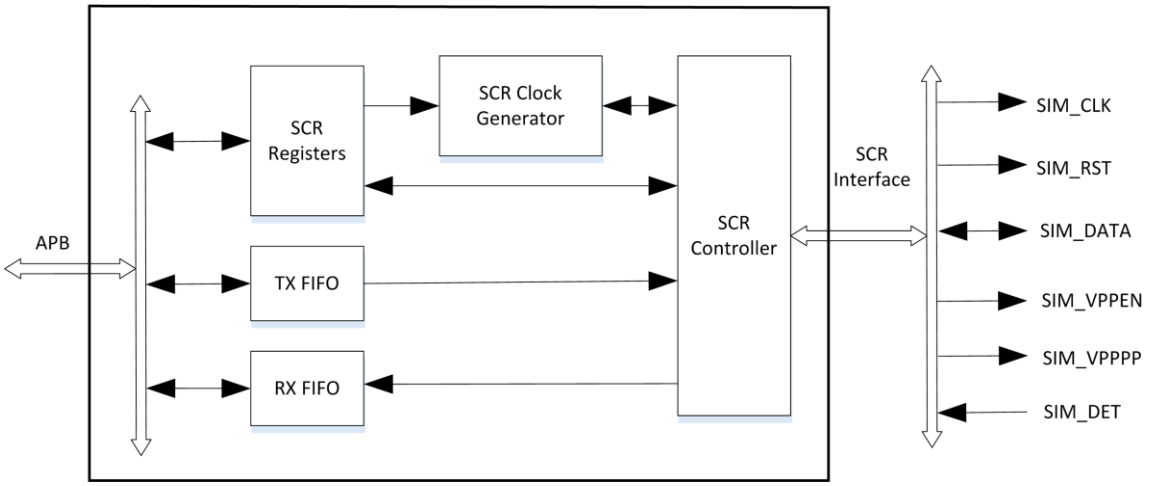

Figure 10- 62. SCR Block Diagram

10.13.3. Operations and Functional Descriptions

10.13.3.1. External Signals

The following table describes the external signals of SCR.

Table 10- 24. SCR External Signals

Signal	Description	Type
SIM_PWREN	Smart Card Power Enable	O
SIM_CLK	Smart Card Clock	O
SIM_DATA	Smart Card Data	I/O
SIM_RST	Smart Card Reset	O
SIM_DET	Smart Card Detect	I
SIM_VPPEN	Smart Card Program Voltage Enable	O
SIM_VPPPP	Smart Card Vpp Pause and Program Control	O

10.13.3.2. Clock Sources

The following table describes the clock sources of SCR.

Table 10- 25. SCR Clock Sources

Clock Sources	Description
APB2_CLK	APB2 Clock, Default value is 24MHz Crystal

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10.13.3.3. Timing Diagram

Please refer ISO/IEC 7816 and EMV2000 Specification.

10.13.3.4. Clock Generator

The clock generator generates clock signal and the baud clock impulse signal of the Smart Card, which are used in timing of the Smart Card Reader.

The Smart Card clock signal is used as the main clock for the smart card. Its frequency can be adjusted by using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock. The SCCLK frequency is given by the following equation:

$$f_{scclk} = \frac{f_{sysclk}}{2 * (SCCDIV + 1)}$$

f_{scclk} -- Smart Card Clock Frequency

f_{sysclk} -- System Clock (PCLK) Frequency

The baud clock impulse signal is used to transmit and receive serial between the SCR and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV). The value is used to divide the system clock. The BUAD rate is given by the following equation:

$$BAUD = \frac{f_{sysclk}}{2 * (BAUDDIV + 1)}$$

$BAUD$ -- Baud rate of the data stream between Smart Card and Reader.

The duration of one bit, Elementary Time Unit (ETU), is defined in the ISO/IEC 7816-3 specification. During the first answer to reset response after the cold reset, the initial ETU must be equal to 372 Smart Card Clock Cycles.

$$\frac{1}{BAUD} = ETU = \frac{372}{f_{scclk}}$$

In this case, the BAUDDIV should be

$$BAUDDIV = \frac{372 * f_{sysclk}}{2 * f_{scclk}} - 1 = 372 * (SCCDIV + 1) - 1 .$$

After the ATR is completed, the ETU can be changed according to Smart Card abilities.

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$$\frac{1}{BAUD} = ETU = \frac{F}{D} * \frac{1}{f_{scclk}}$$

F is the clock rate conversion integer. **D** the baud rate adjustment integer.

10.13.3.5. SCR IO Pad Configuration

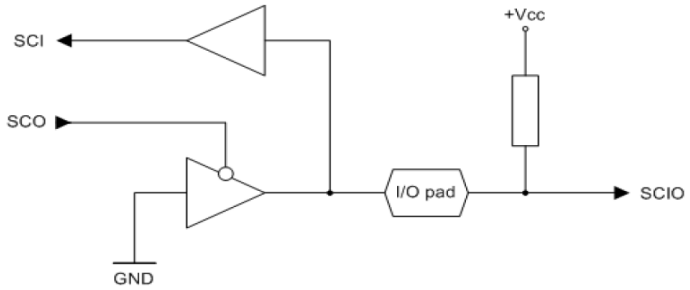

Figure 10- 63. SCR IO Pad Configuration Diagram

10.13.4. Register List

Module Name	Base Address
SCR	0x05005000

Register Name	Offset	Description
SCR_CSR	0x0000	Smart Card Reader Control and Status Register
SCR_INTEN	0x0004	Smart Card Reader Interrupt Enable Register 1
SCR_INTST	0x0008	Smart Card Reader Interrupt Status Register 1
SCR_FCSR	0x000C	Smart Card Reader FIFO Control and Status Register
SCR_FCNT	0x0010	Smart Card Reader RX and TX FIFO Counter Register
SCR_RPT	0x0014	Smart Card Reader RX and TX Repeat Register
SCR_DIV	0x0018	Smart Card Reader Clock and Baud Divisor Register
SCR_LTIM	0x001C	Smart Card Reader Line Time Register
SCR_CTIM	0x0020	Smart Card Reader Character Time Register
SCR_LCTLR	0x0030	Smart Card Reader Line Control Register
SCR_FSM	0x003C	Smart Card Reader FSM Register
SCR_DT	0x0040	Smart Card Reader Debounce Time Register
SCR_FIFO	0x0100	Smart Card Reader RX and TX FIFO Access Point

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10.13.5. Register Description

10.13.5.1. Smart Card Reader Control and Status Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: SCR_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	SCDET Smart Card Detected This bit is set to '1' when the scdetect input is active at least for a debounce time.
30:25	/	/	/
24	R/W	0x0	SCDETPOL Smart Card Detect Polarity This bit set polarity of scdetect signal. 0: Low Active 1: High Active
23:22	R/W	0x0	Protocol Selection (PTLSEL) 00: T=0 01: T=1, no character repeating and no guard time is used when T=1 protocol is selected. 10: Reserved 11: Reserved
21	R/W	0x0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
20	R/W	0x0	TSRXE TS Receive Enable When setting to '1', the TS character (the first ATR character) will be stored in RXFIFO during card session.
19	R/W	0x0	CLKSTPPOL Clock Stop Polarity The value of the scclk output during the clock stop state.
18	R/W	0x0	PECRXE Parity Error Character Receive Enable Enables storage of the characters received with wrong parity in RX FIFO.
17	R/W	0x0	MSBF MSB First When high, inverse bit ordering convention (msb to lsb) is used.
16	R/W	0x0	DATAPOL Data Plorarity When high, inverse level convention is used (A='1', Z='0').
15:12	/	/	/
11	R/W	0x0	DEACT Deactivation.

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			Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
10	R/W	0x0	ACT Activation. Setting of this bit initializes the activation sequence. When the activation is finished, the ACT bit is automatically cleared.
9	R/W	0x0	WARMRST Warm Reset Command. Writing '1' to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
8	R/W	0x0	CLKSTOP Clock Stop. When this bit is asserted and the smart card I/O line is in 'Z' state, the SCR core stops driving of the smart card clock signal after the CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is deasserted. New character transmission can be started after CLKSTARTDELAY time. The expiration of both times is signaled by the CLKSTOPRUN bit in the interrupt registers.
7:3	/	/	/
2	R/W	0x0	GINTEN Global Interrupt Enable. When high, IRQ output assertion is enabled.
1	R/W	0x0	RXEN Receiving Enable. When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
0	R/W	0x0	TXEN Transmission Enable. When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card.

10.13.5.2. Smart Card Reader Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: SCR_INTEN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt Enable.
22	R/W	0x0	SCACT Smart Card Activation Interrupt Enable.
21	R/W	0x0	SCINS Smart Card Inserted Interrupt Enable.

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20	R/W	0x0	SCREM Smart Card Removed Interrupt Enable.
19	R/W	0x0	ATRDONE ATR Done Interrupt Enable.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt Enable.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt Enable.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt Enable.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt Enable.
11	R/W	0x0	RXDONE RX Done Interrupt Enable.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt Enable.
9	R/W	0x0	RXFIFOFULL RX FIFO Full Interrupt Enable.
8:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt Enable.
3	R/W	0x0	TXDONE TX Done Interrupt Enable.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt Enable.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt Enable.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt Enable.

10.13.5.3. Smart Card Reader Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: SCR_INTST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W1C	0x0	SCDEA Smart Card Deactivation Interrupt. When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete. Write ‘1’ to clear.
22	R/W1C	0x0	SCACT Smart Card Activation Interrupt.

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			When enabled, this interrupt is asserted after the Smart Card activation sequence is complete. Write '1' to clear.
21	R/W1C	0x0	SCINS Smart Card Inserted Interrupt. When enabled, this interrupt is asserted after the smart card insertion. Write '1' to clear.
20	R/W1C	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal. Write '1' to clear.
19	R/W1C	0x0	ATRDONE ATR Done Interrupt. When enabled, this interrupt is asserted after the ATR sequence is successfully completed. Write '1' to clear.
18	R/W1C	0x0	ATRFAIL ATR Fail Interrupt. When enabled, this interrupt is asserted if the ATR sequence fails. Write '1' to clear.
17	R/W1C	0x0	C2CFULL Two Consecutive Characters Limit Interrupt. When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards. Write '1' to clear.
16	R/W1C	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt. When enabled, this interrupt is asserted in two cases: ● When the smart card clock is stopped. ● When the new character can be started after the clock restart. To distinguish between the two interrupt cases, we recommend reading the CLKSTOP bit in SCR_CTRL1 register. Write '1' to clear.
15:13	/	/	/
12	R/W1C	0x0	RXPERR RX Parity Error Interrupt. When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used. Write '1' to clear.
11	R/W1C	0x0	RXDONE

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			RX Done Interrupt. When enabled, this interrupt is asserted after a character was received from the Smart Card. Write '1' to clear.
10	R/W1C	0x0	RXFIFOTHD RX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold. Write '1' to clear.
9	R/W1C	0x0	RXFIFOFULL RX FIFO Full Interrupt. When enabled, this interrupt is asserted if the RX FIFO is filled up. Write '1' to clear.
8:5	/	/	/
4	R/W1C	0x0	TXPERR TX Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard time after the character transmission was repeated TXREPEAT times or T=1 protocol is used. Write '1' to clear.
3	R/W1C	0x0	TXDONE TX Done Interrupt. When enabled, this interrupt is asserted after one character was transmitted to the smart card. Write '1' to clear.
2	R/W1C	0x0	TXFIFOTHD TX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold. Write '1' to clear.
1	R/W1C	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out. Write '1' to clear.
0	R/W1C	0x0	TXFIFODONE TX FIFO Done Interrupt. When enabled, this interrupt is asserted after all bytes from TX FIFO ware transferred to the Smart Card. Write '1' to clear.

10.13.5.4. Smart Card Reader FIFO Control and Status Register(Default Value: 0x0000_0101)

Offset: 0x000C			Register Name: SCR_FCSR
Bit	**Read/Write**	**Default/Hex**	**Description**

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31:11	/	/	/
10	R/W	0x0	RXFIFOFLUSH Flush RX FIFO. RX FIFO is flushed, when '1' is written to this bit.
9	R	0x0	RXFIFOFULL RX FIFO Full.
8	R	0x1	RXFIFOEMPTY RX FIFO Empty.
7:3	/	/	/
2	R/W	0x0	TXFIFOFLUSH Flush TX FIFO. TX FIFO is flushed, when '1' is written to this bit.
1	R	0x0	TXFIFOFULL TX FIFO Full.
0	R	0x1	TXFIFOEMPTY TX FIFO Empty.

10.13.5.5. Smart Card Reader FIFO Count Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SCR_FIFOCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	RXFTH RX FIFO Threshold These bits set the interrupt threshold of RX FIFO. The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold.
23:16	R/W	0x0	TXFTH TX FIFO Threshold These bits set the interrupt threshold of TX FIFO. The interrupt is asserted when the number of bytes in TX FIFO is equal to or less than the threshold.
15:8	R	0x0	RXFCNT RX FIFO Counter These bits provide the number of bytes stored in the RXFIFO.
7:0	R	0x0	TXFCNT TX FIFO Counter These bits provide the number of bytes stored in the TXFIFO.

10.13.5.6. Smart Card Reader Repeat Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: SCR_REPEAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:4	R/W	0x0	RXRPT

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			RX Repeat This is a 4-bit register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the error signal during the guard time.
3:0	R/W	0x0	TXRPT TX Repeat This is a 4-bit register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guard time.

10.13.5.7. Smart Card Reader Clock Divisor Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SCR_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	BAUDDIV Baud Clock Divisor. This 16-bit register defines the divisor value used to generate the Baud Clock impulses from the system clock. $BAUD = \frac{f_{sysclk}}{2 * (BAUDDIV + 1)}$
15:0	R/W	0x0	SCCDIV Smart Card Clock Divisor. This 16-bit register defines the divisor value used to generate the Smart Card Clock from the system clock. $f_{scclk} = \frac{f_{sysclk}}{2 * (SCCDIV + 1)}$ f_{scclk} is the frequency of Smart Card Clock Signal. f_{sysclk} is the frequency of APB Clock.

10.13.5.8. Smart Card Reader Line Time Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SCR_LTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	ATR ATR Start Limit. This 16-bit register defines the maximum time between the rising edge of the *scrstn* signal and the start of ATR response.

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			ATR Start Limit = 256* ATR* T_{scclk} .
15:8	R/W	0x0	RST Reset Duration. This 16-bit register sets the duration of the Smart Card reset sequence. This value is same for the cold and warm reset. Cold/Warm Reset Duration = 256* RST* T_{scclk} .
7:0	R/W	0x0	ACT Activation/Deactivation Time. This 16-bit register sets the duration of each part of the activation and deactivation sequence. Activation/Deactivation Duration = 256* ACT * T_{scclk} . $T_{scclk} = \frac{1}{f_{scclk}}$ is Smart Card Clock Cycle.

10.13.5.9. Smart Card Reader Character Time Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SCR_CTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	CHARLIMIT Character Limit. This 16-bit register sets the maximum time between the leading edges of two consecutive characters. The value is ETUs.
15:8	/	/	/
7:0	R/W	0x0	GUARDTIME Character Guard time. This 8-bit register sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in ETUs. The parity error is besides signaled during the guard time.

10.13.5.10. Smart Card Reader Line Control Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SCR_PAD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DSCVPPPP Direct Smart Card Vpp Pause/Prog. It provides direct access to SCVPPPP output.
6	R/W	0x0	DSCVPPEN Direct Smart Card Vpp Enable.

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			It provides direct access to SCVPPEN output.
5	R/W	0x0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSVPPEN and DSVPPPP signals during activation and deactivation sequence.
4	R/W	0x0	DSCVCC Direct Smart Card VCC. When DIRACCPADS='1', the DSCVCC bit provides direct access to SCVCC pad.
3	R/W	0x0	DSCRST Direct Smart Card Clock. When DIRACCPADS='1', the DSCRST bit provides direct access to SCRST pad.
2	R/W	0x0	DSCCLK Direct Smart Card Clock. When DIRACCPADS='1', the DSCCLK bit provides direct access to SCCLK pad.
1	R/W	0x0	DSCIO Direct Smart Card Input/Output. When DIRACCPADS='1', the DSCIO bit provides direct access to SCIO pad.
0	R/W	0x0	DIRACCPADS Direct Access to Smart Card Pads. When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

10.13.5.11. Smart Card Reader FSM Register(Default Value: 0x0000_0000)

Offset: 0x003C			**Register Name: SCR_FSM**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ATR_STRUCTURE_FSM
23:16	R	0x0	ATR_FSM
15:8	R	0x0	ACT_FSM
7:0	R	0x0	SCR_FSM

10.13.5.12. Smart Card Reader Debounce Time Register(Default Value: 0x0000_03FF)

Offset: 0x0040			**Register Name: SCR_DT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x3ff	SCR_DEBOUNCE_TIME Set the debounce time value for card insert detecting.The time uint is the cycle of SCCLK.

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10.13.5.13. Smart Card Reader FIFO Data Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SCR_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	FIFO_DATA This 8-bit register provides access to the RX and TX FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer.

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Chapter 11 Security System

11.1. Crypto Engine

11.1.1. Overview

The Crypto Engine(CE) module is one encryption/decryption algorithm accelerator. It supports kinds of symmetric, asymmetric, Hash, and RNG algorithms. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels, and has an internal DMA controller to transfer data between CE and memory.

The CE has the following features:

- Symmetrical algorithm: AES, DES, 3DES
- Hash algorithm: MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC-SHA1,HMAC-SHA256
- Asymmetrical algorithm: RSA512/1024/2048bit
- 160-bit hardware PRNG with 175-bit seed
- 256-bit hardware TRNG
- ECB, CBC, CTR, CTS, OFB, CFB modes for AES
- ECB, CBC, CTR modes for DES/3DES
- 16-, 32-, 64-, 128-bit wide size for AES CTR
- 1-, 8-, 64-, 128-bit width for AES-CFB
- 16-, 32-, 64-bit wide size for DES/3DES CTR
- 128-, 192-, 256-bit key size for AES
- Multi-package mode for MD5/SHA1/SHA224/SHA256/SHA384/SHA512
- Internal DMA controller for data transfer with memory
- Supports secure and non-secure interfaces respectively

11.1.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

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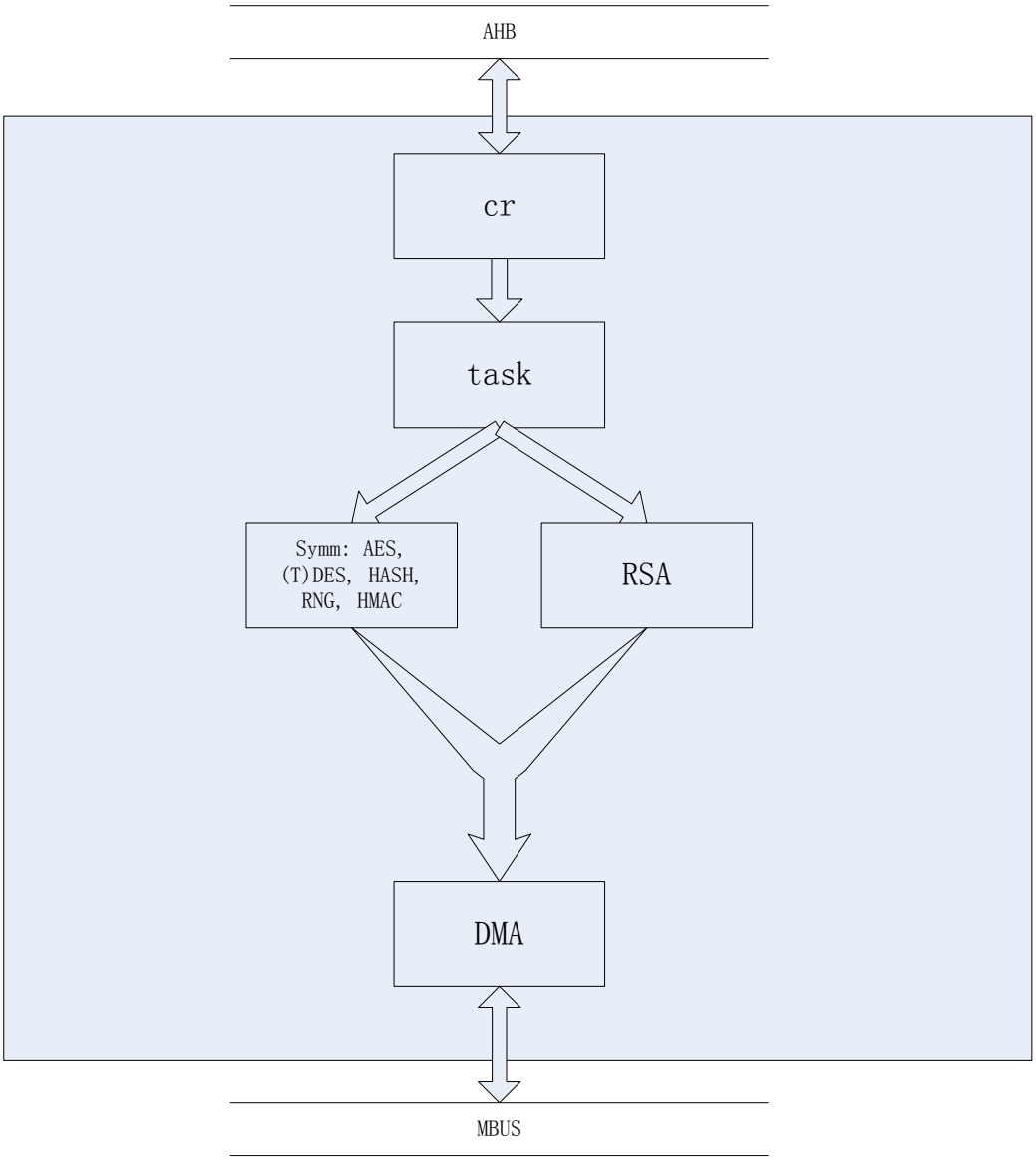

Figure 11- 1. CE Block Diagram

11.1.3. Operations and Functional Descriptions

11.1.3.1. Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

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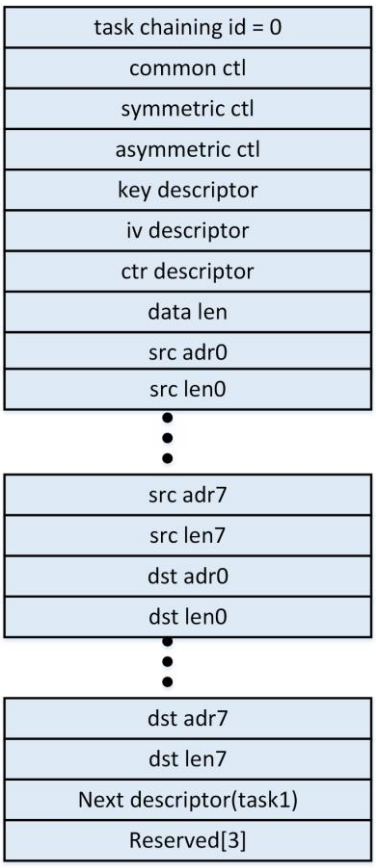

Figure 11- 2. Task Chaining

Task chaining id supports 0~3.

11.1.3.2. Task Descriptor Queue Common Control

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:17	/	/	/
16	R/W	0x0	IV mode IV mode for SHA1/SHA224/SHA256/SHA384/SHA512/MD5 or constants 0: use initial constants defined in FIPS-180 1: use input iv
15	R/W	0x0	Last HMAC plaintext 0: not the last HMAC plaintext package 1: the last HMAC plaintext package
14:9	/	/	/
8	R/W	0x0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption

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7	/	/	/
6:0	R/W	0x0	Algorithm Type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x10: MD5 0x11: SHA-1 0x12: SHA-224 0x13: SHA-256 0x14: SHA-384 0x15: SHA-512 0x16: HMAC-SHA1 0x17: HMAC-SHA256 0x20: RSA 0x30: TRNG 0x31: PRNG Others: reserved

11.1.3.3. Task Descriptor Queue Symmetric Control

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	KEY_SELECT key select for AES 0000: Select input CE_KEYx (Normal Mode) 0001: Select {SSK} 0010: Select {HUK} 0011: Select {RSSK} 0100-0111: Reserved 1000-1111: Select internal Key n (n from 0 to 7)
19:18	R/W	0x0	CFB_WIDTH For AES-CFB width 00: CFB1 01: CFB8 10: CFB64 11: CFB128
17	R/W	0x0	PRNG_LD Load new 15bits key into lfsr for PRNG
16	R/W	0x0	AES CTS last package flag When setting to '1', it means this is the last package for AES-CTS mode(the size of the last package >128bit).
15:12	/	/	/
11:8	R/W	0x0	ALGORITHM_MODE CE algorithm mode

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			0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: CipherText Stealing (CTS) mode 0100: Output feedback (OFB)mode 0101: Cipher feedback (CFB)mode Other: reserved
7:4	/	/	/
3:2	R/W	0x0	CTR WIDTH Counter width for CTR mode 00: 16-bit Counter 01: 32-bit Counter 10: 64-bit Counter 11: 128-bit Counter
1:0	R/W	0x0	AES KEY SIZE 00: 128-bit 01: 192-bit 10: 256-bit 11: Reserved

11.1.3.4. Task Descriptor Queue Asymmetric Control

Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x0	RSA Pubic Modulus Width 000:512-bit 001:1024-bit 010:2048-bit Other: reserved
27:0	/	/	/

11.1.3.5. Task Request

Basically, there are 4 steps for one task handling from software.

Step1: Software should configure task descriptor in memory, including all fields in descriptor. Channel id corresponds to one channel in CE.According to algorithm type, software should set the fields in common control, symmetric control, asymmetric control, then provide key/iv/ctr address and the data length of this task. Source and destination sg address and size are set based on upper application. If there is another task concatenating after this task, then set its descriptor address at next descriptor field.

Step 2: Software should set registers, including task descriptor address, interrupt control.

Step 3: Software reads load register to ensure that the bit0 is zero, then starts request by pulling up the bit0 of the load register.

Step 4: Wait interrupt status.

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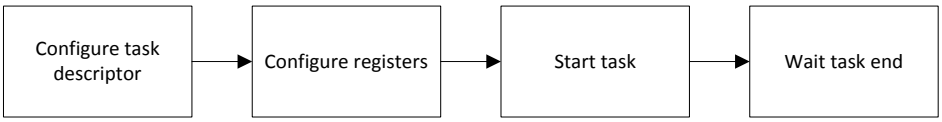

Figure 11- 3. Task Request Process

11.1.3.6. Data Length Setting

Data length field in task descriptor has different meaning for different algorithms.
For AES-CTS, data length field indicates valid source data byte number, for others indicate source data words number.
For PRNG, data length should be 5 words aligned.
For TRNG should be 8 words aligned.
Data size in source and destination sg is as words, whose value should corresponds with data length field, or else CE will report error and stop execution.

11.1.3.7. Security Operation

When CPU issues request to CE module, CE module will save the secure mode of CPU. When executing this request, this state bit works as access tag for inner and system resource. For HUK/RSSK/SSK from SID, only secure mode can access, or else these keys will be used as 0. For access to SID and keysram module through AHB bus, only secure mode can success, or else will read 0 or can not write. When issuing MBUS read and write requests, CE will use send this secure mode bit to BUS, so secure request can access secure and non secure space, but non secure request only can access non secure space.

11.1.3.8. Error Check

CE module includes error detection for task configuration, data computing error, and authentication invalid. When algorithm type in task description is read into module, CE will check if this type is supported through checking algorithm type field in common control. If type value is out of scope, CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting task descriptor, input size and output size configuration will be checked to avoid size error. If size configuration is wrong, CE will issue interrupt signal and set error state.

11.1.3.9. Clock Requirement

Clock Name	Description	Requirement
hclk	AHB bus clock	24MHz ~ 200MHz
mclk	MBUS clk	24MHz ~ 400MHz
ce_clk	CE work clock	24MHz ~ 300MHz

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11.1.4. Register List

Module Name	Base Address
CE_NS	0x01904000
CE_S	0x01904800

Register Name	Offset	Description
CE_TDA	0x0000	Task Descriptor Address
CE_CTL	0x0004	Control Register
CE_ICR	0x0008	Interrupt Control Register
CE_ISR	0x000C	Interrupt Status Register
CE_TLR	0x0010	Task Load Register
CE_TSR	0x0014	Task Status Register
CE_ESR	0x0018	Error Status Register
CE_CSA	0x0024	DMA Current Source Address
CE_CDA	0x0028	DMA Current Destination Address
CE_TPR	0x002C	Throughput Register

11.1.5. Register Description

11.1.5.1. CE Task Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Task Descriptor Address

11.1.5.2. CE Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	RSA CLK Gating Enable(only for CE_S) 0: RSA clk gating enable 1: RSA clk gating disable
2:0	/	/	/

11.1.5.3. CE Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

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3:0	R/W	0x0	Task Channel3~0 Interrupt Enable 0: Disable 1: Enable

11.1.5.4. CE Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W1C	0x0	Task Channel3~0 End Pending 0: Not finished 1: Finished It indicates if task has been completed . Write '1' to clear it.

11.1.5.5. CE Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	Task Load When setting, CE can load the descriptor of task if task FIFO is not full.

11.1.5.6. CE Task Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R	0x0	Running Channel Number 00: Task channel0 01: Task channel1 10: Task channel2 11: Task channel3

11.1.5.7. CE Error Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W1C	0x0	Task Channel3 Error Type

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			xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write '1' to clear. 1xxx: Reserved
11:8	R/W1C	0x0	Task Channel2 Error Type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write '1' to clear. 1xxx: Reserved
7:4	R/W1C	0x0	Task Channel1 Error Type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write '1' to clear. 1xxx: Reserved
3:0	R/W1C	0x0	Task Channel0 Error Type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write '1' to clear. 1xxx: Reserved

11.1.5.8. CE Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_CSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Current source address

11.1.5.9. CE Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_CDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Current destination address

11.1.5.10. CE Throughput Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_TPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/WC	0x0	It indicates the throughput writing to this register at last time. Writing to this register will clear it to 0.

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11.2. Security ID

The Security ID(SID) is 2.5 Kbits electrical efuse for saving key, which includes chip ID, thermal sensor, HASH code and security key,etc.

The SID module has the following features:

- The module register is non-secure forever, efuse has secure zone and non-secure zone
- A fuse only can program one time
- Loading the key to CE

For complete SID information, refer to the ***Allwinner T7 SID Specification***.

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