Features

- XuanTie 64-bit RISC-V C906 CPU, up to 480 MHz
- HiFi5 Audio DSP, up to 400 MHz
- Arm M33 Star MCU, up to 192 MHz
- Memories
  - 1MB SRAM
  - SiP 8 MB/16 MB Flash
  - 8 MB HS-PSRAM in R128-S1
  - 8 MB LS-PSRAM & 8 MB HS-PSRAM in R128-S2
  - 32 MB HS-PSRAM in R128-S3
  - 2048-bit efuse
- Image and Graphics
  - Supports Graphic 2D accelerator with rotate, mixer, and 4 layers
  - Supports RGB output interface, up to 1024 x 768@60fps
  - Supports display engine
- Video Input
  - 8-bit parallel CSI interface
  - Supports both online and offline mode for JPEG encoder
  - Supports JPEG encoder, 1920 x 1088
- Analog Audio Codec
  - 2 DAC channels 24-bit audio codec for R128-S1 and R128-S2
  - 1 DAC channel 24-bit for R128-S3
  - 3 ADC channels
  - Supports USB audio playback
  - Up to 119dB SNR during DAC playback path (signal through DAC and lineout with A-weighted filter)
  - Up to 98dB SNR during ADC record path (signal through PGA and ADC with A-weighted filter)
- One I2S/TDM/PCM external interface (I2S0)
- Security Engine
  - Symmetrical algorithm: AES, DES, 3DES
  - Hash algorithm: MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC
  - Asymmetrical algorithm: RSA512/1024/2048bit
  - Supports TRNG
- External Peripherals
  - One USB 2.0 DRD
  - Up to 3 UART controllers (UART0, UART1, UART2)
  - Up to 2 SPI controllers (SPI0, SPI1)
  - Up to 2 TWIs
  - One CIR RX and one CIR TX
  - Up to 8 PWM channels (PWM[7:0])
  - Up to 7 GPADC input channels (R128-S1 & R128-S2)/8 channels (R128-S3)

- One LEDC used to control the external intelligent control LED lamp

- Package

  QFN80, 0.35 mm pitch, 8 mm x 8 mm body

Revision History

Revision	Date	Author	Description
0.1	Jan 27, 2022	KPA0569	Draft version
0.2	Mar 18, 2022	KPA0569	Modified contents based on suggestions raised by reviewers
0.3	Mar 25, 2022	KPA0569	Modified contents based on suggestions raised by reviewers
0.4	Apr 18, 2022	KPA0569	Modified contents based on suggestions raised by reviewers
0.5	July 19, 2022	KPA0569	Modified contents based on suggestions raised by reviewers
0.6	November 14, 2022	KPA0570	1. Update some pin names and pinmap 2. Delete VCC-IO-5V 3. Add the pin of VCC33-USB
0.7	December 23, 2022	KPA0570	1. Update the block diagram. 2. Update the Memory Subsystem. 3. Delete the operating temperature in Table 6-1. 4. Delete the pin of RSTN. 5. Update the voltages of VDD-SYS, VDD-DSP, and VDD-RTC. 6. Delete the section 6-8 Internal Reset Electrical Characteristics. 7. Update the voltage range of PMU and GPADC. 8. Update the section 6.5 the parameter of GPADC electrical. 9. Update the junction temperature of chip. 10. Update the features in the cover page. 11. Update the section 3.8.1 Audio Codec, 3.8.4 OWA, 3.10.6 GPADC 12. Update section 6.1, 6.2, 6.6, 6.8, 6.9, 6.10, 6.11, 6.12.

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package, and part reliability of the R128 processor. For details about register descriptions of each module, see the ***Allwinner_R128_User_Manual***.

Intended Audience

The document is intended for:

Hardware designers and maintenance personnel for electronics

Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	Indicates potential risk of injury or death exists if the instructions are not obeyed.
CAUTION	Indicates potential risk of equipment damage, data loss, performance degradation, or unexpected results exists if the instructions are not obeyed.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1 Overview

R128 is a highly integrated wireless audio SoC with high performance. It features a XuanTie RISC-V CPU, a HiFi5 DSP, an Arm M33 star MCU, an 802.11b/g/n WLAN & Dual-mode Bluetooth5.0 subsystem, a Voice & Audio CODEC subsystem, and a Power Management Unit (PMU). RISC-V C906 CPU and HiFi5 DSP provide powerful and energy-efficient computing power for applications and audio processing respectively. R128 integrates 3 differential ADCs and 2 differential DACs and can be applied to microphone array-based voice recognition and stereo audio playback solutions. Wi-Fi and bluetooth enable R128 to implement various network applications with an exclusive antenna for each to simultaneously transmit and receive data on 2.4 GHz. R128 also integrates a JPEG encoder, a RGB display engine, and a 2D graphics acceleration system, making it possible to achieve some display applications.

2 Device Difference

R128 is configured with different sets of features in different devices. The following table shows the feature differences across different devices.

Table 2-1 Out-of-bag Duration

Contents	R128-S1	R128-S2	R128-S3
SIP Nor Flash	8 MB	16 MB	Not Support
PSRAM	8 MB	16 MB	32 MB
Audio Codec Output	LINEOUTLP/N LINEOUTRP/N	LINEOUTLP/N LINEOUTRP/N	LINEOUTLP/N
GPADC Channels	7	7	8

3 Features

3.1 CPU Architecture

- XuanTie C906 64-bit RISC-V CPU, up to 480 MHz
  - 32 KB I-cache + 32 KB D-cache
- ARM M33 Star MCU, up to 192 MHz
  - 32 KB I-cache + 32 KB D-cache
  - Trust Zone

3.2 DSP Architecture

- HiFi5 Audio DSP@400 MHz
  - 32 KB I-cache + 32 KB D-cache

3.3 Memory Subsystem

3.3.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
  - SD/eMMC
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Secure BROM supports load only certified firmware
- Secure BROM ensures that the secure boot is a trusted environment
- Support USB eFEX protocol and UART mboot protocol for firmware upgrade

3.3.2 PSRAMC

- Up to 2 PSRAM controllers (HS_PSRAMC, LS_PSRAMC)

HS_PSRAMC:

- R128-S1/R128-S2: SIP 8 MB PSRAM
- R128-S3: SIP 32 MB PSRAM
- Supports AP memory PSRAM
- Supports 64 Mbit/256 Mbit PSRAM
- Supports OPI as the interface of PSRAM
- Supports the auto-refreshing and self-refreshing of PSRAM
- Supports up to 800 MHz PSRAM. The ratio of PSRAM controller and PSRAM clock is 1:4.

- Supports indirectly accessing the registers of PSRAM through interface configuration
- Supports selecting various PSRAM clocks to reach capacity expansion.
- Supports caching reading/writing commands through CAM
- Supports out-of-order execution of commands
- Supports prefetching read channel

LS_PSRAMC:

- R128-S2: SIP 8 MB PSRAM
- Supports any frequency ratio of AHB and OPI clock
- Supports CPU/DMA to operate PSRAM through SBUS
- Supports PSRAM Wrap Mode (enter/exit)
- Supports 4 offset address ranges
- Supports CBUS out-of-order reading/writing and XIP code execution

3.3.3 SMHC

- Compatible with Secure Digital Memory (SD 2.0)
- Compatible with Secure Digital I/O (SDIO 3.0)
- Compatible with embedded MultiMediaCard (eMMC 5.0)
- Supports Card insertion and removal interrupt
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 1024-Bytes RX FIFO and 1024-Bytes TX FIFO
- Supports 1-bit, 4-bit SD and SDIO data bus width
- Supports 1-bit, 4-bit eMMC data bus width

3.3.4 Flashc_Enc

- Supports arbitrary frequency ratio of AHB clock and SPI clock
- Supports 4 segments of offset address range
- Supports receiving and transmitting in 1/2/4-wire SPI
- Supports flash programing and reading by configuring registers (SBUS)
- Supports out-of-order reading CBUS and running codes through XIP
- Supports continuous reading mode (enter/exit) and wrap mode (enter/exit)
- Supports the basic operation of SPI flash
- Supports 8 MB SIP Nor Flash (for R128-S1) and 16 MB SIP Nor Flash (for R128-S2)

- Supports real-time AES encoding and decoding when reading and writing data through SBUS data and reading data through CBUS

3.4 System Peripherals

3.4.1 PMU

- Supports 3.0 V-5.5 V external single supply
- Integrates DCDC/LDO and other power modules, and power all circuits within the IC
- The internal digital circuit is divided into power domains. Each of them has independent power switch, which is determined by system low-power status.
- Supports standby, hibernation and other low-power modes, which can be switched over by PMU.
- Manages the opening and close of analog modules like DCDC/LDO, DCXO/DPLL. The starting duration is configured by the software.

3.4.2 GPRCM

- Manages the power of this system
- Manages the reset of each system
- Manages the OSC clock

3.4.3 Clock Controller Unit (CCU)

- Up to 2 CCU controllers (CCU, CCU_AON)

CCU:

- Supports configuring module clock
- Supports clock output control
- Supports bus clock gating
- Supports bus software reset

CCU_AON:

- Supports managing the OSC clock
- Supports bus source and divisions
- Supports configuring modules clock
- Supports clock output control
- Supports bus clock gating
- Supports bus software reset

3.4.4 DMAC

- Up to 2 DMACs
- Up to 16 DMA channels for each DMAC
- Provides 32 peripheral DMA requests for data reading and 32 peripheral DMA requests for data writing
- Supports transferring data with a linked list

- Supports programmable 8-bit, 16-bit, 32-bit, and 64-bit data width
- Supports programmable DMA burst length
- DRQ response includes the waiting mode and handshake mode
- DMA channel supports pause function
- Memory devices support non-aligned transfer

3.4.5 Timer

- 8 timers: 5 for SW domain and 3 for AON domain
- Configurable counting clock: LOSC and OSC40M. Whether LOSC is internal low-frequency clock or external low-frequency clock (with greater accuracy) depends on LOSC_SRC_SEL.
- Supports 8 prescale factors
- Programmable 32-bit down timer
- Supports two timing modes: periodic mode and single counting mode
- Generates an interrupt when the count is decreased to 0

3.4.6 Watchdog

- Up to 4 watchdogs, among which one is secure world watchdog
- HOSC_32K clock sources and 32K system
- Supports 12 configurable initial count value
- Supports generating timeout interrupt
- Supports outputting reset signal
- Supports restarting timer

3.4.7 Message Box (MSGBOX)

- Supports 3 CPU to transmit information through channels. Each CPU has a MSGBOX
  - CPU0: M33
  - CPU1: C906
  - CPU2: DSP
- There are four channels every two CPU, and the FIFO depth of one channel is 8 x 32 bits
- Supports interrupts

3.4.8 Spinlock

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable (less than 200 cycles)

3.4.9 RTC

- Implements time counter and timing wakeup
- Provides counters for counting year, month, day, hour, minute, and second

- 4-channel clock sources: HOSC_32K, RCCAL_32K, RCOSC, LOSC_CLK
- Configures initial value by software anytime
- Supports timing alarm, and generates interrupt and wake up the PMU system

3.5 Video and Graphics

3.5.1 DE

- Supports output size up to 1024x1024
- Supports two alpha blending UI channels for main display
- Supports four overlay layers in each channel, and channel0 has an independent scaler
- Supports potter-duff compatible blending operation
- Supports input format ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Supports SmartColor2.0 for excellent display experience
  - Fully programmable color matrix
  - Dynamic gamma
- Supports write back only for verification

3.5.2 G2D

- Supports layer size up to 1024x1024 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports any format convert function above
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter and 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate for normal buffer

3.6 Video Input

CSI_JPEG

CSI:

- Supports YUV422 format input and YUV420 format NV12 output
- Supports cropwin
- Supports receiving JPEG streams directly output by sensor

- Supports receiving the images with unconventional resolutions (X and Y can be an integer multiple of 16, such as: 192*192, 304*224)
- Supports receiving the images with conventional resolutions (such as 128*128, 256*256, 320*240, 640*480, 1280*720, 1920*1088)

JPEG:

- Supports 640*480@60fps in the online mode, and 640*480@30fps in the offline mode
- Supports 1280*720@40fps in the online mode, and 1280*720@20fps in the offline mode
- Supports up to 1920*1088 online/offline encoding
- Supports encoding after scaling images down 1/2 and cropwin
- Supports block output in the online mode to reduce SRAM usage and improve bandwidth utilization ratio
- Supports online/offline encoding (such as 192*192 and 304*224) the images with non-conventional resolution
- Supports the online/offline encoding the images with conventional resolution images

3.7 Video Output

TCON_LCD

- Supports RGB interface with DE/SYNC mode, up to 1024x768@60fps
- Supports serial RGB/dummy RGB interface, up to 800x480@60fps
- Supports i8080 interface, up to 800x480@60fps
- Supports BT656 interface for NTSC and PAL
- Supports RGB666 and RGB565 with dither function

3.8 Audio Interfaces

3.8.1 Audio Codec

- HiFi Audio ADC
  - 3-channel ADCs @ 24-bit
  - Up to 98dB SNR during ADC recording path (signal through PGA and ADC with A-weighted filter)
  - 3 fully-differential analog microphone inputs with 0dB~30dB amplifier gain
  - Support sample rates ranging from 8 kHz to 96 kHz
  - Digital volume control with 0.5dB step
  - Digital high-pass filter
  - 128x24-bit FIFO for recording received data
- HiFi Audio DAC
  - 2-channel DACs @ 24-bit (for R128-S1 and R128-S2)
  - 1-channel DAC @ 24-bit (for R128-S3)
  - Up to 119dB SNR in the DAC playback path (signal through DAC and lineout with A-weighted filter)

- Supports sample rates ranging from 8 kHz to 192 kHz
- Digital volume control with 0.5dB step
- 20-band Biquads filter for EQ
- 3-band dynamic range control
- 128x24-bit FIFO for playing transmitted data

- Three differential microphone inputs: MICIN1P/N, MICIN2P/N, MICIN3P/N
- Two stereo LINEOUT outputs: LINEOUTLP/N and LINEOUTRP/N (for R128 S1 and R128 S2)
- One differential LINEOUT output: LINEOUTLP/N (for R128 S3)
- Built-in audio PLL with flexible clocking scheme
- DMA and interrupt support both receiving and transmitting
- Integrated ALDO for analog part
- One low-noise analog microphone bias output three audio inputs

3.8.2 I2S/PCM

- One I2S/PCM external interface for connecting external power amplifier and MIC ADC
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and Receive data FIFOs
  - Programmable FIFO thresholds
  - 128 depth x 32-bit width TXFIFO,64 depth x 32-bit width RXFIFO
- Supports multiple function clock
  - Clock up to 24.576MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
  - Clock up to 12.288MHz Data Input of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)
- Supports TX/RX DMA Slave interface
- Supports Multiple application scenarios
  - Up to 16 channel (fs = 48khz) which has adjustable width from 8-bit to 32-bit
  - Sample rate from 8KHz to 384KHz (CHAN = 2)
  - 8-bits u-law and 8-bits A-law companded sample
- Supports Master/Slave mode

3.8.3 DMIC

- Supports up to 8 channels
- Sample rate from 8 kHz to 48 kHz

3.8.4 OWA

- One OWA TX and one OWA RX
- Compliance with S/PDIF Interface
- Compatible with standard IEC-60958 and IEC-61937
  - IEC-60958 supports 16-bit, 20-bit and 24-bit data formats
  - IEC-61937 uses the IEC-60958 series for the conveying of non-linear PCM bit streams, each sub-frame transmits 16-bit
- TXFIFO and RXFIFO
  - One 128 x 24bits TXFIFO and one 64 x 24bits RXFIFO for audio data transfer
  - Programmable FIFO thresholds
- Supports TX/RX DMA slave interface
- Supports multiple function clock
  - Separate clock for OWA TX and OWA RX
  - The TX function clock supports the frequency of 24.576 MHz and 22.579 MHz
  - The RX function clock supports the frequency of 60MHz and 240MHz, which can realize the sampling rate of 8 kHz to 96 kHz and 32 kHz to 192 kHz respectively
- Supports hardware parity on TX/RX
  - Hardware parity generation on the transmitter
  - Hardware parity checking on the receiver
- Supports channel status capture for the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter
- Supports interrupts and DMA

3.9 Security Subsystem

3.9.1 Crypto Engine (CE)

- Supports Symmetrical Algorithm: AES, DES, 3DES
- Supports 128-bits, 192-bits and 256-bits key size for AES
- Supports ECB, CBC, CTR, CTS, OFB, CFB modes for AES
- Supports 1, 8, 64, 128bit width for AES-CFB
- Supports 16bit, 32bit, 64bit, 128bit wide size for AES CTR
- Supports ECB, CBC, CTR, CBC_MAC modes for DES/3DES
- Supports 16bit, 32bit, 64bit wide size for DES/3DES CTR
- Supports Hash Algorithms: MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC
- Supports multi-package mode for MD5, SHA1, SHA224, SHA256, SHA384, SHA512

- Supports Asymmetrical Algorithm: RSA512/1024/2048bit
- Supports internal DMA Controller for data transfer with memory
- Supports secure and non-secure interfaces respectively
- Supports accessing Secure and non-secure inferfaces by non-secure host when secure_mode is 0

3.9.2 Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Sets secure area of HSPSRAM
- Sets secure property that Master accesses to HSPSRAM

3.9.3 Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Sets secure property of peripherals

3.10 External Peripherals

3.10.1 USB 2.0 DRD

- Complies with USB 2.0 Specification
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 10 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, and Endpoint5)
- Supports up to (8KB+64Bytes) FIFO for EPs (Including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every Eps

3.10.2 UART

- Up to 3 UART controllers (UART0, UART1, and UART2)
- Compatible with industry-standard 16450/16550 UARTs

- 64-Bytes Transmit and receive data FIFOs
- Supports DMA controller interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485 mode

3.10.3 SPI and SPI_DBI

- Up to 2 SPI controllers (SPI0, SPI1)
- The SPI0 only supports SPI mode. The SPI1 supports SPI mode and display bus interface (DBI) mode

SPI mode:

- Full-duplex synchronous serial interface
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable, and four chips select to support multiple peripherals.
- Support interrupts and DMA
- Support mode0, mode1, mode2, and mode3
- Support 3-wire/4-wire SPI
- Support programmable serial data frame length: 0 bit to 32 bits
- Support standard SPI, dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI
- Support maximum IO rate of the mass production: 96 MHz
- Support 5 clock sources

DBI mode:

- Support DBI Type C 3 Line/4 Line Interface Mode
- Support 2 Data Lane Interface Mode
- Support data source from CPU or DMA
- Support RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Support Tearing effect
- Support software flexible control video frame rate

3.10.4 Two Wire Interface (TWI)

- Supports 2 TWIs
- Software-programmable for Slave or Master
- Supports Repeated START signal
- Allows 10-bit addressing with TWI bus

- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400 kbits/s (fast mode)
- Allows operation from a wide range of input clock frequencies
- TWI Driver Supports packet transmission and DMA when TWI works in Master mode

3.10.5 PWM

- Supports 8 independent PWM channels (PWM0 to PWM7)
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range: 0 to 24 MHz or 100 MHz
  - Various duty-cycle: 0% to 100%
  - Minimum resolution: 1/65536
- Supports 4 complementary pairs output
  - PWM01 pair (PWM0 + PWM1), PWM23 pair (PWM2 + PWM3), PWM45 pair (PWM4 + PWM5), PWM67 pair (PWM6 + PWM7)
  - Supports dead-zone generator, and the dead-zone time is configurable
- Supports 4 groups of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Supports 8 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

3.10.6 General Purpose ADC (GPADC)

- 12-bit Resolution and 7-bit effective SAR type A/D converter
- 9-channel multiplexer for R128-S1 and R128-S2
  - 7 channels external GPADC: ADC0-ADC6
  - 2 channels internal ADC: ADC8, ADC12
- 10-channel multiplexer for R128-S3
  - 8 channels external GPADC: ADC0-ADC7
  - 2 channels internal ADC: ADC8, ADC12
- The ADC8 is used for VBAT voltage detection and the ADC12 is used for temperature sensor
- 64 FIFO depth of data register
- Power Supply Voltage: 2.5V, Analog Input Range: 0 to 2V
- Maximum Sampling frequency: 1 MHz

- Support self-calibration
- Support data compare and interrupt
- Support four operation modes
  - Single conversion mode
  - Single-cycle conversion mode
  - Continuous conversion mode
  - Outbreak conversion mode

3.10.7 CIR Receiver (CIR_RX)

- Supports CIR remote control receiver
- Supports NEC IR protocol
- 64x8 bits RX FIFO for data buffer
- Programmable RX FIFO thresholds
- Supports interrupt
- Sample clock up to 1 MHz

3.10.8 CIR Transmitter (CIR_TX)

- Supports CIR remote control transmitter
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Supports Interrupt and DMA
- Supports handshake mode and waiting mode of DMA

3.10.9 LEDC

- Configurable LED input high-/low-level width
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- LED data transfer rate up to 800 kbit/s
- Configurable RGB display mode

3.10.10 SCR

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for completing smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card

- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- 128bits FIFO for data transmit & receive
- Supports FIFOs for receive and transmit buffers (up to 128 bits) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

3.11 Wi-Fi Subsystem

3.11.1 Wi-Fi MAC

- 802.11d - Regulatory domain operation
- 802.11e - QoS including WMM
- 802.11h - Transmit power control dynamic and frequency selection
- 802.11i - Security including WPA2 compliance
- 802.11w-Supports STA Mode with PMF, SA Query, SAE

3.11.2 Wi-Fi Baseband

- Compatible with IEEE 802.11 b/g/n standard on 2.4 GHz
- Up to 20 MHz bandwidth
- 802.11n MCS0-7 with data rate up to 72.2Mbps (BPSK, r=1/2 through 64QAM, r=5/6)
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Short Guard Interval
- Long Guard Interval
- RX antenna Diversity
- Supports RX STBC

3.11.3 Wi-Fi Radio

- Integrated 2.4GHz PA, LNA, and T/R switch
- Internal impedance matching network and harmonic filter allow chip to connect to antenna directly

- High Power Amplifier with 3~5.5V full range directly support XRADIOTECH's MPDTM technology ensure linearity tracking automatically to always keep EVM and mask within specifications
- Special Architecture and Device design to keep the reliability of PA and also deliver high output power (>25dBm)

3.12 Bluetooth Subsystem

- BLE V5.0
  - Bluetooth 5.0 Dual Mode complies with V2.1/4.0/4.2/5.0
  - Supports GFSK,π/4 DQPSK and 8DPSK modulation
  - Data rates support: 125Kbps, 500Kbps, 1Mbps, 2Mbps
  - supports long range
  - TRNG generator
  - AES-128 data encryption with ECB and CCM mode
  - Supports advertising extension
  - Packet assembly and disassembly
  - Data Whitening and De-whitening
  - Data CRC generation and checking
  - Packet filtering based on filter policies (white and resolving lists)
  - Private address generation and Accelerate address resolution
  - Access address generation and matching
  - Frequency hopping and channel mapping
  - RSSI Reporting to host
- BR/EDR
  - Adaptive Frequency Hopping
  - SCO and eSCO support
  - 1, 3 and 5 slots all packet types support
  - Transcoders for A-law, μ-law and CVSD voice over air
  - Supports piconet
  - Secure simple pairing
  - Supports sniff/low power mode
- Transmit Power: -20 dBm (0.01 mW) to +10 dBm (10 mW)
- Receiver Sensitivity:
  - -95.0 dBm@BR
  - -98 dBm@BLE 1 Mbit/s
  - -105 dBm@BLE S = 8

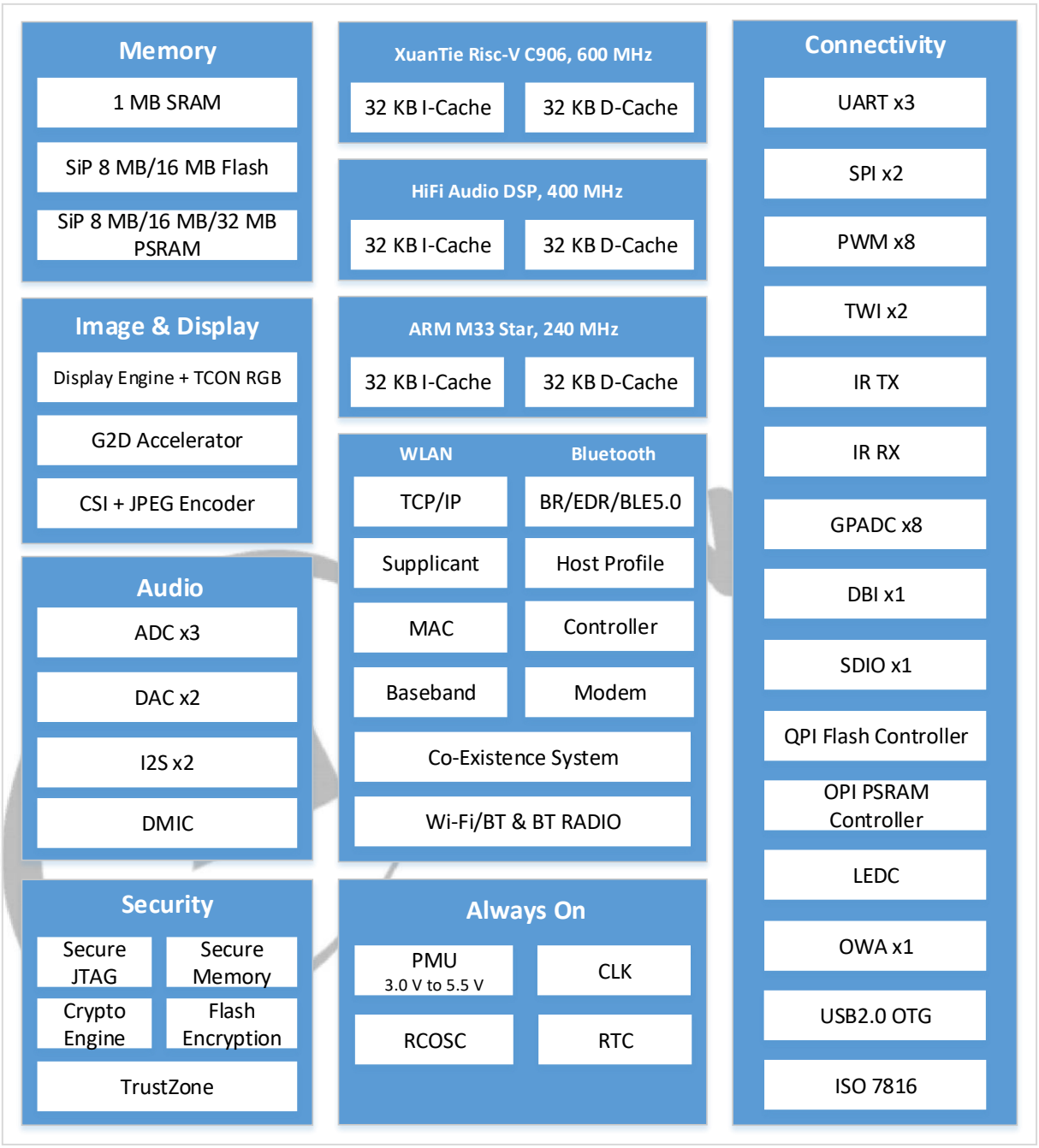
3.13 Package

QFN80, 0.35mm pitch, 8mm x 8mm body

4 Block Diagram

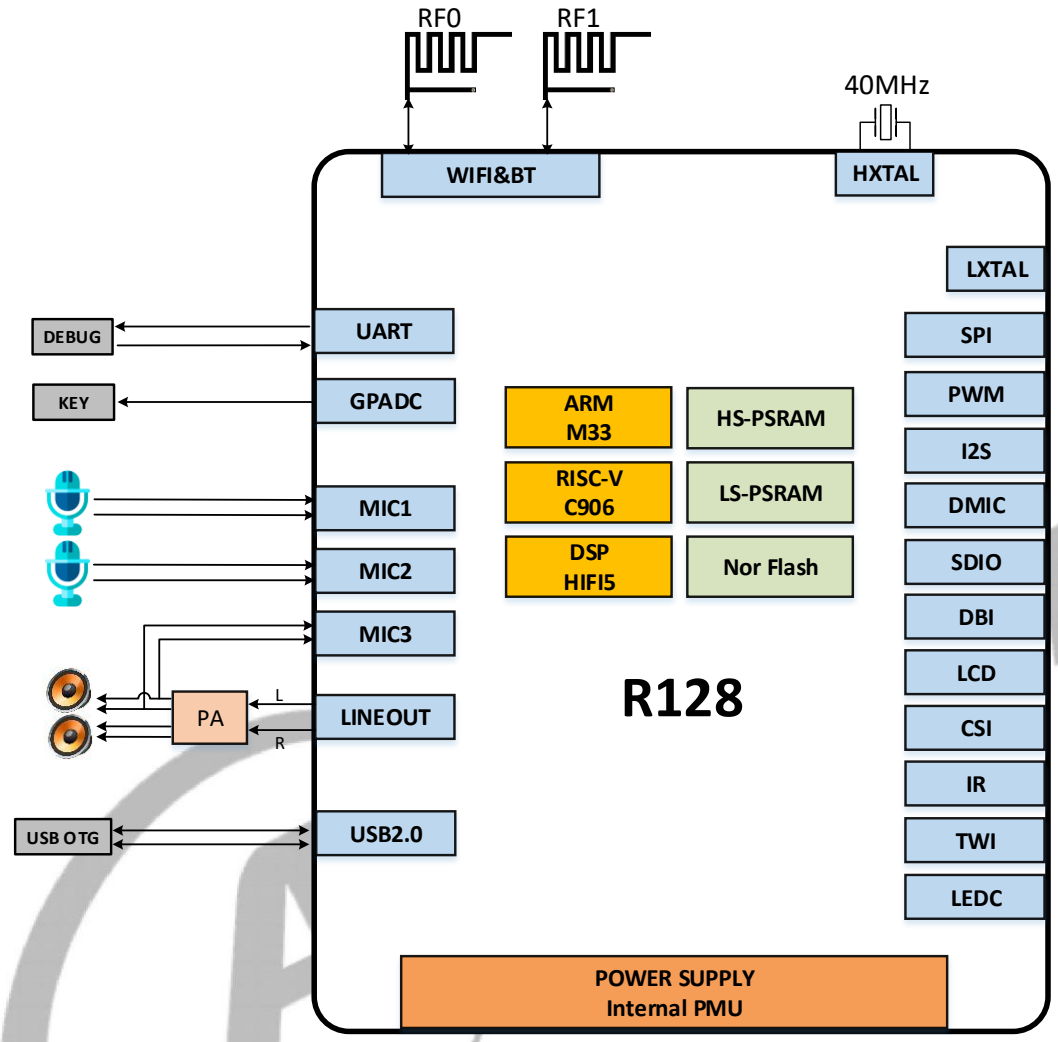
The following figure shows the system block diagram of the R128.

Figure 4-1. R128 System Block Diagram



The following figure shows the intelligent white goods solution of the R128.

Figure 4-2. R128 Intelligent White Goods Solution



NOTE

- 8 MB PSRAM in R128-S1
- 16 MB PSRAM in R128-S2
- 32 MB PSRAM in R128-S3

5 Pin Description

5.1 Pin Quantity

The following table lists the pin quantity of the R128.

Table 5-1 Pin Quantity

Pin Type	Quantity
I/O	57
Power	22
Ground	1
Total	80

5.2 Pin Characteristics

5.2.1 R128-S1 & R128-S2

The following table lists the characteristics of the R128-S1 and R128-S2 pins from the following seven aspects.

[1].Ball#: Package ball numbers associated with each signals.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction.

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

[4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

[6].Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.

[7].Power Supply: The voltage supply for the terminal's IO buffers.

Table 5-2 Pin Characteristics of R128-S1 and R128-S2

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
GPIOA[2]						
65	PA0	I/O	Z	PU/PD	4	VCC-IO2
66	PA1/FEL0	I/O	Z	PU/PD	4	VCC-IO2
67	PA2/FEL1	I/O	Z	PU/PD	4	VCC-IO2
68	PA3	I/O	Z	PU/PD	4	VCC-IO2
69	PA4	I/O	Z	PU/PD	4	VCC-IO2
70	PA5	I/O	Z	PU/PD	4	VCC-IO2
72	PA6	I/O	Z	PU/PD	4	VCC-IO2
73	PA7	I/O	Z	PU/PD	4	VCC-IO2
74	PA8	I/O	Z	PU/PD	4	VCC-IO2
71	PA9	I/O	Z	PU/PD	4	VCC-IO2
75	PA10	I/O	Z	PU/PD	4	VCC-IO2
5	PA11/WUPIO0	I/O	Z	PU/PD	4	VCC-IO2
6	PA12/WUPIO1	I/O	Z	PU/PD	4	VCC-IO2
7	PA13/WUPIO2	I/O	Z	PU/PD	4	VCC-IO2
12	PA14/WUPIO3	I/O	Z	PU/PD	4	VCC-IO2
30	PA15	I/O	Z	PU/PD	4	VCC-IO1
28	PA16	I/O	Z	PU/PD	4	VCC-IO1
29	PA17	I/O	Z	PU/PD	4	VCC-IO1
8	PA18/WUPIO4	I/O	Z	PU/PD	4	VCC-IO2
9	PA19/WUPIO5	I/O	Z	PU/PD	4	VCC-IO2
10	PA20/WUPIO6	I/O	Z	PU/PD	4	VCC-IO2
11	PA21/WUPIO7	I/O	Z	PU/PD	4	VCC-IO2
13	PA22/WUPIO8	I/O	Z	PU/PD	4	VCC-IO2
14	PA23/WUPIO9	I/O	Z	PU/PD	4	VCC-IO2
35	PA24	I/O	Z	PU/PD	4	VCC-IO1
34	PA25	I/O	Z	PU/PD	4	VCC-IO1
32	PA26	I/O	Z	PU/PD	4	VCC-IO1
31	PA27	I/O	Z	PU/PD	4	VCC-IO1
36	PA28	I/O	Z	PU/PD	4	VCC-IO1
33	PA29	I/O	Z	PU/PD	4	VCC-IO1
GPIOB[2]						
42	PB0/ADC0	I/O	Z	PU/PD	4	VCC-IO1
41	PB1/ADC1	I/O	Z	PU/PD	4	VCC-IO1

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
38	PB2/ADC2	I/O	Z	PU/PD	4	VCC-IO1
37	PB3/ADC3	I/O	Z	PU/PD	4	VCC-IO1
43	PB4/ADC4	I/O	Z	PU/PD	4	VCC-IO1
39	PB14/ADC6	I/O	Z	PU/PD	4	VCC-IO1
40	PB15/ADC7	I/O	Z	PU/PD	4	VCC-IO1
HS-PSRAM PHY IO						
27	VDD12-PSM	P	NA	NA	NA	VDD12-PSM VDD18-PSM1
RF0						
79	ANT0	A	Z	NA	NA	VCC18-ANA0
78	VCC33-RFPA0	P	NA	NA	NA	NA
77	VCC18-TX0	P	NA	NA	NA	NA
1, 80	VCC18-ANA0	P	NA	NA	NA	NA
RF1						
63	ANT1	A	Z	NA	NA	VCC18-ANA1
62	VCC33-RFPA1	P	NA	NA	NA	NA
61	VCC18-TX1	P	NA	NA	NA	NA
64	VCC18-ANA1	P	NA	NA	NA	NA
PMU						
20	VIN-VBAT	P	NA	NA	NA	NA
16	VDD-RTC	P	NA	NA	NA	NA
76	VDD-AON	P	NA	NA	NA	NA
15	VDD-DSP	P	NA	NA	NA	NA
21	LX	P	NA	NA	NA	NA
17	EXT-LDO33	P	NA	NA	NA	NA
22	VDD-SENSE	P	NA	NA	NA	NA
26, 44	VDD-SYS	P	NA	NA	NA	NA
Reset[3]						
18	CHIP-PWD	I	PD	NA	NA	VIN-VBAT
USB						
23	VCC33-USB	P	NA	NA	NA	VCC33-USB
24	USB-DM[4]	A	Z	NA	NA	VCC33-USB
25	USB-DP[4]	A	Z	NA	NA	VCC33-USB
Audio Codec						
46	MBIAS	AO	NA	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
47	MICIN1P(5)	A	Z	NA	NA	AVCC
48	MICIN1N(5)	A	Z	NA	NA	AVCC
49	MICIN2P(5)	A	Z	NA	NA	AVCC
50	MICIN2N(5)	A	Z	NA	NA	AVCC
51	MICIN3P(5)	A	Z	NA	NA	AVCC
52	MICIN3N(5)	A	Z	NA	NA	AVCC
53	VRA1(6)	A	Z	NA	NA	AVCC
54	VRA2(6)	A	Z	NA	NA	AVCC
55	AGND	G	NA	NA	NA	AVCC
56	AVCC	P	NA	NA	NA	AVCC
60	LOUTRN	A	Z	NA	NA	AVCC
59	LOUTRP	A	Z	NA	NA	AVCC
58	LOUTLP	A	Z	NA	NA	AVCC
57	LOUTLN	A	Z	NA	NA	AVCC
Clock						
6	LXTAL-IN	I/O	Z	PU/PD	4	VCC-IO2
7	LXTAL-OUT	I/O	Z	PU/PD	4	VCC-IO2
3	HXTAL-IN	A	Z	NA	NA	VCC18-ANA0
2	HXTAL-OUT	A	Z	NA	NA	VCC18-ANA0
Power (specifies only power sources irrelevant to the inner PMU module)						
45	VCC-IO1	P	NA	NA	NA	VCC-IO1
4	VCC-IO2	P	NA	NA	NA	VCC-IO2
NC						
19	NC	NA	NA	NA	NA	NA

(1) NA: no application.

(2) If all IOs of a GPIO port are unused, we suggest that the GPIO port has normal power supply, all IOs shall be floated, and the corresponding register of all IOs can be set to Disable.

(3) RESET needs ESD protection and is suggested to connect to an external pull-up resistor.

(4) The differential characteristics impedance of each pair of differential signals (USB-DP, USB-DM) must be within (90Ω±10%).

(5) MICIN[3:1]P/[3:1]N is analog differential input signals that shall be far away from interference signals.

(6) The external capacitors of VRA1, VRA2 shall be placed near the R128 chip, and in order to reduce loop area, the negative terminals of these capacitors shall be placed near AGND.

For details about schematic diagram and PCB design recommendations, see the *Allwinner R128 Hardware Design Guide*.

5.2.2 R128-S3

The following table lists the characteristics of the R128-S3 pins from the following seven aspects.

[1] Ball#: Package ball numbers associated with each signals.

[2] Pin Name: The name of the package pin.

[3] Type: Denotes the signal direction.

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

[4] Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5] Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

[6] Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.

[7] Power Supply: The voltage supply for the terminal's IO buffers.

Table 5-3 Pin Characteristics of R128-S3

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
GPIOA[(2)]						
65	PA0	I/O	Z	PU/PD	4	VCC-IO2
66	PA1/FEL0	I/O	Z	PU/PD	4	VCC-IO2
67	PA2/FEL1	I/O	Z	PU/PD	4	VCC-IO2
68	PA3	I/O	Z	PU/PD	4	VCC-IO2
69	PA4	I/O	Z	PU/PD	4	VCC-IO2
70	PA5	I/O	Z	PU/PD	4	VCC-IO2
72	PA6	I/O	Z	PU/PD	4	VCC-IO2
73	PA7	I/O	Z	PU/PD	4	VCC-IO2
74	PA8	I/O	Z	PU/PD	4	VCC-IO2
71	PA9	I/O	Z	PU/PD	4	VCC-IO2
75	PA10	I/O	Z	PU/PD	4	VCC-IO2

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
5	PA11/WUPIO0	I/O	Z	PU/PD	4	VCC-IO2
6	PA12/WUPIO1	I/O	Z	PU/PD	4	VCC-IO2
7	PA13/WUPIO2	I/O	Z	PU/PD	4	VCC-IO2
12	PA14/WUPIO3	I/O	Z	PU/PD	4	VCC-IO2
29	PA15	I/O	Z	PU/PD	4	VCC-IO1
27	PA16	I/O	Z	PU/PD	4	VCC-IO1
28	PA17	I/O	Z	PU/PD	4	VCC-IO1
8	PA18/WUPIO4	I/O	Z	PU/PD	4	VCC-IO2
9	PA19/WUPIO5	I/O	Z	PU/PD	4	VCC-IO2
10	PA20/WUPIO6	I/O	Z	PU/PD	4	VCC-IO2
11	PA21/WUPIO7	I/O	Z	PU/PD	4	VCC-IO2
13	PA22/WUPIO8	I/O	Z	PU/PD	4	VCC-IO2
14	PA23/WUPIO9	I/O	Z	PU/PD	4	VCC-IO2
34	PA24	I/O	Z	PU/PD	4	VCC-IO1
33	PA25	I/O	Z	PU/PD	4	VCC-IO1
31	PA26	I/O	Z	PU/PD	4	VCC-IO1
30	PA27	I/O	Z	PU/PD	4	VCC-IO1
35	PA28	I/O	Z	PU/PD	4	VCC-IO1
32	PA29	I/O	Z	PU/PD	4	VCC-IO1
GPIOB[2]						
43	PB0/ADC0	I/O	Z	PU/PD	4	VCC-IO1
44	PB1/ADC1	I/O	Z	PU/PD	4	VCC-IO1
38	PB2/ADC2	I/O	Z	PU/PD	4	VCC-IO1
37	PB3/ADC3	I/O	Z	PU/PD	4	VCC-IO1
45	PB4/ADC4	I/O	Z	PU/PD	4	VCC-IO1
40	PB5/ADC5	I/O	Z	PU/PD	4	VCC-IO1
39	PB6	I/O	Z	PU/PD	4	VCC-IO1
36	PB7	I/O	Z	PU/PD	4	VCC-IO1
41	PB14/ADC6	I/O	Z	PU/PD	4	VCC-IO1
42	PB15/ADC7	I/O	Z	PU/PD	4	VCC-IO1
HS-PSRAM PHY IO						
26	VDD12-PSM	P	NA[1]	NA	NA	NA
RF0						
79	ANT0	A	Z	NA	NA	VCC18-ANA0
78	VCC33-RFPA0	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
77	VCC18-TX0	P	NA	NA	NA	NA
80, 1	VCC18-ANA0	P	NA	NA	NA	NA
RF1						
63	ANT1	A	Z	NA	NA	VCC18-ANA1
62	VCC33-RFPA1	P	NA	NA	NA	NA
61	VCC18-TX1	P	NA	NA	NA	NA
64	VCC18-ANA1	P	NA	NA	NA	NA
PMU						
19	VIN-VBAT	P	NA	NA	NA	NA
16	VDD-RTC	P	NA	NA	NA	NA
76	VDD-AON	P	NA	NA	NA	NA
24	VDD-SYS	P	NA	NA	NA	NA
15	VDD-DSP	P	NA	NA	NA	NA
20	LX	P	NA	NA	NA	NA
21	VDD-SENSE	P	NA	NA	NA	NA
17	EXT-LDO33	P	NA	NA	NA	NA
46	VDD-SYS	P	NA	NA	NA	VDD-SYS
Reset(3)						
18	CHIP-PWD	I	PD	NA	NA	VIN-VBAT
USB						
22	VCC33-USB	P	NA	NA	NA	VCC33-USB
23	USB-DM(4)	A	Z	NA	NA	VCC33-USB
24	USB-DP(4)	A	Z	NA	NA	VCC33-USB
Audio Codec						
49	MICIN1P(5)	A	Z	NA	NA	AVCC
50	MICIN1N(5)	A	Z	NA	NA	AVCC
51	MICIN2P(5)	A	Z	NA	NA	AVCC
52	MICIN2N(5)	A	Z	NA	NA	AVCC
53	MICIN3P(5)	A	Z	NA	NA	AVCC
54	MICIN3N(5)	A	Z	NA	NA	AVCC
48	MBIAS	AO	Z	NA	NA	AVCC
55	VRA1(6)	A	Z	NA	NA	AVCC
56	VRA2(6)	A	Z	NA	NA	AVCC
60	LOUTLP	A	Z	NA	NA	AVCC
59	LOUTLN	A	Z	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
58	AVCC	P	NA	NA	NA	AVCC
57	AGND	G	NA	NA	NA	AVCC
Clock						
6	LXTAL-IN	I/O	Z	PU/PD	4	VCC-IO2
7	LXTAL-OUT	I/O	Z	PU/PD	4	VCC-IO2
3	HXTAL-IN	A	Z	NA	NA	VCC18-ANA0
2	HXTAL-OUT	A	Z	NA	NA	VCC18-ANA0
Power (specifies only power sources irrelevant to the inner PMU module)						
47	VCC-IO1	P	NA	NA	NA	VCC-IO1
4	VCC-IO2	P	NA	NA	NA	VCC-IO2

(1) NA: no application.

(2) If all IOs of a GPIO port are unused, we suggest that the GPIO port has normal power supply, all IOs shall be floated, and the corresponding register of all IOs can be set to Disable.

(3) RESET needs ESD protection and is suggested to connect to an external pull-up resistor.

(4) The differential characteristics impedance of each pair of differential signals (USB-DP, USB-DM) must be within (90Ω±10%).

(5) MICIN[3:1]P/[3:1]N is analog differential input signals that shall be far away from interference signals.

(6) The external capacitors of VRA1, VRA2 shall be placed near the R128 chip, and in order to reduce loop area, the negative terminals of these capacitors shall be placed near AGND.

For details about schematic diagram and PCB design recommendations, see the *Allwinner R128 Hardware Design Guide*.

5.3 GPIO Multiplex Function

NOTE

For each GPIO, Function0 is input function; Function1 is output function.

The following table provides a description of the R128 GPIO multiplex function.

Table 5-4 GPIO Multiplex Function of R128

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PA0	GPIOA	I/O	IR_RX		PWM7	TWI0_SCL	TWI1_SCL	LCD_VSYNC	LCD_D2	PA_EINT0
PA1/FEL0		I/O	IR_TX	FEM_CTRL1	IR_RX	TWI0_SDA	TWI1_SDA		LCD_D3	PA_EINT1
PA2/FEL1		I/O	SPI1_CS<DBI_CSX>	DMIC_DATA0	JTAG_RV_TMS	SDC_DATA1	I2S_LRCLK	JTAG_DSP_TMS	LCD_D4	PA_EINT2
PA3		I/O	SPI1_CLK<DBI_SCLK>	DMIC_DATA1	JTAG_RV_TDI	SDC_DATA0	I2S_BCLK	JTAG_DSP_TDI	LCD_D5	PA_EINT3
PA4		I/O	SPI1_MOSI<DBI_SDO>	DMIC_DATA2	UART0_TX	SDC_CLK	I2S_DIN	PWM1	LCD_D6	PA_EINT4
PA5		I/O	SPI1_MISO<DBI_SDI/DBI_TE/DBI_DCX>	DMIC_DATA3	JTAG_RV_TDO	SDC_CMD	I2S_DOUT	JTAG_DSP_TDO	LCD_D7	PA_EINT5
PA6		I/O	SPI1_HOLD<DBI_DCX/DBI_WRX>	DMIC_CLK	UART0_RX	SDC_DATA3	I2S_MCLK	LCD_CLK	LCD_D14	PA_EINT6
PA7		I/O	SPI1_WP<DBI_TE>	OWA_IN	JTAG_RV_TCK	SDC_DATA2	JTAG_DSP_TCK	LCD_HSYNC	LCD_D13	PA_EINT7
PA8		I/O	UART0_RX	OWA_OUT	PWM0	OWA_IN	TWI1_SCL	FEM_CTRL2	LCD_D12	PA_EINT8
PA9		I/O	UART0_TX		PWM1	LEDC	TWI1_SDA	LCD_DE	LCD_D15	PA_EINT9
PA10		I/O	UART2_RTS	IR_RX	PWM2	TWI1_SCL			LCD_D11	PA_EINT10
PA11/WUPIO0		I/O	UART2_CTS	IR_TX	PWM3	TWI1_SDA	32KOSCO	FEM_CTRL1	LCD_D10	PA_EINT11
PA12/WUPIO1 / LXTAL_IN		I/O	UART2_TX	TWI0_SCL	UART2_RTS	IR_RX	SPI1_CS<DBI_CSX>	LCD_VSYNC	LCD_D18	PA_EINT12
PA13/WUPIO2 / LXTAL_OUT		I/O	UART2_RX	TWI0_SDA	UART2_CTS	IR_TX	SPI1_CLK<DBI_SCLK>	LEDC	LCD_D19	PA_EINT13
PA14/WUPIO3		I/O	PWM0	SPI1_MOSI<DBI_SDO>	UART2_RX	SIM_DATA	UART1_RTS	TWI1_SCL	LCD_D20	PA_EINT14
PA15		I/O	PWM1	SPI1_HOLD<DBI_DCX/DBI_WRX>	UART2_TX	SIM_CLK	UART1_CTS	TWI1_SDA	LCD_D21	PA_EINT15
PA16		I/O	TWI0_SCL	OWA_IN	TWI1_SCL	UART0_TX	IR_RX	UART2_TX	SWD_TMS	PA_EINT16
PA17		I/O	TWI0_SDA	OWA_OUT	TWI1_SDA	UART0_RX	IR_TX	UART2_RX	SWD_TCK	PA_EINT17
PA18/WUPIO4		I/O	I2S_MCLK	IR_RX	IR_TX		SPI1_MOSI<DBI_SDO>	NCSI_HSYNC	LCD_VSYNC	PA_EINT18
PA19/WUPIO5		I/O	I2S_LRCLK	UART1_RTS	PWM4	DMIC_DATA0	SPI1_HOLD<DBI_DCX/DBI_WRX>	NCSI_VSYNC	LCD_HSYNC	PA_EINT19
PA20/WUPIO6		I/O	I2S_BCLK	UART1_CTS	PWM5	DMIC_DATA1	SPI1_WP<DBI_TE>	NCSI_PCLK	LCD_CLK	PA_EINT20
PA21/WUPIO7		I/O	I2S_DIN	UART1_RX	PWM6	DMIC_DATA2	SPI1_MISO<DBI_SDI/DBI_TE/DBI_DCX>	NCSI_MCLK	LCD_DE	PA_EINT21
PA22/WUPIO8		I/O	I2S_DOUT	UART1_TX	PWM7	DMIC_DATA3		LEDC	NCSI_D0	PA_EINT22
PA23/WUPIO9		I/O	I2S_MCLK	DCXO_PUP_OUT	SWD_SWO	DMIC_CLK	TWI0_SCL	PWM0	NCSI_D1	PA_EINT23
PA24		I/O	SDC_DATA3	SPI0_MISO	PWM4	UART2_RX	TWI0_SDA	SIM_DATA	NCSI_D6	PA_EINT24
PA25		I/O	SDC_CMD	SPI0_WP	PWM5	JTAG_M33_TDO	JTAG_RV_TDO	SIM_CLK	NCSI_D5	PA_EINT25
PA26		I/O	SDC_DATA0	SPI0_CLK	PWM6	JTAG_M33_TDI	JTAG_RV_TDI	LEDC	NCSI_D3	PA_EINT26

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function14
PA27		I/O	SDC_DATA1	SPI0_HOLD	PWM7	JTAG_M33_TMS	JTAG_RV_TMS	SIM_DET	NCSI_D2	PA_EINT27
PA28		I/O	SDC_DATA2	SPI0_CS	FEM_CTRL1	JTAG_M33_TCK	JTAG_RV_TCK	SIM_RST	NCSI_D7	PA_EINT28
PA29		I/O	SDC_CLK	SPI0_MOSI	FEM_CTRL2	UART2_TX	PWM1	LEDC	NCSI_D4	PA_EINT29
NOTE: LXTAL is the low-frequency clock exclusively for the RTC domain.										
For R128_S1/S2										
PB0/ADC0	GPIOB	I/O	UART0_TX	TWI1_SCL	IR_RX	UART2_RTS	PWM2		NCSI_HSYNC	PB_EINT0
PB1/ADC1		I/O	UART0_RX	TWI1_SDA	IR_TX	UART2_CTS	PWM3		NCSI_VSYNC	PB_EINT1
PB2/ADC2		I/O	PWM2	SPI1_MISO<DBI_SDI/DBI_TE/DBI_DCX>	TWI1_SCL	SIM_RST	UART1_RX	UART2_RTS	LCD_D23	PB_EINT2
PB3/ADC3		I/O	PWM3	SPI1_WP<DBI_TE>	TWI1_SDA	SIM_DET	UART1_TX	UART2_CTS	LCD_D22	PB_EINT3
PB4/ADC4		I/O				FLASH CS	PWM4		LCD_DE	PB_EINT4
PB14/ADC6		I/O	UART1_TX			FLASH WP/IO2			NCSI_PCLK	PB_EINT14
PB15/ADC7		I/O	UART1_RX			FLASH MISO/IO1	PWM0		NCSI_MCLK	PB_EINT15
For R128_S3										
PB0/ADC0	GPIOB	I/O	UART0_TX	TWI1_SCL	IR_RX	UART2_RTS	PWM2		NCSI_HSYNC	PB_EINT0
PB1/ADC1		I/O	UART0_RX	TWI1_SDA	IR_TX	UART2_CTS	PWM3		NCSI_VSYNC	PB_EINT1
PB2/ADC2		I/O	PWM2	SPI1_MISO<DBI_SDI/DBI_TE/DBI_DCX>	TWI1_SCL	SIM_RST	UART1_RX	UART2_RTS	LCD_D23	PB_EINT2
PB3/ADC3		I/O	PWM3	SPI1_WP<DBI_TE>	TWI1_SDA	SIM_DET	UART1_TX	UART2_CTS	LCD_D22	PB_EINT3
PB4/ADC4		I/O	UART1_RTS	SDC_CLK	SPI0_CS	FLASH CS	PWM4		LCD_DE	PB_EINT4
PB5/ADC5		I/O	UART1_CTS	SDC_DATA1	SPI0_MOSI	FLASH MOSI/IO0	PWM5			PB_EINT5
PB6		I/O	UART1_TX	SDC_DATA0	SPI0_CLK	FLASH CLK	PWM6			PB_EINT6
PB7		I/O	UART1_RX	SDC_DATA3	SPI0_HOLD	FLASH HOLD/IO3	PWM7			PB_EINT7
PB14/ADC6		I/O	UART1_TX	SDC_DATA2	SPI0_WP	FLASH WP/IO2			NCSI_PCLK	PB_EINT14
PB15/ADC7		I/O	UART1_RX	SDC_CMD	SPI0_MISO	FLASH MISO/IO1	PWM0		NCSI_MCLK	PB_EINT15

5.4 Detailed Signal Description

5.4.1 R128-S1 & R128-S2

The following table shows the detailed function description of every signal based on the different interface of R128-S1 & R128-S2.

[1].Signal Name: The name of every signal.

[2].Description: The detailed function description of every signal.

[3].Type: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

Table 5-5 Detailed Signal Description of R128-S1 & R128-S2

Signal Name[1]	Description[2]	Type[3]
HS-PSRAM PHY IO		
VDD12-PSM	Power Supply of PSRAM	P
RF0		
ANT0	Antenna of RF0	A
FEM-CTRL1	Front End Module Control, TX-EN	I/O
FEM-CTRL2	Front End Module Control, RX-EN	I/O
VCC33-RFPA0	Power Supply of RF0 Input	P
VCC18-TX0	Power Supply of RF0 Input	P
VCC18-ANA0	Power Supply of RF0 Analog/RF Input	P
Note: HXTAL is the system clock of the whole chip, which includes the clocks required by the RF module and other modules.		
RF1		
ANT1	Antenna of RF1	A
FEM-CTRL1	Front End Module Control, TX-EN	I/O
FEM-CTRL2	Front End Module Control, RX-EN	I/O

Signal Name[1]	Description[2]	Type[3]
VCC33-RFPA1	Power Supply of RF1 Input	P
VDD18-TX1	Power Supply of RF1 Input	P
VCC18-ANA1	Power Supply of RF1 Analog/RF Input	P
PMU		
VIN-VBAT	VBAT System Power Input	P
VDD-RTC	RTC Power	P
VDD-AON	VDD-AON Power Supply of AON Domain	P
VDD-DSP	VDD-DSP Power Supply of DSP	P
LX	Power Supply of DCDC Output	P
EXT-LDO33	VDD-3V3 Power Output of 3.3V	P
VDD-SENSE	DCDC Feedback and Power	P
VDD-SYS	Power Supply for System	P
RESET		
CHIP-PWD	System Power on Reset	I
USB		
VCC33-USB	Power Supply of USB	P
USB-DM	USB Data Signal DM	A I/O
USB-DP	USB Data Signal DP	A I/O
Audio Codec		
MBIAS	Master Analog Microphone Bias Voltage Output	AO
MICIN1P	Microphone Positive Input 1	AI
MICIN1N	Microphone Negative Input 1	AI
MICIN2P	Microphone Positive Input 2	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN3P	Microphone Positive Input 3	AI
MICIN3N	Microphone Negative Input 3	AI
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
AGND	Analog Ground	G
AVCC	Power Supply for Analog Part	P
LOUTRN	Stereo Lineout Output Right Negative Channel	AO
LOUTRP	Stereo Lineout Output Right Positive Channel	AO
LOUTLP	Stereo Lineout Output Left Positive Channel	AO
LOUTLN	Stereo Lineout Output Left Negative Channel	AO
Power		
VCC-IO1	Power Supply of IO1 Domain	P

Signal Name[1]	Description[2]	Type[3]
VCC-IO2	Power Supply of IO2 Domain	P
CIR Receiver		
IR-RX	Consumer Infrared Receiver	I/O
CIR Transmitter		
IR-TX	Consumer Infrared Transmitter	I/O
SPI		
SPI0-CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active	I/O
SPI0-HOLD	SPI0 Hold Signal	I/O
SPI1-CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-HOLD	SPI1 Hold Signal	I/O
SPI1-WP	SPI1 Write Protect, Low Active	I/O
SPI_DBI		
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge	I/O
DBI-DCX	DCX pin is the select output signal of data and command DCX = 0: register command DCX = 1: data or parameter	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable. It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
UART		
UART0-RX	UART0 Data Receive	I/O

Signal Name[1]	Description[2]	Type[3]
UART0-TX	UART0 Data Transmit	I/O
UART1-RTS	UART1 Data Request to Send	I/O
UART1-CTS	UART1 Data Clear to Send	I/O
UART1-RX	UART1 Data Receive	I/O
UART1-TX	UART1 Data Transmit	I/O
UART2-RTS	UART2 Data Request to Send	I/O
UART2-CTS	UART2 Data Clear to Send	I/O
UART2-RX	UART2 Data Receive	I/O
UART2-TX	UART2 Data Transmit	I/O
PWM		
PWM[7:0]	Pulse Width Modulation Output Channel0	I/O
TWI		
TWI0-SCL	TWI0 Serial CLOCK Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCL	TWI1 Serial CLOCK Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
I2S		
I2S-LRCLK	I2S sample rate clock	I/O
I2S-BCLK	I2S Bit Rate Clock	I/O
I2S-DIN	I2S Serial Data Input	I/O
I2S-DOUT	I2S Serial Data Input	I/O
I2S-MCLK	I2S Master Clock	I/O
SDIO		
SDC-CMD	SDIO Command Signal	I/O
SDC-DATA[3:0]	SDIO data Signal	I/O
SDC-CLK	SDIO clock Signal	I/O
Flash		
FLASH WP/IO2	Flash Write Protect Signal	I/O
FLASH MISO/IO1	Flash Slave Output/Master Input Signal	I/O
FLASH CS	Flash Chip Select Signal	I/O
SDC-CLK	SDIO clock Signal	I/O
DMIC		
DMIC-DATA[3:0]	Digital MIC Data input signal	I/O
DMIC-CLK	Digital Microphone Clock Output	I/O
OWA		
OWA-IN	One Wire Audio Input	I/O

Signal Name[1]	Description[2]	Type[3]
OWA-OUT	One Wire Audio Output	I/O
GPADC		
GPADC[7:0]	General Purpose ADC Input Channel	AI
Wake-up IO		
WUPIO0	Wake-up input/output 0	I/O
WUPIO1	Wake-up input/output 1	I/O
WUPIO2	Wake-up input/output 2	I/O
WUPIO3	Wake-up input/output 3	I/O
WUPIO4	Wake-up input/output 4	I/O
WUPIO5	Wake-up input/output 5	I/O
WUPIO6	Wake-up input/output 6	I/O
WUPIO7	Wake-up input/output 7	I/O
WUPIO8	Wake-up input/output 8	I/O
WUPIO9	Wake-up input/output 9	I/O
JTAG		
JTAG-RV-TMS	RISC-V JTAG TMS signal	I/O
JTAG-DSP-TMS	DSP JTAG TMS signal	I/O
JTAG-RV-TDI	RISC-V JTAG TDI signal	I/O
JTAG-DSP-TDI	DSP JTAG TDI signal	I/O
JTAG-RV-TDO	RISC-V JTAG TDO signal	I/O
JTAG-DSP-TDO	DSP JTAG TDO signal	I/O
JTAG-RV-TCK	RISC-V JTAG TCK signal	I/O
JTAG-DSP-TCK	DSP JTAG TDO signal	I/O
JTAG-M-TDO	ARM M33 JTAG TDO signal	I/O
JTAG-M-TDI	ARM M33 JTAG TDI signal	I/O
JTAG-M-TMS	ARM M33 JTAG TMS signal	I/O
JTAG-M-TCK	ARM M33 JTAG TCK signal	I/O
SWD		
SWD-SWO	Serial Wire Debug data signal	I/O
SWD-TMS	Serial Wire Debug TMS signal	I/O
SWD-TCK	Serial Wire Debug clock signal	I/O
Smart Card		
SIM-DATA	Smart Card data signal	I/O
SIM-CLK	Smart Card clock signal	I/O
SIM-DET	Smart Card detect signal	I/O
SIM-RST	Smart Card reset signal	I/O

Signal Name[1]	Description[2]	Type[3]
DCXO		
DCXO-PUP-OUT	Power Control of External DCDC	I/O
LEDC		
LEDC	Intelligent control LED signal output	I/O
CLOCK		
LXTAL-IN	32KHz Crystal Input	AI
LXTAL-OUT	32KHz Crystal Output	AO
HXTAL-IN	26/40MHz Crystal Input	AI
HXTAL-OUT	26/40MHz Crystal Output	AO
LCD		
LCD-VSYNC	LCD Vertical Sync	I/O
LCD-D[7:2]	LCD Data Output	I/O
LCD-D[15:10]	LCD Data Output	I/O
LCD-D[23:18]	LCD Data Output	I/O
LCD-CLK	LCD CLOCK	I/O
LCD-HSYNC	LCD Horizontal Sync	I/O
LCD-DE	LCD Data Output Enable	I/O
NCSI		
NCSI-HSYNC	DVP-CSI Horizontal Sync signal	I/O
NCSI-VSYNC	DVP-CSI Vertical Sync signal	I/O
NCSI-PCLK	DVP-CSI pixel clock signal	I/O
NCSI-MCLK	DVP-CSI master clock signal	I/O
NCSI-D[7:0]	DVP-CSI data signal[7:0]	I/O
Interrupt		
PA_EINT[29:0]	GPIO A Interrupt	I/O
PB_EINT[4:0]	GPIO B Interrupt	I/O
PB_EINT[15:14]	GPIO B Interrupt	I/O

5.4.2 R128-S3

The following table shows the detailed function description of every signal based on the different interface of R128-S3.

[1].**Signal Name**: The name of every signal.

[2].**Description**: The detailed function description of every signal.

[3].**Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

Table 5-6 Detailed Signal Description of R128-S3

Signal Name[1]	Description[2]	Type[3]
HS-PSRAM PHY IO		
VDD12-PSM	Power Supply of PSRAM	P
USB		
VCC33-USB	Power Supply of PSRAM	P
USB-DP	USB Data Signal DP	A I/O
USB-DM	USB Data Signal DM	A I/O
RF0		
ANT0	Antenna of RF0	A
FEM-CTRL1	Front End Module Control, TX-EN	I/O
FEM-CTRL2	Front End Module Control, RX-EN	I/O
VCC33-RFPA0	Power Supply of RF0 Input	P
VCC18-TX0	Power Supply of RF0 Input	P
VCC18-ANA0	Power Supply of RF0 Analog/RF Input	P
NOTE: HXTAL is the system clock of the whole chip, which includes the clocks required by the RF module and other modules.		
RF1		
ANT1	Antenna of RF1	A
FEM-CTRL1	Front End Module Control, TX-EN	I/O
FEM-CTRL2	Front End Module Control, RX-EN	I/O
VCC33-RFPA1	Power Supply of RF1 Input	P
VDD18-TX1	Power Supply of RF1 Input	P
VCC18-ANA1	Power Supply of RF1 Analog/RF Input	P
PMU		
VIN-VBAT	VBAT System Power Input	P
VDD-RTC	RTC Power	P
VDD-AON	VDD-AON Power Supply of AON Domain	P

Signal Name[1]	Description[2]	Type[3]
VDD-SYS	Power Supply for System	P
VDD-DSP	VDD-DSP Power Supply of DSP	P
VDD-LX	Power Supply of DCDC Output	P
VDD-SENSE	DCDC Feedback and Power	P
EXT-LDO33	VDD-3V3 Power Output of 3.3V	P
RESET		
CHIP-PWD	System Power on Reset	I
Audio Codec		
MICIN1P	Microphone Positive Input 1	AI
MICIN1N	Microphone Negative Input 1	AI
MICIN2P	Microphone Positive Input 2	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN3P	Microphone Positive Input 3	AI
MICIN3N	Microphone Negative Input 3	AI
MBIAS	Master Analog Microphone Bias Voltage Output	AO
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
LOUTLP	Stereo Lineout Output Left Positive Channel	AO
LOUTLN	Stereo Lineout Output Left Negative Channel	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
Power		
VCC-IO1	Power Supply of IO1 Domain	P
VCC-IO2	Power Supply of IO2 Domain	P
CIR Receiver		
IR-RX	Consumer Infrared Receiver	I/O
CIR Transmitter		
IR-TX	Consumer Infrared Transmitter	I/O
SPI		
SPI0-CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protect, Low Active	I/O
SPI0-HOLD	SPI0 Hold Signal	I/O
SPI1-CS	SPI1 Chip Select Signal, Low Active	I/O

Signal Name[1]	Description[2]	Type[3]
SPI1-CLK	SPI1 Clock Signal	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-HOLD	SPI1 Hold Signal	I/O
SPI1-WP	SPI1 Write Protect, Low Active	I/O
SPI_DBI		
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge	I/O
DBI-DCX	DCX pin is the select output signal of data and command DCX = 0: register command DCX = 1: data or parameter	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable. It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
UART		
UART0-RX	UART0 Data Receive	I/O
UART0-TX	UART0 Data Transmit	I/O
UART1-RTS	UART1 Data Request to Send	I/O
UART1-CTS	UART1 Data Clear to Send	I/O
UART1-RX	UART1 Data Receive	I/O
UART1-TX	UART1 Data Transmit	I/O
UART2-RTS	UART2 Data Request to Send	I/O
UART2-CTS	UART2 Data Clear to Send	I/O
UART2-RX	UART2 Data Receive	I/O
UART2-TX	UART2 Data Transmit	I/O
PWM		
PWM[7:0]	Pulse Width Modulation Output Channel0	I/O
TWI		
TWI0-SCL	TWI0 Serial CLOCK Signal	I/O

Signal Name[1]	Description[2]	Type[3]
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCL	TWI1 Serial CLOCK Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
I2S		
I2S-LRCLK	I2S sample rate clock	I/O
I2S-BCLK	I2S Bit Rate Clock	I/O
I2S-DIN	I2S Serial Data Input	I/O
I2S-DOUT	I2S Serial Data Input	I/O
I2S-MCLK	I2S Master Clock	I/O
SDIO		
SDC-CMD	SDIO Command Signal	I/O
SDC-DATA[3:0]	SDIO data Signal	I/O
SDC-CLK	SDIO clock Signal	I/O
Flash		
FLASH WP/1O2	Flash Write Protect Signal	I/O
FLASH HOLD/IO3	Flash Hold Signal	I/O
FLASH MOSI/IO0	Flash Master Output/Slave Input Signal	I/O
FLASH MISO/IO1	Flash Master Input/Slave Output Signal	I/O
FLASH CS	Flash Chip Select Signal	I/O
FLASH CLK	Flash Clock Signal	I/O
DMIC		
DMIC-DATA[3:0]	Digital MIC Data input signal	I/O
DMIC-CLK	Digital Microphone Clock Output	I/O
OWA		
OWA-IN	One Wire Audio Input	I/O
OWA-OUT	One Wire Audio Output	I/O
GPADC		
GPADC[7:0]	General Purpose ADC Input Channel	AI
Wake-up IO		
WUPIO0	Wake-up input/output 0	I/O
WUPIO1	Wake-up input/output 1	I/O
WUPIO2	Wake-up input/output 2	I/O
WUPIO3	Wake-up input/output 3	I/O
WUPIO4	Wake-up input/output 4	I/O
WUPIO5	Wake-up input/output 5	I/O
WUPIO6	Wake-up input/output 6	I/O

Signal Name[1]	Description[2]	Type[3]
WUPIO7	Wake-up input/output 7	I/O
WUPIO8	Wake-up input/output 8	I/O
WUPIO9	Wake-up input/output 9	I/O
JTAG		
JTAG-RV-TMS	RISC-V JTAG TMS signal	I/O
JTAG-DSP-TMS	DSP JTAG TMS signal	I/O
JTAG-RV-TDI	RISC-V JTAG TDI signal	I/O
JTAG-DSP-TDI	DSP JTAG TDI signal	I/O
JTAG-RV-TDO	RISC-V JTAG TDO signal	I/O
JTAG-DSP-TDO	DSP JTAG TDO signal	I/O
JTAG-RV-TCK	RISC-V JTAG TCK signal	I/O
JTAG-DSP-TCK	DSP JTAG TDO signal	I/O
JTAG-M-TDO	ARM M33 JTAG TDO signal	I/O
JTAG-M-TDI	ARM M33 JTAG TDI signal	I/O
JTAG-M-TMS	ARM M33 JTAG TMS signal	I/O
JTAG-M-TCK	ARM M33 JTAG TCK signal	I/O
SWD		
SWD-SWO	Serial Wire Debug data signal	I/O
SWD-TMS	Serial Wire Debug TMS signal	I/O
SWD-TCK	Serial Wire Debug clock signal	I/O
Smart Card		
SIM-DATA	Smart Card data signal	I/O
SIM-CLK	Smart Card clock signal	I/O
SIM-DET	Smart Card detect signal	I/O
SIM-RST	Smart Card reset signal	I/O
DCXO		
DCXO-PUP-OUT	Power Control of External DCDC	I/O
LEDC		
LEDC	Intelligent control LED signal output	I/O
CLOCK		
LXTAL-IN	32KHz Crystal Input	AI
LXTAL-OUT	32KHz Crystal Output	AO
HXTAL-IN	26/40MHz Crystal Input	AI
HXTAL-OUT	26/40MHz Crystal Output	AO
LCD		
LCD-VSYNC	LCD Vertical Sync	I/O

Signal Name[1]	Description[2]	Type[3]
LCD-D[7:2]	LCD Data Output	I/O
LCD-D[15:10]	LCD Data Output	I/O
LCD-D[23:18]	LCD Data Output	I/O
LCD-DCLK	LCD CLOCK	I/O
LCD-HSYNC	LCD Horizontal Sync	I/O
LCD-DE	LCD Data Output Enable	I/O
NCSI		
NCSI-HSYNC	DVP-CSI Horizontal Sync signal	I/O
NCSI-VSYNC	DVP-CSI Vertical Sync signal	I/O
NCSI-PCLK	DVP-CSI pixel clock signal	I/O
NCSI-MCLK	DVP-CSI master clock signal	I/O
NCSI-D[7:0]	DVP-CSI data signal[7:0]	I/O
Interrupt		
PA_EINT[29:0]	GPIO A Interrupt	I/O
PB_EINT[7:0]	GPIO B Interrupt	I/O
PB_EINT[15:14]	GPIO B Interrupt	I/O

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Once the Absolute Maximum Ratings are exceeded, damage to the device may occur. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed as below may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 6.2 *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
VIN-VBAT	Power Supply for R128 chip input		-0.3	6	V
VDD-SENSE	Internal DCDC Output Voltage		-0.3	2.16	V
LX	DCDC output to inductor		-0.3	6	V
VCC18-ANA0	Power Supply for RF Analog Part		-0.3	2.16	V
VCC18-ANA1					
VCC18-TX0	Power Supply for RF TX		-0.3	2.16	V
VCC18-TX1					
AVCC	Power supply of codec		-0.3	2.16	V
VDD-AON	Internal LDO Output Voltage for AON and HSPSRAM		-0.3	1.5	V
VDD12-PSM					
VDD-SYS	Internal LDO Output Voltage for System		-0.3	1.5	V
VDD-DSP	Internal LDO Output Voltage for DSP		-0.3	1.5	V
VDD-RTC	Internal LDO Output Voltage for RTC		-0.3	1.5	V
VCC33-RFPA0	Power Supply for RF PA		-0.3	3.96	V
VCC33-RFPA1					
EXT-LDO33	Internal LDO Output Voltage		-0.3	3.96	V
VCC-IO1	Power supply of GPIO input		-0.3	3.96	V
VCC-IO2					
VCC33-USB	USB Analog Power		-0.3	3.96	V
T_j	Working Junction Temperature		-25	110	°C
T_{stg}	Storage Temperature		-55	125	°C
V_{ESD}	Electrostatic Discharge(2)	Human Body Model(HBM) (3)	-2000	2000	V
V_{ESD}		Charged Device Model(CDM)(4)	-500	500	V

$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)	Pass
	Latch-up over-voltage performance voltage injection on each IO pin(6)	Pass

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

6.2 Recommended Operating Conditions

All R128 modules are used under the operating conditions contained in the following table.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Ta	Ambient Operating Temperature (when VDD-SYS & VDD-DSP are supplied by external power, and a heatsink is added for the chip)	-25	-	85	°C
VIN-VBAT	Power Supply for R128 chip input	3	3.8	5.5	V
VDD-SENSE	Internal DCDC Output Voltage	1.7	1.8	1.95	V
LX	DCDC output to inductor	3	3.8	5.5	V
VCC18-ANA0	Power Supply for RF Analog Part	1.7	1.8	1.95	V
VCC18-ANA1					
VCC18-TX0	Power Supply for RF TX	1.7	1.8	1.95	V
VCC18-TX1					
AVCC	Power supply of codec	1.764	1.8	1.836	V
VDD-AON	Internal LDO Output Voltage for AON and HSPSRAM	1.14	1.2	1.3	V
VDD12-PSM					
VDD-SYS	Internal LDO Output Voltage for System	1.1	1.1	1.35	V

VDD-DSP	Internal LDO Output Voltage for DSP	1.1	1.2	1.35	V
VDD-RTC	Internal LDO Output Voltage for RTC	0.6	1.2	1.35	V
VCC33-RFPA0	Power Supply for RF PA	2.97	3.3	3.63	V
VCC33-RFPA1					
EXT-LDO33	Internal LDO Output Voltage	2.97	3.3	3.63	V
VCC-IO1	Power supply of GPIO input	2.97	3.3	3.63	V
VCC-IO2	Power supply of GPIO input	2.97	3.3	3.63	V
VCC33-USB	Power supply of USB	2.97	3.3	3.63	V

(1) The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 6-1.

(2) In the hibernation status, the typical current of VDD-RTC is 0.775V.

(3) When the frequency of DSP is 400M, the VDD-DSP will be 1.2V. However, when the frequency is lowered to 274M, the VDD-DSP can be 1.1V.

6.3 DC Electrical Characteristics

The following tables summarize the DC electrical characteristics of the R128.

Table 6-3 DC Characteristics of VCC-IO=3.3V

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VCC-IO=3.3V	-	1.32	V
V_{IH}	Input High Voltage	VCC-IO=3.3V	2.06	-	V
V_{OL}	Output Low Voltage	$\|I_{OH}\|$ = 10~40 mA *	-	0.3	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 10~40 mA *	VCC-IO-0.3	-	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	35	95	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	35	95	KΩ
NOTE: * : Double for SPI/SDIO					

Table 6-4 DC Characteristics of VCC-IO=1.8V

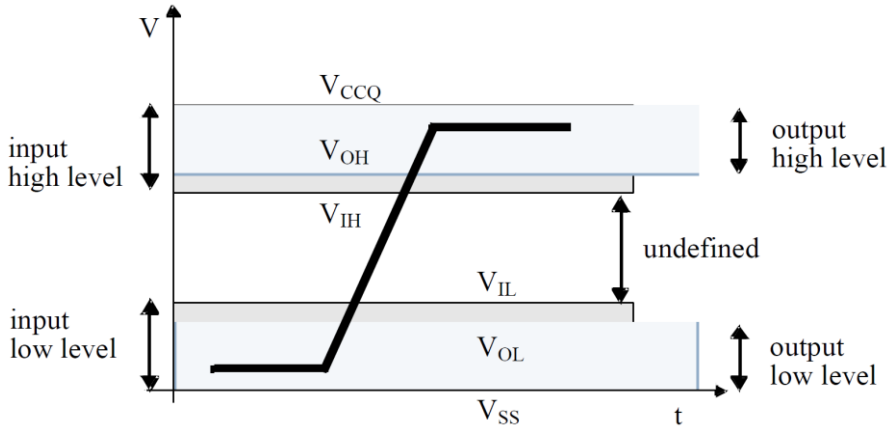
Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input Low Voltage	VCC-IO=1.8V	-	0.65	V
V_{IH}	Input High Voltage	VCC-IO=1.8V	1.18	-	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 3~12 mA *	-	0.3	V
V_{OH}	Output High Voltage	$\|I_{OL}\|$ = 3~12 mA *	VCC-IO-0.3	-	V
R_{PU}	Input Pull-up Resistance	PU=high, PD=low	63	190	KΩ
R_{PD}	Input Pull-down Resistance	PU=high, PD=low	63	190	KΩ

Symbol	Parameter	Condition	Min.	Max.	Unit
NOTE: * : Double for SPI/SDIO					

6.4 SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

Figure 6-1 SDIO Voltage Waveform



NOTE

The **input** and **output** in Figure 6-1 apply to the device side.

The following table shows 3.3V SDIO electrical parameters.

Table 6-5 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} - 0.3	-	0.25 * V_{CCQ}	V

NOTE

The **input** and **output** in Table 6-5 apply to the device side.

6.5 GPADC Electrical Characteristics

GPADC contains 7-ch analog-to-digital (ADC) converter for R128-S1 and R128-S2, and 8-ch analog-to-digital (ADC) converter for R128-S3. The ADC is a type of successive approximation register (SAR) converter. The following table lists GPADC electrical characteristics.

Table 6-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	2	V
Quantizing Error	-	7	-	bits
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

6.6 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 1.1 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, Input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 6-7 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DAC to LINEOUTLP/N or LINEOUTRP/N(R=100K)**					
	Full-scale	0dBFS 1kHz	-	1.1	-	Vrms
	SNR(A-weighted)	0data	-	119	-	dB
	THD+N	0dBFS 1kHz	-	-90	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-119	-	dB
ADC Path	**MICIN via ADC**					
	Output Level	MICP=3.6Vpp/2,MICN=3.6Vpp/2, 1kHz，0dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	98	-	dB
	THD+N		-	-60	-	dB
	Output Level	MICP=1.4Vpp/2,MICN=1.4Vpp/2, 1kHz，0dB Gain	-	670	-	mFFS
	THD+N		-	-93	-	dB
	Output Level	MICP=0.9Vpp/2,MICN=0.9Vpp/2, 1kHz，6dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	-60	-	dB
	THD+N		-	98	-	dB
	Output Level	MICP=0.7Vpp/2,MICN=0.7Vpp/2, 1kHz，6dB Gain	-	670	-	mFFS
	THD+N		-	-92	-	dB
	Output Level	MICP=0.454Vpp/2,MICN=0.454Vpp/2, 1kHz，12dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	96	-	dB
	THD+N		-	-60	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Output Level	MICP=0.353Vpp/2,MICN=0.353Vpp/2, 1kHz，12dB Gain	-	670	-	mFFS
	THD+N		-	-92	-	dB
	Output Level	MICP=0.231Vpp/2,MICN=0.231Vpp/2, 1kHz，18dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	94	-	dB
	THD+N		-	-60	-	dB
	Output Level	MICP=0.17975Vpp/2,MICN=0.17975Vpp/2,1kHz，18dB Gain	-	670	-	mFFS
	THD+N		-	-90	-	dB
	Output Level	MICP=0.1181Vpp/2,MICN=0.1181Vpp/2, 1kHz，24dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	91	-	dB
	THD+N		-	-60	-	dB
	Output Level	MICP=0.0918Vpp/2,MICN=0.0918Vpp/2, 1kHz，24dB Gain	-	670	-	mFFS
	THD+N		-	-88	-	dB
	Output Level	MICP=0.0615Vpp/2,MICN=0.0615Vpp/2, 1kHz，30dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	88	-	dB
	THD+N		-	-55	-	dB
	Output Level	MICP=0.0478Vpp/2,MICN=0.0478Vpp/2, 1kHz，30dB Gain	-	670	-	mFFS
	THD+N		-	-85	-	dB
	Output Level	MICP=0.0331pp/2,MICN=0.0331Vpp/2, 1kHz，36dB Gain	-	860	-	mFFS
	SNR(A-weighted)		-	84	-	dB
	THD+N		-	-50	-	dB
	Output Level	MICP=0.0215Vpp/2,MICN=0.0215Vpp/2, 1kHz，36dB Gain	-	670	-	mFFS
	THD+N		-	-79	-	dB

6.7 Frequency Reference Clock

6.7.1 High Frequency Reference Clock

Table 6-8 External Reference Clock Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
FIN	Clock input frequency list using an external clock source	-	40	-	MHz
	Clock input frequency list using a XTAL and the built-in oscillator	-	40	-	MHz
FINTOL	Tolerance on input frequency without trimming	-20	-	+20	ppm
T_{stable}	Clock stabilization time	-	-	10	ms
ILEAK	Input leakage current, both for analog and digital	-	-	1	uA

6.7.1.1 Clock Source Detection

An integrated automatic detection mechanism detects the clock source from the connections of the HXTAL1 and HXTAL2 pins:

- When an external reference clock source is used, the clock input pin is HXTAL2. The R128 supports both an analog and digital source. An analog source shall be AC coupled to HXTAL2 while a digital source shall be DC coupled to HXTAL2. In both cases, HXTAL1 shall be DC grounded.
- When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to HXTAL1 and HXTAL2.

6.7.1.2 External Clock Source

Table 6-9 External Clock Requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit
AC coupled signal					
F_{IN}	Frequency	-	40	-	MHz
V_{PP}	Peak-to-peak voltage range of the AC coupled analog input	0.6	1.0	1.5	V
N_H	Total harmonic content of the input signal	-	-	-25	dBc
DC coupled signal					
V_{IL}	input low voltage on HXTAL2	0	-	0.3*1.5	V
V_{IH}	input high voltage on HXTAL2	0.7*1.5	-	1.5	V
Tr/T_f	10%-90% rise and fall time	-	-	5	ns
Duty Cycle	Cycle-to-cycle	40	50	60	%
Both analog and digital signals					

Symbol	Parameter	Min.	Typ.	Max.	Unit
Phase Noise	Ref clock @ 24 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	 -123 -133 -138 -138	dBc/Hz

6.7.1.3 External XTAL and Built-in Oscillator

Table 6-10 External High Frequency Crystal Characteristics Requirements

Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency Range		-	40	-	MHz
ESR		-	-	60	Ω
Cin_xtal[1]	Single-ended	0	3.5	15	pF
Load Capacitance[1]		-	16	27	pF
Oscillator Tuning Range[2]		+/-20	+/-50	+/-70	ppm
Crystal Frequency Accuracy at Nominal Temp.	25 °C	-10	-	+10	ppm
Crystal Drift Due to Temperature	-20 to +85 °C	-10	-	+10	ppm
Crystal Pull Ability		10	-	150	ppm/pF

NOTE

1. The load capacitance value (C_{load}) and shunt capacitance value(C_{shunt}) depends on XTAL model. XTAL1 and XTAL2 pin have inside capacitance (C_{in_xtal}), so external added load capacitance value (PCB Welding Capacitance) $C_{load\_ext} = C_{load} * 2 - C_{in\_xtal} - C_{pcb} - C_{shunt} * 2$, C_{pcb} is PCB parasitic capacitance (single-ended). C_{in_xtal} has tuning range about 25.4pF, which is controlled by software.

2. Tuning range depends on XTAL load capacitance requirement, typical case is based on 24MHz XTAL, 16pF Cload.

6.7.2 Low Frequency Reference Clock

R128 uses low frequency reference clock. It can use an external low frequency crystal, or a built-in oscillator, or internal RCOSC. The external crystal and a built-in oscillator is used during power save modes.

6.7.2.1 External XTAL and Built-in Oscillator

Table 6-11 External Low Frequency Crystal Characteristics Requirements

Symbol	Conditions	Min.	Typ.	Max.	Unit
Nominal Frequency	-	-	32.768	-	KHz
Load Capacitance[1]	-	-	-	-	pF
C_{shunt}1	-	-	2	-	pF

NOTE

The load capacitance value (C_{load}) and shunt capacitance value (C_{shunt}) depends on LXTAL model, external added load capacitance value (PCB Welding Capacitance) C_{load_ext} = C_{load} * 2 - C_{pcb} - C_{shunt} * 2, C_{pcb} is PCB parasitic capacitance (single-ended).

6.7.2.2 Internal RCOSC Reference Clock Source

R128 has an integrated RC oscillator low frequency reference clock source inside. This clock is calibrated by CPU clock source from high frequency reference. RCOSC takes effect automatically when there is no external crystal.

6.8 Wi-Fi 2.4G RF Receiver Specifications

Table 6-12 Wi-Fi 2.4G RF Receiver Specifications

Test Condition: VBAT= 5 V, VDD_ANA= 1.8 V, Temperature= 25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412	2442	2484	MHz
RX Sensitivity (802.11b)	1Mbps DSSS	-	-97	-95	dBm
	2Mbps DSSS	-	-95.7	-93.7	dBm
	5.5Mbps CCK	-	-93.8	-91.8	dBm
	11Mbps CCK	-	-90.7	-88.7	dBm
RX Sensitivity (802.11g)	6Mbps OFDM	-	-93.6	-91.6	dBm
	9Mbps OFDM	-	-92.9	-90.9	dBm
	12Mbps OFDM	-	-91.5	-89.5	dBm
	18Mbps OFDM	-	-88.9	-86.9	dBm
	24Mbps OFDM	-	-86.2	-84.2	dBm
	36Mbps OFDM	-	-83.0	-81.0	dBm
	48Mbps OFDM	-	-79.0	-77.0	dBm
	54Mbps OFDM	-	-77.3	-75.3	dBm
RX Sensitivity	MCS 0	-	-93.0	-91.0	dBm

(802.11n, 20MHz)	MCS 1	-	-90.0	-88.0	dBm
	MCS 2	-	-87.7	-85.7	dBm
	MCS 3	-	-85.0	-83.0	dBm
	MCS 4	-	-81.8	-79.8	dBm
	MCS 5	-	-77.4	-75.4	dBm
	MCS 6	-	-76.0	-74.0	dBm
	MCS 7	-	-74.4	-72.4	dBm
Maximum Receive Level	6 Mbps OFDM	-10	18.0	-	dBm
	54 Mbps OFDM	-10	2.0	-	dBm
	MCS0	-10	18.0	-	dBm
	MCS7	-20	2.0	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	41.1	43.1	-	dBc
	11 Mbps CCK	35.4	37.4	-	dBc
	BPSK rate 1/2, 6 Mbps OFDM	35.4	37.4	-	dBc
	64QAM rate 3/4, 54 Mbps OFDM	24.2	26.2	-	dBc
	HT20, MCS 0, BPSK rate 1/2	28.8	30.8	-	dBc
	HT20, MCS 7, 64QAM rate 5/6	7.2	9.2	-	dBc

NOTE

The minimum limit considers the variation of process, voltage and temperature.

6.9 Wi-Fi 2.4G RF Transmitter Specifications

Table 6-13 Wi-Fi 2.4G RF Transmitter Specifications

Condition: VBAT= 5 V, VDD_ANA= 1.8 V, Temperature= 25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2412	2442	2484	MHz
TX output Power with mask and EVM compliance[1]	1Mbps DSSS	18.6	19.1	-	dBm
	11Mbps CCK	19.4	19.9	-	dBm
	6Mbps OFDM	18.3	18.8	-	dBm
	54Mbps OFDM	16.6	17.1	-	dBm

	HT20, MCS 0	17.1	17.6	-	dBm
	HT20, MCS 7	16.7	17.2	-	dBm
TX EVM	1Mbps DSSS	-	-22.2	-20.2	dB
	11Mbps CCK	-	-21.9	-19.9	dB
	6Mbps OFDM	-	-31.2	-29.2	dB
	54Mbps OFDM	-	-32.0	-30.0	dB
	HT20, MCS 0	-	-30.8	-28.8	dB
	HT20, MCS 7	-	-31.9	-29.9	dB
Carrier Suppression		-	-	-40	dBc
Accuracy of Power Control	Closed-loop control across all temperature ranges and channels	-1.5	-	+1.5	dB
Harmonic Output Power	2nd Harmonic	-	-42.5	-	dBm/MHz
	3rd Harmonic	-	-41.1	-	dBm/MHz

NOTE

1.Refer to IEEE 802.11 specification for Tx spectrum limits:
802.11b mask (18.4.7.3)
802.11g mask (19.5.4)
802.11g EVM (17.3.9.6.3)
802.11n HT20 mask (20.3.21.1)
802.11n HT20 EVM (20.3.21.7.3)

2. The minimum limit considers the variation of process, voltage and temperature.

6.10 Bluetooth RF Receiver Specifications

Table 6-14 Bluetooth RF Receiver Specifications

Condition: VBAT= 5 V, VDD18_ANA= 1.8 V, Temperature= 25°C

Symbol	Description	Performance			
		Min.	Typ.	Max.	unit
Frequency Range	Center channel frequency	2402	2441	2480	MHz
RX Sensitivity	BR Sensitivity at 1Mbps, BER≤0.1%	-	-95	-93	dBm
	EDR Sensitivity at 2Mbps, BER≤0.01%	-	-95	-93	dBm
	EDR Sensitivity at 3Mbps, BER≤0.01%	-	-89	-87	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%	-	-100	-98	dBm
	BLE Sensitivity at 2Mbps, PER≤30.8%	-	-97	-95	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%, S=2	-	-102	-100	dBm

	BLE Sensitivity at 1Mbps, PER≤30.8%, S=8	-	-107	-105	dBm
Maximum Receiving Power	BR Sensitivity at 1Mbps, BER≤0.1%	-	-2	-	dBm
	EDR Sensitivity at 2Mbps, BER≤0.01%	-	-2	-	dBm
	EDR Sensitivity at 3Mbps, BER≤0.01%	-	-2	-	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%	-	0	-	dBm
	BLE Sensitivity at 2Mbps, PER≤30.8%	-	0	-	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%, S=2	-	0	-	dBm
	BLE Sensitivity at 1Mbps, PER≤30.8%, S=8	-	0	-	dBm
BR C/I (1Mbps)	Co-channel	-	6.5	-	dB
	±1MHz offset	-	-9.0	-	dB
	±2MHz offset	-	-34.5	-	dB
	>=±3MHz offset	-	-43.2	-	dB
EDR C/I (3Mbps)	Co-channel	-	16.3	-	dB
	1MHz offset	-	-4.8	-	dB
	2MHz offset	-	-30.7	-	dB
	3MHz offset	-	-40.2	-	dB
BLE C/I (1Mbps)	Co-channel	-	6.2	-	dB
	±1MHz offset	-	-8.8	-	dB
	±2MHz offset	-	-38.7	-	dB
	>=±3MHz offset	-	-47.7	-	dB
BLE C/I (2Mbps)	Co-channel	-	6.8	-	dB
	±1MHz offset	-	-8.2	-	dB
	±2MHz offset	-	-34.5	-	dB
	>=±3MHz offset	-	-45.0	-	dB

NOTE

The minimum limit considers the variation of process, voltage and temperature.

6.11 Bluetooth RF Transmitter Specifications

Table 6-15 Bluetooth RF Transmitter Specifications

Condition: VBAT= 5 V, VDD18_ANA= 1.8 V, Temperature= 25°C

Symbol	Description	Performance

		Min.	Typ.	Max.	Unit
Frequency Range	Center channel frequency	2402	2441	2480	MHz
Output Power Range	BR/EDR/BLE	-20	6	10	dBm
TX RF Output Steps	BR@1Mbps	2	4	8	dB
	EDR@3Mbps	2	4	8	dB
TX Power Variation vs. Temp	-40~125 oC	-	+/-1	-	dB
TX Power Variation vs. Frequency	-40~125 oC	-	+/-1	-	dB
Out of Band Spurious Emissions (at 6dBm)	Frequencies<2.4GHz	-	-	-50	dBm
Out of Band Spurious Emissions (at 20dBm)	2.48-12GHz, including harmonics	-	-	-40	dBm

NOTE

The minimum limit considers the variation of process, voltage and temperature.

6.12 Power Consumption Parameters

6.12.1 System Power Consumption

If you have questions about system power consumption parameters, contact Allwinner FAE.

6.12.2 Wi-Fi Power Consumption

Table 6-16 Wi-Fi Power Consumption

Test Condition: Temp= 25°C, VBAT= 3.3V, VDD18_ANA= 1.8V

Symbol	MCU State	Wi-Fi State	TX/RX	Test Condition (Signaling Mode)		Performance Min.	Typ.	Max.	Unit
ACTIVE	ACTIVE	ACTIVE	TX	1M DSSS	17dBm	-	338	-	mA
				11M CCK	17dBm	-	343	-	mA
				6M OFDM	16dBm	-	335	-	mA
				54M OFDM	16dBm	-	333	-	mA
				HT20, MCS0	16dBm	-	333	-	mA
				HT20, MCS7	15dBm	-	318	-	mA
			RX	1M DSSS	-	-	153	-	mA
				11M CCK	-	-	153	-	mA
				6M OFDM	-	-	154	-	mA
				54M	-	-	154	-	mA

				OFDM					
				HT20, MCS0	-	-	152	-	mA
				HT20, MCS7	-	-	152	-	mA
STANDBY	SLEEP	ACTIVE	TX	1M DSSS, null frame	17dBm	-	272	-	mA
			RX	RX listen	-	-	48.3	-	mA
				1M DSSS	-	-	43.4	-	mA
		PS Mode	RX	DTIM1	-	-	1284	-	uA
				DTIM3	-	-	741	-	uA
				DTIM8	-	-	582	-	uA
				DTIM10	-	-	546	-	uA
		OFF	-	-	-	-	410	-	uA
HIBERNATION	OFF	OFF	-	-	-	-	79.7	-	uA
SHUTDOWN	OFF	OFF	-	-	-	-	33.4	-	uA

6.12.3 Bluetooth Power Consumption

Table 6-17 Bluetooth Power Consumption

Test Condition: Temp= 25°C, VBAT= 3.3V, VDD18_ANA= 1.8V

Symbol	MCU State	BT State	TX/RX	Test Condition	Performance			
					Min.	Typ.	Max.	Unit
ACTIVE	ACTIVE	ACTIVE	TX	DH1@Tx=8.6dBm	-	161	-	mA
				2DH3@Tx=8.6dBm	-	160	-	mA
				3DH5@Tx=8.6dBm	-	160	-	mA
				1Ms/s@Tx=8.6dBm	-	188	-	mA
				2Ms/s@Tx=8.6dBm	-	175	-	mA
				Code S=2@Tx=8.6dBm	-	188	-	mA
				Code S=8@Tx=8.6dBm	-	187	-	mA
			RX	DH1	-	137	-	mA
				2DH3	-	137		mA
				3DH5	-	137		mA
				1Ms/s	-	134	-	mA
				2Ms/s	-	136	-	mA
				Code S=2	-	137	-	mA
				Code S=8	-	137	-	mA
HIBERNATION	OFF	OFF	-	-	-	79.7	-	uA
SHUTDOWN	OFF	OFF	-	-	-	33.4	-	uA

6.13 External Peripheral Electrical Characteristics

6.13.1 SMHC AC Electrical Characteristics

6.13.1.1 HS-SDR/HS-DDR Mode

NOTE

IO voltage is 1.8V.

The following figures and table show the output timing in HS-SDR/HS-DDR mode.

Figure 6-2. SMHC Output Timing Diagram in HS-SDR Mode

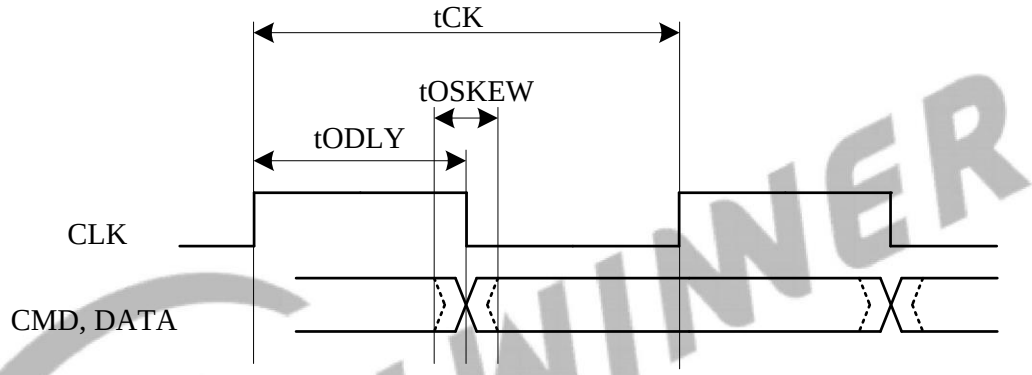


Figure 6-3. SMHC Output Timing Diagram in HS-DDR Mode

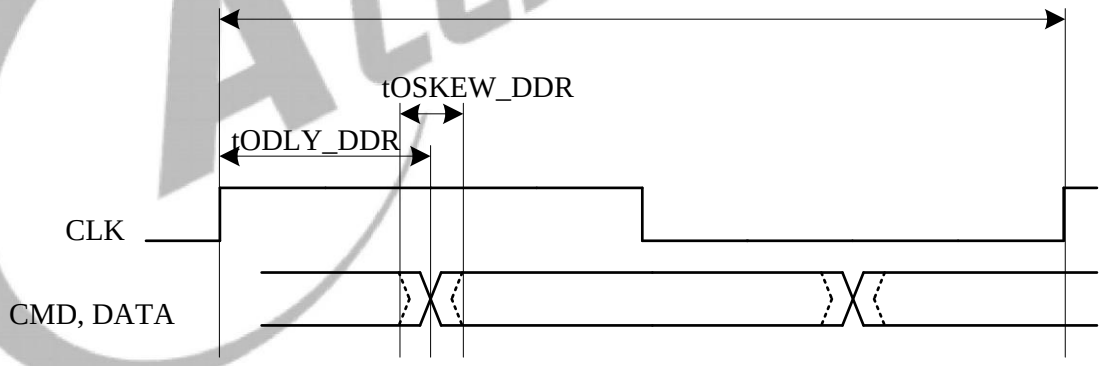


Table 6-18 Output timing parameter for HS-SDR/HS-DDR

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
NOTE: 1. Unit Interval (UI) is one-bit nominal time. For example, UI=20ns at 50MHz. 2. The GPIO's driver strength level is 2 for test.						

The following figures and table show the input timing in HS-SDR/HS-DDR mode.

Figure 6-4 SMHC Input Timing Diagram in HS-SDR Mode

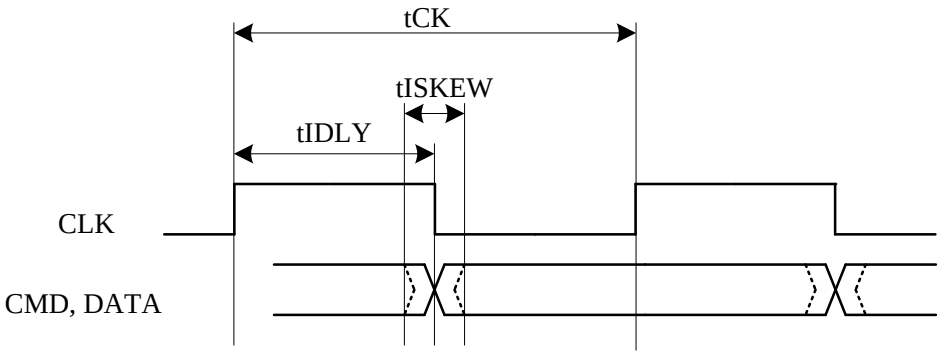


Figure 6-5 SMHC Input Timing Diagram in HS-DDR Mode

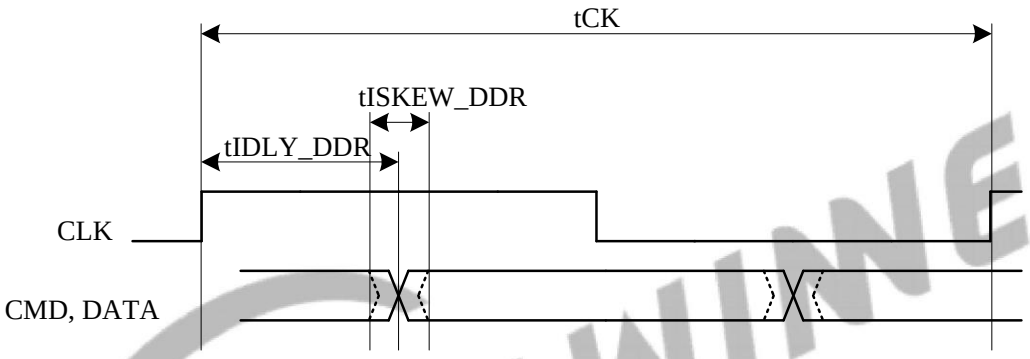


Table 6-19 Input timing parameter for HS-SDR/HS-DDR

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-		ns	
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-		ns	
Data input skew time in SDR mode	tISKEW	-	-		ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-		ns	
NOTE: The GPIO's driver strength level is 2 for test.						

6.13.1.2 HS200 Mode

NOTE

The HS200 mode supports only the 4-bit bandwidth.

The following figure and table show the output timing in HS200 mode.

Figure 6-6 SMHC HS200 Output Timing Diagram

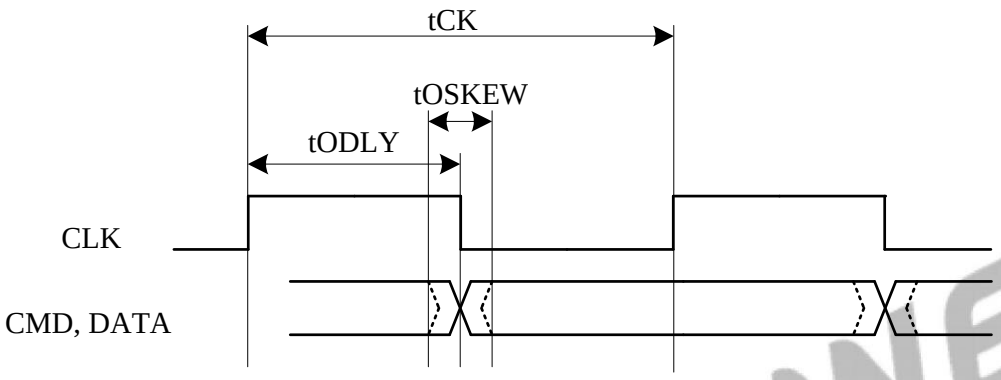


Table 6-20 Output timing parameter for HS200

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-		ns	
NOTE: 1. Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. 2. The GPIO's driver strength level is 3 for test.						

The following figures and tables shows the input timing in HS200 mode.

Figure 6-7 HS200 Device input timing

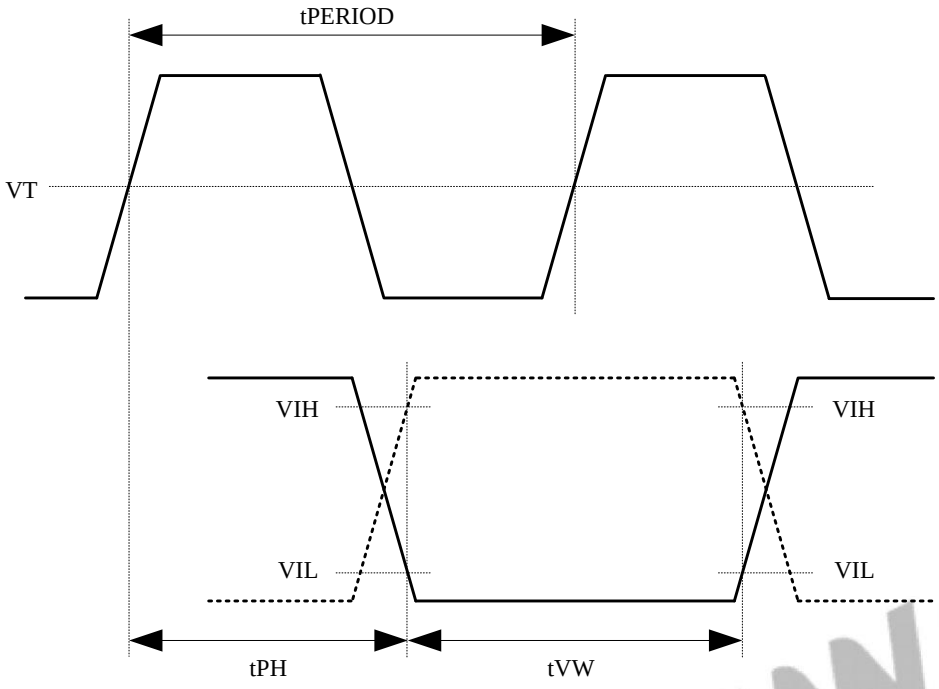


Table 6-21 Intput timing parameter for HS200

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, Data valid window	tVW	0.575	-	-	UI	
NOTE: 1. Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. 2. The GPIO's driver strength level is 3 for test. 3.Temperature variation: -20°C 4.Temperature variation: 90°C						

6.13.2 SPI AC Electrical Characteristics

The following figures and table show the timing of SPI.

Figure 6-8 SPI MOSI Timing

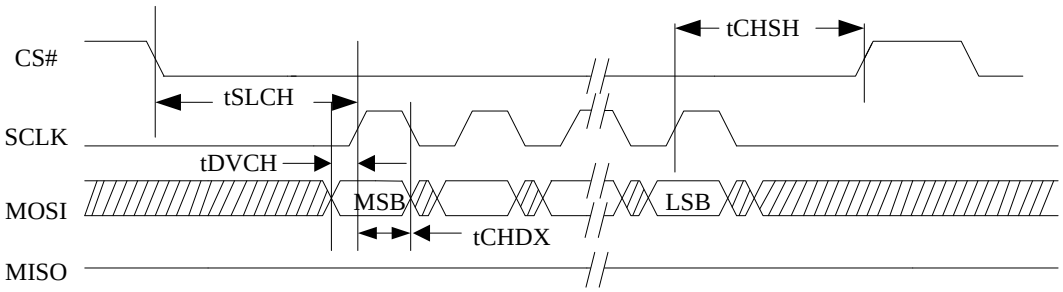


Figure 6-9 SPI MISO Timing

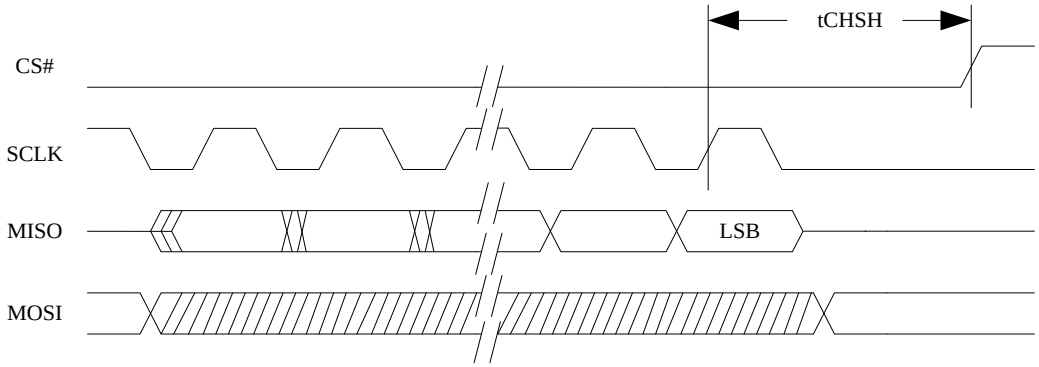


Table 6-22 SPI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CS# Active Setup Time	tSLCH	-	2T	-	ns
CS# Active Hold Time	tCHSH	-	2T(1)	-	ns
Data In Setup Time	tDVCH	-	T/2-3	-	ns
Data In Hold Time	tCHDX	-	T/2-3	-	ns

NOTE: T is the cycle of clock.

6.13.3 SPI_DBI AC Electrical Characteristics

Figure 6-10 DBI 3-Line Interface

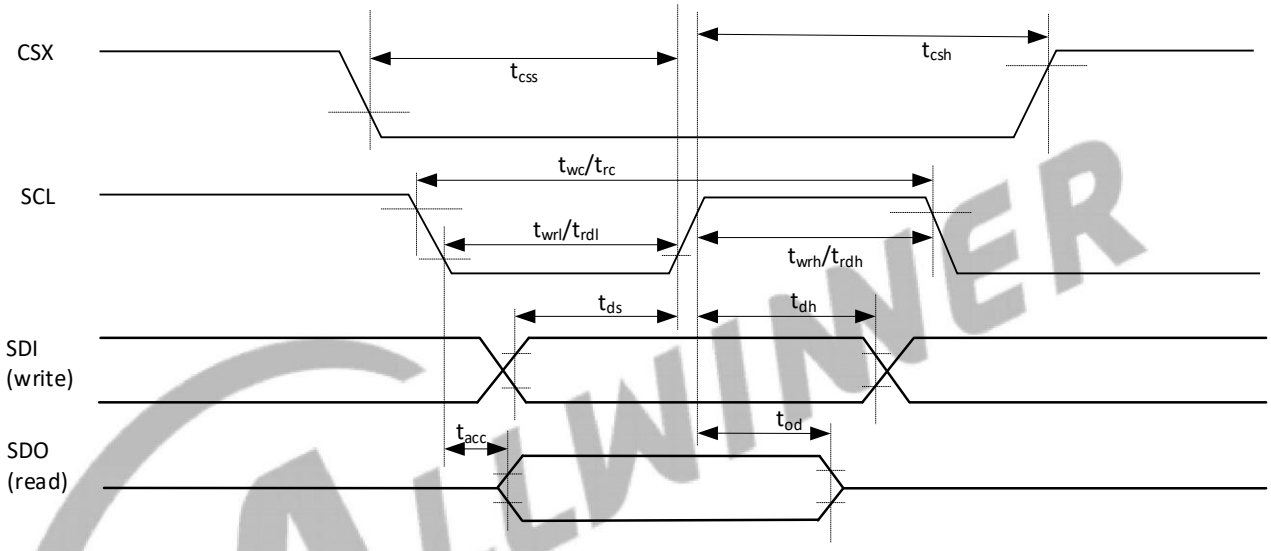


Table 6-23 DBI 3-line Serial Interface Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time (Write)	t_{css}	15		ns
	Chip select setup time (Read)	t_{csh}	60		ns
SCL (write)	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SCL (read)	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Data setup time	t_{ds}	7		ns

(write)	Data hold time	t_{dt}	7		ns
SDI/SDO (read)	Read access time	t_{racc}	10	50	ns
	Output disable time	t_{od}	15	50	ns

Figure 6-11 DBI 4-line Serial Interface Timing

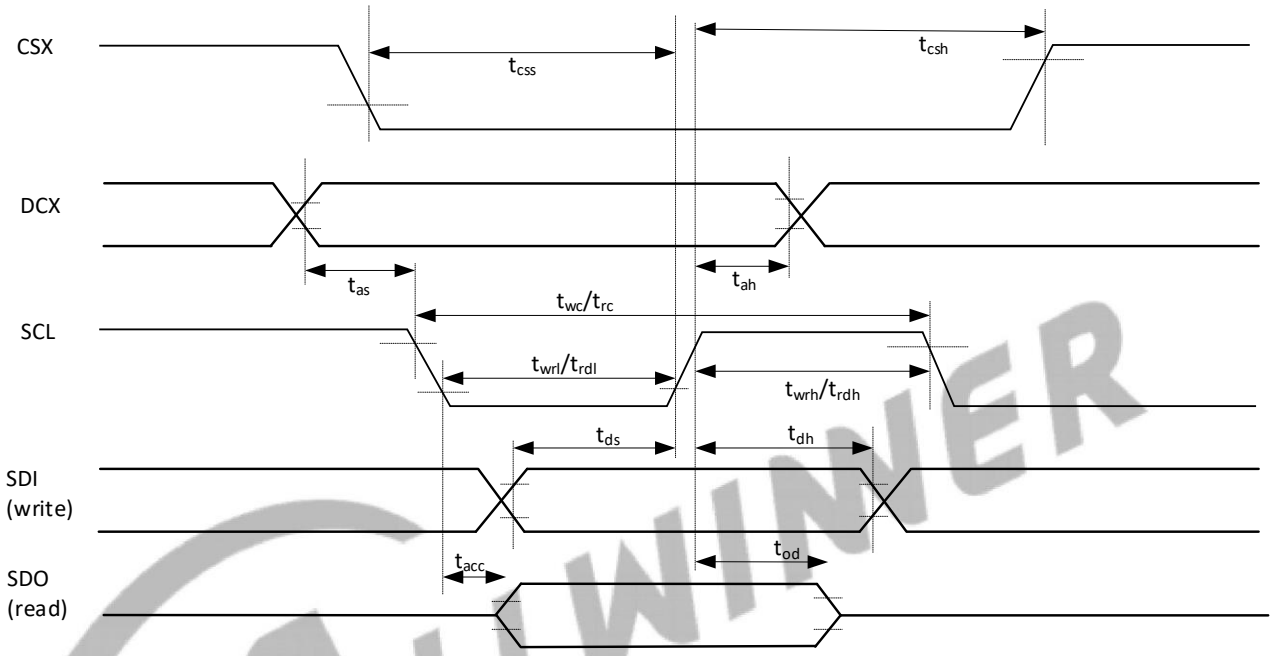


Table 6-24 DBI 4-line Serial Interface Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time (Write)	t_{css}	15		ns
	Chip select setup time (Read)	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time (Write/Read)	t_{ah}	10		ns
SCL (write)	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SCL (read)	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns

SDI/SDO (write)	Data setup time	t_{ds}	7		ns
	Data hold time	t_{dt}	7		ns
SDI/SDO (read)	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15	50	ns

6.13.4 SPI Flash AC Electrical Characteristics

The timing of SPI shows in Figure 6-12 and Figure 6-13.

Figure 6-12 SPI MOSI Timing

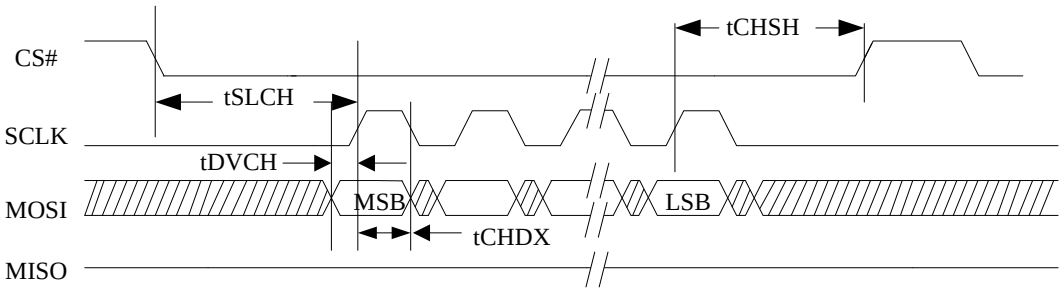


Figure 6-13 SPI MISO Timing

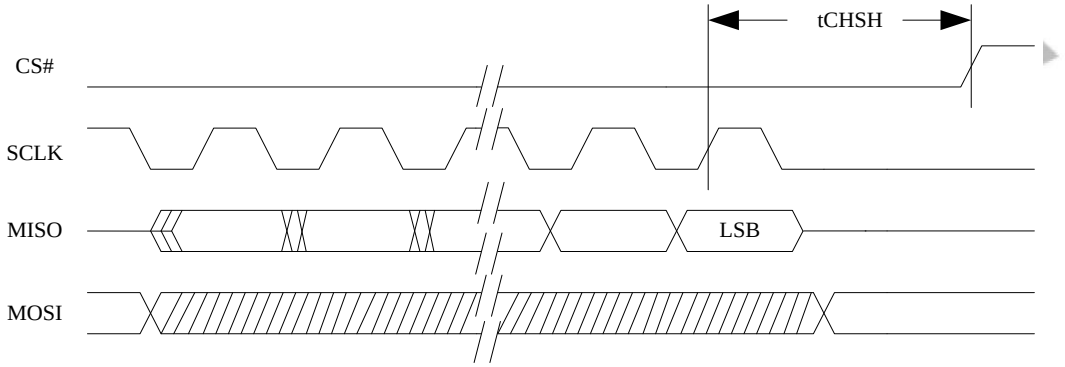


Table 6-25 SPI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CS# Active Setup Time	tSLCH	-	2T	-	ns
CS# Active Hold Time	tCHSH	-	2T(1)	-	ns
Data In Setup Time	tDVCH	-	T/2-3	-	ns
Data In Hold Time	tCHDX	-	T/2-3	-	ns

NOTE (1): T is the cycle of clock.

6.13.5 UART AC Electrical Characteristics

Figure 6-14 UART RX Timing

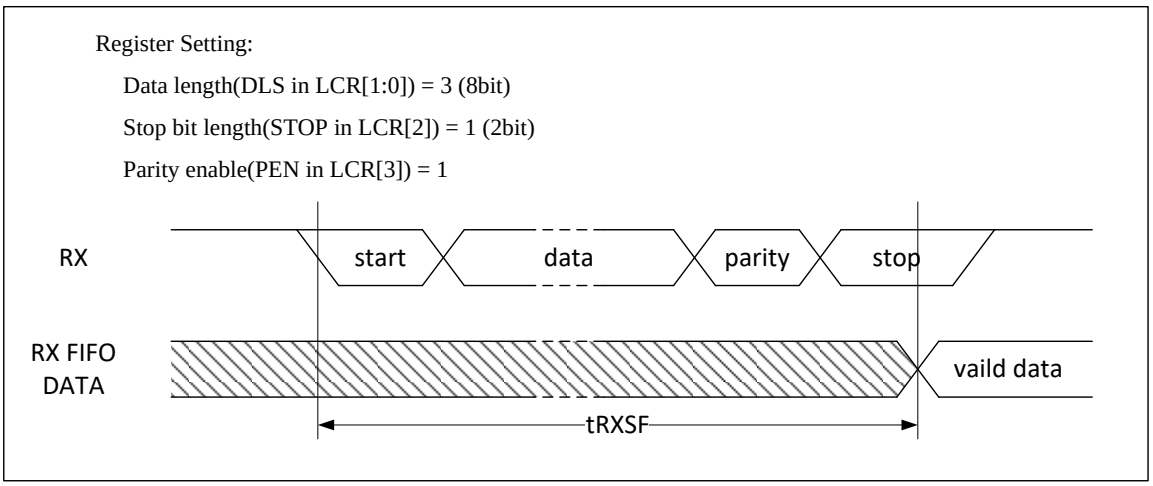


Figure 6-15 UART nCTS Timing

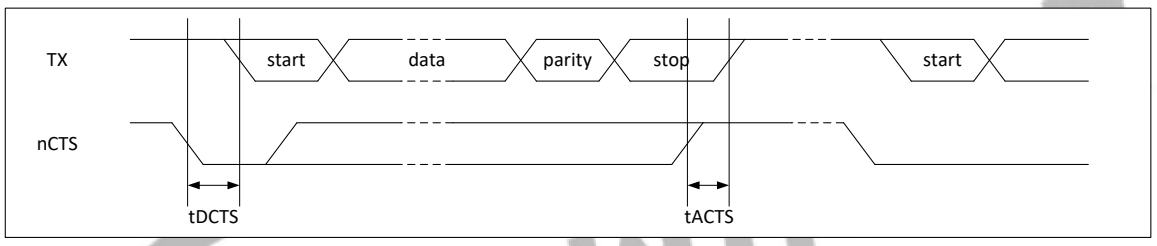


Figure 6-16 UART nRTS Timing

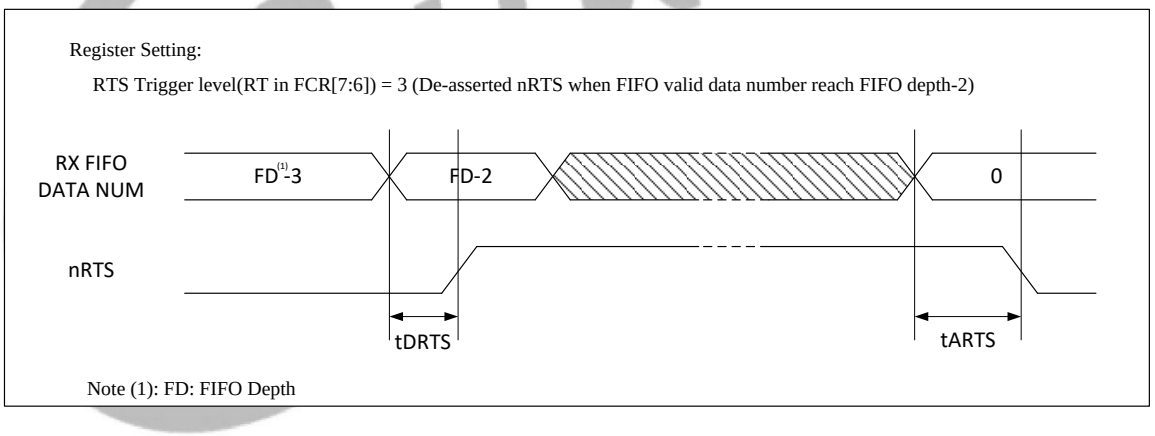


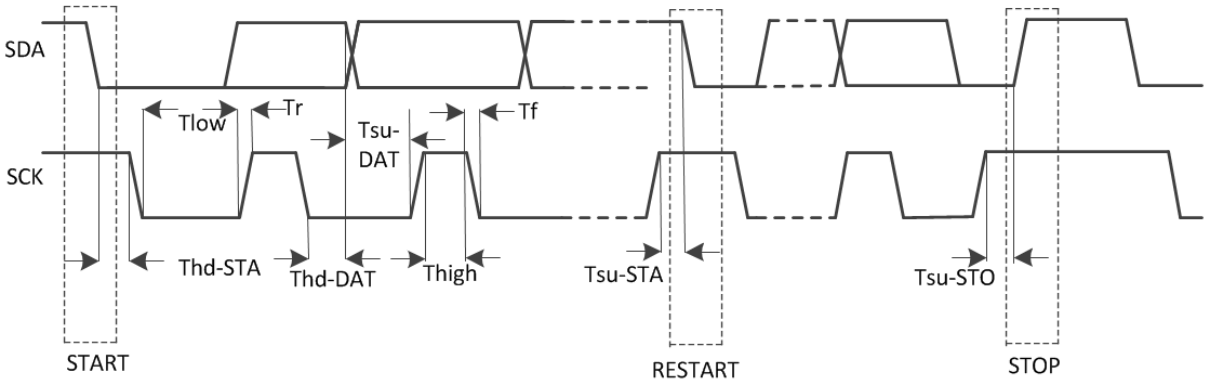
Table 6-26 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5 * BRP(1)	-	11 * BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
Note: BRP: Baud-Rate Period.					

6.13.6 TWI AC Electrical Characteristics

The following figure provides an illustration of the relation of SDA signal line and SCL signal line on the TWI serial bus.

Figure 6-17 TWI Timing Diagram



The timing parameters of TWI timing shows in the following table.

Table 6-27 TWI Timing Constants

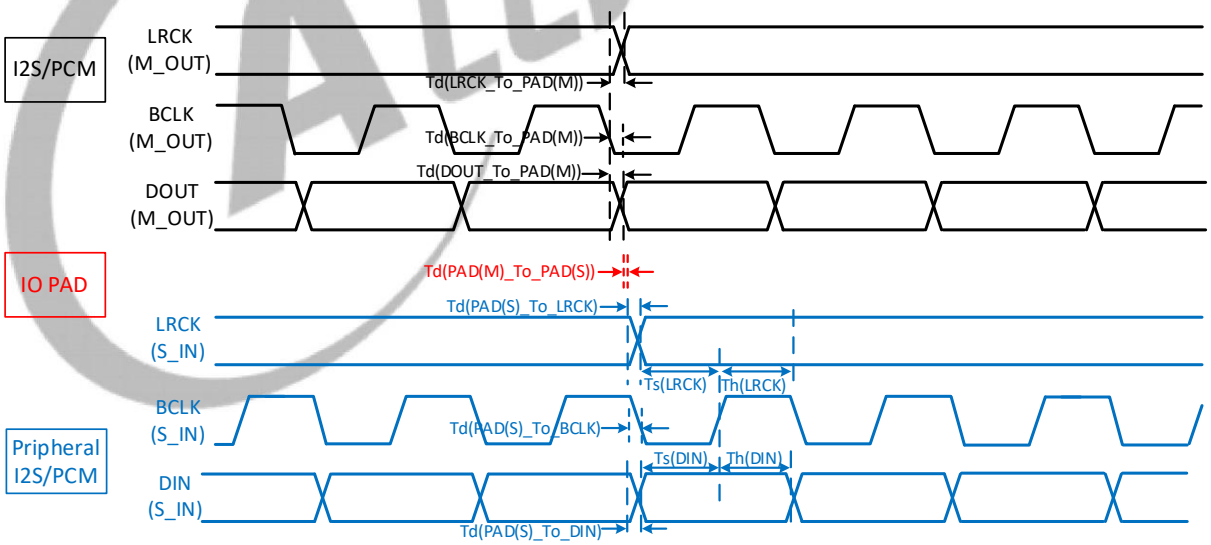
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	5.0	-	-	-	ns
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

6.13.7 I2S/PCM AC Electrical Characteristics

6.13.7.1 Data Output timing of I2S/PCM in Master mode

The Data Output timing of I2S/PCM in Master mode and the Data Input timing of Peripheral I2S/PCM in Slave mode show in Figure 6-18.

Figure 6-18 Data Output Timing of I2S/PCM in Master Mode



The Data Output timing parameters of I2S/PCM in Master mode and The Data Input timing parameters of Peripheral I2S/PCM in Slave mode show in the following table.

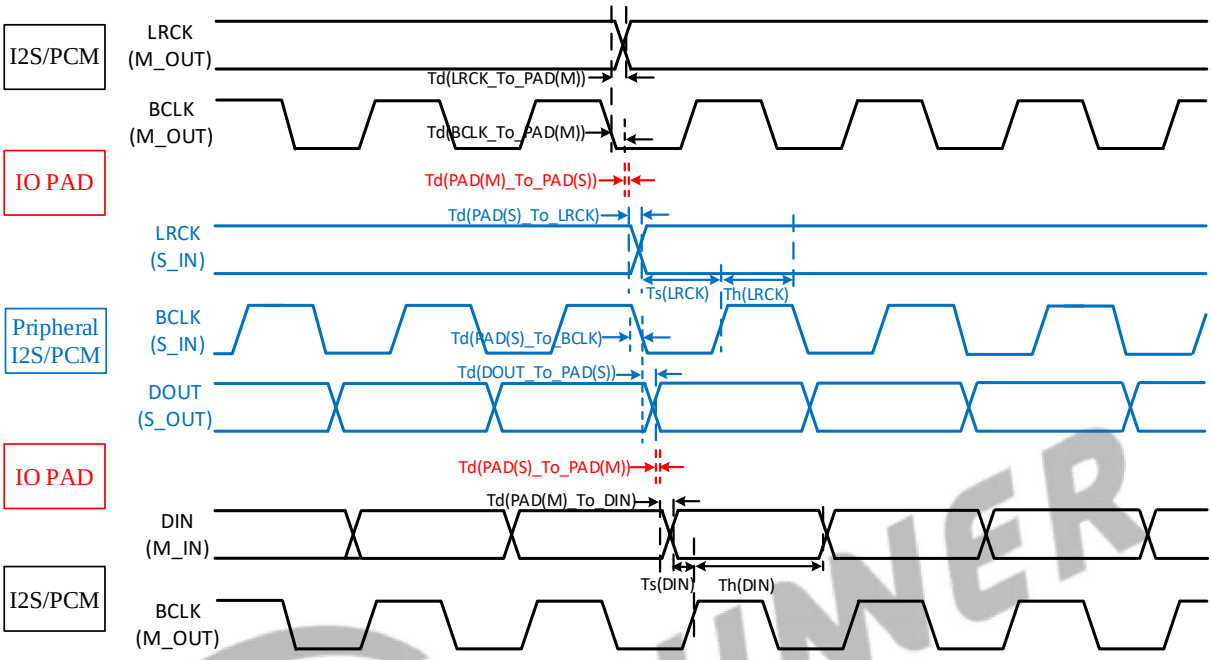
Table 6-28 Data Output Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
T_d(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5 (restriction)	T_w1<2.5(requirement)	ns
T_d(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(restriction)		
T_d(DOUT_To_PAD(M))	DOUT to PAD(M) Delay	/	T3<6.5(restriction)		
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
T_d(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T4*<7.0(estimation)	T_w2*<1.0(requirement)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay	/	T5*<7.0(estimation)		
	DOUT PAD(M) to DIN PAD(S) Delay	/	T6*<7.0(estimation)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
T_d(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T7*<6.5(assumption)	T_w3*<2.5(requirement)	ns
T_d(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T8*<6.5(assumption)		
T_d(PAD(S)_To_DIN)	PAD(S) to DIN Delay	/	T9*<6.5(assumption)		
T_s(LRCK)	LRCK Setup Slack	T10*(analysis)	/	/	ns
T_h(LRCK)	LRCK Hold Slack	T11*(analysis)	/	/	ns
T_s(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
T_h(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

6.13.7.2 Data Input timing of I2S/PCM in Master Mode

The Data Input timing of I2S/PCM in Master mode and the Data Output timing of Peripheral I2S/PCM in Slave mode show in Figure 6-19.

Figure 6-19 Data Input Timing of I2S/PCM in Master Mode



The Data Input timing parameters of I2S/PCM in Master mode and The Data Output timing parameters of Peripheral I2S/PCM in Slave mode are shown in the following table.

Table 6-29 Data Input Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5(requirement)	Tw1<2.5 (estimation)	ns
Td(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(requirement)		ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T3*<7.0(requirement)	Tw2*<1.0 (estimation)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay		T4*<7.0(requirement)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T5*<6.5(requirement)	Tw3*<2.5 (estimation)	ns

Parameter		Min	Max	Skew	Units
Td(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T6*<6.5(requirement)		ns
Td(DOUT_To_PAD(S))	DOUT to PAD(S) Delay	/	T7*<6.5(requirement)	/	ns
Ts(LRCK)	LRCK Setup Slack	T8*(analysis)	/	/	ns
Th(LRCK)	LRCK Hold Slack	T9*(analysis)	/	/	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_PAD(M))	DOUT PAD(S) to DIN PAD(M) Delay	/	T10*<7.0 (requirement)	/	ns
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(PAD(M)_To_DIN)	PAD(M) to DIN Delay	/	T11<6.5(requirement)	/	ns
Ts(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
Th(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

6.13.8 OWA AC Electrical Characteristics

Figure 6-20 OWA Timing

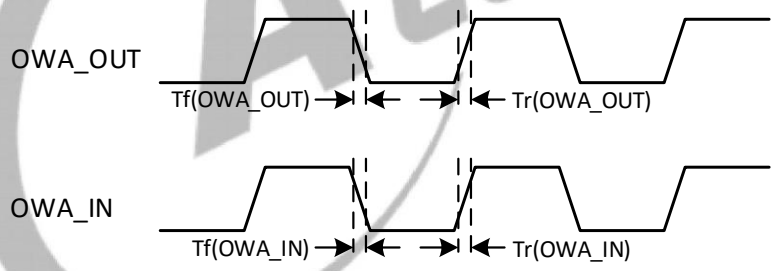


Table 6-30 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN rise time	Tr(OWA_IN)	-	-	4	ns
OWA_IN fall time	Tf(OWA_IN)	-	-	4	ns

6.13.9 CIR_RX AC Electrical Characteristics

Figure 6-21 CIR_RX Timing

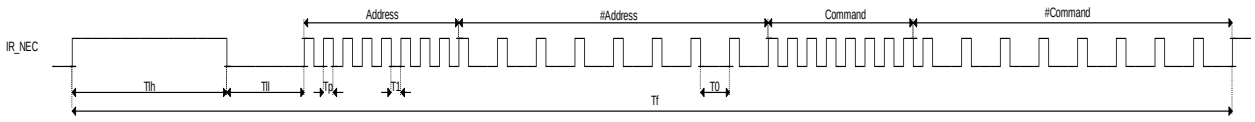


Table 6-31 CIR_RX Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1690	-	us
Logical 0 low time	T0	-	560	-	us

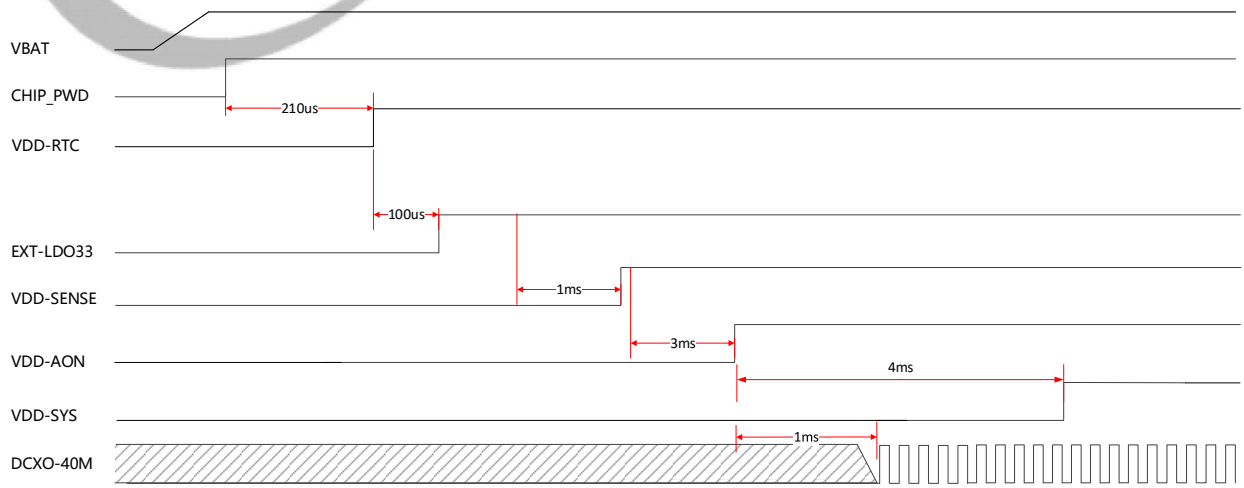
6.14 Power-On and Power-Off Sequence

6.14.1 Power-On Sequence

The following figure shows an example of the power on sequence for the R128 device. The description of the power on sequence is as follows.

- The time required by the three phases between CHIP_PWD release and EXT_LDO33 output is determined by the time the analog circuit takes for stabilization. The time periods shown in the following figure are all the typical values predicted.
- The time of each phase between EXT_LDO33 output and DCXO start is controlled by PMU through RCOSC counting. The counting waiting time can be re-configured after CPU start. The time shown in the following figure is controlled by the default waiting value, and RCOSC is calculated based on the typical 1.4 MHz clock frequency.
- The typical frequency of RCOSC is 1.4 MHz and ranges from 1 to 2 MHz. DCXO supports frequencies of 40 MHz.

Figure 6-22 Power On Sequence



NOTE:

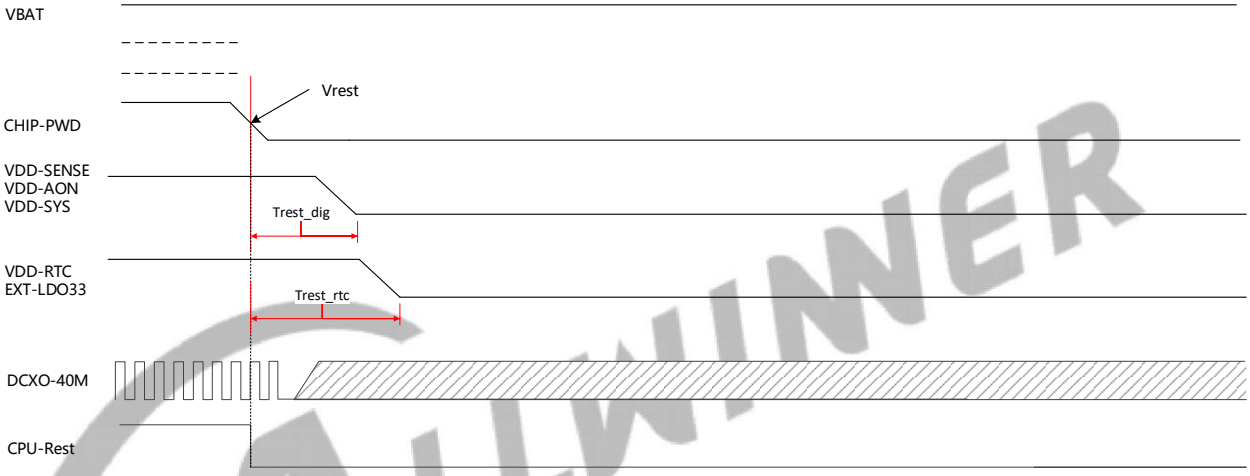
VBAT and CHIP_PWD are external IO interfaces. VBAT is battery and CHIP_PWD is reset pin. The rest is internal circuits.

6.14.2 Power-Off Sequence

The power-off requirements are as follows.

- After VDD-SENSE goes low, DCXO clock starts to stop oscillating.
- No special restrictions for other power rails.

Figure 6-23 Power Off Sequence



NOTE:

VBAT and CHIP_PWD are external IO interfaces. VBAT is battery and CHIP_PWD is reset pin. The rest is internal circuits.

7 Package Thermal Characteristics

The following tables show thermal resistance parameters of the R128. The following thermal resistance characteristics are based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board, natural convection, no air flow.

7.1 R128-S1

Table 7-1 R128-S1 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	33.62	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	14.87	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	5.49	-	°C/W

7.2 R128-S2

Table 7-2 R128-S2 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	35.04	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	15.05	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	5.44	-	°C/W

7.3 R128-S3

Table 7-3 R128-S3 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	34.94	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	15.1	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	5.86	-	°C/W

8 Pin Assignment

8.1 Pin Map

R128-S1, R128-S2 and R128-S3 have 80 balls in the QFN package. The ball pitch is 0.35 mm and the chip body size is 8 mm x 8 mm.

8.1.1 R128-S1 & R128-S2

The following figure shows the pin map of R128-S1 and R128-S2.

Figure 8-1 R128-S1 & R128-S2 Pin Map

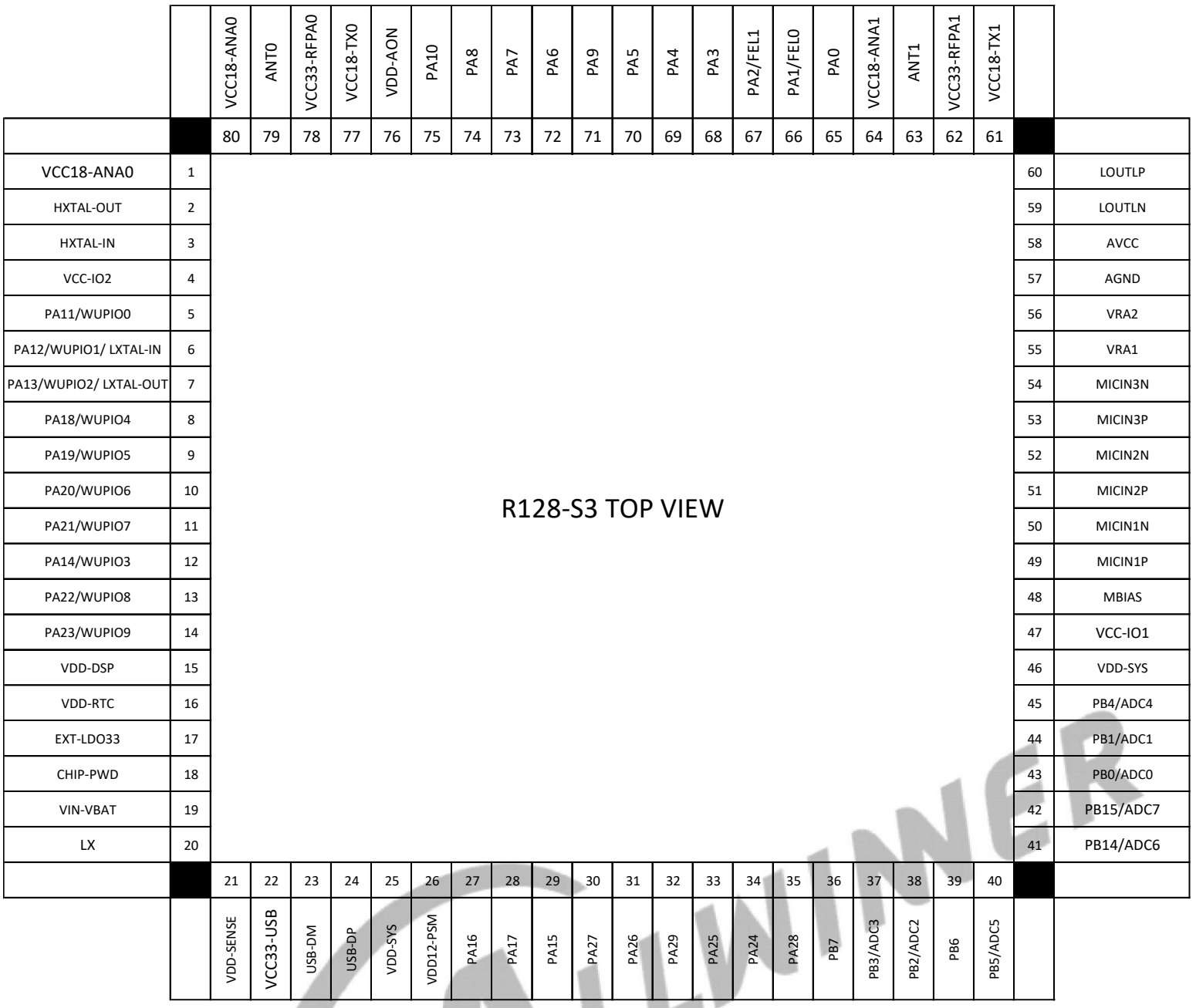
		80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	
		VCC18-ANA0	ANT0	VCC33-RFPA0	VCC18-TX0	VDD-AON	PA10	PA8	PA7	PA6	PA9	PA5	PA4	PA3	PA2/FEL1	PA1/FEL0	PA0	VCC18-ANA1	ANT1	VCC33-RFPA1	VCC18-TX1	
VCC18-ANA0	1																					60 LOUTRN
HXTAL-OUT	2																					59 LOUTRP
HXTAL-IN	3																					58 LOUTLP
VCC-IO2	4																					57 LOUTLN
PA11/WUPIO0	5																					56 AVCC
PA12/WUPIO1/ LXTAL-IN	6																					55 AGND
PA13/WUPIO2/ LXTAL-OUT	7																					54 VRA2
PA18/WUPIO4	8																					53 VRA1
PA19/WUPIO5	9																					52 MICIN3N
PA20/WUPIO6	10																					51 MICIN3P
PA21/WUPIO7	11																					50 MICIN2N
PA14/WUPIO3	12																					49 MICIN2P
PA22/WUPIO8	13																					48 MICIN1N
PA23/WUPIO9	14																					47 MICIN1P
VDD-DSP	15																					46 MBIAS
VDD-RTC	16																					45 VCC-IO1
EXT-LDO33	17																					44 VDD-SYS
CHIP-PWD	18																					43 PB4/ADC4
NC	19																					42 PB0/ADC0
VIN-VBAT	20																					41 PB1/ADC1
		21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	
		LX	VDD-SENSE	VCC33-USB	USB-DM	USB-DP	VDD-SYS	VDD12-PSM	PA16	PA17	PA15	PA27	PA26	PA29	PA25	PA24	PA28	PB3/ADC3	PB2/ADC2	PB14/ADC6	PB15/ADC7	

R128-S1/R128-S2 Top View

8.1.2 R128-S3

The following figure shows the pin map of R128-S3.

Figure 8-2 R128-S3 Pin Map



8.1.3 Pin Map Difference Between R128-S1/R128-S2 and R128-S3

Table 8-1 The Pin Map Difference between R128-S1/R128-S2 and R128-S3

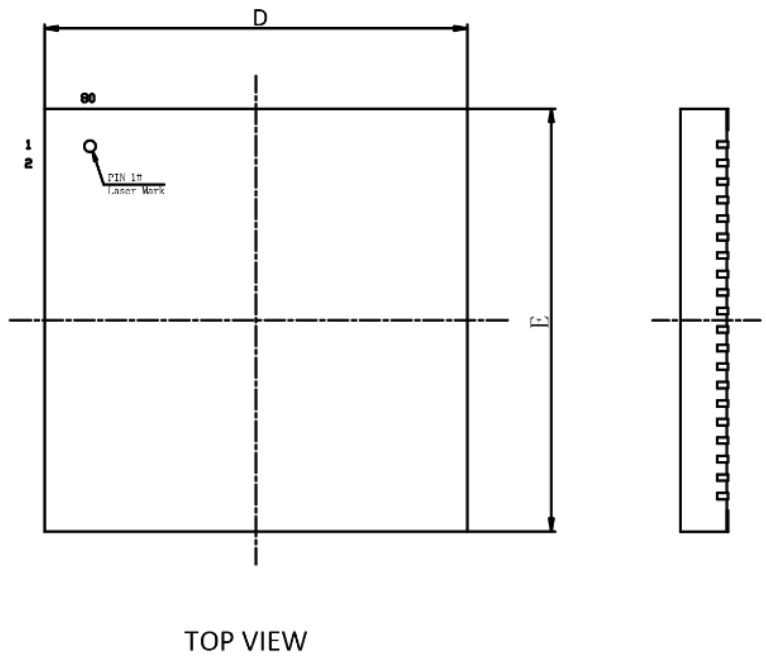
Ball Number	R128-S1/R128-S2 Pin	R128-S3 Pin
19	NC	VIN-VBAT
20	VIN-VBAT	LX
21	LX	VDD-SENSE
22	VDD-SENSE	VCC33-USB
23	VCC33-USB	USB-DM
24	USB-DM	USB-DP
25	USB-DP	VDD-SYS
26	VDD-SYS	VDD12-PSM
27	VDD12-PSM	PA16
28	PA16	PA17
29	PA17	PA15
30	PA15	PA27
31	PA27	PA26
32	PA26	PA29
33	PA29	PA25
34	PA25	PA24
35	PA24	PA28
36	PA28	PB7
39	PB14/ADC6	PB6
40	PB15/ADC7	PB5/ADC5

Ball Number	R128-S1/R128-S2 Pin	R128-S3 Pin
41	PB1/ADC1	PB14/ADC6
42	PB0/ADC0	PB15/ADC7
43	PB4/ADC4	PB0/ADC0
44	VDD-SYS	PB1/ADC1
45	VCC-IO1	PB4/ADC4
46	MBIAS	VDD-SYS
47	MICIN1P	VCC-IO1
48	MICIN1N	MBIAS
49	MICIN2P	MICIN1P
50	MICIN2N	MICIN1N
51	MICIN3P	MICIN2P
52	MICIN3N	MICIN2N
53	VRA1	MICIN3P
54	VRA2	MICIN3N
55	AGND	VRA1
56	AVCC	VRA2
57	LOUTLN	AGND
58	LOUTLP	AVCC
59	LOUTRP	LOUTLN
60	LOUTRN	LOUTLP

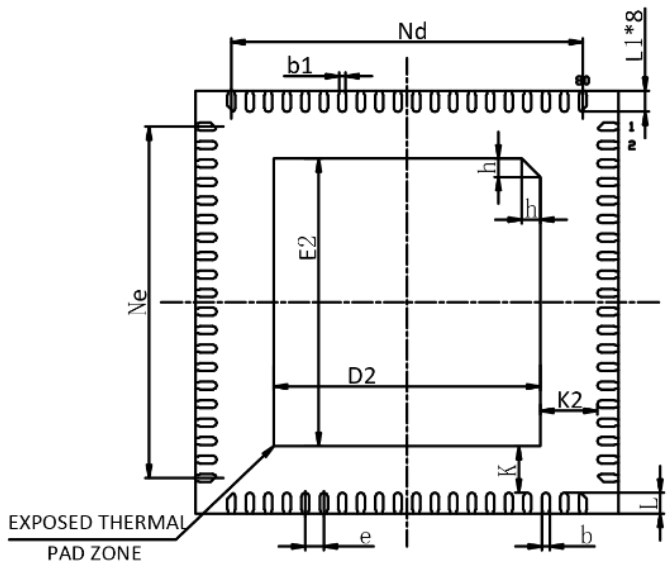
8.2 Package Dimension

Figure 8-3 shows the top, the bottom, and the side views of the R128-S1, R128-S2, and R128-S3 package dimension.

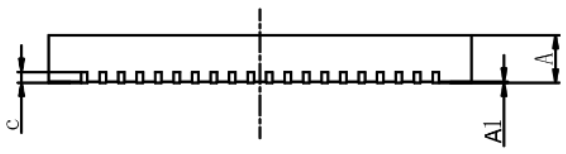
Figure 8-3 R128 Package Dimension of R128-S1, R128-S2, and R128-S3



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0. 90	0.95
A1	0	0.0 2	0.05
b	0.10	0.15	0.20
b1	0.12REF		
c	0.20 3REF		
D	7.90	8.00	8.10
D2	4.94	5.04	5.14
e	0.35BSC		
Ne	6.65BSC		
Nd	6.65BSC		
E	7.90	8.00	8.10
E2	5.34	5.44	5.54
L	0.35	0. 40	0.45
L1	0.29	0. 39	0.49
h	0.30	0.35	0.40
K	0.88REF		
K2	1.08REF		

9 Carrier, Storage and Baking Information

9.1 Carrier

Matrix Tray Information

The following table shows the R128 matrix tray carrier information.

Table 9-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315mm x 136mm x 7.62mm	348 Qty/Tray
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm	Surface impedance:$10^9\Omega$ Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm	
Inner Box	White	396mm x 196mm x 96mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420mm x 410mm x 320mm	6 Inner box/Carton

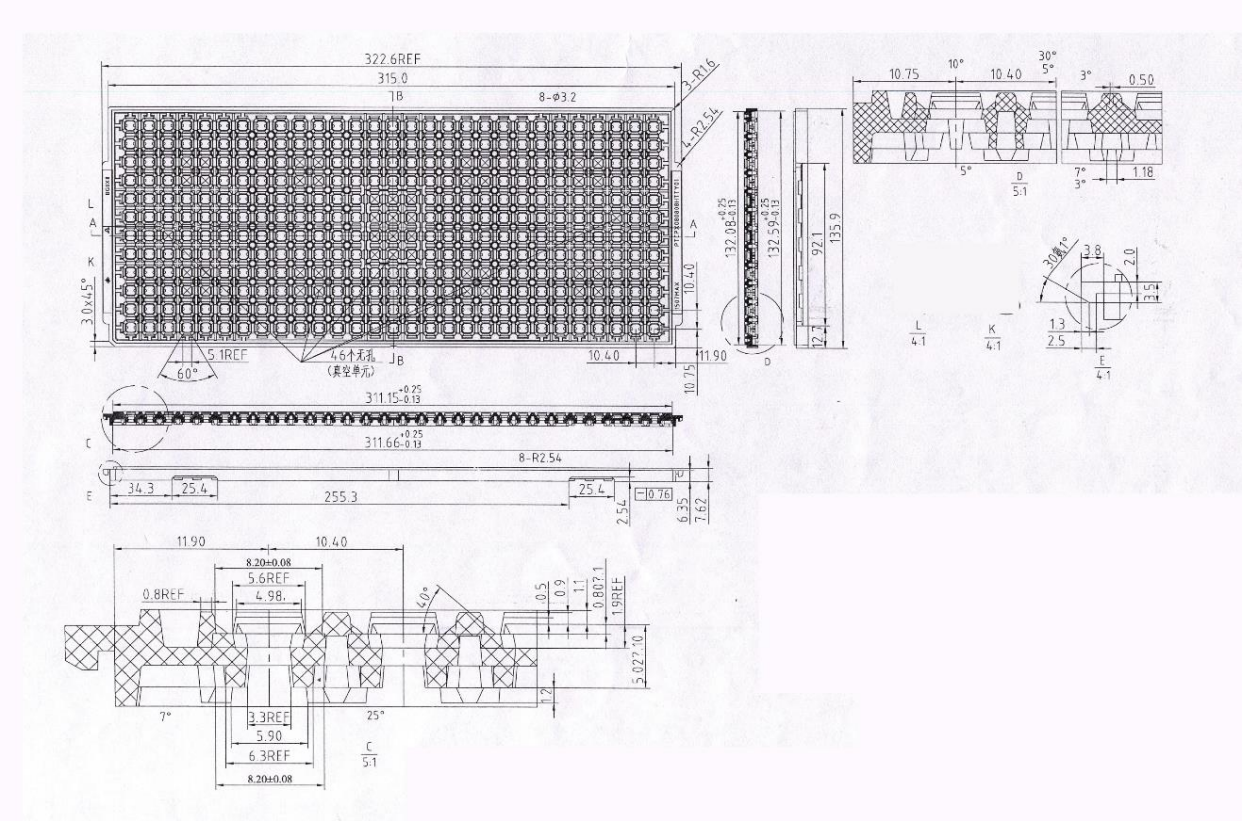
The following table shows the R128 packing quantity.

Table 9-2 R128 Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
R128-S1 /R128-S 2/R128-S3	8 x 8	348	10	3480	6	20880

Figure 9-1 shows tray dimension drawing of the R128.

Figure 9-1 Tray Dimension Drawing



9.2 Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

9.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined as below.

Table 9-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The R128 device samples are classified as MSL3.

9.2.2 Bagged Storage Conditions

The shelf life of the R128 device samples are defined as below.

Table 9-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

9.2.3 Out-of-bag Duration

It is defined by the device MSL rating, and the out-of-bag duration of the R128 is as follows.

Table 9-5 Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

9.3 Baking

It is not necessary to bake the R128 if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the R128 if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake the R128 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the sample baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

10 FT and IQC Test

10.1 FT Test

FT test includes two parts, module verification and Linux system testing. For module verification, it verifies the logic function of each module; for Linux system testing, it mainly tests CPU, DDR, memory test and linpack, etc. The Linux system testing can cover areas where module verification does not cover, with the goal of increasing coverage as much as possible.

10.2 IQC Test

IQC test system is used for sampling inspection before delivery, it is the final test for chip shipment before delivery to the customer. IQC test system includes QA test and QC test.

10.2.1 QA Test

QA test is a testing for each function module of chip by writing the Linux system firmware similar to terminal client into SPI nor flash, which can judge whether chip can reach production standard by system total running results, single module testing fluency.

10.2.2 QC Test

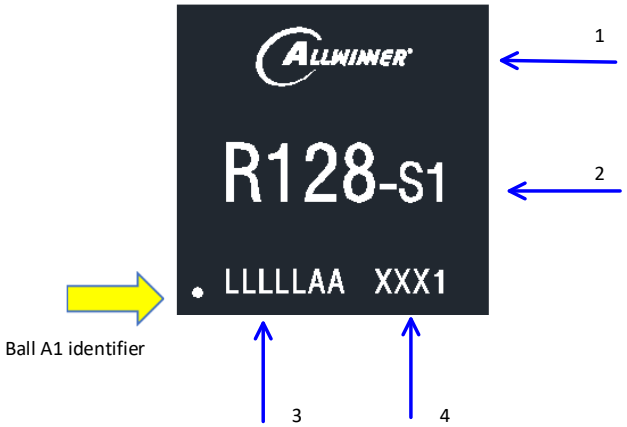
QC test is used to test each module code booting from SPI nor flash, and run schedule by using PC control code, then read the return value of each module testing. If the return value is PASS, then continue to perform the next module testing; or else stop testing and remind the testing module FAIL.

11 Part Marking

11.1 R128-S1

The following figure shows the R128-S1 marking.

Figure 11-1 R128-S1 Marking



The following table describes the R128-S1 marking definitions.

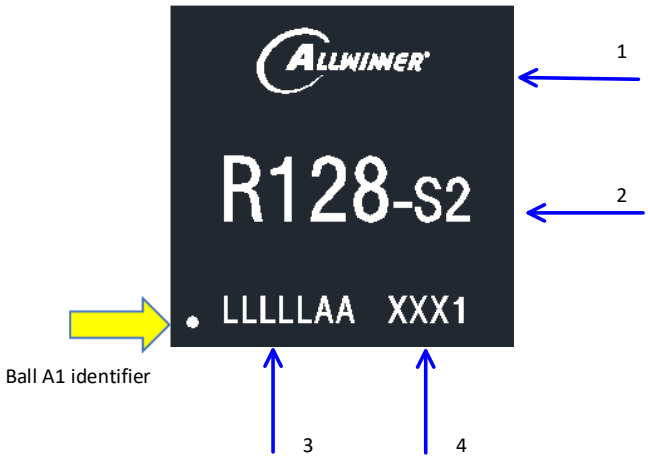
Table 11-1 R128-S1 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R128-S1	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

11.2 R128-S2

The following figure shows the R128-S2 marking.

Figure 11-2 R128-S2 Marking



The following table describes the R128-S2 marking definitions.

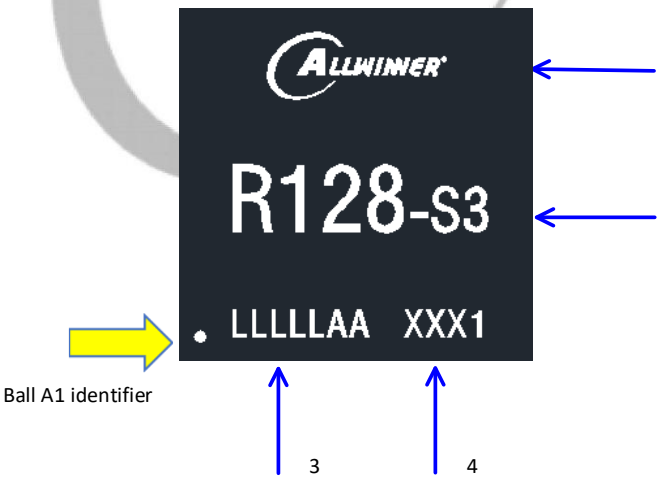
Table 11-2 R128-S2 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	R128-S2	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

11.3 R128-S3

The following figure shows the R128-S3 marking.

Figure 11-3 R128-S3 Marking



The following table describes the R128-S3 marking definitions.

Table 11-3 R128-S3 Marking Definitions

No.	Marking	Description	Fixed/Dynamic

1	ALLWINNER	Allwinner logo or name	Fixed
2	R128-S3	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

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