AXP813 Datasheet

AXP813 Optimized For Multi-Core High-Performance System

Revision 1.2

2015.11.05

Revision History

Revision	Date	Description
Rev 1.0	2014.09.01	Release Version1.0
Rev 1.1	2014.12.20	Change REG 24H(DCDC5 voltage control)
Rev 1.2	2015.11.05	Revise the ball number of LRCK2 in Ball Description

Declaration

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Catalog

1 Overview

The AXP813 is a high integrated power management and audio Codec integrated circuit available in 11mm x 11mm 218-ball BGA package. The device contains power management, audio codec, USB3.0-compatible Flash Charger, real-time clock(RTC), analog to digital converter(ADC) and hardware DSP.

AXP813 integrates power management subsystem for applications powered by one Li-battery(Li-ion or Li-polymer) ,and which requires multiple power rails. The AXP813 provides 21 channels power outputs (including 7-CH Bucks) and multiple channels 12-bit ADC for voltage/current/temperature monitor and integrates protection circuits such as OVP, UVP, OTP, and OCP to ensure the security and stability of the power system. The portion of power management also features a unique E-Gauge™(Fuel Gauge) system, making power gauge easy and exact.

An IPS™ (Intelligent Power Select) circuit is included to transparently select the type of charger and provide charging with USB3.0-compatible chargers(up to 2.8A charge current), external AC chargers, and Li-battery.

In addition, AXP813 embraces a fast interface for the system to dynamically adjust output voltage and enable power outputs so that the battery life can be extended to the largest extent.

An integrated digital PLL supports a large range of input/output frequencies, and It can generate required audio clocks for codec from standard audio crystal rate such as 22.5792MHz and 24.576MHz, also can be from common reference clock frequencies such as 12MHz, 13MHz and 19.2MHz, and an internal RC oscillator can be used in Free-running Mode, where the application processor can be inactive during voice call application. The 2 ADC and 2 DAC in device use advanced multi-bit delta-sigma modulation technique to convert data between analog and digital. The SNR performance can reach 100 dB A-weight.

A mono, differential BTL drive amplifier is available for driving the handset receiver.

The flexible analogue and digital mixers form a varied signal routing to support a complicated application.

All LDOs and DCDC is controlled through TWSI(2-wire serial interface) or RSB① (reduced serial bus) to convert voltage. It works only in the slave mode .

The integrated DRC(Dynamic Range Controller) function in AXP813 provide an useful digital sound processing capability in DAC playback path to speaker . It is used to attenuate the peak signals and boost the low-level signals by adjusting the output signal gain in some conditions. The DRC functions can be enable or disable in the playback path .

The integrated AGC(Automatic Gain Controller) function can be used to maintain a constant recording level in ADC record path. The DRC can make an improvement in background noise by setting a programmable Noise Gate to attenuate very low-level input signals .

Note: ① The RSB is independent R&D by x-powers, supports a special protocols with a simplified two wire protocol on a push-pull bus. The transfer speed in AXP813 can be up to 10MHz .

Applications :

• Tablet, Smart phone, DVR, Desktop, Dongle

• UMPC-like, Student Computer

2 Feature

--7 Frequency spread Bucks

- DCDC4: PFM/PWM, 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM
- DCDC7: PFM/PWM, 0.6-1.10V, 10mV/step, 1.12-1.52V, 20mV/step, IMAX=1.8A, DVM
- DCDC6: PFM/PWM, 0.6-1.10V, 10mV/step, 1.12-1.52V, 20mV/step, IMAX=2.5A, DVM
- DCDC5: PFM/PWM, 0.8-1.12V, 10mV/step, 1.14-1.84V, 20mV/step, IMAX=2.5A, DVM, default set by DC5SET
- DCDC2: PFM/PWM, 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM,
- DCDC3: PFM/PWM, 0.5-1.20V, 10mV/step, 1.22-1.30V, 20mV/step, IMAX=3A, DVM,
- DCDC1: PFM/PWM, 1.6-3.4V, 0.1V/step, 19 steps, IMAX=1.5A
- DCDC2/3/4:71+5 steps; DCDC6/7:51+21steps; DCDC5:33+37 steps
- DVM(Dynamic Voltage scaling Management) ramp rate: 2.5mV/us at buck frequency 3MHz

--15 LDOs & Switch

- RTCLDO: VCC_RTC=3V, IMAX=60mA, always enable
- ALDO1: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=500mA, input is ALDOIN
- ALDO2: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=300mA, input is ALDOIN
- ALDO3: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=200mA, input is ALDOIN
- DLDO1: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps; IMAX=500mA, input is DLDOIN
- DLDO2: Analog LDO, 0.7-3.4V, 100mV/step; 28 steps; 3.4-4.2V, 200mV/step, 5 steps. IMAX=400mA, input is DLDOIN
- DLDO3: Analog LDO, 0.7-3.3V, 100mV/step; 27 steps, IMAX=300mA, input is DLDOIN
- DLDO4: Analog LDO, 0.7-3.3V, 100mV/step; 27 steps, IMAX=500mA, input is DLDOIN
- ELDO1: Digital LDO, 0.7-1.9V, 50mV/step; 25 steps, IMAX=400mA, input is ELDOIN
- ELDO2: Digital LDO, 0.7-1.9V, 50mV/step; 25 steps, IMAX=200mA, input is ELDOIN
- ELDO3: Digital LDO, 0.7-1.9V, 50mV/step; 25 steps, IMAX=200mA, input is ELDOIN
- FLDO1: Digital LDO, 0.7-1.45V, 50mV/step, 16 steps, IMAX=300mA, input is FLDOIN
- FLDO2: Digital LDO, 0.7-1.45V, 50mV/step, 16 steps, IMAX=100mA, input is FLDOIN
- FLDO3: Sink and Source LDO, FLDOIN/2, DCDC5/2, IMAX=30mA, input is FLDOIN, for VREFDQ, default on
- GPIO0LDO: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=100mA, input is ALDOIN
- GPIO1LDO: Analog LDO, 0.7-3.3V, 100mV/step, 27 steps, IMAX=150mA, input is ALDOIN
- CHGLED: GND switch for motor or LED, IMAX=100mA

--TWI/RSB control interface supporting standard and quick slave mode

--Intelligent Power Select (IPS), VBUS-IPSOUT is 80mΩ typically

--Adaptive Li battery PWM charger with current total up to 2.8A

--Battery Fuel Gauge and coulomb counter

--Power output on/off touch key

--Internal Temperature sensor and protection

--Safe and Soft start up

--2 ADCs and 2 DACs @ 24-bit and inter PLL processing with flexible clocking scheme

--Up to 100dB SNR during DAC playback path (A ' weight)

--Up to 95dB SNR during ADC record path (A ' weight)

--Capless stereo headphone driver

- Integrated charge pump for 0V reference
- 18mW @1.8V

--Mono differential earpiece driver

- 65 mW/CH (THD+N ≤ -70dB, 16Ohm Load)

--Two stereo differential speaker outputs using external amplifier to drive the loud speaker

--Differential Line output with 1 Vrms full scale output voltage

--Mono differential earpiece driver

- Three differential analog microphone inputs with 30dB~48dB boost amplifier gain
- One mono differential or single-ended line-in input
- One stereo auxiliary input for external accessory connection

--Two low noise analog microphone bias

--Audio jack insert/ button press detection

--24-bit 8KHz ~ 192KHz I2S/PCM interface

--Support Dynamic Range Controller (DRC) adjusting the DAC playback output

--Support Automatic Gain Control (AGC) adjusting the ADC recording output

--SRC for synchronisation between audio interface or digital audio data mixing

--Soft mute circuit for pop noise suppression

--Support digital microphone interface

-- RTC and Three clock output

3 Power Management Typical Application

Figure 3-1 shows the typical application of the power management.

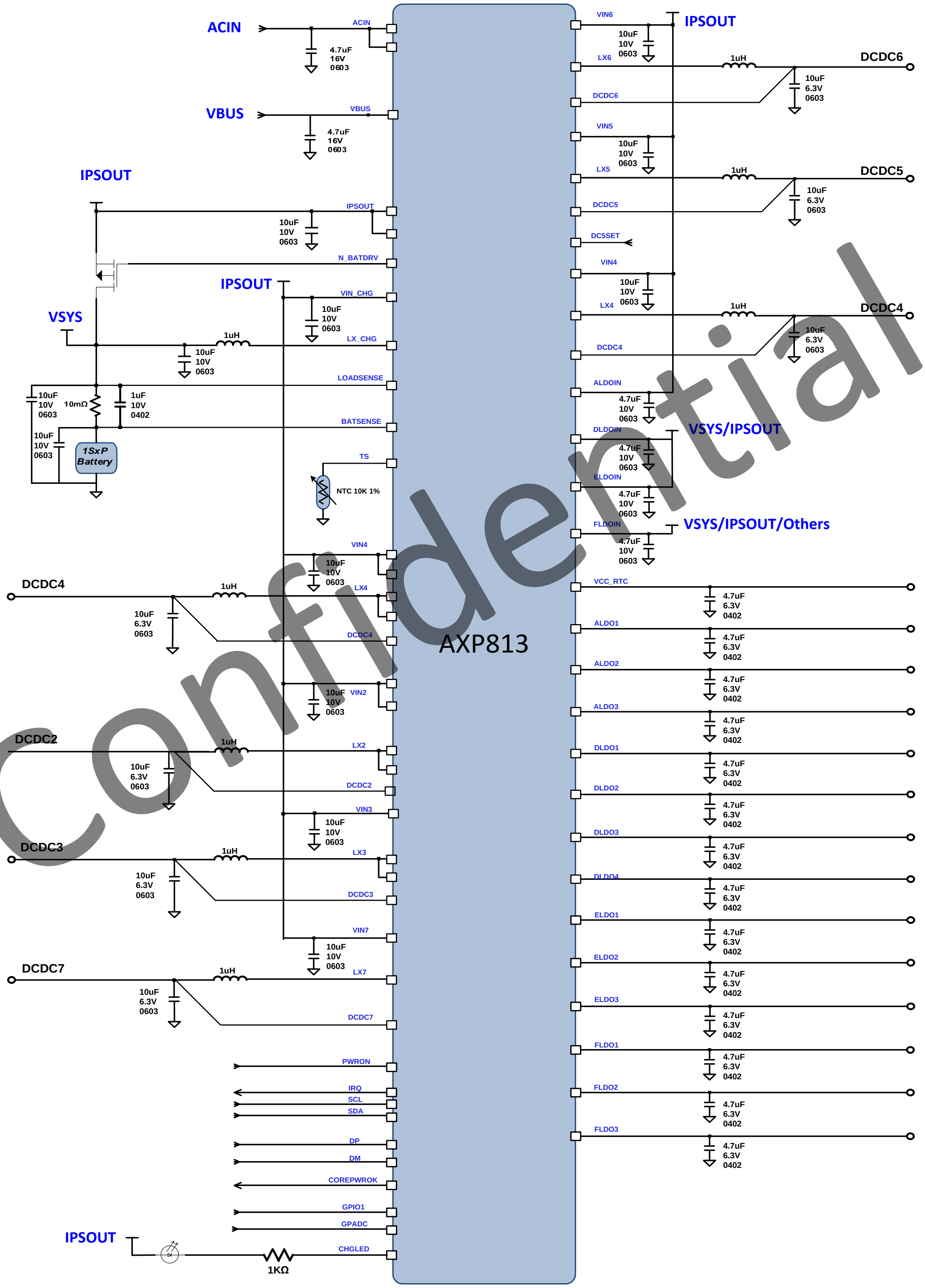

Figure 3-1 Power Management

4 Ball Map

Figure 4-1 shows the top pin maps views of the 218-pin BGA package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	EAROUTP	LINEOUTN	LINEINR	MIC2P	MIC1P	AXIR	MIC3N	LDOIN	VDD_CORE	X32KO	IRQ_RTC					
B	EAROUTN	LINEOUTP	LINEINL	MIC2N	MIC1N	AXIL	MIC3P	CKO3_RTC	X32KI	SCK_A						
C	SPORP	AVCC	AGND	VRP	HBIAS	MBIAS	CKO2_RTC	CKO1_RTC	SDA_A			LX6		LX5		
D	SPOLP	SPORN	AGND	GND_A	GND_A	GND_A	GND_A	VCC_RTC_A				LX6		LX5	FLDO3	ELDO2
E	VRA2	SPOLN	AGND	GND_A	GND_A		GND_A		DLDOIN	DLDO4		DCDC6			FLDO1	ELDO3
F	VEE	HPOUTFB	GND_A	GND_A	GND_A	GND_A	DLDO1	DLDO2		DLDO3	VIN6	DCDC5	VIN5	FLDO2	FLDOIN	ELDOIN
G	CPVEE	HPOUTL	GND_A	GND_A	GND_A	GND_A	GND	PGND6	PGND6	GND	PGND5	PGND5	GND	PGND7	ELDO1	DCDC7
H	HPOUTR	VPP	GND_A	GND_A	GND_A	GND_A	GND	GND	GND	GND	GND	GND	GND	PGND7	LX7	VIN7
J	DACDAT3	VCC_IO2	LRCK3		SWOUT	SWIN	GND	GND	GND	GND	GND	GND	GND	PGND_CHG	VIN_CHG	VIN_CHG
K	ADCDAT3	BCLK3				DCDC1	PGND1	GND	GND	GND	GND	GND	GND	PGND_CHG	LX_CHG	LX_CHG
L	IRQ_AUDIO	DACDAT2			LX1	VIN1	PGND4	GND	GND	GND	GND	GND	GND	GND	BATSENSE	LOADSENSE
M	ADCDAT2	LRCK2			VIN4	VIN4	PGND4	GND	GND	GND	GND	GND	GND	GND	PWRON	DC5SET
N	BCLK2	VCC_IO1		DCDC4		LX4	GND	GND	GND	GND	GND	GND	GND	GND	ACIN	ACIN
P	DACDAT1	ADCDAT1		FBGND	GND	LX4	GND	PGND3	PGND3	PGND2	PGND2	GND	GND	GND	PS	PS
R	LRCK1	BCLK1		DM	TS	ALDO1	ALDOIN	LX3	LX3	VIN2	DCDC3	LX2	SDA	SCK	CHGLED	VBUS
T	MCLK2	MCLK1	DP	ALDO2	ALDO3	VREF	GPIO1	GPIO0	VIN3	VIN2	DCDC2	LX2	PWROK	VCC_RTC	N_BATDRV	N_VBUSEN

Figure 4-1 AXP813 Pin Maps

5 Ball Description

Table 5-1 lists the characteristics of the AXP813 Pins.

Table 5-1

Ball	Name	Type	Condition	Description
G15	ELDO1	O		Output pin of ELDO1
D16	ELDO2	O		Output pin of ELDO2
E16	ELDO3	O		Output pin of ELDO3
E15	FLDO1	O		Output Pin of FLDO1
F15	FLDOIN	PI		FLDO input source
F14	FLDO2	O		Output Pin of FLDO2
D15	FLDO3	O		Output Pin of FLDO3
F13	VIN5	PI		DCDC5 input source
C14	LX5	IO		Inductor Pin for DCDC5
D14	LX5	IO		Inductor Pin for DCDC5
F12	DCDC5	I		DCDC5 feedback pin
G11	PGND5	G		PGND Of DCDC5
G12	PGND5	G		PGND Of DCDC5
E12	DCDC6	I		DCDC6 feedback pin
C12	LX6	IO		Inductor Pin for DCDC6
D12	LX6	IO		Inductor Pin for DCDC6
F11	VIN6	PI		DCDC6 input source
G8	PGND6	G		PGND Of DCDC6
G9	PGND6	G		PGND Of DCDC6
E10	DLDO4	O		Output Pin of DLDO4
F10	DLDO3	O		Output Pin of DLDO3
E9	DLDOIN	PI		DLDOIN input source
F8	DLDO2	O		Output Pin of DLDO2
F7	DLDO1	O		Output Pin of DLDO1
J5	SWOUT	PO		Output Pin of The PMOS Switch
J6	SWIN	PI		Input Pin of The PMOS Switch
L6	VIN1	PI		DCDC1 input source
L5	LX1	IO		Inductor Pin for DCDC1
K6	DCDC1	I		DCDC1 feedback pin
K7	PGND1	G		PGND Of DCDC1
M5	VIN4	PI		DCDC4 input source
M6	VIN4	PI		DCDC4 input source

Ball	Name	Type	Condition	Description
N6	LX4	IO		Inductor Pin for DCDC4
P6	LX4	IO		Inductor Pin for DCDC4
N4	DCDC4	I		DCDC4 feedback pin
L7	PGND4	G		PGND Of DCDC4
M7	PGND4	G		PGND Of DCDC4
P4	FBGND	G		Feedback pin of PGND2
T3	DP	I		Charger detection, USB D+
R4	DM	I		Charger detection, USB D-
R6	ALDO1	O		Output pin of ALDO1
T4	ALDO2	O		Output pin of ALDO2
R5	TS	I		Battery Temperature Sensor Input or an External ADC Input
T5	ALDO3	O		Output pin of ALDO3
R7	ALDOIN	PI		ALDO input source
T6	VREF	O		Internal reference voltage
T7	GPIO1	IO		General purpose I/O or LDO by REG92H. When it's digital input, the logic high level is 1.5V, and the logic low level is 0.5V typically. When it's digital output, the logic high level is decided by REG93H.
T8	GPIO0	I		General purpose I/O/ADC input or LDO by REG90H. When it's digital input, the logic high level is 1.5V, and the logic low level is 0.5V typically. When it's digital output, the logic high level is decided by REG91H.
R8	LX3	IO		Inductor Pin for DCDC3
R9	LX3	IO		Inductor Pin for DCDC3
T9	VIN3	PI		DCDC3 input source
R11	DCDC3	I		DCDC3 feedback pin
P8	PGND3	G		PGND Of DCDC3
P9	PGND3	G		PGND Of DCDC3
R10	VIN2	PI		DCDC2 input source
T10	VIN2	PI		DCDC2 input source
T11	DCDC2	I		DCDC2 feedback pin
R12	LX2	IO		Inductor Pin for DCDC2
T12	LX2	IO		Inductor Pin for DCDC2
P10	PGND2	G		PGND Of DCDC2
P11	PGND2	G		PGND Of DCDC2

Ball	Name	Type	Condition	Description
T13	PWROK	O		Power Good pin, push-pull output , and pull to VCC_RTC internal. PWROK is an active high dedicated output signal. PWROK asserts when all voltage rails to the SOC that are supposed to be on
R14	SCK	I	2.2KΩ Pull High	Clock pin for serial interface, need a 2.2KΩ Pull High.
R13	SDA	IO	2.2KΩ Pull High	Data pin for serial interface, need a 2.2KΩ Pull High.
T14	VCC_RTC	O		Output pin of VCC_RTC
R16	VBUS	PI		VBUS input
T15	N_BATDRV	O		BAT to PS extern PMOS driver
T16	N_VBUSEN	IO		VBUS-PS Path Control pin
R15	CHGLED	O		Charger status indication
P15	PS	PO		System power source
P16	PS	PO		System power source
N15	ACIN	PI		ACIN input
N16	ACIN	PI		ACIN input
M15	PWRON	I		Power On-Off key input， Internal 100k pull high to VINT pin
M16	DC5SET	I		Setting DCDC5 default Output Voltage, this pin must tied to GND/VCC_RTC or floating.
L16	LOADSENSE	I		PWM Charger Current Sense Resistance Positive Input
L15	BATSENSE	I		PWM Charger Current Sense Resistance Negative Input
K15	LX_CHG	IO		Inductor Pin for PWM Charger
K16	LX_CHG	IO		Inductor Pin for PWM Charger
J15	VIN_CHG	I		Charger input source
J16	VIN_CHG	I		Charger input source
J14	PGND_CHG	G		PGND Of Charger
K14	PGND_CHG	G		PGND Of Charger
H15	LX7	IO		Inductor Pin for DCDC7
H16	VIN7	PI		DCDC7 input source
G16	DCDC7	I		Feedback to DCDC7
G14	PGND7	G		PGND Of DCDC7
H14	PGND7	G		PGND Of DCDC7
F16	ELDOIN	PI		ELDO input source
G7	GND	G		GND Of Power Management

Ball	Name	Type	Condition	Description
G10	GND	G		GND Of Power Management
G13	GND	G		GND Of Power Management
H7	GND	G		GND Of Power Management
H8	GND	G		GND Of Power Management
H9	GND	G		GND Of Power Management
H10	GND	G		GND Of Power Management
H11	GND	G		GND Of Power Management
H12	GND	G		GND Of Power Management
H13	GND	G		GND Of Power Management
J7	GND	G		GND Of Power Management
J8	GND	G		GND Of Power Management
J9	GND	G		GND Of Power Management
J10	GND	G		GND Of Power Management
J11	GND	G		GND Of Power Management
J12	GND	G		GND Of Power Management
J13	GND	G		GND Of Power Management
K8	GND	G		GND Of Power Management
K9	GND	G		GND Of Power Management
K10	GND	G		GND Of Power Management
K11	GND	G		GND Of Power Management
K12	GND	G		GND Of Power Management
K13	GND	G		GND Of Power Management
L8	GND	G		GND Of Power Management
L9	GND	G		GND Of Power Management
L10	GND	G		GND Of Power Management
L11	GND	G		GND Of Power Management
L12	GND	G		GND Of Power Management
L13	GND	G		GND Of Power Management
M8	GND	G		GND Of Power Management
M9	GND	G		GND Of Power Management
M10	GND	G		GND Of Power Management
M11	GND	G		GND Of Power Management
M12	GND	G		GND Of Power Management
M13	GND	G		GND Of Power Management
M14	GND	G		GND Of Power Management
N7	GND	G		GND Of Power Management

Ball	Name	Type	Condition	Description
N8	GND	G		GND Of Power Management
N9	GND	G		GND Of Power Management
N10	GND	G		GND Of Power Management
N11	GND	G		GND Of Power Management
N12	GND	G		GND Of Power Management
N13	GND	G		GND Of Power Management
N14	GND	G		GND Of Power Management
P5	GND	G		GND Of Power Management
P7	GND	G		GND Of Power Management
P12	GND	G		GND Of Power Management
P13	GND	G		GND Of Power Management
P14	GND	G		GND Of Power Management
T2	MCLK1	I		I2S interface master input clock 1
P1	SDIN1	I		First I2S interface serial data input
P2	SDOUT1	O		First I2S interface serial data output
R2	BCLK1	I/O		First I2S interface serial bit clock
R1	LRCK1	I/O		First I2S interface synchronous clock
T1	MCLK2	I		I2S interface master input clock 2
L2	SDIN2	I		Second I2S interface serial data input
M1	SDOUT2	O		Second I2S interface serial data output
N1	BCLK2	I/O		Second I2S interface serial bit clock
M2	LRCK2	I/O		Second I2S interface synchronous clock
J1	SDIN3	I		Third I2S interface serial data input
K1	SDOUT3	O		Third I2S interface serial data output
K2	BCLK3	I/O		Third I2S interface serial bit clock
J3	LRCK3	I/O		Third I2S interface synchronous clock
C9	SDA_A	I/O		TWSI interface serial data(Open-drain) Of Codec RSB interface serial data Of Codec
B10	SCK_A	I		TWSI interface serial clock input Of Codec RSB interface serial clock input Of Codec
L1	IRQ_AUDIO	O		IRQ for accessory insert and button detect(Open-drain)
A11	IRQ_RTC	O		IRQ for RTC alarm interrupt…(Open-drain)
B9	X32KI	I		The external oscillator input signal
A10	X32KO	O		The external oscillator output signal
C8	CKO1_RTC	O		RTC 32.768 KHz clock output(Push-pull)

Ball	Name	Type	Condition	Description
C7	CKO2_RTC	O		RTC 32.768 KHz clock output(Open-drain)
B8	CKO3_RTC	O		RTC 32.768 KHz clock output(Open-drain)
A5	MIC1P	I		Positive differential input for MIC1
B5	MIC1N	I		Negative differential input for MIC1
A4	MIC2P	I		Positive differential input for MIC2
B4	MIC2N	I		Negative differential input for MIC2
B7	MIC3P/ DMICCLK	I O		Analog Positive differential input for MIC3 Digital microphone clock output
A7	MIC3N/ DMICDAT	I O		Negative differential input for MIC3 Digital microphone data input
B3	LINEINL	I		Left single-end or differential input for LINE-IN
A3	LINEINR	I		Right single-end or differential input for LINE-IN
B6	AXIL	I		Auxiliary left Channel input
A6	AXIR	I		Auxiliary right Channel input
G2	HPOUTL	O		Headphone amplifier left channel output
H1	HPOUTR	O		Headphone amplifier right channel output
D1	SPOLP	O		Differential positive output to speaker1 amplifier
E2	SPOLN	O		Differential negative output to speaker1 amplifier
C1	SPORP	O		Differential positive output to speaker2 amplifier
D2	SPORN	O		Differential negative output to speaker2 amplifier
A1	EAROUTP	O		Earpiece amplifier positive differential output
B1	EAROUTN	O		Earpiece amplifier negative differential output
B2	LINEOUTP	O		Positive output for LINE-OUT
A2	LINEOUTN	O		Negative output for LINE-OUT
C6	MBIAS	O		First bias voltage output for main microphone
C5	HBIAS	O		Second bias voltage output for headset microphone
F2	HPOUTFB	I		Pseudo differential headphone ground reference
E1	VRA2	O		Internal reference voltage
C4	VRP	O		Internal reference voltage
C2	AVCC	P		Analog power
C3	AGND	G		Analog ground
D3	AGND	G		Analog ground
E3	AGND	G		Analog ground
H2	VPP	P		Analog power for headphone charge pump
G1	CPVEE	P		Charge pump negative decoupling Pin
F1	VEE	P		Headphone PA negative voltage input

Ball	Name	Type	Condition	Description
A9	VDD_CORE	P		Digital power for digital core
N2	VCC_IO1	P		Digital power for digital I/O buffer（I2S1&I2S2）
J2	VCC_IO2	P		Digital power for digital I/O buffer（I2S3）
A8	LDOIN	P		Input power for Audio_LDO
D8	VCC_RTC_A	P		Input power for RTC_LDO
D4	GND_A	G		GND Of Codec
D5	GND_A	G		GND Of Codec
D6	GND_A	G		GND Of Codec
D7	GND_A	G		GND Of Codec
E4	GND_A	G		GND Of Codec
E5	GND_A	G		GND Of Codec
E7	GND_A	G		GND Of Codec
F3	GND_A	G		GND Of Codec
F4	GND_A	G		GND Of Codec
F5	GND_A	G		GND Of Codec
F6	GND_A	G		GND Of Codec
G3	GND_A	G		GND Of Codec
G4	GND_A	G		GND Of Codec
G5	GND_A	G		GND Of Codec
G6	GND_A	G		GND Of Codec
H3	GND_A	G		GND Of Codec
H4	GND_A	G		GND Of Codec
H5	GND_A	G		GND Of Codec
H6	GND_A	G		GND Of Codec

6 Block Diagram

6.1 Power management Block Diagram

Figure 6-1 shows the block diagram of the power management.

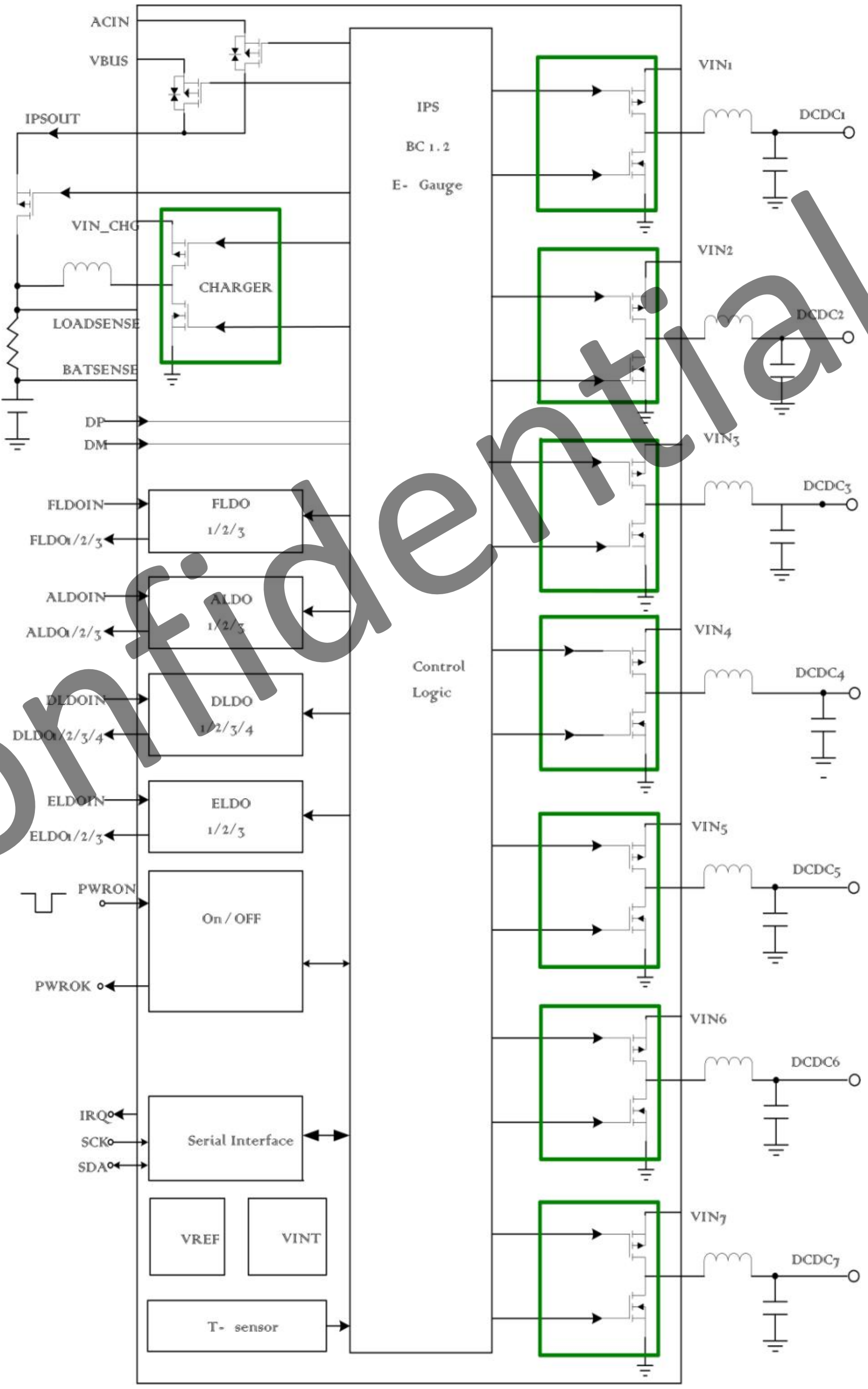

Figure 6-1 Power Management Block Diagram

6.2 Codec Functional Block Diagram

Figure 6-2 shows the block diagram of the codec.

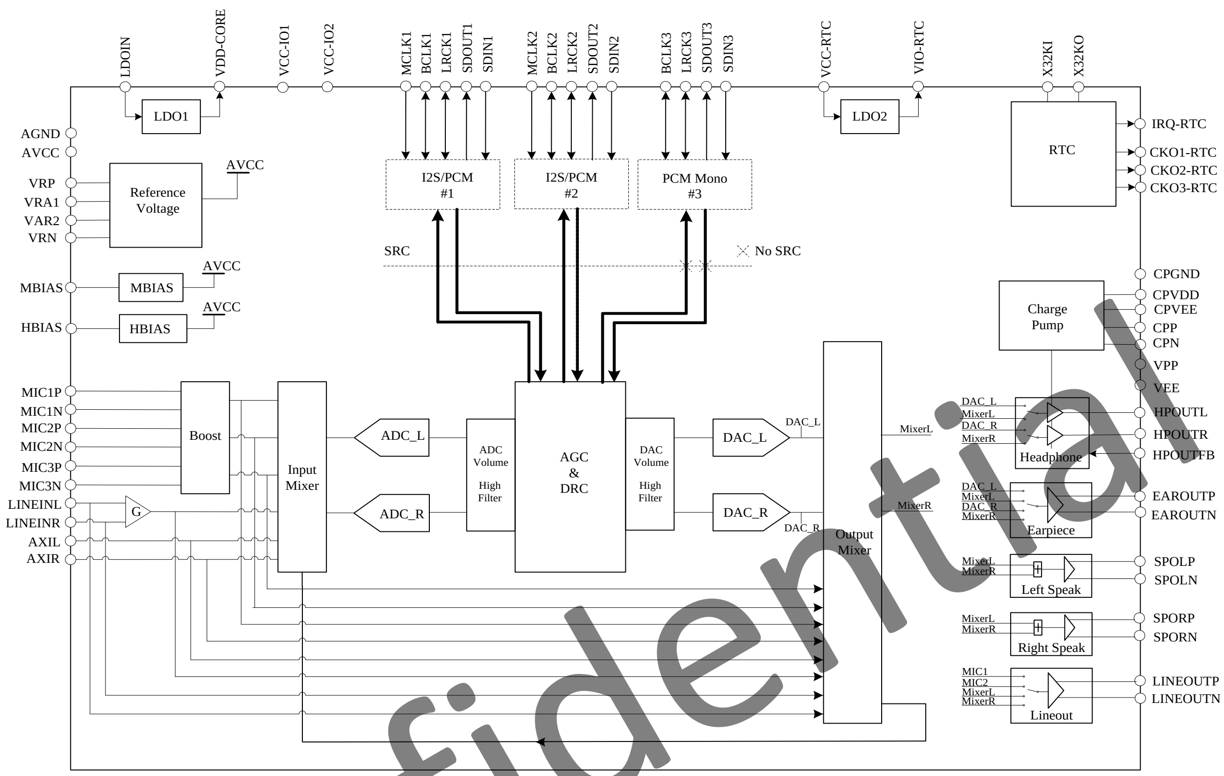

Figure 6-2 Codec Block Diagram

6.3 Codec Data Path Diagram

Figure 6-3 shows the codec data path diagram.

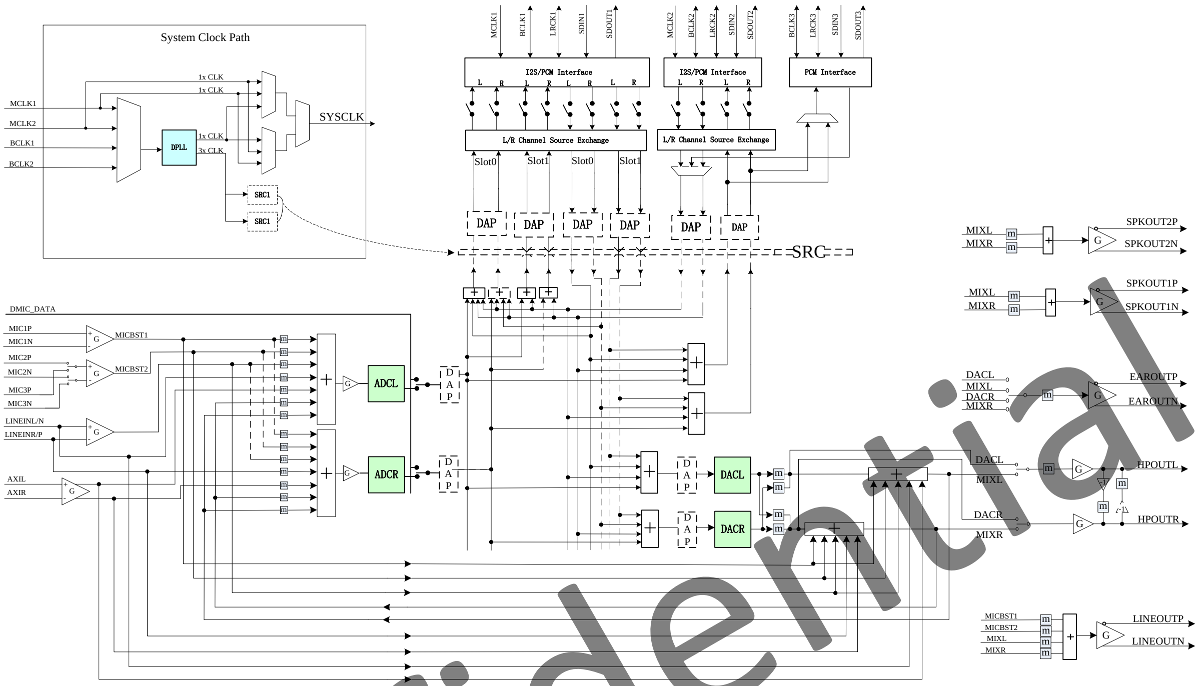

Figure 6-3 Codec Data Path Diagram

7 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 7-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 7-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	VALUE	UNITS
VBUS	Input Voltage Range	-0.3 to 11	V
V_{RIO1}	Voltage Range on pins PWROK	-0.3 to 5.5	V
V_{RIO2}	Voltage Range on pins SCK, SDA, GPIO0, GPIO1,	-0.3 to IPSOUT+0.3	V
V_{RIO3}	Voltage Range on pin PWRON	-0.3 to 2.1	V
LDO_IN	LDO Input power for Audio CODEC	-0.3 to 3.63	V
VDD_CORE	Digital power for Audio digital core, it can be generate by inner LDO	-0.3 to 1.32	V
VCC_IO1	Digital power for digital I/O buffer (I2S1&I2S2)	-0.3 to 3.63	V
VCC_IO2	Digital power for digital I/O buffer (I2S1&I2S3)	-0.3 to 3.63	V
CPVDD	Analog power for headphone charge pump	-0.3 to 2.0	V
VCC_RTC	LDO Input power for RTC	-0.3 to 3.63	V
VIO_RTC	Digital power for RTC digital core, it can be generate by inner LDO	-0.3 to 1.32	V
T_j	Operating Junction Temperature Range	125	℃
T_A	Operating Temperature Range	-20 to 85	℃
Ts	Storage Temperature Range	-40 to 150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads， 10sec)	260	℃
V_{ESD}	Maximum ESD stress voltage， Human Body Model	>2000	V
P_D	Internal Power Dissipation	2700	mW

8 Electrical Characteristics

All AXP813 modules are used under the operating Conditions contained in Table 8-1.

Table 8-1 Operating Conditions

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
ACIN						
V_{IN}	ACIN Input Voltage		3.5		7	V
I_{OUT}	V_{OUT} Current Available		1500	1500	4000	mA
V_{UVLO}	ACIN Under Voltage Lockout			3.5		V
V_{OUT}	IPSOUT Output Voltage		2.9		5.0	V
R_{ACIN}	Internal Ideal Diode On Resistance	ACIN to IPSOUT		94		mΩ
VBUS						
V_{IN}	VBUS Input Voltage		3.5		7	V
I_{OUT}	V_{OUT} Current Available		100	500	4000	mA
V_{UVLO}	VBUS Under Voltage Lockout			3.5		V
V_{OUT}	IPSOUT Output Voltage		2.9		5.0	V
R_{VBUS}	Internal Ideal Diode On Resistance	VBUS to IPSOUT		125		mΩ
Battery Charger						
V_{TRGT}	BAT Charge Target Voltage		4.1	4.2	4.35	V
I_{CHRG}	Charge Current		200	1200	2800	mA
I_{TRKL}	Trickle Charge Current Ratio to I_{CHRG}	I_{CHRG} = 0.2A - 2.8A		10%		
V_{TRKL}	Trickle Charge Threshold Voltage			3.0		V
ΔV_{RECHG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{TARGET}		-100		mV
T_{TIMER1}	Charger Safety Timer Termination Time	Trickle Mode	40	50	70	min

T_{TIMER2}	Charger Safety Timer Termination Time	CC Mode	360	480	720	min
I_{END}	End of Charge Indication Current Ratio to I_{CHRG}	CV Mode	10%	10%	20%	mA
I_{TOLER}	The tolerance of charge current	I_{CHRG} = 0.2A - 2.8A	±3%	±5%	±10%	
V_{TOLER}	The tolerance of charge target voltage				±0.5%	
NTC						
$V_{LTF\text{-}work}$	Cold Temperature Fault Threshold Voltage For Battery Work		0	3.226	3.264	V
$V_{HTF\text{-}work}$	Hot Temperature Fault Threshold Voltage For Battery Work		0	0.282	3.264	V
$V_{LTF\text{-}charge}$	Cold Temperature Fault Threshold Voltage For Battery Charge		0	2.112	3.264	V
$V_{HTF\text{-}charge}$	Hot Temperature Fault Threshold Voltage For Battery Charge		0	0.397	3.264	V
Off Mode Current						
I_{BATOFF}	OFF Mode Current	BAT=3.7V		40		μA
BUCK						
f_{OSC}	Oscillator Frequency	Default		3		MHz
L	Inductor value			1.0		μH
DCDC4						
I_{VIN4}	Input Current	PFM Mode I_{DCDC4} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		3900		mA
I_{DCDC4}	Available Output Current	PWM Mode		3000		mA
V_{DCDC4}	Output Voltage		0.5	0.9	1.3	V
C_{OUT4}	Output capacitor value		10	10	110	μF
DCDC7						

I_{VIN7}	Input Current	PFM Mode I_{DCDC7} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		2300		mA
I_{DCDC7}	Available Output Current	PWM Mode		1800		mA
V_{DCDC7}	Output Voltage		0.6	OFF	1.52	V
C_{OUT7}	Output capacitor value		10	10	66	μF
DCDC6						
I_{VIN6}	Input Current	PFM Mode I_{DCDC6} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		3000		mA
I_{DCDC6}	Available Output Current	PWM Mode		2500		mA
V_{DCDC6}	Output Voltage		0.6	0.9	1.52	V
C_{OUT6}	Output capacitor value		10	10	66	μF
DCDC5						
I_{VIN5}	Input Current	PFM Mode I_{DCDC5} =0		40		μA
	Switch Current Limit of PMOS	PWM Mode		3000		mA
I_{DCDC5}	Available Output Current	PWM Mode		2500		mA
V_{DCDC5}	Output Voltage		0.8	1.24V	1.84	V
C_{OUT5}	Output capacitor value		10	10	66	μF
DCDC2						
I_{VIN2}	Input Current	PFM Mode I_{DCDC2} =0		50		μA
	Switch Current Limit of PMOS	PWM Mode		3900		mA
I_{DCDC2}	Available Output Current	PWM Mode		3000		mA
V_{DCDC2}	Output Voltage		0.5	0.9	1.3	V
C_{OUT2}	Output capacitor value		10	10	132	μF
DCDC3						

I_{VIN3}	Input Current	PFM Mode I_{DCDC3} =0		50		µA
	Switch Current Limit of PMOS	PWM Mode		3900		mA
I_{DCDC3}	Available Output Current	PWM Mode		3000		mA
V_{DCDC3}	Output Voltage		0.5	0.9	1.3	V
C_{OUT3}	Output capacitor value		10	10	132	µF
DCDC1						
I_{VIN1}	Input Current	PFM Mode I_{DCDC1} =0		40		µA
	Switch Current Limit of PMOS	PWM Mode		2000		mA
I_{DCDC1}	Available Output Current	PWM Mode		1500		mA
V_{DCDC1}	Output Voltage (3.3V for AXP813D)		1.6	3.3	3.4	V
C_{OUT1}	Output capacitor value		10	10	66	µF
RTCLDO (always on)						
V_{RTCLDO}	Output Voltage	I_{RTCLDO}=1mA		1.8		V
I_{RTCLDO}	Output Current			60		mA
ALDO1						
V_{ALDO1}	Output Voltage	I_{ALDO1}=1mA	0.7	1.8	3.3	V
I_{ALDO1}	Output Current			500		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{ALDO1}=3V,f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{ALDO1}=1.8V,I_{ALDO1}=10mA		40		µVRMS
ALDO2						
V_{ALDO2}	Output Voltage	I_{ALDO2}=1mA	0.7	1.8	3.3	V
I_{ALDO2}	Output Current			300		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{ALDO2}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{ALDO2}=1.8V,I_{ALDO2}=10mA		40		µVRMS

ALDO3						
V_{ALDO3}	Output Voltage	I_{ALDO1}=1mA	0.7	3.0	3.3	V
I_{ALDO3}	Output Current			200		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{ALDO3}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{ALDO3}=1.8V,I_{ALDO3}=10mA		40		µVRMS
DLDO1						
V_{DLDO1}	Output Voltage	I_{DLDO1}=1mA	0.7	OFF	3.3	V
I_{DLDO1}	Output Current			500		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{DLDO1}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO1}=1.8V,I_{DLDO1}=10mA		40		µVRMS
DLDO2						
V_{DLDO2}	Output Voltage	I_{DLDO2}=1mA	0.7	OFF	4.2	V
I_{DLDO2}	Output Current			400		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{DLDO2}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO2}=1.8V,I_{DLDO2}=10mA		40		µVRMS
DLDO3						
V_{DLDO3}	Output Voltage	I_{DLDO3}=1mA	0.7	OFF	3.3	V
I_{DLDO3}	Output Current			300		mA
I_Q	Quiescent Current			60		µA
PSRR	Power Supply Rejection Ratio	V_{DLDO3}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO3}=1.8V,I_{DLDO3}=10mA		40		µVRMS
DLDO4						
V_{DLDO4}	Output Voltage	I_{DLDO4}=1mA	0.7	OFF	3.3	V
I_{DLDO4}	Output Current			500		mA
I_Q	Quiescent Current			60		µA

PSRR	Power Supply Rejection Ratio	V_{DLDO4}=3V, f=1kHz		70		dB
e_N	Output Noise,20Hz-80KHz	V_{DLDO4}=1.8V,I_{DLDO4}=10mA		40		µVRMS
ELDO1						
V_{ELDO1}	Output Voltage (1.8V for AXP813D)	I_{ELDO1}=1mA	0.7	OFF	1.9	V
I_{ELDO1}	Output Current			400		mA
I_Q	Quiescent Current			35		µA
PSRR	Power Supply Rejection Ratio	V_{ELDO1}=1.2V, f=1kHz		65		dB
ELDO2						
V_{ELDO2}	Output Voltage	I_{ELDO2}=1mA	0.7	OFF	1.9	V
I_{ELDO2}	Output Current			200		mA
I_Q	Quiescent Current			35		µA
PSRR	Power Supply Rejection Ratio	V_{ELDO2}=1.2V, f=1kHz		65		dB
ELDO3						
V_{ELDO3}	Output Voltage	I_{ELDO3}=1mA	0.7	OFF	1.9	V
I_{ELDO3}	Output Current			200		mA
I_Q	Quiescent Current			35		µA
PSRR	Power Supply Rejection Ratio	V_{ELDO3}=1.2V, f=1kHz		65		dB
FLDO1						
V_{FLDO1}	Output Voltage	I_{FLDO1}=1mA	0.7	OFF	1.45	V
I_{FLDO1}	Output Current			300		mA
I_Q	Quiescent Current			35		µA
PSRR	Power Supply Rejection Ratio	V_{FLDO1}=1.2V, f=1kHz		65		dB
FLDO2						
V_{FLDO2}	Output Voltage	I_{FLDO2}=1mA	0.7	0.9	1.45	V
I_{FLDO2}	Output Current			100		mA
I_Q	Quiescent Current			35		µA
PSRR	Power Supply Rejection Ratio	V_{FLDO2}=1.2V, f=1kHz		65		dB
FLDO3						

V_{FLDO3}	Output Voltage	I_{FLDO3}=1mA		0.5*V_{DCDC5}(default) Or 0.5*V_{FLDOIN}		V
I_{FLDO3}	Output Current			30		mA
I_Q	Quiescent Current			35		μA
GPADC						
$V_{GPIO0LDO}$	Output Voltage	REG90H[2:0]=011, $I_{GPIO0LDO}$=1mA	0.7	OFF	3.3	V
$I_{GPIO0LDO}$	Output Current	REG90H[2:0]=011		100		mA
I_Q	Quiescent Current	REG90H[2:0]=011		35		μA
PSRR	Power Supply Rejection Ratio	REG90H[2:0]=011 V_{GPADC}=3V, f=1kHz		65		dB
GPIO1						
$V_{GPIO1LDO}$	Output Voltage	REG92H[2:0]=011, $I_{GPIO1LDO}$=1mA	0.7	OFF	3.3	V
$I_{GPIO1LDO}$	Output Current	REG92H[2:0]=011		150		mA
I_Q	Quiescent Current	REG92H[2:0]=011		35		μA
PSRR	Power Supply Rejection Ratio	REG92H[2:0]=011 V_{GPIO1}=3V, f=1kHz		65		dB
CHGLED						
R_{CHGLED}	Internal Ideal Resistance	Supply Voltage is 0.3V		2		Ω
TWSI						
V_{CC}	Input Supply Voltage		1.8	3.3		V
Addr	TWSI Slave Address (7 bits)			0x34		
f_{SCK}	Clock Operating Frequency			400		kHz
V_{IL}	SCK/SDA Logic Low Voltage	SDA is Open drain pin			0.3*V_{CC}	V
V_{IH}	SCK/SDA Logic Low Voltage	SDA is Open drain pin	0.7*V_{CC}			V
t_f	Clock Data Fall Time	2.2Kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2Kohm Pull High		100		ns
VINT						
V_{INT}	Internal power supply for logic circuit			1.8		V
Related IO: PWRON						

$R_{pull-up}$	Internal resister to VINT		50	100		KΩ
V_{IL}	Logic Low Voltage			0.5		V
V_{IH}	Logic High Voltage			1.3	2.1	V
Related IO: IRQ						
V_{IL}	Logic Low Voltage	IRQ is open drain output pin, pull up to IO power (V_{IO}) by 10KΩ			0.3	V
V_{IH}	Logic High Voltage		0.7*V_{IO}		V_{IO}	V
Related IO: PWROK						
V_{IL}	Logic Low Voltage	PWROK is push-pull output pin, pull up to V_{RTCLDO} internal			0.3	V
V_{IH}	Logic High Voltage		0.7* V_{RTCLDO}		V_{RTCLDO}	V
Related IO: GPADC						
V_{IL}	Logic Low Voltage	REG90H[2:0]=010, digital input		0.5		V
V_{IH}	Logic High Voltage			1.3		V
V_{IL}	Logic Low Voltage	REG90H[2:0]=000, drive low			0.3	V
V_{IH}	Logic High Voltage	REG90H[2:0]=001, drive high (high level set by REG91H)	0.7	3.3	3.3	V
Related IO: GPIO1						
V_{IL}	Logic Low Voltage	REG92H[2:0]=010, digital input		0.5		V
V_{IH}	Logic High Voltage			1.3		V
V_{IL}	Logic Low Voltage	REG92H[2:0]=000, drive low			0.3	V
V_{IH}	Logic High Voltage	REG92H[2:0]=001, drive high (high level set by REG93H)	0.7	3.3	3.3	V
Codec Power Supply Input						
LDO_IN	LDO Input power for Audio Codec		1.35	1.8/1.5	3.63	V
VDD_CORE	Digital power for Audio digital core, it can be generate by inner LDO		1.08	1.2	1.32	V
VCC_IO1	Digital power for digital I/O buffer (I2S1&I2S2)		--	1.8/3.3	3.63	V

VCC_IO2	Digital power for digital I/O buffer (I2S1&I2S3)		--	1.8/3.3	3.63	V
CPVDD	Analog power for headphone charge pump		1.2	1.8	1.98	V
VCC_RTC	LDO Input power for RTC		1.35	1.8/3.3	3.63	V
VIO_RTC	Digital power for RTC digital core, it can be generate by inner LDO		1.08	1.2	1.32	V
GND,AGND	Ground reference		--	0	--	V
Codec Static Characteristics						
V_{IN}	Input Voltage Range	--	-0.3	--	VCCIO1+0.3 VCCIO2+0.3	V
V_{IH}	High Level Input Voltage	VCCIO=3.0V	2.4	--	3.6	V
		VCCIO=1.8V	1.4	--	1.98	
V_{IL}	Low Level Input Voltage	VCCIO=3.0V	-0.3	--	0.7	V
		VCCIO=1.8V	-0.3	--	0.7	
V_{OH}	High Level Output Voltage	VCCIO=3.0V	2.7	--	NA	V
		VCCIO=1.8V	1.5	--	NA	
V_{OL}	Low Level Output Voltage	VCCIO=3.0V	NA	--	0.4	V
		VCCIO=1.8V	NA	--	0.4	
I_{OZ}	Tri-state Output Leakage Current	--	TBD	TBD	TBD	uA
C_{IN}	Input Capacitance	--	NA	NA	5	pF
C_{OUT}	Output Capacitance	--	NA	NA	5	pF

9 Analog Performance Characteristics

Table 9-1 summarizes the analog performance characteristics of AXP813.

Table 9-1 Analog Performance Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UINT
DAC Output Path Performance	**DAC to Headphone on HPOUTL or HPOUTR(R=10kΩ)**					
	FScale Output Level	0dB 1KHz		0.9		Vrms
	SNR(A-weighted)	0dB 1KHz		100		dB
	THD+N(NO-Aweight)	0dB 1KHz		-84		dB
	Crosstalk（L/R）	0dB 1KHz		-88/-88		dB
	DAC to Headphone on HPOUTL or HPOUTR(R=16Ω)					
	FScale Output Level	0dB 1KHz		0.5		Vrms
	SNR(A-weighted)	0dB 1KHz		99		dB
	THD+N(P0=15mW)	0dB 1KHz		-81		dB
	THD+N(P0=5mW)	0dB 1KHz		-82		dB
	Crosstalk（L/R）	0dB 1KHz		-82/-82		dB
	DAC to Headphone on HPOUTL or HPOUTR(R=32Ω)					
	FScale Output Level	0dB 1KHz		0.7		Vrms
	SNR(A-weighted)	0dB 1KHz		100		dB
	THD+N(P0=15mW)	0dB 1KHz		-83		dB
	THD+N(P0=5mW)	0dB 1KHz		-83		dB
	Crosstalk（L/R）	0dB 1KHz		-86/-86		dB
	DAC to Earpiece Driver on EAROUTP and EAROUTN(R=16Ω)					
	FScale Output Level	0dB 1KHz		1.0		Vrms
	SNR(A-weighted)	0dB 1KHz		100		dB
	THD+N(P0=12mW)	0dB 1KHz		-81		dB
	DC Offset at load	0dB 1KHz		2		mV
	DAC to SPK signal on SPKOUTLP and SPKOUTLN(R=10KΩ)					
	FScale Output Level	0dB 1KHz		1.8		Vrms
	SNR(A-weighted)	0dB 1KHz		102		dB
	THD+N	0dB 1KHz		-82		dB
	DC Offset at load	0dB 1KHz		0.7		mV
	DAC to LINEOUT signal on LINEOUTP and LINEOUTN(R=10KΩ)					
	FScale Output	0dB 1KHz		0.9		Vrms

	Level					
	SNR(A-weighted)	0dB 1KHz		98		dB
	THD+N	0dB 1KHz		-81		dB
	DC Offset at load	0dB 1KHz		0.5		mV
ADC Input Path Performance	**MIC1 /2/3to ADC via ADC mixer**					
	FScale Input Level	0dB Gain 1KHz		0.5		Vrms
	SNR(A-weighted)	-1dB 1KHz, 0dB Gain		96		dB
	THD+N	-1dB 1KHz, 0dB Gain		-85		dB
	SNR(A-weighted)	30mV,1KHz, 30dB Gain		81		dB
	THD+N	30mV,1KHz, 30dB Gain		-76		dB
	SNR(A-weighted)	30mV,1KHz, 39dB Gain		81		dB
	THD+N	30mV,1KHz, 39dB Gain		-76		dB
	SNR(A-weighted)	10mV,1KHz, 48dB Gain		73		dB
	THD+N	10mV,1KHz, 48dB Gain		-72		dB
	LINEIN to ADC via ADC mixer					
	FScale Input Level	0dB 1KHz		0.9		Vrms
	SNR(A-weighted)	1KHz		93		dB
	THD+N	1KHz		-85		dB
	Crosstalk（L/R）	1KHz		-85/-85		dB
	AXIIN to ADC via ADC mixer					
	FScale Input Level	0dB 1KHz		0.9		Vrms
	SNR(A-weighted)	1KHz		92		dB
	THD+N	1KHz		-82		dB
	Crosstalk（L/R）	1KHz		-88/-88		dB
Bypass Path Performance	**MIC1/2/3 to Headphone via output mixer**					
	FScale Input Level	0dB Gain 1KHz		0.5		Vrms
	SNR(A-weighted)	-1dB 1KHz, 0dB Gain		98		dB
	THD+N	-1dB 1KHz, 0dB Gain		-91		dB
	SNR(A-weighted)	30mV,1KHz, 30dB Gain		83		dB
	THD+N	30mV,1KHz, 30dB Gain		-78		dB
	SNR(A-weighted)	30mV,1KHz, 39dB Gain		83		dB
	THD+N	30mV,1KHz, 39dB Gain		-79		dB

	SNR(A-weighted)	10mV,1KHz, 48dB Gain		74		dB
	THD+N	10mV,1KHz, 48dB Gain		-73		dB
	LINEIN to Headphone via output mixer					
	FScale Input Level	0dB 1KHz		1		Vrms
	SNR(A-weighted)	-1dB 1KHz		98		dB
	THD+N(-1dBFS)	-1dB 1KHz		-92		dB
	Crosstalk（L/R）	-1dB 1KHz		-89/-89		dB
	AXIIN to Headphone via output mixer					
	FScale Input Level	0dB 1KHz		1		Vrms
	SNR(A-weighted)	-1dB 1KHz		102		dB
	THD+N(-1dBFS)	-1dB 1KHz		-93		dB
	Crosstalk（L/R）	-1dB 1KHz		-88/-88		dB

10 Typical Power Consumption

Default Test Conditions:
LDOIN=CPVDD=1.5V,AVCC=3.0V,VCC-IO1=VCC-IO2=1.8V,VCC-RTC=3.0V
Table 10-1 summarizes the typical power consumption of AXP813.

Table 10-1 Typical Power Consumption

OPERATING MODE	TEST CONDITIONS	LDOIN	AVCC	VCC-IO 1	VCC-IO 2	CPVDD	VCC-RTC
RTC only							
LDO enabled XTAL enabled	LDOIN,VCC-RTC supplies, 32.768KHz clock, three output enable	1.8V	3V	1.8V	3V	1.8V	3V
		0uA	0uA	0uA	0uA	0uA	12uA
Standby							
LDO enabled XTAL enabled	All supplies present, No clocks supply, Default register settings	1.8V	3V	1.8V	3V	1.8V	3V
		73uA	62uA	0uA	0uA	0uA	12uA
Music Playback to Headphone(32Ω load)							
AIF1 to DAC to HPOUT(stereo)	fs=44.1KHz, SYSCLK=MCLK=24.576 MHz, 24bit I2S,Slave mode	1.8V	3V	1.8V	3V	1.8V	3V
		1.5mA	4.1mA	0.013mA	0mA	2.4mA	12uA
Voice record to AIF1							
MIC1 to ADC to AIF1(mono)	fs=44.1KHz, SYSCLK=MCLK=24.576 MHz, 24bit I2S,Slave mode	1.8V	3V	1.8V	3V	1.8V	3V
		1.4mA	4.5mA	0.023mA	0mA	0mA	12uA
Analog-Analog Voice Path (eg. Analog Voice call)							
Mic1 to Lineout, Linein to Hp,	fs=8 kHz, SYSCLK=MCLK=24.576 MHz	1.8V	3V	1.8V	3V	1.8V	3V
		0.75mA	4.1mA	0mA	0mA	2.0mA	12uA

11 Power Management Control and Operation

When AXP813 works, the TWSI or RSB(More detail to see TWSI/RSB Interface), and this interface can be used by HOST to access and adjust AXP813's working status.
Note that the external power hereinafter is VBUS or ACIN input.

11.1 Power On/Off and Sleep/Wakeup

AXP813 has power off and power on status. When at off state, all voltage outputs are turned off except VCC_RTC ,IPSOUT and charger. At this time if powered by battery, the total power consumption is typically 40uA.

11.1.1 Power On/Off Sources

Power on source

Below are the 2 power up sources supported by AXP813 in mechanical off state:

1. Charger insertion (including ACIN and VBUS insertion)
2. Power on key pressed

Power off source

Below are the few sources that can trigger power down of AXP813:

1. ALDOIN < V_{OFF} (indicating IPSOUT too low)
2. Faulty condition
3. Power on key pressed

Power on from charger insertion

The AXP813 should be able to start the boot sequence from a charger insertion. A charger insertion is detected from a rising voltage on the ACIN/VBUS node. If 4.1V< ACIN/VBUS < 7.0V, the charger will start charging immediately and autonomously.

Power on from power key pressed

POK----Power On Key

The Power On Key(POK) can be connected between PWRON pin and GND of AXP813. AXP813 can automatically identify the status and then correspond respectively.

The AXP813 should be able to start the boot sequence from a power on key pressed. The AXP813 has a configurable timer to detect the power on key hold time. Power on key signal in AXP813 is referred as POK. Once falling edge is detected on POK, AXP813 timer will start counting the hold time. POK signal has to be low for at least 32ms for it to be considered a valid signal. If the power on key hold time exceeds the timer threshold (ONLEVEL determined by REG36H [7:6]), the AXP813 will continue to boot . Otherwise the AXP813 will remain off.

Power off from ALDOIN< V_{OFF}

AXP813 will constantly monitor voltage level of ALDOIN which is connected to IPSOUT. When VALDOIN < V_{OFF} (default is 2.9V, set in REG 31H[2:0]), AXP813 will force shutdown. There will be 500us de-bounce circuit for ALDOIN detection and adjusted hysteresis voltage to prevent false trigger. After force shutdown occurred, AXP813 will remain off and wait for power on event to boot up.

V_{OFF} and the compensated hysteresis voltage as below:

Table 11-1 V_{OFF} and the Compensated Hysteresis Voltage

V_{OFF} **condition**	**VX condition (Hysteresis)**
V_{OFF}<=3.0V	0.3V
V_{OFF} = 3.1V	0.2V
V_{OFF} = 3.2V or 3.3V	0.1V

Power off due to faulty condition

AXP813 will force shutdown once faulty event happened. Faulty event includes VBUS>7V, AXP813 internal temperature exceeds warning level3 (set in REG 8FH [2]) and buck output drop more than 15% than the targeted output voltage (set in Reg 81H).

Power off by power on key pressed

Once power on key pressed, POK signal assert low and need to remain low for 32ms to be considered valid. AXP813 has configurable timer to detect power on key hold time. If POK remain low for less than IRQLEVEL (set in REG 36H [5:4]), POKSIRQ will be set. For POK hold time > IRQLEVEL, POKLIRQ will be set. Typically, the system uses POKLIRQ to allow user to express their demands for Host shutdown.

If POK remain low for more than OFFLEVEL (set in REG 36H [1:0]), POKOIRQ will be issued. After IRQ issued, AXP813 will wait for a period of time before it force shutdown (set in REG36H[3]). The AXP813 can be turned on automatically (set in REG36[2]). The waiting period is programmable from 0s to 70s(set in REG37H[2:0]).

If POK width is more than 16s, then AXP813 will force shutdown immediately. This feature can be set in REG 8FH [3]. When AXP813 force shutdown, VCC_RTC will be shut off for 2 seconds, with 1K resistor to pull VCC_RTC to ground and then it will turn back on.

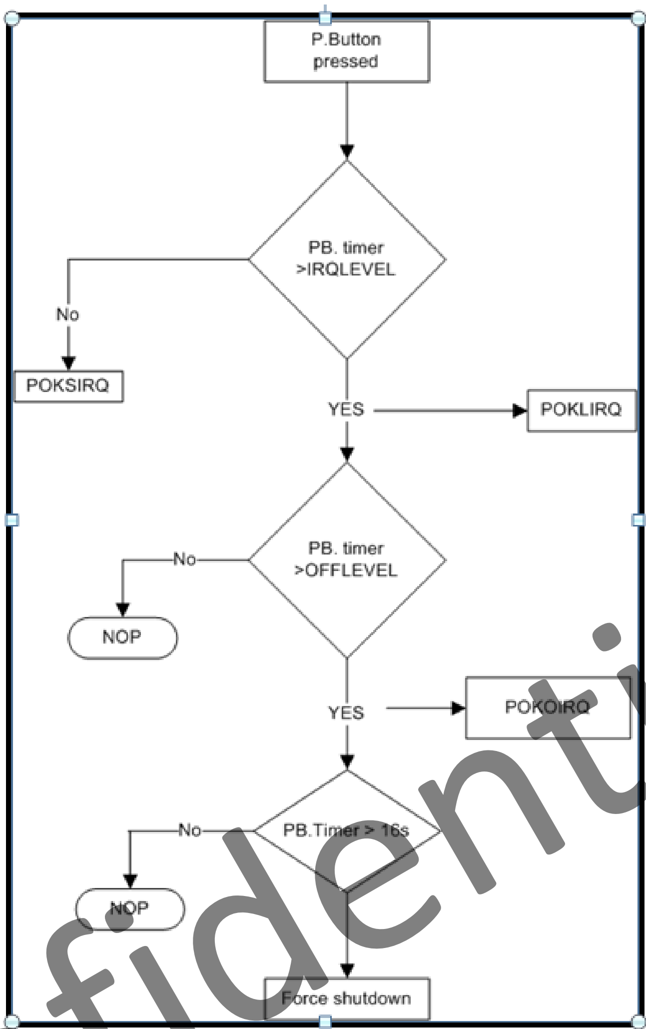

Figure 11-1 Power off Process

11.1.2 Sleep and Wakeup

To switch from power on mode to sleep mode, several power outputs should be disable. After that,REG31[3] can be used to control whether following sources can be used to trigger wakeup.

1. ACIN connection/disconnection(REG40[6:5] is set to 1)
2. VBUS connection/disconnection(REG40[3:2} is set to 1)
3. POK press-long-key(REG44[3] is set to 1)
4. POK negative edge(REG44[5] is set to 1)
5. Battery low power warning Level 2(REG43[1:0]are set to 1)
6. Detection of positive/negative edge when GPIO[1:0] functions input(REG4C[1:0],REG90[7:6] and REG92[7:6] are set to 1)
7. Software wakeup(REG31[5] is set to 1)
8. IRQ wakeup(REG8F[7] is set to 1)
9. Charging or Charger Done(REG41[3:2] are set to 1)

After wakeup is triggered, each power output can be restored to default state in right power on sequence. Here is the Sleep/Wakeup control process:

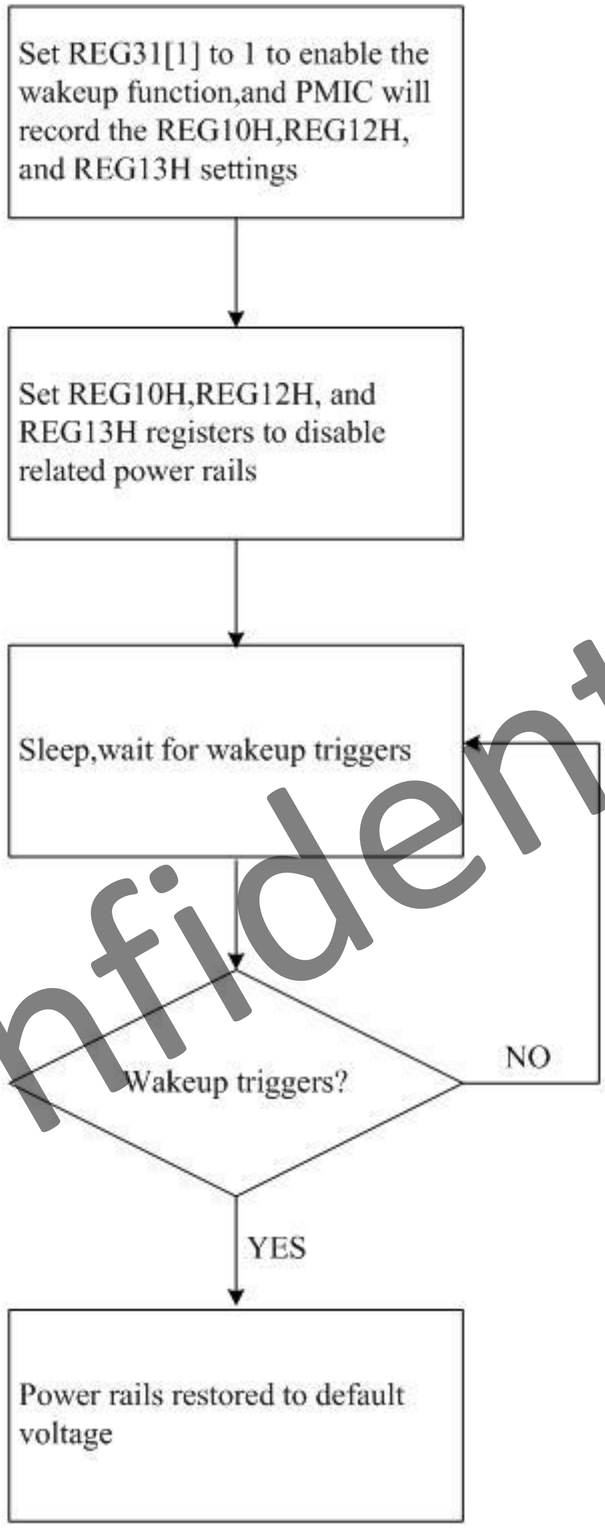

Figure 11-2 Sleep/Wakeup Control Process

11.2 IPS (Intelligent Power Select)

AXP813 has Intelligent Power Select (IPS) to select the appropriate source to power the system. The output of IPS, IPSOUT will then be used as power source for downstream regulators and battery charger.

11.2.1 IPS Overview

Figure 11-3 shows the input power sources of IPS.

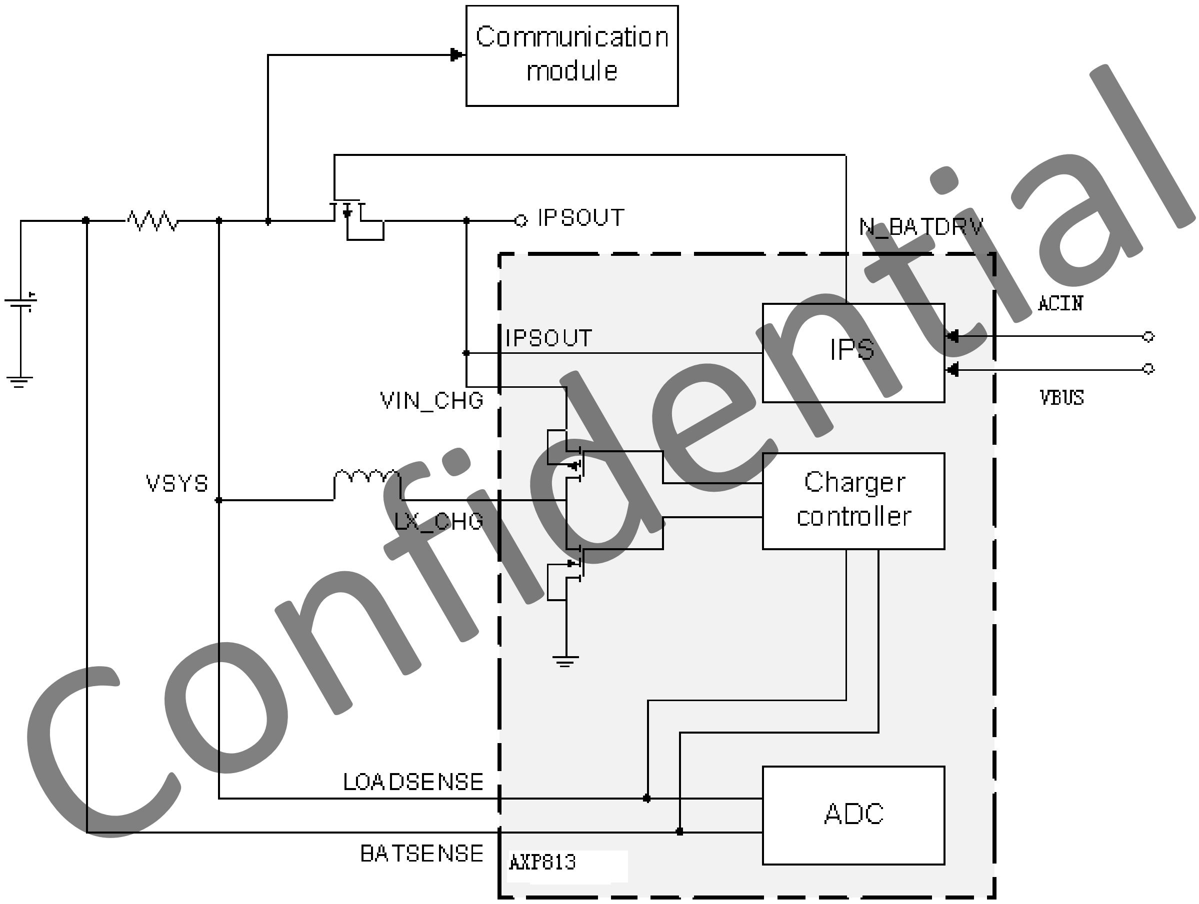

Figure 11-3 Input Power Sources of IPS

- If only Li- Battery is available, and no external power input, Li- Battery is used for power input;
- If external power is available (ACIN or VBUS), it is preferred in power supply
- If both ACIN and VBUS are available but not short together, then ACIN is preferred in power supply
- If both ACIN and VBUS are available and short together,
- If Li- Battery is available, it will “Seamlessly” switch to Li- Battery once external power is removed
- If the current is still insufficient, charge current will be reduced to zero, and Battery is used for one of power sources

11.2.2 IPSOUT Source Selection

There are two power source, ACIN source is channeled to IPSOUT when REG 3AH[7] is set to 0 (default). For whatever reason, if ACIN source need to be disconnected from IPSOUT, set REG 3AH[7] to 1. VBUS source is channeled to IPSOUT when REG 30H[7] is set to 0 (default). For whatever reason, if VBUS source need to be disconnected from IPSOUT, set REG 30H[7] to 1. Note that when BC Detection module is detecting, REG 2CH[2] = 1, VBUS to IPSOUT channel is OFF. We can shorted ACIN and VBUS together to Reduce power path Resistor, and AXP813 can auto detect it and report it in REG00H[1].

Table 11-2 ACIN Path Select Control

REG 3AH	Description	R/W	Default
Bit 7	ACIN path select control when ACIN valid 0: ACIN path selected 1: ACIN path not selected	RW	0

VBUS Select Setting

Table 11-3 VBUS Select Setting

REG 30H[7]	REG 2CH[2]	VBUS_SEL
0	0	1
1	X	0
X	1	0

Table 11-4 REG30H

REG 30H	Description	R/W	Default
Bit 7	VBUS path select control (VBUS_SEL) when VBUS valid 0: VBUS path selected 1: VBUS path not selected	RW	0

Table 11-5 REG2CH

REG 2CH	Description	R/W	Default
Bit 2	**BC_status (BC Detection status)** 1: Detecting, this bit is set when BC Detection start 0: Detection complete	RW	0

Input Source Select Setting

Table 11-6 Input Source Select Setting

VBUS_SEL	REG 00H[6]	REG 00H[4]	REG 00H[1]	IPSOUT from
×	0	0	×	VSYS
×	1	×	0	ACIN
0	0	1	×	VSYS
1	0	1	0	VBUS
1	0	1	1	VBUS
0	1	1	1	VSYS

×	1	0	1	ACIN
1	1	1	1	ACIN+VBUS

Table 11-7 Indication ACIN and VBUS

REG 00H	Description	R/W	Default
Bit 6	Indication ACIN can be used or not	R	0
Bit 4	Indication VBUS can be used or not	R	0

11.2.3 ACIN Current/Voltage Limitation

ACIN input power source has minimum hold voltage (VHOLD) setting and current limit setting. When the input source voltage drops below its VHOLD setting, it is considered as not having sufficient power. IPS will limit the current draw automatically so that the input source voltage is hold to this minimum level.

ACIN VHOLD is set as max of VBAT+0.15V or 3AH[5:3] whereas ACIN current limit can be set through REG 3AH[2:0].

VHOLD minimum voltage value can be set through the REG3AH:

Table 11-8 VHOLD Minimum Voltage Value

5	V_{HOLD} setting bit 2	000: 4.0V; 001: 4.1V; 010: 4.2V 011: 4.3V; 100: 4.4V; 101: 4.5V 110: 4.6V; 111: 4.7V	RW	0
4	V_{HOLD} setting bit 1		RW	0
3	V_{HOLD} setting bit 0		RW	0

VBUS current limit is set by REG3AH[2:0]:

Table 11-9 VBUS Current Limit

2:0	VBUS current limit select when VBUS Current limited mode is enable 000-1500mA 001-2000mA 010-2500mA 011-3000mA 100-3500mA 101-4000mA 110-4000mA 111-4000mA	RW	000

11.2.4 VBUS Current/Voltage Limitation

VBUS input power source has minimum hold voltage (VHOLD) setting and current limit setting. When the input source voltage drops below its VHOLD setting, it is considered as not having sufficient power. IPS will limit the current draw automatically so that the input source voltage is hold to this minimum level.

VBUS VHOLD is set as max of VBAT+0.15V or 30H[5:3] whereas VBUS current limit can be set through REG 35H[7:4].

VHOLD minimum voltage value can be set through the REG30H:

Table 11-10 VHOLD Minimum Voltage Value

5	V_{HOLD} setting bit 2	000: 4.0V; 001: 4.1V; 010: 4.2V	RW	1

4	V_{HOLD} setting bit 1	011: 4.3V; 100: 4.4V; 101: 4.5V 110: 4.6V; 111: 4.7V	RW	0
3	V_{HOLD} setting bit 0		RW	0

VBUS current limit is set by REG35H[7:4]:

Table 11-11 VBUS Current Limit

7:4	VBUS current limit select when VBUS Current limited mode is enable 0000-100mA 0001-500mA 0010-900mA 0011-1500mA 0100-2000mA 0101-2500mA 0110-3000mA 0111-3500mA 1xxx-4000mA	RW	0001

For the case of battery charger detection enabled, once the USB charger detection is completed, VBUS current limit will be guided by the result of the detection. Subject to the type of USB charger detected, the current limit set in REG 35H[7:4] will be auto updated by the value set in REG 30H[1:0]. For example, if the BC detection result indicates SDP, the current limit in REG 35H[7:4] will be set to 500mA (900mA if it is USB 3). If the detected USB charger is CDP or DCP, the current limit in REG 35H[7:4] will then be updated according to the setting in REG 30H[1:0].

Table 11-12 REG2FH[7:5]

REG 2FH[7:5]	Current limit	Description
SDP	500mA	USB connected. After communication, CPU can identify USB3.0,then change the current limit to 900mA
Other	REG30H[1:0]	

VBUS with the BC detection:
AXP813 has battery charger detection module that capable of detecting type of USB charger plug onto the port. Below is the battery charger detection flow.

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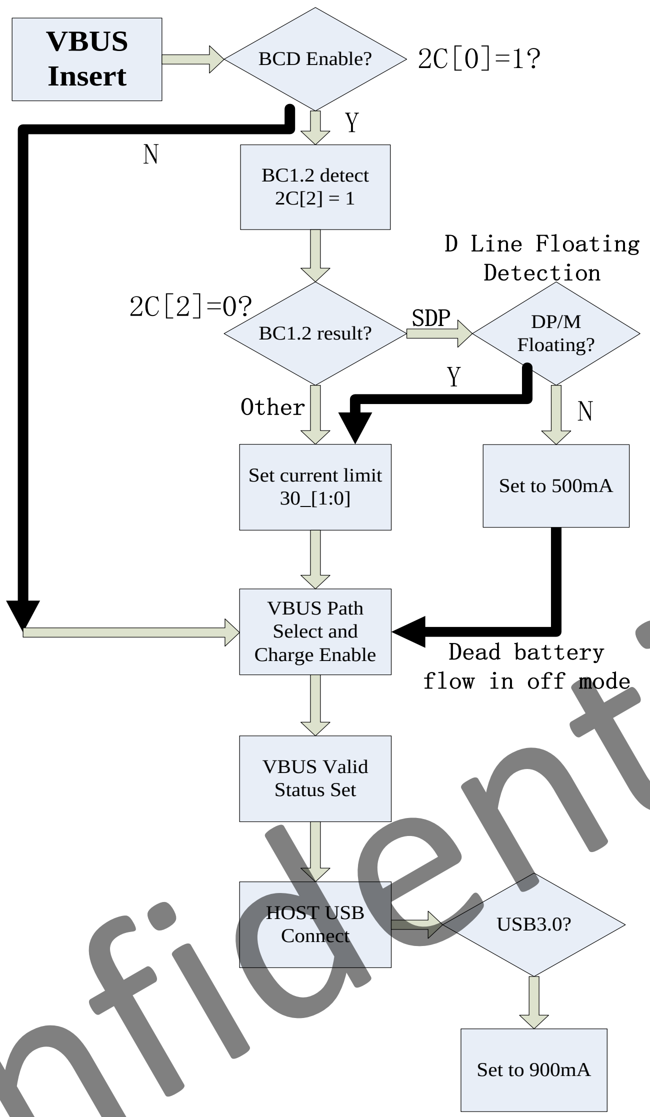


Figure 11-4 AXP818 Battery Charger Detection

When REG 2CH[0] is set to 1, battery charger detection module will start to operate. Upon completion of the BC detection (REG 2CH[2] = 0), AXP813 will automatically update the detection result onto REG 2FH[7:5]. If the BC detection result indicate SDP, the current limit will be set to 500mA (900mA if it is USB 3) or else the current limit will follow the setting in REG 30H[1:0].

11.2.5 ACIN Input Overvoltage Protection

ACIN to IPSOUT path have a regulator, target of 5.0V,Table 11-12 shows the regulator of ACIN to IPSOUT.

Table 11-12 Regulator of ACIN to IPSOUT

Input power	IPSOUT	CHGLED	Contents
>7V	5V	Floating	AXP813 shutdown
>6.3V	5V	2Hz toggle	Work normally
>5.06V	5V	Charge LED	
<5.06	Vin-0.06V	Charge LED	
<3.5V	Vin-0.06V	Charge LED	Invalid

11.2.6 VBUS Input Overvoltage Protection

VBUS to IPSOUT path have a regulator, target of 5.0V,Table 11-13 shows the regulator of VBUS to IPSOUT.

Table 11-13 Regulator of VBUS to IPSOUT

Input power	**IPSOUT**	**CHGLED**	**Contents**
>7V	5V	Floating	AXP813 shutdown
>6.3V	5V	2Hz toggle	Work normally
>5.06V	5V	Charge LED	
<5.06	Vin-0.06V	Charge LED	
<3.5V	Vin-0.06V	Charge LED	Invalid

11.2.7 ACIN Insertion Power Up Condition

The AXP813 will start the boot sequence at the point of ACIN insertion. A ACIN insertion is detected from a rising voltage on the ACIN node as long as it is larger than 4.1V. The existence of ACIN is stored in REG 00H[7]. The charger will start charging immediately and automatically.

11.2.8 VBUS Insertion Power Up Condition

The AXP813 will start the boot sequence at the point of VBUS insertion. A VBUS insertion is detected from a rising voltage on the VBUS node as long as it is larger than 4.1V. The existence of VBUS is stored in REG 00H[5]. The charger will start charging immediately and automatically.

11.3 BC Detection Module

This section is primarily based on battery charging specification, for more information please refer to BC rev1.2 specifications. AXP813 is compatible with BC rev1.2 and can identify SDP/CDP/DCP except ACA . The AXP813 can detect the device type without software activity.

Table 11-14 BC Detection Module

Device	Description	Compatible
SDP	Standard Downstream Port	AXP813 can identify
CDP	Charging Downstream Port	AXP813 can identify
DCP	Dedicated Charging Port	AXP813 can identify
ACA	Accessory Charger Adapter	AXP813 can't identify

Please refer to REG36H for detailed information.

11.4 Adaptive PWM Charger

The AXP813 battery charger solution has two charging modes that it can be in. It is specifically designed to charge Li Ion or Li Polymer type batteries. The two modes are 1) Pre Charge Mode and 2) Fast Charge Mode. The delineation between these two modes is based on the battery voltage level of V_{TRKL} which is set at 3.0V.

When battery voltage, $V_{BATSENSE}$ is between 0V to 3.0V (V_{TRKL}), the charger is in Pre Charge Mode where charging current is limited to a value of I_{TRKL} (10% of I_{CHRG}, default value is 120mA). This mode of operation is intended to prevent damage to the battery. Once $V_{BATSENSE} \geq V_{TRKL}$, the charger will enter Fast Charge Mode. The Fast Charge Mode can be subdivided into two phases, namely the constant current phase (CC) and the constant voltage phase (CV). The CC phase takes place when $V_{BATSENSE}$ is in between V_{TRKL} and V_{TRGT}. It will charge with constant I_{CHRG}. When $V_{BATSENSE}$ reach V_{TRGT}, charger will operate at CV phase. At this phase, charger will charge with constant voltage of V_{TRGT}.

11.4.1 Charger Overview

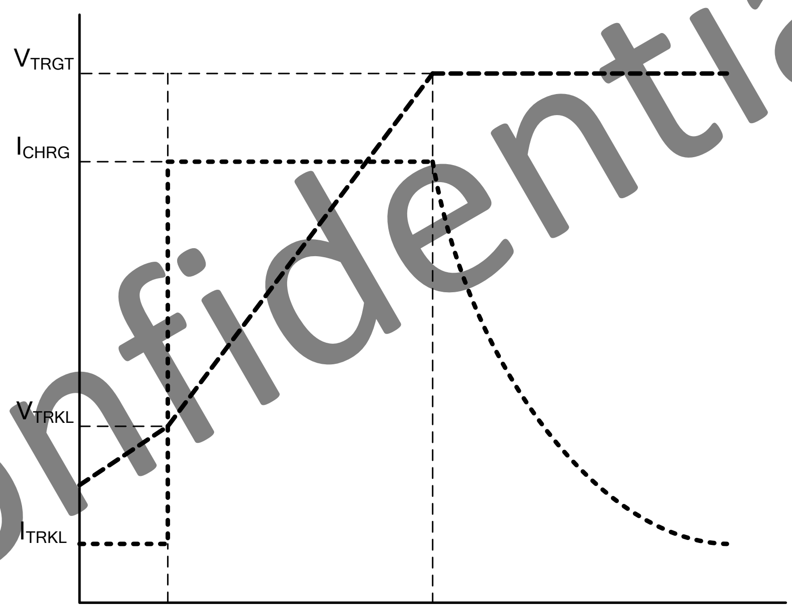


Figure 11-5 Charger Voltage and Current

V_{TRGT} is programmed in REG 33H[6:5] and I_{CHRG} is in REG 33H[3:0] whereas V_{TRKL} is fixed at 3V and I_{TRKL} is set as 10% of I_{CHRG}.

11.4.2 Charging Start and Stop

When $V_{BATSENSE}$ is between 0V to 3.0V (V_{TRKL}), the charge operation will start when VBUS insert and REG 33H[7] is set to 1. The charging operation will cease when $V_{BATSENSE}$ is > $V_{TRGT-0.1V}$ and charging current < 10% of I_{CHRG}.

11.4.3 Timeout Activity

Refer to REG 34H, there are 2 timers that can be programmed as charging expire time, REG 34H[7:6] for Pre Charge and REG 34H[1:0] for Fast Charge Mode. When the actual charge current is less than 20% of the ICHRG, the timer will automatically hold. When the timer expired, charger will no longer charge with programmed charging current. Instead, it will turn into safe mode. Under safe mode, charger will always charge the battery with 5mA until VBATSENSE > VTRGT – 0.1V. When the charger exits from safe mode, it will assert the IRQ. The safe mode status is reflected in REG 01H[3] and SOC can get the mode status through this bit.

Table 11-15 Pre-charge and Fast charge

REG 34H Bit	Description		R/W	Default
7	Pre-charge Timer length setting 1	00: 40 minutes; 01: 50 minutes; 10: 60 minutes; 11: 70 minutes.	RW	0
6	Pre-charge Timer length setting 0		RW	1
1	Fast charge maximum time setting 1	00: 6 hours; 01: 8 hours; 10: 10 hours; 11: 12 hours.	RW	0
0	Fast charge maximum time setting 0		RW	1

Table 11-16 Indicate Battery Active Mode

REG 01H	Description	R/W	Default
Bit3	Indicate battery active mode 0-charger is not in battery active mode 1-charger is in battery active mode	R	

There are two ways to reset or exit from safe mode. One is plug out and re-insert the input power source or toggle charger enable bit.

11.4.4 CHGLED Activity

AXP813 provides CHGLED pin. The LED connected to this pin can be used to indicate charger status and input power sources over voltage alarm. There are two Charge LED modes that can be configured through REG 34H[4] if REG 32H[3] is set to 1. Table 11-17,11-18,11-19 show the definition of charge LED mode, pin control, indicator.

Table 11-17 Charge LED Modes

REG 34H	Description	R/W	Default
Bit 4	CHGLED Mode select when REG 32H[3] is 1 0: Type A; 1: Type B	RW	0

Table 11-18 CHGLED Pin Control

REG 32H	Description		R/W	Default
Bit 5-4	CHGLED pin control	00: Hi-Z 01: 25% 0.5Hz toggle 10: 25% 2Hz toggle 11: drive low	RW	00
Bit 3	CHGLED pin control	0: controlled by REG 32H[5:4]	RW	0

		1: controlled by Charger		

Table 11-19 CHGLED Indicator

CHGLED pin	Mode A	Mode B
Z (tri-state)	Not charging	Not charging due to 1. no external power source or 2. external power source is insufficient and battery is discharging
25% duty 1Hz (Z/Low)	Abnormality alarm due to 1. charger timeout or 2. IC temperature > warning level 2)	Charging
25% duty 4Hz (Z/Low)	Overvoltage alarm (VBUS > 6.3V)	Alarm due to 1. VBUS > 6.3V or 2. charger timeout or 3. IC temperature > warning level 2)
Low	Charging	Not charging due to battery is fully charged

11.4.5 Battery Detection

When the VBATSENSE<2.2V, AXP813 judge it as battery is not present. When VBATSENSE goes higher than 2.2V, it indicates battery present or is inserted. For the case of battery insertion or removal, IRQ will be asserted. Battery presence status is indicated in REG01H[5]and the battery detection function can be set by REG 32H[6]. When charger insert, AXP813 will send a pulse to detect battery is present or not per 16 seconds.

11.4.6 Temperature Protection

AXP813 has built in thermal protection for the IC itself with 3 levels of warning. Each warning level has 6.8˚C different in threshold compare to the next level and each warning level has hysteresis gap of 13.6˚C. Table 11-20 ,11-21,11-22 and 11-23 are the charger responses with respect to each thermal warning level.

Table 11-20 Charger Responses of Each Thermal Warning Level

Warning	AXP813 Response
Level 1	Once the IC temperature exceeds this level, charger will charge at minimum charging current. When IC temperature drops below hysteresis limit, charger will automatically go back to its original charging state.
Level 2	If IC temperature continue to rise and exceeds this level, charger will continue to charge at minimum charging current. If IRQ is enabled in REG43H[7], IRQ will be asserted and its

	status can be read from REG 01H[7].
Level 3	If IC temperature exceeds this level, all the behavior is the same as level 2 but if REG8FH[2] is set to 1, IC will automatically shut down.

Table 11-21 AXP818 Temperature OTIRQ Enable

REG 43H Bit	Description	R/W	Default
7	The AXP813 temperature over the warning level 2 IRQ (OTIRQ) enable	RW	0

Table 11-22 Indication AXP818 Die Over Temperature

REG 01H Bit	Description	R/W	Default
7	Indication AXP813 die over temperature or not 0: not over temperature; 1: over temperature	R	0

Table 11-23 AXP818 Shut Down

REG 8FH	Description	R/W	Default
Bit 2	The AXP813 shut down or not when Die temperature is over the warning level 3 0: not shut down 1: shut down	RW	0

Beside built in IC thermal protection, AXP813 has the capability to sense one external thermal sensor (for battery temperature) through TS pin.

Figure 11-6 shows block diagram of battery temperature measurement.

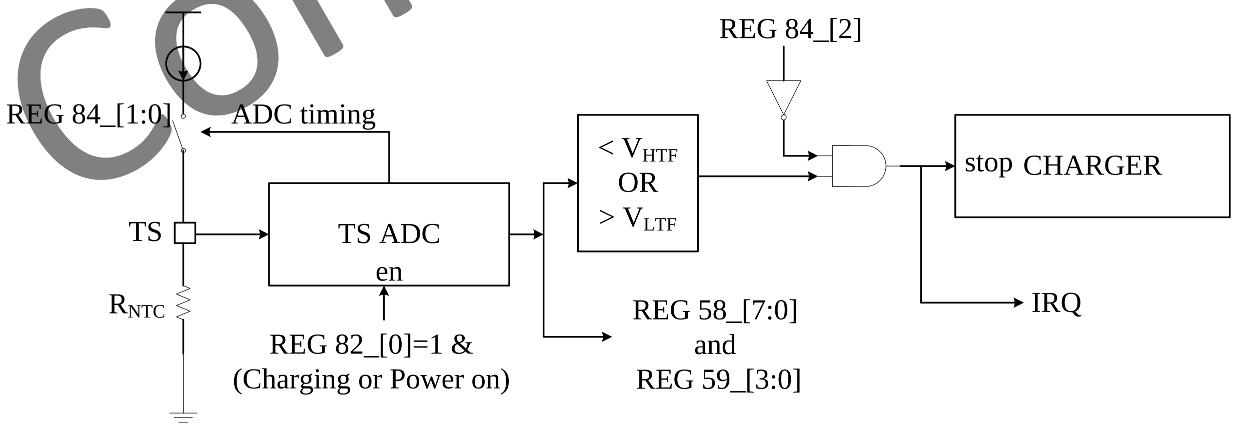


Figure 11-6 Battery Temperature Measurement Block Diagram

AXP813 has built in current source that can be used to inject to external thermal sensor thru TS pin for temperature reading. This current source has 4 level of current which can be programmed through REG 84H[5:4]. By default, the current source will only be injected when ADC is going to read the temperature data. The ADC to read TS pin input is enabled by setting REG 82H[0] to 1. However the current source switch can be programmed to always OFF or ON or only ON when charger is charging through REG

84H[1:0].Table 11-24,11-25 list the bit definition of REG84H and REG82H.

Table 11-24 REG84H

REG 84H Bit	Description		R/W	Default
5-4	Current source from TS pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA		RW	11
1-0	Current source from TS pin on/off enable bit [1:0]	00: off 01: on when charging battery, off when not charging 10: on in ADC phase and off when out of the ADC phase, for power saving 11: always on	RW	10

Table 11-25 REG82H

REG 82H Bit	Description		R/W	Default
0	TS pin input to ADC enable	0: off, 1: on	RW	0

When the current source is injected to thermal sensor (NTC), it will create a voltage drop across NTC and this voltage will be read by 12 bits ADC thru TS pin. The 12 bits code output of the ADC will then be stored in REG 58H (HSB 8) & REG 59H (LSB 4). The relation of TS pin voltage to 12 bits ADC output code is as below:

$$\text{12 bits ADC output code} = R\_NTC(\Omega) * REG\ 84[5:4](\mu A) / (0.8 * 10^3).$$

Table 11-26 is the example by using 10K NTC from Murata (NCP15XH103F03R).

Table 11-26 Example by using 10K NTC from Murata

Temperature (˚C)	R_NTC (Ω)	TS Pin Voltage (V)	12 bits ADC output code	
			REG 58H[7:0]	REG 59H[3:0]
-10	40260	3.221	FBH	AH
0	26490	2.119	A5H	8H
25	10000	0.800	3EH	8H
40	5840	0.467	24H	7H
45	4924	0.394	1EH	CH
55	3550	0.284	16H	3H

Two battery over temperature (OTP) and two under temperature (UTP) thresholds can be set to protect the battery by either controlling the charger or shutdown the system. The first level OTP & UTP thresholds are programmed by REG 38H & REG 39H. The second level OTP & UTP threshold are programmed by REG 3CH & REG 3DH. When battery temperature is higher or lower than the first level OTP or UTP threshold, IRQ is asserted, charger will stop charging and REG 01H[6] change to 0 to reflect the status. When battery temperature is higher or lower than the second level OTP or UTP threshold, IRQ is asserted. System may or may not shutdown subject to SW decision. There is a hysteresis of 460.8 mV(refer to TS pin voltage) for UTP threshold, and there is a hysteresis of 57.6 mV for OTP threshold. Every time when the battery temperature comes out from first level over or under temperature, IRQ is asserted. Charger restores the original charging state and REG 01H[6] change to 1. In normal case, first level of OTP & UTP thresholds should be set within the second level OTP & UTP thresholds.

Using TS pin current source and obtain TS pin data of the table 11-27:

Table 11-27 TS Pin Current Source and Data

Usage condition	setting	Key point
Don't need temperature protection	TS = GND，REG 84H[1:0] = 00，(default 00)，REG84H[2] = 1	TS work as GPADC
Temperature protection when in charger	REG 84H[1:0] = 01	Current source on when charging
Temperature protection when in charging and discharging	REG 84H[1:0] = 10	
TS for GPADC or GPIO	REG 84H[1:0] = 11 when need current source REG 84H[1:0] = 00 when not need current source	

Logic Table：

Table 11-28 Logic Table

REG84H[2] Function	REG82H[0] ADC Enable	REG84H[1:0] Current	Work mode	IRQ	Note
0	0	xx	TS	NO	
0	1	00	TS	NO	
0	1	01	TS	IRQ when in Charging	all IRQ work
0	1	10/11	TS	IRQ all times	
1	0	xx	GPADC	NO	TS function disable

11.5 Multi-Power Outputs

DCDC1-7 are dual mode (PFM / PWM), by default is auto switch mode. All Buck and PWM charger are synchronized with frequency of 3MHz (with spread spectrum option), hence small value external inductors and capacitors components can be used.

All Buck and LDO have current limiting protection function. When the load current exceeds the current limit, the output voltage will drop. Meanwhile, all of the Buck output voltage will be monitored. If the Buck output voltage is 15% lower than the set value and BUCK 85% low voltage turn off AXP813 function (REG 81H) is enabled, AXP813 will automatically force a shutdown and PWROK pin becomes low. Buck output voltage monitor de-bounce time setting is available at REG 8EH[7:6].

DCDC2-7 has DVM enable option. In DVM mode, when there is a change in the output voltage, BUCK will change to the new targeted value step by step. If the application does not require use of any Buck, the LX pin can be left floating while VIN and PGND need to be connected. AXP813 will automatically detect this state to turn off the Buck.

Table 11-29 Multi-Power Outputs

X-Powers	Input	Default Voltage	Max Current	Default State	Application
DCDC4	IPSOUT	0.9V	3A	on	GPU
DCDC7	IPSOUT	-	1.8A	off	-
DCDC6	IPSOUT	0.9V	2.5A	on	SYS
DCDC5	IPSOUT	1.24V	2.5A	on	DRAM
DCDC2	IPSOUT	0.9V	3A	on	CPUA
DCDC3	IPSOUT	0.9V	3A	on	CPUB
DCDC1	IPSOUT	3.3V	1.5	on	VCC-IO
ELDO1	IPSOUT	-	0.4A	off	DVDD-CSI-R
ALDO3	IPSOUT	3.0V	0.2A	on	AVCC
FLDO1	>1.2V	-	0.3A	off	HSIC
FLDO2	>1.2V	0.9V	0.1A	on	CPUS
FLDO3	>1.2V	-	0.03A	off	-
RTCLDO	IPSOUT	1.8V	60mA	Always on	RTC

VCC_RTC input from IPSOUT. As long as any of the VBUS or ACIN or BAT power exists, It will not power down. VCC_RTC is fixed at 1.8V.

11.6 ADC

AXP813 has a 12Bit SAR ADC. The ADC input range is 0V to 2.0475V, with is 0.5mV/step. Voltage and current ADC has sampling frequency option of 800/400/200/100Hz. The relationship between input signal and data is listed table 11-30:

Table 11-30 Relationship between Input Signal and Data

Channel function	000H	STEP	FFFH	Condition
BAT voltage (BATSENSE)	0mV	1.1mV	4.5045V	Power On
Current offset	0mA	1mA	4.095A	Charging or power on
BAT discharge current	0mA	1mA	4.095A	Power on
Internal temperature				Charging or Power on
BAT charge current	0mA	1mA	4.095A	Charging or Power on
TS pin input	0mV	0.8mV	3.276V	Charging or Power on
GPIO0 pin input	0mV	0.8mV	3.276V	Power On

Current ADC measured the current through the 10mohm resistor between BATSENSE and LOADSENSE. For internal temperature, internal logic will do the ADC data comparison with register set warning level for sending over-temperature alarm or shutdown. To identify the battery current direction, the charge current and discharge current value will be compare base on status of charger enable, battery present and VBUS present indication.

11.7 Fuel Gauge

The Fuel Gauge comprises 3 modules – Rdc calculation module; OCV (Open Circuit Voltage) and Coulomb counter module; and calibration module. The Fuel Gauge system is able to export information about battery to application such as Battery capacity percentage (REG B9H), Battery Voltage (REG 78H, REG 79H), Battery charging current (REG 7AH, REG 7BH), Battery discharge current (REG 7CH, REG 7DH), Battery maximum capacity (REG E0H, REG E1H), Battery Rdc value (REG BAH, REG BBH). The Fuel Gauge can be enabled or disabled via REG B8H. The Battery low warning can be set in REG E6, and IRQ (REG 4BH) will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set in REG E6H.

Once a default battery is selected for a particular design, it is highly recommended to calibrate the battery to achieve better Fuel Gauge accuracy. The calibration procedure is documented in separate Application Guide – **AXP813 Battery Calibration Application Guide**. Once the calibration data are available, user can write the calibration info to the following register – REG C0H – DFH (OCV percentage table) on each boot. Or user can choose not to do the calibration and use the default OCV percentage value. Additionally, the Fuel Gauge system is capable to learn the battery characteristic on each Full charge cycle. Information such as Battery Maximum capacity (REG E0H, REG E1H) and Rdc (REG BAH, REG BBH) will be updated automatically over time.

OCV Percentage is showed by Table 11-31.

Table 11-31 OCV Percentage

Reg Address	Percent	OCV
	0	2.9920
C0	RW(H)	3.1328
C1	RW(H)	3.2736
C2	RW(H)	3.3440
C3	RW(H)	3.4144
C4	RW(H)	3.4848
C5	RW(H)	3.5552
C6	RW(H)	3.5904
C7	RW(H)	3.6080
C8	RW(H)	3.6256
C9	RW(H)	3.6432
CA	RW(H)	3.6608
CB	RW(H)	3.6960
CC	RW(H)	3.7312
CD	RW(H)	3.7664
CE	RW(H)	3.8016
CF	RW(H)	3.8192
D0	RW(H)	3.8368

D1	RW(H)	3.8544
D2	RW(H)	3.8720
D3	RW(H)	3.9072
D4	RW(H)	3.9424
D5	RW(H)	3.9776
D6	RW(H)	4.0128
D7	RW(H)	4.0480
D8	RW(H)	4.0832
D9	RW(H)	4.1184
DA	RW(H)	4.1360
DB	RW(H)	4.1536
DC	RW(H)	4.1888
DD	RW(H)	4.224
DE	RW(H)	4.2592
DF	RW(H)	4.2944
	100	4.3296

11.8 Interrupt Controller

AXP813 Interrupt Controller monitors such as low power, bad battery, PWRON pin signal, over temperature, GPIO input edge signals such as trigger events. When the events occur, corresponding IRQ status will be set to 1, and will drive IRQ pin (NMOS open drain) asserted low. When host detect triggered IRQ signal, host will scan through the trigger events and respond accordingly. Meanwhile, Host will reset the IRQ status by writing "1" to status bit. Host will always check every IRQ status from time to time and only will take effect with respective relevant enabled IRQ bit only.

The input edge IRQ of GPIO will only functions when GPIO pin is set as Digital input, and the function will take effect when input edge IRQ is enable . The input will go through about 1ms of de-bounce and corresponding IRQ will trigger when detect rising and falling edge. Rising, falling, or both edge triggering is control by corresponding IRQ register bit.

8bits event timer will issue timeout IRQ. Clearing IRQ doesn't start counter.

12 Codec Function Description

12.1 Power

There are a Power-Reset circuit in AXP813 used to reset all the circuit and register to a standby state after power up. The Power-Reset circuit make all the supply power need no specific timing. All the supply voltages are illustrated in the figure 12-1.

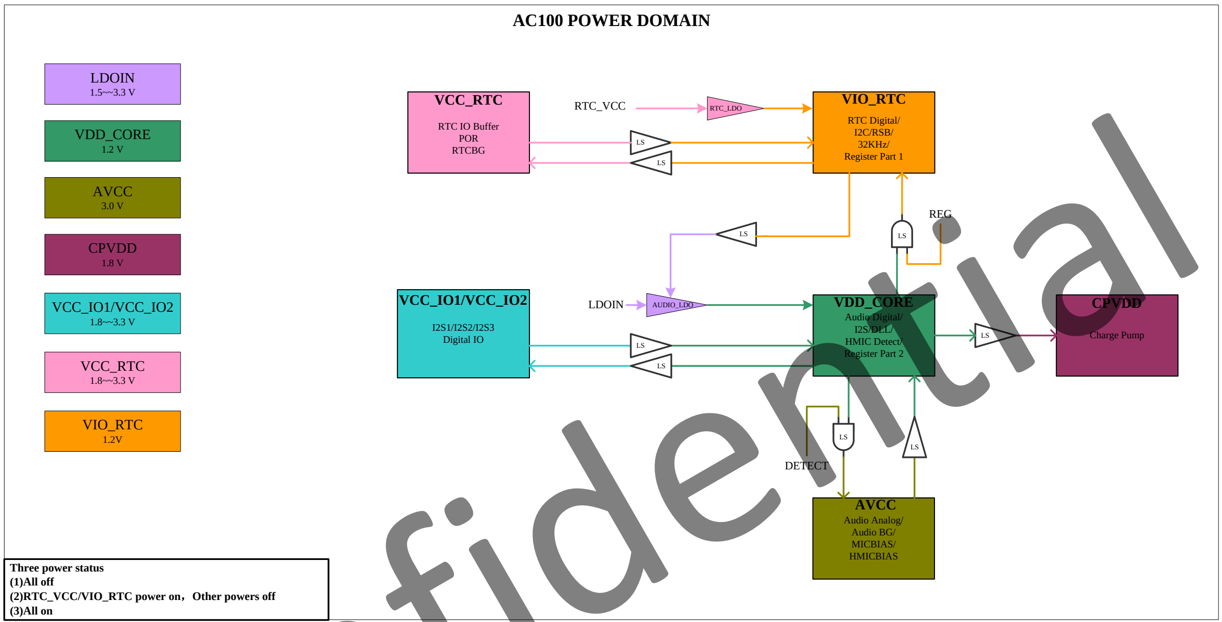


Figure 12-1 Codec Power Domain

VDD-CORE is 1.2V for audio digital core power generated from LODIN pin, which also can be direct supplied from VDD-CORE pin. VDD-IO1 is digital I/O power for I2S1 and I2S2. VDD-IO2 is digital I/O power for I2S3. AVCC is for analog power. CPVDD for charge pump power. VIO-RTC is RTC digital core power generated from VCC-RTC.

When the AXP813 is not working, it need to set the supply properly to prevent power leakage. There are two settings to select. It's best to power off all the supply. The other is to make sure AVCC and CPVDD both power on.

At the setting of the table 12-1 , AXP813 has the best performance.

Table 12-1 Power Setting

LDOIN	VDD_CORE	AVCC	CPVDD	VCC-IO1	VCC-IO2	VCC_RTC	VIO_RTC
1.5~~3.3 V	1.2 V	3 V	1.8 V	1.8/3.3 V	1.8/3.3 V	1.8/3.3 V	1.2 V
Supplied	N/A	Supplied	Supplied	Supplied	Supplied	Supplied	N/A

* VDD_CORE and VIO_RTC generated by internal LDO.

12.2 Clock

The system clock(SYSCLK) of AXP813 must be 512*fs(fs=48KHz or 44.1KHz). So the system should arrange the divider to generate 24.576MHz for audio clock series of 48KHz or 22.5792MHz for series of 44.1KHz.

SYSCLK can be selected from I2S1CLK or I2S2CLK which derived from MCLK1, MCLK2 or PLL. MCLK1 and MCLK2 are always provided externally while the PLL reference clock can be select from MCLK1, MCLK2, BCLK1, BCLK2.

I2S1CLK is the reference of the first I2S clocking zone. I2S2CLK is the reference of the second I2S clocking zone. The third I2S only support master mode. Its clocking zone must be synchronized with either of the I2SnCLK(n=1,2). In master mode, LRCK and BCLK are derived internally from I2SnCLK. In slave mode, LRCK and SCLK are supplied externally and BCLK can be used as the PLL input reference.

SYSCLK is the reference of ADC, DAC, DVC, MIXER, AGC and DRC module. If SRC1 or SRC2 is used, SYSCLK must be set by PLL, then the SRCnCLK is auto provided for SRC module. If all the relevant module above is not used, the SYSCLK needn't be configured.

There are also an internal Oscillator to generate a clock signal for direct-path mode. In this mode, the oscillator supply clock to charge pump, adjustment circuit, headphone detect circuit .In direct-path case, no external clock need .

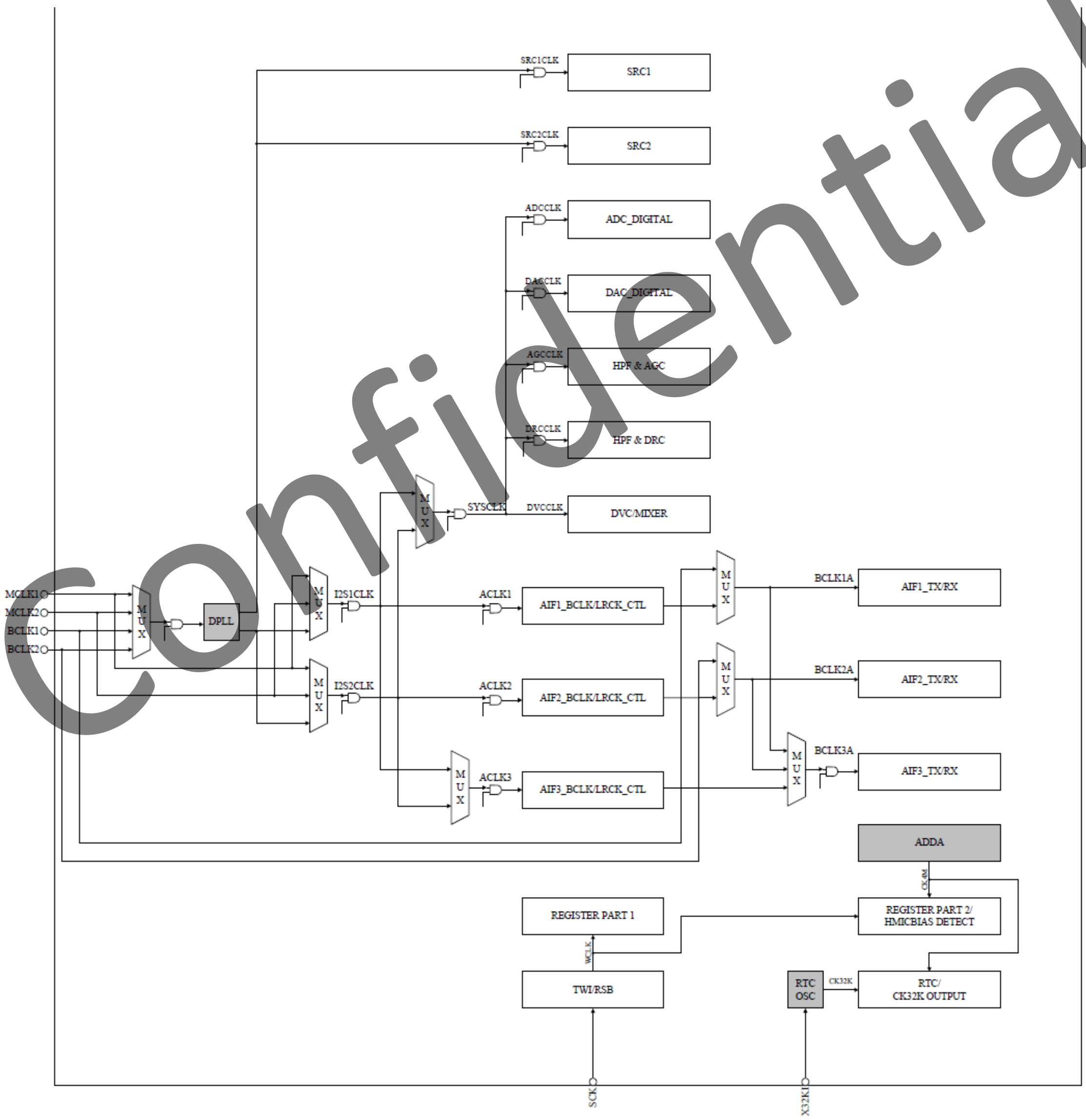


Figure 12-2 Codec Clock System

12.3 PLL

A Phase-Locked Loop(PLL) is used to provide a flexible input clock range from 128KHz to 24MHz. The source of the PLL can be set to MCLK1, MCLK2, BCLK1 or BCLK2 by setting register. The PLL output is always used to provide the system clock(SYSCLK) of AUDIO codec when 24.576MHz or 22.5792MHz can not be provided from MCLK.

The PLL transmit formula as below:

$$FOUT = (FIN * N) / (M * (2K+1)) ; \quad (N = N\_i + 0.2*N\_f)$$

Table 12-2,12-3 show clock setting of SYSCLK.

Table 12-2 Clock Setting for SYSCLK=24.576 MHz

FIN	M	N	K	FOUT
128K	1	576	1	24.576M
192K	1	384	1	24.576M
256K	1	288	1	24.576M
384K	1	192	1	24.576M
...	....	...	1	24.576M
6M	25	307.2	1	24.576M
13M	42	238.2	1	24.576M
19.2M	25	96	1	24.576M

Table 12-3 Clock Setting for SYSCLK=22.5792 MHz

FIN	M	N	K	FOUT
128K	1	529.2	1	22.5792M
192K	1	352.8	1	22.5792M
256K	1	264.6	1	22.5792M
384K	1	176.4	1	22.5792M
...	....	...	1	22.5792M
6M	38	429	1	22.5789M
13M	19	99	1	22.5789M
19.2M	25	88.2	1	22.5792M

12.4 I2S/PCM Interface

There are three I2S/PCM interfaces which can be configured as master mode or slave mode in AXP813. The three I2S/PCM interfaces provide flexible connectivity with multiple processors (e.g. Application processor, Baseband processor and Wireless transceiver).

Interface I2S1 and I2S2 can be configured as Master or Slave, the third interface I2S3 operates in Master mode and supports PCM mode only.

In the general case, the digital audio interface uses four pins as below:

- BCLK: Bit clock for data synchronization
- LRCK: Left/Right data alignment clock
- SDOUT: output data for ADC data
- SDIN: input data for DAC data

I2S1 and I2S2 audio interface support four different data formats as below. But I2S3 supports PCM short mode only. On the first digital audio interface I2S1, TDM is available for all four format and AXP813 can use it to transmit or receive up to four channel data on timeslot0 and timeslot1 simultaneously.

- I2S mode
- Left justified mode
- Right justified mode
- PCM short mode

Below diagrams(from Figure 12-3 to 12-11) show the timing diagram of I2S/PCM.

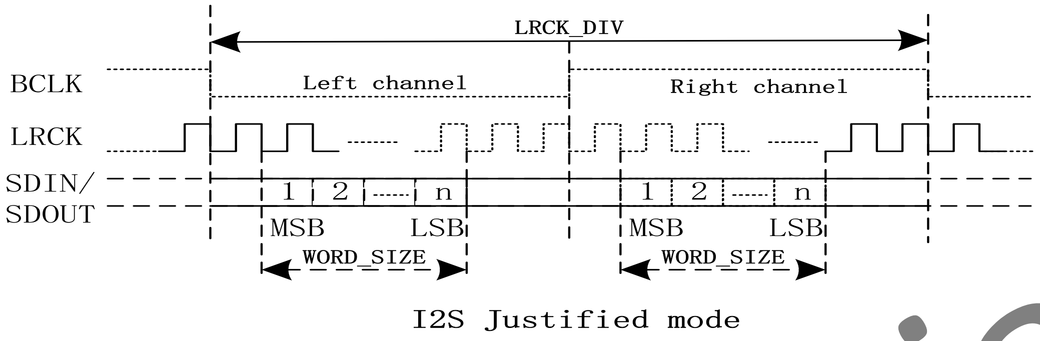


Figure 12-3 I2S Justified mode

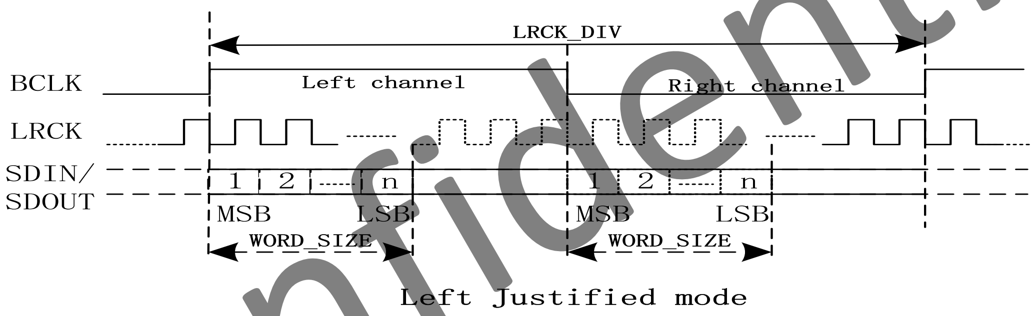


Figure 12-4 Left Justified mode

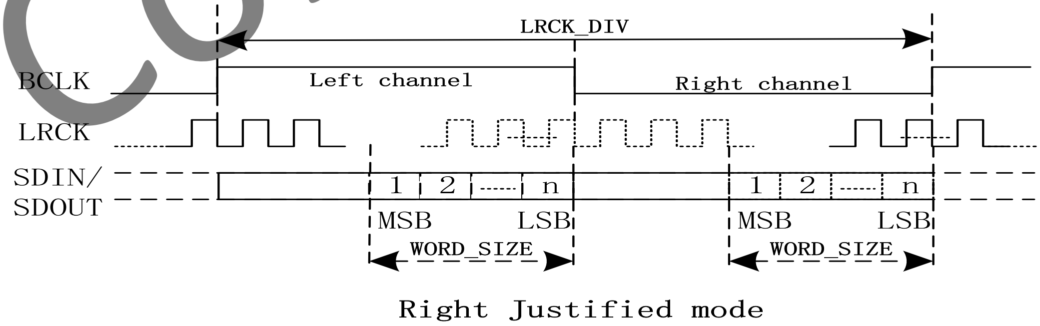


Figure 12-5 Right Justified mode

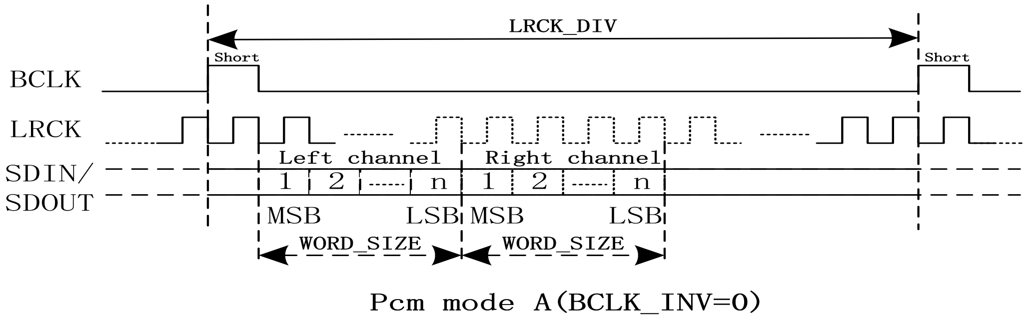


Figure 12-6 PCM mode A(LRCK_INV=0)

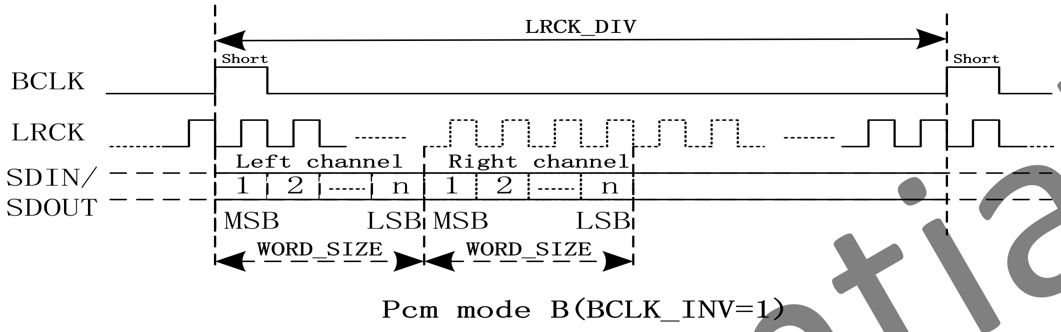


Figure 12-7 PCM mode B(LRCK_INV=1)

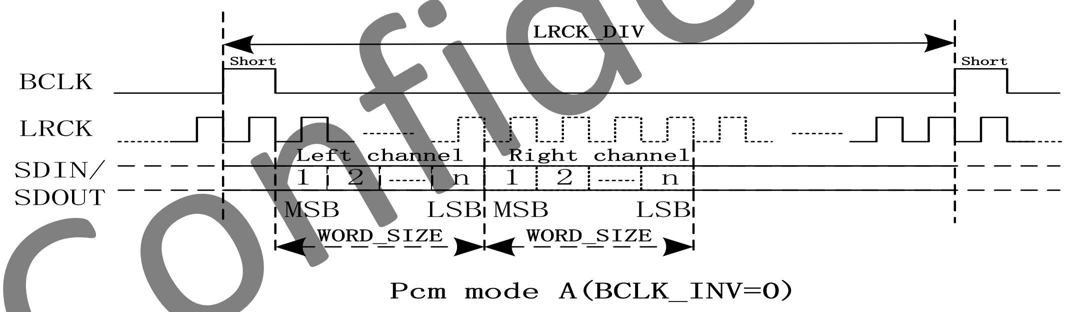


Figure 12-8 PCM mode A mono(LRCK_INV=0)

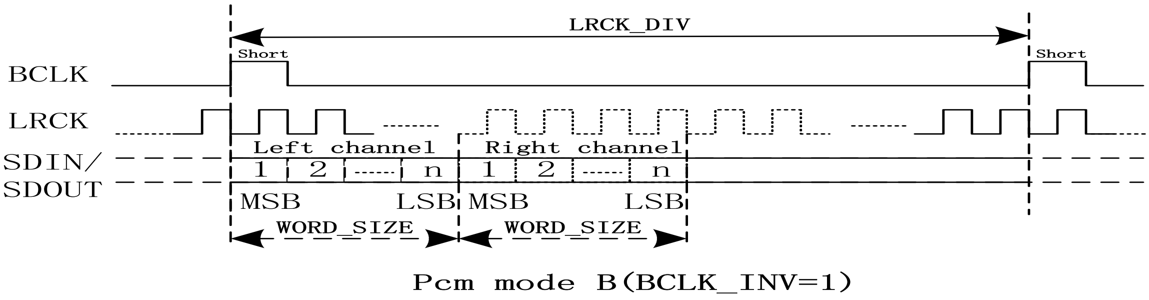


Figure 12-9 PCM mode B mono(LRCK_INV=1)

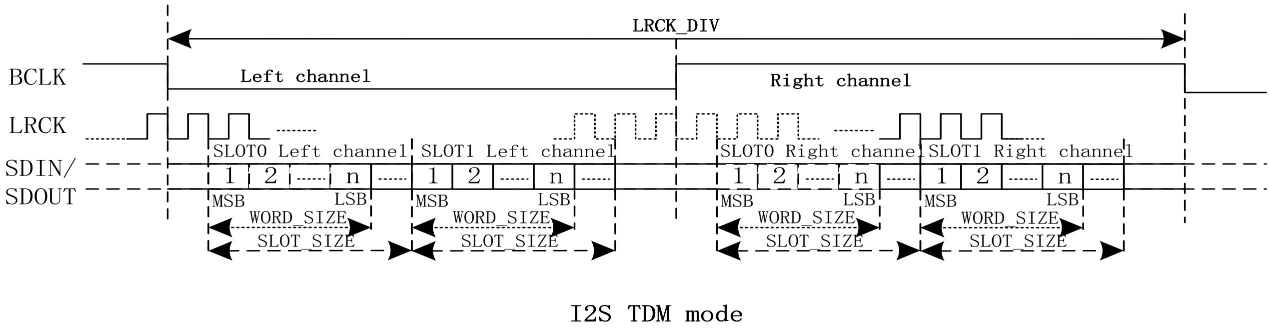


Figure 12-10 I2S TDM mode

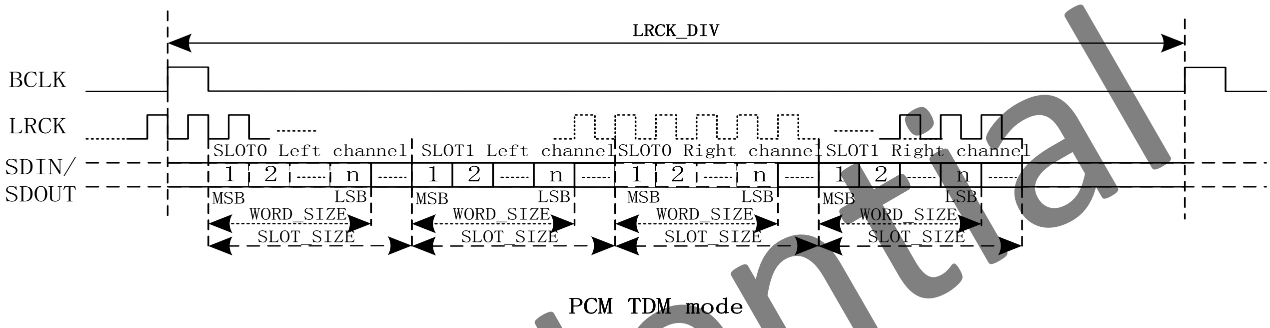


Figure 12-11 PCM TDM mode

12.5 Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC can not be independent of DAC sample rate. In other words, the stereo ADC and DAC must work at a same sample rate. The sample rate is configured by the register ADDA_FS_I2S1 or ADDA_FS_I2S2 depending on which I2SnCLK selected as the system clock(SYSCLK).

In order to save power, the left and right analog ADC part can be enabled/disabled separately by setting register ADC_APC_CTRL Bit15 & Bit11. The digital ADC part can be enabled/ disabled by ADC_DIG_CTRL Bit15.

The volume control of the stereo ADC is set via register ADC_APC_CTRL Bit14:12 & ADC_APC_CTRL Bit10:8.

12.6 Stereo DAC

The stereo DAC sample rate is the same as the stereo ADC. The sample rate is configured by the register ADDA_FS_I2S1 or ADDA_FS_I2S2 depending on which I2SnCLK selected as the system clock(SYSCLK).

In order to save power, the left and right DAC can be enabled/disabled separately by setting register OMIXER_DACA_CTRL Bit15:14. The digital DAC part can be enabled/ disabled by DAC_DIG_CTRL Bit15.

12.7 Mixer

The Codec supports three series of mixers for all function requirements:

- 2 channels DAC Output mixers
- 2 channels ADC Record mixers
- Digital mixers

12.7.1 DAC Output Mixers

The output mixer is used to drive analog output, including headphone, earpiece, speaker, lineout. The following signals can be mixed into the output mixer:

- LINEINL/R
- AXIL/R
- MIC1P/N,MIC2P/N
- Stereo DAC output

12.7.2 ADC Record Mixers

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. The following signals can be mixed into the output mixer:

- LINEINL/R
- AXIL/R
- MIC1P/N,MIC2P/N
- Stereo DAC output

12.7.3 Digital Mixers

The digital mixers are provided for digital audio data mixing on four I2S1 output paths, two I2S2 output paths and two paths to the stereo DAC. It's separately controlled by the register I2S1_MXR_SRC, I2S2_MXR_SRC and DAC_MXR_SRC. Figure 12-12 show the block diagram of digital mixers.

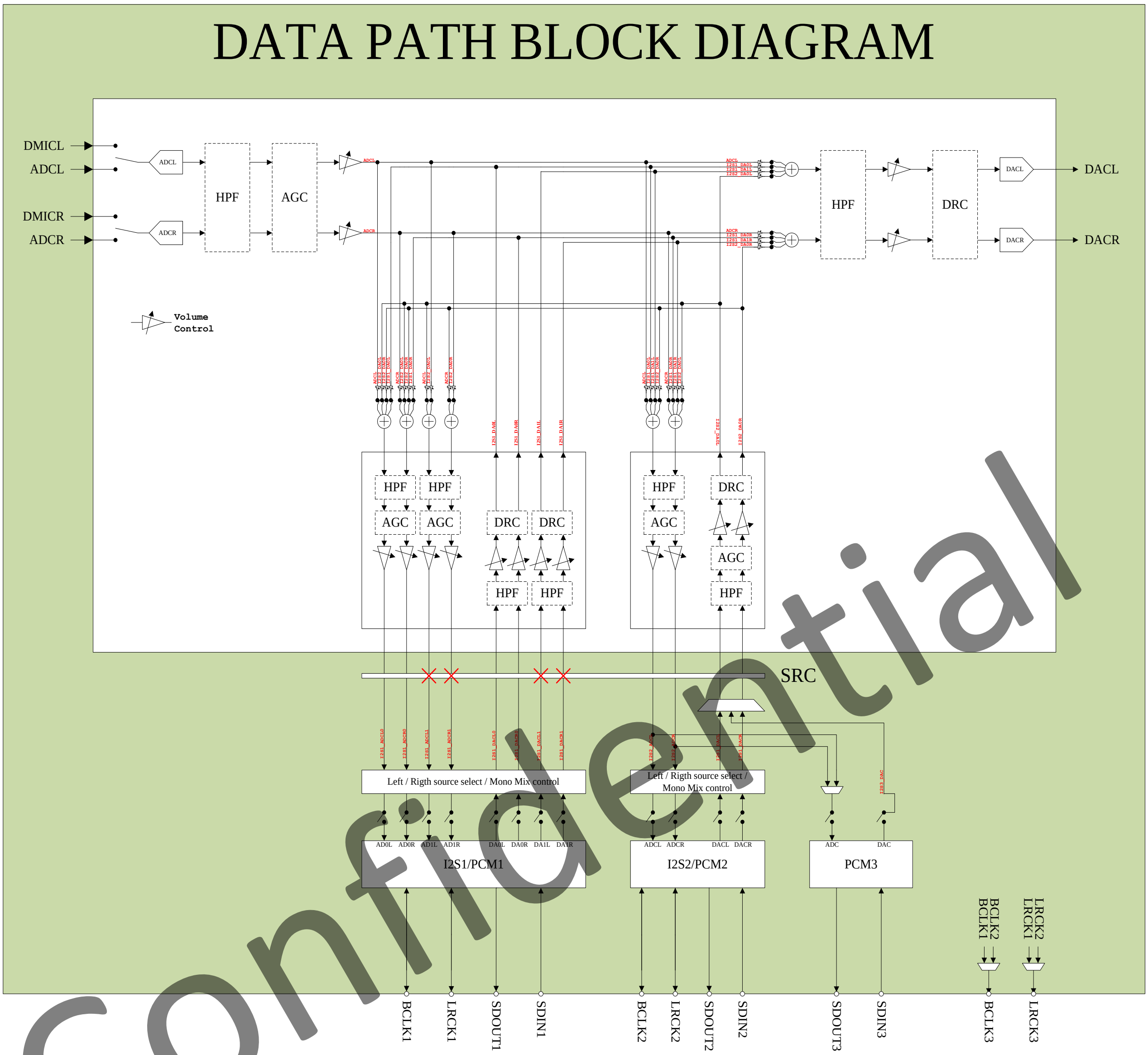


Figure 12-12 Digital Data Path

12.8 Analogue Audio Input Path

The Codec supports five Analogue Audio Input paths:

- LINEINL/R
- AXIL/R
- MIC1P/N,MIC2P/N,MIC3P/N

12.8.1 Microphone Input

MICIN1P/N, MICIN2P/N, MIC3INP/N provide differential input that can be mixed into the ADC record mixer, or DAC output mixer. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. There are only two microphone pre-amplifiers for the 3 differential microphone inputs. MICIN1P/N are input to the first pre-amplifier, MICIN2P/N & MICIN3P/N are selected to input the 2nd pre-amplifier by the register ADC_SRCBST_CTRL bit7. Each microphone preamplifier has a separate enable bit, ADC_SRCBST_CTRL Bit15 & Bit11. The gain for each pre-amplifer can be set independently using MIC1BOOST, MIC2BOOST. MBIAS provide reference voltage for electret condenser type(ECM) microphones.

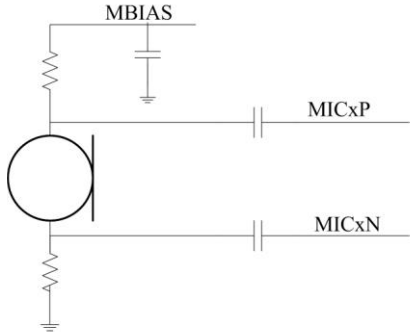


Figure 12-13 Suggested External Microphone Input

12.8.2 AXIL/R Input

Auxiliary inputs AXIL and AXIR provide 2-channel stereo single-ended input that can be mixed into the DAC output mixer and ADC record mixer. The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external audio equipment or audio FM module .

Both auxiliary inputs include programmable volume level adjustments and ADC input mute. The scheme is illustrated below. Passive RF and active Anti_Alias filters are also incorporated within the auxiliary inputs. These prevent high frequencies aliasing into the audio band , otherwise degrading performance.

The gain between the AXI inputs and the ADC is logarithmically adjustable from -9dB to 12dB in 1.5dB step by the register AXI_PREG set. The ADC Full Scale input is 1.0Vrms at AVCC =3.0volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVCC.

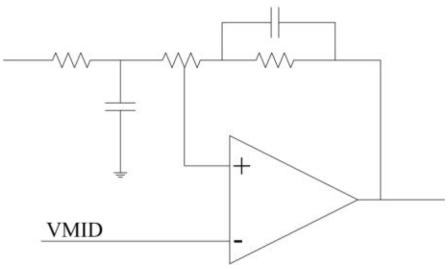


Figure 12-14 AXI Input Schematic

12.8.3 LINEINL/R Input

LINEINL/R provide one-channel mono differential input or stereo single-ended input that can be mixed

into the ADC record mixer or the stereo output mixer. The inputs are suited to receiving line level signals such as external audio equipment or baseband module .
When the linein input is set as differential signal input LINEINL-LININR to the ADC or to DAC mixer, the linein gain is logarithmically adjustable from -9dB to 12dB in 1.5dB step by the register LINEIN_DIFF_PREG set.

12.9 Analogue Audio Output Path

The Codec supports five Analogue Audio Output paths:

- HPOUTL/R, HPOUTFB
- SPOLP/N
- SPORP/N
- EAROUTP/N
- LINEOUTP/N

12.9.1 Headphone Output

HPOUTL/R provides two-channel single-ended output to headphone driver. The HPOUTL/R PA input source can be selected from output mixer or directly from DAC by register HPOUT_CTRL Bit15 & Bit14 set. It also can be muted by register HPOUT_CTRL Bit13 & Bit12 set. The headphone PA power up or down by register HPOUT_CTRL Bit11 set.
HPOUTL/R can drive a 16R or 32R headphone load without DC capacitors by using Charge Pump to generate the negative rails. HPOUTFB is the ground loop noise rejection feedback. HBIAS provides reference voltage for electret condenser type(ECM) microphones. Audio jack insert/ button press detection function is also provided through measuring the HBIAS current.

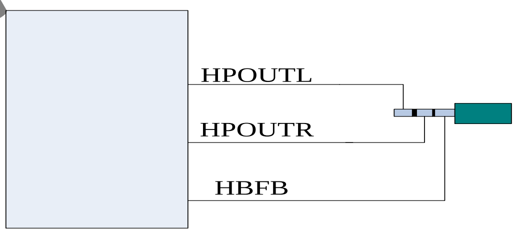


Figure 12-15 Suggested Headphone Output Application

HPOUTL/R volumes can be independently adjusted under software control using the HP_VOL[5:0] of the headphone output control registers. The adjustment is logarithmic with an 64dB rang in 1dB step from 0dB to -62dB. The headphone outputs can be muted by writing codes 0x0 to HP_VOL[5:0] bits.
There are a DC offset cancellation circuit to remove the headphone output DC offset for preventing POP noise in AXP813. The function can be enabled or disabled by the register HP_DCRM_EN.   This bit must be set 0xf before headphone PA enabled, and this bit must be set 0x0 before headphone PA disabled.
A zero cross detect circuit is provided at the input to the headphones under the control of the ZCROSS_EN bit . Using these controls the volume control values are only updated when the input signal to the gain stage is close to the analogue ground level. This minimizes and audible clicks and zipper noise as the gain values are changed or the device muted.

12.9.2 Earpiece Output

EAROUTP/N provides one differential output to drive handset receiver. The EAROUTP/N input source can be selected from left DAC, right DAC, left output mixer or right output mixer. The earpiece volume controlled by the register ERPOUT_CTRL Bit4:0 set. The volume control is logarithmic with an 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The earpiece PA power up or down by register ERPOUT_CTRL Bit5set.

12.9.3 Speaker Output

SPOLP/N, SPORP/N provides two differential output without internal speaker amplifier. Using external amplifier, a stereo speakers can be implemented. The SPOLP/N input source can be selected from left output mixer or (left+right) output mixer. The SPORP/N input source can be selected from right output mixer or (left+right) output mixer. So in mono speaker application, The best choice for SPOLP/N or SPORP/N input source is selected from (left+right) output mixer avoiding sound loss. The volume control is logarithmic with a 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The left and right speaker output buffer can independently power up or down by register SPKOUT_CTRL Bit11 & Bit7 set.

12.9.4 Line Output

LINEOUTP/N provides one differential BTL output to drive line level signals to external audio equipment or baseband module .The LINEOUTP/N input source can be selected from MIC1 pre-amplifier output, MIC2 pre-amplifier output, left output mixer or right output mixer. The volume control is logarithmic with an 10.5dB rang in 1.5dB step from -4.5dB to 6dB. The LINEOUT output buffer power up or down by register LOUT_CTRL Bit4 set.

12.10 Digital Microphone Interface

AXP813 supports a stereo digital microphone interface. The DMICCLK/ DMICDAT pins are multiplexed on the MIC3P/MIC3N pins. The circuit share decimation filter with audio ADC. And DMICCLK can be output 128fs (fs= ADC sample rate).

Digital Microphone power usually falls between the range 1.6V-3.6V, typical 1.8V. And the Clock frequency is between the range 1.0MHz-3.25MHz, typical 2.4MHz.

Digital Microphone Block Diagram as the figure 12-16:

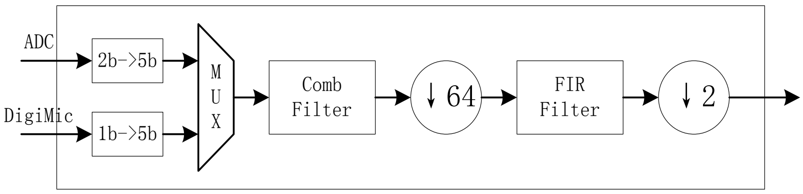


Figure 12-16 Digital Microphone Block Diagram

Digital Microphone timing as the figure 12-17:

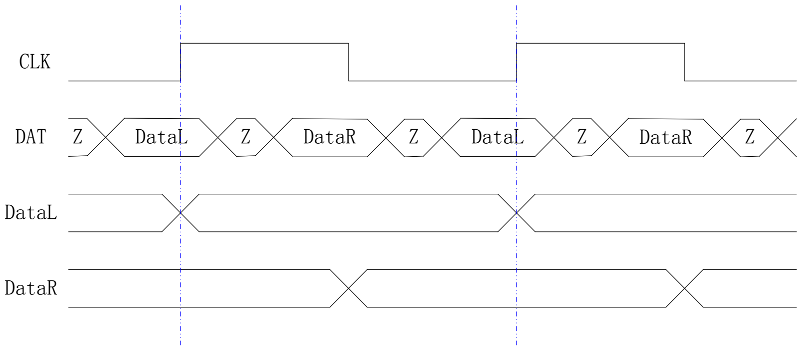


Figure 12-17 Digital Microphone timing

Digital Microphone application as the figure 12-18:

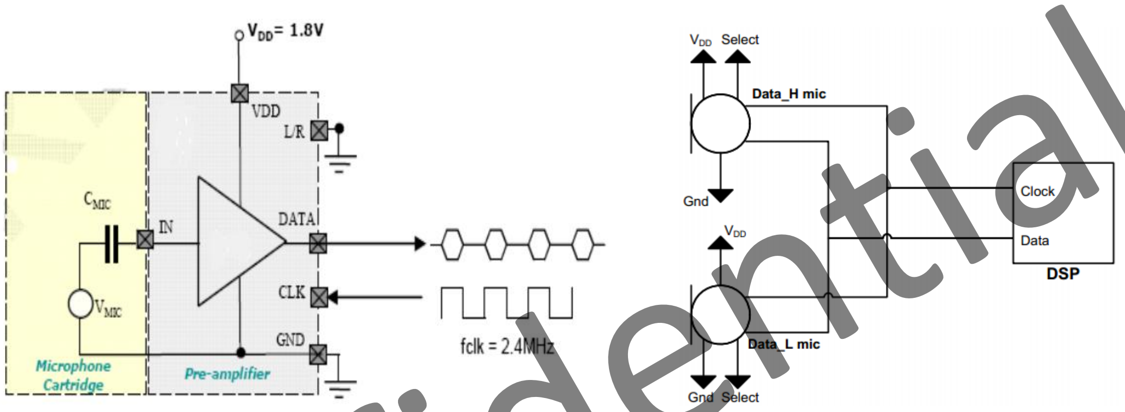


Figure 12-18 Digital Microphone Application

12.11 Audio Jack Detect

The microphone bias output pin HBIAS provide a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network. Hbias is designed to drive headset microphone, and a bias current detect function is provided for external accessory detection by measuring the Hbias current. In some application, it's used to detect the insertion/removal of an audio jack and the button press. These events will cause a significant change in bias current flow, which can be detected and used to generate a signal to the processor.

When HBIAS current detect is enabled, 5 bit ADC will send out sample data at 16/32/64/128Hz clock rate. Digital logic trigger an interrupt event controlled by register setting when the data is changed.

The digital circuit generates five IRQ signals that can be disabled by register, the data from ADC can be read from register HMIC_STATUS Bit12:8.

IRQ Timing Diagram shows in figure 12-19:

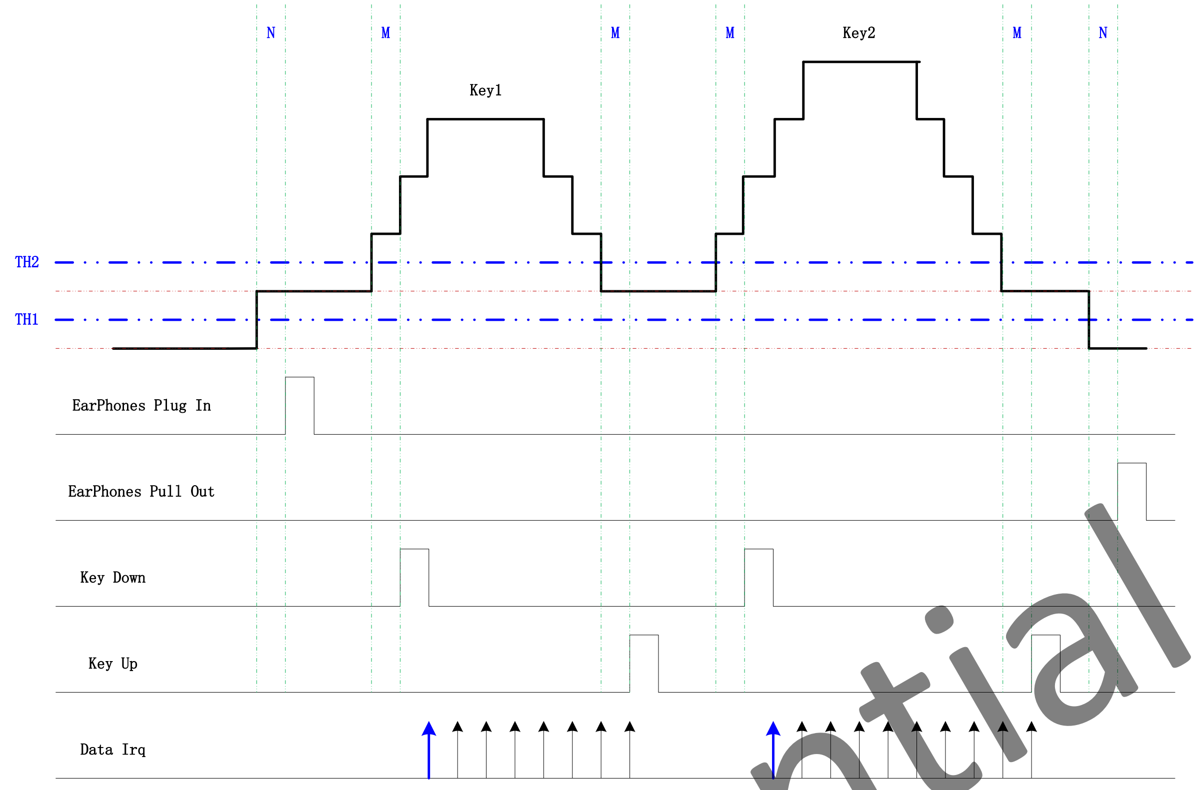


Figure 12-19 HBIAS Detect IRQ Timing Diagram

12.13 Interrupt

The Interrupt circuits in AXP813 generate an Interrupt (IRQ) event to enable the detection of audio jack status. The Interrupt pin IRQ_AUDIO is open-drain. It's usually drives a high level voltage via the external pull-up resistor while it output a low level when the IRQ is active.

It supports the following triggered events illustrated in the figure 12-20:

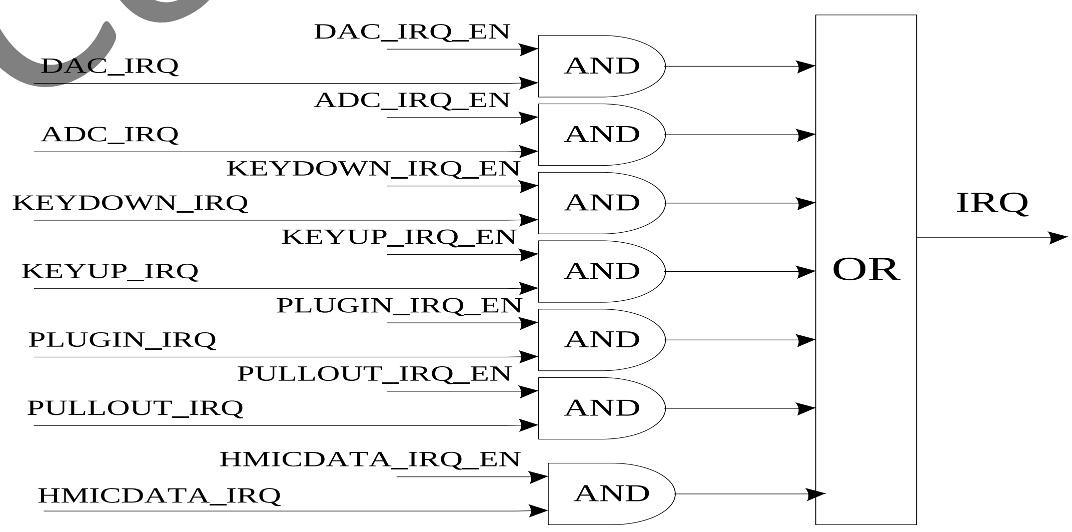


Figure 12-20 Interrupt trigger Diagram

12.14 Digital Audio Process for ADC

Figure 12-21 shows the DAP System Block Diagram for ADC.

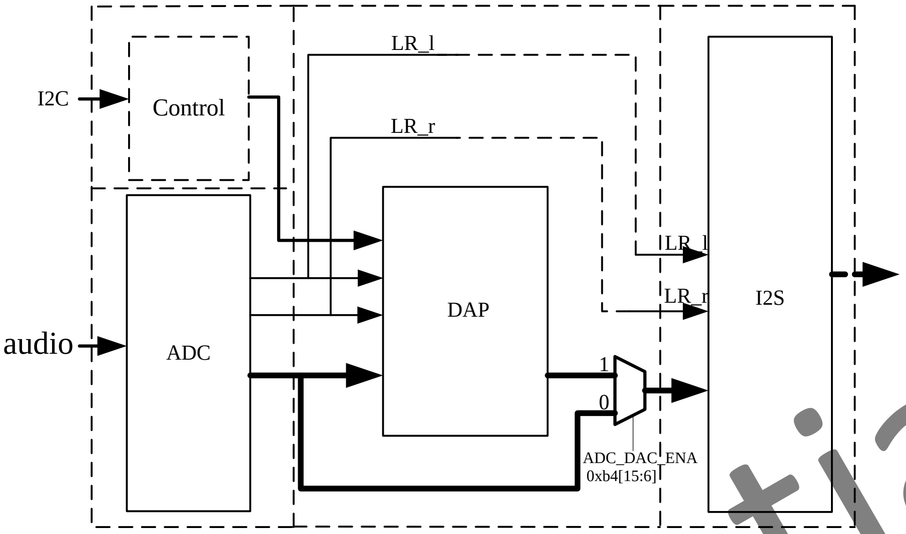


Figure 12-21 ADC DAP System Block

Figure 12-22 shows DAP for ADC Data Flow:

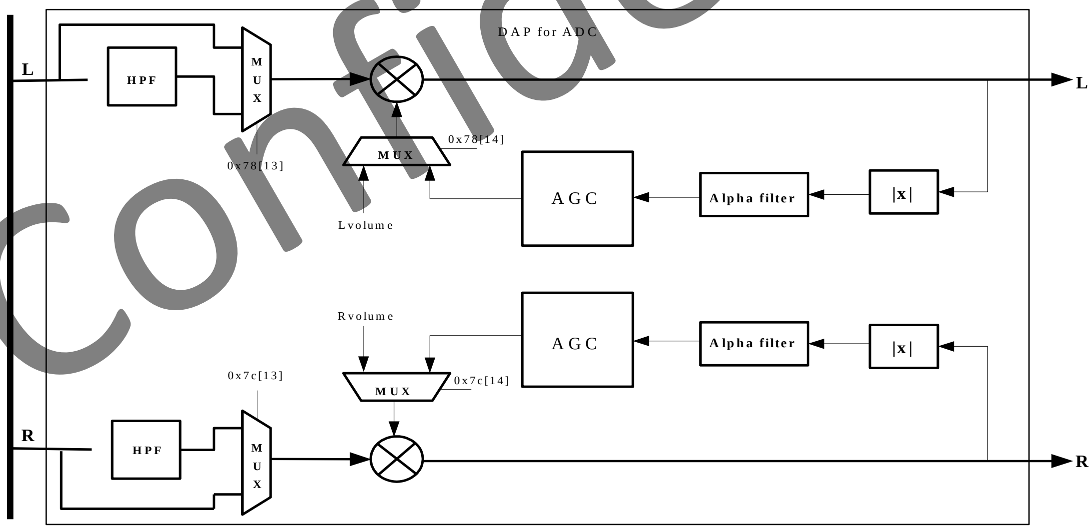


Figure 12-22 ADC DAP Data Flow

12.14.1 High Pass Filter

The High Pass Filter (HPF, –3dB cutoff < 1Hz) remove DC offset from ADC recording data. The HPF can also be bypassed.

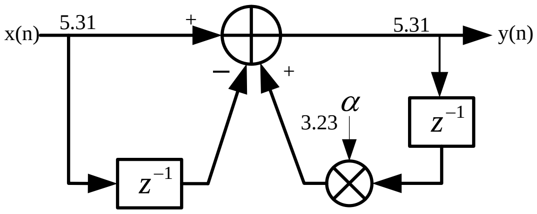


Figure 12-23 HPF Characteristic in DAP

12.14.2 Auto Gain Control

The automatic gain control(AGC) can be enabled in the digital recording path of AXP813. It automatically adjusts the ADC recording volume gain to a target volume level.

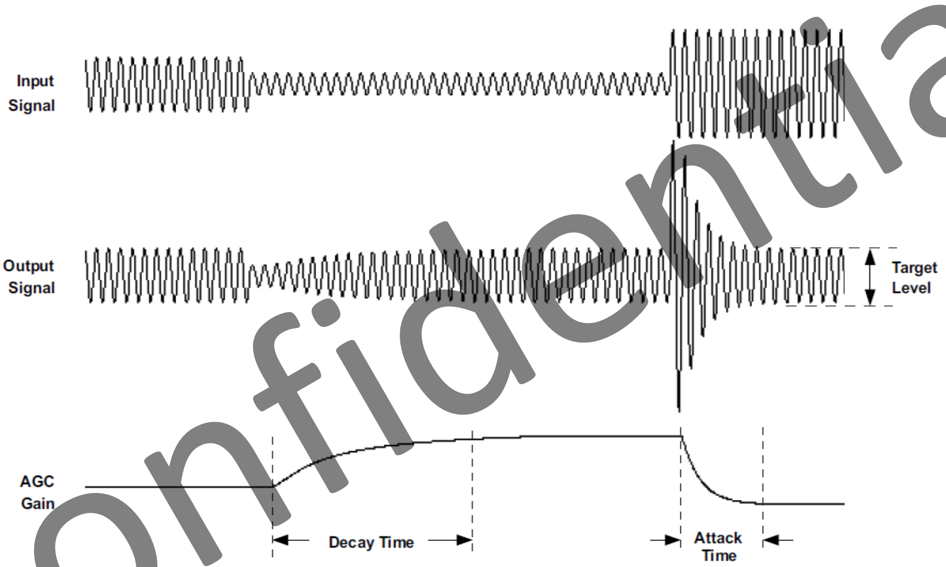


Figure 12-24 AGC Response Characteristic

The ADC Digital Part includes automatic gain control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or weak, such as when a person speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine-tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Because the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate. The AGC programs to a wide range of attack and decay skew time from 32/fs to 2^15*32/fs.

When noise cancellation used in system, the AGC should be implement by soft because of no hardware noise cancellation. The AGC process should be after noise cancellation process.

- **The AGC Control Parameters**

·**Target level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The ADC allows programming of different target levels, which can be programmed from –1dB to –30dB relative to a full-scale signal. Because the ADC reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margins to avoid clipping at the occurrence of loud sounds.

·**Attack skew time** determine show quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. A wide range of attack-time programmability is supported in terms of number of samples (i.e., number of ADC sample-frequency clock cycles).

·**Decay skew time** determine show quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. A wide range of decay time programmability is supported in terms of number of samples (i.e., number of ADC sample-frequency clock cycles).

·**Noise threshold** is a reference level. If the input speech average value falls below the noise threshold, the AGC considers it as asilence and hence brings down the gain to 0dB in steps of 0.5dB every sample period and sets the noise-threshold flag. The gain stay sat 0dB unless the input speech signal average is es above the noise threshold setting. This ensures that noise is not amplified in the absence of speech. Noise threshold level in the AGC algorithm is programmable from –30dB to –90dB of full-scale. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0dB when signals are near the noise threshold level. The noise (or silence) detection feature can be entirely disabled by the user.

·**Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA applicable can be programmed from 0dB to 40dB in steps of 0.5dB.

·**Hysteresis**, as the name suggests, determines a window around the noise threshold which must be exceeded to detect that the recorded signal is indeed either noise or signal. If initially the energy of the recorded signal is greater than the noise threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the noise threshold by a value given by hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the noise threshold by a value given by the hysteresis setting. In order to prevent the AGC from jumping between noise and signal states, (which can happen when the energy of recorded signal is close to the noise threshold) a non-zero hysteresis value should be chosen. The hysteresis feature can also be disabled.

·**Debounce time** (noise and signal) determines the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set noise threshold, then the AGC does not increase the input gain to achieve the target level. However, to handle audible artifacts which can occur when the energy of the input signal is close to the noise threshold, the AGC checks if the energy of the recorded signal is less than the noise threshold for a time greater than the noise debounce time. Similarly, the AGC starts increasing the input-signal gain to reach the target level when the calculated energy of the input signal is greater than the noise threshold. Again, to avoid audible artifacts when the input-signal energy is close to noise threshold, the energy of the input signal must continuously exceed the noise threshold value for the signal-debounce time. If the debounce times are kept small, then audible artifacts can result by rapid enabling and disabling the AGC function. At the same time, if the debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signals with respect to the noise threshold. Both noise and signal-debounce time can be disabled.

- **The AGC Output Information**

·The AGC noise-threshold flag is a read-only flag indicating that the input signal has levels lower than the noise threshold, and thus is detected as noise (or silence). In such a condition, the AGC applies a gain of 0 dB.

·Gain applied by AGC is a read-only register setting which gives a real-time feed back to the system on the gain applied by the AGC to the recorded signal. This, a long with the target setting, can be used to determine the input signal level. In a steady-state situation TargetLevel (dB) = GainAppliedbyAGC(dB) +Input Signal Level(dB) When the AGC noise threshold flag is set, then the status of gain applied by AGC is not valid.

·The AGC saturation flag is a read-only flag indicating that the ADC output signal has not reached its target level. However, the AGC is unable to increase the gain further because the required gain is higher than the maximum allowed PGA gain. Such a situation can happen when the input signal has low energy and the noise threshold is also set low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.

·The ADC saturation flag is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC target level is kept high and the energy in the input signal increases faster than the attack time.

- **The AGC signal level detect**

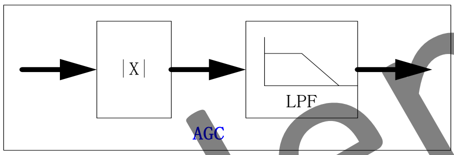


Figure 12-25 AGC Signal level detect

· **An AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low-pass filter is in the form of a first-order IIR filter. The transfer function of the filter implemented for signal level detection is given by

$$H(z) = \frac{\alpha}{1 - (1 - \alpha) z^{-1}}$$

Where: Coefficient α (3.24 format) is 26-bit 2s complement and will determine the time window over which average level to be made. The parameter is computed by.

$$\alpha = 1 - e^{-2.2Ts/ta}$$

Default time window is 108.8963 *Ts.

- **The AGC Characteristics**

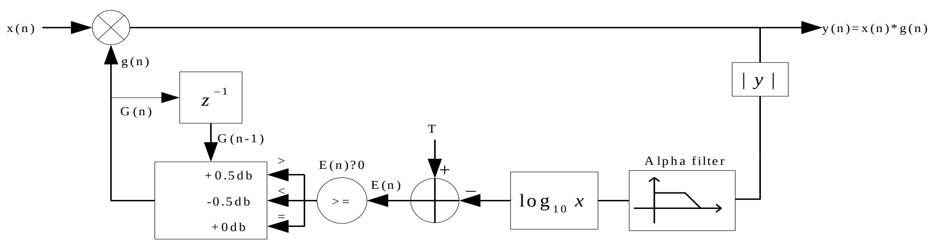


Figure 12-26 AGC Module Characteristic

12.15 Digital Audio Process for DAC

Figure 12-27 shows the DAP System Block Diagram For DAC.

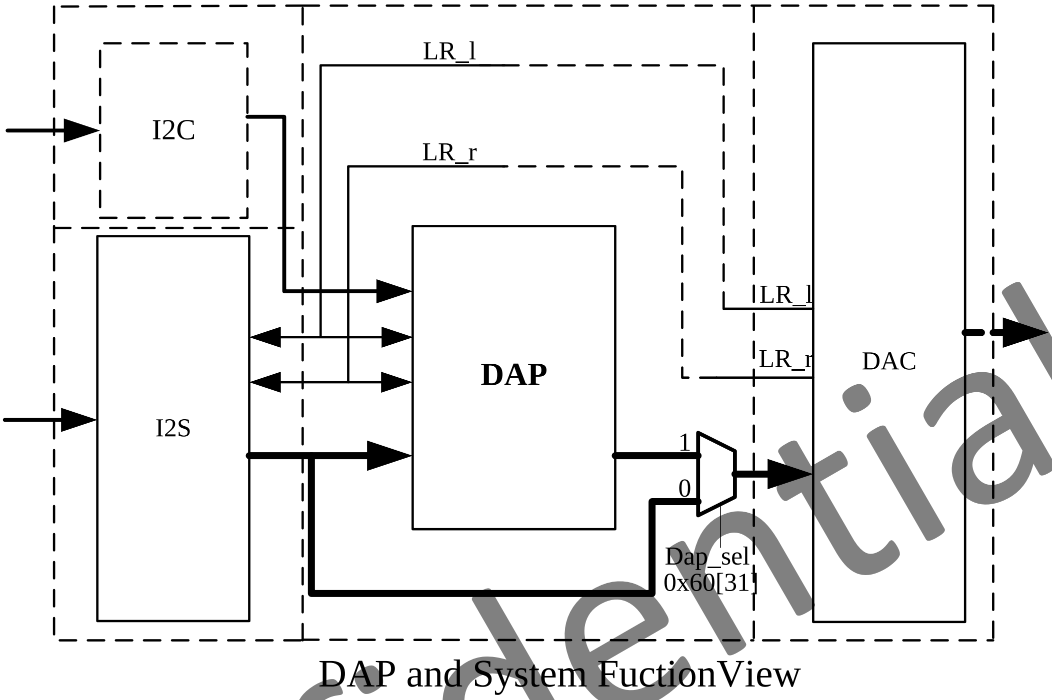


Figure 12-27 DAC DAP System Block

Figure 12-28 shows DAP for DAC Data Flow:

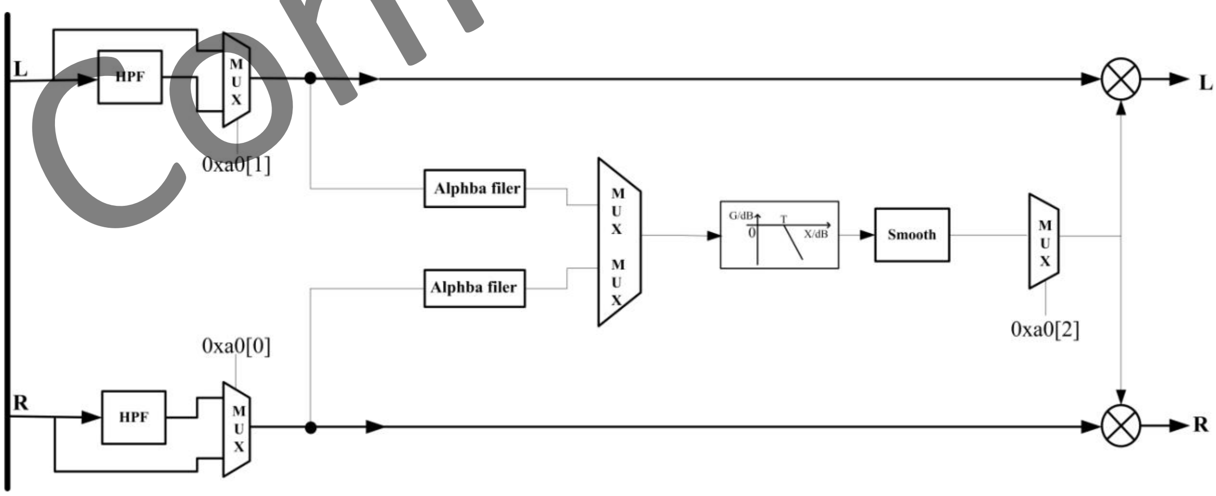


Figure 12-28 DAC DAP Data Flow

12.15.1 High Pass Filter

The DAP has individual channel high pass filter that can be enabled and disabled. The filter cutoff frequency is less than 1Hz.

$$H(z) = \frac{1 - z^{-1}}{1 - az^{-1}}$$

12.15.2 Dynamic Range Control

The dynamic range control(DRC) can be enabled in the digital playback path of AXP813. It automatically adjusts the wide volume gain to flatten volume level .Figure 12-29 shows DRC Response characteristic.

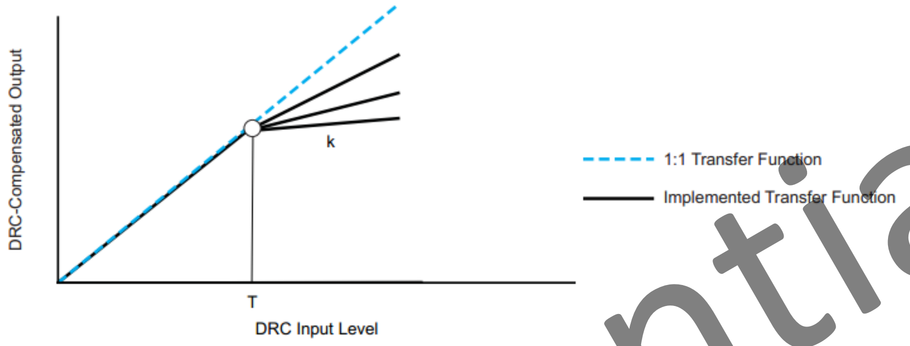


Figure 12-29 DRC Response Characteristic

The DRC supports the main feature shows in figure 12-30.

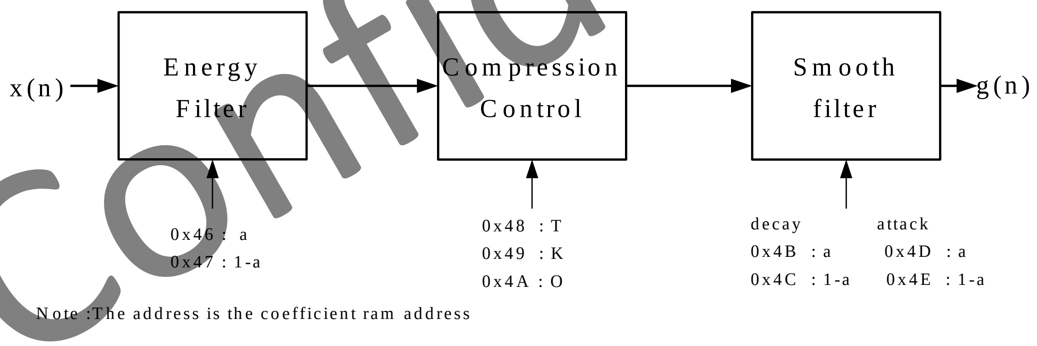


Figure 12-30 DRC Block and Register Control

- Adjustable threshold, offset, and compression levels
- Programmable energy coefficient, attack, and decay time constants
- Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

◆ **DRC parameter setting**

Numbers formatted as N.M numbers means that there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 3.24 means that there are 3 bits at the left of the decimal point and 24 bits at the right decimal point.

◆ **Energy Filter**

The Energy Filter is to estimate of the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by $\alpha = 1 - e^{-2.2Ts/ta}$

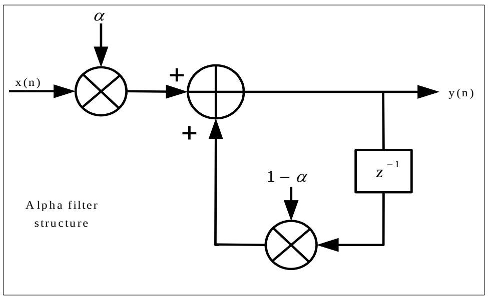


Figure 12-31 Energy Filter Structure

- **Compression Control**

This element has three parameters (T, K, O), which are all programmable, and the computation will be explained as below:

T parameter (Threshold Parameter Computation)

The threshold is the value that determines the signal to be compressed or not. When the signal's RMS is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by

$$Tin = -\frac{T_{dB}}{6.0206}$$

There, T_{dB} must less than zero, the positive value is illegal.

For example, it desired to set the T=-30dB, then $T_{in} = -\frac{-30}{6.0206} = 4.982$, and the 8.24 format of the Tin is 0x04FB_9ED0.

K parameter (Slope Parameter Computation)

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB as RMS input increase n dB. The k input to the coefficient register is computed by

$$k = \frac{1}{n} - 1$$

There, n is from 1 to 50, and must be integer.

For example, for n=5, the $k = \frac{1}{5} - 1 = -0.8$, and the 3.23 format of the k is 0x733_3333

O parameter (Offset Parameter Computation)

The *O* is the offset of the compression static curve. The offset input to the coefficient register is computed by $O_{in} = 10^{O/20}$

There, *O* is -24dB to 24dB.

For example, it desired to set O=6dB, then $O_{in} = 10^{6/20} = 1.995$, and the 5.24 format of the O_{in} is 0x1FE_C982.

◆ **Gain Smooth Filter**

The Gain Smooth Filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 12-32. The structure of the Gain Smooth filter is also the Alpha filter, so the rise time computation is the same as the Energy filter which is

$$\alpha = 1 - e^{-2.2Ts/ta}$$

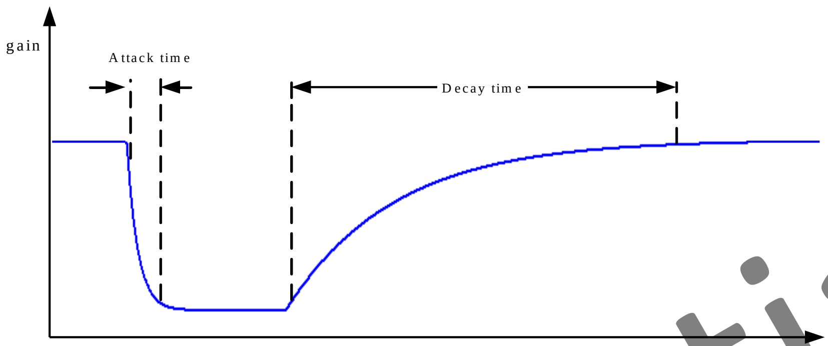


Figure 12-32 Smooth Filter Characteristic

12.16 RTC Module

There is a real time clock(RTC) module in AXP813 for calendar usage. The RTC module provides second, minute, hour, weekday, day, month, and year information as well as alarm wakeup. The external 32.768kHz crystal oscillator is need to provide a low power, accurate reference.

The RTC fans out three 32.768 kHz outputs CKO1_RTC, CKO2_RTC, and CKO3_RTC derived from external oscillator, while the source also can be configured as 4MHz frequency dividing output from ADDA oscillator. The outputs are controlled by register CK32K_OUT_CTRLx(x=1,2,3). The first output CKO1_RTC is push-pull pin connected with AP, the CKO2_RTC and CKO3_RTC outputs are open-drain pins for other components such as baseband, or wifi module.

The general purpose registers e0h-efh are used for storing data, since the RTC domain is always power-on. Figure 12-33 shows the block diagram of the RTC:

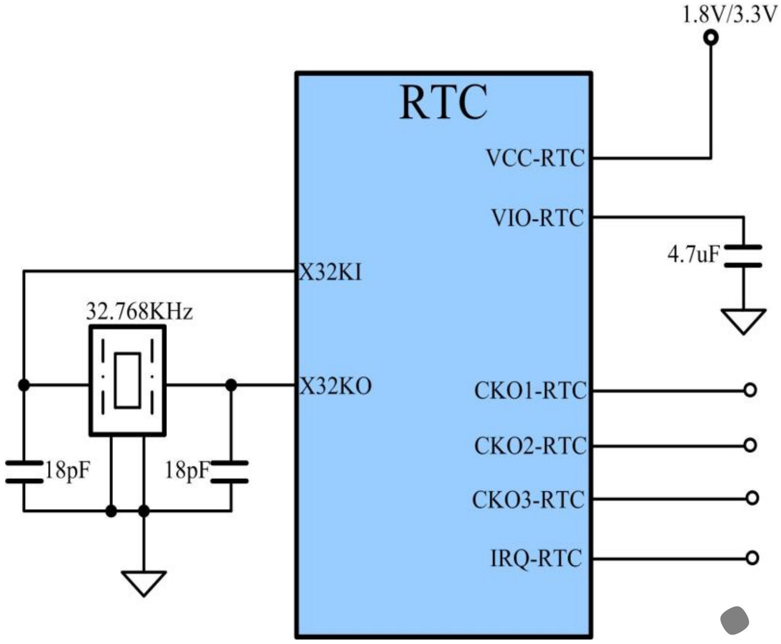


Figure 12-33 RTC Block Diagram

13 TWSI/RSB Interface

AXP813 can support two series control interface protocol for writing to or read back from registers on SCK and SDA pins . One is TWSI interface, the other is RSB interface. RSB is top-priority for higher efficiency and lower power consumption. When using TWSI interface, there are two slave address,7'H34 is for Power Management and 7'H1A is for Codec, and when using RSB interface, there are two slave address too,15'H01D1 is for Power Management and 15'H0744 is for Codec.

13.1 TWSI Interface

TWSI is a 2-wire (SCK/SDA) half-duplex serial communication interface, supporting only slave mode. SCK is used for clock and SDA is for data. SCK clock supports up to 400 KHz rate and SDA data is a open drain structure.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave address. It is a 7-bit chip address followed by a R/W bit. If accessing the registers of Codec, the chip address must be 0011010x, if accessing the registers of Power Management, the chip address must be 0111000x. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCK is high.

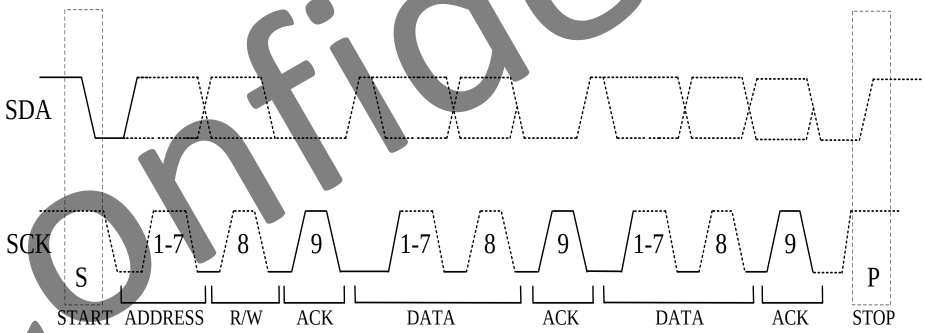


Figure 13-1 TWSI Interface

The formats of “write” and “read” instructions are shown in figure 13-2.

Write Word Protocol

1	7	1	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	Data Byte High	A	P

Read Word Protocol

1	7	1	1	8	1	1	8	1	1	8	1	8	1	1
S	Device Address	Wr	A	Register Address	A	S	Device Address	Rd	A	Data Byte High	A	Data Byte Low	A	P

S: start Condition

Slave Address: 7-bit Device Address

Wr: 0 for Write Command

Rd: 1 for Read Command

Command Code: 8-bit Register Address

A: 0 for ACK, 1for NACK

Data Byte: 16-bit Mixer data

□ : Master-to-Slave

■ : Slave-to-Master

Figure 13-2 TWSI Read and Write

13.2 RSB Interface

RSB interface supports a special protocol with a simplified two wire protocol on a push-pull bus. So the transfer speed can be up to 10MHz and the performance will be improved much. AXP813 works only in slave mode.

RSB support multi-slaves. It uses CK as clock and uses CD to transmit command and data. The Bus Topology is showed in figure 13-3.:

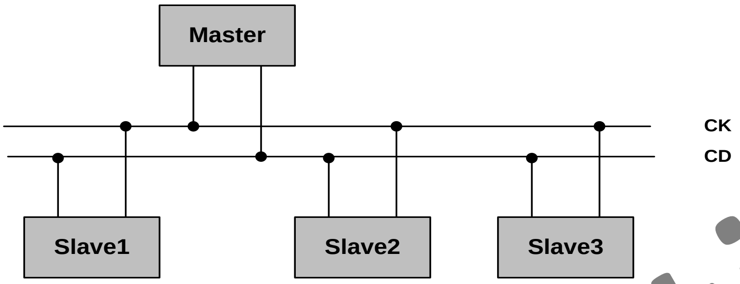


Figure 13-3 RSB Bus Topology

The start bit marks the beginning of a transaction with the slave device. When CK is high, a change from high to low on CD is defined as a start condition. This start condition notifies the selected device to start a transfer.

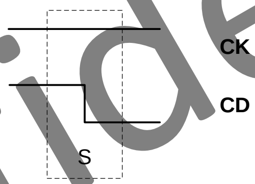


Figure 13-4 Start signal

RSB protocol uses parity bit to check the correction of every byte,The checked object is the 7, 8 or 15 bit in front of the parity bit.

ACK bit is the acknowledgement from device to host, The ACK is active low. When device finds the parity bit is error, it will not send ACK to host, so host can know that an error happens in the transaction.

7	6	5	4	3	2	1	0	C

Figure 13-5 Parity bit

Set run-time slave address(RTSADDR) command. It is used to set run time slave address(RTSADDR) for different devices in the same system. There are 15 devices in a system at most. The RTSADDR can be selected from the command code set and a device 's RTSADDR can be modified many times by using set run-time slave address command.

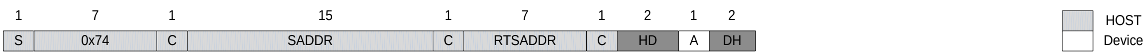


Figure 13-6 RTSADDR command

Read command is used to read data from device. It has byte, half word and word operation. When devices receives the command, they shall check if the command's RTSADDR matches their own RTSADDR. The device's RTSADDR is set by set run-time slave address(RTSADDR) command.

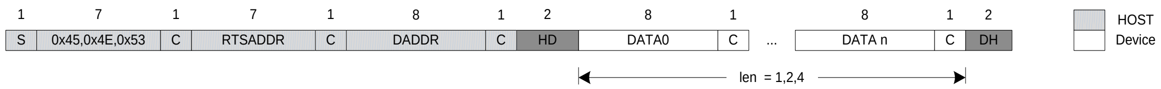


Figure 13-7 Read command

Write command is used to write data to the devices. It has byte, half word and word operation. When devices receive the command, they shall check if the command's RTSADDR matches their own RTSADDR. The device's RTSADDR is set by set run-time slave address(RTSADDR) command.

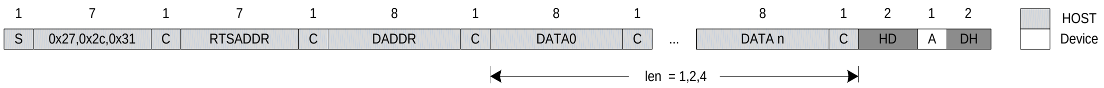


Figure 13-8 Write command

14 Power Management Register

Note: hereinafter, "system reset" means that the Register will be reset when the AXP813 power off, and "power on reset" means that the Register will be reset when IPSOUT voltage drop below 2.1V .

Register List

Address	Description	R/W	Default
00	Power source status	R	
01	Power mode and Charger status	R	
02	Power up/down reason register	RW	
03	IC type number	R	51H
04-0F	12 Data buffers	RW	00H
10	Output power on-off control 1	RW	XXH
12	Output power on-off control 2	RW	08H
13	Output power on-off control 3	RW	9CH
14	On/Off synchronous control	RW	48H
15	DLDO1 voltage control	RW	16H
16	DLDO2 voltage control	RW	16H
17	DLDO3 voltage control	RW	16H
18	DLDO4 voltage control	RW	1AH
19	ELDO1 voltage control	RW	00H
1A	ELDO2 voltage control	RW	00H
1B	ELDO3 voltage control	RW	00H
1C	FLDO1 voltage control	RW	0BH
1D	FLDO2/3 voltage control	RW	0BH
20	DCDC1 voltage control	RW	02H
21	DCDC2 voltage control	RW	B2H
22	DCDC3 voltage control	RW	XXH
23	DCDC4 voltage control	RW	B2H
24	DCDC5 voltage control	RW	XXH
25	DCDC6 voltage control	RW	B2H
26	DCDC7 voltage control	RW	B2H
27	DCDC4/2/3/4/5 DVM control	RW	XCH
28	ALDO1 voltage control	RW	17H
29	ALDO2 voltage control	RW	17H
2A	ALDO3 voltage control	RW	1AH
2C	BC Module Global Register	RW	00H
2D	BC Module VBUS Control and Status Register	RW	30H
2E	BC USB Status Register	RW	00H
2F	BC Detect Status Register	R	20H
30	VBUS path control & Hold voltage setting	RW	21H

31	Power wakeup control & V_{OFF} setting	RW	03H
32	Power Disable, BAT detect and CHGLED pin control	RW	4XH
33	Charger Control 1	RW	CXH
34	Charger Control 2	RW	45H
35	Charger Control 3	RW	18H
36	POK setting	RW	59H
37	POK Power off activity time setting	RW	00H
38	$V_{LTF\text{-}charge}$ setting	RW	A5H
39	$V_{HTF\text{-}charge}$ setting	RW	1FH
3A	Reserved	RW	XXH
3B	BUCK frequency setting	RW	08H
3C	$V_{LTF\text{-}work}$ setting	RW	FCH
3D	$V_{HTF\text{-}work}$ setting	RW	16H
3E	Reserved	RW	XXH
40	IRQ enable 1	RW	D8H
41	IRQ enable 2	RW	FFH
42	IRQ enable 3	RW	FFH
43	IRQ enable 4	RW	03H
44	IRQ enable 5	RW	7CH
45	IRQ enable 6	RW	00H
48	IRQ Status 1	RW	00H
49	IRQ Status 2	RW	00H
4A	IRQ Status 3	RW	00H
4B	IRQ Status 4	RW	00H
4C	IRQ Status 5	RW	00H
4D	IRQ Status 6	R	00H
58	TS pin input ADC data, highest 8bit	R	00H
59	TS pin input ADC data, lowest 8bit	R	00H
5A	GPIO0 pin input ADC data, highest 8bit	R	00H
5B	GPIO0 pin input ADC data, lowest 8bit	R	00H
78	Average data bit[11:4] for Battery voltage (BATSENSE)	R	00H
79	Average data bit[3:0] for Battery voltage (BATSENSE)	R	00H
7A	Average data bit[11:4] for Battery charge current	R	00H
7B	Average data bit[3:0] for Battery charge current	R	00H
7C	Average data for Battery discharge current highest 8 bit	R	00H
7D	Average data for Battery discharge current lowest 4 bit	R	00H
80	BUCK PWM/PFM mode select	RW	80H
81	Off-Discharge and Output monitor control	RW	FFH
82	ADC Enable	RW	E1H
84	ADC speed setting, TS pin Control	RW	F2H
85	ADC speed setting	RW	B0H
8A	Timer control	RW	00H
8E	Buck output voltage monitor de-bounce time setting	RW	00H/00H/40H

8F	IRQ pin, hot-over shut down	RW	00H
90	GPIO0(GPADC) control	RW	07H
91	GPIO0LDO and GPIO0 high level voltage setting	RW	1AH
92	GPIO1 control	RW	07H
93	GPIO1LDO and GPIO1 high level voltage setting	RW	1AH
94	GPIO signal bit	R	00H
97	GPIO pull down control	RW	00H
9A	Run time Sleep power up sequence 1	RW	00H
9B	Run time Sleep power up sequence 2	RW	00H
9C	Run time Sleep power down sequence 1	RW	00H
9D	Run time Sleep power down sequence 2	RW	00H
9E	Power rail mode in Sleep state	RW	00H
A0	Real time data bit[11:4] for Battery voltage (BATSENSE)	R	00H
A1	Real time data bit[3:0] for Battery voltage (BATSENSE)	R	00H
B8	Fuel Gauge Control	RW	E8H
B9	Battery capacity percentage for indication	R	64H
BA	RDC 1	RW	80H
BB	RDC 0	RW	5DH
BC	OCV 1	R	00H
BD	OCV 0	R	X0H
E0	Battery maximum capacity	RW	00H
E1	Battery maximum capacity	RW	00H
E2	Coulomb meter counter	RW	00H
E3	Coulomb meter counter	RW	00H
E4	OCV Percentage of battery capacity	R	64H
E5	Coulomb meter percentage of battery capacity	R	64H
E6	Battery capacity percentage warning level	RW	A0H
E8	Fuel gauge tuning control 0	RW	00H
E9	Fuel gauge tuning control 1	RW	00H
EA	Fuel gauge tuning control 2	RW	00H
EB	Fuel gauge tuning control 3	RW	00H
EC	Fuel gauge tuning control 4	RW	00H
ED	Fuel gauge tuning control 5	RW	00H

REG 00H: Power source status

Bit	Description	R/W
7	ACIN presence indication 0- ACIN not presence （VBUS<3.5V） 1- ACIN presence （VBUS>4.1V）	R
6	Indication of ACIN valid (ACIN_Val)	R
5	VBUS presence indication 0- VBUS not presence （VBUS<3.5V）	R

	1- VBUS presence （VBUS>4.1V）	
4	Indication of VBUS valid (VBUS_Val)	R
3	VBAT>3.5V or not	R
2	Indication Battery current direction 0: Battery discharge 1: Charging battery	R
1	Indication ACIN and VBUS are shorted or not on PCB,IN_SHORT status	R
0	STARTUP_TRIGGER: indicate the startup trigger is VBUS or not 0: startup trigger is not VBUS; 1: startup trigger is VBUS	R

REG 01H: Power mode and Charger status

Bit	Description	R/W
7	Indication AXP813 die over temperature or not 0-not over temperature; 1-over temperature	R
6	Charging indication 0-Charger is not charging or charging is done; 1-Charger is charging	R
5	Battery presence indication 0-No Battery is connected to AXP813; 1-Battery is connected	R
4	REG 01H[5] valid flag 0- REG 01H[5] is invalid 1- REG 01H[5] is valid Indicate whether Battery detected or not yet	R
3	Indicate battery safe mode 0-charger is not in battery safe mode; 1-charger is in battery safe mode	R
2:0	Reserved	R

REG 02H: Power up/down reason register

Reset: Power on reset

Bit	Description	R/W	Default
7	Power on key override was the shutdown reason, write 1 to clear	R/W	0
6	SOC initiated cold off was the shutdown reason, write 1 to clear	R/W	0
5	AXP813 UVLO threshold was the shutdown reason, write 1 to clear	R/W	0
4	Cold reset was the start up reason, write 1 to clear	R/W	0
3	SOC initiated Global Reset was the start up reason, write 1 to clear	R/W	0
2	Battery insertion was the start up reason, write 1 to clear, write 1 to clear	R/W	0
1	Charger insertion was the start up reason, write 1 to clear	R/W	0

0	Power on key was the start up reason, write 1 to clear	R/W	0

REG 03H: IC type no

Default : 51H

Bit	Description	R/W
5-4	Reserved	R
7-6& 3-0	IC type No. 010001: IC is AXP813 Others: Reserved	R

REG 04-0FH: 12 Data buffers

Default: 00H
Reset: Power on reset
Note: As long as one of the external powers, batteries or backup batteries exists, this data will be reserved and free from the startup and shutdown influence.

REG 10H: Output power on-off control 1

Default：3FH
Reset: system reset

Bit	Description		R/W	Default
7	Reserved			
6	DCDC7 on-off control	0-off; 1-on	RW	0
5	DCDC6 on-off control	0-off; 1-on	RW	1
4	DCDC5 on-off control	0-off; 1-on	RW	1
3	DCDC4 on-off control	0-off; 1-on	RW	1
2	DCDC3 on-off control	0-off; 1-on	RW	1
1	DCDC2 on-off control	0-off; 1-on	RW	1
0	DCDC1 on-off control	0-off; 1-on	RW	1

REG 12H: Output power on-off control 2

Default：00H
Reset: system reset

Bit	Description	R/W	Default

7	Reserved			
6	DLDO4 on-off control	0-off; 1-on	RW	0
5	DLDO3 on-off control	0-off; 1-on	RW	0
4	DLDO2 on-off control	0-off; 1-on	RW	0
3	DLDO1 on-off control	0-off; 1-on	RW	0
2	ELDO3 on-off control	0-off; 1-on	RW	0
1	ELDO2 on-off control	0-off; 1-on	RW	0
0	ELDO1 on-off control	0-off; 1-on	RW	0

REG 13H: Output power on-off control 3

Default：E8H
Reset: system reset

Bit	Description		R/W	Default
7	ALDO3 on-off control	0-off; 1-on	RW	1
6	ALDO2 on-off control	0-off; 1-on	RW	1
5	ALDO1 on-off control	0-off; 1-on	RW	1
4	FLDO3 on-off control	0-off; 1-on	RW	0
3	FLDO2 on-off control	0-off; 1-on	RW	1
2	FLDO1 on-off control	0-off; 1-on	RW	0
1-0	Reserved			

REG 14H: On/Off synchronous control

Default：00H
Reset: system reset

Bit	Description	R/W	Default
7	Reserved		
6	DCDC2 & 3 poly-phase control 0： no poly-phase 1： dual phase	RW	0
5	DCDC5 & 6 change to poly-phase Buck 0: DCDC5 & 6 is independent, not poly-phase Buck 1: DCDC5 3 & 6 is poly-phase Buck	RW	0
4-0	Reserved		

REG 15H: DLDO1 voltage control

Default：16H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved		
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.3V, 100mV/step	RW	16H

REG 16H: DLDO2 voltage control

Default：16H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.4V, 100mV/step 3.4V-4.2V, 200mV/step	RW	10110

REG 17H: DLDO3 voltage control

Default：16H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 2.9V 0.7V-3.3V, 100mV/step	RW	10110

REG 18H: DLDO4 voltage control

Default：1AH
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.3V	RW	11010

	0.7V-3.3V, 100mV/step		

REG 19H: ELDO1 voltage control

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-1.9V, 50mV/step	RW	00000

REG 1AH: ELDO2 voltage control

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-1.9V, 50mV/step	RW	00000

REG 1BH: ELDO3 voltage control

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-1.9V, 50mV/step	RW	00000

REG 1CH: FLDO1 voltage control

Default：0BH
Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	RW	000

3-0	voltage setting Bit 3-0, default is 1.25V 0.7-1.45V, 50mV/step	RW	1011

REG 1DH: FLDO2/3 voltage control

Default：04H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4	FLDO3 voltage setting 0:DCDC5 / 2 1:FLDOIN/2	RW	0
3-0	FLDO2 voltage setting Bit 3-0, default is 0.9V 0.7-1.45V, 50mV/step	RW	0100

REG 20H: DCDC1 voltage control

Default：11H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, 1.6-3.4V, 100mV/step, default is 3.3V	RW	10001

REG 21H: DCDC2 voltage control

Default：A8H
Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 0.9V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	0101000

REG 22H: DCDC3 voltage control

Default：A8H
Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	0101000

REG 23H: DCDC4 voltage control

Default：A8H
Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.50-1.20V：10mV/step 1.22-1.30V：20mV/step	RW	0101000

REG 24H: DCDC5 voltage control

Default：A6H
Reset: System reset

Bit	Description	R/W	Default			
7	DVM finished or not status bit 0: not finished 1: finished	R	1			
6-0	voltage setting Bit 6-0 0.80-1.12V：10mV/step 1.14-1.84V：20mV/step	RW	DCDC5SET is tied to :	GND	VCC_RTC	Floating
			Type 0	1.5V	1.36V	1.24V
			Type 1	0.9V	1.8V	1.0V

Note：type 0 or 1 set by OTP

REG 25H: DCDC6 voltage control

Default：9EH

Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.60-1.10V： 10mV/step 1.12-1.52V： 20mV/step	RW	0011110

REG 26H: DCDC7 voltage control

Default： A8H
Reset: System reset

Bit	Description	R/W	Default
7	DVM finished or not status bit 0: not finished 1: finished	R	1
6-0	voltage setting Bit 6-0, default is 1.0V 0.60-1.10V： 10mV/step 1.12-1.52V： 20mV/step	RW	0101000

REG 27H: DCDC2 /3 /4 /5 /6/7 DVM control

Default： FCH
Reset: System reset

Bit	Description	R/W	Default
7	DCDC7 DVM on-off control 0: disable; 1: enable	RW	1
6	DCDC6 DVM on-off control 0: disable; 1: enable	RW	1
5	DCDC5 DVM on-off control 0: disable; 1: enable	RW	1
4	DCDC4 DVM on-off control 0: disable; 1: enable	RW	1
3	DCDC3 DVM on-off control 0: disable; 1: enable	RW	1
2	DCDC2 DVM on-off control 0: disable; 1: enable	RW	1

1-0	Reserved		

REG 28H: ALDO1 voltage control

Default：0BH
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0 0.7-3.3V, 100mV/step, default is 1.8V	RW	01011

REG 29H: ALDO2 voltage control

Default：0BH
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 1.8V 0.7-3.3V, 100mV/step	RW	01011

REG 2AH: ALDO3 voltage control

Default：17H
Reset: System reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	voltage setting Bit 4-0, default is 3.0V 0.7-3.3V, 100mV/step	RW	1AH

REG 2CH: BC Module Global Register

Default：00H
Reset: bit7 is system reset, bit[6:0] Power On reset

Bit	Description	R/W	Default
7	**DCD_SEL** **DCD Detect Select** Software writes 1 to this bit to select DCD Detection during BC Detect.	RW	0
6-5	**DCD_TIMEOUT_CTL** **DCD Timeout Control** Software writes these fields to configure the DCD timeout value. When the DCD_SEL is set, the BC Module read the MultValIdBc if pin contact has been detected or the time defined on these fields has been expired . When the DCD_SEL is not set, he BC Module read the MultValIdBc if the time defined on these fields has been expired . 00: 300ms 01: 100ms 10: 500ms 11: 900ms	RW	0
4	**Vlgc_Com_Sel** **Vlgc Compare Select** Software writes 1 to this bit to choose the Vlgc compare during Primary Detect when the ID pin is float. When this bit is set, the BC Module is optionally allowed to compare D- with Vlgc beside the Vdp_src comparing. The BC Module determine that it is attached to a DCP or CDP if D- is greater than Vdat_ref, but less than Vlgc. Otherwise, the BC Module determine that it is attached to a SDP, which may actually be a SDP, or a PS2 port, or a proprietary charge.	RW	0
3	**DBP_Timeout_CTL** **DBP Hardware Timeout Control** If this bit is set, the BC Module would clear the DB_Perform bit on the BC_USB_Sta_R register after Tsvld_con_wkb when the DB_Perform bit is set. Note: Tsvld_con_wkb = 45min	RW	0
2	**BC_status** **BC Detection status** Detection finish or not 1:Detecting,when starting BC Detect, set this bit 0:Detect finish	RW	0
1	**Reserved**	RW	0
0	**RS** **Run/Stop** Software writes 1 to this bit to start the BC Module operation. A transition from a zero to a one would cause the reset on the BC Module logic. If this bit = 1,when VBUS low go high, BC detection start automatically	RW	0

REG 2DH: BC Module VBUS Control and Status Register

Default：30H
Reset: Power On reset

Bit	Description	R/W	Default
7	Reserved	R	0
6	Indicate the first power on status Software write 1 to this bit to indicate not first time power on If Battery not present, and this bit is 0,the VBUS current limit set to 3A,for the F/W update in factory	RW	0
5	DP/DM floating Detection enable 0:disable 1:enable	RW	1
4	DP/DM pull down enable 0:disable 1:enable	RW	1
3	RID detect enable 0:disable 1:enable 1,VBUS presence and REG_2C[0]=1,RID was enabled automatically,do not depend on this bit; 2,VBUS presence or in power on state,set this bit to 1 will enable RID detect	RW	0
2-0	Reserved	RW	0

REG 2EH: BC USB Status Register

Default：40H
Reset: Reset by the VBUS negative edge

Bit	Description	R/W	Default
7	DB_Perform Dead Battery Perform Both BC Module and software write 1 to this bit to perform unconfig DBP clause and clean it to 0 to stop the unconfig DBP clause.	RW	0
6	Dead battery detect enable bit (Reset: power on reset) 0:disable 1:enable	RW	1
5	Reserved		
4	USB_Mode USB Speed Mode Flag This bit is used in good battery state. It is set by the USB driver to indicate the USB speed mode for the power manage. 0: High-Speed, Full-Speed or Low-Speed Mode 1: Super-Speed Mode	RW	0
	Dev_Bus_State Device Bus State Flag These fields are used in good battery state. They are set by the USB driver to		

3-0	indicate the USB bus state for the power manage. 000b: attached, physical signal pin contact 001b: connected, attached and when the downstream terminal is valid 010b: suspended 011b: configured 100b-111b: reserved	RW	0

REG 2FH: BC Detect Status Register

Default：00H
Reset: Reset by the VBUS negedge

<table>
<tr><th>Bit</th><th>Description</th><th>R/W</th><th>Default</th></tr>
<tr><td>7-5</td><td>BC_Result
BC Detect Result
These fields indicate the result of BC Detect performance. These fields should be used by the BC Module when the BC_Per bit of the BC_GLOBAL_R register transaction from 1 to 0.
<table>
<tr><th>Value</th><th>Meaning</th><th>Descriptor</th></tr>
<tr><td>000b</td><td>Reserved</td><td>/</td></tr>
<tr><td>001b</td><td>SDP</td><td>The insert port is Standard Downstream Port</td></tr>
<tr><td>010b</td><td>CDP</td><td>The insert port is Charging Downstream Port</td></tr>
<tr><td>011b</td><td>DCP</td><td>The insert port is Dedicated Charging Port</td></tr>
<tr><td>100b</td><td>Reserved</td><td>/</td></tr>
<tr><td>101b</td><td>Reserved</td><td>/</td></tr>
<tr><td>110b</td><td>Reserved</td><td>/</td></tr>
<tr><td>111b</td><td>Reserved</td><td>/</td></tr>
</table></td><td>R</td><td>001</td></tr>
<tr><td>4-0</td><td>Reserved</td><td>R</td><td>00000</td></tr>
</table>

REG 30H: VBUS path control & Hold voltage setting

Default：01H
Reset: Bit [7] & bit [2] reset signal is System reset, and Bit [6:3] & bit [1:0] reset signal is Power on reset

Bit	Description	R/W	Default
7	VBUS path select control (VBUS_SEL) when VBUS valid 0: VBUS path select ed 1: VBUS path Not selected	RW	0

6	Reserved			
5	V_{HOLD} setting bit 2	000: 4.0V; 001: 4.1V; 010: 4.2V 011: 4.3V; 100: 4.4V; 101: 4.5V 110: 4.6V; 111: 4.7V	RW	0
4	V_{HOLD} setting bit 1		RW	0
3	V_{HOLD} setting bit 0		RW	0
2	Reserved		RW	0
1-0	Current limit default when BC1.2 detection result is non SDP ： 00： 900mA 01： 1500mA 10： 2000mA 11： 2500mA		RW	01

REG 31H: Power wakeup control & V_{OFF} setting

Default：03H

Reset: Bit 3 reset signal is system reset, Bit [7-4] and Bit [2-0] reset signal is Power on reset

Bit	Description		R/W	Default
7	PWROK drive low or not when Power wake up and REG 31_[3]=1 0: not drive low 1: drive low in wake up period		RW	0
6	Reserved		RW	0
5	Soft Power wakeup, Write 1 to this bit, the output power will be waked up, then this bit will clear itself		RW	0
4	Control bit for IRQ output and wakeup trigger when REG 31_[3] is 1 0: IRQ pin is masked and IRQ can wakeup AW1660 when REG 31_[3] is 1 1: IRQ pin is normal and IRQ can't wakeup AW1660 when REG 31_[3] is 1		RW	0
3	Enable bit for the function that output power be waked up by IRQ source, or IRQ pin, or REG 31_[5], etc. write 1 to this bit will clear itself 0: function is disable 1: function is enable		RW	0
2	V_{OFF} setting bit 2	000-2.6V; 001-2.7V; 010-2.8V; 011-2.9V; 100-3.0V; 101-3.1V; 110-3.2V; 111-3.3V	RW	0
1	V_{OFF} setting bit 1		RW	1
0	V_{OFF} setting bit 0		RW	1

REG 32H: Power Disable, BAT detect and CHGLED pin control

Default：43H

Reset: Bit 7 reset signal is system reset, and Bit [6:0] reset signal is Power on reset

Bit	Description		R/W	Default
7	Writing '1' closes AXP813 and the bit clears to '0' automatically. RTCLDO and Charger are not influenced by the bit.		RW	0
6	Battery detection function control: 0-disable; 1-enable		RW	1
5-4	CHGLED pin control	00: Hi-Z	RW	00

		01: 25% 0.5Hz toggle 10: 25% 2Hz toggle 11: drive low		
3	CHGLED pin control	0: controlled by REG 32H[5:4] 1: controlled by Charger	RW	0
2	Reserved		RW	0
1-0	Control bit for Delay time between PWROK signal and power good time 00: 8ms; 01: 16ms; 10: 32ms; 11: 64ms		RW	11

REG 33H: Charger Control 1

Default：C5H
Reset: Bit [7] reset is system reset, Bit [6:0] reset is power on reset

Bit	Description	R/W	Default
7	Charger enable control 0-disable, 1-enable	RW	1
6-5	Charger target voltage setting 00: 4.10V; 01: 4.15V; 10: 4.2V; 11: 4.35V	RW	10
4	Charger end condition setting: 0-when I_{CHARGE}<10% I_{CHG}， Charge is done; 1-when I_{CHARGE}<20% I_{CHG}， Charge is done;	RW	0
3-0	Charge Current setting 200mA-2.8A, 200mA/step, default is 1200mA, 14steps, 1110-1111 reserved.	RW	0101

REG 34H: Charger Control 2

Default：45H
Reset: Power on reset

Bit	Description		R/W	Default
7	Pre-charge Timer length setting 1	00: 40 minutes; 01: 50 minutes; 10: 60 minutes; 11: 70 minutes.	RW	0
6	Pre-charge Timer length setting 0		RW	1
5	Charger output turn off or not when charging is end & the AXP813 is on state 0: turn off; 1: do not turn off		RW	0
4	CHGLED Type select when REG 32_[3] is 1 0: Type A; 1: Type B		RW	0
3	reserved		RW	0
2	reserved		RW	1
1	Fast charge maximum time setting 1	00: 6 hours; 01: 8 hours; 10: 10 hours; 11: 12 hours.	RW	0
0	Fast charge maximum time setting 0		RW	1

REG 35H: Charger Control 3

Default：18H
Reset: [7:4] is VBUS negedge reset , others Power on reset

Bit	Description	R/W	Default
7-4	VBUS current limit select when VBUS Current limited mode is enable 0000-100mA 0001-500mA 0010-900mA 0011-1500mA 0100-2000mA 0101-2500mA 0110-3000mA 0111-3500mA 1xxx-4000mA	RW	0001
3	Charger temperature loop enable 0: disable 1:enable	RW	1
2-0	Reserved		

REG 36H: POK setting

Default：59H
Reset: Bit 3 is reset by system reset, the others is reset by Power on reset

Bit	Description		R/W	Default
7	ONLEVEL setting 1	00: 128ms; 01: 1s; 10: 2s; 11: 3s.	RW	0
6	ONLEVEL setting 0		RW	1
5	IRQLEVEL setting 1	00: 1s; 01: 1.5s; 10: 2s; 11: 2.5s.	RW	0
4	IRQLEVEL setting 0		RW	1
3	Enable bit of the function which will shut down the AXP813 when POK is larger than OFFLEVEL 0-disable; 1-enable		RW	1
2	The AXP813 auto turn on or not when it shut down after off level POK 0: not turn on; 1: auto turn on		RW	0
1	OFFLEVEL setting 1	00: 4s; 01: 6s; 10: 8s; 11: 10s.	RW	0
0	OFFLEVEL setting 0		RW	1

REG 37H: POK Power off activity time setting

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7-3	Reserved		
2-0	Power off activity time setting 0/10/20/30/40/50/60/70 S	R/W	000

REG 38H: $V_{LTF\text{-}charge}$ setting

Default：A5H
Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LTF\text{-}charge}$ setting, M	M*10H，M=A5H:2.112V;range is 0V-3.264V	RW	A5H

REG 39H: $V_{HTF\text{-}charge}$ setting

Default：1FH
Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LHF\text{-}charge}$ setting, N	N*10H，N=1FH:0.397V;range is 0V-3.264V	RW	1FH

REG 3AH: ACIN path control

Default：80H
Reset: Power on reset, bit7 is system reset

Bit	Description	R/W	Default
7	ACIN path select control (VBUS_SEL) when VBUS valid 0: ACIN path Not selected 1: ACIN path selected	RW	1
6	Reserved		
5-3	000:4.0V 001:4.1V 010:4.2V 011 4.3V 100:4.4V 101:4.5V 110:4.6V 111:4.7V	RW	000
2-0	000:1500mA 001:2000mA 010:2500mA 011:3000mA 100:3500mA 101:4000mA 110:4000mA 111:4000mA	RW	000

REG 3BH: Buck frequency setting

Default：08H
Reset: Power on reset

Bit	Description	R/W	Default
7	Buck and PWM charger frequency spread enable 0: disable; 1: enable	RW	0

6	Buck and PWM charger frequency spread range control 0: 50KHz; 1: 100KHz		RW	0
5	Reserved			
4	DCDC4/5 mode select 0:Always PWM 1:PSM/PWM Auto switch		RW	0
3-0	Buck frequency setting bit 3-0	f_{OSC}: 3MHz *(1+ (8-N) *0.04) N=08: 3MHz Every step f_{OSC} error is ±5%	RW	1000

REG 3CH: $V_{LTF-work}$ setting

Default：FCH
Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{LTF-work}$ setting, M	M*10H，M=FCH:3.226V;range is 0V-3.264V	RW	FCH

REG 3DH: $V_{HTF-work}$ setting

Default：16H
Reset: Power on reset

Bit	Description		R/W	Default
7-0	$V_{HTF-work}$ setting, N	N*10H，N=16H:0.282V;range is 0V-3.264V	RW	16H

REG 40H: IRQ enable 1

Default：D8H
Reset: Power on reset

Bit	Description	R/W	Default
7	Same as bit4	RW	1
6	Same as bit3	RW	1
5	Same as bit2	RW	0
4	VBUS over voltage IRQ enable	RW	1
3	VBUS from low go high IRQ enable	RW	1
2	VBUS from high go low IRQ enable	RW	0
1-0	Reserved		

REG 41H: IRQ enable 2

Default：FFH
Reset: Power on reset

Bit	Description	R/W	Default
7	Battery append IRQ enable	RW	1
6	Battery absent IRQ enable	RW	1
5	Battery maybe bad IRQ enable	RW	1
4	Quit battery safe mode IRQ enable	RW	1
3	Charger is charging IRQ enable	RW	1
2	Battery charge done IRQ enable	RW	1
1-0	Reserved		

REG 42H: IRQ enable 3

Default：FFH
Reset: Power on reset

Bit	Description	R/W	Default
7	Battery over temperature in charge mode IRQ (CBTOIRQ) enable	RW	1
6	Quit Battery over temperature in charge mode IRQ (QCBTOIRQ) enable	RW	1
5	Battery under temperature in charge mode IRQ (CBTUIRQ) enable	RW	1
4	Quit Battery under temperature in charge mode IRQ (QCBTUIRQ) enable	RW	1
3	Battery over temperature in work mode IRQ (WBTOIRQ) enable	RW	1
2	Quit Battery over temperature in work mode IRQ (QWBTOIRQ) enable	RW	1
1	Battery under temperature in work mode IRQ (WBTUIRQ) enable	RW	1
0	Quit Battery under temperature in work mode IRQ (QWBTUIRQ) enable	RW	1

REG 43H: IRQ enable 4

Default：03H
Reset: Power on reset

Bit	Description	R/W	Default
7	The AXP813 temperature over the warning level 2 IRQ (OTIRQ) enable	RW	0
6-3	Reserved		
2	GPADC(GPIO0) ADC convert finished IRQ enable	RW	0
1	Enable bit for IRQ which indicate battery capacity ratio being lower than warning level 1, (WL1IRQ); normally, for low power warning requisition	RW	1
0	Enable bit for IRQ which indicate battery capacity ratio being lower than warning level 2, (WL2IRQ); normally, for power off requisition	RW	1

REG 44H: IRQ enable 5

Default：7CH
Reset: System reset

Bit	Description	R/W	Default
7	Event timer timeout IRQ enable	RW	0
6	POK positive edge IRQ (POKPIRQ) enable	RW	1
5	POK negative edge IRQ (POKNIRQ) enable	RW	1
4	POK short time active IRQ (POKSIRQ) enable	RW	1
3	POK long time active IRQ (POKLIRQ) enable	RW	1
2	POK off time active IRQ (POKOIRQ) enable	RW	1
1	GPIO1 input edge IRQ enable	RW	0
0	GPIO0 input edge IRQ enable	RW	0

REG 45H: IRQ enable 6

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-2	Reserved		
1	BC_USB_ChngInEn BC USB Status Change Interrupt Enable BC_USB_ChngEvnt Interrupt Enable. BC Detection result changed or not	RW	0
0	MV_ChngIntEn Rid MV_ChngEvnt Interrupt Enable.	RW	0

REG 48H: IRQ Status 1

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7	Same as bit4, write 1 to it or VBUS drop to normal will clear it	RW	0
6	Same as bit3, write 1 to it or VBUS from high go low will clear it	RW	0
5	Same as bit2, write 1 to it or VBUS from low go high will clear it	RW	0
4	VBUS over voltage IRQ, write 1 to it or VBUS drop to normal will clear it	RW	0
3	VBUS from low go high IRQ, write 1 to it or VBUS from high go low will clear it	RW	0

2	VBUS from high go low IRQ, write 1 to it or VBUS from low go high will clear it	RW	0
1-0	Reserved	RW	0

REG 49H: IRQ Status 2

Default：00H
Reset: power on reset

Bit	Description	R/W	Default
7	Battery append IRQ, write 1 to it or Battery remove will clear it	RW	0
6	Battery absent IRQ, write 1 to it or Battery append will clear it	RW	0
5	Battery maybe bad IRQ, write 1 to it or AXP813 quit battery safe mode will clear it	RW	0
4	Quit battery safe mode IRQ, write 1 to it or The AXP813 enter battery- safe mode will clear it	RW	0
3	Charger is charging IRQ, write 1 to it or charging is stop will clear it	RW	0
2	Battery charge done IRQ, write 1 to it or charger restart charging will clear it	RW	0
1-0	Reserved		

REG 4AH: IRQ Status 3

Default：00H
Reset: power on reset

Bit	Description	R/W	Default
7	CBTOIRQ, write 1 to it or Battery temperature drop to normal will clear it	RW	0
6	QCBTOIRQ, write 1 to it or Battery over temperature will clear it	RW	0
5	CBTUIRQ, write 1 to it or Battery temperature rise to normal will clear it	RW	0
4	QCBTUIRQ, write 1 to it or Battery under temperature will clear it	RW	0
3	WBTOIRQ, write 1 to it or Battery drop to temperature will clear it	RW	0
2	QWBTOIRQ, write 1 to it or Battery over temperature will clear it	RW	0
1	WBTUIRQ, write 1 to it or Battery rise to temperature will clear it	RW	0
0	QWBTUIRQ, write 1 to it or Battery under temperature will clear it	RW	0

REG 4BH: IRQ Status 4

Default：00H
Reset: Bit [7] reset is power on reset, Bit [6:0] reset is system reset

Bit	Description	R/W	Default
7	OTIRQ, write 1 to it or IC temperature drop to normal will clear it	RW	0

6-3	Reserved	RW	0
2	GPADC(GPIO0) ADC convert finished IRQ, write 1 will clear it	RW	0
1	IRQ which indicate battery capacity ratio being lower than warning level 1, (WL1IRQ); write 1 to it or system power rise up to warning level 1 will clear it	RW	0
0	IRQ which indicate battery capacity ratio being lower than warning level 2, (WL2IRQ); write 1 to it or system power rise up to warning level 2 will clear it	RW	0

REG 4CH: IRQ Status 5

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7	Event timer timeout IRQ, write 1 will clear it	RW	0
6	POKPIRQ, write 1 to it will clear it	RW	0
5	POKNIRQ, write 1 to it will clear it	RW	0
4	POKSIRQ, write 1 to it will clear it	RW	0
3	POKLIRQ, write 1 to it will clear it	RW	0
2	POKOIRQ, write 1 to it will clear it	RW	0
1	GPIO1 input edge IRQ, write 1 will clear it	RW	0
0	GPIO0 input edge IRQ, write 1 will clear it	RW	0

REG 4DH: IRQ Status 6

Default：00H
Reset: Reset by VBUS negedge

Bit	Description	R/W	Default
7-2	Reserved		
1	BC_USB_ChngEvnt BC USB Status Change Event This bit indicates that there is a change in the BC_USB_Sta_R register. When this bit is 1, and the interrupt on the BC_Charge_ChngInEn is 1, the BC Module will issue an interrupt to the controller. This bit and associated interrupt is clean by writing '1'.	R	0
0	MV_ChngEvnt MultValIdBc Multi-Valued input changed Event This bit indicates that there is a change in the value of MultValIdBc field. When this bit is 1, and the interrupt on the MV_ChngIntEn is 1, the BC Module will issue an interrupt to the controller. This bit and associated interrupt is clean by writing ‘1’.	R	0

REG 58H: TS pin input ADC data, highest 8bit

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-0	TS pin input ADC data highest 8bits， Default is Battery temperature	R	00

REG 59H: TS pin input ADC data, lowest 4bit

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	TS pin input ADC data lowest 4bits， Default is Battery temperature	R	00

REG 5AH: GPADC pin input ADC data, highest 8bit

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-0	GPADC pin input ADC data, highest 8bit	R	00

REG 5BH: GPADC pin input ADC data, lowest 4bit

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	GPADC pin input ADC data, lowest 4bit	R	00

REG 78H: Average data bit[11:4] for Battery voltage (BATSENSE)

Default：00H
Reset: System reset

Bit	Description	R/W	Default

7-0	Average data bit[11:4] for Battery voltage (BATSENSE)	R	00

REG 79H: Average data bit[3:0] for Battery voltage (BATSENSE)

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery voltage (BATSENSE)	R	00

REG 7AH: Average data bit[11:4] for Battery charge current

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery charge current	R	00

REG 7BH: Average data bit[3:0] for Battery charge current

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery charge current	R	00

REG 7CH: Average data bit[11:4] for Battery discharge current

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-0	Average data bit[11:4] for Battery discharge current	R	00

REG 7DH: Average data bit[3:0] for Battery discharge current

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-4	Reserved	R	00
3-0	Average data bit[3:0] for Battery discharge current	R	00

REG 80H: Buck PWM/PFM mode select

Default：80H
Reset: system reset

Bit	Description	R/W	Default
7	BUCK output over voltage turn off AXP813 function enable: 0-disable; 1-enable Suggest set this bit to 0 when performing Vrun going down to Vsleep	R/W	1
	DCDC2/DCDC3/ DCDC4: 0.5~1.13V, 33.3%; 1.14~1.3V, 25%		
	DCDC7/DCDC6: 0.6~1.36V, 33.3%; 1.37~1.52V, 25%		
	DCDC5: 0.8~1.11V, 33.3%; 1.12~1.43V, 29%; 1.44~1.84V, 21.2%		
	DCDC1: 1.6~2.3V, 21%; 2.4~3.1V, 17.6%; 3.2~3.4V, 11%		
6	DCDC7 PFM/PWM control: 0: auto switch 1: always PWM	RW	0
5	DCDC6 PFM/PWM control: 0: auto switch 1: always PWM	RW	0
4	DCDC5 PFM/PWM control: 0: auto switch 1: always PWM	RW	0
3	DCDC4 PFM/PWM control: 0: auto switch 1: PSM/PWM When this bit is set as ‘1’, refer to REG3B bit [4] for BUCK mode select	RW	0
1	DCDC3 PFM/PWM control: 0: auto switch 1: PSM/PWM When this bit is set as ‘1’, refer to REG3B bit [4] for BUCK mode select	RW	0
1	DCDC2 PFM/PWM control: 0: auto switch 1: PSM/PWM When this bit is set as ‘1’, refer to REG3B bit [4] for BUCK mode select	RW	0
0	DCDC1 PFM/PWM control: 0: auto switch 1: always PWM	RW	0

REG 81H: Off-Discharge and Output monitor control

Default：80H
Reset: Power on reset

Bit	Description	R/W	Default
7	Internal off-Discharge enable for Buck & LDO 0-disable; 1-enable	RW	1
6	DCDC7 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0
5	DCDC6 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0

4	DCDC5 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0
3	DCDC4 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0
1	DCDC3 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0
1	DCDC2 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0
0	DCDC1 85% Low voltage turn off AXP813 function enable: 0-disable; 1-enable;	RW	0

REG 82H: ADC Enable

Default：E1H
Reset: Power on reset

Bit	Description		R/W	Default
7	BAT voltage ADC enable	0: off, 1: on	RW	1
6	BAT current ADC enable	0: off, 1: on	RW	1
5	Die temperature ADC enable	0: off, 1: on	RW	1
4	GPIO0 ADC enable	0: off, 1: on	RW	0
3-1	Reserved			
0	TS pin input to ADC enable	0: off, 1: on	RW	1

REG 84H: ADC speed setting, TS pin Control

Default：F2H
Reset: power on reset

Bit	Description	R/W	Default
7-6	Current source from GPIO0 pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA	RW	11
5-4	Current source from TS pin control: 00: 20uA; 01: 40uA; 10: 60uA; 11: 80uA	RW	11
3	reserved	RW	0
2	TS pin function select: 0-TS pin is the battery temperature sensor input and will affect the charger 1-TS pin is an External input for ADC and do not affect the charger	RW	0

1-0	Current source from TS pin on/off enable bit [1:0]	00: off 01: on when charging battery, off when not charging 10: on in ADC phase and off when out of the ADC phase, for power saving 11: always on	RW	10

REG 85H: ADC speed setting

Default：B0H
Reset: power on reset

Bit	Description		R/W	Default
7	TS/GPIO0 ADC speed setting bit 1	100×2^n So Fs=25, 50, 100, 200Hz	RW	1
6	TS/GPIO0 ADC speed setting bit 0		RW	0
5	Vol/Cur ADC speed setting bit 1	100×2^n So Fs=100, 200, 400, 800Hz	RW	1
4	Vol/Cur ADC speed setting bit 0		RW	1
3	Reserved			
2	GPIO0 ADC work mode 1:output current 0:not output current		RW	0
1-0	Reserved		RW	00

REG 8AH: Timer control

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7	Timer time out status It indicate that timer time out when this bit from low go high Write this bit to 1, will clear the status and the timer	RW	0
6-0	Set threshold of the timer Write these 7 bits to all 0, will disable the timer	RW	0000000

REG 8EH: Buck output voltage monitor de-bounce time setting

Default：40H
Reset: Power on reset

Bit	Description	R/W	Default
7-6	Buck output voltage monitor de-bounce time setting, 00-62us; 01-124us; 10-186us; 11-248us	RW	01
5-0	Reserved	RW	00

REG 8FH: IRQ pin, hot-over shut down

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-4	Reserved		
3	The function control that 16s' POK trigger power on reset: 0-disable; 1-enable	RW	0
2	The AXP813 shut down or not when Die temperature is over the warning level 3 0-not shut down; 1-shut down	RW	0
1	Voltage recovery enable bit when AXP813 wakeup from REG31H[3]=1 0: recovery to the vboot 1: not recovery to the vboot	RW	0
0	Reserved	RW	0

REG 90H: GPIO0 (GPADC) control

Default：07H
Reset: system reset

Bit	Description		R/W	Default
7	Enable GPIO0 Positive edge trigger IRQ or wake up when GPIO0 is digital input 0: disable; 1: enable		RW	0
6	Enable GPIO0 Negative edge trigger IRQ or wake up when GPIO0 is digital input 0: disable; 1: enable		RW	0
5-3	Reserved		RW	0
2	GPIO0 pin function control bit 2	000: drive low 001: drive high 010: digital input, trigger point is about 1.2V 011: low noise LDO on 100: low noise LDO off 101-111: Floating, if ADC enable，then	RW	1
1	GPIO0 pin function control bit 1		RW	1
0	GPIO0 pin function control bit		RW	1

	0	work as ADC input mode		

REG 91H: GPIO0LDO and GPIO0 high level voltage setting

Default：1AH
Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved		
4-0	GPIO0LDO and GPIO0 High level voltage setting bit 4-0 From 0.7 to 3.3V, 100mV/step, 11011-11111 reserved	RW	11010

REG 92H: GPIO1 control

Default：07H
Reset: system reset

Bit	Description		R/W	Default
7	Enable GPIO1 Positive edge trigger IRQ or wake up when GPIO1 is digital input 0: disable; 1: enable		RW	0
6	Enable GPIO1 Negative edge trigger IRQ or wake up when GPIO1 is digital input 0: disable; 1: enable		RW	0
5-3	Reserved			
2	GPIO1 pin function control bit 2	000: drive low 001: drive high 010: digital input, trigger point is about 1.2V 011: low noise LDO on 100: low noise LDO off 101-111: Floating	RW	1
1	GPIO1 pin function control bit 1		RW	1
0	GPIO1 pin function control bit 0		RW	1

REG 93H: GPIO1LDO and GPIO1 high level voltage setting

Default：1AH
Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	GPIO1LDO and GPIO1 High level voltage setting bit 4-0 From 0.7 to 3.3V, 100mV/step, 11011-11111 reserved	RW	11010

REG 94H: GPIO signal bit

Default：00H
Reset: system reset

Bit	Description	R/W	Default
7-2	Reserved		
1	This bit reflect the logic level of the GPIO1 pin when configured as digital input	R	0
0	This bit reflect the logic level of the GPIO0 pin when configured as digital input	R	0

REG 97H: GPIO pull down control

Default：00H
Reset: system reset

Bit	Description	R/W	Default
7-2	Reserved		
1	GPIO1 Pull down control in digital input mode 0: off 1: on	RW	0
0	GPIO0 Pull down control in digital input mode 0: off 1: on	RW	0

REG A0H: Real time data bit[11:4] for Battery voltage (BATSENSE)

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-0	Real time data bit[11:4] for Battery voltage (BATSENSE)	R	00

REG A1H: Real time data bit[3:0] for Battery voltage (BATSENSE)

Default：00H
Reset: System reset

Bit	Description	R/W	Default
7-4	Real time data bit[3:0] for Battery voltage (BATSENSE)	R	00
3-0	Reserved	R	00

REG B8H: Fuel Gauge Control

Default：E8H
Reset: power on reset

Bit	Description	R/W	Default
7	fuel gauge enable control(including OCV and coulomb meter) 0-Disable 1-Enable	RW	1
6	Coulomb meter enable control 0-Disable 1-Enable	RW	1
5	Battery maximum capacity calibration enable control 0-Disable 1-Enable	RW	1
4	Battery maximum capacity calibration status 0: Not calibrating 1: Is calibrating	R	0
3	OCV-SOC curve calibration enable control 0-Disable 1-Enable Suggest set this bit as 0	RW	1
2	OCV-SOC curve calibration status 0-Not calibrating 1-Is calibrating	R	0
1-0	Reserved	RW	0

REG B9H: Battery capacity percentage for indication

Default：64H
Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if battery capacity percentage for indication is valid: 0-Not valid 1-Is valid	R	0
6-0	Battery capacity percentage for indication	R	64H

REG BAH: RDC 1

Default：80H
Reset: Bit [7] & [4-0] reset is power on reset

Bit	Description	R/W	Default
7	RDC calculation control; 0: disable; 1: enable	RW	1
6	RDC was right detected or not flag： 1-Y 0-N	R	0
5	RDC has detected or not during this power on time： 1-Y 0-N	R	0
4-0	RDC value HSB 5 bit	RW	00000

REG BBH: RDC 0

Default：5DH
Reset: power on reset

Bit	Description	R/W	Default
7-0	RDC value LSB 8bit	RW	5DH

REG BCH: OCV 1

Default：00H
Reset: power on reset

Bit	Description	R/W	Default
7-0	OCV HSB 8bit	R	00H

REG BDH: OCV0

Default：00H
Reset: power on reset

Bit	Description	R/W	Default
7-4	Reserved		
3-0	OCV LSB 4bit	R	0000

REG E0H: Battery maximum capacity

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if battery maximum capacity is valid: 0-Not valid 1-Is valid	R/W	0
6-0	battery maximum capacity bit[14:8]	RW	00H

REG E1H: Battery maximum capacity

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7-0	battery maximum capacity bit[7:0](Unit: 1.456mAh)	RW	00H

REG E2H: Coulomb meter counter1

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if coulomb meter counter is valid: 0-Not valid 1-Is valid	RW	0
6-0	Coulomb meter counter[14:8]	RW	00H

REG E3H: Coulomb meter counter2

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7-0	Coulomb meter counter[7:0] (Unit: 1.456mAh)	RW	00H

REG E4H: OCV Percentage of battery capacity

Default：64H
Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if OCV percentage of battery capacity is valid 0-Not valid 1-Is valid	R	0
6-0	OCV percentage of battery capacity	R	64H

REG E5H: Coulomb meter percentage of battery capacity

Default：64H
Reset: Power on reset

Bit	Description	R/W	Default
7	Indicating if coulomb meter percentage of battery capacity is valid: 0-Not valid 1-Is valid	R	0
6-0	Coulomb meter percentage of battery capacity	R	64H

REG E6H: Battery capacity percentage warning level

Default：A0H
Reset: Power on reset

Bit	Description	R/W	Default
7-4	Warning level 1: Warning threshold, 5-20%, 1% per step	RW	1010
3-0	Warning level 2: Shutting down threshold, 0-15%, 1% per step	RW	0000

REG E8H: Fuel gauge tuning control 0

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7-3	Reserved		
2-0	Battery capacity percentage for indication update minimum interval 000-30s 001-60s 010-120s 011-164s 100-immediately update when changed 101-5s 110-10s 111-20s	RW	0

REG E9H: Fuel gauge tuning control 1

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7-6	OCV Percentage calibrate the Coulomb meter percentage, maximum time interval 00-60s 01-120s 10-15s 11-30s	RW	0
5-3	Wait for the stability for charge when in RDC calculation 000-180s 001-240s 010-300s 011-600s 100-30s 101-60s 110-90s 111-120s	RW	0
2-0	Wait for the stability for discharge when in RDC calculation 000-180s 001-240s 010-300s 011-600s 100-30s 101-60s 110-90s 111-120s	RW	0

REG EAH: Fuel gauge tuning control 2

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7-6	OCV Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00-4 01-8 10-1	RW	0

	11-2		
5-4	Coulomb meter Percentage Debounce setting(only when the change continuous the same direction as more than N times, then the ocv percentage increase or decrease)N: 00-4 01-8 10-1 11-2	RW	0
3	Battery maximum capacity calibration start condition: 0-OCV percentage ＜ (REG E6H[3:0] + 3) 1-OCV percentage ＜ (REG E6H[3:0] + 6)	RW	0
2	Battery maximum capacity calibration end condition 0 0-OCV percentage ≥ 95% 1-OCV percentage ＝ 100%	RW	0
1	Battery maximum capacity calibration end condition 1 0-wait for charge finished 1-do not wait for charge finished	RW	0
0	Battery maximum capacity calibration end condition 2 (wait Nms for the charge finished indication signal after REG 01H[6] clear to 0,N: 0-68 1-120	RW	0

REG EBH: Fuel gauge tuning control 3

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7	When charge status bit REG 01H[6] = 1,the percentage of indication can be decrease or not 0-decrease enable 1-decrease disable	RW	0
6-4	When REG 01H[6] = 1，percentage of indication decrease hysteresis(N) setting 000-4% 001-5% 010-6% 011-7% 100-0% 101-1% 110-2% 111-3%	RW	0
3	Calculation RDC current condition setting 0-≥300mA	RW	0

	1-≥150mA		
2-0	Calibrate RDC percentage changed threshold setting 000-4% 001-5% 010-6% 011-7% 100-0% 101-1% 110-2% 111-3% calibration： △ OCVPCT > N	RW	0

REG ECH: Fuel gauge tuning control 4

Default： 00H
Reset: Power on reset

Bit	Description	R/W	Default
7	ADC current data include offset0 or not(For debug) 0-Enable 1-Disable	RW	0
6	ADC current data offset0 smooth control(For debug) 0-Enable 1-Disable	RW	0
5	RDC re-calculate when AXP813 power on for power off 0-Disable 1-Enable	RW	0
4-3	The minimum battery voltage for RDC calculation 00-3.5V 01-3.6V 10-3.7V 11-3.4V	RW	00
2-0	Coulomb counter calibration threshold， relative with REG_E6_[3:0] 000-REG_E6H[3:0]+7(default) 001-REG_E6H[3:0]+8 010-REG_E6H[3:0]+9 011-REG_E6H[3:0]+10 100-REG_E6H[3:0]+3 101-REG_E6H[3:0]+4 110-REG_E6H[3:0]+5 111-REG_E6H[3:0]+6	RW	000

REG EDH: Fuel gauge tuning control 5

Default：00H
Reset: Power on reset

Bit	Description	R/W	Default
7	OCV percentage relative with the charge/discharge rate control 0-Disable 1-Enable	RW	0
6	Update time when rate > 0.5C 0-30S 1-15S	RW	0
5-4	Update time when rate < 0.5C and rate > 0.1C 00-60S 01-75S 10-30S 11-45S	RW	00
3-2	Update time when rate < 0.1C 00-120S 01-180S 10-240S 11-60S	RW	00
1-0	Fixed update time 00-30S 01-45S 10-60S 11-15S	RW	00

15 Codec Register

Register List

Register Name	Offset	Description
CHIP_AUDIO_RST	00H	Chip Soft Reset
PLL_CTRL1	02H	PLL Configure Control 1
PLL_CTRL2	03H	PLL Configure Control 2
SYSCLK_CTRL	04H	System Clocking Control
MOD_RST_CTRL	05H	Module Clock Enable Control
ADDA_SR_CTRL	06H	ADDA Sample Rate Configuration
I2S1LCK_CTRL	10H	I2S1 BCLK/LRCK Control
I2S1_SDIN_CTRL	11H	I2S1 SDIN Control
I2S1_SDOUT_CTRL	12H	I2S1 SDOUT Control
I2S1_DIG_MIXER	13H	I2S1 Digital Mixer Control
I2S1_VOL_CTRL1	14H	I2S1 Volume Control 1
I2S1_VOL_CTRL2	15H	I2S1 Volume Control 2
I2S1_VOL_CTRL3	16H	I2S1 Volume Control 3
I2S1_VOL_CTRL4	17H	I2S1 Volume Control 4
I2S1_MXR_GAIN	18H	I2S1 Digital Mixer Gain Control
I2S2_CLK_CTRL	20H	I2S2 BCLK/LRCK Control
I2S2_SDIN_CTRL	21H	I2S2 SDIN Control
I2S2_SDOUT_CTRL	22H	I2S2 SDOUT Control
I2S2_DIG_MIXER	23H	I2S2 Digital Mixer Control
I2S2_VOL_CTRL1	24H	I2S2 Volume Control 1
I2S2_VOL_CTRL2	26H	I2S2 Volume Control 2
I2S2_MXR_GAIN	28H	I2S2 Digital Mixer Gain Control
I2S3_CLK_CTRL	30H	I2S3 BCLK/LRCK Control
I2S3_SDIN_CTRL	31H	I2S3 SDIN Control
I2S3_SDOUT_CTRL	32H	I2S3 SDOUT Control
I2S3_SGP_CTRL	33H	I2S3 Signal Path Control
ADC_DIG_CTRL	40H	ADC Digital Control
TBD	…	…
RTC_CTRL_REG	B0'h	RTC Control Register
RTC_RESET_REG	B1'h	RTC Reset Register
ALM_INT_ENA_REG	B2'h	Alarm Interrupt Enable Register
ALM_INT_STA_REG	B3'h	Alarm Interrupt Status Register
RTC_SEC_REG	B4'h	RTC Seconds Register
RTC_MIN_REG	B5'h	RTC Minutes Register
RTC_HOU_REG	B6'h	RTC Hours Register
RTC_WEE_REG	B7'h	RTC Weekdays Register

RTC_DAY_REG	B8'h	RTC Days Register
RTC_MON_REG	B9'h	RTC Months Register
RTC_YEA_REG	BA'h	RTC Years Register
ALM_SEC_REG	C3'h	Alarm Seconds Register
ALM_MIN_REG	C4'h	Alarm Minutes Register
ALM_HOU_REG	C5'h	Alarm Hours Register
ALM_WEE_REG	C6'h	Alarm Weekdays Register
ALM_DAY_REG	C7'h	Alarm Days Register
ALM_MON_REG	C8'h	Alarm Months Register
ALM_YEA_REG	C9'h	Alarm Years Register
RTC_GP_REGn	D0'h	RTC General Purpose Register n(n = 0,1,2……31)

REG 00H_Chip Soft Reset Register

Default: 0x0101			Register Name: CHIP_AUDIO_RST
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0101	Writing to this register resets all register to their default state. Reading from this register will indicate device type and version.

REG 01H_PLL Configure Control 1 Register

Default: 0x0141			Register Name: PLL_CTRL1
Bit	**Read/Write**	**Default**	**Description**
15:14	R/W	0x0	DPLL_DAC_BIAS 00： min 11： max
13:8	R/W	0x1	PLL_POSTDIV_M PLL Post-Divider Factor M Factor=0， M=64 Factor=1， M=1 ... Factor=63， M=63
7	R/W	0x0	Reserved
6	R/W	0x1	Close_loop. 1: work as a PLL. 0: work as a free running VCO at a pre-fixed frequency.
5:0	R/W	0x1	INT Integ[5:0], the loop bandwidth config. 0: works as free running mode. 1: small bandwidth, need more time to lock. .... 63: large bandwidth, need less time to lock, but may result in failing.

REG 02H_PLL Configure Control 2 Register

Default: 0x0000			Register Name: PLL_CTRL2
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	PLL_EN PLL Enable 0: Disable 1: Enable The PLL output FOUT= FIN*N/(M*(2K+1)), N=N_i+N_f;
14	R	0x0	PLL Locked status 0: Not locked or not enabled 1: Enabled and locked
13:4	R/W	0x0	PLL_PREDIV_NI PLL Integer Part of Pre-Divider Factor N. Factor=0， N_i=0 ; Factor=1， N_i=1 ; ... Factor=1023, N_i=1023 ;
3	/	/	/
2:0	R/W	0x0	PLL_POSTDIV_NF PLL Fractional Part of Pre-Divider Factor N. Factor=0， N_f=0*0.2 ; Factor=1， N_f=1*0.2 ; ... Factor=7, N_f=7*0.2 ;

REG 03H_System Clocking Control Register

Default: 0x0000			Register Name: SYSCLK_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	PLLCLK_ENA PLLCLK Enable 0: Disable 1: Enable
14	R/W	0x0	Reserved
13:12	R/W	0x0	PLLCLK_SRC PLL Clock Source Select 00: MCLK1 01: MCLK2 10: BCLK1 11: BCLK2
11	R/W	0x0	I2S1CLK_ENA

			I2S1CLK Enable 0: Disable 1: Enable
10	R/W	0x0	Reserved
9:8	R/W	0x0	I2S1CLK_SRC I2S1CLK Source Select 00: MLCK1 01: MLCK2 1X: PLL
7	R/W	0x0	I2S2CLK_ENA I2S2CLK Enable 0: Disable 1: Enable
6	R/W	0x0	Reserved
5:4	R/W	0x0	I2S2CLK_SRC I2S2CLK Source Select 00: MLCK1 01: MLCK2 1X: PLL
3	R/W	0x0	SYSCLK_ENA SYSCLK Enable 0: Disable 1: Enable
2:1	R/W	0x0	Reserved
0	R/W	0x0	SYSCLK_SRC System Clock Source Select 0: I2S1CLK 1: I2S2CLK

REG 04H_Module Clock Enable Control Register

Default: 0x0000			**Register Name: MOD_CLK_ENA**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	Module clock enable control 0-Clock disable 1-Clock enable BIT15-I2S1 BIT14-I2S2 BIT13-I2S3 BIT12-Reserved BIT11-SRC1 BIT10-SRC2 BIT9-Reserved BIT8-Reserved

			BIT7-HPF & AGC BIT6-HPF & DRC BIT5-Reserved BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

REG 05H_Module Reset Control Register

Default: 0x0000			Register Name: MOD_RST_CTRL
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	Module reset control 0-Reset asserted 1-Reset de-asserted BIT15-I2S1 BIT14-I2S2 BIT13-I2S3 BIT12-Reserved BIT11-SRC1 BIT10-SRC2 BIT9-Reserved BIT8-Reserved BIT7-HPF & AGC BIT6-HPF & DRC BIT5-Reserved BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

REG 06H_ADDA Sample Rate Configuration Register

Default: 0x0000			Register Name: I2S_SR_CTRL
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	ADDA_FS_I2S1 ADDA Sample Rate synchronised with I2S1 clock zone 0000: 8KHz 0001: 11.025KHz 0010: 12KHz 0011: 16KHz

			0100: 22.05KHz 0101: 24KHz 0110: 32KHz 0111: 44.1KHz 1000: 48KHz 1001: 96KHz 1010: 192KHz Other: Reserved
11:8	R/W	0x0	ADDA_FS_I2S2 ADDA Sample Rate synchronised with I2S2 clock zone 0000: 8KHz 0001: 11.025KHz 0010: 12KHz 0011: 16KHz 0100: 22.05KHz 0101: 24KHz 0110: 32KHz 0111: 44.1KHz 1000: 48KHz 1001: 96KHz 1010: 192KHz Other: Reserved
3	R/W	0x0	SRC1_ENA SRC1 Enable. SRC1 Performs sample rate conversion of digital audio input to the AC100. 0: Disable 1: Enable
2	R/W	0x0	SRC1_SRC From which the input data will come. 0: I2S1 DAC Timeslot 0 1: I2S2 DAC
1	R/W	0x0	SRC2_ENA SRC2 Enable. SRC2 Performs sample rate conversion of digital audio output from the AC100. 0: Disable 1: Enable
0	R/W	0x0	SRC2_SRC To which the converted data will be output. 0: I2S1 ADC Timeslot 0 1: I2S2 ADC

REG 10H_I2S1 BCLK/LRCK Control Register

Default: 0x0000	**Register Name: I2S1LCK_CTRL**

Bit	Read/Write	Default	Description
15	R/W	0x0	I2S1_MSTR_MOD I2S1 Audio Interface mode select 0 = Master mode 1 = Slave mode
14	R/W	0x0	I2S1_BCLK_INV I2S1 BCLK Polarity 0: Normal 1: Inverted
13	R/W	0x0	I2S1_LRCK_INV I2S1 LRCK Polarity 0: Normal 1: Inverted
12:9	R/W	0x0	I2S1_BCLK_DIV Select the I2S1CLK/BCLK1 ratio 0000: I2S1CLK/1 0001: I2S1CLK/2 0010: I2S1CLK/4 0011: I2S1CLK/6 0100: I2S1CLK/8 0101: I2S1CLK/12 0110: I2S1CLK/16 0111: I2S1CLK/24 1000: I2S1CLK/32 1001: I2S1CLK/48 1010: I2S1CLK/64 1011: I2S1CLK/96 1100: I2S1CLK/128 1101: I2S1CLK/192 1110: Reserved 1111: Reserved
8:6	R/W	0x0	I2S1_LRCK_DIV Select the BCLK1/LRCK ratio 000: 16 001: 32 010: 64 011: 128 100: 256 1xx: Reserved
5:4	R/W	0x0	I2S1_WORD_SIZ I2S1 digital interface word size 00: 8bit 01: 16bit 10: 20bit

			11: 24bit
3:2	R/W	0x0	I2S1_DATA_FMT I2S digital interface data format 00: I2S mode 01: Left mode 10: Right mode 11: DSP mode
1	R/W	0x0	DSP_MONO_PCM DSP Mono mode select 0: Stereo mode select 1: Mono mode select
0	R/W	0x0	I2S1_TDMM_ENA I2S1 TDM Mode enable 0: Disable 1: Enable

REG 11H_I2S1 SDOUT Control Register

Default: 0x0000			Register Name: I2S1_SDOUT_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S1_ADCL0_ENA I2S1 ADC Timeslot 0 left channel enable 0: Disable 1: Enable
14	R/W	0x0	I2S1_ADCR0_ENA I2S1 ADC Timeslot 0 right channel enable 0: Disable 1: Enable
13	R/W	0x0	I2S1_ADCL1_ENA I2S1 ADC Timeslot 1 left channel enable 0: Disable 1: Enable
12	R/W	0x0	I2S1_ADCR1_ENA I2S1 ADC Timeslot 1 right channel enable 0: Disable 1: Enable
11:10	R/W	0x0	I2S1_ADCL0_SRC I2S1 ADC Timeslot 0 left channel data source select 00: I2S1_ADCL0 01: I2S1_ADCR0 10: (I2S1_ADCL0+ I2S1_ADCR0) 11: (I2S1_ADCL0+ I2S1_ADCR0)/2
9:8	R/W	0x0	I2S1_ADCR0_SRC I2S1 ADC Timeslot 0 right channel data source select

			00: I2S1_ADCR0 01: I2S1_ADCL0 10: (I2S1_ADCL0+I2S1_ADCR0) 11: (I2S1_ADCL0+I2S1_ADCR0)/2
7:6	R/W	0x0	I2S1_ADCL1_SRC I2S1 ADC Timeslot 1 left channel data source select 00: I2S1_ADCL1 01: I2S1_ADCR1 10: (I2S1_ADCL1+I2S1_ADCR1) 11: (I2S1_ADCL1+I2S1_ADCR1)/2
5:4	R/W	0x0	I2S1_ADCR1_SRC I2S1 ADC Timeslot 1 right channel data source select 00: I2S1_ADCR1 01: I2S1_ADC1L 10: (I2S1_ADCL1+I2S1_ADCR1) 11: (I2S1_ADCL1+I2S1_ADCR1)/2
3	R/W	0x0	I2S1_ADCP_ENA I2S1 ADC Companding enable(8-bit mode only) 0: Disable 1: Enable
2	R/W	0x0	I2S1_ ADCP_SEL I2S1ADC Companding mode select 0: A-law 1: u-law
1:0	R/W	0x0	I2S1_SLOT_SIZ Select the slot size(only in TDM mode) 00: 8 01: 16 10: 32 11: Reserved

REG 12H_I2S1 SDIN Control Register

Default: 0x0000			Register Name: I2S1_SDIN_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S1_DACL0_ENA I2S1 DAC Timeslot 0 left channel enable 0: Disable 1: Enable
14	R/W	0x0	I2S1_DACR0_ENA I2S1 DAC Timeslot 0 right channel enable 0: Disable 1: Enable
13	R/W	0x0	I2S1_DACL1_ENA

			I2S1 DAC Timeslot 1 left channel enable 0: Disable 1: Enable
12	R/W	0x0	I2S1_DACR1_ENA I2S1 DAC Timeslot 1 right channel enable 0: Disable 1: Enable
11:10	R/W	0x0	I2S1_DACL0_SRC I2S1 DAC Timeslot 0 left channel data source select 00: I2S1_DACL0 01: I2S1_DACR0 10: (I2S1_DACL0+I2S1_DACR0) 11: (I2S1_DACL0+I2S1_DACR0)/2
9:8	R/W	0x0	I2S1_DACR0_SRC I2S1 DAC Timeslot 0 right channel data source select 00: I2S1_DACR0 01: I2S1_DACL0 10: (I2S1_DACL0+I2S1_DACR0) 11: (I2S1_DACL0+I2S1_DACR0)/2
7:6	R/W	0x0	I2S1_DACL1_SRC I2S1 DAC Timeslot 1 left channel data source select 00: I2S1_DACL1 01: I2S1_DACR1 10: (I2S1_DACL1+I2S1_DACR1) 11: (I2S1_DACL1+I2S1_DACR1)/2
5:4	R/W	0x0	I2S1_DACR1_SRC I2S1 DAC Timeslot 1 right channel data source select 00: I2S1 DACR1 01: I2S1 DACL1 10: (I2S1 DACL1+I2S1 DACR1) 11: (I2S1 DACL1+I2S1 DACR1)/2
3	R/W	0x0	I2S1_DACP_ENA I2S1 DAC Companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	I2S1_ DACP_SEL I2S1 DAC Companding mode select 0: A-law 1: u-law
1	R/W	0x0	Reserved
0	R/W	0x0	I2S1_LOOP_ENA I2S1 loopback enable 0: No loopback 1: Loopback(SDOUT1 data output to SDOUT1 data input)

REG 13H_I2S1 Digital Mixer Source Select Register

Default: 0x0000			Register Name: I2S1_MXR_SRC
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	I2S1_ADCL0_MXL_SRC I2S1 ADC Timeslot 0 left channel mixer source select 0: Disable 1: Enable Bit15: I2S1_DA0L data Bit14: I2S2_DACL data Bit13: ADCL data Bit12: I2S2_DACR data
11:8	R/W	0x0	I2S1_ADCR0_MXR_SRC I2S1 ADC Timeslot 0 right channel mixer source select 0: Disable 1: Enable Bit11: I2S1_DA0R data Bit10: I2S2_DACR data Bit9: ADCR data Bit8: I2S2_DACL data
7:6	R/W	0x0	I2S1_ADCL1_MXR_SRC I2S1 ADC Timeslot 1 left channel mixer source select 0: Disable 1: Enable Bit7: I2S2_DACL data Bit6: ADCL data
5:4	R/W	0x0	Reserved
3:2	R/W	0x0	I2S1_ADCR1_MXR_SRC I2S1 ADC Timeslot 1 right channel mixer source select 0: Disable 1: Enable Bit3: I2S2_DACR data Bit2: ADCR data
1:0	R/W	0x0	Reserved

REG 14H_I2S1 Volume Control 1 Register

Default: 0xA0A0			Register Name: I2S1_VOL_CTRL1
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	I2S1_ADCL0_VOL I2S1 ADC Timeslot 0 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB .... 0x9F = -0.75dB 0xA0 = 0dB

			0xA1 = 0.75dB ……………… 0xFF = 71.25dB
7:0	R/W	0xA0	I2S1_ADCR0_VOL I2S1 ADC Timeslot 0 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB

REG 15H_I2S1 Volume Control 2 Register

Default: 0xA0A0			Register Name: I2S1_VOL_CTRL2
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	I2S1_ADCL1_VOL I2S1 ADC Timeslot 1 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB
7:0	R/W	0xA0	I2S1_ADCR1_VOL I2S1 ADC Timeslot 1 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB

REG 16H_I2S1 Volume Control 3 Register

Default: 0xA0A0			Register Name: I2S1_VOL_CTRL3
Bit	Read/Write	Default	Description
15:8	R/W	0xA0	I2S1_DACL0_VOL I2S1 DAC Timeslot 0 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB
7:0	R/W	0xA0	I2S1_DACR0_VOL I2S1 DAC Timeslot 0 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB

REG 17H_I2S1 Volume Control 4 Register

Default: 0xA0A0			Register Name: I2S1_VOL_CTRL4
Bit	Read/Write	Default	Description
15:8	R/W	0xA0	I2S1_DACL1_VOL I2S1 DAC Timeslot 1 left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB
7:0	R/W	0xA0	I2S1_DACR1_VOL

			I2S1 DAC Timeslot 1 right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB

REG 18H_I2S1 Digital Mixer Gain Control Register

Default: 0x0000			**Register Name: I2S1_MXR_GAIN**
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	I2S1_ADCL0_MXR_GAIN I2S1 ADC Timeslot 0 left channel mixer gain control 0: 0dB 1: -6dB Bit15: I2S1_DA0L data Bit14: I2S2_DACL data Bit13: ADCL data Bit12: I2S2_DACR data
11:8	R/W	0x0	I2S1_ADCR0_MXR_GAIN I2S1 ADC Timeslot 0 right channel mixer gain control 0: 0dB 1: -6dB Bit11: I2S1_DA0R data Bit10: I2S2_DACR data Bit9: ADCR data Bit8: I2S2_DACL data
7:6	R/W	0x0	I2S1_ADCL1_MXR_GAIN I2S1 ADC Timeslot 1 left channel mixer gain control 0: 0dB 1: -6dB Bit7: I2S2_DACL data Bit6: ADCL data
5:4	R/W	0x0	Reserved
3:2	R/W	0x0	I2S1_ADCR1_MXR_GAIN I2S1 ADC Timeslot 1 right channel mixer gain control 0: 0dB 1: -6dB Bit3: I2S2_DACR data Bit2: ADCR data
1:0	R/W	0x0	Reserved

REG 20H_I2S2 BCLK/LRCK Control Register

Default: 0x0000			Register Name: I2S2_CLK_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S2_MSTR_MOD I2S2 Audio Interface mode select 0 = Master mode 1 = Slave mode
14	R/W	0x0	I2S2_BCLK_INV I2S2 BCLK Polarity 0: Normal 1: Inverted
13	R/W	0x0	I2S2_LRCK_INV I2S2 LRCK Polarity 0: Normal 1: Inverted
12:9	R/W	0x0	I2S2_BCLK_DIV Select the I2S2CLK/BCLK2 ratio 0000: I2S2CLK/1 0001: I2S2CLK/2 0010: I2S2CLK/4 0011: I2S2CLK/6 0100: I2S2CLK/8 0101: I2S2CLK/12 0110: I2S2CLK/16 0111: I2S2CLK/24 1000: I2S2CLK/32 1001: I2S2CLK/48 1010: I2S2CLK/64 1011: I2S2CLK/96 1100: I2S2CLK/128 1101: I2S2CLK/192 1110: Reserved 1111: Reserved
8:6	R/W	0x0	I2S2_LRCK_DIV Select the BCLK2/LRCK2 ratio 000: 16 001: 32 010: 64 011: 128 100: 256 1xx: Reserved
5:4	R/W	0x0	I2S2_WORD_SIZ I2S2 digital interface world length

			00: 8bit 01: 16bit 10: 20bit 11: 24bit
3:2	R/W	0x0	I2S2_DATA_FMT I2S digital interface data format 00: I2S mode 01: Left mode 10: Right mode 11: DSP mode
1	R/W	0x0	I2S2_MONO_PCM I2S2 Mono PCM mode select 0: Stereo mode select 1: Mono mode select
0	R/W	0x0	Reserved

REG 21H_I2S2 SDOUT Control Register

Default: 0x0000			**Register Name: I2S2_SDOUT_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S2_ADCL_EN I2S2 ADC left channel enable 0: Disable 1: Enable
14	R/W	0x0	I2S2_ADCR_EN I2S2 ADC right channel enable 0: Disable 1: Enable
13:12	R/W	0x0	Reserved
11:10	R/W	0x0	I2S2_ADCL_SRC I2S2 ADC left channel data source select 00: I2S2_ADCL 01: I2S2_ADCR 10: (I2S2_ADCL+I2S2_ADCR) 11: (I2S2_ADCL+I2S2_ADCR)/2
9:8	R/W	0x0	I2S2_ADCR_SRC I2S2 ADC right channel data source select 00: I2S2_ADCR 01: I2S2_ADCL 10: (I2S2_ADCL+I2S2_ADCR) 11: (I2S2_ADCL+I2S2_ADCR)/2
7:4	R/W	0x0	Reserved
3	R/W	0x0	I2S2_ADCP_ENA I2S2 ADC Companding enable(8-bit mode only)

			00: Disable 01: Enable
2	R/W	0x0	I2S2_ADCP_SEL I2S2 ADC Companding mode select 0: A-law 1: u-law
1:0	/	/	/

REG 22H_I2S2 SDIN Control Register

Default: 0x0000			Register Name: I2S2_SDIN_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S2_DACL_ENA I2S2 DAC left channel enable 0: Disable 1: Enable
14	R/W	0x0	I2S2_DACR_ENA I2S2 DAC right channel enable 0: Disable 1: Enable
13:12	R/W	0x0	Reserved
11:10	R/W	0x0	I2S2_DACL_SRC I2S2 DAC left channel data source select 00: I2S2_DACL 01: I2S2_DACR 10: (I2S2_DACL+I2S2_DACR) 11: (I2S2_DACL+I2S2_DACR)/2
9:8	R/W	0x0	I2S2_DACR_SRC I2S2 DAC right channel data source select 00: I2S2_DACR 01: I2S2_DACL 10: (I2S2_DACL+I2S2_DACR) 11: (I2S2_DACL+I2S2_DACR)/2
7:4	R/W	0x0	Reserved
3	R/W	0x0	I2S2_DACP_ENA I2S2 DAC Companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	I2S2_ DACP_SEL I2S2 DAC Companding mode select 0: A-law 1: u-law
1	R/W	0x0	Reserved

0	R/W	0x0	I2S2_LOOP_EN I2S2 loopback enable 0: No loopback 1: Loopback(SDOUT2 data output to SDOUT2 data input)

REG 23H_I2S2 Digital Mixer Source Select Register

Default: 0x0000			Register Name: I2S2_MXR_SRC
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	I2S2_ADCL_MXR_SRC I2S2 ADC left channel mixer source select 0: Disable 1:Enable Bit15: I2S1_DA0L data Bit14: I2S1_DA1L data Bit13: I2S2_DACR data Bit12: ADCL data
11:8	R/W	0x0	I2S2_ADCR_MXR_SRC I2S2 ADC right channel mixer source select 0: Disable 1:Enable Bit11: I2S1_DA0R data Bit10: I2S1_DA1R data Bit9: I2S2_DACL data Bit8: ADCR data
7:0	R/W	0x0	Reserved

REG 24H_I2S2 Volume Control 1 Register

Default: 0xA0A0			Register Name: I2S2_VOL_CTRL1
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	I2S2_ADCL_VOL I2S2 ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …………….. 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …………….. 0xFF = 71.25dB
7:0	R/W	0xA0	I2S2_ADCR_VOL I2S2 ADC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step)

			0x00: Mute 0x01: -119.25dB …………….. 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …………….. 0xFF = 71.25dB

REG 26H_I2S2 Volume Control 2 Register

Default: 0xA0A0			Register Name: I2S2_VOL_CTRL2
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	I2S2_DACL_VOL I2S2 DAC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …………….. 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …………….. 0xFF = 71.25dB
7:0	R/W	0xA0	I2S2_DACR_VOL I2S2 DAC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …………….. 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …………….. 0xFF = 71.25dB

REG 28H_I2S2 Digital Mixer Gain Control Register

Default: 0x0000			Register Name: I2S2_MXR_GAIN
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	I2S2_ADCL_MXR_GAIN I2S2 ADC left channel mixer gain control 0: 0dB 1: -6dB

			Bit15: I2S1_DA0L data Bit14: I2S1_DA1L data Bit13: I2S2_DACR data Bit12: ADCL data
11:8	R/W	0x0	I2S2_ADCR_MXR_GAIN I2S2 ADC right channel mixer gain control 0: 0dB 1: -6dB Bit11: I2S1_DA0R data Bit10: I2S1_DA1R data Bit9: I2S2_DACL data Bit8: ADCR data
7:0	R/W	0x0	Reserved

REG 30H_I2S3 BCLK/LRCK Control Register

Default: 0x0000			**Register Name: I2S3_CLK_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	Reserved
14	R/W	0x0	I2S3_BCLK_INV I2S3 BCLK Polarity 0: Normal 1: Inverted
13	R/W	0x0	I2S3_LRCK_INV I2S3 LRCK Polarity 0: Normal 1: Inverted
12:6	R/W	0x0	Reserved
5:4	R/W	0x0	I2S3_WORD_SIZ I2S3 digital interface world length 00: 8bit 01: 16bit 10: 20bit 11: 24bit
3:2	R/W	0x0	Reserved
1:0	R/W	0x0	I2S3_CLOC_SRC I2S3 BCLK/LRCK source control 0: BCLK/LRCK Come from I2S1 1: BCLK/LRCK Come from I2S2 2: BCLK/LRCK is generated by I2S3, and the source clock is I2S1CLK 3: Reserved

REG 31H_I2S3 SDOUT Control Register

Default: 0x0000			Register Name: I2S3_SDOUT_CTRL
Bit	**Read/Write**	**Default**	**Description**
15:4	R/W	0x0	Reserved
3	R/W	0x0	I2S3_ADCP_ENA I2S3 ADC Companding enable 00: Disable 01: Enable
2	R/W	0x0	I2S3_ ADCP_SEL I2S3 ADC Companding mode select 0: A-law 1: u-law
1:0	R/W	0x0	Reserved

REG 32H_I2S3 SDIN Control Register

Default: 0x0000			Register Name: I2S3_SDIN_CTRL
Bit	**Read/Write**	**Default**	**Description**
15:4	R/W	0x0	Reserved
3	R/W	0x0	I2S3_DACP_ENA I2S3 DAC Companding enable(8-bit mode only) 00: Disable 01: Enable
2	R/W	0x0	I2S3_ DACP_SEL I2S3 DAC Companding mode select 00: u-law 01: A-law
1	R/W	0x0	Reserved
0	R/W	0x0	I2S3_LOOP_ENA I2S3 loopback enable 0: No loopback 1: Loopback(SDOUT3 data output to SDOUT3 data input)

REG 33H_I2S3 Signal Path Control Register

Default: 0x0000			Register Name: I2S3_SGP_CTRL
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	Reserved
11:10	R/W	0x0	I2S3_ADC_SRC I2S3 PCM output source select 00: None

			01: I2S2_ADCL 10: I2S2_ADCR 11: Reserved
9:8	R/W	0x0	I2S2_DAC_SRC I2S2 DAC input source select 00: (I2S2_ADCL+ I2S2_ADCR) 01: Left input from I2S3_DAC; Right input from I2S2_ADCR 10: Left input from I2S2_ADCL; Right input from I2S3_DAC 11: Reserved
7:0	R/W	0x0	Reserved

REG 40H_ADC Digital Control Register

Default: 0x0000			**Register Name: ADC_DIG_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ENAD ADC Digital part enable 0: Disable 1: Enable
14	R/W	0x0	ENDM Digital microphone enable 0: Analog ADC mode 1: Digital microphone mode
13	R/W	0x0	ADFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12:4	R/W	0x0	Reserved
3:2	R/W	0x0	ADOUT_DTS ADC Delay Time For transmitting data after ENAD 00:5ms 01:10ms 10:20ms 11:30ms
1	R/W	0x0	ADOUT_DLY ADC Delay Function enable for transmitting data after ENAD 0: Disable 1: Enable
0	R/W	0x0	Reserved

REG 41H_ADC Volume Control Register

Default: 0xA0A0			Register Name: ADC_VOL_CTRL
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	ADC_VOL_L ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB
7:0	R/W	0xA0	ADC_VOL_R ADC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB ……………… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB ……………… 0xFF = 71.25dB

REG 44H_HMIC Control 1 Register

Default: 0x0000			Register Name: HMIC_CTRL1
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	HMIC_M debounce when Key down or key up
11:8	R/W	0x0	HMIC_N debounce when earphone plug in or pull out
7	R/W	0x0	HMIC_DATA_IRQ_MODE Hmic Data Irq Mode Select 0: Hmic data irq once after key down 1: Hmic data irq from key down, util key up
6:5	R/W	0x0	HMIC_TH1_HYSTERESIS Hmic Hysteresis Threshold1 00: no Hysteresis 01: Pull Out when Data <= (Hmic_th2-1)

			10: Pull Out when Data <= (Hmic_th2-2) 11: Pull Out when Data <= (Hmic_th2-3)
4	R/W	0x0	HMIC_PULLOUT_IRQ_EN Hmic Earphone Pull out Irq Enable 00: disable 11: enable
3	R/W	0x0	HMIC_PLUGIN_IRQ_EN Hmic Earphone Plug in Irq Enable 00: disable 11: enable
2	R/W	0x0	HMIC_KEYUP_IRQ_EN Hmic Key Up Irq Enable 00: disable 11: enable
1	R/W	0x0	HMIC_KEYDOWN_IRQ_EN Hmic Key Down Irq Enable 00: disable 11: enable
0	R/W	0x0	HMIC_DATA_IRQ_EN Hmic Data Irq Enable 0: disable 1: enable

REG 45H_HMIC Control 2 Register

Default: 0x0000			**Register Name: HMIC_CTRL2**
Bit	**Read/Write**	**Default**	**Description**
15:14	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11: Down by 8, 16Hz
13	R/W	0x0	HMIC_TH2_HYSTERESIS Hmic Hysteresis Threshold2 0: no Hysteresis 1: Key Up when Data <= (Hmic_th2-1)
12:8	R/W	0x0	HMIC_TH2 Hmic_th2 for detecting Key down or Key up.
7:6	R/W	0x0	HMIC_SF Hmic Smooth Filter setting 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8
5	R/W	0x0	KEYUP_CLEAR Key Up Irq Pending bit auto clear when Key Down Irq 0: don't clear 1: auto clear
4:0	R/W	0x0	HMIC_TH1

			Hmic_th1[4:0], detecting eraphone plug in or pull out.

REG 46H_HMIC Status Register

Default: 0x0000			**Register Name: HMIC_STATUS**
Bit	**Read/Write**	**Default**	**Description**
15:13	R/W	0x0	Reserved
12:8	R	0x0	HMIC_DATA HMIC Average Data
7:5	R/W	0x0	Reserved
4	R/W	0x0	HMIC_PULLOUT_PENDING Hmic Earphone Pull out Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Pull out Irq Pending Interrupt
3	R/W	0x0	HMIC_PLUGIN_PENDING Hmic Earphone Plug in Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Plug in Irq Pending Interrupt
2	R/W	0x0	HMIC_KEYUP_PENDING Hmic Key Up Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key up Irq Pending Interrupt
1	R/W	0x0	HMIC_KEYDOWN_PENDING Hmic Key Down Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Key down Irq Pending Interrupt
0	R/W	0x0	HMIC_DATA_PENDING Hmic Data Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Data Irq Pending Interrupt

REG 48H_DAC Digital Control Register

Default: 0x0000			**Register Name: DAC_DIG_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ENDA. DAC Digital Part Enable 0: Disabe 1: Enable
14	R/W	0x0	ENHPF HPF Function Enable 0: Enable 1: Disable

13	R/W	0x0	DAFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12	R/W	0x0	Reserved
11:8	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
7:0	R/W	0x0	Reserved

REG 49H_DAC Volume Control Register

Default: 0xA0A0			**Register Name: DAC_VOL_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	DAC_VOL_L DAC left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB .... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB .... 0xFF = 71.25dB
7:0	R/W	0xA0	DAC_VOL_R DAC right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB .... 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB .... 0xFF = 71.25dB

REG 4CH_DAC Digital Mixer Source Select Register

Default: 0x0000			**Register Name: DAC_MXR_SRC**
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	DACL_MXR_SRC

			DAC left channel mixer source select 0: Disable 1:Enable Bit15: I2S1_DA0L Bit14: I2S1_DA1L Bit13: I2S2_DACL Bit12: ADCL
11:8	R/W	0x0	DACR_MXR_SRC DAC right channel mixer source select 0: Disable 1:Enable Bit11: I2S1_DA0R Bit10: I2S1_DA1R Bit9: I2S2_DACR Bit8: ADCR
7:0	R/W	0x0	Reserved

REG 4DH_DAC Digital Mixer Gain Control Register

Default: 0x0000			**Register Name: DAC_MXR_GAIN**
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	DACL_MXR_GAIN DAC left channel mixer gain control 0: 0dB 1: -6dB Bit15: I2S1_DA0L Bit14: I2S1_DA1L Bit13: I2S2_DACL Bit12: ADCL
11:8	R/W	0x0	DACR_MXR_GAIN DAC right channel mixer gain control 0: 0dB 1: -6dB Bit11: I2S1_DA0R Bit10: I2S1_DA1R Bit9: I2S2_DACR Bit8: ADCR
7:0	R/W	0x0	Reserved

REG 50H_ADC Analog Control Register

Default:0x3340			**Register Name: ADC_APC_CTRL**
Bit	**R/W**	**Default**	**Description**
15	R/W	0x0	ADCREN ADC Right channel Enable 0: Disable; 1: Enable
14:12	R/W	0x3	ADCRG

			ADC Right channel input Gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
11	R/W	0x0	ADCLEN ADC Left channel Enable 0: Disable; 1: Enable
10:8	R/W	0x3	ADCLG ADC Left channel input Gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
7	R/W	0x0	MBIASEN Master microphone BIAS Enable 0: Disable; 1: Enable
6	R/W	0x1	MMIC_BIAS_CHOPPER_EN Main MICrophone BIAS chopper Enable 0: Disable; 1: Enable
5:4	R/W	0x0	MMIC_BIAS_CHOPPER_CKS Main MICrophone BIAS chopper Clock select 00: 250k 01: 500k 10: 1Meg 11: 2Meg
3	/	/	/
2	R/W	0x0	HBIASMOD HBIAS&ADC working mode 0: HBIAS is enabled only when with load 1: HBIAS is enabled when HBIASEN write 1
1	R/W	0x0	HBIASEN Headset microphone BIAS Enable 0: Disable; 1: Enable
0	R/W	0x0	HBIASADCEN Headset microphone BIAS Current sensor & ADC Enable 0: Disable; 1: Enable

REG 51H_ADC Source Select Register

Default:0x0000			**Register Name: ADC_SRC**
Bit	**R/W**	**Default**	**Description**
15:14	/	/	/
13:7	R/W	0x0	RADC_MIXMUTE Right ADC Mixer Mute Control: 0: Mute; 1:On Bit 13: MIC1 Boost stage Bit 12: MIC2 Boost stage Bit 11: LINEINL-LINEINR Bit 10: LINEINR

			Bit 9: AUXINR Bit 8: Right output mixer Bit 7: Left output mixer
6:0	R/W	0x0	LADC_MIXMUTE Left ADC Mixer Mute Control: 0: Mute; 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: LINEINL-LINEINR Bit 3: LINEINL Bit 2: AUXINL Bit 1: Left output mixer Bit 0: Right output mixer

REG 52H_ADC Source Boost Control Register

Default:0x4444			**Register Name: ADC_SRCBST_CTRL**
Bit	**R/W**	**Default**	**Description**
15	R/W	0x0	MIC1AMPEN MIC1 boost AMPlifier ENable 0: Disable; 1: Enable
14:12	R/W	0x4	MIC1BOOST MIC1 boost amplifier Gain control 0dB when 000, and from 30dB to 48dB when 001 to 111
11	R/W	0x0	MIC2AMPEN MIC2 boost AMPlifier ENable 0: Disable; 1: Enable
10:8	R/W	0x4	MIC2BOOST MIC2 boost amplifier Gain control 0dB when 000, and from 30dB to 48dB when 001 to 111
7	R/W	0x0	MIC2SLT MIC2 Source select 0: MIC2; 1: MIC3
6:4	R/W	0x4	LINEIN_DIFF_PREG LINEINL-LINEINR differential signal pre-amplifier gain control -12dB to 9dB, 3dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x4	AXI_PREG AXI pre-amplifier gain control -12dB to 9dB, 3dB/step, default is 0dB

REG 53H_Output Mixer & DAC Analog Control Register

Default:0x0f80			Register Name: OMIXER_DACA_CTRL
Bit	**R/W**	**Default**	**Description**
15	R/W	0x0	DACAREN Internal DAC Analog Right channel Enable 0:Disable 1:Enable
14	R/W	0x0	DACALEN Internal DAC Analog Left channel Enable 0:Disable 1:Enable
13	R/W	0x0	RMIXEN Right Analog Output Mixer Enable 0:Disable 1:Enable
12	R/W	0x0	LMIXEN Left Analog Output Mixer Enable 0:Disable 1:Enable
11:9	R/W	0xf	HP_DCRM_EN Headphone DC offset remove function enable 0:Disable 1:Enable To remove the headphone buffer DC offset, this bit must be set 0xf before headphone PA enabled, and this bit must be set 0x0 before headphone PA disabled
7:0	R/W	0x80	Reserved

REG 54H_Output Mixer Source Select Register

Default:0x0000			Register Name: OMIXER_SR
Bit	**R/W**	**Default**	**Description**
15:14	/	/	/
13:7	R/W	0x0	RMIXMUTE Right Output Mixer Mute Control 0-Mute, 1-On Bit 13: MIC1 Boost stage Bit 12: MIC2 Boost stage Bit 11: LINEINL-LINEINR Bit 10: LINEINR Bit 9: AUXINR Bit 8: DACR

			Bit 7: DACL
6:0	R/W	0x0	LMIXMUTE Left Output Mixer Mute Control 0-Mute, 1-On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: LINEINL-LINEINR Bit 3: LINEINL Bit 2: AUXINL Bit 1: DACL Bit 0: DACR

REG 55H_Output Mixer Source Boost Register

Default:0x56DB			**Register Name: OMIXER_BST1_CTRL**
Bit	**R/W**	**Default**	**Description**
15:14	R/W	0x1	HBIASSEL HMICBIAS voltage level select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V
13:12	R/W	0x1	MBIASSEL MMICBIAS voltage level select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V
11:9	R/W	0x3	AXG AXin to L or R output mixer Gain control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
8:6	R/W	0x3	MIC1G MIC1 to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
5:3	R/W	0x3	MIC2G MIC2 to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
2:0	R/W	0x3	LINEING LINEINL/R to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

REG 56H_Headphone Output Control Register

Default:0x0001			**Register Name: HPOUT_CTRL**
Bit	**R/W**	**Default**	**Description**
15	R/W	0x0	RHPS Right Headphone Power Amplifier (PA) Input Source Select 0: DACR 1: Right Analog Mixer
14	R/W	0x0	LHPS Left Headphone Power Amplifier (PA) Input Source Select 0: DACL 1: Left Analog Mixer
13	R/W	0x0	RHPPA_MUTE All input source to Right Headphone PA mute, including Right Output mixer and Internal DACR: 0:Mute, 1: On
12	R/W	0x0	LHPPA_MUTE All input source to Left Headphone PA mute, including Left Output mixer and Internal DACL: 0:Mute, 1: On
11	R/W	0x0	HPPA_EN Right & Left Headphone Power Amplifier Enable 0: Disable 1: Enable
10	/	/	/
9:4	R/W	0x0	HP_VOL Headphone Volume Control, (HPVOL): Total 64 level, from 0dB to -62dB, 1dB/step, mute when 000000
3:2	R/W	0x0	HPPA_DEL Headphone delay time when start up 00: 4ms 01: 8ms 10: 16ms 11: 32ms
1:0	R/W	0x1	HPPA_IS Headphone PA output stage current select 00 is minimum, 11 is maximum

REG 57H_Earpiece Output Control Register

Default:0x8200			**Register Name: ERPOUT_CTRL**
Bit	**R/W**	**Default**	**Description**
15	R/W	0x1	Reserved

14:12	R/W	0x0	/
12:11	R/W	0x0	EAR_RAMP_TIME Earpiece ramp time select 00: 256ms 01: 512ms 10: 640ms 11: 768ms
10:9	R/W	0x1	ESPA_OUT_CURRENT Earpiece output stage current set 00 is minimum, 11is maximum
8:7	R/W	0x0	ESPSR Earpiece input source select 00: DACR 01: DACL 10: Right Analog Mixer 11: Left Analog Mixer
6	R/W	0x0	ESPPA_MUTE All input source to Earpiece PA mute, including Left Output mixer and Internal DACL: 0:Mute, 1: On
5	R/W	0x0	ESPPA_EN Earpiece Power Amplifier Enable 0: Disable 1: Enable
4:0	R/W	0x0	ESP_VOL Earpiece Volume Control, Total 31 level, from 0dB to -43.5dB, 1.5dB/step, mute when 00000 & 00001

REG 58H_Speaker Output Control Register

Default:0x0880			**Register Name: SPKOUT_CTRL**
Bit	**R/W**	**Default**	**Description**
15:13	R/W	0x0	Reserved
12	R/W	0x0	RSPKS Right speaker input source select 0: MIXR 1: MIXL+MIXR
11	R/W	0x1	RSPKINVEN Right speaker negative output enable 0: Disable; 1: Enable
10	/	/	/
9	R/W	0x0	RSPK_EN Right Speaker Enable 0: Disable; 1: Enable

8	R/W	0x0	LSPKS Left speaker input source select 0: MIXL 1: MIXL+MIXR
7	R/W	0x1	LSPKINVEN Left speaker negative output enable 0: Disable; 1: Enable
6	/	/	/
5	R/W	0x0	LSPK_EN Left Speaker Enable 0: Disable; 1: Enable
4:0	R/W	0x0	SPK_VOL Right & Left speaker VOLume control Total 31 level, from 0dB to -43.5dB, 1.5db/step, mute when 00000&00001

REG 59H_Lineout Control Register

Default:0x8060			**Register Name: LOUT_CTRL**
Bit	**R/W**	**Default**	**Description**
15:8	R/W	0x80	Reservd
7:5	R/W	0x3	LINEOUTG Line out Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
4	R/W	0x0	LINEOUTEN Line out Enable 0: disable 1: enable
3	R/W	0x0	LINEOUTS0 MIC1 Boost stage to Line out mute 0: Mute, 1: On
2	R/W	0x0	LINEOUTS1 MIC2 Boost stage to Line out mute 0: Mute, 1: On
1	R/W	0x0	LINEOUTS2 Right Output mixer to Line out mute 0: Mute, 1: On
0	R/W	0x0	LINEOUTS3 Left Output mixer to Line out mute 0: Mute, 1: On

REG 80H_ADC DAP Left Status Register

Default: 0x0000	**Register Name: AC_ADC_DAPLSTA**

Bit	Read/Write	Default	Description
15:10	R	0x0	Reserved
9	R	0x0	Left AGC saturation flag
8	R	0x0	Left AGC noise-threshold flag
7:0	R	0x0	Left Gain applied by AGC (7.1 format 2s complement(-20dB – 40dB), 0.5B/ step) 0x50: 40dB 0x4F: 39.5dB --------------- 0x00: 00dB 0xFF: -0.5dB

REG 81H_ADC DAP Right Status Register

Default: 0x0000			**Register Name: AC_ADC_DAPRSTA**
Bit	**Read/Write**	**Default**	**Description**
11:10	R	0x0	Reserved
9	R	0x0	Right AGC saturation flag
8	R	0x0	Right AGC noise-threshold flag
7:0	R	0x0	Right Gain applied by AGC (7.1 format 2s complement(-20dB – 40dB), 0.5dB /step) 0x50: 40dB 0x4F: 39.5dB --------------- 0x00: 00dB 0xFF: -0.5dB

REG 82H_ADC DAP Left Channel Control Register

Default: 0x0000			**Register Name: AC_ADC_DAPLCTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	Reserved
14	R/W	0x0	Left AGC enable 0: disable 1: enable
13	R/W	0x0	Left HPF enable 0: disable 1: enable
12	R/W	0x0	Left Noise detect enable 0: disable 1: enable
11:10	R/W	0x0	Reserved
9:8	R/W	0x0	Left Hysteresis setting 00: 1dB 01: 2dB 10: 4dB

			11: disable;
7:4	R/W	0x0	Left Noise debounce time 0000: disable 0001: 4/fs 0010: 8/fs ------------ 1111: 16*4096/fs T=$2^{(N+1)}$/fs, except N=0
3:0	R/W	0x0	Left Signal debounce time 0000: disable 0001: 4/fs 0010: 8/fs ------------ 1111: 16*4096/fs T=$2^{(N+1)}$/fs, except N=0

REG 83H_ADC DAP Right Channel Control Register

Default: 0x0000			**Register Name: AC_ADC_DAPRCTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	Reserved
14	R/W	0x0	Right AGC enable 0: disable 1: enable
13	R/W	0x0	Right HPF enable 0: disable 1: enable
12	R/W	0x0	Right Noise detect enable 0: disable 1: enable
11:10	R/W	0x0	Reserved
9: 8	R/W	0x0	Right Hysteresis setting 00: 1dB 01: 2dB 10: 4dB 11: disable
7: 4	R/W	0x0	Right Noise debounce time 0000: disable 0001: 4/fs 0010: 8/fs ------------ 1111: 16*4096/fs T=$2^{(N+1)}$/fs ,except N=0
3: 0	R/W	0x0	Right Signal debounce time 0000: disable 0001: 4/fs 0010: 8/fs

			------------ 1111: 16*4096/fs $T=2^{(N+1)}/fs$, except N=0

REG 84H_ADC DAP Left Target Level Register

Default: 0x2C28			**Register Name: AC_ADC_DAPLTL**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:8	R/W	0x2C (-20dB)	Left channel target level setting(-1dB -- -30dB).(6.0format 2s complement)
7:0	R/W	0x28 (20dB)	Left channel max gain setting(0-40dB).(7.1format 2s complement)

REG 85H_ADC DAP Right Target Level Register

Default: 0x2C28			**Register Name: AC_ADC_DAPRTL**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:8	R/W	0x2C(-20dB)	Right channel target level setting(-1dB -- -30dB).(6.0format 2s complement)
7:0	R/W	0x28(20dB)	Right channel max gain setting (0-40dB). (7.1format 2s complement)

REG 86H_ADC DAP Left High Average Coef Register

Default: 0x0005			**Register Name: AC_ADC_DAPLHAC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Left channel output signal average level coefficient setting(the coefficient [reg86[10:0],reg87] is 3.24 format 2s complement)

REG 87H_ADC DAP Left Low Average Coef Register

Default: 0x1EB8			**Register Name: AC_ADC_DAPLLAC**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	Left channel output signal average level coefficient setting(the coefficient [reg86[10:0],reg87] is 3.24 format 2s complement)

REG 88H_ADC DAP Right High Average Coef Register

Default: 0x0005			Register Name: AC_ADC_DAPRHAC
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Right channel output signal average level coefficient setting(the coefficient [reg88[10:0],reg89] is 3.24 format 2s complement)

REG 89H_ADC DAP Right Low Average Coef Register

Default: 0x1EB8			Register Name: AC_ADC_DAPRLAC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	Right channel output signal average level coefficient setting(the coefficient [reg88[10:0],reg89] is 3.24 format 2s complement)

REG 8AH_ADC DAP Left Decay Time Register

Default: 0x001F			Register Name: AC_ADC_DAPLDT
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x001F (32x32fs)	Left decay time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ------------------------ 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

REG 8BH_ADC DAP Left Attack Time Register

Default: 0x0000			Register Name: AC_ADC_DAPLAT
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x0000	Left attack time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ------------------------ 7FFF: 2^{15} x32/fs

			T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.

REG 8CH_ADC DAP Right Decay Time Register

Default: 0x001F			**Register Name: AC_ADC_DAPRDT**
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x001F (32x32fs)	Right decay time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ------------------------ 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

REG 8DH_ADC DAP Right Attack Time Register

Default: 0x0000			**Register Name: AC_ADC_DAPRAT**
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x0000	Right attack time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ------------------------ 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.

REG 8EH_ADC DAP Noise Threshold Register

Default: 0x1E1E			**Register Name:AC_ADC_DAPNTH**
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12:8	R/W	0x1E (-90dB)	Left channel noise threshold setting. 0x00: -30dB 0x01: -32dB 0x02: -34dB --

			0x1D: -88dB 0x1E: -90dB 0x1F: -90dB(the same as 0x1E)
7:5	/	/	/
4:0	R/W	0x1E(-90dB)	Right channel noise threshold setting(-90 -- -30dB). 0x00: -30dB 0x01: -32dB 0x02: -34dB --- 0x1D: -88dB 0x1E: -90dB 0x1F: -90dB(the same as 0x1E

REG 8FH_ADC DAP Left Input Signal High Average Coef Register

Default: 0x0005			**Register Name: AC_ADC_DAPLHNAC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Left input signal average filter coefficient to check noise or not(the coefficient [reg8f[10:0],reg90] is 3.24 format 2s complement), always the same as the left output signal average filter's.

REG 90H_ADC DAP Left Input Signal Low Average Coef Register

Default: 0x1EB8			**Register Name: AC_ADC_DAPLLNAC**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0005	Left input signal average filter coefficient to check noise or not(the coefficient [reg8f[10:0],reg90] is 3.24 format 2s complement) always the same as the left output signal average filter's

REG 91H_ADC DAP Right Input Signal High Average Coef Register

Default: 0x0005			**Register Name: AC_ADC_DAPRHNAC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Right input signal average filter coefficient to check noise or not(the coefficient [reg91[10:0],reg92] is 3.24 format 2s complement), always the same as the right output signal average filter's

REG 92H_ADC DAP Right Input Signal Low Average Coef Register

Default: 0x1EB8			Register Name: AC_ADC_DAPRLNAC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	Right input signal average filter coefficient to check noise or not(the coefficient [reg91[10:0],reg92] is 3.24 format 2s complement), always the same as the right output signal average filter's

REG 93H_ADC DAP High HPF Coef Register

Default: 0x00FF			Register Name: AC_DAPHHPFC
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x00FF	HPF coefficient setting(the coefficient [reg93[10:0],reg14] is 3.24 format 2s complement)

REG 94H_ADC DAP Low HPF Coef Register

Default: 0xFAC1			Register Name: AC_DAPLHPFC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xFAC1	HPF coefficient setting(the coefficient [reg93[10:0],reg14] is 3.24 format 2s complement)

REG 95H_ADC DAP Optimum Register

Default: 0x0000			Register Name: AC_DAPOPT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10	R/W	0	Left energy default value setting(include the input and output) 0: min 1: max
9:8	R/W	00	Left channel gain hystersis setting. The different between target level and the signal level must larger than the hystersis when the gain change. 00: 0.4375db 01: 0.9375db 10: 1.9375db 11: 3db
7:6	/	/	/

5	R/W	0	The input signal average filter coefficient setting 0: is the [reg8f[10:0], reg90] and [reg91[1:0], reg92]; 1: is the [reg86[10:0], reg87] and [reg88[1:0], reg89];
4	R/W	0	AGC output when the channel in noise state 0: output is zero 1: output is the input data
3	/	/	/
2	R/W	0	Right energy default value setting(include the input and output) 0: min 1: max
1:0	R/W	00	Right channel gain hystersis setting. The different between target level and the signal level must larger than the hystersis when the gain change. 00: 0.4375db 01: 0.9375db 10: 1.9375db 11: 3db

REG A0H_DAC DAP Control Register

Default: 0x0000			**Register Name: AC_DAC_DAPCTRL**
Bit	**Read/Write**	**Default**	**Description**
15:3	/	/	/
2	R/W	0	DRC enable control 0: disable 1: enable
1	R/W	0	Left channel HPF enable control 0: disable 1: enable
0	R/W	0	Right channel HPF enable control 0: disable 1: enable

REG A1H_DAC DAP High HPF Coef Register

Default: 0x00FF			**Register Name: AC_DAC_DAPHHPFC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting(the coefficient [reg a1[10:0], reg a2] is 3.24 format 2s complement)

REG A2H_DAC DAP Low HPF Coef Register

Default: 0xFAC1	**Register Name: AC_DAC_DAPLHPFC**

Bit	Read/Write	Default	Description
15:0	R/W	0xFAC1	HPF coefficient setting(the coefficient [reg a1[10:0], reg a2] is 3.24 format 2s complement)

REG A3H_DAC DAP Left High Energy Average Coef Register

Default: 0x0100			Register Name: AC_DAC_DAPLHAVC
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0100	Left channel energy average filter coefficient setting(the coefficient [reg a3[10:0], reg a4] is 3.24 format 2s complement)

REG A4H_DAC DAP Left Low Energy Average Coef Register

Default: 0x0000			Register Name: AC_DAC_DAPLLAVC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	Left channel energy average filter coefficient setting(the coefficient [rega3[10:0],rega4] is 3.24 format 2s complement)

REG A5H_DAC DAP Right High Energy Average Coef Register

Default: 0x0100			Register Name: AC_DAC_DAPRHAVC
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0100	Right channel energy average filter coefficient setting(the coefficient [reg a5[10:0], reg a6] is 3.24 format 2s complement)

REG A6H_DAC DAP Right Low Energy Average Coef Register

Default: 0x0000			Register Name: AC_DAC_DAPRLAVC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	Right channel energy average filter coefficient setting(the coefficient [reg a5[10:0],reg a6] is 3.24 format 2s complement)

REG A7H_DAC DAP High Gain Decay Time Coef Register

Default: 0x0100	Register Name: AC_DAC_DAPHGDEC

Bit	Read/Write	Default	Description
15:11	/	/	/
10:0	R/W	0x0100	Gain smooth filter decay time coefficient setting(the coefficient [reg a7[10:0], reg a8] is 3.24 format 2s complement)

REG A8H_DAC DAP Low Gain Decay Time Coef Register

Default: 0x0000			**Register Name: AC_DAC_DAPLGDEC**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	Gain smooth filter decay time coefficient setting(the coefficient [reg a7[10:0], reg a8] is 3.24 format 2s complement)

REG A9H_DAC DAP High Gain Attack Time Coef Register

Default: 0x0100			**Register Name: AC_DAC_DAPHGATC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0100	Gain smooth filter attack time coefficient setting(the coefficient [reg a9[10:0], reg aa] is 3.24 format 2s complement)

REG AAH_DAC DAP Low Gain Decay Time Coef Register

Default: 0x0000			**Register Name: AC_DAC_DAPLGATC**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	Gain smooth filter attack time coefficient setting(the coefficient [reg a9[10:0], reg aa] is 3.24 format 2s complement)

REG ABH_DAC DAP High Energy Threshold Register

Default: 0x04FB			**Register Name: AC_DAC_DAPHETHD**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x04FB	The DRC Energy compress threshold parameter T setting(the T = [reg ab, reg ac] is 8.24 format 2s complement)

REG ACH_DAC DAP Low Energy Threshold Register

Default: 0x9ED0			**Register Name: AC_DAC_DAPLETHD**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x9ED0	The DRC Energy compress threshold parameter T setting(the T = [reg ab, reg ac] is 8.24 format 2s complement)

REG ADH_DAC DAP High Gain K Parameter Register

Default: 0x0780			**Register Name: AC_DAC_DAPHGKPA**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0780	The DRC gain curve slope k parameter setting(the K = [reg ad[10:0], reg ae] is 3.24 format 2s complement)

REG AEH_DAC DAP Low Gain K Parameter Register

Default: 0x0000			**Register Name: AC_DAC_DAPLGKPA**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	The DRC gain curve slope k parameter setting(the K = [reg ad[10:0], reg ae] is 3.24 format 2s complement)

REG AFH_DAC DAP High Gain Offset Parameter Register

Default: 0x0100			**Register Name: AC_DAC_DAPHGOPA**
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12:0	R/W	0x0100	The DRC gain curve offset O parameter setting(the O = [reg af[12:0], reg b0] is 5.24 format 2s complement)

REG B0H_DAC DAP Low Gain Offset Parameter Register

Default: 0x0000			**Register Name: AC_DAC_DAPLGOPA**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	The DRC gain curve offset O parameter setting(the K = [reg af[12:0], regb0] is 5.24 format 2s complement)

REG B1H _DAC DAP Optimum Register

Default: 0x0000			**Register Name: AC_DAC_DAPOPT**
Bit	**Read/Write**	**Default**	**Description**
15:6	/	/	/
5	R/W	0	DRC gain defaut value setting 0: The default gain is 1 1: The default gain is 0
4:0	R/W	0x00	The hysteresis of the gain smooth filter to use the decay time coefficient or the attack time coefficient. When in the decay time state, if g(n-1)-g(n)>hysteresis, then the state will change to attack time state, and when in the attack time, if g(n)-g(n-1)>hysteresis, then the state will change to decay time state. Note the hysteresis of 0x00 and 0x04 is the same. 00000: 2^{-16} 00001: 2^{-19} 00010: 2^{-18} 00011: 2^{-17} 00100: 2^{-16} ----------------- 10011: 2^{-1} 10100 ~11111: 1 hysteresis = 2^{n-20} ,except n=0x00, and n less 0x14.

REG B4H_ADC DAP Enable Register

Default: 0x0000			**Register Name: ADC_DAP_ENA**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S1_ADCL0_AGC_ENA I2S1 ADC timeslot 0 left channel AGC enable 0: Disable 1: Enable
14	R/W	0x0	I2S1_ADCR0_AGC_ENA I2S1 ADC timeslot 0 right channel AGC enable 0: Disable

			1: Enable
13	R/W	0x0	I2S1_ADCL1_AGC_ENA I2S1 ADC timeslot 1 left channel AGC enable 0: Disable 1: Enable
12	R/W	0x0	I2S1_ADCR1_AGC_ENA I2S1 ADC timeslot 1 right channel AGC enable 0: Disable 1: Enable
11	R/W	0x0	I2S2_ADCL_AGC_ENA I2S2 ADC left channel AGC enable 0: Disable 1: Enable
10	R/W	0x0	I2S2_ADCR_AGC_ENA I2S2 ADC right channel AGC enable 0: Disable 1: Enable
9	R/W	0x0	I2S2_DACL_AGC_ENA I2S2 DAC left channel AGC enable 0: Disable 1: Enable
8	R/W	0x0	I2S2_DACR_AGC_ENA I2S2 DAC right channel AGC enable 0: Disable 1: Enable
7	R/W	0x0	ADCL_AGC_ENA ADC left channel AGC enable 0: Disable 1: Enable
6	R/W	0x0	ADCR_AGC_ENA ADC right channel AGC enable 0: Disable 1: Enable
5:0	R/W	0x0	Reserved

REG B5H_DAC DAP Enable Register

Default: 0x0000			**Register Name: DAC_DAP_ENA**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	I2S1_DAC0_DRC_ENA I2S1 DAC timeslot 0 DRC enable 0: Disable 1: Enable

14	R/W	0x0	Reserved
13	R/W	0x0	I2S1_DAC1_DRC_ENA I2S1 DAC timeslot 1 DRC enable 0: Disable 1: Enable
12	R/W	0x0	Reserved
11	R/W	0x0	I2S2_DAC_DRC_ENA I2S2 DAC DRC enable 0: Disable 1: Enable
10:8	R/W	0x0	Reserved
7	R/W	0x0	DAC_DRC_ENA DAC DRC enable 0: Disable 1: Enable
6:0	R/W	0x0	Reserved

REG B8H_SRC1 Control 1 Register

Default: 0x0000			**Register Name: SRC1_CTRL1**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	SRC1_RATI_ENA SRC1 Manual setting ratio enable 0-disable 1-enable
14	R	0x0	SRC1_LOCK_STS SRC1 Ratio lock status 0-not locked 1-locked
13	R	0x0	SRC1_FIFO_OVR SRC1 FIFO Overflow status 0-normal 1-overflowed
12:10	R	0x0	SRC1_FIFO_LEV_[8:6] SRC1 FIFO Level high 3-bit
9:0	R/W	0x0	SRC1_RATI_SET_[25:16] Manual setting ratio high 10-bit

REG B9H_SRC1 Control 2 Register

Default: 0x0000			**Register Name: SRC1_CTROL2**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	SRC1_RATI_StET_[15:0] Manual setting ratio low 16-bi

REG BAH_SRC1 Control 3 Register

Default: 0x0040			**Register Name: SRC1_CTRL3**
Bit	**Read/Write**	**Default**	**Description**
15:10	R	0x0	SRC1_FIFO_LEV_[5:0] SRC1 FIFO Level low 6-bit
9:0	R	0x40	SRC1_RATI_VAL_[25:16] Calculated ratio high 10-bit

REG BBH_SRC1 Control 4 Register

Default: 0x0000			**Register Name: SRC1_CTRL4**
Bit	**Read/Write**	**Default**	**Description**
15:0	R	0x0	SRC1_RATI_VAL_[15:0] Calculated ratio low 16-bit

REG BCH_SRC2 Control 1 Register

Default: 0x0000			**Register Name: SRC2_CTRL1**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	SRC2_RATI_ENA SRC2 Manual setting ratio enable 0-disable 1-enable
14	R	0x0	SRC2_LOCK_STS SRC2 Ratio lock status 0-not locked 1-locked
13	R	0x0	SRC2_FIFO_OVR SRC2 FIFO Overflow status 0-normal 1-overflowed
12:10	R	0x0	SRC2_FIFO_LEV_[8:6] SRC2 FIFO Level high 3-bit
9:0	R/W	0x0	SRC2_RATI_SET_[25:16] Manual setting ratio high 10-bit

REG BDH_SRC2 Control 2 Register

Default: 0x0000			**Register Name: SRC2_CTRL2**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	SRC2_RATI_SET_[15:0] Manual setting ratio low 16-bit

REG BEH_SRC2 Control 3 Register

Default: 0x0040			**Register Name: SRC2_CTRL3**
Bit	**Read/Write**	**Default**	**Description**
15:10	R	0x0	SRC2_FIFO_LEV_[5:0] SRC2 FIFO Level low 6-bit
9:0	R	0x0	SRC2_RATI_VAL_[25:16] Calculated ratio high 10-bit

REG BFH_SRC2 Control 4 Register

Default: 0x0000			**Register Name: SRC2_CTRL4**
Bit	**Read/Write**	**Default**	**Description**
15:0	R	0x0	SRC2_RATI_VAL_[15:0] Calculated ratio low 16-bit

REG C0H_RTC Analog Control Register

Default: 0x003F			**Register Name: CLK32KOUT_ACTRL**
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0x00	Reserved
7	R/W	0x0	CLK32AP_OD_CTR CLK32KAP Output Pin Open Drain mode control 0: push-pull 1: reserved
6:4	R/W	0x3	VBG_TRM VIO_RTC Voltage trimming 0: 1.08V 1: 1.12V 2: 1.16V 3: 1.2V 4: 1.24V 5: 1.28V 6: 1.32V 7: 1.36V
3:2	R/W	0x3	XTAL_G xtal gain control 3: largest gain 0: smallest gain
1	R/W	0x1	XTAL_DEB xtal fater startup config 0: slower startup 1: faster startup
0	R/W	0x1	XTAL_EN xtal enable 0: xtal disable

			1: xtal enable

REG C1H_CK32K Output Control Register 1

Default: 0x00e1			Register Name: CK32K_OUT_CTRL1
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0x0	Reserved
7:5	R/W	0x3	CK32KAP_PRE_DIV Pre-division after 4MHz input from ADDA. 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 122(32KHz)
4	R/W	0x0	CK32KAP_MUX_SEL CK32KAP Output source select control. 0: 32KHz from RTC 1: 4MHz from ADDA
3:1	R/W	0x0	CK32KAP_POST_DIV Post-division after clock selection. 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
0	R/W	0x1	CK32KAP_ENA CK32KAP Output enable control. 0: Disable output 1: Enable output

REG C2H_CK32K Output Control Register 2

Default: 0x0000			Register Name: CK32K_OUT_CTRL2
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0x0	Reserved
7:5	R/W	0x0	CK32KBB_PRE_DIV Pre-division after 4MHz input from ADDA.

			000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 122(32KHz)
4	R/W	0x0	CK32KBB_MUX_SEL CK32KBB Output source select control. 0: 32KHz from RTC 1: 4MHz from ADDA
3:1	R/W	0x0	CK32KBB_POST_DIV Post-division after clock selection. 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
0	R/W	0x0	CK32KBB_ENA CK32KBB Output enable control. 0: Disable output 1: Enable output

REG C3H_CK32K Output Control Register 3

Default: 0x0000			**Register Name: CK32K_OUT_CTRL3**
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0x0	Reserved
7:5	R/W	0x0	CK32KMD_PRE_DIV Pre-division after 4MHz input from ADDA. 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 122(32KHz)
4	R/W	0x0	CK32KMD_MUX_SEL CK32KMD Output source select control.

			0: 32KHz from RTC 1: 4MHz from ADDA
3:1	R/W	0x0	CK32KMD_POST_DIV Post-division after clock selection. 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
0	R/W	0x0	CK32KMD_ENA CK32KMD Output enable control. 0: Disable output 1: Enable output

REG C6H_RTC Reset Register

Default: 0x0000			**Register Name: RTC_RST_REG**
Bit	**Read/Write**	**Default**	**Description**
15:8	WO	0x0	RTC_KEY_FIELD. RTC key field should be written at value 0x53. Writing any other value in this field aborts the write operation.
7:1	/	/	/
0	R/W	0x0	RTC_RESET. When this bit is set to 1, then all registers of time will be reset to default values. 0: No effect; 1: Reset relevant registers.

REG C7H_RTC Control Register

Default: 0x0000			**Register Name: RTC_CTRL_REG**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	RTC_SIM RTC simulation bit. When this bit is set ‘1’, the relevant registers will rolling-over faster, such as second/minute/hour ext. 0: Normal mode, 1: Simulation mode.
14:3	/	/	/
2	R/W	0x0	Error mode

			0 = Do not affect current Time/Week/Date 1 = Set the wrong segment to max value
1	R/W	0x0	RTC_STOP RTC stop bit. When this bit is set '1', the relevant registers will stop rolling-over, such as second/minute/hour ext. 0: No stop, 1: Stop rolling-over.
0	R/W	0x0	12H_24H_MODE. 0: 12 hour mode. 1: 24 hour mode.

REG C8H_RTC Seconds Register

Default: 0x0000			**Register Name: RTC_SEC_REG**
Bit	**Read/Write**	**Default**	**Description**
15:7	/	/	/
6:0	R/W	0x0	RTC_SEC These bits represent the current second value coded in BCD format. The value should be from 0 to 59. For example, if the [6:0] is '1011001', this represents the value 59.

REG C9H_RTC Minutes Register

Default: 0x0000			**Register Name: RTC_MIN_REG**
Bit	**Read/Write**	**Default**	**Description**
15:7	/	/	/
6:0	R/W	0x0	RTC_MIN These bits represent the current minute value coded in BCD format. The value should be from 0 to 59.

REG CAH_RTC Hours Register

Default: 0x0001			**Register Name: RTC_HOU_REG**
Bit	**Read/Write**	**Default**	**Description**
15:9	/	/	/
8	R/W	0x0	AM_PM_SEL AM/PM select. 0: AM, 1: PM.
7:6	/	/	/
5:0	R/W	0x1	RTC_HOU

			These bits represent the current hour value coded in BCD format. The value should be from 0 to 23.

REG CBH_RTC Weekdays Register

Default: 0x0000			**Register Name: RTC_WEE_REG**
Bit	**Read/Write**	**Default**	**Description**
15:3	/	/	/
2:0	R/W	0x0	RTC_WEE These bits represent the current weekday value coded in BCD format. The value should be from 0 to 6. 000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday

REG CCH_RTC Days Register

Default: 0x0001			**Register Name: RTC_DAY_REG**
Bit	**Read/Write**	**Default**	**Description**
15:6	/	/	/
5:0	R/W	0x1	RTC_DAY These bits represent the current day value coded in BCD format. The value should be from 1 to 31.

REG CDH_RTC Months Register

Default: 0x0001			**Register Name: RTC_MON_REG**
Bit	**Read/Write**	**Default**	**Description**
15:5	/	/	/
4:0	R/W	0x1	RTC_MON These bits represent the current day value coded in BCD format. The value should be from 1 to 12.

REG CEH_RTC Years Register

Default: 0x0000			**Register Name: RTC_YEA_REG**
Bit	**Read/Write**	**Default**	**Description**

15	R/W	0x0	LEAP_YEAR 0: Not leap year 1: Leap year. This bit will not set by hardware. It should be set or clear by software.
14:8	/	/	/
7:0	R/W	0x0	RTC_YEA These bits represent the current day value coded in BCD format. The max value is 99(0x10011001).

REG CFH_RTC Update Trigger

Default: 0x0000			Register Name: RTC_UPD_TRIG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	Time/Week/Date write trigger 0 = Nothing will happen. 1 = Writing a 1 to this bit will update the Time/Week/Date value. This bit will always be 0 when being read.
14:1	R/W	0x0	Reserved
0	R/W	0x0	REG_C8H-REG_CEH Read control 0: Read the effective real time clock value 1: Read the value of REG_C8H-REG_CEH written by host

REG D0H_Alarm Interrupt Enable Register

Default: 0x0000			Register Name: ALM_INT_ENA
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/
0	R/W	0x0	ALM_INT_ENA Alarm interrupt enable. 0: Alarm interrupt disable 1: Alarm interrupt enable

REG D1H_Alarm Interrupt Status Register

Default: 0x0000			Register Name: ALM_INT_STA_REG
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/
0	R/W	0x0	ALM_INT_STS Alarm interrupt status. Set 1 to this bit will clear it. 0: Alarm interrupt is not pending; 1: Alarm interrupt is pending.

REG D8H_Alarm Seconds Register

Default: 0x0000			Register Name: ALM_SEC_REG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_SEC_ENA Second alarm enable bit. 0: Disable second alarm; 1: Enable second alarm.
14:7	/	/	/
6:0	R/W	0x0	ALM_SEC_SET These bits represent the current second value coded in BCD format. The value should be from 0 to 59. For example, if the [6:0] is ‘1011001’, this represents the value 59.

REG D9H_Alarm Minutes Register

Default: 0x0000			Register Name: ALM_MIN_REG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_MIN_ENA Minute alarm enable bit. 0: Disable minute alarm; 1: Enable minute alarm.
14:7	/	/	/
6:0	R/W	0x0	ALM_MIN_SET These bits represent the current minute value coded in BCD format. The value should be from 0 to 59.

REG DAH_Alarm Hours Register

Default: 0x0001			Register Name: ALM_HOU_REG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_HOU_ENA Hour alarm enable bit. 0: Disable hour alarm; 1: Enable hour alarm.
14:9	/	/	/
8	R/W	0x0	AM_PM_SEL AM/PM select. 0: AM, 1: PM.
7:6	/	/	/
5:0	R/W	0x1	ALM_HOU_SET

			These bits represent the current hour value coded in BCD format. The value should be from 0 to 23.

REG DBH_Alarm Weekdays Register

Default: 0x0000			**Register Name: ALM_WEEK_REG**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_WEE_ENA Week alarm enable bit. 0: Disable hour alarm; 1: Enable hour alarm.
14:3	/	/	/
2:0	R/W	0x0	ALM_WEE_SET These bits represent the current weekday value coded in BCD format. The value should be from 0 to 6. 000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday

REG DCH_Alarm Days Register

Default: 0x0001			**Register Name: ALM_DAY_REG**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_DAY_ENA Day alarm enable bit. 0: Disable day alarm; 1: Enable day alarm.
14:6	/	/	/
5:0	R/W	0x1	ALM_DAY_SET These bits represent the current day value coded in BCD format. The value should be from 1 to 31.

REG DDH_Alarm Months Register

Default: 0x0001			**Register Name: ALM_MON_REG**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_MON_ENA Month alarm enable bit.

			0: Disable month alarm; 1: Enable month alarm.
14:5	/	/	/
4:0	R/W	0x1	ALM_MON_SET These bits represent the current day value coded in BCD format. The value should be from 1 to 12.

REG DEH_Alarm Years Register

Default: 0x0000			Register Name: ALM_YEA_REG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ALM_YEA_ENA Year alarm enable bit. 0: Disable year alarm; 1: Enable year alarm.
14:5	/	/	/
7:0	R/W	0x0	ALM_YEA_SET These bits represent the current day value coded in BCD format.

REG DFH_Alarm Update Trigger

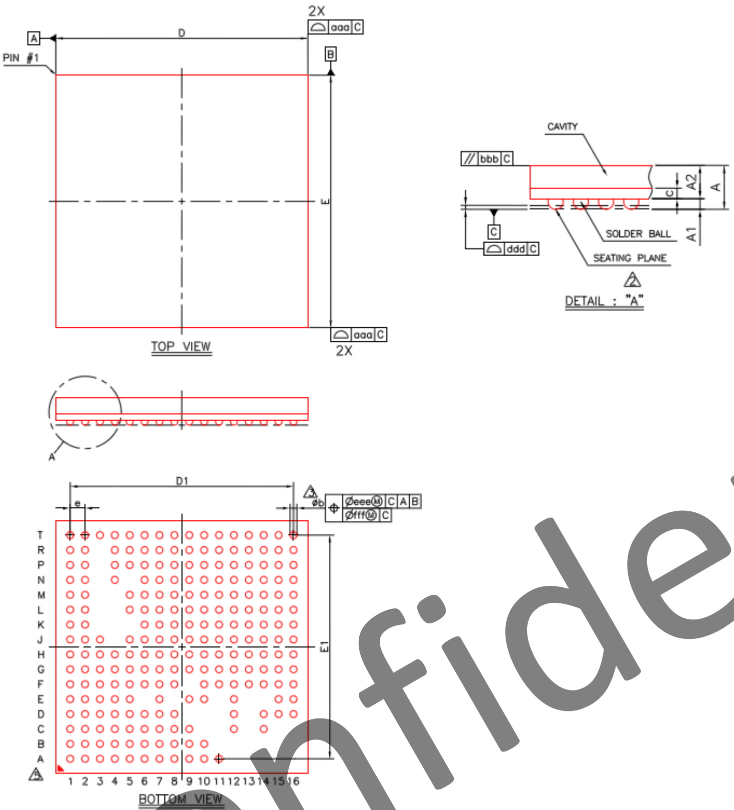
Default: 0x0000			Register Name: ALM_UPD_TRIG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	Time/Week/Date write trigger 0 = Nothing will happen. 1 = Writing a 1 to this bit will update the alarm Time/Week/Date value. This bit will always be 0 when being read.
14:1	R/W	0x0	Reserved
0	R/W	0x0	REG_D8H-REG_DEH Read control 0: Read the effective alarm setting value 1: Read the value of REG_D8H-REG_DEH written by host

REG E0H-EFH RTC General Purpose Register n(n=0-15)

Default: 0x0000			Register Name: RTC_GP_REGn
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	RTC_GP_DATn These bits art used to save data.(n = 0~15)

16 Package

Figure 16-1 shows the package dimension of AXP813(11mm x 11mm, 218-ball, BGA).



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.17	1.24	0.043	0.046	0.049
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	---	9.75	---	---	0.384	---
E1	---	9.75	---	---	0.384	---
e	---	0.65	---	---	0.026	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	16 / 16					

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5

TITLE :218LD TFBGA (11X11 mm) PACKAGE OUTLINE			
APPR.			
PE. (M/D,B/P,S/P,S/G)		DWG NO.	PS00102
PD.		REV NO.	A
QM.		DATE	06/20/'14
CHK.		DWG.	Victor Liu

Figure 16-1 AXP813 Package

Order Information:

Table 16-1

Type	Quantity	Part Number
Tray	pcs/Tray Trays/package	AXP813

