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AIC800G3 Datasheet

Quad-Core Application Processor

Version 1.4

July 20, 2020

Revision History

Version	Date	Description
V1.0	2020-04-11	Initial release version
V1.1	2020-05-15	Updated information of EMAC and PWM
V1.2	2020-05-26	Updated information of Pin number
V1.3	2020-06-09	Updated Block Diagram
V1.4	2020-07-20	Updated Operate Temperature

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1. Overview

The AIC800G3 is a high performance quad-core application processor that based on ARM Cortex™-A53 CPU architecture.

Main features of AIC800G3 include:

- **CPU architecture :** High efficient 64-bit quad-core Cortex™-A53
- **Display :** support various kind display interface for high resolution LCD panel, including MIPI DSI 1920 x 1200, LVDS 1920 x 1200, RGB 1920 x 1200
- **Memory :** SIP 1GB LPDDR4, support many types of external memory devices, including NAND Flash, Nor Flash and SD/SDIO/SMMC
- **Camera** : Support time division multiplexing ISP for 2x MIPI-CSI
- **Peripheral** : Support a broad range of hardware interfaces, including 1x USB OTG, 1x USB HOST, 8x TWI, 8x UART, 3x I2S, 3x SPI, etc.
- **Network** : Support 2x 10/100/1000Mbps EMAC complied to IEEE802.3-2002
- **OS** : Android 10.0

2. Feature

2.1. CPU Architecture

- Quad-core ARM Cortex Cortex™ -A53 processor
- Power-efficient ARM v8 architecture
- 64 -bit and 32-bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced SIMD (Single Instruction Multiple Data) instruction for acceleration of media and signal processing functions
- VFPv4 Floating Point Unit
- 32 KB L1 Instruction cache and 32 KB L1 Data cache for per CPU
- 512 KB L2 cache shared

2.2. GPU Architecture

- Imagination GE8300
- Support OpenGL ES 1.1/2.0/3.2. Vulkan 1.1, OpenCL 1.2

2.3. Memory Subsystem

Boot ROM

- On -chip memory
- Supports system boot from the following devices:
  - SD/eMMC(SMHC0, SMHC2)
  - Nand Flash
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Supports mandatory upgrade process through SMHC0 and USB
- Supports GPIO pin to select the kind of boot media to boot
- Supports GPADC to select the kind of boot media to boot
- Supports SID(effuse) to select the kind of boot media to boot
- Secure brom supports load only certified firmware
- Secure brom ensures that the secure boot is a trusted environment

SDRAM

- SIP 1GB 32bit LPDDR4
- Clock frequency up to 792MHz
- Runtime-configurable parameters setting for application flexibility

NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 1 ready_busy signals
- Supports SLC/ML C flash and EF-NAND
- Supports SDR, ONFI DDR 1.0, Toggle DDR 1.0, ONFI DDR 2.0 and Toggle DDR 2.0 RAW NAND FLASH

SD/MMC Interface

- Three SD/MMC host controller(SMHC) interfaces
- SMHC0 controls the devices that comply with the Secure Digital(SD3.0)
  - 4-bit bus width
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output(SDIO3.0)
  - 4-bit bus width
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- SMHC2 controls the devices that comply with the Multimedia Card(eMMC 5.1)
  - 8-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.4. System Peripherals

Timer

- The timer module implements the timing and counting functions, which includes Timer0, Timer1, Watchdog and AVS0, AVS1
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factors
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0

- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing
- 2 AVS counters (AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime
  - 12 -bit frequency divider factor
  - Pause/Start function

High Speed Timer

- One high speed timer with 56 -bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low low-frequency oscillator for count clock
- Timer frequency: 1 kHz
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- Supports a calibration function of 32.768 kHz obtained by RC16M clock division
- Supports fanout function of internal 32K clock
- 8 general purpose registers for storing power power-off information

GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 160 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization

DMA

- Up to 8-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes

- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to -peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

CCU

- 12 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

Thermal Sensor Controller

- Temperature accuracy: ±3 °C from 0°C to +100 °C , ±5°C from -25 °C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Three thermal sensors: sensor0 located in the CPU, sensor1 located in the GPU , and sensor2 located in the DDR

CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc.
- Capable of other CPU-related control, including interface control, CP15 control, and power on/off control
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc.
- Including CPU debug control and status register

IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE0, VE, CSI, ISP, G2D parallel address mapping
- Supports DE0, VE, CSI, ISP, G2D bypass function independently
- Supports DE0, VE, CSI, ISP, G2D prefetch independently
- Supports DE0, VE, CSI, ISP, G2D interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

Spinlock

- Provides a hardware synchronization mechanism in multi-core system
- Supports 32 lock units to prevent multi processors from handling the shared data at the same time
- Two kinds of lock status: locked and unlocked

- The lock time of the processor is less than 200 cycles

Message Box

- Provides interrupt communication mechanism for on-chip processor
- The communication parties transmit information by a channel
- Interrupt alarm function

2.5. Video and Graphics

Display Engine

- Output size up to2048x 2048
- Four alpha blending channels for main display, three channels for aux display
- Four overlay layers in each channel, and has an independent scaler
- Potter-duff compatible blending operation
- Input format: YUV422/ YUV420/ YUV411/ ARGB8888/ XRGB8888/ RGB888/ ARGB4444/ ARGB1555 and RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  -Adaptive detail/edge enhancement
  -Adaptive color enhancement
  -Adaptive contrast enhancement and fresh tone rectify
  -Content adaptive backlight control
- Supports write back only for high efficient main display and miracast

Graphic 2D (G2D)

- Supports layer size up to 2048x2048 pixels
- Supports input/output formats: YUV422(semi-planar and planar format)/YUV420(semi-planar and planar format)/P010/P210/P410/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ARGB2101010 and RGB565
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

2.6. Video Engine

Video Decoding

- Supports multi-format video decoder, including:
  -H.265 MP@L5.0: 4K@30fps
  -H.264 BP/MP/HP@L5.1: 4K@30fps
  -VP9: 720p@30fps
  -MPEG-4 SP/ASP: 1080p@60fps
  -MPEG-2 MP/HL: 1080p@60fps
  -MPEG-1 MP/HL: 1080p@60fps
  -VP8: 1080p@60fps

-AVS/AVS+ JiZhun@L6.0: 1080p@60fps

-H.263 BP: 1080p@60fps

-MJPEG: 1080p@60fps

-VC1 SP/MP/AP: 1080p@30fps

Video Encoding

- H.264 BP/MP/HP
- Maximum 16-megapixel(4096 x 4096) resolution for H.264 encoding
- H.264 encoding performance of 1080p@60fps
- MJPEG encoding performance of 1080p@30fps

2.7. Image Input

MIPI CSI

- Supports 2 MIPI CSI interfaces(one for 4-lane, the other for 2-lane)
- Supports image crop function
- Supports MIPI Version 1.0
- Supports 1.0 Gbps/lane
- Maximum video capture resolution up to 8M@30fps(for online mode) or 13M@10fps(for offline mode) or 4*1080p@25fps(for de-interleaver conversion chip)

ISP

- Supports one sensor in online mode, or two sensors in offline mode
- Maximum frame rate of 8M@30fps(for online mode) or 13M@10fps(for offline mode)
- Adjustable 3A functions, including automatic exposure(AE), automatic white balance(AWB) and automatic focus(AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D denoising
- Global tone mapping
- Graphics mirror and flip
- ISP tuning tools for the PC

2.8. Video Output

TCON_LCD

- RGB interface with DE/SYNC mode, up to 1920 x 1200@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- LVDS interface with dual link, up to 1920 x 1200@60fps
- LVDS interface with single link, up to 1366 x 768@60fps
- i8080 interface, up to 800 x 480@60fps

- Supports BT656 interface for NTSC and PAL
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

MIPI DSI

- One 4-lane MIPI DSI
- Compliance with MIPI DSI v1.01
- Compliance with MIPI DCSv1.01, bidirectional communication in LP through data lane 0
- Maximum performance up to 1920 x 1200@60fps
- Supports non-burst mode with sync pulse/sync event, burst mode and command mode
- Supports pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports ULPS and escape modes
- Hardware checksum capabilities

2.9. Audio Subsystem

Audio Codec

- Two audio digital digital-to-analog(DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8kHz to 192kHz DAC sample rate
  - 95 ±3dB SNR
- Two audio analog analog-to-digital(ADC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8kHz to 48kHz ADC sample rate
  - 95 ±3dB SNR
- One audio output interfaces:
  - One differential line output (LINEOUTLP and LINEOUTLNLINEOUTLN)
- Two audio input interfaces:
  - Two differential microphone inputs (MICIN 1P/N and MICIN 2P/N)
- Two low-noise analog microphone bias out output
- Supports Dynamic Range Controller adjusting the DAC playback and ADC capture
- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- DMA and Interrupt support

I2S/PCM

- Three I2S/PCM interfaces
- Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode
- I2S mode supports 8 channels, and 32-bit/192kbit sample rate
- I2S and TDM modes support maximum 16 channels, and 32-bit/96kbit sample rate

One Wire Audio (OWA)

- One OWA TX
- Compliance with S/PDIF interface
- IECIEC-60958 transmitter functionality
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit , 20-bit and 24-bit data formats

2.10. Security Engine

Crypto Engine (CE)

- Encryption and decryption algorithms implemented by using hardware, including AES, XTS-AES, DES, TDES , SM4
  - ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC, GCM mode for AES
  - 128/192/256-bit key for AES
  - 256-bit, 512-bit key for XTS-AES
  - ECB, CBC, CTR, CBC-MAC mode for DES
- Hash tamper proofing algorithms implemented by using hardware, including MD5, SHA, SM3, HMAC
  - SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - HMAC-SHA1, HMAC HMAC-SHA256 for HMAC
  - Supports hardware padding
  - Supports multi-package mode
- Signature and verification algorithms implemented by using hardware, including RSA , ECC
  - RSA supports 512/1024/2048/3072/4096-bit width
  - ECC supports 160/224/256/384/521-bit width
- Hardware random number generator: PRNG, TRNG, HASH+DRBG
- Security strategy and system feature
  - Symmetric, asymmetric, HASH/RBG control logics are separate, which can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time
  - Supports task chain mode for each request. Task or task chain are executed at request order
  - 8 scatter group(sg) are supported for both input and output data
  - Supports secure and non-secure interfaces respectively, each world issues task request through its own interface, they do not know the existence of each other
  - Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other

Security ID

- Supports 2 Kbits EFUSE for chip ID and security application

- EFUSE has secure zone and non-secure zone
- Supports a SRAM to backup fuse information

Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Set secure area of DRAM
- Set secure property that Master accesses to DRAM
- Set DRM area
- Set whether DRM master can access to DRM area or not

Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Set secure property of peripherals

2.11. External Peripherals

USB

- One USB 2.0 OTG(USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) in host mode
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
  - Up to 10 User-Configurable Endpoints (EPs) for Bulk, Isochronous and Interrupt bi-directional transfers
  - Supports (8 KB+64 Bytes) FIFO for all EPs (including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- One USB 2.0 HOST(USB1), with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) device

Ethernet

- 2x EMAC interface
- Compliant with IEEE 802.3-2002 standard
- Supports 10/100/1000 Mbit/s data transfer rates
- Supports RMII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes

- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

UART

- Up to 8 UART controllers(UART0, UART1, UART2, UART3, UART4, UART5, UART6, S_UART)
- UART0, UART4, UART6: 2-wire; UART1, UART2, UART3, UART5: 4-wire
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

SPI

- Up to 3 SPI controllers(SPI0, SPI1, SPI2)
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
- Interrupt or DMA support
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1-bit to32-bit
- Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI

TWI

- Up to 8 TWI controllers(TWI0, TWI1, TWI2, TWI3, TWI4, TWI5, S_TWI0, S_TWI1)
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master system supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection

- Interrupt on address detection
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in Master mode

PWM

- 11 PWM channels (PWM1~10, S_PWM PWM)
- PWM2~9 channels divide to 2 PWM pairs: PWM23 pair, PWM45 pair, PWM67 pair, PWM89 pair
- S_PWM channel has the single channel characteristics of PWM module, and has no pair function
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveforms: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0~24 MHz/100 MHz
- Various duty duty-cycle: 0%~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input
- Supports PWM group mode(4 groups), the starting phase of each channel in same group is configurable

Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit resolution
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Power supply voltage: 1.8 V, power reference voltage: 1.35 V, analog input and detected voltage range: 0~LEVELB (the maximum value is 1.266 V)

General Purpose ADC (GPADC)

- Two GPADC input channel
- 12 -bit resolution and 8-bit effective SAR type A/D converter
- Power supply voltage: 1.8 V, analog input range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Support three operation mode modes
  - Single conversion mode
  - Continuous conversion mode
  - Outbreak conversion mode

LEDC

- LEDC is used to control the external intelligent control LED lamp

- Configurable input high/low level width of LED
- Configurable LED reset time
- LEDC data supports DMA configuration mode and CPU configurable mode
- Maximum 1024 LEDs serial connect

CIR Transmitter (CIR_TX)

- Supports arbitrary wave generator
- Configurable carrier frequency
- Supports DMA shake and wait mode
- 128 bytes FIFO for data buffer

CIR Transmitter (CIR_RX)

- Full physical layer implementation
- Supports NEC format infra data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.12. Package

- TFBGA 318 balls, 0.65 mm ball pitch, 0.35 mm ball size, 18 mm x 16 mm body

3. Block Diagram

The following figure shows the block diagram of AIC800G3 processor.

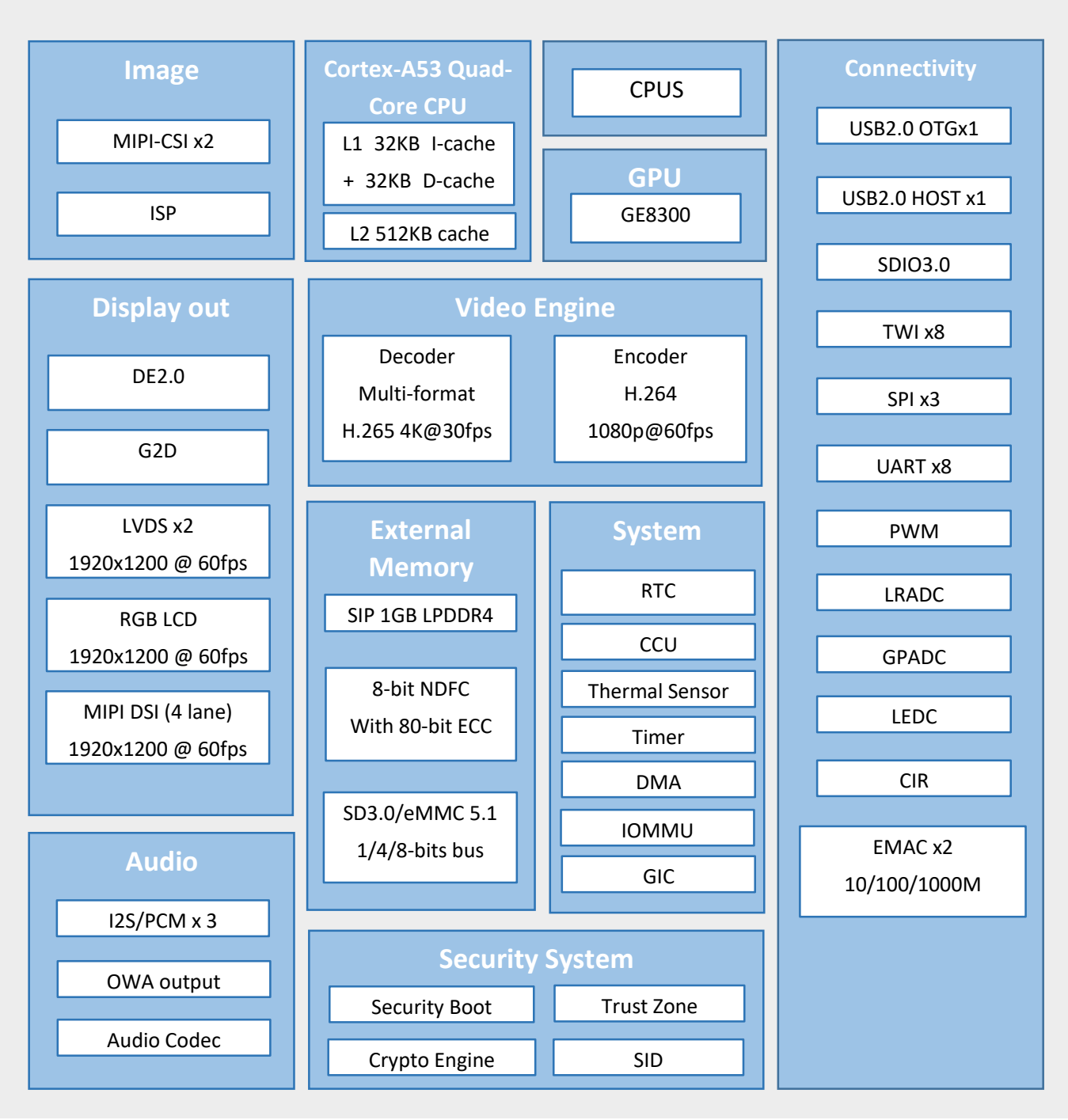


Figure 3-1. AIC800G3 Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of AIC800G3 Pins from seven aspects.

[1].Ball#: Package ball numbers associated with each signals.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

[4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled by software.

[6].Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6mA.

[7].Power Supply: The voltage supply for the terminal's IO buffers.

Table 4-1. Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
DRAM						
W2	DDRZQ	AI	Z	NA	NA	VCC_DRAM
V1	SZQ	AI	Z	NA	NA	VCC_DRAM
U2	ODT_CA_A	I	Z	NA	NA	VCC_DRAM
V2	ODT_CA_B	I	Z	NA	NA	VCC_DRAM
K8, L8, L9, M8, M9, N8, N9, P8, P9, R8	VCC_DRAM	P	NA	NA	NA	NA
T8	VDD18_DRAM	P	NA	NA	NA	NA
GPIO B						
B14	PB0	I/O	Z	PU/PD	4	VCC_IO
A14	PB1	I/O	Z	PU/PD	4	VCC_IO
B13	PB2	I/O	Z	PU/PD	4	VCC_IO
A13	PB3	I/O	Z	PU/PD	4	VCC_IO
B12	PB4	I/O	Z	PU/PD	4	VCC_IO
A12	PB5	I/O	Z	PU/PD	4	VCC_IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
B11	PB6	I/O	Z	PU/PD	4	VCC_IO
A11	PB7	I/O	Z	PU/PD	4	VCC_IO
B10	PB8	I/O	Z	PU/PD	4	VCC_IO
A10	PB9	I/O	Z	PU/PD	4	VCC_IO
A9	PB10	I/O	Z	PU/PD	4	VCC_IO
GPIO C						
AD6	PC0	I/O	Z	PU/PD	4	VCC_PC
AC6	PC1	I/O	Z	PU/PD	4	VCC_PC
AD3	PC2	I/O	Z	PU/PD	4	VCC_PC
AC3	PC3	I/O	PU	PU/PD	4	VCC_PC
AC4	PC4	I/O	PU	PU/PD	4	VCC_PC
AD5	PC5	I/O	Z	PU/PD	4	VCC_PC
AC5	PC6	I/O	PU	PU/PD	4	VCC_PC
AC7	PC8	I/O	Z	PU/PD	4	VCC_PC
AD7	PC9	I/O	Z	PU/PD	4	VCC_PC
AC8	PC10	I/O	Z	PU/PD	4	VCC_PC
AD8	PC11	I/O	Z	PU/PD	4	VCC_PC
AD4	PC12	I/O	Z	PU/PD	4	VCC_PC
AC9	PC13	I/O	Z	PU/PD	4	VCC_PC
AD9	PC14	I/O	Z	PU/PD	4	VCC_PC
AC10	PC15	I/O	Z	PU/PD	4	VCC_PC
AD10	PC16	I/O	Z	PU/PD	4	VCC_PC
T12,U12	VCC_PC	P	NA	NA	NA	NA
GPIO D						
AC1	PD0	I/O	Z	PU/PD	4	VCC_PD
AD2	PD1	I/O	Z	PU/PD	4	VCC_PD
AB1	PD2	I/O	Z	PU/PD	4	VCC_PD
AC2	PD3	I/O	Z	PU/PD	4	VCC_PD
Y1	PD4	I/O	Z	PU/PD	4	VCC_PD
AA2	PD5	I/O	Z	PU/PD	4	VCC_PD
AA1	PD6	I/O	Z	PU/PD	4	VCC_PD
AB2	PD7	I/O	Z	PU/PD	4	VCC_PD
W1	PD8	I/O	Z	PU/PD	4	VCC_PD
Y2	PD9	I/O	Z	PU/PD	4	VCC_PD
U11	VCC_PD	P	NA	NA	NA	NA
U13	VCC_LVDS0	P	NA	NA	NA	NA
GPIO E						
AC14	PE0	I/O	Z	PU/PD	4	VCC_PE
AD15	PE1	I/O	Z	PU/PD	4	VCC_PE
AC15	PE2	I/O	Z	PU/PD	4	VCC_PE
AD16	PE3	I/O	Z	PU/PD	4	VCC_PE
AC16	PE4	I/O	Z	PU/PD	4	VCC_PE

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
AD14	PE5	I/O	Z	PU/PD	4	VCC_PE
AC13	PE6	I/O	Z	PU/PD	4	VCC_PE
AD13	PE7	I/O	Z	PU/PD	4	VCC_PE
T13	VCC_PE	P	NA	NA	NA	NA
GPIO F						
A26	PF0	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
B26	PF1	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
A25	PF2	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
B25	PF3	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
A24	PF4	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
B24	PF5	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
B27	PF6	I/O	Z	PU/PD	4	VCC_IO, or VCC_EFUSE
GPIO G						
E2	PG0	I/O	Z	PU/PD	4	VCC_PG
G2	PG1	I/O	PU	PU/PD	4	VCC_PG
F1	PG2	I/O	PU	PU/PD	4	VCC_PG
F2	PG3	I/O	PU	PU/PD	4	VCC_PG
D1	PG4	I/O	PU	PU/PD	4	VCC_PG
E1	PG5	I/O	PU	PU/PD	4	VCC_PG
G1	PG6	I/O	Z	PU/PD	4	VCC_PG
H2	PG7	I/O	Z	PU/PD	4	VCC_PG
H1	PG8	I/O	Z	PU/PD	4	VCC_PG
J2	PG9	I/O	Z	PU/PD	4	VCC_PG
J17	VCC_PG	P	NA	NA	NA	NA
GPIO H						
B17	PH0	I/O	Z	PU/PD	4	VCC_IO
A18	PH1	I/O	Z	PU/PD	4	VCC_IO
B18	PH2	I/O	Z	PU/PD	4	VCC_IO
A19	PH3	I/O	Z	PU/PD	4	VCC_IO
A16	PH4	I/O	Z	PU/PD	4	VCC_IO
B16	PH5	I/O	Z	PU/PD	4	VCC_IO
A17	PH6	I/O	Z	PU/PD	4	VCC_IO
B15	PH7	I/O	Z	PU/PD	4	VCC_IO
B19	PH9	I/O	Z	PU/PD	4	VCC_IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
A20	PH10	I/O	Z	PU/PD	4	VCC_IO
B20	PH13	I/O	Z	PU/PD	4	VCC_IO
B21	PH14	I/O	Z	PU/PD	4	VCC_IO
A21	PH15	I/O	Z	PU/PD	4	VCC_IO
B22	PH16	I/O	Z	PU/PD	4	VCC_IO
A22	PH17	I/O	Z	PU/PD	4	VCC_IO
B23	PH18	I/O	Z	PU/PD	4	VCC_IO
A23	PH19	I/O	Z	PU/PD	4	VCC_IO
GPIO I						
B8	PI0	I/O	Z	PU/PD	4	VCC_IO
A8	PI1	I/O	Z	PU/PD	4	VCC_IO
B7	PI2	I/O	Z	PU/PD	4	VCC_IO
A7	PI3	I/O	Z	PU/PD	4	VCC_IO
B6	PI4	I/O	Z	PU/PD	4	VCC_IO
A6	PI5	I/O	Z	PU/PD	4	VCC_IO
B5	PI6	I/O	Z	PU/PD	4	VCC_IO
A5	PI7	I/O	Z	PU/PD	4	VCC_IO
B4	PI8	I/O	Z	PU/PD	4	VCC_IO
A4	PI9	I/O	Z	PU/PD	4	VCC_IO
GPIO J						
H26	PJ0	I/O	Z	PU/PD	4	VCC_PJ
G27	PJ1	I/O	Z	PU/PD	4	VCC_PJ
G26	PJ2	I/O	Z	PU/PD	4	VCC_PJ
F27	PJ3	I/O	Z	PU/PD	4	VCC_PJ
F26	PJ4	I/O	Z	PU/PD	4	VCC_PJ
E27	PJ5	I/O	Z	PU/PD	4	VCC_PJ
E26	PJ6	I/O	Z	PU/PD	4	VCC_PJ
D27	PJ7	I/O	Z	PU/PD	4	VCC_PJ
M26	PJ8	I/O	Z	PU/PD	4	VCC_PJ
L27	PJ9	I/O	Z	PU/PD	4	VCC_PJ
L26	PJ10	I/O	Z	PU/PD	4	VCC_PJ
K27	PJ11	I/O	Z	PU/PD	4	VCC_PJ
K26	PJ12	I/O	Z	PU/PD	4	VCC_PJ
J27	PJ13	I/O	Z	PU/PD	4	VCC_PJ
J26	PJ14	I/O	Z	PU/PD	4	VCC_PJ
H27	PJ15	I/O	Z	PU/PD	4	VCC_PJ
T26	PJ16	I/O	Z	PU/PD	4	VCC_PJ
R27	PJ17	I/O	Z	PU/PD	4	VCC_PJ
R26	PJ18	I/O	Z	PU/PD	4	VCC_PJ
P27	PJ19	I/O	Z	PU/PD	4	VCC_PJ
P26	PJ20	I/O	Z	PU/PD	4	VCC_PJ
N27	PJ21	I/O	Z	PU/PD	4	VCC_PJ

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
N26	PJ22	I/O	Z	PU/PD	4	VCC_PJ
M27	PJ23	I/O	Z	PU/PD	4	VCC_PJ
T27	PJ24	I/O	Z	PU/PD	4	VCC_PJ
C26	PJ25	I/O	Z	PU/PD	4	VCC_PJ
D26	PJ26	I/O	Z	PU/PD	4	VCC_PJ
C27	PJ27	I/O	Z	PU/PD	4	VCC_PJ
U16	VCC_PJ	P	NA	NA	NA	NA
T16	VCC_LVDS1	P	NA	NA	NA	NA
GPIO L						
R1	PL0	I/O	PU	PU/PD	4	VCC_PL
P2	PL1	I/O	PU	PU/PD	4	VCC_PL
P1	PL2	I/O	Z	PU/PD	4	VCC_PL
N2	PL3	I/O	Z	PU/PD	4	VCC_PL
N1	PL4	I/O	Z	PU/PD	4	VCC_PL
M2	PL5	I/O	Z	PU/PD	4	VCC_PL
M1	PL6	I/O	Z	PU/PD	4	VCC_PL
L2	PL7	I/O	Z	PU/PD	4	VCC_PL
L1	PL8	I/O	Z	PU/PD	4	VCC_PL
K2	PL9	I/O	Z	PU/PD	4	VCC_PL
K1	PL10	I/O	Z	PU/PD	4	VCC_PL
J1	PL11	I/O	Z	PU/PD	4	VCC_PL
H17	VCC_PL	P	NA	NA	NA	NA
USB						
AD12	USB0_DM	A I/O	NA	NA	NA	VCC_USB
AC12	USB0_DP	A I/O	NA	NA	NA	VCC_USB
AD11	USB1_DM	A I/O	NA	NA	NA	VCC_USB
AC11	USB1_DP	A I/O	NA	NA	NA	VCC_USB
U17	VCC_USB	P	NA	NA	NA	NA
P19	VDD_USB	P	NA	NA	NA	NA
Audio Codec						
AA26	MBIAS	AO	NA	NA	NA	VCC_IO
Y26	MICIN1N	AI	NA	NA	NA	AVCC
Y27	MICIN1P	AI	NA	NA	NA	AVCC
W26	MICIN2N	AI	NA	NA	NA	AVCC
W27	MICIN2P	AI	NA	NA	NA	AVCC
V26	VRA1	AO	NA	NA	NA	AVCC
V27	VRA2	AO	NA	NA	NA	AVCC
AB26	AVCC	P	NA	NA	NA	NA
U20	AGND	G	NA	NA	NA	NA
AD25	CPVEE	P	NA	NA	NA	CPVIN
AA27	LINEOUTLP	AO	NA	NA	NA	AVCC
AB27	LINEOUTLN	AO	NA	NA	NA	AVCC
AC26	CPVIN	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
AC25	CPVDD	P	NA	NA	NA	CPVIN
ADC						
U26	LRADC	AI	NA	NA	NA	AVCC
AD26	GPADC1	AI	NA	NA	NA	AVCC
AC27	GPADC2	AI	NA	NA	NA	AVCC
MIPI-CSIA						
AD20	MCSIA_D0N	AI	NA	NA	NA	VCC_MCSI
AC20	MCSIA_D0P	AI	NA	NA	NA	VCC_MCSI
AD18	MCSIA_D1N	AI	NA	NA	NA	VCC_MCSI
AC18	MCSIA_D1P	AI	NA	NA	NA	VCC_MCSI
AD21	MCSIA_D2N	AI	NA	NA	NA	VCC_MCSI
AC21	MCSIA_D2P	AI	NA	NA	NA	VCC_MCSI
AD17	MCSIA_D3N	AI	NA	NA	NA	VCC_MCSI
AC17	MCSIA_D3P	AI	NA	NA	NA	VCC_MCSI
AD19	MCSIA_CKN	AI	NA	NA	NA	VCC_MCSI
AC19	MCSIA_CKP	AI	NA	NA	NA	VCC_MCSI
T17	VCC_MCSI	P	NA	NA	NA	NA
MIPI-CSIB						
AD22	MCSIB_D0N	AI	NA	NA	NA	VCC_MCSI
AC22	MCSIB_D0P	AI	NA	NA	NA	VCC_MCSI
AD24	MCSIB_D1N	AI	NA	NA	NA	VCC_MCSI
AC24	MCSIB_D1P	AI	NA	NA	NA	VCC_MCSI
AD23	MCSIB_CKN	AI	NA	NA	NA	VCC_MCSI
AC23	MCSIB_CKP	AI	NA	NA	NA	VCC_MCSI
System						
U27	FEL	I	PU	PU/PD	NA	VCC_IO
H18	BOOT_SEL	I	PU	PU/PD	NA	VCC_IO
J18	JTAG_SEL	I	PU	PU/PD	NA	VCC_IO
T1	NMI	I/O, OD	No Pull	PU/PD	NA	VCC_RTC
R2	RESET	I/O	No Pull	PU/PD	NA	VCC_PLL
RTC						
B2	X32KIN	AI	NA	NA	NA	VCC_RTC
A2	X32KOUT	AO	NA	NA	NA	VCC_RTC
A3	X32KFOUT	AO, OD	NA	NA	NA	VCC_PL, or VDD_CPUS
U1	VCC_RTC	P	NA	NA	NA	NA
T2	RTC_VIO	AO	NA	NA	NA	VCC_RTC
DXCO						
C2	DXIN	AI	NA	NA	NA	VCC_RTC
C1	DXOUT	AO	NA	NA	NA	VCC_RTC
B1	REFCLK_OUT	AO	NA	NA	NA	VCC_RTC
B3	DXLDO_OUT	AO	NA	NA	NA	VCC_RTC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength (mA)[6]	Power Supply[7]
D2	WREQIN	I	NA	NA	NA	VCC_PG
POWER						
U18	VCC_EFUSE	P	NA	NA	NA	NA
J16	VCC_PLL	P	NA	NA	NA	NA
H16	VDD_CPUS	P	NA	NA	NA	NA
H10, H11, H12, H13, H14, J11, J12, J13, J14	VDD_CPU	P	NA	NA	NA	NA
K20, L19, L20, M19, M20, N19, N20, P20	VDD_SYS	P	NA	NA	NA	NA
T14, T15, U14, U15	VCC_IO	P	NA	NA	NA	NA
H15, J15	VDD_CPUFB	P	NA	NA	NA	NA
R20,T20	VDD_SYSFB	P	NA	NA	NA	NA
A1, A15, A27, B9, H8, H9, H19, H20, J8, J9, J10, J19, J20, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, L10, L11, L12, L13, L14, L15, L16, L17, L18, M10, M11, M12, M13, M14, M15, M16, M17, M18, N10, N11, N12, N13, N14, N15, N16, N17, N18, P10, P11, P12, P13, P14, P15, P16, P17, P18, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, T9, T10, T11, T18, T19, U8, U9, U10, U19, AD1, AD27	GND	G	NA	NA	NA	NA

4.2. GPIO Multiplexing Functions

The following table provides a description of the AIC800G3 GPIO multiplexing functions.

Table 4-2. Multiplexing Functions

Pin Name	GPIO Group	IO Type	Function 2	Function3	Function 4	Function 5	Function 6
PB0	GPIOB	I/O	UART2_TX	SPI2_CS	JTAG_MS		PB_EINT0
PB1		I/O	UART2_RX	SPI2_CLK	JTAG_CK		PB_EINT1
PB2		I/O	UART2_RTS	SPI2_MOSI	JTAG_DO		PB_EINT2
PB3		I/O	UART2_CTS	SPI2_MISO	JTAG_DI		PB_EINT3
PB4		I/O	TWI1_SCK	I2S0_MCLK	JTAG_MS_GPU		PB_EINT4
PB5		I/O	TWI1_SDA	I2S0_BCLK	JTAG_CK_GPU		PB_EINT5
PB6		I/O		I2S0_LRCK	JTAG_DO_GPU		PB_EINT6
PB7		I/O		I2S0_DOUT0	I2S0_DIN1		PB_EINT7
PB8		I/O	OWA_OUT	I2S0_DIN0	I2S0_DOUT1		PB_EINT8
PB9		I/O	UART0_TX	TWI0_SCK	JTAG_DI_GPU		PB_EINT9
PB10		I/O	UART0_RX	TWI0_SDA	PWM1		PB_EINT10
PC0	GPIOC	I/O	NAND_WE	SDC2_DS			PC_EINT0
PC1		I/O	NAND_ALE	SDC2_RST			PC_EINT1
PC2		I/O	NAND_CLE		SPI0_MOSI		PC_EINT2
PC3		I/O	NAND_CE1		SPI0_CS0		PC_EINT3
PC4		I/O	NAND_CE0		SPI0_MISO		PC_EINT4
PC5		I/O	NAND_RE	SDC2_CLK			PC_EINT5
PC6		I/O	NAND_RB0	SDC2_CMD			PC_EINT6
PC8		I/O	NAND_DQ7	SDC2_D3			PC_EINT8
PC9		I/O	NAND_DQ6	SDC2_D4			PC_EINT9
PC10		I/O	NAND_DQ5	SDC2_D0			PC_EINT10
PC11		I/O	NAND_DQ4	SDC2_D5			PC_EINT11
PC12		I/O	NAND_DQS		SPI0_CLK		PC_EINT12
PC13		I/O	NAND_DQ3	SDC2_D1			PC_EINT13
PC14		I/O	NAND_DQ2	SDC2_D6			PC_EINT14
PC15		I/O	NAND_DQ1	SDC2_D2	SPI0_WP		PC_EINT15
PC16		I/O	NAND_DQ0	SDC2_D7	SPI0_HOLD		PC_EINT16
PD0	GPIOD	I/O	LCD0_D2	LVDS0_D0P	DSI_DP0	EINK0_D0	PD_EINT0
PD1		I/O	LCD0_D3	LVDS0_D0N	DSI_DM0	EINK0_D1	PD_EINT1
PD2		I/O	LCD0_D4	LVDS0_D1P	DSI_DP1	EINK0_D2	PD_EINT2
PD3		I/O	LCD0_D5	LVDS0_D1N	DSI_DM1	EINK0_D3	PD_EINT3
PD4		I/O	LCD0_D6	LVDS0_D2P	DSI_CKP	EINK0_D4	PD_EINT4
PD5		I/O	LCD0_D7	LVDS0_D2N	DSI_CKM	EINK0_D5	PD_EINT5
PD6		I/O	LCD0_D10	LVDS0_CKP	DSI_DP2	EINK0_D6	PD_EINT6
PD7		I/O	LCD0_D11	LVDS0_CKN	DSI_DM2	EINK0_D7	PD_EINT7
PD8		I/O	LCD0_D12	LVDS0_D3P	DSI_DP3	EINK0_D8	PD_EINT8
PD9		I/O	LCD0_D13	LVDS0_D3N	DSI_DM3	EINK0_D9	PD_EINT9
PE0		I/O	MIPI_MCLK0				PE_EINT0

Pin Name	GPIO Group	IO Type	Function 2	Function3	Function 4	Function 5	Function 6
PE1	GPIOE	I/O	TWI2_SCK				PE_EINT1
PE2		I/O	TWI2_SDA				PE_EINT2
PE3		I/O	TWI3_SCK				PE_EINT3
PE4		I/O	TWI3_SDA				PE_EINT4
PE5		I/O	MIPI_MCLK1	PLL_LOCK_DBG	I2S2_MCLK	LEDC	PE_EINT5
PE6		I/O		BIST_RESULT0	I2S2_BCLK		PE_EINT6
PE7		I/O	CSI_SM_VS	BIST_RESULT1	I2S2_LRCK	TCON_TRIG	PE_EINT7
PF0	GPIOF	I/O	SDC0_D1	JTAG_MS	JTAG_MS_GPU		PF_EINT0
PF1		I/O	SDC0_D0	JTAG_DI	JTAG_DI_GPU		PF_EINT1
PF2		I/O	SDC0_CLK	UART0_TX			PF_EINT2
PF3		I/O	SDC0_CMD	JTAG_DO	JTAG_DO_GPU		PF_EINT3
PF4		I/O	SDC0_D3	UART0_RX			PF_EINT4
PF5		I/O	SDC0_D2	JTAG_CK	JTAG_CK_GPU		PF_EINT5
PF6		I/O	SDC0_DET				PF_EINT6
PG0	GPIOG	I/O	SDC1_CLK				PG_EINT0
PG1		I/O	SDC1_CMD				PG_EINT1
PG2		I/O	SDC1_D0				PG_EINT2
PG3		I/O	SDC1_D1				PG_EINT3
PG4		I/O	SDC1_D2				PG_EINT4
PG5		I/O	SDC1_D3				PG_EINT5
PG6		I/O	UART1_TX				PG_EINT6
PG7		I/O	UART1_RX				PG_EINT7
PG8		I/O	UART1_RTS				PG_EINT8
PG9		I/O	UART1_CTS	I2S1_MCLK			PG_EINT9
PH0	GPIOH	I/O	TWI0_SCK			RGMII0_RXD1/ RMII0_RXD1	PH_EINT0
PH1		I/O	TWI0_SDA			RGMII0_RXD0/ RMII0_RXD0	PH_EINT1
PH2		I/O	TWI1_SCK	CPU_CUR_W		RGMII0_RXCTL/ RMII0_CRS_DV	PH_EINT2
PH3		I/O	TWI1_SDA	CIR_OUT		RGMII0_CLKIN/ RMII0_RXER	PH_EINT3
PH4		I/O	UART3_TX	SPI1_CS	CPU_CUR_W	RGMII0_TXD1/ RMII0_TXD1	PH_EINT4
PH5		I/O	UART3_RX	SPI1_CLK	LEDC	RGMII0_TXD0/ RMII0_TXD0	PH_EINT5
PH6		I/O	UART3_RTS	SPI1_MOSI	SPDIF_IN	RGMII0_TXCK/ RMII0_TXCK	PH_EINT6
PH7		I/O	UART3_CTS	SPI1_MISO	SPDIF_OUT	RGMII0_TXCTL/ RMII0_TXEN	PH_EINT7
PH9		I/O	DMIC_DATA0	SPI2_CLK	I2S2_BCLK	MDC0	PH_EINT9
PH10		I/O	DMIC_DATA1	SPI2_MOSI	I2S2_LRCK	MDIO0	PH_EINT10
PH13		I/O		TWI3_SDA	I2S3_MCLK	EPHY0_25	PH_EINT13

Pin Name	GPIO Group	IO Type	Function 2	Function3	Function 4	Function 5	Function 6
PH14		I/O			I2S3_BCLK	RGMII0_RXD3/ RMII0_NULL	PH_EINT14
PH15		I/O			I2S3_LRCK	RGMII0_RXD2/ RMII0_NULL	PH_EINT15
PH16		I/O		I2S3_DOUT0	I2S3_DIN1	RGMII0_RXCK/ RMII0_NULL	PH_EINT16
PH17		I/O		I2S3_DOUT1	I2S3_DIN0	RGMII0_TXD3/ RMII0_NULL	PH_EINT17
PH18		I/O	CIR_OUT	I2S3_DOUT2	I2S3_DIN2	RGMII0_TXD2/ RMII0_NULL	PH_EINT18
PH19		I/O	CIR_IN	I2S3_DOUT3	I2S3_DIN3	LEDC	PH_EINT19
PI0	GPIOI	I/O	TWI4_SCK	UART4_TX	PWM1		PI_EINT0
PI1		I/O	TWI4_SDA	UART4_RX	PWM2		PI_EINT1
PI2		I/O	UART5_TX	SPI1_CS	PWM3	I2S2_BCLK	PI_EINT2
PI3		I/O	UART5_RX	SPI1_CLK	PWM4	I2S2_LRCK	PI_EINT3
PI4		I/O	UART5_RTS	SPI1_MOSI	PWM5	I2S2_DOUT0	PI_EINT4
PI5		I/O	UART5_CTS	SPI1_MISO	PWM6	I2S2_DIN0	PI_EINT5
PI6		I/O	UART6_TX		PWM7	SPI2_CS	PI_EINT6
PI7		I/O	UART6_RX		PWM8	SPI2_CLK	PI_EINT7
PI8		I/O	TWI5_SCK	CIR_IN	PWM9	SPI2_MOSI	PI_EINT8
PI9		I/O	TWI5_SDA	SDC3_CLK	PWM10		PI_EINT9
PJ0	GPIOJ	I/O	LCD1_D0	LVDS2_D0P	EINK1_D0	RGMII1_RXD1/ RMII1_RXD1	PJ_EINT0
PJ1		I/O	LCD1_D1	LVDS2_D0N	EINK1_D1	RGMII1_RXD0/ RMII1_RXD0	PJ_EINT1
PJ2		I/O	LCD1_D2	LVDS2_D1P	EINK1_D2	RGMII1_RXCTL/ RMII1_CRS_DV	PJ_EINT2
PJ3		I/O	LCD1_D3	LVDS2_D1N	EINK1_D3	RGMII1_CLKIN/ RMII1_RXER	PJ_EINT3
PJ4		I/O	LCD1_D4	LVDS2_D2P	EINK1_D4	RGMII1_TXD1/ RMII1_TXD1	PJ_EINT4
PJ5		I/O	LCD1_D5	LVDS2_D2N	EINK1_D5	RGMII1_TXD0/ RMII1_TXD0	PJ_EINT5
PJ6		I/O	LCD1_D6	LVDS2_CKP	EINK1_D6	RGMII1_TXCK/ RMII1_TXCK	PJ_EINT6
PJ7		I/O	LCD1_D7	LVDS2_CKN	EINK1_D7	RGMII1_TXCTL/ RMII1_TXEN	PJ_EINT7
PJ8		I/O	LCD1_D8	LVDS2_D3P	EINK1_D8	MDC1	PJ_EINT8
PJ9		I/O	LCD1_D9	LVDS2_D3N	EINK1_D9	MDIO1	PJ_EINT9
PJ10		I/O	LCD1_D10	LVDS3_D0P	EINK1_D10	EPHY1_25	PJ_EINT10
PJ11		I/O	LCD1_D11	LVDS3_D0N	EINK1_D11	RGMII1_RXD3/ RMII1_NULL	PJ_EINT11
PJ12		I/O	LCD1_D12	LVDS3_D1P	EINK1_D12	RGMII1_RXD2/ RMII1_NULL	PJ_EINT12
PJ13		I/O	LCD1_D13	LVDS3_D1N	EINK1_D13	RGMII1_RXCK/ RMII1_NULL	PJ_EINT13

Pin Name	GPIO Group	IO Type	Function 2	Function3	Function 4	Function 5	Function 6
PJ14		I/O	LCD1_D14	LVDS3_D2P	EINK1_D14	RGMII1_TXD3/ RMII1_NULL	PJ_EINT14
PJ15		I/O	LCD1_D15	LVDS3_D2N	EINK1_D15	RGMII1_TXD2/ RMII1_NULL	PJ_EINT15
PJ16		I/O	LCD1_D16	LVDS3_CKP	SPI1_CS		PJ_EINT16
PJ17		I/O	LCD1_D17	LVDS3_CKN	SPI1_CLK		PJ_EINT17
PJ18		I/O	LCD1_D18	LVDS3_D3P	SPI1_MOSI		PJ_EINT18
PJ19		I/O	LCD1_D19	LVDS3_D3N	SPI1_MISO		PJ_EINT19
PJ20		I/O	LCD1_D20	SPI2_CS	UART3_RTS	UART2_TX	PJ_EINT20
PJ21		I/O	LCD1_D21	SPI2_CLK	UART3_CTS	UART2_RX	PJ_EINT21
PJ22		I/O	LCD1_D22	SPI2_MOSI	UART3_TX	UART2_RTS	PJ_EINT22
PJ23		I/O	LCD1_D23	SPI2_MISO	UART3_RX	UART2_CTS	PJ_EINT23
PJ24		I/O	LCD1_CLK	TWI4_SCK	UART4_TX		PJ_EINT24
PJ25		I/O	LCD1_DE	TWI4_SDA	UART4_RX		PJ_EINT25
PJ26		I/O	LCD1_HSYNC	TWI5_SCK	UART4_RTS		PJ_EINT26
PJ27		I/O	LCD1_VSYNC	TWI5_SDA	UART4_CTS		PJ_EINT27
PL0	GPIOL	I/O	S_TWI0_SCK				S_PL_EINT0
PL1		I/O	S_TWI0_SDA				S_PL_EINT1
PL2		I/O	S_UART_TX				S_PL_EINT2
PL3		I/O	S_UART_RX				S_PL_EINT3
PL4		I/O	S_JTAG_MS				S_PL_EINT4
PL5		I/O	S_JTAG_CK				S_PL_EINT5
PL6		I/O	S_JTAG_DO				S_PL_EINT6
PL7		I/O	S_JTAG_DI				S_PL_EINT7
PL8		I/O	S_TWI1_SCK				S_PL_EINT8
PL9		I/O	S_TWI1_SDA				S_PL_EINT9
PL10		I/O	S_PWM				S_PL_EINT10
PL11		I/O	S_CPU_CUR_W	S_CIR_IN			S_PL_EINT11

4.3. Detailed Pin/Signal Description

Table 4-3 shows the detailed function of every pin/signal based on the different interface.

Table 4-3.Detailed Pin Description

Pin/Signal Name	Description	Type
DRAM		
DDRZQ	SIP LPDDR4 ZQ Calibration	A
SZQ	DRAM Controller ZQ Calibration	A
ODT_CA_A	LPDDR4 Channel A CA ODT Control	I
ODT_CA_B	LPDDR4 Channel B CA ODT Control	I
VCC-DRAM	DRAM Power Supply	P
VDD18_DRAM	SDRAM controller power supply	P

Pin/Signal Name	Description	Type
System Control		
NMI	Non-maskable interrupt	OD
FEL	Boot select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process.	I
BOOT_SEL	Boot media select	I
JTAG_SEL	JTAG mode select The signal is used to select the port from which JTAG function outputs.	I
RESET	Reset signal (low active)	I/O
RTC		
X32KIN	Clock input of 32.768kHz crystal	AI
X32KOUT	Clock output of 32.768kHz crystal	AO
X32KFOUT	32.768kHz clock fanout Provides low frequency clock for external devices	OD
RTC_VIO	RTC low voltage (generated by internal LDO)	AO
VCC_RTC	RTC power	P
DCXO		
DXIN	Digital compensated crystal oscillator input	AI
DXOUT	Digital compensated crystal oscillator output	AO
REFCLK_OUT	Digital compensated crystal oscillator clock fanout	AO
DXLDO_OUT	Internal supply regulator output	AO
WREQIN	Request signal of REFCLK_OUT	AI
USB		
USB0_DM	USB DM signal	A I/O
USB0_DP	USB DP signal	A I/O
USB1_DM	USB DM signal	A I/O
USB1_DP	USB DP signal	A I/O
VCC_USB	USB analog power supply	P
VDD_USB	USB digital power supply	P
GPADC		
GPADC1	GPADC input channel1	AI
GPADC2	GPADC input channel2	AI
LRADC		
LRADC	LRADC input channel	AI
AUDIO CODEC		
LINEOUTL	LINE-OUT left channel output	AO
LINEOUTR	LINE-OUT right channel output	AO
MBIAS	Master analog microphone bias	AO
MICIN1N	Microphone negative input 1	AI
MICIN1P	Microphone positive input 1	AI
MICIN2N	Microphone negative input 2	AI
MICIN2P	Microphone positive input 2	AI

Pin/Signal Name	Description	Type
VRA1	Reference voltage	AO
VRA2	Reference voltage	AO
CPVEE	Charge pump negative voltage output	P
CPVIN	Analog power for LDO	P
CPVDD	Analog power for headphone charge pump	P
AVCC	Analog power	P
AGND	Analog ground	G
MIPI-CSIA		
MCSIA_D0N	MIPI CSI controller A data0 negative signal	AI
MCSIA_D0P	MIPI CSI controller A data0 positive signal	AI
MCSIA_D1N	MIPI CSI controller A data1 negative signal	AI
MCSIA_D1P	MIPI CSI controller A data1 positive signal	AI
MCSIA_D2N	MIPI CSI controller A data2 negative signal	AI
MCSIA_D2P	MIPI CSI controller A data2 positive signal	AI
MCSIA_D3N	MIPI CSI controller A data3negative signal	AI
MCSIA_D3P	MIPI CSI controller A data3 positive signal	AI
MCSIA_CKN	MIPI CSI controller A clock negative signal	AI
MCSIA_CKP	MIPI CSI controller A clock positive signal	AI
MCSIB_D0N	MIPI CSI controller B data0 negative signal	AI
MCSIB_D0P	MIPI CSI controller B data0 positive signal	AI
MCSIB_D1N	MIPI CSI controller B data1 negative signal	AI
MCSIB_D1P	MIPI CSI controller B data1 positive signal	AI
MCSIB_CKN	MIPI CSI controller B clock negative signal	AI
MCSIB_CKP	MIPI CSI controller B clock positive signal	AI
MIPI_MCLK0	MIPI CSI controller A master clock	O
MIPI_MCLK1	MIPI CSI controller B master clock	O
VCC_MCSI	MIPI CSI power supply	P
CSI_SM_VS	MIPI CSI slave mode vertical SYNC	O
LEDC		
LEDC	Intelligent control LED signal output	O
NAND Flash		
NAND_WE	NAND Flash write enable	O
NAND_ALE	NAND Flash address latch enable	O
NAND_CLE	NAND Flash command latch enable	O
NAND_CE[1:0]	NAND Flash chip select	O
NAND_RE	NAND Flash read enable	O
NAND_RB0	NAND Flash ready/busy status indicator signal	I
NAND_DQ[7:0]	NAND Flash data bit	I/O
NAND_DQS	NAND Flash data strobe	I/O
SMHC		
SDC0_D[3:0]	SDC0 data bit	I/O
SDC0_CLK	SDC0 clock	O

Pin/Signal Name	Description	Type
SDC0_CMD	SDC0 command signal	I/O, OD
SDC0_DET	SDC0 detect signal	I
SDC1_CLK	SDC1 clock	O
SDC1_CMD	SDC1 command signal	I/O, OD
SDC1_D[3:0]	SDC1 data bit	I/O
SDC2_D[7:0]	SDC2 data bit	I/O
SDC2_CLK	SDC2 clock	O
SDC2_CMD	SDC2 command signal	I/O, OD
SDC2_DS	SDC2 data strobe	I
SDC2_RST	SDC2 reset	O
LCD		
LCD1_D[23:0]	LCD data bit	O
LCD1_CLK	LCD clock signal	O
LCD1_DE	LCD data enable	O
LCD1_HSYNC	LCD horizontal sync	O
LCD1_VSYNC	LCD vertical sync	O
TCON_TRIG	TCON outputs to LCD fro sync	O
LVDS		
LVDS0_D[3:0]P	LVDS0 differential data positive signal	O
LVDS0_D[3:0]N	LVDS0 differential data negative signal	O
LVDS0_CKP	LVDS0 differential clock positive signal	O
LVDS0_CKN	LVDS0 differential clock negative signal	O
LVDS1_D[3:0]P	LVDS1 differential data positive signal	O
LVDS1_D[3:0]N	LVDS1 differential data negative signal	O
LVDS1_CKP	LVDS1 differential clock positive signal	O
LVDS1_CKN	LVDS1 differential clock negative signal	O
VCC_LVDS0	LVDS0/1 power	P
LVDS2_D[3:0]P	LVDS2 differential data positive signal	O
LVDS2_D[3:0]N	LVDS2 differential data negative signal	O
LVDS2_CKP	LVDS2 differential clock positive signal	O
LVDS2_CKN	LVDS2 differential clock negative signal	O
LVDS3_D[3:0]P	LVDS3 differential data positive signal	O
LVDS3_D[3:0]N	LVDS3 differential data negative signal	O
LVDS3_CKP	LVDS3 differential clock positive signal	O
LVDS3_CKN	LVDS3 differential clock negative signal	O
VCC_LVDS1	LVDS2/3 power	P
DSI		
DSI_DP0	DSI differential data0 positive signal	I/O
DSI_DM0	DSI differential data0 negative signal	I/O
DSI_DP1	DSI differential data1 positive signal	O
DSI_DM1	DSI differential data1 negative signal	O
DSI_CKP	DSI differential clock positive signal	O

Pin/Signal Name	Description	Type
DSI_CKM	DSI differential clock negative signal	O
DSI_DP2	DSI differential data2 positive signal	O
DSI_DM2	DSI differential data2 negative signal	O
DSI_DP3	DSI differential data3 positive signal	O
DSI_DM3	DSI differential data3negative signal	O
I2S/PCM		
I2S0_MCLK	I2S0 master clock	O
I2S0_LRCK	I2S0/PCM0 sample rate clock/sync	I/O
I2S0_BCLK	I2S0/PCM0 sample rate clock	I/O
I2S0_DOUT[1:0]	I2S0/PCM0 serial data output channel [1:0]	O
I2S0_DIN[1:0]	I2S0/PCM0 serial data input channel [1:0]	I
I2S2_MCLK	I2S2 master clock	O
I2S2_LRCK	I2S2/PCM2 sample rate clock/sync	I/O
I2S2_BCLK	I2S2/PCM2 sample rate clock	I/O
I2S2_DOUT0	I2S2/PCM2 serial data output channel 0	O
I2S2_DIN0	I2S2/PCM2 serial data input channel 0	I
I2S3_MCLK	I2S3 master clock	O
I2S3_LRCK	I2S3/PCM3 sample rate clock/sync	I/O
I2S3_BCLK	I2S3/PCM3 sample rate clock	I/O
I2S3_DOUT[3:0]	I2S3/PCM3 serial data output channel [3:0]	O
I2S3_DIN[3:0]	I2S3/PCM3 serial data input channel [3:0]	I
OWA		
OWA_OUT	One wire audio output	O
Interrupt		
PB_EINT[10:0]	GPIO B interrupt	I
PC_EINT[6:0] PC_EINT[16:8]	GPIO C interrupt	I
PD_EINT[9:0]	GPIO D interrupt	I
PE_EINT[7:0]	GPIO E interrupt	I
PF_EINT[6:0]	GPIO F interrupt	I
PG_EINT[9:0]	GPIO G interrupt	I
PH_EINT[7:0] PH_EINT[10:9] PH_ENIT[19:13]	GPIO H interrupt	I
PI_EINT[9:0]	GPIO I interrupt	I
PJ_EINT[27:0]	GPIO J interrupt	I
S_PL_EINT[11:0]	GPIO L interrupt	I
PWM		
PWM[10:1]	Pulse width modulation output channel [10:1] in CPUX	I/O
S_PWM	Pulse width modulation output channel in CPUS	I/O
CIR Receiver		

Pin/Signal Name	Description	Type
CIR_IN	Consumer infrared receiver in CPUX	I
S_CIR_IN	Consumer infrared receiver in CPUS	I
CIR_OUT	Consumer infrared transmitter	O
EMAC		
RGMII0_RXD3/RMII0_NULL	RGMII0 receive data3	I
RGMII0_RXD2/RMII0_NULL	RGMII0 receive data2	I
RGMII0_RXD1/RMII0_RXD1	RGMII0/RMII0 receive data1	I
RGMII0_RXD0/RMII0_RXD0	RGMII0/RMII0 receive data0	I
RGMII0_RXCK/RMII0_NULL	RGMII0 receive clock	I
RGMII0_RXCTL/RMII0_CRS_DV	RGMII0 receive control/ RMII0 carrier sense receive data valid	I
RGMII0_CLKIN/RMII0_RXER	RGMII0 transmit clock from external/ RMIII0 receiver error For RGMII0, IO type is output; For RMII0, IO type is input	I/O
RGMII0_TXD3/RMII0_NULL	RGMII0 transmit data3	O
RGMII0_TXD2/RMII0_NULL	RGMII0 transmit data2	O
RGMII0_TXD1/RMII0_TXD1	RGMII0/RMII0 transmit data1	O
RGMII0_TXD0/RMII0_TXD0	RGMII0/RMII0 transmit data0	O
RGMII0_TXCK/RMII0_TXCK	RGMII0/RMII0 transmit clock For RGMII0, IO type is output; For RMII0, IO type is input	I/O
RGMII0_TXCTL/RMII0_TXEN	RGMII0 transmit control/ RMII0 transmit enable	O
MDC0	RGMII0/RMII0 management data clock	O
MDIO0	RGMII0/RMII0 management data input/output	I/O
EPHY0_25	25MHz output for EMAC PHY	O
RGMII1_RXD3/RMII1_NULL	RGMII1 receive data3	I
RGMII1_RXD2/RMII1_NULL	RGMII1 receive data2	I
RGMII1_RXD1/RMII1_RXD1	RGMII1/RMII1 receive data1	I
RGMII1_RXD0/RMII1_RXD0	RGMII1/RMII1 receive data0	I
RGMII1_RXCK/RMII1_NULL	RGMII1 receive clock	I
RGMII1_RXCTL/RMII1_CRS_DV	RGMII1 receive control/ RMII0 carrier sense receive data valid	I
RGMII1_CLKIN/RMII1_RXER	RGMII1 transmit clock from external/ RMIII0 receiver error For RGMII0, IO type is output; For RMII0, IO type is input	I/O
RGMII1_TXD3/RMII1_NULL	RGMII1 transmit data3	O
RGMII1_TXD2/RMII1_NULL	RGMII1 transmit data2	O
RGMII1_TXD1/RMII1_TXD1	RGMII1/RMII1 transmit data1	O
RGMII1_TXD0/RMII1_TXD0	RGMII1/RMII1 transmit data0	O
RGMII1_TXCK/RMII1_TXCK	RGMII1/RMII1 transmit clock For RGMII0, IO type is output; For RMII0, IO type is input	I/O
RGMII1_TXCTL/RMII1_TXEN	RGMII1 transmit control/ RMII1 transmit enable	O

Pin/Signal Name	Description	Type
MDC1	RGMII1/RMII1 management data clock	O
MDIO1	RGMII1/RMII1 management data input/output	I/O
EPHY1_25	25MHz output for EMAC PHY	O
SPI		
SPI0_CS0	SPI0 chip select0 signal, low active	I/O
SPI0_CLK	SPI0 clock signal	I/O
SPI0_MOSI	SPI0 master data out, slave data in	I/O
SPI0_MISO	SPI0 master data in, slave data out	I/O
SPI0_WP	SPI0 write protect, low active	I/O
SPI0_HOLD	SPI0 hold signal	I/O
SPI1_CS	SPI1 chip select signal, low active	I/O
SPI1_CLK	SPI1 clock signal	I/O
SPI1_MOSI	SPI1 master data out, slave data in	I/O
SPI1_MISO	SPI1 master data in, slave data out	I/O
SPI2_CS	SPI2 chip select signal, low active	I/O
SPI2_CLK	SPI2 clock signal	I/O
SPI2_MOSI	SPI2 master data out, slave data in	I/O
SPI2_MISO	SPI2 master data in, slave data out	I/O
UART		
UART0_TX	UART0 data transmit	O
UART0_RX	UART0 data receive	I
UART1_TX	UART1 data transmit	O
UART1_RX	UART1 data receive	I
UART1_CTS	UART1 data clear to send	I
UART1_RTS	UART1 data request to send	O
UART2_TX	UART2 data transmit	O
UART2_RX	UART2 data receive	I
UART2_CTS	UART2 data clear to send	I
UART2_RTS	UART2 data request to send	O
UART3_TX	UART3 data transmit	O
UART3_RX	UART3 data receive	I
UART3_CTS	UART3 data clear to send	I
UART3_RTS	UART3 data request to send	O
UART4_TX	UART4data transmit	O
UART4_RX	UART4 data receive	I
UART5_TX	UART5 data transmit	O
UART5_RX	UART5 data receive	I
UART5_CTS	UART5 data clear to send	I
UART5_RTS	UART5 data request to send	O
UART6_TX	UART6 data transmit	O
UART6_RX	UART6 data receive	I
S_UART_TX	S_UART data transmit	O

Pin/Signal Name	Description	Type
S_UART_RX	S_UART data receive	I
TWI		
TWI0_SCK	TWI0 serial clock signal	I/O
TWI0_SDA	TWI0 serial data signal	I/O
TWI1_SCK	TWI1 serial clock signal	I/O
TWI1_SDA	TWI1 serial data signal	I/O
TWI2_SCK	TWI2 serial clock signal	I/O
TWI2_SDA	TWI2 serial data signal	I/O
TWI3_SCK	TWI3 serial clock signal	I/O
TWI3_SDA	TWI3 serial data signal	I/O
TWI4_SCK	TWI4 serial clock signal	I/O
TWI4_SDA	TWI4 serial data signal	I/O
TWI5_SCK	TWI5 serial clock signal	I/O
TWI5_SDA	TWI5 serial data signal	I/O
S_TWI0_SCK	S_TWI0 serial clock signal	I/O
S_TWI0_SDA	S_TWI0 serial data signal	I/O
S_TWI1_SCK	S_TWI1 serial clock signal	I/O
S_TWI1_SDA	S_TWI1 serial data signal	I/O
JTAG		
JTAG_MS	JTAG mode select	I
JTAG_CK	JTAG clock select	I
JTAG_DO	JTAG data output	O
JTAG_DI	JTAG data input	I
JTAG_MS_GPU	JTAG mode select	I
JTAG_CK_GPU	JTAG clock select	I
JTAG_DO_GPU	JTAG data output	O
JTAG_DO_GPU	JTAG data input	I
S_JTAG_MS	S_JTAG mode select	I
S_JTAG_CK	S_JTAG clock select	I
S_JTAG_DO	S_JTAG data output	O
S_JTAG_DI	S_JTAG data input	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Functional operation of the device at these or any other conditions beyond the absolute maximum ratings listed in Table 5-1 can cause permanent damage to the device.

Table 5-1.Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage Temperature	-40	125	°C
AVCC	Analog Part Power	-0.3	2.16	V
VCC_PC	Digital GPIO C Power	-0.3	3.96	V
VCC_PD	Digital GPIO D Power	-0.3	3.96	V
VCC_PE	Digital GPIO E Power	-0.3	3.96	V
VCC_PG	Digital GPIO G Power	-0.3	3.96	V
VCC_PJ	Digital GPIO J Power	-0.3	3.96	V
VCC_PL	Digital GPIO L Power	-0.3	3.96	V
VCC_IO	GPIO B, GPIO F, GPIO H, GPIO I and System Control Power	-0.3	3.96	V
VCC_LVDS0	LVDS0/1 Power	-0.3	2.16	V
VCC_LVDS1	LVDS2/3 Power	-0.3	2.16	V
VCC_USB	USB Analog Power	-0.3	3.96	V
VDD_USB	USB Digital Power	-0.3	1.08	V
VCC_MCSI	MIPI CSI Power	-0.3	2.16	V
VCC_RTC	RTC Power	-0.3	2.16	V
VCC_EFUSE	EFUSE Program Mode Power	-0.3	2.16	V
VDD_CPUS	CPUS Power	-0.3	1.3	V
VDD_CPU	CPU Power	-0.3	1.3	V
VCC_PLL	System PLL Power	-0.3	2.16	V
VDD_SYS	Power Supply for System	-0.3	1.3	V
VCC_DRAM	DRAM Power	-0.3	1.5	V
VDD18_DRAM	DRAM 1.8V internal PAD Power	-0.3	2.16	V

5.2. Recommended Operating Conditions

All AIC800G3 modules are used under the operating Conditions contained in Table 5-2.

Table 5-2.Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_a	Ambient Temperature	-20	-	85	°C
AVCC	Analog Part Power	1.764	1.8	1.836	V
VCC_PC	Digital GPIO C Power				
	1.8V Voltage	1.62	1.8	1.98	V
	3.3V Voltage	2.97	3.3	3.63	
VCC_PD	Digital GPIO D Power				
	1.8V Voltage	1.62	1.8	1.98	V
	3.3V Voltage	2.97	3.3	3.63	

VCC_PE	Digital GPIO E Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	 V
VCC_PG	Digital GPIO G Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	 V
VCC_PJ	Digital GPIO J Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	 V
VCC_PL	Digital GPIO L Power 1.8V Voltage 3.3V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	 V
VCC_IO	GPIO B, GPIO F, GPIO H, GPIO I and System Control Power	2.97	3.3	3.63	V
VCC_LVDS0	LVDS0/1 Power	1.75	1.8	1.98	V
VCC_LVDS1	LVDS2/3 Power	1.75	1.8	1.98	V
VCC_USB	USB Analog Power	2.97	3.3	3.63	V
VDD_USB	USB Digital Power	0.837	0.9	0.99	V
VCC_MCSI	MIPI CSI Power	1.62	1.8	1.98	V
VCC_RTC	RTC Power	1.62	1.8	1.98	V
VCC_EFUSE	EFUSE Program Mode Power	1.8	1.89	1.98	V
VDD_CPUS	CPUS Power	0.87	0.9	0.93	V
VDD_CPU	CPU Power	0.81	-	1.2	V
VCC_PLL	System PLL Power	1.62	1.8	1.98	V
VDD_SYS	Power Supply for System	0.9	-	1.0	V
VCC_DRAM	DRAM Power	1.06	1.1	1.17	V
VDD18_DRAM	DRAM 1.8V internal PAD Power	1.7	1.8	1.95	V

5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of AIC800G3.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7*VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3*VCC-IO	V
R_{PU}	Input Pull-up Resistance	80 3.76 12	100 4.7 15	120 5.64 18	KΩ
R_{PD}	Input Pull-down Resistance	80 3.76 12	100 4.7 15	120 5.64 18	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA

V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. Oscillator Electrical Characteristics

The AIC800G3 contains two oscillators:a 24MHz oscillator and a 32768Hz oscillator.Each oscillator requires a specific crystal.The AIC800G3 device operation requires the following two input clocks:
The 32.768kHz frequency is used for low frequency operation.
The 24.000MHz frequency is used to generate the main source clock of the AIC800G3 device.

Table 5-4. 24MHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range	-	24.000	-	MHz
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–

Table 5-5. 32.768kHz Oscillator Characteristics

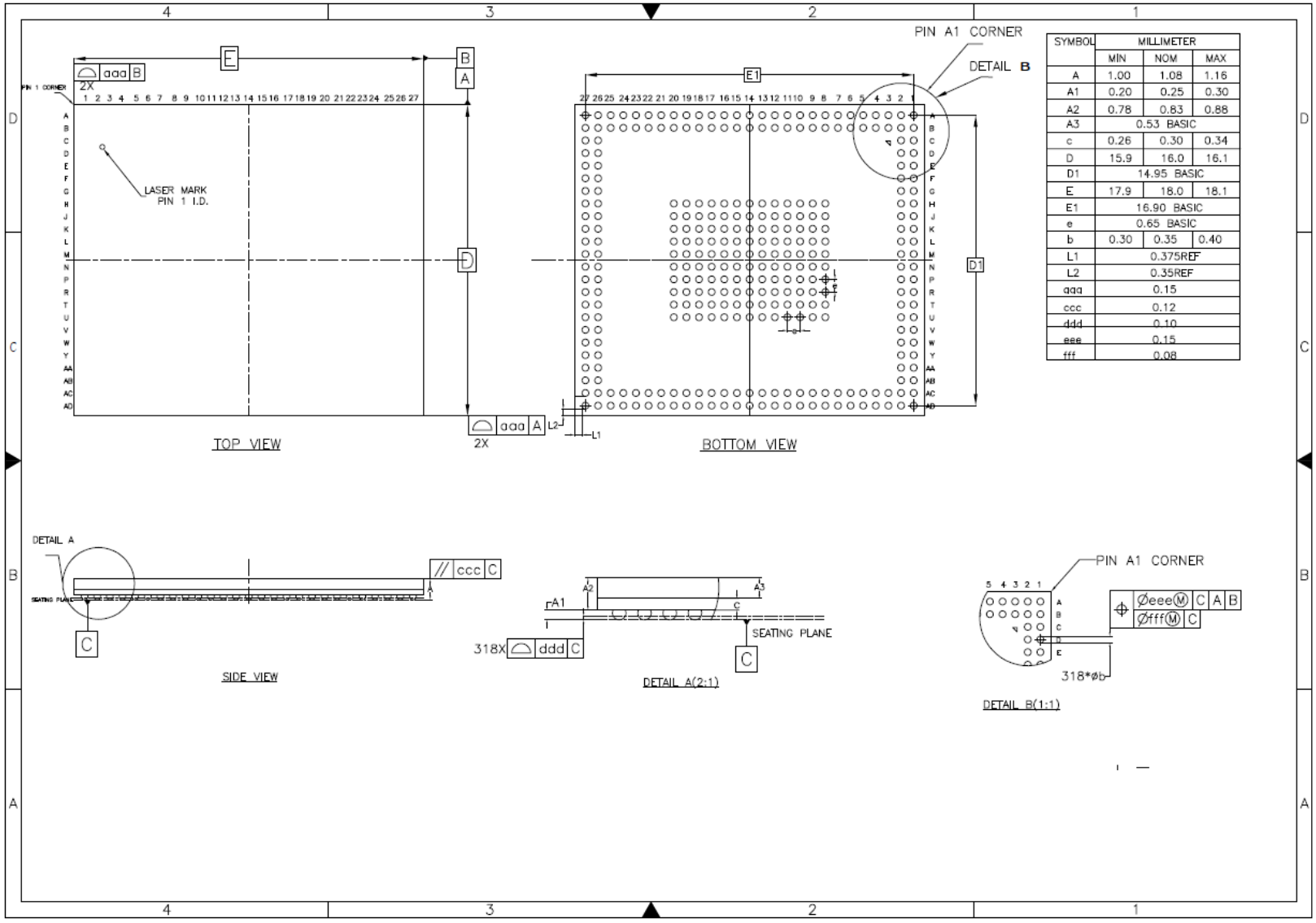
Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range	–	32768	–	Hz
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–

6. Pin Assignment

6.1. Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A	GND	X32K OUT	X32K FOUT	PI9	PI7	PI5	PI3	PI1	PB10	PB9	PB7	PB5	PB3	PB1	GND	PH4	PH6	PH1	PH3	PH10	PH15	PH17	PH19	PF4	PF2	PF0	GND
B	REFCLK _OUT	X32KIN	DXLDO_ OUT	PI8	PI6	PI4	PI2	PI0	GND	PB8	PB6	PB4	PB2	PB0	PH7	PH5	PH0	PH2	PH9	PH13	PH14	PH16	PH18	PF5	PF3	PF1	PF6
C	DXOUT	DXIN																								PJ25	PJ27
D	PG4	WREQIN																								PJ26	PJ7
E	PG5	PG0																								PJ6	PJ5
F	PG2	PG3																								PJ4	PJ3
G	PG6	PG1																								PJ2	PJ1
H	PG8	PG7						GND	GND	VDD _CPU	VDD _CPU	VDD _CPU	VDD _CPU	VDD _CPU	VDD _CPUFB	VDD _CPUS	VCC_PL	BOOT _SEL	GND	GND						PJ0	PJ15
J	PL11	PG9						GND	GND	GND	VDD _CPU	VDD _CPU	VDD _CPU	VDD _CPU	VDD _CPUFB	VCC _PLL	VCC_PG	JTAG _SEL	GND	GND						PJ14	PJ13
K	PL10	PL9						VCC _DRAM	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD _SYS						PJ12	PJ11
L	PL8	PL7						VCC _DRAM	VCC _DRAM	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD _SYS	VDD _SYS						PJ10	PJ9
M	PL6	PL5						VCC _DRAM	VCC _DRAM	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD _SYS	VDD _SYS						PJ8	PJ23
N	PL4	PL3						VCC _DRAM	VCC _DRAM	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD _SYS	VDD _SYS						PJ22	PJ21
P	PL2	PL1						VCC _DRAM	VCC _DRAM	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD _USB	VDD _SYS						PJ20	PJ19
R	PL0	RESET						VCC _DRAM	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD _SYSFB						PJ18	PJ17
T	NMI	RTC _VIO						VDD18 _DRAM	GND	GND	GND	VCC_PC	VCC_PE	VCC_IO	VCC_IO	VCC _LVDS1	VCC _MCSI	GND	GND	VDD _SYSFB						PJ16	PJ24
U	VCC _RTC	ODT _CA_A						GND	GND	GND	VCC_PD	VCC_PC	VCC _LVDS0	VCC_IO	VCC_IO	VCC_PJ	VCC _USB	VCC _EFUSE	GND	AGND						LRADC	FEL
V	SZQ	ODT _CA_B																								VRA1	VRA2
W	PD8	DDRZQ																								MICIN2N	MICIN2P
Y	PD4	PD9																								MICIN1N	MICIN1P
AA	PD6	PD5																								MBIAS	LINE OUTLP
AB	PD2	PD7																								AVCC	LINE OUTLN
AC	PD0	PD3	PC3	PC4	PC6	PC1	PC8	PC10	PC13	PC15	USB1 _DP	USB0 _DP	PE6	PE0	PE2	PE4	MCSIA _D3P	MCSIA _D1P	MCSIA _CKP	MCSIA _D0P	MCSIA _D2P	MCSIB _D0P	MCSIB _CKP	MCSIB _D1P	CPVDD	CPVIN	GPADC2
AD	GND	PD1	PC2	PC12	PC5	PC0	PC9	PC11	PC14	PC16	USB1 _DM	USB0 _DM	PE7	PE5	PE1	PE3	MCSIA _D3N	MCSIA _D1N	MCSIA _CKN	MCSIA _D0N	MCSIA _D2N	MCSIB _D0N	MCSIB _CKN	MCSIB _D1N	CPVEE	GPADC1	GND

6.2. Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.08	1.16
A1	0.20	0.25	0.30
A2	0.78	0.83	0.88
A3		0.53 BASIC	
c	0.26	0.30	0.34
D	15.9	16.0	16.1
D1		14.95 BASIC	
E	17.9	18.0	18.1
E1		16.90 BASIC	
e		0.65 BASIC	
b	0.30	0.35	0.40
L1		0.375REF	
L2		0.35REF	
aaa		0.15	
ccc		0.12	
ddd		0.10	
eee		0.15	
fff		0.08	